Large-Area Electronics HF RFID Reader Array for Object-Detecting Smart Surfaces

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***Abstract*—This letter presents a system that enables identification and localization of objects through an array of RFID-readers integrated into a thin sheet via large-area electronics, for lining everyday surfaces. We demonstrate a 5 × 5 active matrix of RFID readers based on thin-film transistor (TFT) LC oscillators, using in-house fabricated ZnO TFTs. The array is designed to read commercial ISO14443 13.56 MHz tags, employing a tag-talks-first protocol to maximize readout speed for high array frame rate. The spatial resolution is set by the reader coil dimensions, which are 3.7 cm × 3.7 cm, for a maximum of 730 pixels/m^2. Using a 2.4 cm × 2.4 cm tag the array achieves a vertical read range of 3 cm and lateral range of 1.6 cm at a readout speed of 5 ms per element (set by the commercial tag). Readout is accomplished by sensing the current via the shared V_{DD} line of the array, in order to reduce interfacing requirements as array size scales. After filtering and amplification, the demodulated data has an amplitude of > 350 mV and the maximum power consumed by the reader array is < 280 mW.**

***Index Terms*—Cross-coupled LC oscillators, large-area electronics (LAE), RFID reader array, smart homes, zinc oxide thin film transistors.**

I. Introduction

Identifying and localizing objects is a primary application driver for the Internet of Things. Such capability can be utilized in many ways, such as for merchandise security, warehouse management, and smart spaces. For example, with regards to smart spaces, detecting the position of objects on a table enhances machine-learning algorithms for perception of human activity, since object interactions are strong features of the activity being performed [1], [2]. Currently, the primary technology for object localization is vision-based sensing. This is limited by line-of-sight, requires extensive training data, and is computationally expensive. A more direct approach is to distribute sensors over a large area, embedding them in everyday surfaces, to locally detect objects, wherever they are placed. While the range of technology tradeoffs impacting such applications are still being investigated, in [3] it is shown that such an approach can significantly improve the learning efficiency and recognition accuracy for human-activity perception. A potential technology for "sensing" an object's identity is RFID, and the tight read range of 13.56 MHz HF RFID can provide effective localization. Fig. 1(a) illustrates an envisioned application, where a table lined with a thin, dense array of RFID readers unobtrusively detects tagged objects placed on its surface.

In this letter, we implement such a reader array using large-area electronics (LAE). With LAE, the entire array can be fabricated on a single glass or plastic sheet, eliminating the assembly challenge of wiring thousands of discrete RFID readers together when scaling to large and high-resolution sensing surfaces. To achieve this, we demonstrate an LAE array of RFID readers implemented with thin-film transistors (TFTs) which can read standard compliant (ISO14443) RFID tags. While previous work has demonstrated the use of LAE to create standard-compliant RFID tags [4], these can avoid the challenges of high-frequency operation by directly rectifying the RF signal. An LAE reader, on the other hand, must deliver power to the tags at 13.56 MHz with f_T/f_{MAX}-limited TFTs.

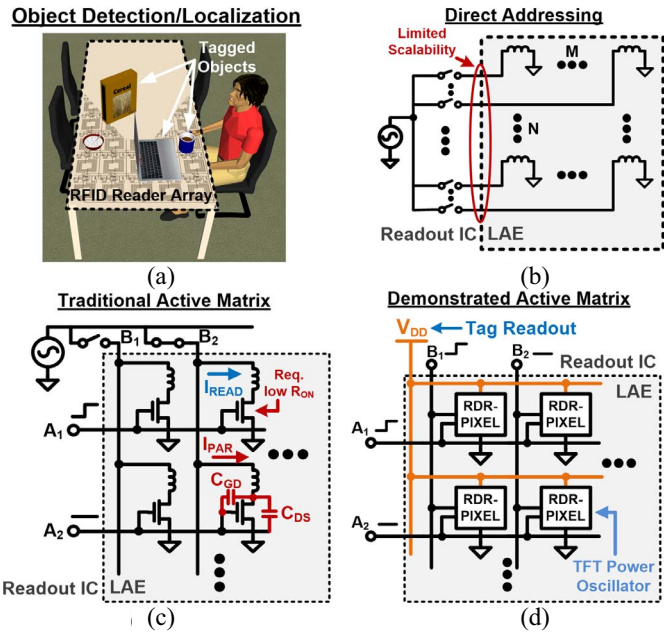

Fig. 1. System concept and architectures. (a) Concept of object-detection/localization. (b) RFID reader array using direct address scheme. (c) Array with TFT-switch-based active matrix control. (d) Proposed active matrix design, with oscillations produced locally by RDR-PIXELs.

II. System Architecture

The overall system architecture is based on the following rationale: 1) LAE should be used only for functions which are spatially distributed, while efficient CMOS ICs should be used for computation and system control that can be performed centrally; 2) the array should scale to large surface dimensions, notably implying the need to mitigate the number of physical connections between a large number of distributed reader elements and the centralized CMOS IC; and 3) readers should be individually addressable, operating without interfering with each other. For the first requirement, LAE is used to create an array of reader pixels (RDR-PIXELs), each of which consists of a planar coil antenna, and an IC is used for data demodulation and processing.

Fig. 1(b)–(d) considers various addressing schemes that can be employed to mitigate connections to the IC and enable interference-free readout from RDR-PIXELs. Direct addressing [Fig. 1(b)] delegates all addressing to a CMOS IC, with the advantage that it avoids TFTs in the high-frequency signal path. However, this requires a connection between the IC and the reader array for each RDR-PIXEL,

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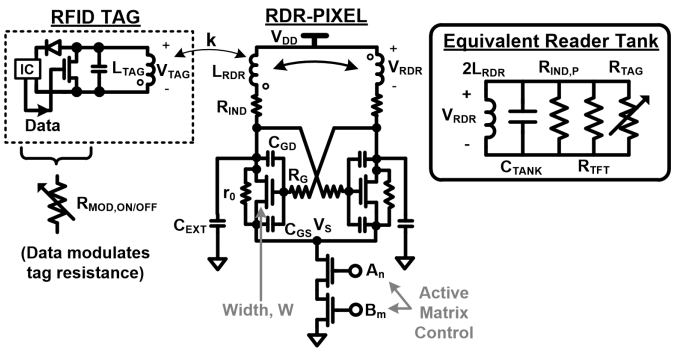

Fig. 2. RDR-PIXEL circuit and equivalent RLC-tank model used for design analysis.

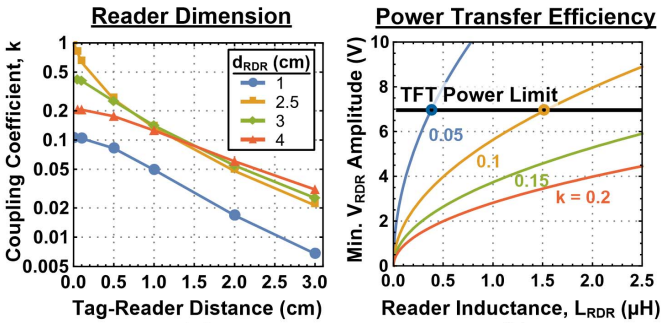

Fig. 3. (a) Coupling coefficient k versus distance, for different coil dimensions d_{RDR}. (b) RDR-PIXEL voltage requirement for tag powering. Plotted as a function of L_{RDR}, for various k.

limiting scalability. Alternatively, an active matrix can be employed [Fig. 1(c)]. Here, TFTs are used for addressing by switching the driver signal between the N rows (the IC can still be used for switching between the M columns with no additional LAE-IC connections). This reduces the number of LAE-IC connections from $N \times M$ to $N+M$. But now, TFT switches must provide low on-resistance R_{ON} and high off-impedance $1/(j\omega(C_{\mathrm{GD}}+C_{\mathrm{DS}}))$ at a high frequency, to avoid interference current I_{PAR} from unselected RDR-PIXELs. Thus, at 13.56 MHz, limited TFT f_T (35 MHz in this work) prevents robust readout. Instead, this work demonstrates the active matrix shown in Fig. 1(d), where each RDR-PIXEL is a TFT-based LC oscillator, generating the 13.56 MHz tag-powering signal locally. This reduces row/column selection to low-frequency control signals which enable a single RDR-PIXEL for tag readout via current demodulation on the shared V_{DD}. The LC oscillator design (described below) exploits the ability to create large planar inductors in LAE, having wide, low-resistance traces and thus high quality factors [5]. This resonates out TFT capacitances, enabling frequencies beyond f_T, instead limited by f_{MAX}, which is typically 2–3× higher for TFTs (100 MHz in this work). While active matrices reduce the connections, they require sequential readout of pixels. To maximize frame rate as array size scales, commercial ISO14443 tags employing a tag-talks-first protocol are used [6]; this decreases readout time from >100 ms to <5 ms, and reduces RDR-PIXEL requirements to tag powering, avoiding the need for tag control.

III. Circuit Design

Fig. 2 shows the RDR-PIXEL circuit (with coupled tag), consisting of a cross-coupled TFT LC oscillator with tail TFTs for row/column selection (via A_n/B_m signals) and external capacitors C_{EXT} for frequency tuning. For design analysis, an equivalent model of the reader tank is shown on the right. We analyze the system for the case where tag loading does not significantly affect the resonance of the reader tank, such that the reader can be designed to operate at a fixed resonant frequency. This corresponds to loose-coupling between tag and reader, which for the tags used in our demonstration is when the mutual-inductance coupling coefficient k is less than 0.2 [this corresponds to tag-reader distance >0.5 cm for the demonstrated inductor geometries, see Fig. 3(a)]. Under this assumption, the oscillation frequency is determined purely by reader inductance $2\times L_{\mathrm{RDR}}$ (factor of 2 from coupling between oscillator branches) and tank capacitance $C_{\mathrm{TANK}} = 4C_{\mathrm{GD}} + C_{\mathrm{GS}} + C_{\mathrm{EXT}}$, where C_{GD} and C_{GS} are the TFT gate-to-drain and gate-to-source capacitances, respectively. The loss associated with the tank, R_{TANK}, results from three parallel sources.

1) R_{TAG} due to tag powering

$$R_{\mathrm{TAG}} = 2\frac{V_{\mathrm{RDR}}^2}{V_{\mathrm{TAG}}^2}R_{\mathrm{MOD}} \tag{1}$$

in which V_{RDR} and V_{TAG} are the voltage across the reader and tag coils, respectively, and R_{MOD} is the resistance of the tag (which is modulated as the tag transmits data). A factor of 2 appears in (1), since tag powering is divided between the two oscillator branches.

2) R_{TFT} due to TFT output and gate resistances r_0 and R_G [5]

$$R_{\mathrm{TFT}} = r_0 || \frac{1}{\omega^2(C_{\mathrm{GS}}+2C_{\mathrm{GD}})^2 R_G} \tag{2}$$

where the series gate resistance has been transformed to a parallel equivalent resistance, introducing a dependence on frequency ω and TFT capacitances.

3) $R_{\mathrm{IND},P}$ due to parallel transformation of inductor series resistance R_{IND}

$$R_{\mathrm{IND},P} = \frac{\omega^2(2L_{\mathrm{RDR}})^2}{R_{\mathrm{IND}}}. \tag{3}$$

The design of the reader circuit primarily requires choosing L_{RDR} (value and geometry), the width of the oscillator TFTs (W), and V_{DD}. As we explain later, these affect the power consumption and read range, presenting a direct tradeoff between the two. The design must meet four requirements:

1) Oscillation frequency $f_{\mathrm{OSC}} = 13.56$ MHz;
2) Tag powering, specified as a minimum tag voltage, $V_{\mathrm{TAG,MIN}} = 6$ V at $R_{\mathrm{MOD,OFF}} = 1.5$ kΩ;
3) The Barkhausen oscillation criterion

$$g_m R_{\mathrm{TANK}} = g_m\left(R_{\mathrm{TAG}} \| R_{\mathrm{TFT}} \| R_{\mathrm{IND},P}\right) > 1 \tag{4}$$

4) Margin against TFT breakdown, represented by the maximum dc voltage across the TFT, V_{DD}-$V_S < 7$ V (described further in Section IV). Note that the amplitude of the ac voltage across the RDR inductor, V_{RDR}, is about equal to the dc voltage across the TFT.

First consider the geometry of the reader inductor, which we design as a square coil with dimension d_{RDR}. This dimension determines both the minimum reader inductance L_{RDR} (corresponding to half a loop) and how k varies with distance, as shown in Fig. 3(a). The relationships shown were calculated by simulating the magnetic field of a single square loop, to represent the reader coil dimension, through a fixed dimension loop for the tag ($d_{\mathrm{TAG}} = 2.5$ cm). As d_{RDR} increases, k drops off more slowly with tag-reader distance, potentially increasing read range, thereby presenting a tradeoff between array density and read range. However, as the coil dimension becomes much larger than the tag dimension, the maximum k decreases (since a large portion of the magnetic field will not couple to the 2.5 cm tag even when in physical contact). Eventually, even the maximum k becomes too small to power the tag within the design limits, as discussed below. For our technology, the max. d_{RDR} is thus ∼10 cm.

Once the reader-coil dimension is chosen for array density, the value of L_{RDR} can be varied through the number of coil loops. Accordingly, Fig. 3(b) shows the minimum voltage swing required

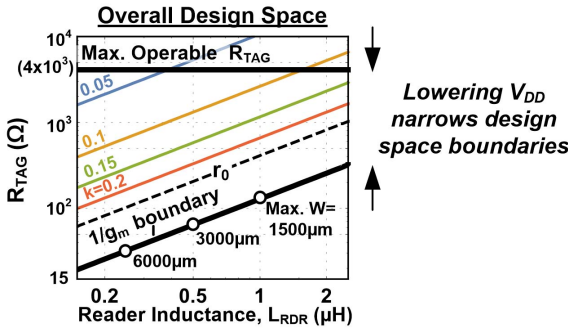

Fig. 4. Effective resistance seen by the reader R_{TAG} (colored lines) due to the tag load R_{MOD} as a function of L_{RDR}. RDR-PIXEL operation is limited to R_{TAG} falling within $1/gm$ and max R_{TAG} boundaries.

across the reader coil to sufficiently power the tag as a function of the reader inductance for various k, which at tag resonance is given by [7]

$$V_{RDR,MIN} = \frac{\sqrt{k^4 R_{MOD,OFF}^2 + \omega^2 L_{TAG}^2 (1-k^2)^2}}{kR_{MOD,OFF}} \sqrt{\frac{L_{RDR}}{L_{TAG}}} \times V_{TAG,MIN} \quad (5)$$

with $R_{MOD,OFF} = 1.5$ kΩ, $V_{TAG,MIN} = 6$ V, tag inductance $L_{TAG} = 2.77\mu$H, and frequency $\omega = 2\pi \times 13.56$ MHz, for the tag used in our system demonstration. As L_{RDR} is scaled down, V_{TAG}/V_{RDR} increases, enabling tag powering at lower V_{RDR} and thus lower V_{DD} (5). This reduces both the ac and dc power consumption in the reader. Alternatively, if V_{RDR} is kept fixed, scaling down L_{RDR} enables operation at lower k (i.e., greater distance) under the limit to the magnitude of V_{RDR} (7 V) imposed by TFT breakdown.

On the other hand, as V_{TAG}/V_{RDR} increases, the effective parallel resistance of the tag as seen by the reader, R_{TAG}, decreases. Fig. 4 shows R_{TAG}, as a function of reader inductance [from (1) and (5)], for various k. Lower R_{TAG} reduces oscillator tank resistance R_{TANK}, which can result in a failure to meet the oscillation criterion ($g_m R_{TANK} > 1$). This gets worse as k increases. Therefore, the oscillation criterion effectively limits the nearest read distance. However, since TFT width is limited by the tank capacitance for $f_{osc} = 13.56$ MHz, scaling down L_{RDR} enables a proportional increase in TFT width for increasing g_m. More specifically, the maximum width is

$$W_{MAX} = \frac{1}{\omega^2 2L_{RDR} C_{OX}(L_{ch} + 5X_{ov})} \quad (6)$$

where L_{ch} is TFT channel length X_{ov} is S/D-gate overlap, and C_{ox} is the gate oxide capacitance. Accordingly, Fig. 4 shows the $1/g_m$ boundary at the maximum TFT width for a given L_{RDR}, which must remain below R_{TAG}, to meet the oscillation criterion. As can be seen, $1/g_m$ and R_{TAG} scale at the same rate, such that the minimum read distance can be maintained as L_{RDR} is scaled down. However, larger TFT width results in greater dc current, resulting in higher power consumption, again highlighting the tradeoff between read-range and power consumption. We also represent in Fig. 4 the TFT breakdown limit as a maximum R_{TAG} (2 kΩ) given by $2R_{MOD,OFF} \times V_{RDR,MAX}^2/V_{TAG,MIN}^2$ [as per (1)]. This line represents the upper bound to R_{TAG} or, equivalently, the maximum read distance (through k), as shown previously in Fig. 3(b). Overall, the read-range is bounded by $1/g_m$ below and $R_{TAG,MAX}$ above, with the absolute maxima shown in Fig. 4.

Another major source of loss in the LC-oscillator is the TFT output resistance r_0. This is plotted in Fig. 4 (dashed line) for each value of maximum TFT width. This can be quite low for short-channel TFTs ($r_0 W = 600$ kΩ·µm in this work), introducing notable additional loss and further constraining the oscillation criterion. Furthermore, low r_0 (which dominates the ac losses from the reader) reduces the reader sensitivity to modulated tag data, which appears as a modulated resistance in parallel to r_0. Therefore, readout of the signal cannot be

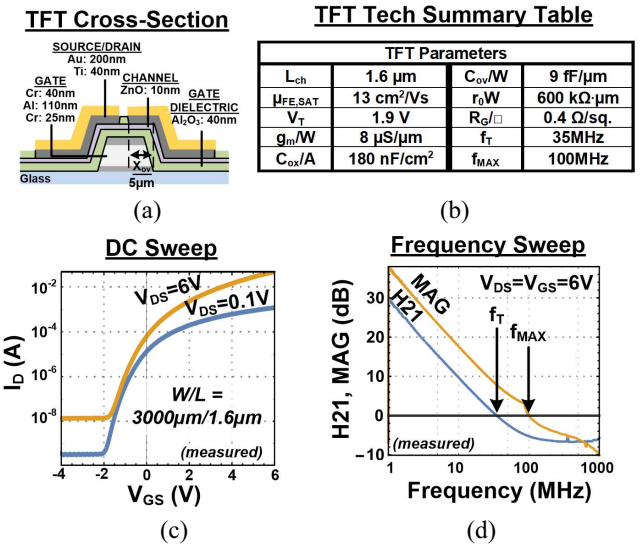

Fig. 5. Details of in-house fabricated n-channel ZnO TFTs (process temp. < 200 °C).

achieved for $R_{TAG} >> r_0$. Focusing primarily on maximizing read range and on values of k where R_{TAG} dominates, $W = 3000$ µm and $L_{RDR} = 300$ nH are chosen for our prototype, leaving room for $C_{EXT} \approx 80$ pF to robustly tune oscillator frequency to 13.56 MHz.

IV. TFT Design

For implementing the system, we use flex-compatible ZnO-channel TFTs (fabricated in house at process temp. < 200 °C), with field-effect mobility (13 cm²/V·s) comparable to state-of-the-art indium gallium zinc oxide (IGZO) TFTs in display manufacturing. The TFT cross section is shown in Fig. 5(a). Given the oscillation criterion requirement, g_m is maximized by using short channel length ($L_{ch} = 1.6$ µm). Gate resistance R_G is minimized by: 1) a tri-layer gate with thick aluminum sandwiched between chromium layers and 2) multifinger layout (finger width = 150 µm). To reduce capacitance, 5-µm S/D-G overlap (X_{OV}) is used (limited by mask alignment). The high-frequency performance of the TFTs is characterized in Fig. 5(d), where measured S-parameters are used to derive H21 and the maximum available gain (MAG). From the H21/MAG 0-dB crossing we find $f_T = 35$ MHz and $f_{MAX} = 100$ MHz at $V_{DS} = V_{GS} = 6$ V, where f_{MAX} is sufficient for power transfer at 13.56 MHz.

The TFT voltage limit mentioned in Section III arises from breakdown due to self-heating at high voltages/currents. From measurement, we find that the power limit is $P_{BD}/W = 0.25$ mW/µm. It should be noted that efforts to increase this power limit are unlikely to significantly improve the read-range, since the power transferred to the tag drops cubically with distance, presenting a power wall at distances on the order of the reader coil dimension.

TFT process variations can introduce nonuniformity in TFT capacitance (primarily from variation in C–V characteristics) across the array, leading to variation in the resonant frequency of the tank. Across a 3"×3" sample, we measure ±15% variation in capacitance at V_{DD}. For our design, this results in up to 0.7 MHz deviation from the desired 13.56 MHz resonant frequency. The contribution of TFT capacitance can be reduced by minimizing X_{OV} (such as through a self-alignment technique [8], [9]), reducing the impact of TFT variation.

V. System Demonstration

Fig. 6 shows the prototype, demonstrating a 5×5 RFID-reader array. The flex-compatible (process temp. < 200 °C) ZnO-TFTs for forming RDR-PIXELs are fabricated in-house on glass and then wire bonded to the RDR-inductor array PCB to ease prototyping. In actual

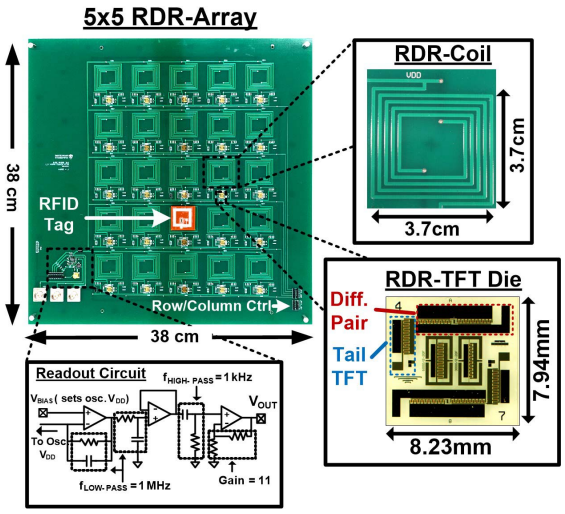

Fig. 6. Photos of prototype demonstration of 5×5 reader array and readout circuit schematic.

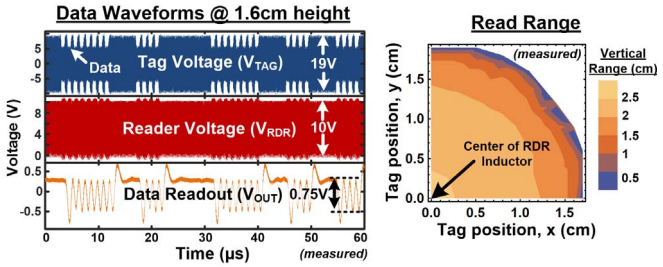

Fig. 7. Tag readout details. (a) Waveforms showing proper powering and readout of ISO14443-compliant tag. (b) Lateral and vertical read-range.

deployment, the reader TFTs and inductors would be fabricated on a single glass or plastic sheet. Data demodulation is performed by sensing the array V_{DD} current, via a readout-IC TIA, followed by gain and filtering around the 100 kb/s Manchester-encoded base-band data, using the op-amp stages shown ($f_{HIGH\text{-}PASS}$ = 1 kHz, $f_{LOW\text{-}PASS}$ = 1 MHz). RDR-PIXELs are powered at V_{DD} = 7 V (provided by the readout TIA) and selected using 8-V pulses on tail TFTs.

Fig. 7(a) shows measured waveforms (at read distance of 1.6 cm) for tag voltage V_{TAG}, reader voltage V_{RDR}, and demodulated data V_{OUT}, highlighting clear recovery of tag data (note, oscilloscope probe capacitance slightly affects tag and reader resonant frequency). The sensitivity and power consumption of the reader are analyzed in Fig. 8. Over the entire read-range, the amplitude of the demodulated output, V_{OUT}, remains above 350 mV, providing large SNR (clear eye observed but BER not characterized). The power consumption of the reader is plotted as a function of distance in Fig. 8(b). As distance increases, power consumption decreases, since less power is transferred to the tag, as expected. Above 3 cm, insufficient power is transferred to the tag such that it no longer transmits data. Therefore, tag powering rather than reader sensitivity limits the read distance. We note that readout was achieved even with the tag and reader coils in direct contact (strong-coupling regime), albeit at a shifted carrier frequency. We, thus, achieve a maximum vertical read range of 0–3 cm. The vertical read range as a function of the tag's lateral displacement from the reader-coil's center is shown in Fig. 7(b). Tag powering is achieved at a maximum of 1.6-cm lateral displacement. As shown in the summary table, the total reader-array power consumption is less than 280 mW (worst case for direct tag-reader contact). The tag read rate is 5 ms/tag, set by the ISO14443 tags [6], giving an overall array frame rate of 8 Hz.

As we consider scaling up the array, aside from frame rate, a key consideration is the loading of deactivated pixels on the readout

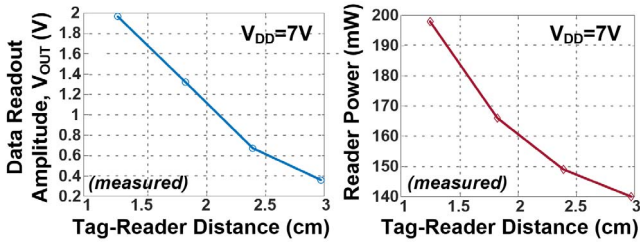

Fig. 8. (a) Amplitude of readout signal V_{OUT}, highlighting large readout signal over full read range. (b) Power consumption by reader and tag which increases as tag is brought closer to reader.

TABLE I
SYSTEM SUMMARY

Freq.	13.56MHz	**Tech.**	ZnO TFT
V_{DD}	7V	**Channel Length**	1.6µm
Tot. Power	<280mW	**W (diff. pair)**	3000µm
Read time/tag	5 ms	**W (tail)**	6000µm
Vertical read range	0-3cm	**L_{RDR}**	300nH
Lateral read range	0-1.6cm	**RDR Ind. Dim.**	3.7cm
C_{EXT}	78pF	**Tag Ind. Dim.**	2.4cm

TIA. The loading can be represented by a series inductor-capacitor ($L = (1/N) \times 150$ nH, $C = N \times 187$ pF for our design, where N is the total number of pixels), which becomes predominantly capacitive as the array scales. This can introduce TIA ringing and reduce stability [slight ringing observed in the readout in Fig. 7(a)]. This can be mitigated through TIA design, at the cost of power. For standard low-power commercially available op-amps > 1000 pixels are readily supported. Furthermore, the array can be divided into multiple subarrays through the use of multiple TIAs to allow for even further scaling. Finally, utilizing parallel subunits has the added advantage of reducing the total frame rate.

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