Reduction of p^+-n^+ Junction Tunneling Current for Base Current Improvement in Si/SiGe/Si Heterojunction Bipolar Transistors

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Abstract—**We report a three order of magnitude reduction in parasitic tunneling current at heavily doped p^+-n^+ Si/Si and SiGe/Si junctions grown by rapid thermal epitaxial chemical vapor deposition compared to previously reported results in Si junctions fabricated by ion implantation [1]. The results are very important for the reduction of base current in scaled bipolar transistors, especially for SiGe heterojunction bipolar transistors (HBT's), and also show the high quality of the epitaxial interface.**

I. Introduction

Several studies have shown that the forward current of heavily doped silicon junctions is dominated by a parasitic tunneling current [1]–[5]. This current is not band-to-band tunneling, but rather the tunneling of both electrons and holes to midgap states at the p-n interface. However, heavily doped layers are desired for good performance of bipolar junction transistors (BJT's) and heterojunction bipolar transistors (HBT's). Scaling of BJT's requires an increase in the base doping to avoid punchthrough, and heavily doped bases are also desired for low base resistance and high Early voltages. High emitter dopings are desired for high emitter efficiency and low series resistance. When the lightly doped side of the base-emitter junction exceeds a certain doping ($>10^{18}$ cm^{-3} according to [1]), the space-charge region narrows, and tunneling barrier becomes very small. This causes nonnegligible tunneling to the midgap states. This tunneling current becomes a significant component of the base current, especially at low forward biases.

In this paper a significant reduction of tunneling current is reported in epitaxial p^+-n^+ junctions grown by rapid thermal chemical vapor deposition (RTCVD) compared to the previous ion implantation results [1]. The implications of these results for HBT performance are also shown. Since Si/SiGe/Si HBT's generally contain high base dopings (e.g., 10^{19} cm^{-3} [6] or more), the tunneling base current component becomes especially important. This is illustrated in Fig. 1 where it is shown how the tunneling current is predicted to limit the current gain in a Si/Si$_{0.85}$Ge$_{0.15}$/Si HBT with a base doping $N_B = 5 \times 10^{19}$ cm^{-3} as the emitter doping is increased. Without the presence of tunneling the gain would follow the ideal curve shown in the figure. At high emitter doping levels, the ideal curve bends due to the bandgap narrowing in the heavily doped silicon emitter. With tunneling, the gain curves are predicted to drop rapidly after a certain doping is reached since tunneling causes a significant increase in the base current.

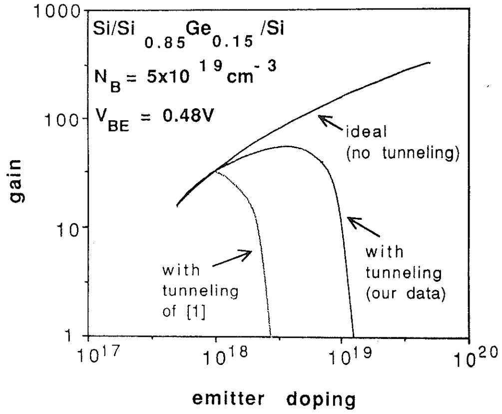

Fig. 1. Calculated effects of the tunneling current on the gain of Si/Si$_{0.85}$Ge$_{0.15}$/Si HBT's as the emitter doping is increased. Both curves based on the data of [1] and our data are given for comparison, as well as the ideal curve (no tunneling).

II. Experiments and Results

Epitaxial p^+-n^+ (i.e., like a base-emitter) Si/Si and Si$_{0.8}$Ge$_{0.2}$/Si diodes were fabricated by RTCVD. Thick silicon n^+ layers (3–13 × 10^{-4} cm) were grown on n-type substrates at high temperature (850–1000°C). The dopings ranged from 1×10^{17} to 1×10^{19} cm^{-3}. After the high-temperature step, the growth was stopped for 30 s and the temperature was lowered to 700°C to prevent outdiffusion and provide an abrupt junction. Thin epitaxial p^+ silicon layers (50 nm), doped 5×10^{19} cm^{-3}, were then grown at low temperature (700°C). On some of the samples, a thin p^+ (30 nm) Si$_{0.8}$Ge$_{0.2}$ strained epitaxial layer was grown at 625°C (doped 5×10^{19} cm^{-3}) between the n^+ and p^+ silicon layers. This provided a n^+-Si/p^+-SiGe junction. The dopings were confirmed by spreading resistance and *CV* measurements. The values calculated from zero-bias capacitances confirmed the dopings calculated from the slope of $1/C^2$ versus voltage. The junctions were isolated by a

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Manuscript received November 2, 1990; revised January 13, 1991. This work was supported by ONR under Contract N00014-90-J-1316 and by NSF under Grant ECS-86157227.

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IEEE Log Number 9143219.

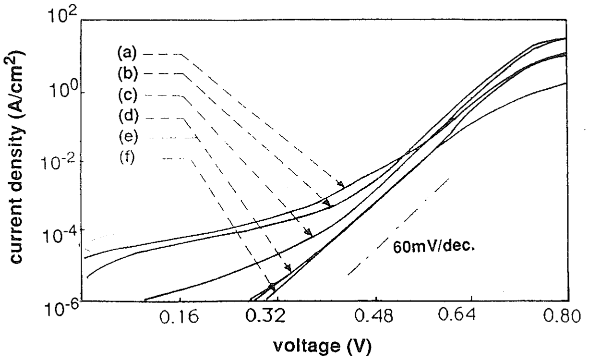

Fig. 2. Room-temperature forward-bias I-V characteristics of several Si/Si and Si/SiGe devices with the following n-type dopings: (*a*) 1×10^{19} cm^{-3} (Si/SiGe); (*b*) 9×10^{18} cm^{-3} (Si/Si); (*c*) 7×10^{18} cm^{-3} (Si/Si); (*d*) 3×10^{18} cm^{-3} (Si/Si); (*e*) 1.5×10^{18} cm^{-3} (Si/Si and Si/SiGe); and (*f*) 1.3×10^{17} cm^{-3} (Si/Si).

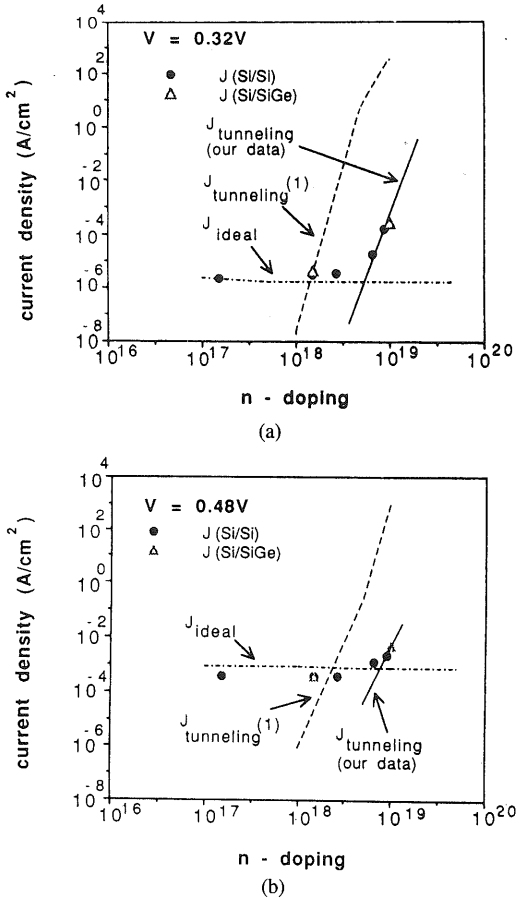

Fig. 3. Current density versus n-type doping for (a) $V = 0.32$ V, and (b) $V = 0.48$ V. J_{ideal} is the calculated ideal current density, $J_{\text{tunneling}}$[1] corresponds the tunneling data of [1], and $J_{\text{tunneling}}$(our data) is a fit to our data of tunneling current density.

simple mesa process. Room-temperature forward-bias I-V curves are shown in Fig. 2. The effect of the tunneling, referred to in the introduction, is clearly evident in the heavily doped devices at low current levels as the large $n > 2$ current (n represents the ideality factor of the diode). Since the hole and electron currents to the traps must be equal, the current is controlled by the lightly doped side of the junction, which has a larger tunneling barrier. Therefore the tunneling current increases as the doping on the lightly doped side is increased. It should be stressed that this is not the typical space-charge region recombination current ($1 < n < 2$), which should increase at low base dopings with larger space-charge regions, but is tunneling current which requires a small space-charge region (heavy doping) to reduce the tunneling barriers. I-V curves among the same area devices with the same doping were uniform, and measurements on the several different area devices (1.4×10^{-2} to 9.5×10^{-5} cm^2) confirmed that the peripheral current components were negligible. The flattening of the I-V curves at high voltages is due to the parasitic contact resistances, which varied from sample to sample, and is not important for this analysis. Significant tunneling was observed at doping levels of the order of 1×10^{19} cm^{-3} for both Si/Si and SiGe/Si devices. Simulations of band diagrams showed a slightly lower tunneling barrier (of the order of 100 meV) for electrons in the SiGe/Si devices compared to the Si/Si devices for similar n-doping densities (since the n-type side has a substantially larger tunneling barrier for electrons than that for holes on the p-side, the electron barrier will control the tunneling recombination rate). No significant difference in the behavior of Si/Si and SiGe/Si devices at the same doping levels was observed, however.

In Fig. 3, the current density is plotted as a function of doping at two different bias levels. Also plotted are calculated values of the ideal diode current, which should be the same in all devices since it is dominated by electron injection into the p$^+$ Si layer. Previous results for tunneling limits in ion-implanted p$^+$-n$^+$ junctions [1] are also shown for comparison to the tunneling current lines fit to our data. At high biases or low doping levels, ideal current dominates over tunneling in all devices, but at lower bias levels tunneling causes a several orders of magnitude increase in the junction current of heavily doped devices. That these high currents were indeed tunneling was confirmed with temperature-dependent measurements. Since the injected currents are vastly reduced at lower temperatures and the tunneling currents are fairly insensitive to temperature, the effect of tunneling is even more significant at low temperatures. Current–voltage characteristics were measured in the temperature range from 175 to 350 K. The concave shape of the current versus temperature curve (on a linear scale) of heavily doped devices (Fig. 4), as well as the linear shape of the current versus bandgap curve (on a logarithm-linear scale) were consistent with the expected shape of excess tunneling current curves [4], [5].

For the same n-type doping, the tunneling currents in our devices are approximately three orders of magnitude lower than those of the ion-implanted devices previously reported [1]. If the implanted junctions were somewhat compensated due to the nonabrupt implantation profiles, the actual junction doping would be less than indicated, making the RTCVD results even better in comparison. Since the tunneling current is mediated by midgap states at the junction, the vast reduction in tunneling currents of the devices fabricated by RTCVD implies a commensurate reduction of density of defects at the interface. This may be due to the absence of residual implant-related damage in the RTCVD junctions. We have no independent measurement of the midgap state densities at

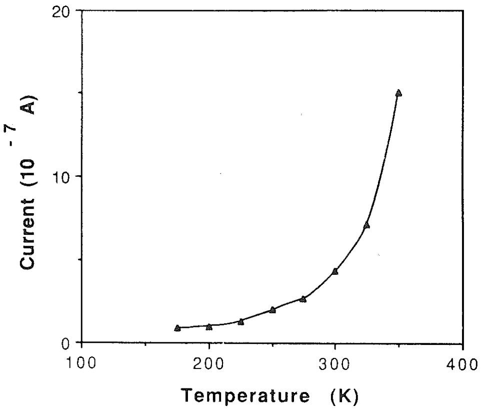

Fig. 4. Typical current versus temperature dependence of a heavily doped SiGe device ($N_D = 10^{19}$ cm^{-3}, $V = 0.32$ V, area = 3.25×10^{-4} cm^2).

the junction to confirm this hypothesis, however. Significant tunneling currents have also been observed in base–emitter junctions formed by the poly-Si emitter process [3], [4], but to the knowledge of the authors no data on tunneling current densities as a function of doping at the junction, like that of [1], have been reported.

The beneficial effect of the reduced tunneling current on heavily doped HBT properties can be seen in the simulations of Fig. 1, where the effects of the tunneling levels in our epitaxially grown junctions are contrasted to those previously reported. The reduction in parasitic tunneling current at the same doping level that we observed predicts a shift towards higher emitter doping and an increase in the peak gain. The low tunneling current enables high gain to be maintained to higher base doping levels, enabling reduced base resistances and increased Early voltages.

III. SUMMARY

Vastly reduced forward-bias tunneling current densities of RTCVD-fabricated Si/Si and Si/SiGe junctions compared to ion-implanted results [1] are reported. These results demonstrate the high quality of the epitaxial interface. Low tunneling currents allow higher limits to transistor base and emitter doping levels, which imply higher gains, reduced base resistances, and higher Early voltages of scaled bipolar devices as well as Si/SiGe/Si heterojunction bipolar transistors.

ACKNOWLEDGMENT

The assistance of S. A. Schwarz of Bellcore for SIMS is greatly appreciated.

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