Hole Confinement in MOS-Gated Ge_xSi_{1-x}/Si Heterostructures

P. M. Garone, V. Venkataraman, and J. C. Sturm, *Member, IEEE*

***Abstract*—In this paper the confinement of carriers in a MOS-gated Ge_xSi_{1-x} heterostructure is numerically modeled and experimentally confirmed. The structure uses a MOS gate to modulate the hole density at a buried Si/Ge_xSi_{1-x} interface. Numerical modeling is used to predict the maximum number of carriers achievable at the interface as a function of the structural design, and clear experimental evidence for such carrier confinement is given.**

I. Introduction

The performance of CMOS circuits is largely limited by the low transconductance of pMOS transistors. This transconductance could be improved by raising the hole mobility. One path to such mobility improvement may be to place a buried Ge_xSi_{1-x} layer under the gate of a pMOS transistor [1]. A "quantum" well for holes is then created [2], since the bandgap discontinuity is predominantly in the valence band. The band structure of such a device near flat band is shown in Fig. 1(*a*). The MOS-gated Ge_xSi_{1-x} heterostructures may be able to increase the hole mobility either by reduced surface scattering (by moving the hole inversion layer away from scattering sites at the Si–SiO_2 interface) or by mobility enhancement due to strain in the Ge_xSi_{1-x} well, as predicted in [3].

By applying a negative gate voltage, one can modulate the number of holes in the Ge_xSi_{1-x} well, eventually forming an inversion layer (Fig. 1(*b*)). As the gate voltage is increased further an inversion layer will also begin to form at the Si–SiO_2 interface, and eventually the dominant hole population will reside at the Si–SiO_2 interface for increasing negative biases (Fig. 1(*c*)). In this paper the number of holes in the well is modeled as a function of structure and gate bias. The hole confinement is then confirmed by capacitance–voltage and Hall measurements.

II. Numerical Model

A numerical model was developed which finds the one-dimensional electrostatic solution of Poisson's equation for a MOS-gated Ge_xSi_{1-x} capacitor at a given gate bias. After the gate voltage is input a trial surface potential is selected (thus setting the surface electric field) and the solution to

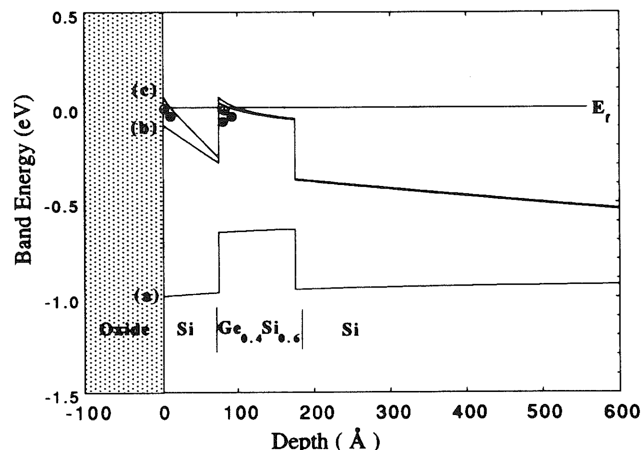

Fig. 1. Valence band of a MOS-gated Ge_xSi_{1-x} heterostructure. (*a*) No applied gate voltage. (*b*) V_{gate} = -1.9 V; Ge_xSi_{1-x} well is inverted. (*c*) V_{gate} = −4.0 V; Si–SiO_2 interface also inverted.

Poisson's equation is propagated using the fourth-order Runge–Kutta method. The surface potential is refined during successive iterations until convergence is reached when the potential in the bulk semiconductor goes to zero (within 0.2 mV). A constant quasi-Fermi level in the thin Si and Ge_xSi_{1-x} layers equal to that deep within the bulk was assumed (i.e., no channel–substrate bias). Fermi–Dirac statistics are used to obtain carrier concentrations, and information regarding the band offsets was taken from calculations by Van de Walle and Martin for commensurately strained Ge_xSi_{1-x} on silicon substrates [4]. The strain-induced splitting of the band degeneracies is included. The device structures for the simulations consist of a 100-Å gate oxide and a 100-Å Ge_xSi_{1-x} well that lies underneath a thin Si spacer layer. The background doping is 10^{16}-cm^3 n-type.

In Fig. 2 simulations of the hole density versus gate voltage for a device with a Si spacer layer thickness of 30 Å and $Ge_{0.2}Si_{0.8}$ well show that initially (after threshold) the holes are added predominantly to the Ge_xSi_{1-x} well, which has an effective gate capacitance (slope of the hole density versus V_g) given by the series combination of the oxide and the Si spacer layer capacitances. Eventually the rate of increase of holes at the Si–SiO_2 interface will equal the rate of increase of holes in the Ge_xSi_{1-x} well. Beyond this point the additional holes will be added predominantly to the inversion layer at the Si–SiO_2 interface instead of the Ge_xSi_{1-x} well, with the effective gate capacitance becoming that of the oxide. The slope change (change in the effective gate capacitance) causes a "kink" in the plot of the total hole density versus V_g and can be seen experimentally.

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The authors are with the Department of Electrical Engineering, Princeton University, Princeton, NJ 08544.

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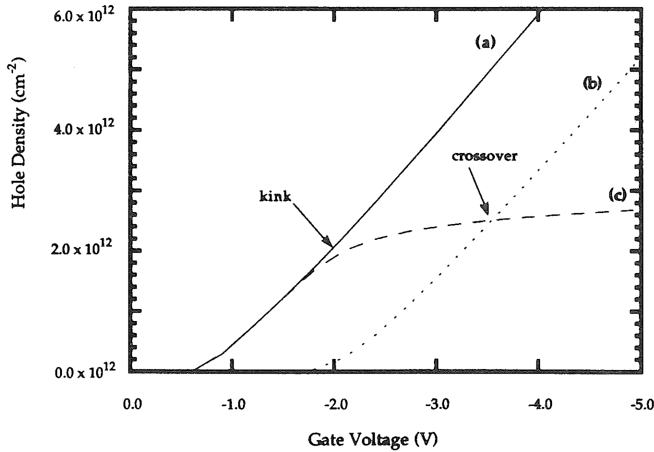

Fig. 2. Two-dimensional hole density versus gate voltage. V_{kink} marks the transition from carriers being predominantly added to the well to carriers being predominantly added to the $Si-SiO_2$ interface. Crossover marks the point where the number of holes at the $Si-SiO_2$ interface equals the number of holes in the Ge_xSi_{1-x} well. (*a*) Total hole density. (*b*) Hole density at Si/SiO_2 interface. (*c*) Hole density in Ge_xSi_{1-x} well.

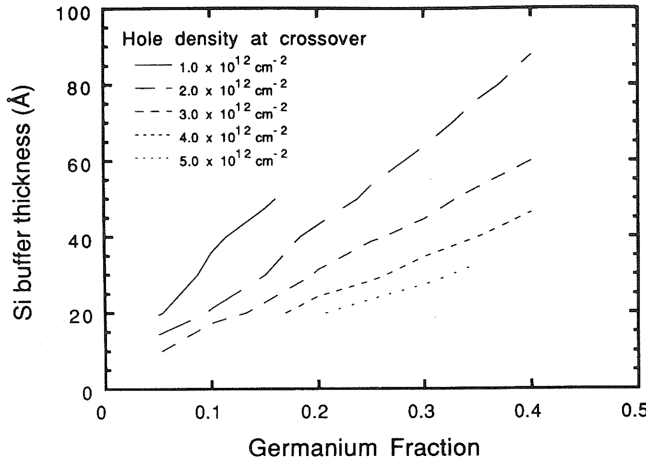

Fig. 3. Contour curves for the crossover points of MOS-gated heterostructures, with varying Ge fractions and Si spacer thicknesses.

Another important point on these curves is the point at which the number of holes in the Ge_xSi_{1-x} well equals the number of holes at the $Si-SiO_2$ interface. We will refer to this as the crossover point. One key to optimizing the structure is to have this crossover point occur at the highest possible hole density, maximizing the number of carriers in the well, where one hopes to have a higher mobility. A contour plot of the crossover point for a series of device structures with varying Ge fractions and Si spacer thicknesses is shown in Fig. 3. It is clear from this plot that it is desirable to minimize the Si spacer thickness and increase the Ge fraction to obtain the maximum number of holes at the crossover point.

One can obtain low-frequency capacitance–voltage curves (shown in Fig. 4) by taking the derivative of the total charge versus gate voltage. The plateau below C_{ox} in the inversion region corresponds to the buildup of holes in the Ge_xSi_{1-x} well. The transition from the plateau to C_{ox} represents the change in the effective gate capacitance seen at the kink in the total holes versus gate voltage plots. This low-frequency *CV* plateau is a second piece of experimental evidence which

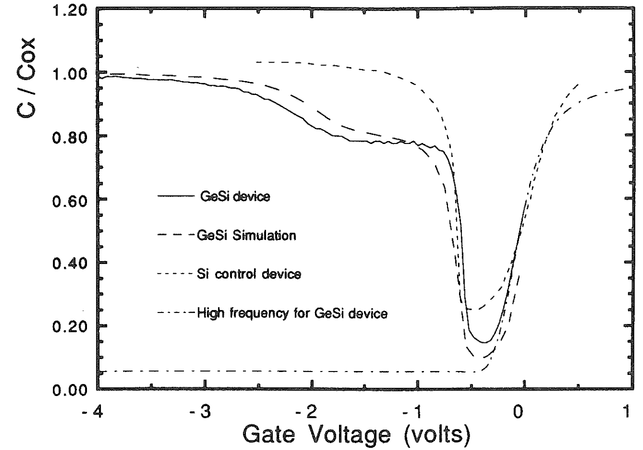

Fig. 4. Low- and high-frequency capacitance–voltage data and low-frequency simulation for a $Ge_{0.4}Si_{0.6}$ device with a 75-Å Si spacer layer and 100-Å gate oxide. Also shown for comparison is low-frequency data for an all-Si control device.

would indicate that inversion is actually occurring in the Ge_xSi_{1-x} well.

III. Experimental Results

Device structures were epitaxially grown on Si(100) n-type substrates in a reactor that uses a combination of rapid thermal processing and chemical vapor deposition. The wafer temperature was stabilized prior to introduction of the deposition gases and continuously controlled using an infrared transmission technique [5]. The Ge_xSi_{1-x} layers were grown at 600°C with dichlorosilane (Si source) and germane (Ge source) and the Si spacer layer was grown at 700°C. Source/drain implants were done for the Hall devices with two boron (B^+) implants, one at 50 keV and a dose of 1×10^{15} cm^{-2} and one at 25 keV and a dose of 1×10^{15} cm^{-2}. The gate oxides were plasma deposited at 350°C/30 s ($t_{ox} \approx 100$ Å) and then annealed at 700°C for 30 min in N_2. (This also served as our implant anneal.) The gate metal is evaporated aluminum.

The high-frequency curves for a structure with a 100-Å $Ge_{0.4}Si_{0.6}$ well and a 75-Å Si spacer were well-behaved (Fig. 4) and confirmed the gate oxide thickness of 100 Å. Low-frequency measurements, made by the quasi-static method, clearly show the plateau in the inversion region below C_{ox}, which indicates that holes are being added to the Ge_xSi_{1-x} well. The plateau is at a value of 255 nF/cm^2, which corresponds well with the estimated (from growth data) thickness of the Si spacer and our simulations of the structure. The transition from carriers being added to the Ge_xSi_{1-x} well to holes being added to the $Si-SiO_2$ interface occurs at a hole density of $\approx 2 \times 10^{12}$ cm^{-2}, which also agrees with simulations. By contrast, an all-Si control device displays no such plateau. (Note that the all-Si device curve was offset by 0.3 V since the threshold was more negative due to a higher doping level.)

Further confirmation of the confinement was made using a MOS-gated Hall device to obtain the hole density versus gate voltage. These measurements were done at 100 K with a ramped magnetic field to reduce noise and remove Hall voltage offsets caused by geometric nonuniformities. Fig. 5

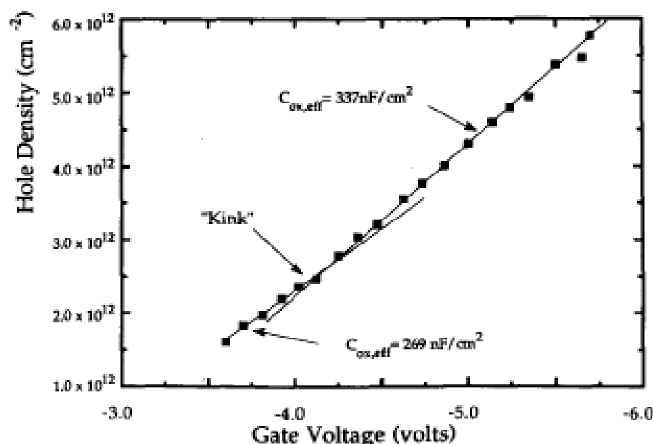

Fig. 5. Experimental two-dimensional hole density versus gate voltage for a MOS-gated Ge_xSi_{1-x} Hall device with a 100-Å gate oxide, a 75-Å Si spacer, and a 100-Å $Ge_{0.4}Si_{0.6}$ well. Note the "kink" at ≈ −4.1 V which marks the transition from carriers being added predominantly to the $Ge_{0.4}Si_{0.6}$ well to carriers being added predominantly to the $Si-SiO_2$ interface.

shows the hole density versus gate voltage for a device with a 100-Å $Ge_{0.4}Si_{0.6}$ well and a 75-Å (nominal) Si spacer. Note that the kink in the curve indicates a change in the effective gate capacitance. At low gate voltages (below −4.2 V) the effective gate capacitance is 269 nF/cm^2, indicating that the holes are being added to the Ge_xSi_{1-x} well. Above a gate voltage of −4.2 V the slope of the curve indicates that the holes are now being added at the $Si-SiO_2$ interface ($C_{ox\,eff}$ = 337 nF/cm^2).

IV. Summary

Numerical modeling and experiment show that it is possible to confine holes in a MOS-gated Ge_xSi_{1-x}/Si heterostructure device. This is confirmed by a change in the slope of the carrier concentration versus gate voltage curve and a plateau in the inversion region of the low-frequency *CV* curve. Also, simulations have shown that it is desirable to employ a minimal Si buffer thickness and a maximum Ge fraction to maximize the number of holes confined in the Ge_xSi_{1-x} well. In practice, however, the germanium fraction will be limited to avoid releasing strain in the Ge_xSi_{1-x} layer and a minimum Si spacer thickness may be required to separate holes from the $Si-SiO_2$ scattering sites.

References

[1] D. Nayak, J. C. S. Woo, J. S. Park, K. L. Wang, and K. P. Macwilliams, "Modulation doped p-channel Ge_xSi_{1-x} MOSFET," presented at the 1990 Device Research Conf., Santa Barbara, CA.

[2] S. S. Iyer *et al.*, "Si/SiGe metal oxide semiconductor devices," presented at the 1990 Device Research Conf., Santa Barbara, CA.

[3] J. M. Hinckley, V. Sankaran, and J. Singh, "Charged carrier transport in $Si_{1-x}Ge_x$ pseudomorphic alloys matched to Si- strain-related transport improvements," *Appl. Phys. Lett.*, vol. 55, no. 19, p. 2008, 1989.

[4] C. G. Van de Walle and R. H. Martin, "Theoretical calculations of heterojunction discontinuities in the Si/Ge system," *Phys. Rev. B.*, vol. 15, p. 5621, 1986.

[5] J. C. Sturm, P. V. Schwartz, and P. M. Garone, "Silicon temperature measurement by infrared transmission for rapid thermal processing applications," *Appl. Phys. Lett.*, vol. 56, no. 10, p. 961, 1989.