

## 61.3: Amorphous Silicon TFT Technology for Rollable OLED Displays

**Sigurd Wagner, Lin Han, Bahman Hekmatshoar, Katherine Song, Prashant Mandlik, Kunigunde H. Cherenack, and James C. Sturm**

Department of Electrical Engineering and Princeton Institute for the Science and Technology of Materials  
Princeton University, Princeton, New Jersey 08544, USA

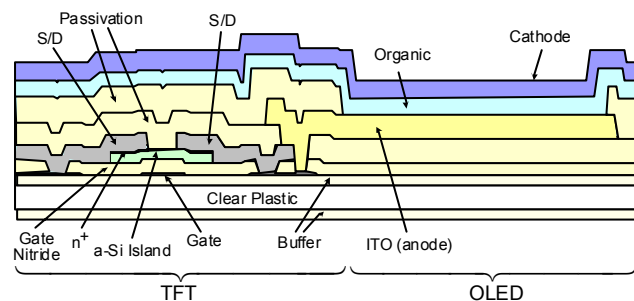
### Abstract

*Amorphous silicon thin-film transistors were designed for roll-out OLED screens in hand-held devices. Separate TFTs reached a saturation current of 6  $\mu\text{A}/\text{square}$ , an output current half-life extrapolating to 1,000 years, and were rolled to 1 mm diameter. All three parameters set new world records.*

### Introduction

Among the most attractive goals for new displays are wide-format roll-out screens for handheld devices. Such screens will have to produce attractive color images at video rates, have low power consumption, be light and sufficiently thin, flexible, and resilient for 1 million winding and unwinding operations from a thin spindle. Because organic light-emitting diodes (OLEDs) can meet most of these criteria, they are considered the frontplane technology of choice for roll-out-displays. OLEDs require drive current levels and stability that has been thought to require polycrystalline TFTs for the active-matrix backplane, instead of the conventional amorphous-silicon thin-film transistors (a-Si:H TFTs). However, because a-Si:H TFTs are the standard backplane technology, with a large industrial base and experience, their upgrading to roll-out AM-OLEDs is highly desirable. Therefore we have been conducting a coordinated program of bringing a-Si:H TFTs to roll-out OLED display readiness. We have reached record drive currents, current stability, and mechanical flexibility. All of these parameters have attained or surpassed the values required for AM-OLEDs.

To distinguish between conventional a-Si:H TFTs that use silicon nitride,  $\text{SiN}_x$ , as the gate dielectric, and the new a-Si:H TFTs with a new gate dielectric, we call the former “ $\text{SiN}_x$  TFT” and the latter “hybrid TFT.”



**Figure 1. Schematic cross section of a bottom-emitting OLED driven by an a-Si:H TFT, integrated on a clear plastic substrate. From ref. 1.**

### Backplane Performance Required for Roll-out OLED Screens

Assume a hand-held device that is 7 mm thick. It can hold a spindle of 3 mm diameter, on which a 100- $\mu\text{m}$  thick screen is wound to a maximum diameter of 5 mm. This screen can be

pulled to a length of 240 mm. If the device is 100 mm tall, such a screen can display the super-wide format of 2.4 to 1. The TFTs and OLEDs for this screen must meet a number of mechanical and opto-electronic requirements. The most important mechanical requirements are sufficient flexibility and layer adhesion, in other words, mechanical stability. Among the important opto-electronic requirements are TFT performance, and electrical stability.

### Mechanical Strain Produced by Rolling

The TFTs (and OLEDs) will be a few micrometers thick and will lie in the neutral surface of the screen where, theoretically, they experience no bending strain, whether rolled up or pulled out. But to make a conservative estimate of the bending strain that the devices might experience we assume that they lie on the surface of a 50- $\mu\text{m}$  thick substrate, i.e., 25- $\mu\text{m}$  away from the neutral surface, as they might prior to encapsulation. The assumed structure corresponds to that of one of our experimental samples, an un-encapsulated a-Si:H TFT-driven bottom emitting OLED integrated on a clear plastic substrate. Its schematic cross section is shown in Fig. 1. Bending such a structure on the surface of a 50- $\mu\text{m}$  thick substrate to a diameter of 3 mm produces a tensile strain in the display's surface of  $\sim 1.7\%$ . We describe results from a new a-Si:H TFT made with a hybrid gate dielectric and on a plastic substrate that exceed this requirement.

### OLED Drive Current

The TFT must source a large current that is stable. A high-quality green phosphorescent OLED with a pixel size of 100 $\mu\text{m}$  $\times$ 100 $\mu\text{m}$  needs 200 nA (2 mA/cm<sup>2</sup>) to produce a luminance of 1,000 cd/m<sup>2</sup>. A conventional a-Si:H driver TFT with a channel width-to-length ratio W/L of  $\sim 1$  and a threshold voltage  $V_T$  of  $\sim 2.5\text{V}$ , a gate voltage  $V_g$  of only  $\sim 7.5\text{V}$  ( $2.5 \times 10^5\text{V}/\text{cm}$  on a 300nm-thick gate nitride) is sufficient to drive the pixel [1]. This low  $V_g$  enables the low power operation that is essential for portable devices. We describe an a-Si:H TFT with the new hybrid gate dielectric. The TFT has a record electron field-effect mobility  $\mu_n$  [3] that, together with a doubling of the specific gate capacitance, quadruples the current a-Si:H TFTs can source in saturation. This new TFT will enable driving OLEDs at even lower  $V_g$ .

### TFT Stability

Over the display's operating life the TFT output current must be stable within  $\sim 10\%$  to ensure a stable RGB color balance, and within 50% to keep the display bright. A new angle to TFT operation at low gate bias voltage  $V_g$  is that the long-term TFT stability under continuous low gate bias is not known well. The reason is that the TFT switch for the AM-LCD pixel has been requiring substantially higher gate voltages, and its duty time is much shorter, than the TFT that drives the OLED [2]. We have conducted a comprehensive program on evaluating and raising the stability of conventional  $\text{SiN}_x$  TFTs. Its result is a  $\text{SiN}_x$  TFT process that raises the extrapolated time-to-half current to 1,000 years, as derived from gate-bias stress tests.

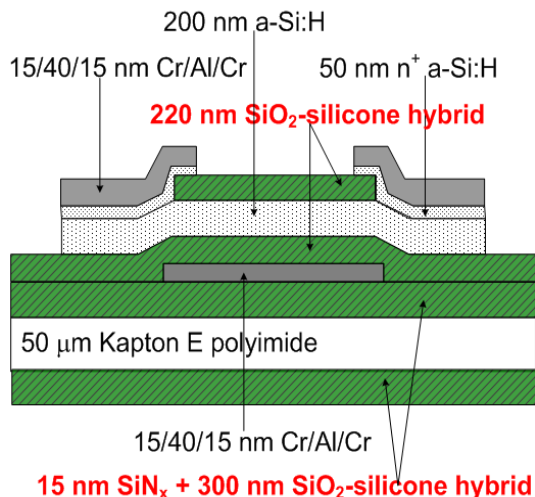
## Experiments and Results

Drawing from our experience with the fabrication and evaluation of flexible  $\text{SiN}_x$  TFTs on polymer and metal foil substrates, we identified several directions along which a-Si:H TFT performance can be improved. These are (i) enhancing flexibility by modifying or substituting several of the TFT layer materials, (ii) (iii) raising the TFT output current by replacing the  $\text{SiN}_x$  gate dielectric with the new hybrid, and (iii) raising the stability of the a-Si:H channel layer and the  $\text{SiN}_x$  gate dielectric for extended operating life. Because several of these advances are enabled by the introduction of a new  $\text{SiO}_2$ -silicone hybrid material, we briefly describe its initial application as a single-layer flexible permeation barrier for OLEDs.

This single-phase hybrid material combines the hermeticity of  $\text{SiO}_2$  with sufficient toughness like that of a silicone polymer, such that it appears not to form microcrack permeation paths. These microcracks are held responsible for the permeability of thin layers of the standard permeation barrier materials,  $\text{Al}_2\text{O}_3$ ,  $\text{SiO}_2$ , and  $\text{SiN}_x$ , which for this use require mechanical isolation by interposed organic polymer layers. In contrast, the hybrid material forms a single-layer ultra-hermetic barrier layer on OLEDs. The barrier is deposited directly on OLEDs by plasma-enhanced chemical vapor deposition (PE-CVD) from hexamethyl disiloxane and oxygen. In accelerated storage tests at  $65^\circ\text{C}$  and 85% relative humidity, half-lives of OLEDs coated with this barrier have exceeded a year [4]. We expect that this hybrid material will contribute to roll-out OLED screens as a flexible environmental barrier.

### Making a-Si:H TFTs Ultra-flexible

The standard test of flexibility of a-Si:H TFTs on a flexible substrate such as polymer or steel foil is to bend the structures around decreasing radii and evaluate the electrical characteristics of the re-flattened TFT. The TFT is taken to have exceeded its critical strain  $\epsilon_{\text{crit}}$  when it has failed electrically. Electrical failure is observed to be associated with tensile cracking after outward



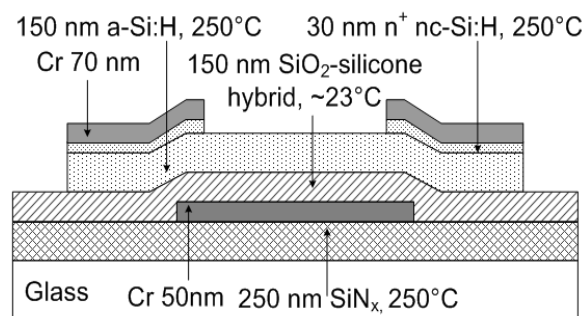
**Figure 2. Schematic cross section of a hybrid a-Si:H TFT on a polyimide foil substrate. All four  $\text{SiN}_x$  buffer and gate layers have been replaced with a new, resilient, hybrid dielectric material that is highly resistant to cracking. Redrawn from ref. 5.**

bending, or buckling coupled with delamination after inward bending. Such tests are very conservative, because the TFT/OLED circuits of a roll-out-screen will be placed in the neutral plane of the roll-out display, where nominally they do not experience any strain.

The  $\epsilon_{\text{crit}}$  of  $\text{SiN}_x$  TFTs is  $\sim 0.5\%$  in tension and  $\sim 2\%$  in compression. Therefore  $\text{SiN}_x$  TFTs already meet the requirement stated in section 2.1. To raise  $\epsilon_{\text{crit}}$  in tension we replaced all four  $\text{SiN}_x$  layers, colored green in Figure 2: two passivation layers for the polyimide substrate (except for 15-nm thick  $\text{SiN}_x$  adhesion layers), the gate dielectric layer, and the backchannel passivation layer. In addition, we replaced our standard gate and source/drain metal, chromium, with a tri-layer composite of ductile aluminum sandwiched between very thin Cr. These hybrid TFTs survived bending to compressive strains of up to  $\sim -2\%$  and to tensile strains of up to  $\sim 5\%$ , which in the particular configuration of Fig. 2 correspond to bending diameters of 2.5 mm and 1 mm, respectively [5]. The 1 mm bending diameter is a new record.

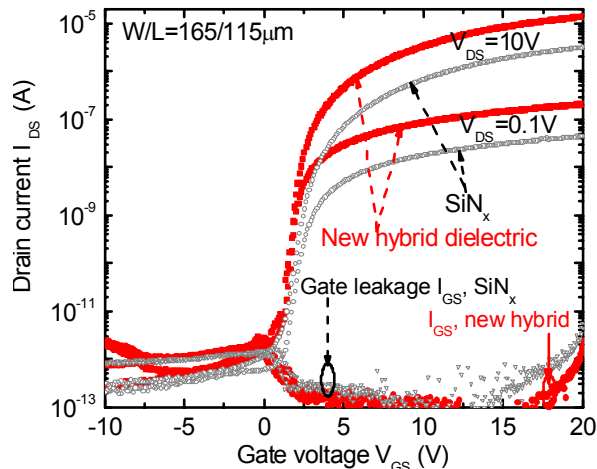
### a-Si:H TFTs With High Output Current

The  $\text{SiO}_2$ -silicone hybrid material enables record-high field-effect mobilities. Fig. 3 shows the cross section of a hybrid TFT that is made as similar as possible to conventional  $\text{SiN}_x$  TFTs on glass substrates, with the exception of the gate dielectric. Like a- $\text{SiN}_x$ , the hybrid dielectric is deposited by plasma-enhanced chemical vapor deposition [6]. The source gases are hexamethyl disiloxane (HMDSO) and oxygen. By varying the HMDSO/ $\text{O}_2$  ratio the properties of the hybrid can be varied over a wide range. We usually employ material with electrical properties close to that of thermal  $\text{SiO}_2$ . When made for gate dielectric application its dielectric breakdown strength is  $\sim 8$  MV/cm, and its relative dielectric constant is 4.0. However, the material is resilient, not brittle like thermal  $\text{SiO}_2$ .

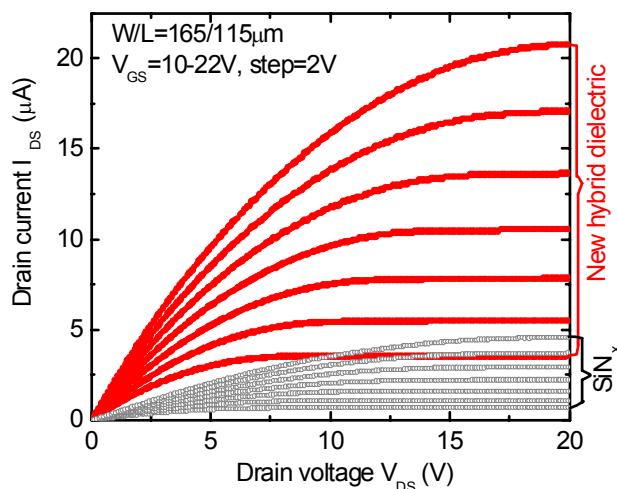


**Figure 3. Cross section of hybrid a-Si:H TFT fabricated for comparison of electrical performance with  $\text{SiN}_x$  TFTs conventionally fabricated on a passivated glass substrate. The hybrid gate dielectric is only half as thick as the conventional  $\text{SiN}_x$  would be. From ref. 3.**

Figure 3 also lists layer thicknesses and process temperatures. The PE-CVD process for hybrid deposition is conducted at nominal room temperature. Because of our equipment layout, the hybrid layer is deposited in a PE-CVD system that is different from the system in which the a-Si:H and nc-Si layers are grown. Therefore the surface of the hybrid layer is exposed to air during transfer



**Figure 4.** Transfer characteristics of the hybrid a-Si:H TFT (red) with a 100-nm thick gate dielectric, and of a SiN<sub>x</sub> TFT made with a 300-nm thick dielectric.



**Figure 5.** Output characteristics of the TFTs of Figure 4. The hybrid TFT can source ~ 4x the current of the SiN<sub>x</sub> TFT, through a combination of higher specific gate capacitance and higher mobility.

from one PE-CVD system to the other. Equipment limitations at this point prevent evaluation of the effects of this exposure, which during the fabrication of a surface-controlled device is avoided if at all possible as it tends to produce trap states at the channel/dielectric interface. We have made both n-channel and p-channel hybrid a-Si:H TFTs [3]. The fact that we obtain record field-effect mobilities suggests that the surface of the hybrid layer is relatively inert against atmospheric contamination.

Fig. 4 shows the transfer characteristic and gate-source leakage current of the n-channel device of Fig. 3. Even though the hybrid dielectric is only 100 nm thick, in contrast to the 300 nm customary with SiN<sub>x</sub> TFTs, the gate leakage current is very low. We surmise that the hybrid dielectric contains few of the nano-cracks that are thought to cause chemical permeation and

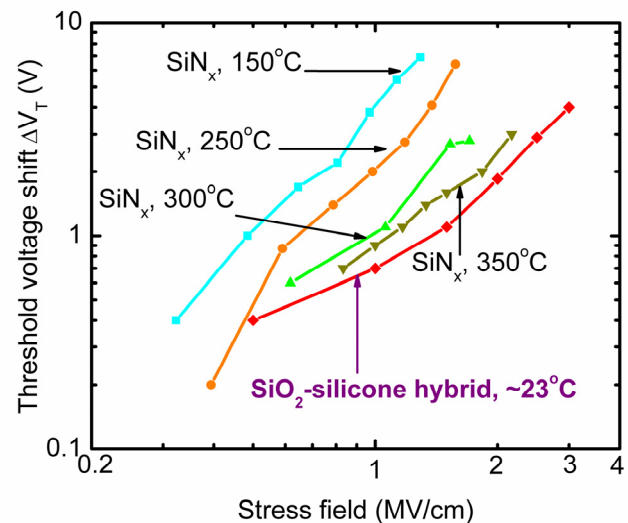
electrical leakage through the layer. The reduced thickness of the hybrid dielectric compensates for its dielectric constant of 4.0, compared to the value of ~ 7.5 of SiN<sub>x</sub>. In fact, the specific capacitance of the hybrid dielectric in most of the TFTs we make is higher than that of SiN<sub>x</sub> TFTs. The high specific capacitance combined with a good quality of the channel/dielectric interface results in a subthreshold slope of ~ 300 mV/decade [7].

The electron field effect mobility extracted from the data shown in Fig. 4 is ~ 2 cm<sup>2</sup>/Vs. It is considerably higher than in the best a-Si:H TFTs reported to date, of 1.2 cm<sup>2</sup>/Vs to 1.4 cm<sup>2</sup>/Vs [8].

Fig. 5 demonstrates the increase in TFT output current available by switching from the SiN<sub>x</sub> to the hybrid dielectric.

Under gate bias-stress testing at high gate field the hybrid transistors are surprisingly stable in comparison to SiN<sub>x</sub> TFTs, as is evident from Fig. 6 [7]. Each TFT was biased for 600 seconds at the field indicated in the figure. Because of the air exposure of the surface of the hybrid, mentioned above, we have not yet systematically evaluated the TFT stability under low-field bias stress conditions.

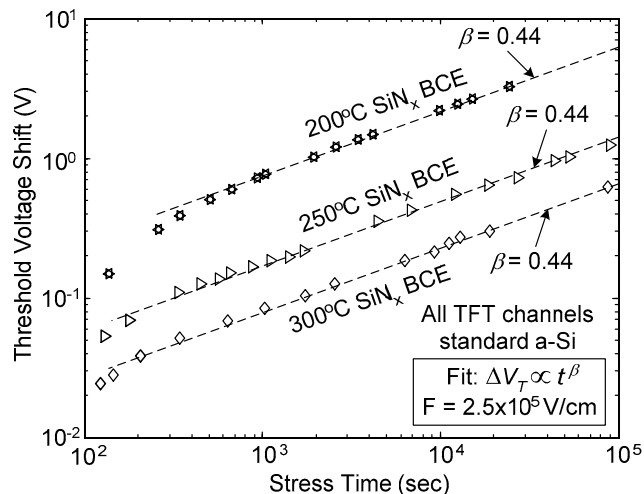
The overall result of substituting SiN<sub>x</sub> with the hybrid is a substantial increase in the TFT output current, as desired for driving OLEDs, and stability at high gate bias-stress.



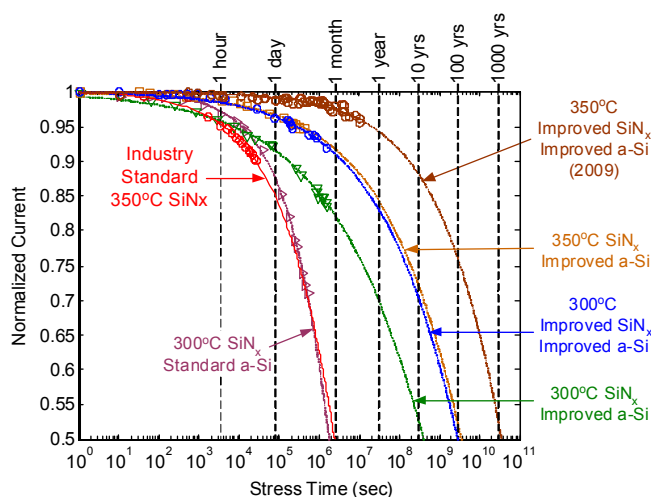
**Figure 6.** Threshold voltage shift of a series of SiN<sub>x</sub> TFTs with gate dielectric deposited over a range of temperatures, and of a hybrid TFT with the dielectric deposited at room temperature. From ref. 7.

### Highly stable SiN<sub>x</sub>/a-Si:H TFTs

In parallel to incorporating the new hybrid material for high electron mobility and mechanical flexibility we have conducted a thorough re-evaluation of the geometry, growth, and processing conditions of conventional SiN<sub>x</sub> TFTs that resulted in highly stable TFTs, as required for the long-term operation of OLEDs. An a-Si:H TFT's threshold voltage shift  $\Delta V_T$  under gate bias is controlled by two physical processes. At high gate field  $V_T$  shifts as charge is injected into the gate dielectric. Therefore this instability depends largely on the quality of the dielectric. At low gate field the shift is driven by the breaking of bonds in the a-Si:H concurrent with charge trapping on the newly formed dangling bonds in the channel.



**Figure 7. Time dependence of the low-field a-Si TFT threshold voltage shift for three different gate nitride growth temperatures. All TFT's have BCE structures and standard a-Si channels. From ref. 2.**



**Figure 8. Normalized TFT current derived from gate bias stress experiments. The current is fitted to models for the threshold voltage shifts caused by charge trapping in the dielectric and in newly broken bonds in the channel. From ref 9.**

We deposited the gate  $\text{SiN}_x$  at high temperature to reduce charge trapping in the dielectric (Fig. 7). To reduce bond-breaking, we deposited the a-Si:H under hydrogen dilution, a technique first introduced for raising the stability of a-Si:H solar cells. These techniques were developed successively, as illustrated by the progress in stability of Fig. 8 [9]. It is seen that the extrapolated TFT lifetime can be raised to over 2 years for 10% current decay, and 1000 years for 50% current decay, respectively. These are the longest lifetimes reported to date for a-Si:H TFTs.

## Summary and Outlook

We are conducting a program to make a-Si:H based TFTs ready for the backplanes of rollable OLED displays. This includes raising the flexibility, the output current, and the electrical stability of the TFTs. Work remains to be done to provide industry with a complete suite of device technologies. As many of the device materials as possible must be made flexible. Techniques for protecting the remaining brittle materials need to be introduced. Statistics of brittle fracture of device layers and devices must be quantified to enable the modeling of manufacturing yield and of product reliability in the field. While the concept of placing devices in the neutral plane for mechanical protection has been noted widely, it has not been systematically evaluated; possible second-order effects yet need to be identified. Our knowledge of the physics a-Si:H TFT operation at low gate fields is inadequate for reliably extrapolating tests of months to operating lifetimes of tens of years. The process techniques that result in a-Si:H TFTs with high mobility and high stability must be brought from the laboratory to industrial practice. However, recent progress has been very encouraging. The fact that we are identifying and addressing such detailed aspects suggests that a-Si:H TFTs has excellent prospects for becoming the technology of choice for roll-out OLED displays.

## Acknowledgements

We thank the U.S. Display Consortium (now FlexTech Alliance), Universal Display Corporation, the Army Research Laboratory, and the New Jersey Commission for Science and Technology for supporting our research. K.H.C. and L.H. are grateful for Princeton Program in Plasma Science and Technology Fellowships through U.S. Department of Energy Contract No. DE-AC02-76-CHO-3073.

## References

- [1] B. Hekmatshoar, A.Z. Kattamis, K. Cherenack, S. Wagner, J.C. Sturm, *J. SID* **16**/1, 183 (2008).
- [2] B. Hekmatshoar, K.H. Cherenack, S. Wagner and James C. Sturm, *Tech. Digest Internat. Electron Devices Meeting 2008*, San Francisco, CA, Dec.15, 2008. Paper 4.5. IEEE, New York, NY, 2008.
- [3] L. Han, P. Mandlik, K.H. Cherenack, and S. Wagner, *Appl. Physics Lett.* **94**, 162105 (2009).
- [4] P. Mandlik, J. Gartside, L. Han, I-C. Cheng, S. Wagner, J.A. Silvernail, R.-Q. Ma, M. Hack, and J.J. Brown, *Appl. Physics Lett.* **92**, 103309 (2008).
- [5] L. Han, K. Song, P. Mandlik, and S. Wagner, *Appl. Physics Lett.* **96**, 042111 (2010).
- [6] L. Han, P. Mandlik, J. Gartside, S. Wagner, J.A. Silvernail, Rui-Qing Ma, M. Hack, and J.J. Brown, *J. Electrochem. Soc.* **156**, H106 (2009).
- [7] L. Han, P. Mandlik, and S. Wagner, *IEEE Electron Device Lett.* **30**, 502 (2009).
- [8] A. J. Kanicki and S. Martin, in *Thin-Film Transistors*, edited by Ch. Kagan and P. Andry, Dekker, New York, 2003, p. 108.
- [9] B. Hekmatshoar, S. Wagner, and J.C. Sturm, *Appl. Phys. Lett.* **95**, 143504 (2009).