Interface Recombination in TiO_2/Silicon Heterojunctions for Silicon Photovoltaic Applications

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Abstract

Solar photovoltaics (PV), the technology that converts sunlight into electricity, has immense potential to become a significant electricity source. Nevertheless, the laws of economics dictate that to grow from the current 2% of U.S. electricity generation and to achieve large scale adoption of solar PV, the cost needs to be reduced to the point where it achieves grid parity. For silicon solar cells, which form 90% of the PV market, a significant and slowly declining component of the cost is due to the high-temperature (> 900 °C) processing required to form p-n junctions. In this thesis, the replacement of the high-temperature p-n junction with a low-temperature amorphous titanium dioxide (TiO_2)/silicon heterojunction is investigated. The TiO_2/Si heterojunction forms an electron-selective, hole-blocking contact. A chemical vapor deposition method using only one precursor is utilized, leading to a maximum deposition condition of 100 °C. High-quality passivation of the TiO_2/Si interface is achieved, with a minimum surface recombination velocity of 28 cm/s. This passivated TiO_2 is used in a double-sided PEDOT/n-Si/TiO_2 solar cell, demonstrating an open-circuit voltage increase of 45 mV. Further, a heterojunction bipolar transistor (HBT) method is developed to investigate the current mechanisms across the TiO_2/p-Si heterojunction, leading to the determination that 4nm of TiO_2 provides the optimal thickness. And finally, an analytical model is developed to explain the current mechanisms observed across the TiO_2/Si interface. From this model, it is determined that once $\Delta E_V(TiO_2/Si)$ is large enough (400 meV), the two key parameters are the Schottky barrier height (resulting in band-bending in silicon) and the recombination velocity at the TiO_2/Si interface. Data corroborates this, indicating the hole-blocking mechanism is due to band-bending induced by the unpinning of the Al/Si interface and TiO_2 charge, as opposed to due to the TiO_2 valence band edge.

Acknowledgements

First and foremost, I thank my advisor, Professor James C. Sturm. I really couldn't have done this without your guidance and patience. Its hard to express in words how critical your presence was in molding my scientific mind and outlook on engineering and research. Joseph Campbell stated that a Heros Journey usually involves an old, wise man lighting the way forward and this was truly the case here. From teaching me how to think like an electron in ELE 545 to pushing me to go beyond the obvious explanations and dig deep into problems, to always encouraging me to submit my work to conferences, to supporting me through my low points throughout the years and congratulating me at my high points, to the culmination of my work into this thesis, thank you so much.

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work, to attend all those PVSC conferences together and to have met a great friend like you.

Speaking of solar cells, this project really came alive with the collaborations with Professors Jeffrey Schwartz, Antoine Kahn and Sigurd Wagner. Thank you all for your incredibly insightful inputs at the DOE group meetings, and especially Professor Schwartz for having the patience to explain chemistry to us engineers. And I cannot forget their students, Gabriel Man and Girija Sahasrabudhe, thank you for providing much needed spectroscopy and chemistry data and insights. You guys were incredible to work with and truly outstanding scientists.

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Ive always had a curious mind, and Ive been blessed to pursue many activities outside of research during my tenure at Princeton. My first three years at Princeton were defined by my interest in dancing. Id like the acknowledge everyone on the Princeton Bhangra team with whom I had the honor of dancing. Huge shout out to the OG group that rebooted the team: Saswathi Natta, Elizabeth LaMontagne, Medha Ranka, Keshav Singh, Amit Shah, Nikhil Bumb, Alan Hatfield, Akshay Kumar, Kanwal Matharu, Zach Garcia, Arjun Dhillon, my always gracious and graceful jodi partners, Merve Gurakar, and Rachel Webb, and our indefatigable captain Aneesh Sahni. Aneesh, you did a fantastic job guiding the team through our tumultuous beginnings and you were a great jodi partner and friend to boot! We got tremendously lucky with a great second batch of dancers: Christina Healy, Lucie Wright, Eskender McCoy, Anand Shah thanks for joining us when we were at a low point and sticking through. Our first year was the most challenging, but perhaps because of that also the most memorable.

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As they approach me, so I receive them. All paths, Arjuna, lead to me.

- Lord Krishna, the Bhagavad Gita

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Chapter 1

Introduction

1.1 Motivation

> The necessaries of life for man in this climate may, accurately enough, be distributed under the several heads of Food, Shelter, Clothing, and Fuel; for not till we have secured these are we prepared to entertain the true problems of life with freedom and a prospect of success. - Walden, Henry David Thoreau [1]

Although these words were written by Thoreau about his secluded living near Walden Pond, the four necessary heads of Food, Shelter, Clothing, and Fuel still apply to modern man living in the 21st century. Even more so, as our Civilization has advanced technologically, energy (Fuel) has arguably become the prime head, supporting everything we do, including an agriculture industry that provides for billions of people (Food), a retail industry that provides a wide gamut of opportunities to dress ourselves as per our individual and tribal tastes (Clothing), and the opportunity to live not just in a wooden cabin, but a high-rise apartment complex in cities that house tens of millions of people (Shelter), not to mention the other wonders and luxuries of modern life.

However, whether we can maintain our modern society remains to be seen. Figure 1.1 shows the projected growth in world population [2]. As one can see, the world population is expected to rise from the current 7.6 billion to 9.8 billion by 2050. Add to that the fact that the developing world is well...developing. According to the OECD, the global middle class is expected to rise from 2 billion in 2009 to 5 billion in 2030. With such vast increases in not just total human population, but middle class population as well, energy needs will need to keep up.

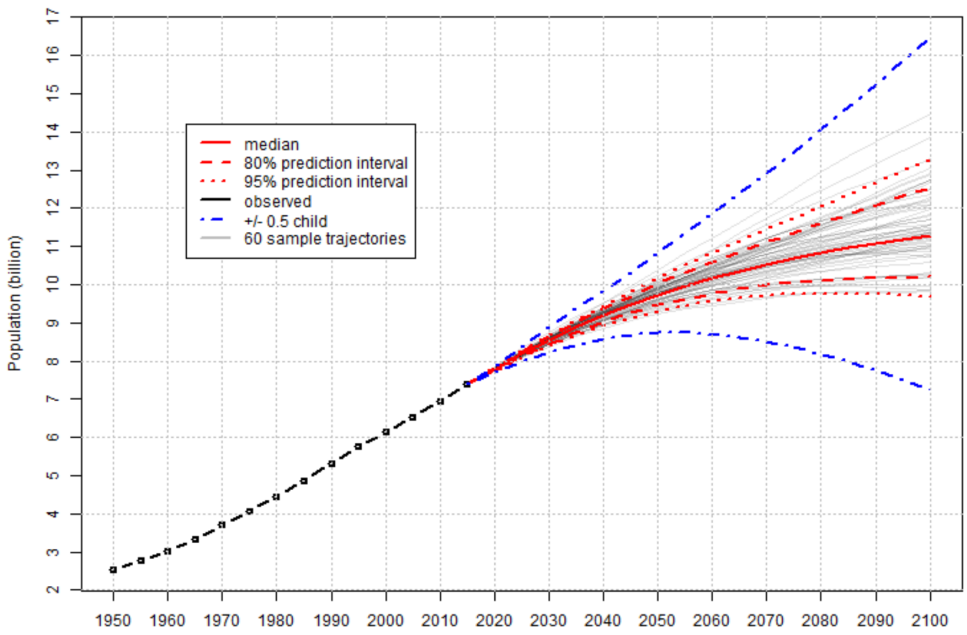


Figure 1.1: UN World Population Projections from 1950 to 2100 [2]

One particular avenue of energy production that is underutilized is solar energy. This thesis will specifically discuss solar photovoltaics (solar PV) the direct conversion of solar energy into electricity. Other methods of conversion of solar energy exist, including solar thermal (conversion to heating for building) and solar biomass (conversion to biomass for fuel).

In fact, one could easily argue that all our energy comes from the sun, directly or indirectly. As Vaclav Smil writes in his book, Energy and Civilization:

"Fundamentally, no terrestrial civilization can be anything but a solar society dependent on the Suns radiation, which energizes a habitable biosphere and produces all of our food, animal feed and wood."

Even our major energy source, fossil fuels, can trace their origin back to the power of the sun:

> The origins of fossil fuels are also in the transformation of solar radiation: peat and coals arose from the slow alteration of dead plants (phytomass), hydrocarbons from more complex transformations of marine and lacustrine single-celled phytoplankton (mostly cyanobacteria and diatoms), zooplankton (mostly foraminifera), and some algae, invertebrates, and fish.

This would explain why mankind has always appreciated the importance of the sun as indicated by the elevation of the sun god in numerous religions pantheons, including the Egyptian king of the gods, Ra, the Greek Apollo, the Babylonian sun-god Marduk, and one of the most revered gods of the Vedas, the Hindu deity Surya.

So how abundant is solar energy exactly? Figure 1.2 shows the solar irradiation in the US. To put this figure in perspective, the total area of Arizona is 295,000 km^2. giving the state a capacity to generate 295,000 GW (295 TW) of power. In practice, due to power conversion losses, intermittency and other factors, only $\sim$ 1/8th of the 295 TW could be produced as electricity. In contrast, what is the total electricity generation capacity of the US today? Only 1 TW! And how much of the total US electricity generation in 2017 came from solar PV? A measly 1.8% according to the US Energy Information Administration [3].

So although Prometheus was able to take the power of fire from the gods for the benefit of humanity, we have not been able to repeat that feat. Two main issues prevent mass-scale adoption of solar PV: 1. intermittency, and 2. cost. Intermittency means electricity generation is not constant, as one might expect due to cloud coverage

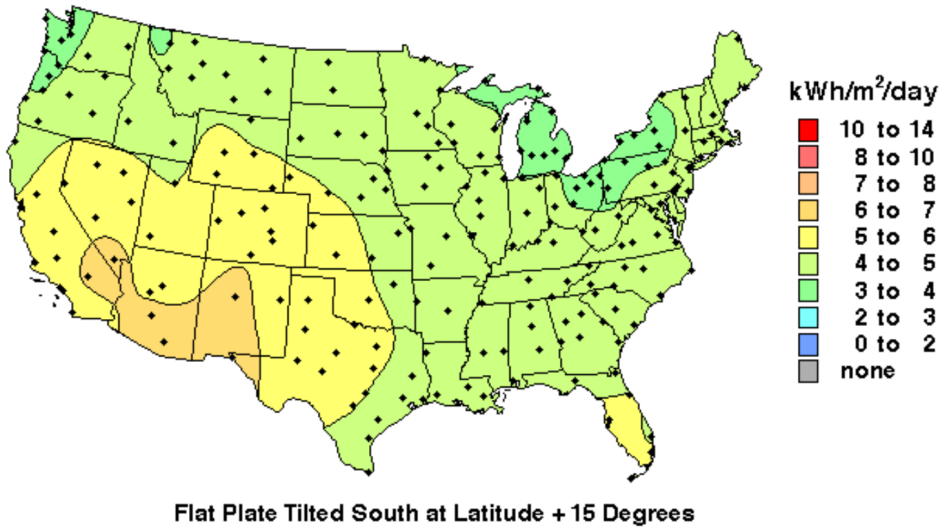


Figure 1.2: United States Solar Irradiation Map, for Flat Plate Tilted South at Latitude + 15 Degrees [4]

during the day and lack of sunlight at night time. This is a problem that could be mitigated through technologies in development right now, including grid-scale storage, microgrids, and demand-side management. The core motivation of this thesis is the second issue: cost.

Different electricity sources are compared to each other with a metric known as levelized cost of electricity (LCOE). LCOE tells us how much one unit of energy (kWh) costs to generate. For solar PV to be competitive, its LCOE needs to be 5-6 cents per kWh (approximately \$1/watt cost for a solar panel). This would achieve "grid parity" - the LCOE being equal to the purchasing price of electricity on the US electric grid. Figure 1.3 shows dropping cost of solar over the years and the Department of Energy's goal for 2020. In pink is shown the module cost. The module cost has dropped significantly from 10 cents/kWh to 3 cents/kWh. However further cost reductions are required to achieve grid parity. The aim of this thesis is towards replacing high-cost Si p-n junction fabricated at high temperatures (>900 °C) with a low-temperature, possibly low-cost TiO_2/Si heterojunction.

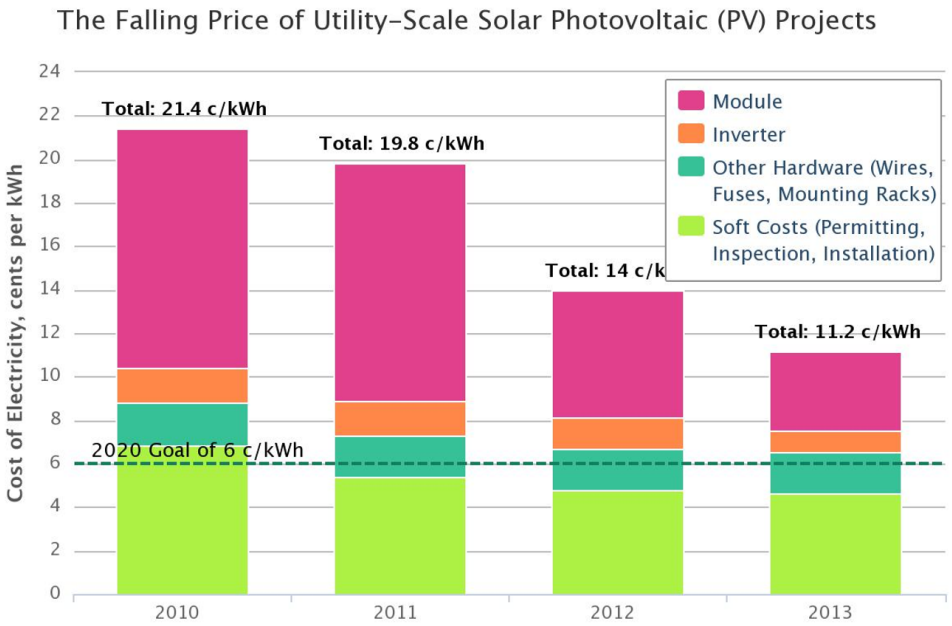


Figure 1.3: The Falling Price of Utility-Scale Solar Photovoltaics [5]

To understand how that would work, we first need to understand how a solar cell operates. In the next section, a silicon p-n junction is used to illustrate this.

1.2 Solar Cell Operation

Figure 1.4 shows a conventional monocrystalline silicon PN junction with the p-doped layer on the left side and the n-doped layer on the right side. Note the large band bending in the center as the fermi-levels in the p- and n-layers line up. In Figure 1.5, we see what happens when a positive voltage (V_A) is applied on the p-side (forward bias). The band-bending in the center is reduced and current flows from the p-layer to the n-layer.

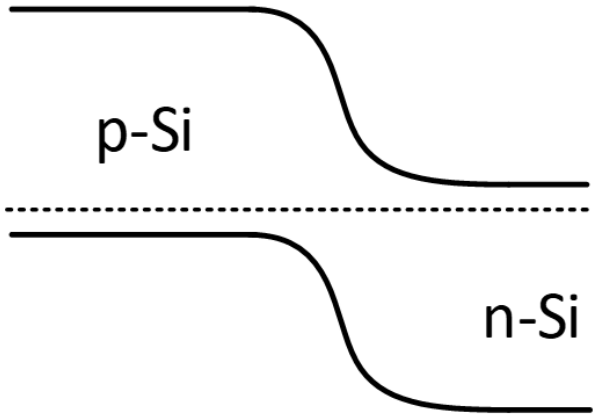


Figure 1.4: Silicon PN junction

The current has two components, as shown in Figures 1.6 and 1.7. Electrons from the n-layer get injected across the barrier into the p-layer, where they recombine with holes (1.6). This current is given by:

$$J_{elec} = \frac{qn_i^2 D_n}{N_A L_n} (e^{\frac{qV_A}{kT}} - 1) \tag{1.1}$$

where q is the electron charge, 1.6x10^{-19} C, n_i is the intrinsic carrier density, D_n is the electron diffusivity, N_A is the doping of the p-layer, and L_n is the diffusion length of electrons in the p-layer. Holes, on the other hand, are injected from the p-layer

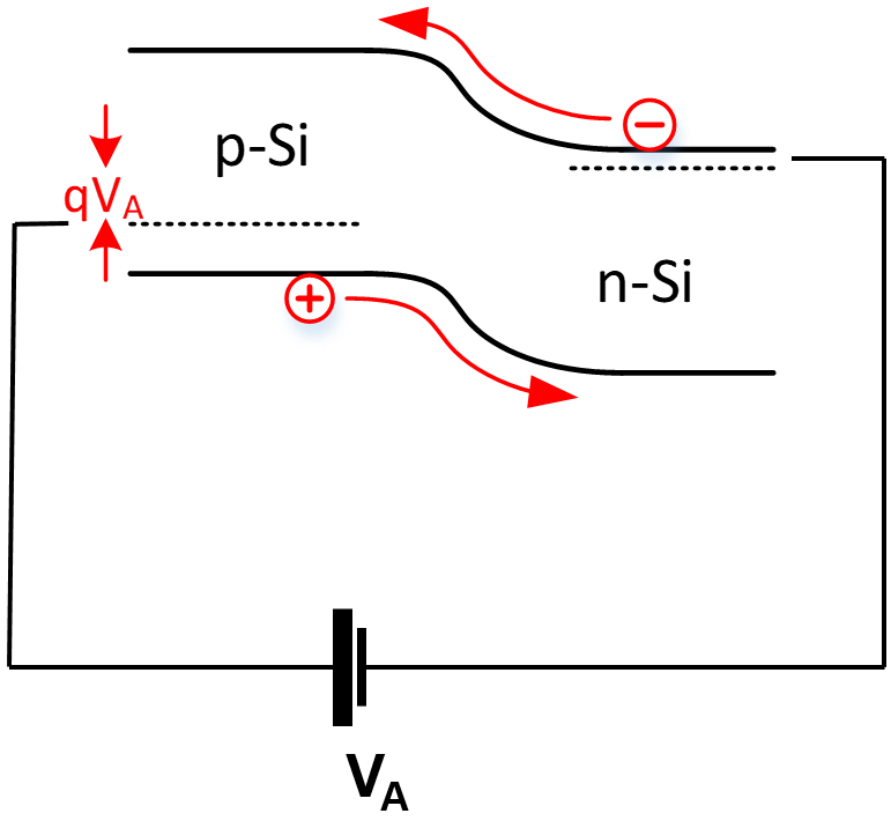


Figure 1.5: Silicon PN junction under forward bias

across the barrier into the n-layer, where they recombine with electrons (1.7). This current is given by:

$$J_{hole} = \frac{qn_i^2 D_p}{N_D L_p} (e^{\frac{qV_A}{kT}} - 1) \tag{1.2}$$

where D_p is the hole diffusivity, N_D is the doping of the n-layer, and L_p is the diffusion length of holes in the n-layer. Combined, we get the equation for the total dark current in a silicon PN diode ("dark" here implying no light):

The sum is given by J_{dark}:

$$J_{dark} = \frac{qn_i^2 D_n}{N_A L_n} (e^{\frac{qV_A}{kT}} - 1) + \frac{qn_i^2 D_p}{N_D L_p} (e^{\frac{qV_A}{kT}} - 1) \tag{1.3}$$

One can separate out the "pre-factors" in both hole and electron currents to obtain:

$$J_{dark} = \left(\frac{qn_i^2 D_n}{N_A L_n} + \frac{qn_i^2 D_p}{N_D L_p}\right)(e^{\frac{qV_A}{kT}} - 1) \tag{1.4}$$

The prefactors can be combined as one term, $\boldsymbol{J_0}$**, known as the saturation current density**. We thus obtain:

$$J_{dark} = J_0(e^{\frac{qV_A}{kT}} - 1) \tag{1.5}$$

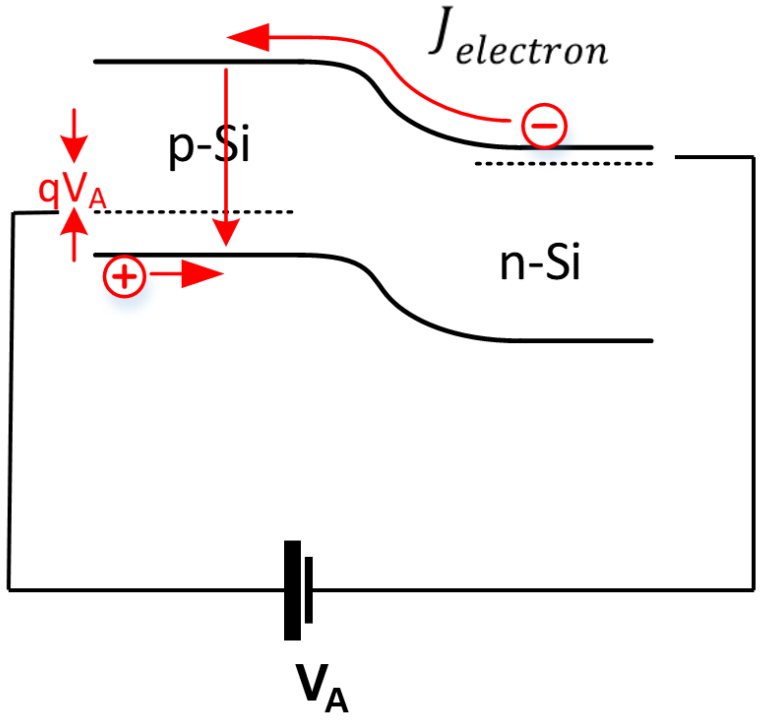


Figure 1.6: Silicon PN junction under forward bias: Electron current

Figure 1.8 shows what happens under light - i.e. when the sun is shining. The total dark current, represented by the dark electron and hole current, is still present since these current components are always present under forward bias. The light itself induces photocurrent: a photon gets absorbed and the energy is given to an

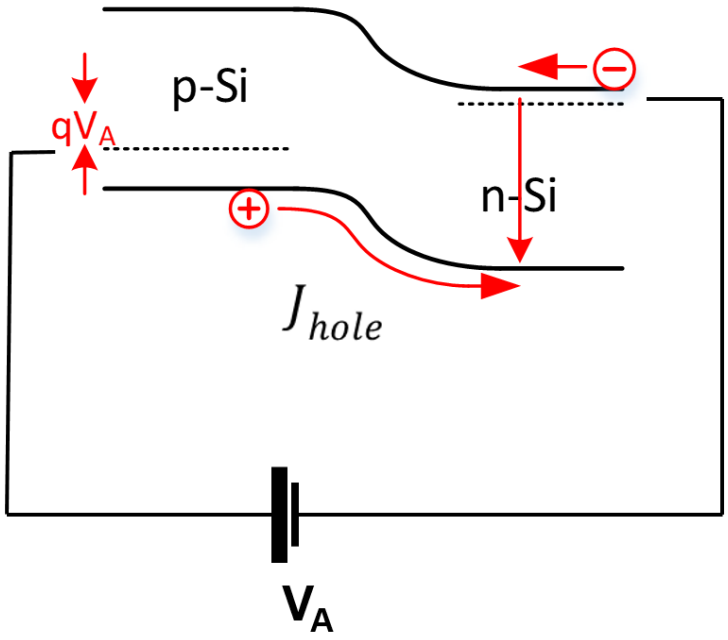


Figure 1.7: Silicon PN junction under forward bias: Hole current

electron in the valence band which jumps to the conduction band. As a result, one now has an electron photocurrent component and a hole photocurrent component. The photocurrent hole cannot cross the PN junction barrier, and thus will move towards the left and recombine at the metal contact on the p-layer (metal contact not shown). The photocurrent electron, on the other hand, will move towards the right, be swept across the barrier region due to the electric field present, traverse the n-region and recombine at the metal contact on the n-layer (metal contact not shown). In other words, the photocurrent moves in the opposite direction of the dark current. A well-designed solar cell ensures that the maximum amount of photocurrent electrons and holes move in the "right" direction. A poorly designed solar cell, in contrast, will cause the photocurrent charges to recombine prematurely (not at the metal contacts), thereby reducing the photocurrent measured.

The equation for J_{total} is given by

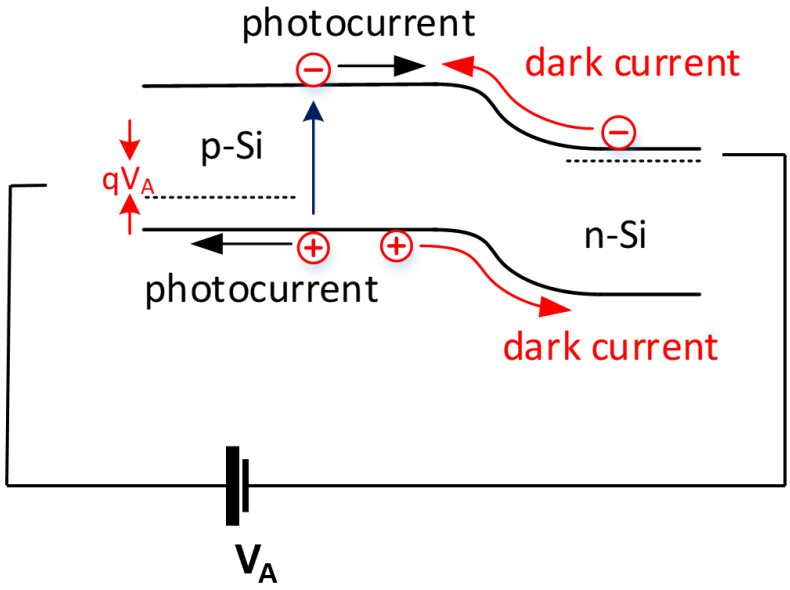


Figure 1.8: Silicon PN solar cell: under light and applied bias

$$J_{total} = J_0 \left(e^{\frac{qV_A}{kT}} - 1 \right) - J_{photo} \tag{1.6}$$

Figure 1.9 shows the current-voltage (I-V) characteristics of a solar cell diode. The dark current (J_{dark}) is shown in blue, and as expected shows an exponential behavior. The total current (dark + photocurrent) is shown in red, it is the dark current exponential superimposed with the constant photocurrent J_{photo}. For solar cells, what we care the most about is the maximum power conversion efficiency (PCE) that this solar cell can produce. The PCE is given by:

$$PCE = \frac{P_{out}}{P_{in}} \tag{1.7}$$

P_{in} can be calculated by determining the spectrum of the light shining on a solar cell, specifically the number of photons per frequency. Typically, to compare power conversion efficiencies, solar cells and panels are measured under the "AM1.5G" spectrum, shown in Figure 1.10. AM1.5G is an industry standard spectrum that emulates

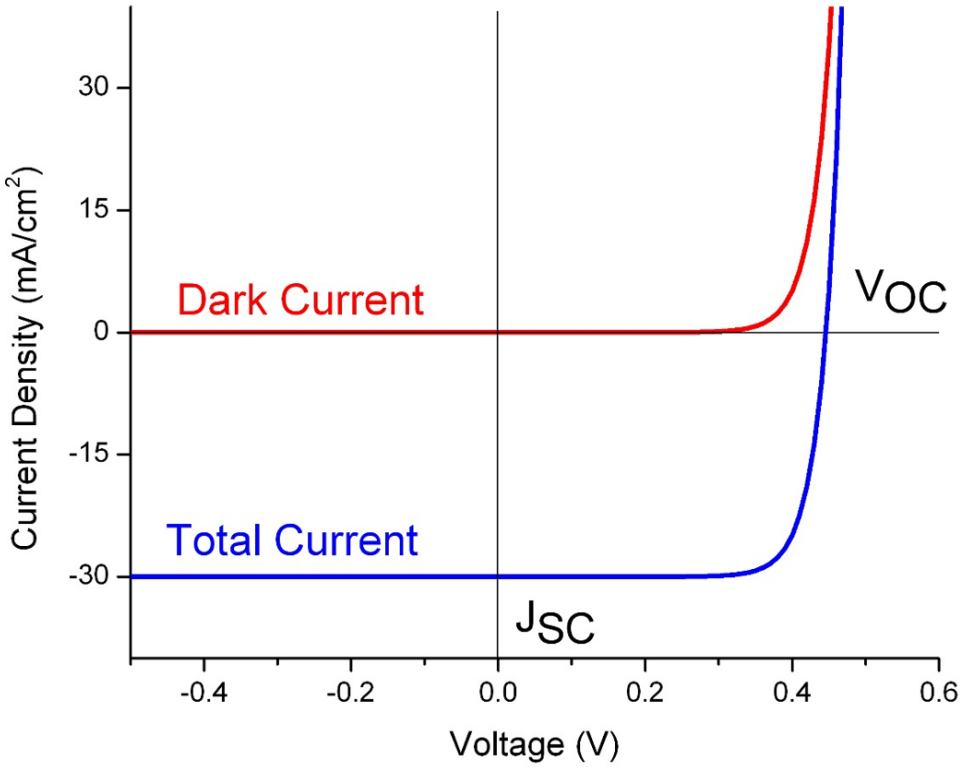


Figure 1.9: I-V characteristics of Silicon PN solar cell under dark and under light

the solar spectrum at an "absolute air mass of 1.5", which corrsponds to a solar zenith angle 48.19 and has an integrated power density of 1000 W/m^2.

P_{out} can be determined by looking at the I-V characteristics. Figure 1.9 is redrawn as Figure 1.14. to illustrate three key points: V_{OC}, J_{SC} and the maximum power point (MPP) as shown as an asterisk at the bottom right corner of the "Maximum Power" box. MPP is given by

$$MPP = V_{MPP}J_{MPP} \tag{1.8}$$

where V_{MPP} and J_{MPP} are the voltage and current values of the asterisk point. J_{SC} is the "short-circuit current", the current when the voltage is 0 V and is typically the same as J_{photo}. J_{SC} is optimized by optimizing a solar cell design for minimal light reflection and maximum light absorption.

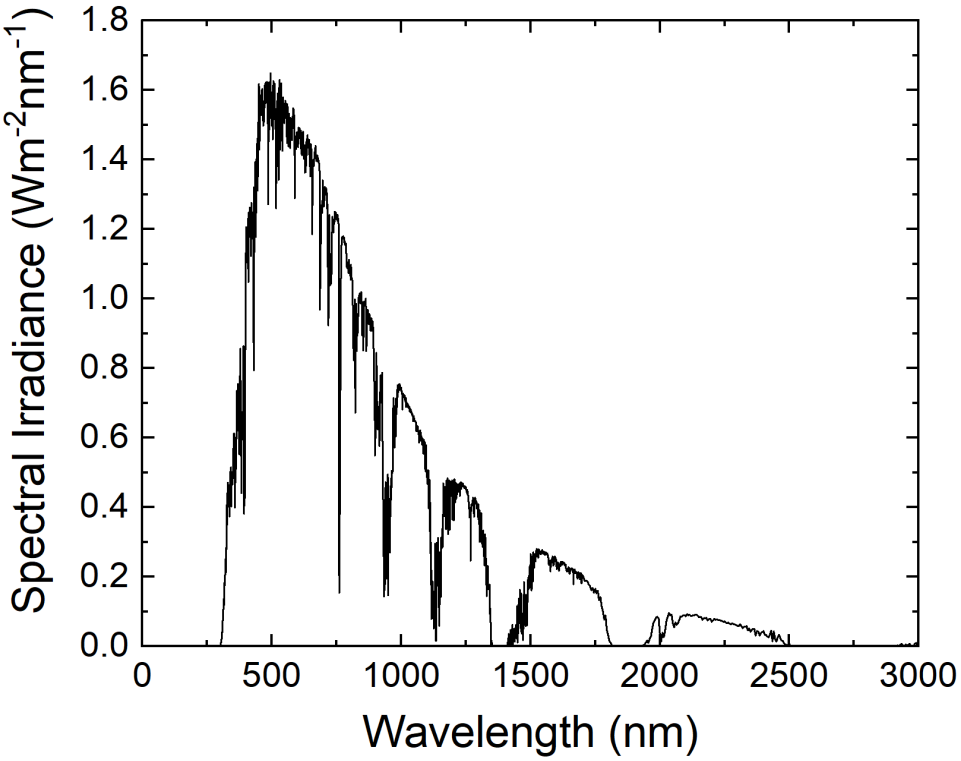


Figure 1.10: AM 1.5G spectrum: Spectral irradiance versus wavelength. [6]

V_{OC} is the "open-circuit voltage", the voltage when the current is 0 A. It can be calculated by setting $J_{total} = 0$ in equation 1.6. The final result ends up being:

$$V_{OC} = kT\ ln(\frac{J_{SC}}{J_0} + 1) \tag{1.9}$$

V_{OC} can be increased by either increasing the short-circuit current J_{SC} or by reducing the saturation current density J_0. The latter will be a key area of focus in this thesis. One particular method to reduce J_0 is by minimizing recombination, especially at silicon surfaces, where Si dangling bonds exist. Passivation of these silicon surface dangling bonds is a common method to reduce surface/interface recombination.

A third parameter is the "Fill Factor" (FF), given by the ratio:

$$FF = \frac{V_{OC} J_{SC}}{MPP} \tag{1.10}$$

Thus, we obtain for maximum power conversion efficiency (η):

$$\eta = \frac{V_{OC} J_{SC} FF}{P_{in}} \tag{1.11}$$

The fill-factor can be affected by parasitic resistances, i.e. non-zero series and non-infinite shunt resistance as shown in Figure 1.11. Change in the maximum power point and thus FF is shown for increasing series resistance (R_s) in Figure 1.12. Similarly, change in the MPP point is shown for decreasing shunt resistance (R_{sh}) in Figure 1.13.

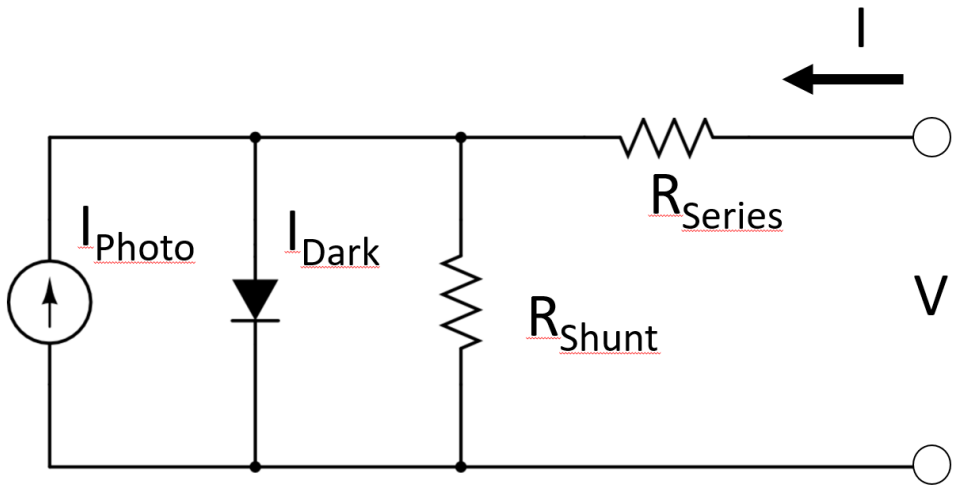


Figure 1.11: Diagram of solar cell with series and shunt resistances

Shockley and Queisser showed that for a single junction silicon solar cell (a bandgap of 1.1eV), the theoretical maximum power conversion efficiency is 31% [7]. So how close are we to optimizing V_{OC}, J_{SC}, the fill-factor and achieving this 31% number? And concomitantly, what is the cost of a high-efficiency solar cell? In the next subsection, these questions are answered by looking at two advanced monocrystalline silicon solar cell designs are discussed.

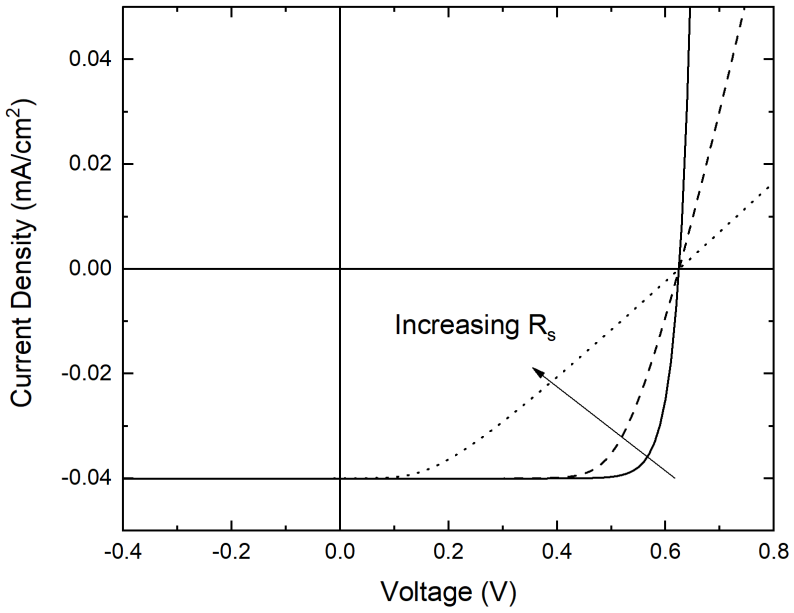


Figure 1.12: I-V characteristics of Silicon PN solar cell under light with effect of non-zero R_s

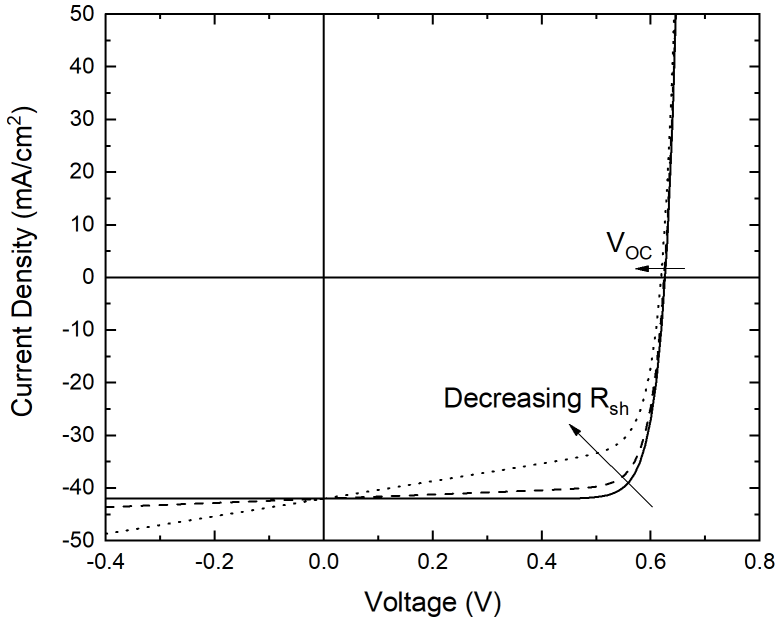


Figure 1.13: I-V characteristics of Silicon PN solar cell under light with effect of non-zero R_{sh}

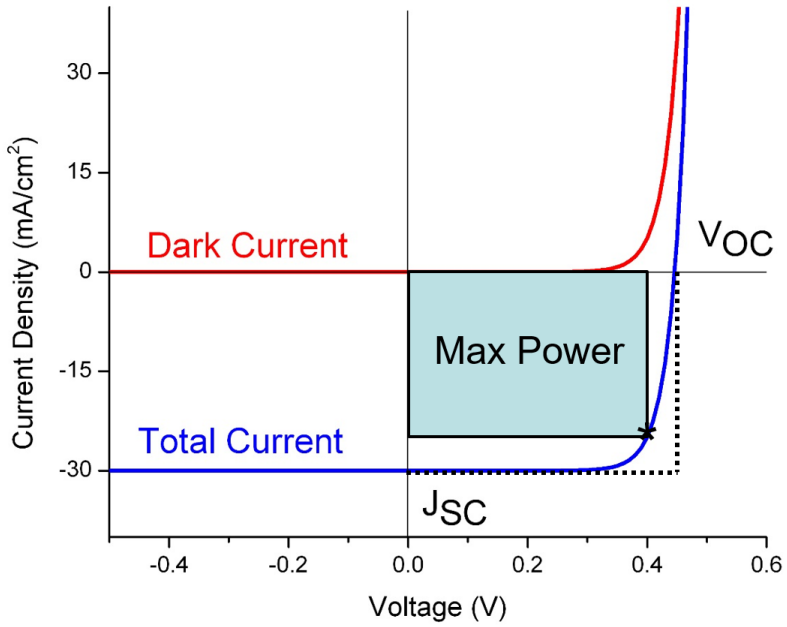


Figure 1.14: I-V characteristics of Silicon PN solar cell under light, showing PCE, V_{OC}, J_{SC}

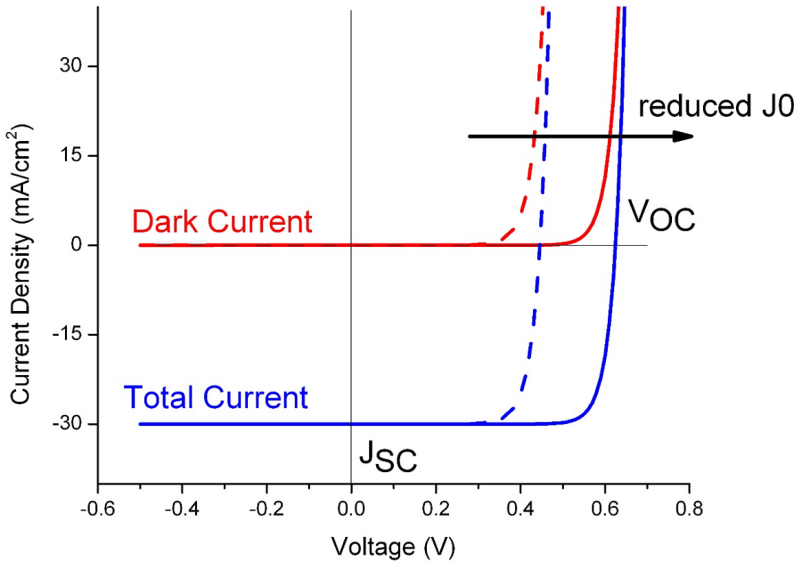


Figure 1.15: I-V characteristics of Silicon PN solar cell under light, after reducing J_0

1.3 Previous Work

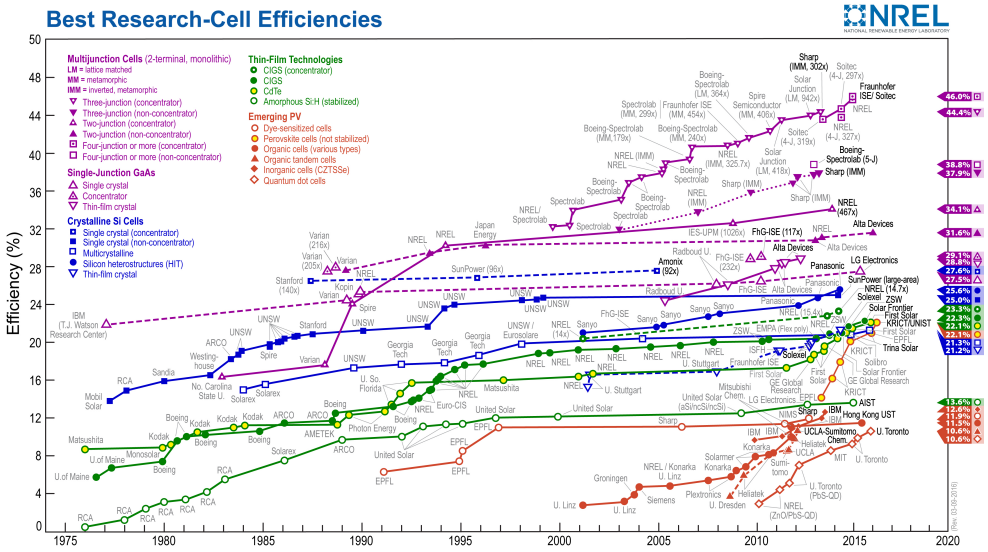
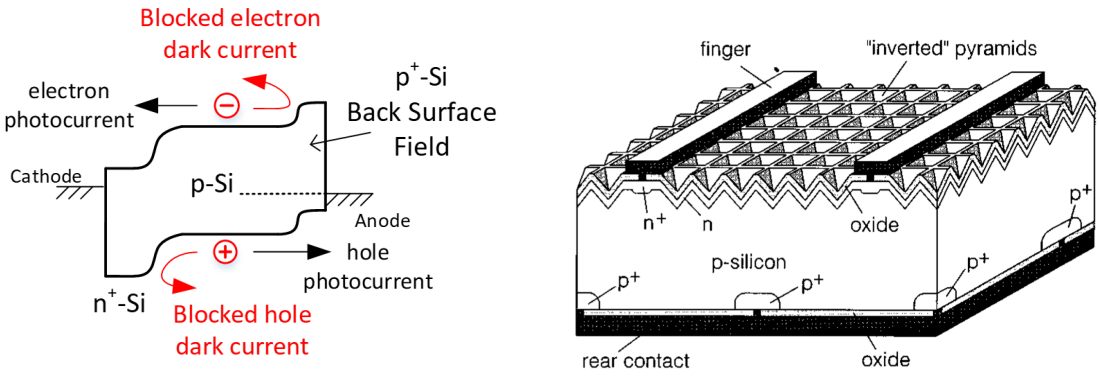


Figure 1.16: NREL: Best Research-cell Efficiencies [8]

Figure 1.16 is the efficiency plot from the National Renewable Energy Lab (NREL), showing different types of solar cells by material (inorganic: Silicon, GaAs and other III-V materials, organic, hybrid, perovskites) and by type of junction (single junction, multi-junction). As this thesis focuses on monocrystalline silicon-based solar cells, this subsection will mention two major forms of silicon solar cells: the passivated emitter rear locally-diffused (PERL) solar cell and the Heterojunction with Intrinsically Thin layer (HIT) solar cell.

The PERL cell was developed in the late 1990s by Martin Green at University of South New Wales, Australia [10, 11]. The cell structure and band diagram is shown in Figure 1.17.

The cell structure consists of a $n^+/p/p^+$ device. The n^+/p junction, formed through a high-temperature diffusion of phosphorus, is utilized to collect photocurrent electrons. A backsurface field (BSF) is created by the $p/p/^+$ junction, formed through a high-temperature diffusion of boron. The BSF collect photocurrent holes, and reduces the bottom contact resistance. The diffused layers in the $n^+/p/p^+$ struc-



(a) (b)

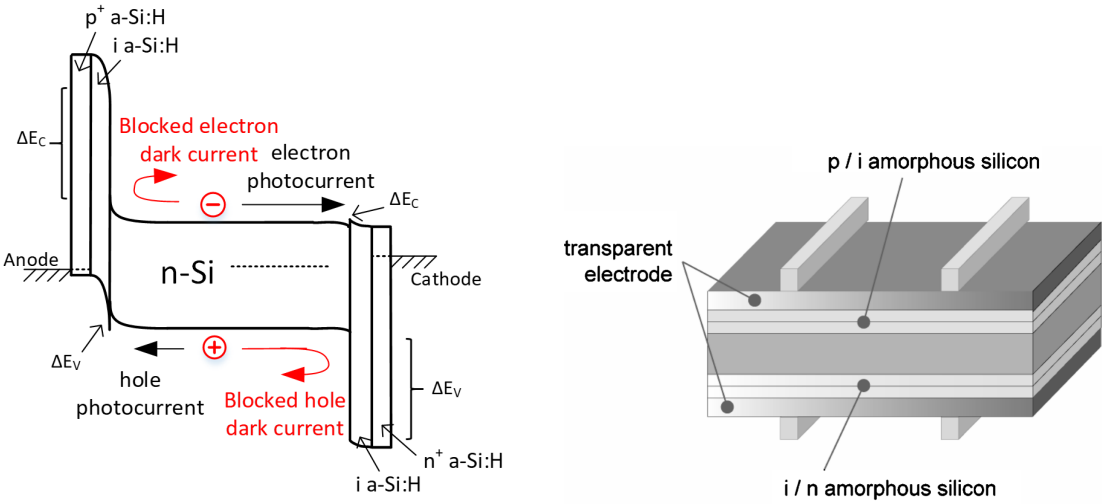
Figure 1.17: PERL solar cell: (a) Band Diagram and (b) Structure. Reproduced from [9], with the permission of AIP Publishing.

ture also work to minimize J_0 (increasing V_{OC}) by blocking dark current components. Both top and bottom surfaces are textured for maximal light absorption and passivated with SiO_x to minimize defects at the silicon interface, which would cause recombination of photo generated carriers (texturing thus increases J_{SC}). Furthermore, the MgF_2/ZnS anti-reflection coating on top reduces light reflection. Point contacts (small contacts formed by first etching SiO_x and metallizing the exposed p^+ and n^+ regions) are utilized further to keep recombination at a minimum.

The PERL cell has achieved a maximum power conversion efficiency of 25.0%. However the complexity of the fabrication process led to it not being commercially viable.

A secondary issue is the heavy doping of the p^+ and n^+ regions, as it is known that Auger recombination reduces the open-circuit voltage [12]. Auger recombination increases with doping [13], thus optimal V_{OC} levels are achieved when the silicon substrate has a very low doping. The high doping of the p^+ and n^+ regions also leads to bandgap narrowing, which can further decrease V_{OC}.

One would be inclined to develop a solar cell without the need of high-temperature diffusion processes and a complex fabrication to form point contacts. This leads to the next solar cell design, the HIT cell.



(a) (b)

Figure 1.18: HIT solar cell: (a) Band Diagram and (b) Structure [14]. Reproduced from [14], with permission.

The HIT cell was developed in the early 1990s by the former Sanyo Electric Company (now part of Panasonic) [15]. The cell structure and band diagram is shown in Figure 1.18.

The HIT cell consists of a base silicon layer, coated on both sides with intrinsic amorphous silicon (a-Si:H). The amorphous silicon is saturated with hydrogen, enabling passivation of the crystalline silicon surface with Si-H bonds. One side further has doped p-type amorphous Si on top of the intrinsic a-Si. This p-type side works as a electron-blocking, hole-selective contact, which blocks electrons from travelling from the silicon to the contact, while allowing holes to pass through.

The other side has doped n-type amorphous Si on top of the intrinsic a-Si. The n-type side works as a hole-blocking, electron-selective contact, which will block holes from travelling from the silicon to the contact, while allowing holes to pass through.

The amorphous silicon is deposited using a plasma-enhanced chemical vapor deposition (PECVD) process, with maximum processing temperature of 200 °C, significantly lower than the >900 °C needed for the high-temperature diffused region for the PERL solar cell.

So how does a HIT solar cell hold up cost-wise? A study published by Goodrich et al. [16] shows cost for monocrystalline silicon in 2011 and future projections. For the HIT cell, it was found that large scale manufacturing would imply a cost of \$0.62/W From the \$0.62/W, fabrication itself would be \$0.30/W. And the PECVD steps would cost \$0.11/W, in other words a third of the total fabrication cost, and almost 20% of the total cell cost.

Thus, there is still an opportunity to reduce cost by focusing on manufacturing. More specifically manufacturing can be reduced by replacing the amorphous silicon layers by a lower fabrication cost material. The next subsection will discuss specifically electron-blocking, hole-selective contacts (hole-selective contacts for short) and hole-blocking, electron-selective contacts (electron-selective contacts for short). These two types of contacts are collectively known as carrier-selective contacts (CSCs).

1.4 Carrier-Selective Contacts

There are 5 requirements for a carrier selective contact.

Let's start with an electron-selective contact as shown in Figure 1.19, which would replace a p^+-p junction:

1. Wide bandgap semiconductor must have a non-existent to small conduction band offset. Electrons must be able to travel from silicon to metal.

2. Wide bandgap semiconductor must have a large valence band offset. Holes must be blocked from travelling from silicon to metal.

3. Bending of the bands downwards in the silicon near the electron-selective contact or no band-bending. Downward band-bending would cause holes to be repelled and electrons to accumulate (wanted). Upward band-bending on the other hand would cause electrons to be repelled and holes to accumulate (unwanted).

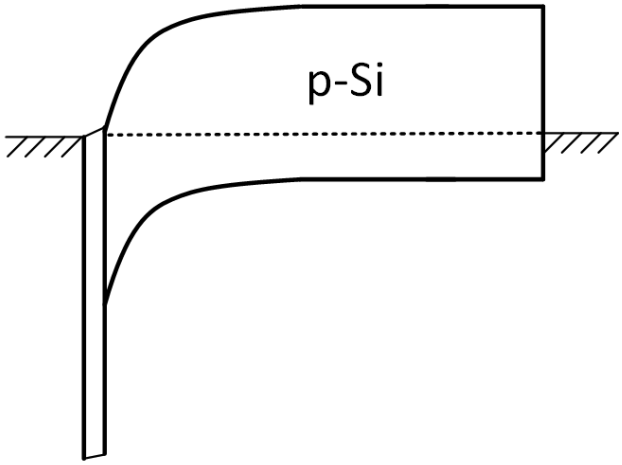


Figure 1.19: Electron-selective contact made of p-type Si in contact with wide bandgap semiconductor material.

4. Passivation of silicon/wide bandgap semiconductor interface. The interface must be well-passivated (very few defect states) to reduce or minimize photocurrent electrons from recombining (reducing J_{SC}) and dark current holes from recombining (increasing J_0). A recombination velocity (discussed in Chapter 3) of 10 cm/s or less is preferred.

5. High mobility for electrons. Assuming a 5 nm wide bandgap semiconductor layer and a 1% voltage drop for an optimal solar cell ($V_{MPP} \sim 700$ mV), electron mobility in the wide bandgap semiconductor layer should be at least 2.5x10^{-3} $cm^2V^{-1}s^{-1}$.

For a hole-selective contact, shown in Figure 1.20, which would replace a n^+-n junction, we obtain:

1. Wide bandgap semiconductor must have a non-existent to small valence band offset. Holes must be able to travel from silicon to metal.

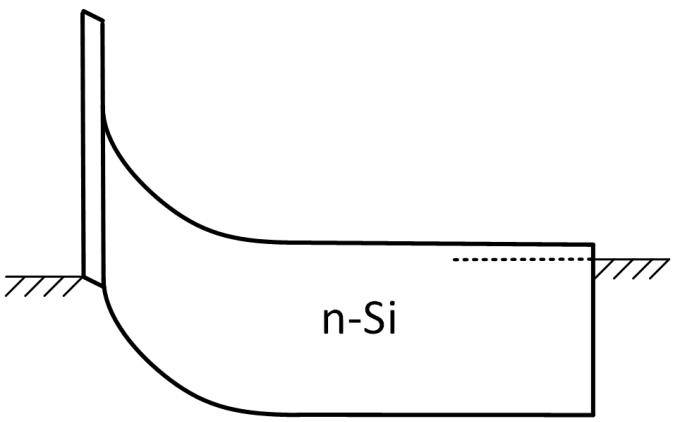


Figure 1.20: Hole-selective contact made of n-type Si in contact with wide bandgap semiconductor material.

2. Wide bandgap semiconductor must have a large conduction band offset. Electrons must be blocked from travelling from silicon to metal.

3. Bending of the bands upwards in the silicon near the hole-selective contact or no band-bending. Upward band-bending would cause electrons to be repelled and holes to accumulate (wanted). Downward band-bending on the other hand would cause holes to be repelled and electrons to accumulate (unwanted).

4. Passivation of silicon/wide bandgap semiconductor interface. The interface must be well-passivated (very few defect states) to reduce or minimize photocurrent holes from recombining (reducing J_{SC}) and dark current electrons from recombining (increasing J_0). A recombination velocity of 10 cm/s or less is preferred.

5. High mobility for holes. Assuming a wide bandgap semiconductor layer and a 1% voltage drop for an optimal solar cell ($V_{MPP} \sim 700$ mV), hole mobility in the wide bandgap semiconductor layer should be at least 2.5x10^{-3} cm^{2}V^{-1}s^{-1}.

For a double-sided heterojunction device - electron-selective contact on one side and a hole-selective contact on the other side - both set of requirements would apply.

Figure 1.21 shows a double-sided device on n-Si with a front side hole-selective contact. In contrast, Figure 1.22 shows a double-sided device on p-Si with a front side electron-selective contact.

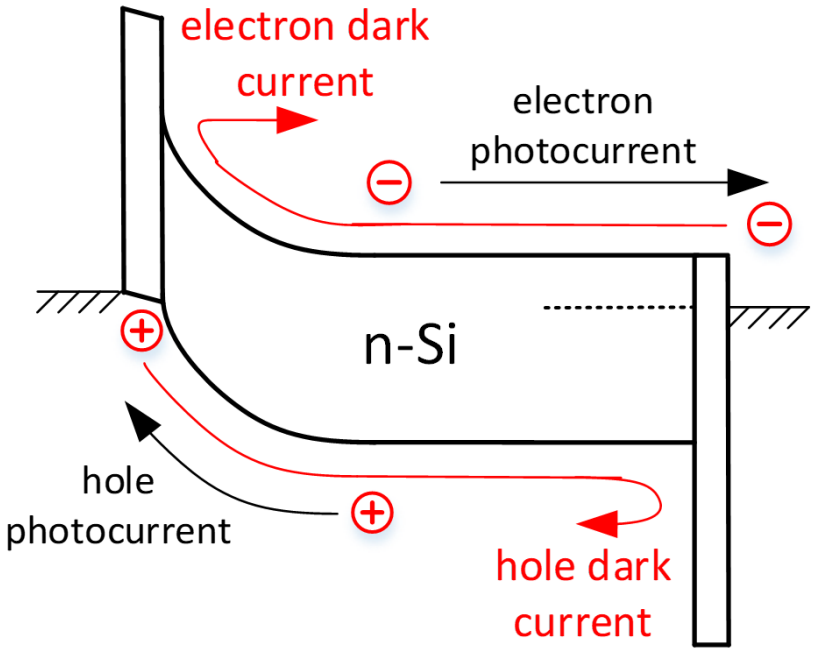


Figure 1.21: Hole-selective contact/n-Si/Electron-selective contact

Figure 1.23 shows a list of a few different materials versus the conduction band (E_C) and valence band (E_V) edge of silicon [17]. As noted before, an ideal hole-blocking, electron-selective contact will have a very small conduction band offset and a large valence band offset. From this figure, we see that two materials fit the bill: ZnO and TiO_2. Titanium oxide was selected, as it is a material that has been used in silicon solar PV as an anti-reflection coating (ARC) due to the fact it absorbs very little in the visible and has a refractive index of 2.4 [18].

The device physics of how such selective contacts can replace p-n and n^+-n junctions in solar cells is described in Chapter 3 in this thesis. It is seen that the recombination at the interface between the Si and the widegap material is a key factor in their performance. Characterizing the interface recombination at the TiO_2/Si, under-

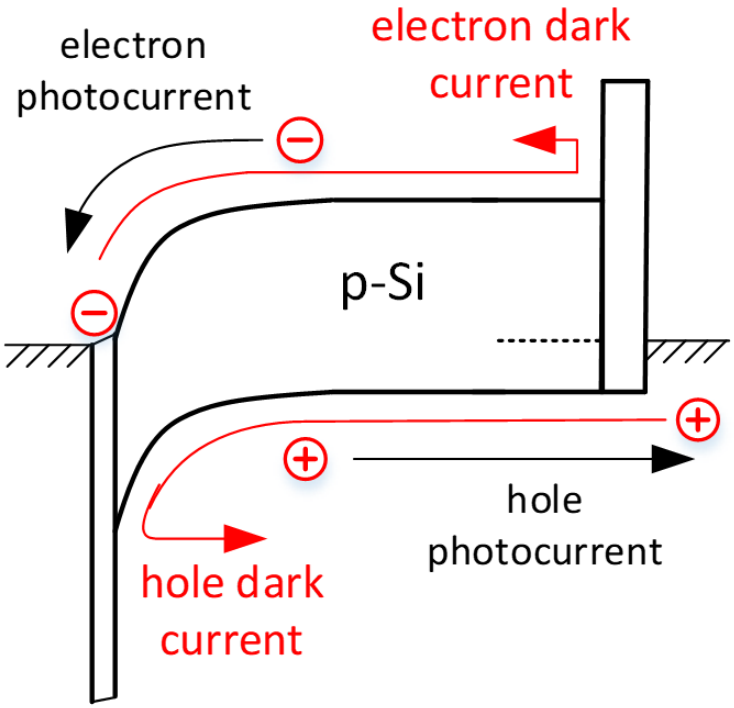


Figure 1.22: Electron-selective contact/p-Si/Hole-selective contact

standing its effect on devices, reducing the interface state density and recombination is the major focus of this thesis.

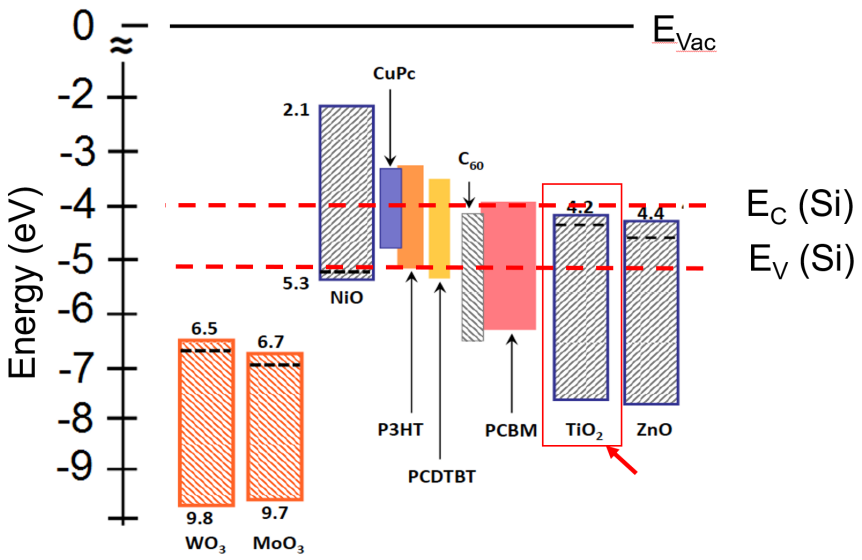


Figure 1.23: Conduction and Valence Band Edges of different materials shown relative to Silicon Conduction and Valence Band Edges (red dotted lines). Reprinted (adapted) with permission from [17]. Copyright 2011 American Chemical Society.

1.5 Thesis Outline

This dissertation aims to replace the high-temperature diffused p-n junctions in silicon solar cells with low-temperature deposited amorphous titanium dioxide/silicon (TiO_2/Si) heterojunction while maintaining high power conversion efficiencies at low cost.

Chapter 2 discusses the deposition of TiO_2 films using a chemical vapor deposition method, how to manipulate layer thickness and characterization of the TiO_2.

In chapter 3, the importance of surface passivation is explained, different passivation methods (annealing) are explored, the interface chemistry behind the annealing steps are investigated and the annealing method is put to the test in an actual double-heterojunction device with the annealed TiO_2 forming the backside electron-selective contact.

Chapter 4 discusses the different current mechanisms that occur across a TiO_2/Si interface. Notably, it is seen that the ideal injected minority carrier current dominates

for 4 nm thick TiO_2/p-Si diodes. Furthermore, a new measurement method, the heterojunction bipolar transistor (HBT), is discussed. The HBT method is used to measure the exact quantities of the majority carrier current components.

Chapter 5 develops an analytical model to understand the interplay of variables that determine the hole current in the TiO_2/p-Si diode. The analytical model shows that the actual TiO_2/Si valence band offset plays an insignificant role once it exceeds 0.4 eV. Furthermore, it is the workfunction of the metal that matters first and foremost, as the Si surface is depinned by the TiO_2 layer. The other key parameter is the quality of the TiO_2/Si interface. Experimental data corroborates this, furthermore it shows that for both 250 °C annealed samples and TiO_2 layers thicker than 4 nm, negative charge bends the band up, thus increasing the current.

And finally, Chapter 6 summarizes this dissertation and explores avenues of future work, including improved passivation methods, the development of transparent conductive contacts for the TiO_2/Si heterojunction, and the use of TiO_2/Si as a selective contact for an interdigitated backcontact (IBC) solar cell structure or an interface layer between silicon and perovskite materials.

Chapter 2

Amorphous TiO_2 Growth and Characterization

2.1 Introduction

The first step in developing a TiO_2/Si heterojunction as a hole-blocking, electron-selective contact is to establish a reliable and low-cost deposition process that has the potential to scale. Second is to characterize the film deposited to ensure it is indeed TiO_2 being grown and to see if the band offsets align with what is needed for an electron-selective contact. Both points are addressed in this chapter.

The work in this chapter was largely published in [19,20]. Collaborators included Sushobhan Avasthi (basic growth and current-voltage measurements) and Gabriel Man (characterization and spectroscopy). I was primarliy responsible for rebuilding the growth system to grow thicker TiO_2 layers - through accommodating a larger bulb, and installing a throttle butterfly valve between the precursor vial and the chamber.

TiO_2 is a transition metal oxide, a type of semiconductor. Also called titania, its three main forms are the minerals anatase, rutile and brookite. TiO_2 has many

applications, including as white pigment, UV blocker in sunscreen, optical coatings, catalysts, sensors and photo-electrochemical water-splitting [21–24].

2.2 Deposition

TiO_2 is typically deposited using an atomic layer deposition (ALD) method [25–32]. This work uses a similar deposition process - as one can deposit nanometer thick layers using an adsorbed precursor. There are two differences that need to be stated: First, unlike ALD, the process used in this work does not utilize a second reactant, such as water, to react with the Ti precursor to form titanium dioxide. The precursor used is the metal-organic titanium(IV) tetra-(tert-butoxide) or $Ti[OC(CH_3)_3]_4$, which is shown in Figure 2.1 [33], and contains both the Ti and O atoms of the TiO_2. The precursor is liquid at room temperature. This simplifies the deposition system, in that no bubblers or high-speed isolation valves are required. Second, unlike ALD precursors, such as titanium tetrachloride, titanium(IV) tetra-(tert-butoxide) is not intrinsically self-limiting. This leads to a deposition regime where more than one monolayer can be deposited in one cycle. Due to the two differences, our deposition process is better described as a modified CVD process. The process also differs because of the relatively low-temperatures used; the maximum temperature reached is 100 °C, in contrast to conventional CVD of TiO_2 which can reach 275 °C to 675 °C.

In concept the TiO_2 deposition system is very simple and involves a minimal number of components, as illustrated in Figure 2.2 and Figure 2.3. The main chamber has a temperature-controlled stage: a thermoelectric device is attached to the bottom of the stage and is used for the heating and cooling. A mechanical roughing pump is connected to one end of the chamber through a pump valve. On the other end, a valve connects the chamber to a vial with the precursor liquid. The surface area

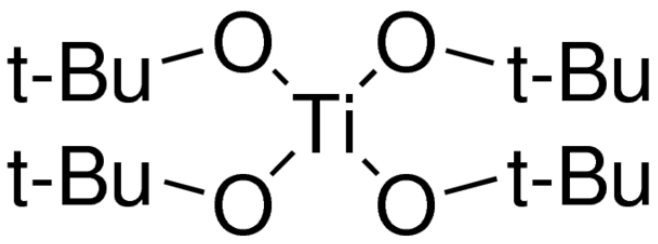


Figure 2.1: Precursor molecule: titanium(IV) tetra-(tert-butoxide) - Reprinted with permission from [33]

of the precursor vial was 3 cm^2. The main chamber also has inlet/outlet lines for the cooling water (seen in Figure 2.3), a nitrogen inlet for venting purposes (seen in Figure 2.4), and a window for observation of samples during depositions.

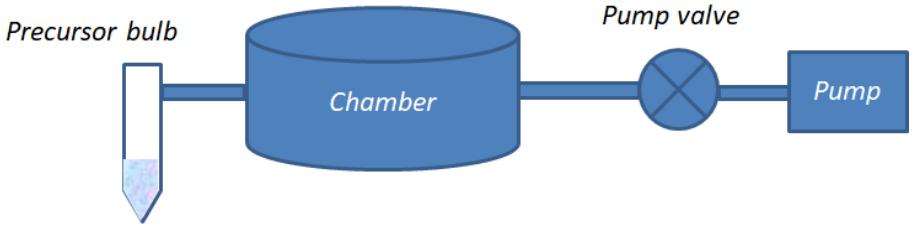


Figure 2.2: Diagram of TiO_2 deposition chamber

The fabrication sequence begins with cleaning of an electronic-grade, polished silicon sample. The cleaning process involves a solvent cleaning procedure and the standard RCA clean with RCA-1 (5:1:1 H_2O:H_2O_2:NH_4OH) and RCA-2 (5:1:1 H_2O:H_2O_2:HCl) steps. Right before placing the samples in the TiO_2 deposition chamber, a dip in 20:1 H_2O:HF acid for 1 minute is performed to remove any oxides and to form a hydrogen-terminated silicon surface. After samples are placed in the chamber, it is pumped down to a base pressure of 30 mtorr and the chamber remains pumped for the remainder of the deposition.

The deposition process consists of cycles, each cycle in turn consists of an adsorption and a thermolysis step as shown in Figure 2.5. The pump valve is opened at

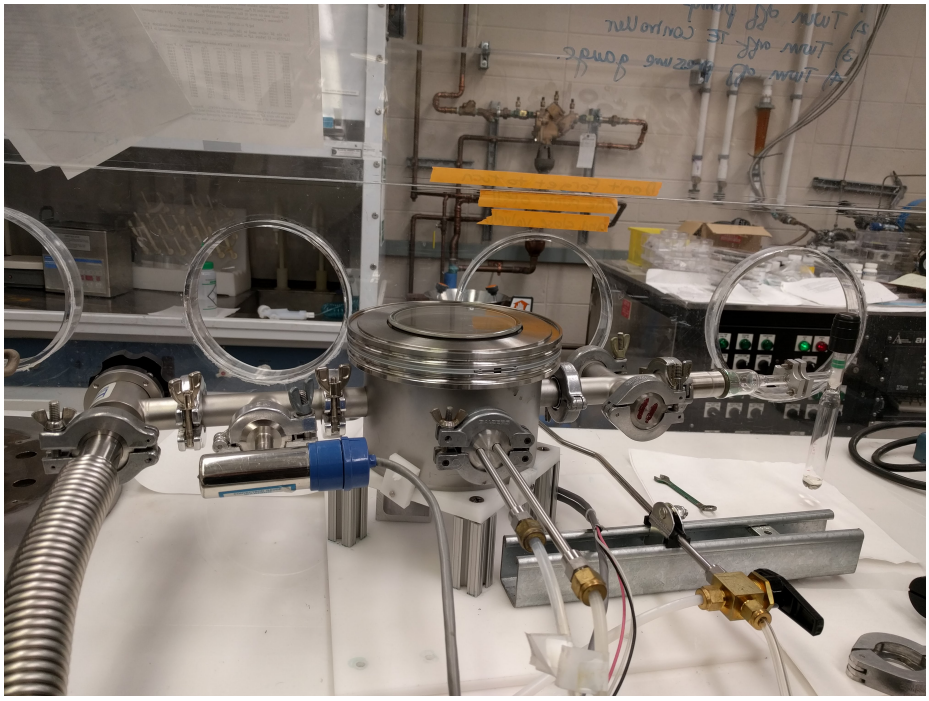


Figure 2.3: Sideview of TiO_2 deposition chamber, TiO_2 precursor bulb is on the right side, pump valve is on the left side. The cooling water lines for the thermoelectric device are in the center

the beginning of each deposition, reducing the chamber pressure from atmospheric pressure to a base pressure of 30 mTorr. The chamber is under this base pressure throughout the entire deposition, and the pump valve is closed only before de-loading samples. During the adsorption step, the samples are first cooled by the thermoelectric stage to -10 °C (cooling takes approximately 6 minutes). The samples are then exposed to vapor from the precursor vial. Typically, in the first cycle, the chamber pressure rises to 50 mTorr for 30 seconds, before dropping back down to 30 mTorr. This is due to air or precursor gas that may be in the vial getting pumped into the chamber at the opening of the precursor vial valve. The standard duration of the adsorption step used is 10 min. The cooling of the sample stage facilitates adsorption of a thin layer of the precursor on the samples. Because the precursor adsorbs on the stage as well, a thin layer of precursor also wicks underneath the samples, so that adsorption occurs on both sides of the sample. The growth process is not performed one

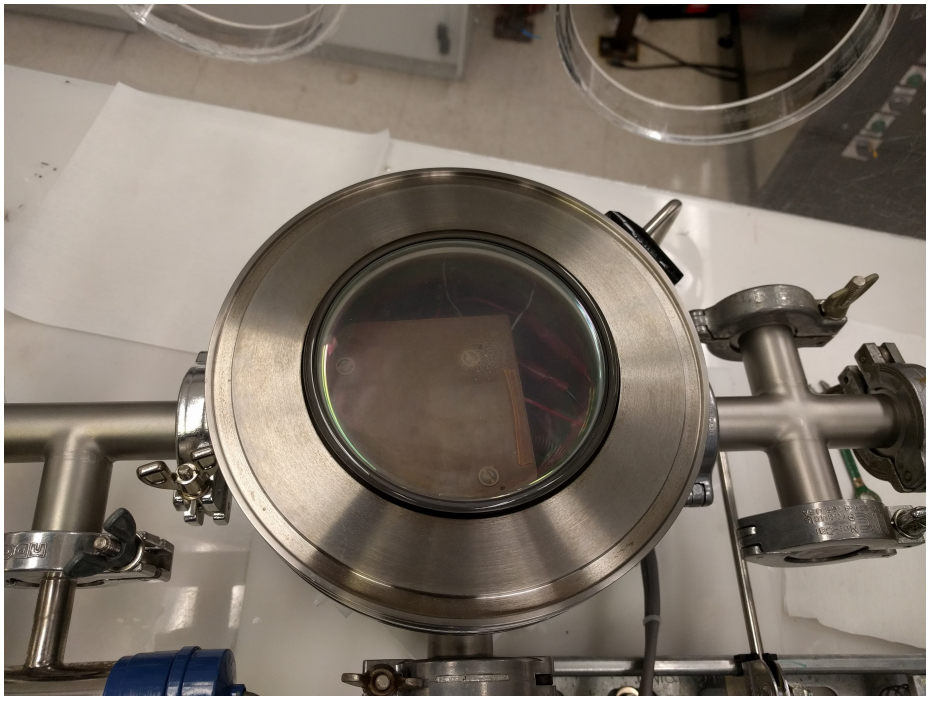


Figure 2.4: Topview of TiO_2 deposition chamber, showing looking window and sample chuck. Nitrogen valve is at the top right of the chamber.

atomic layer at a time, in contrast to ALD, because more than one monolayer of the precursor is adsorbed onto the sample during the cooling step. After adsorption, the stage is heated to 100 °C. The heating takes approximately 5 minutes. Once 100 °C is reached, the precursor is thermolyzed for 10 minutes. This thermolysis step serves to break the iso-butene from the titanium, leaving hydroxyl groups that condense to give a stoichiometric TiO_2 film after elimination of water. TiO_2 is thus formed on both sides as the precursor adsorbs to both sides of the sample. Often one side will be scribed to ensure an ohmic metal/Si contact instead of a metal/TiO_2/Si contact. The standard deposition in this thesis uses three cycles. One cycle takes 32 minutes. Going down from the final thermolysis step to room temperature to de-load samples takes another 5 minutes. The standard 3 cycle deposition results in a film thickness of 4 nm. TiO_2 thickness was measured by a J.A. Woollam spectroscopic ellipsometer and the data was fitted to a vendor-supplied Tauc-Lorentz oscillator model.

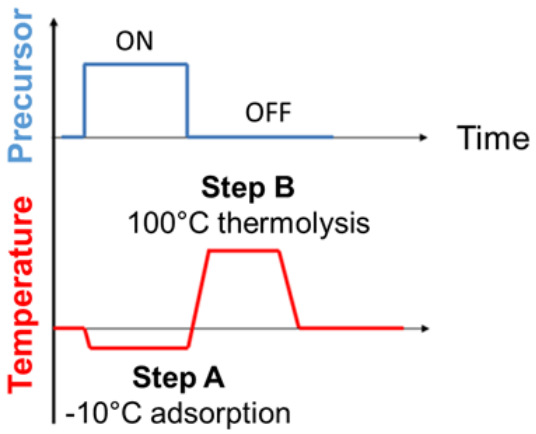


Figure 2.5: Diagram of TiO_2 deposition cycle: adsorption step at -10 °C followed by thermolysis step at 100 °C

However as shown in Figure 2.6, there appears to be a limiting factor to TiO_2 growth relative to number of cycles: increasing the number of deposition cycles offers a slight increase in thickness. Yet the change is not linearly proportional to the number of cycles; 6 and 9 cycles do not offer significant increases in thickness. One possibility is that the TiO_2 layer is porous and further cycles only fill the gaps. Another possibility is that after one cycle, where the hydrocarbons break off, there is very little for the precursor to react with in future cycles. Thus the precursor does not stick well to the TiO_2 layer.

To increase the TiO_2 layer thickness, two variables were investigated: (a) the adsorption temperature and (b) the TiO_2 precursor bulb size.

2.2.1 Effect of Adsorption Temperature

As mentioned previously, the TiO_2 precursor does not adsorb well at room temperature. Hence an adsorption temperature of -10 °C has been used in our standard deposition cycle of (a) adsorption temperature at -10 °C and (b) thermolysis temperature of 100 °C. Adsorption temperatures of -15 °C and -20 °C were investigated as well. The idea was to see if a lower adsorption temperature would result in more

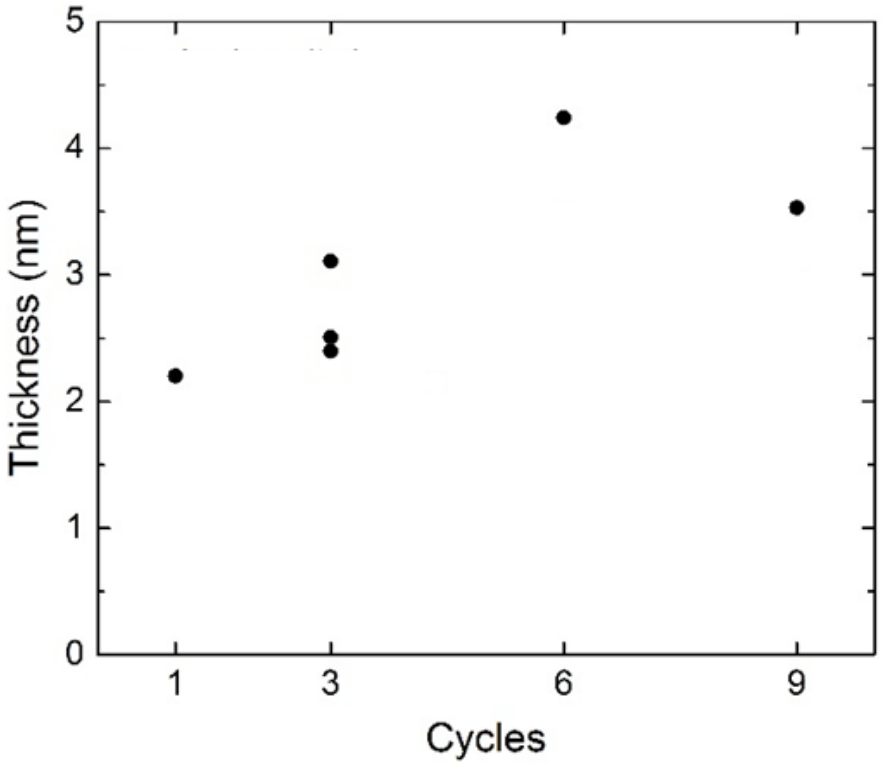


Figure 2.6: TiO_2 thickness versus number of cycles

adsorption and thus a thicker TiO_2 layer. Figure 2.7 shows the results: both -15 °C and -20 °C show a slight decrease in thickness, while . These changes can easily be explained by sample-to-sample variation. Overall no significant changes in the thickness (i.e. several nm) were observed.

2.2.2 Effect of Bulb Size

The precursor bulb was replaced in order to increase the surface area of the precursor liquid (to increase the evaporation rate of the precursor) and to increase the smallest cross section (to increase the flow rate of the precursor). Figures 2.8 and 2.9 show the old (glass) and new (glass-steel) bulbs respectively. For the glass bulb, the liquid surface area was 0.31 cm^2 and the smallest cross section was 0.034 cm^2. The glass-

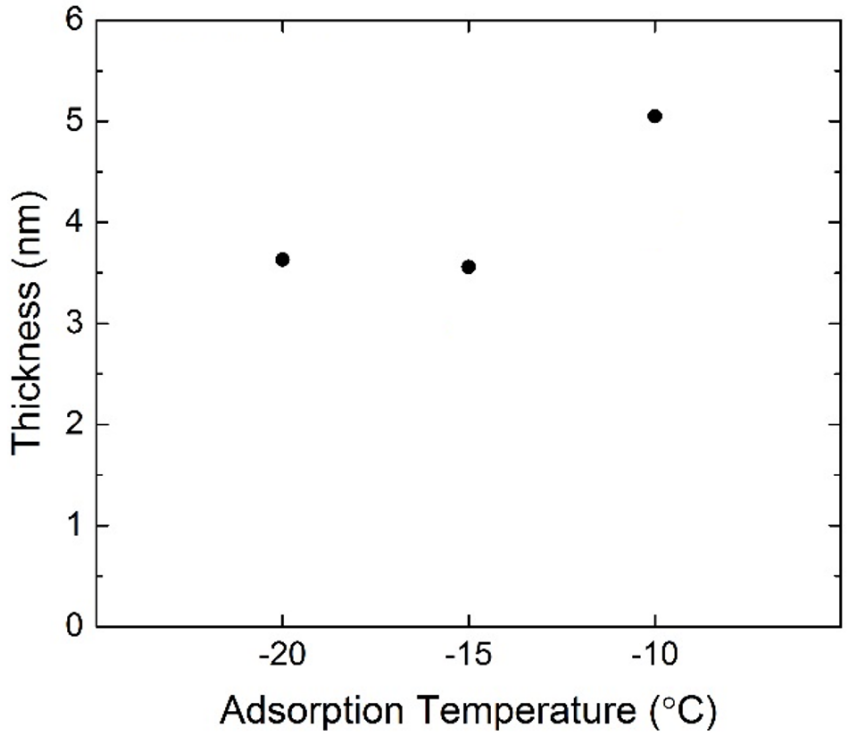


Figure 2.7: Minimal effect of adsorption temperature on thickness of TiO_2 layer

steel bulb, on the other hand, had a liquid surface of 0.94 cm^2 (arrows at the bottom) and smallest cross section of 0.053 cm^2 (arrows near steel).

The larger areas allow for more precursor to enter the chamber. Initially, the formation of spots was observed as shown in Figure 2.10. As the precursor adsorbed onto the chuck and samples, one can visibly notice a liquid layer of the precursor coating everywhere. This visible coating did not appear when using the smaller glass bulb. It is hypothesized that the larger cross-sectional and liquid surface area enable more precursor gas to flow into the chamber and get adsorbed. As the chuck is heated however, the liquid starts evaporating. After all, the main reason for adsorbing at -10 °C was because the precursor did not adsorb well at higher temperatures. With the larger bulb, despite the evaporation while heating, enough precursor remains on the silicon surface to grow TiO_2. The spots in Figure 2.10 range from 30 - 80 nm in

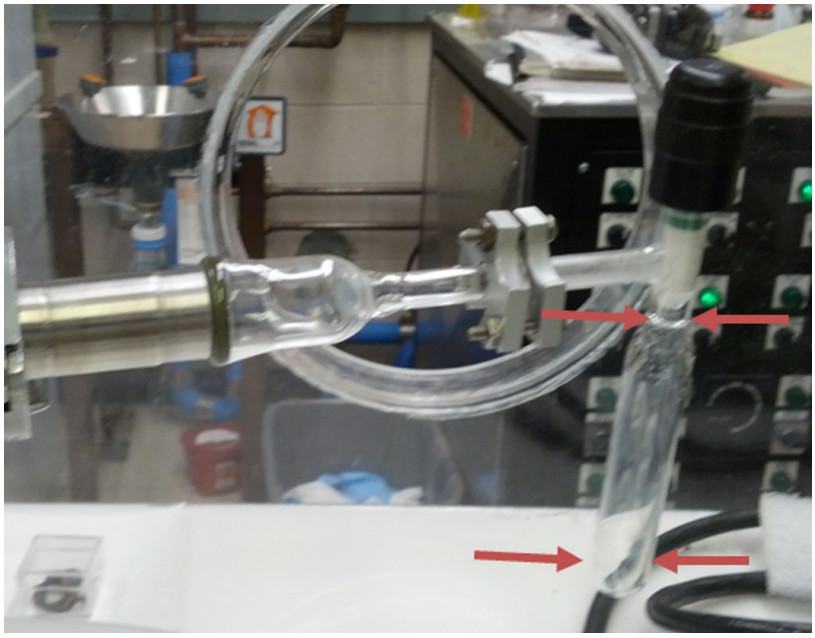


Figure 2.8: Old glass bulb with liquid surface area of 0.31 cm^2 (arrows at the bottom) and smallest smallest cross section of 0.034 cm^2 (arrows near top of bulb)

thickness, after a 3 cycle deposition. Thus the self-limiting problem was due to not enough precursor being adsorbed before heating.

The use of a butterfly valve (Figures 2.11 and 2.12) enabled control of flow rate. After incorporating the butterfly valve, spots were reduced as shown in Figure 2.13a when the butterfly valve is completely open (angle of 90°).

Figures 2.13b and 2.13c show what happens as the butterfly valve is closed to an angle of 60° and 30°. At an angle of 30° no more visible spots were observed.

The combination of the glass-steel bulb and butterfly valve enabled growth of thicker layers. Initial runs gave 4.7 nm for 3 cycles, 7.1 nm for 4 cycles and 12.1 nm for 6 cycles as seen in Figure 2.14. Important to note is that despite the use of a butterfly throttle valve to reduce the amount of precursor adsorption and spotting, there is still more precursor adsorbed compared to the small glass bulb. This enables one to grow thicker layers in a controlled fashion.

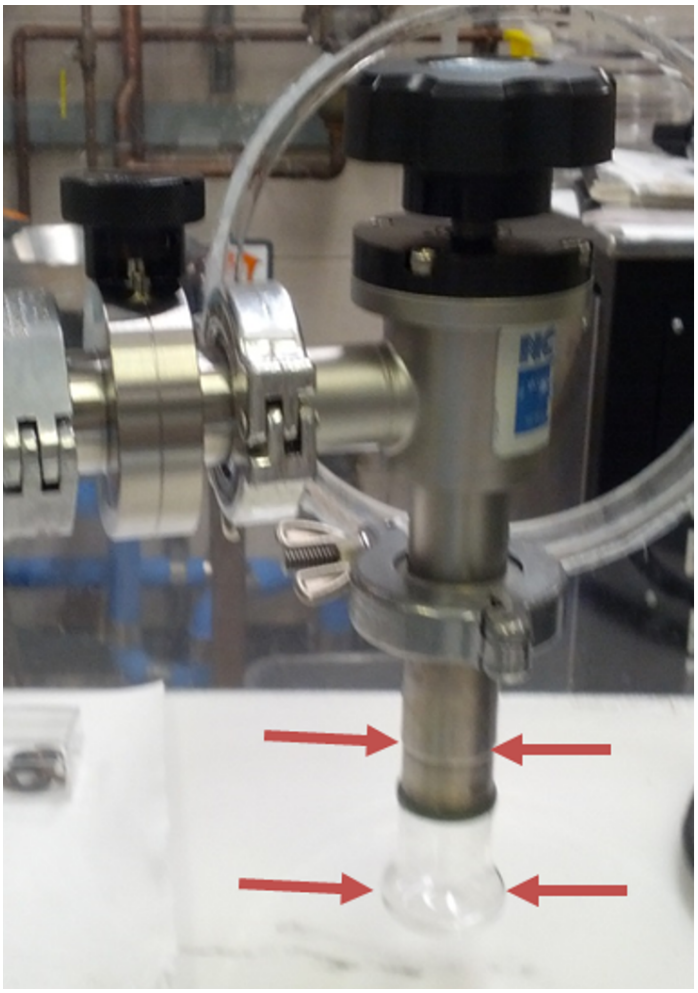


Figure 2.9: New glass-steel bulb with liquid surface area of 0.94 cm^2 (arrows at the bottom) and smallest smallest cross section of 0.053 cm^2 (arrows near steel)

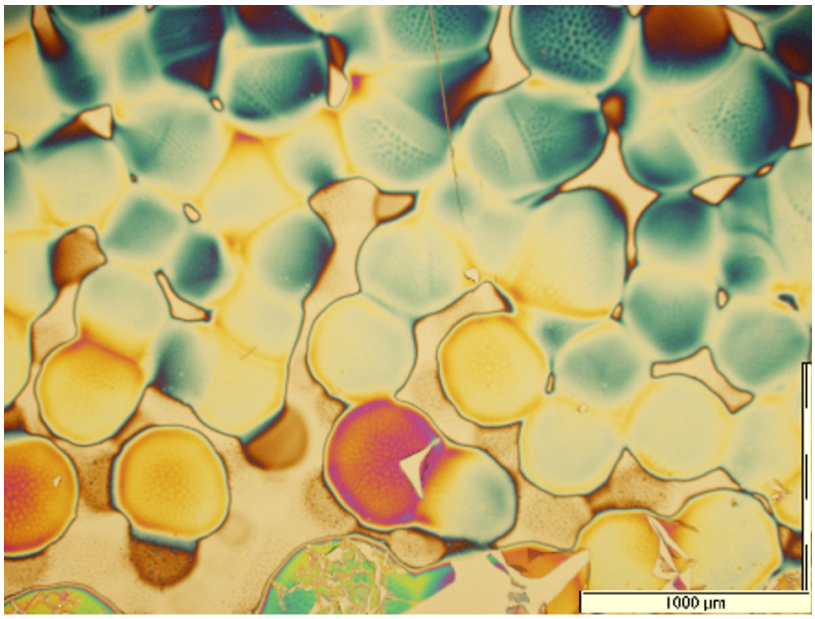


Figure 2.10: Spots due to larger bulb area

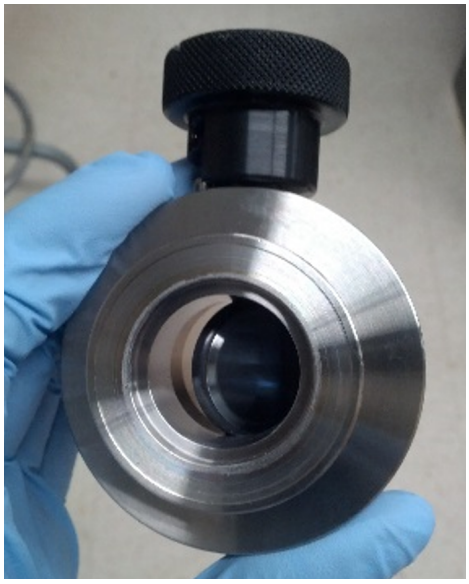


Figure 2.11: Butterfly valve: to be placed between precursor bulb and chamber inlet

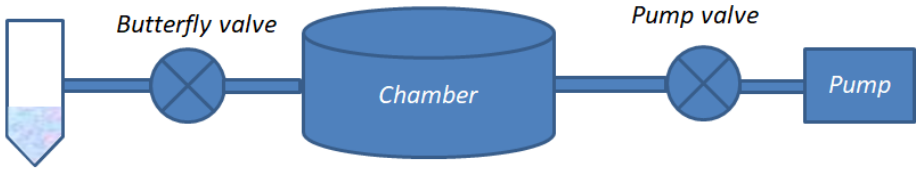
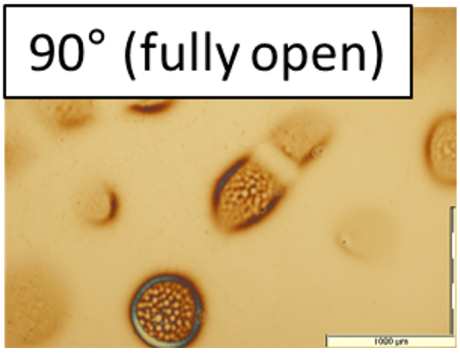
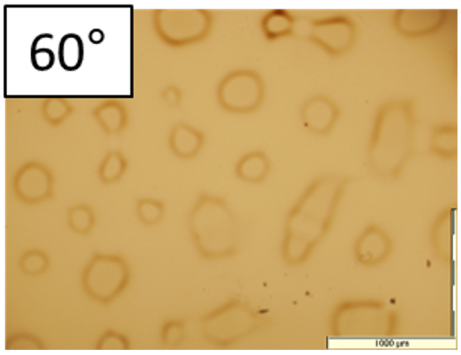


Figure 2.12: New diagram of TiO_2 deposition chamber incorporating butterfly valve



(a)



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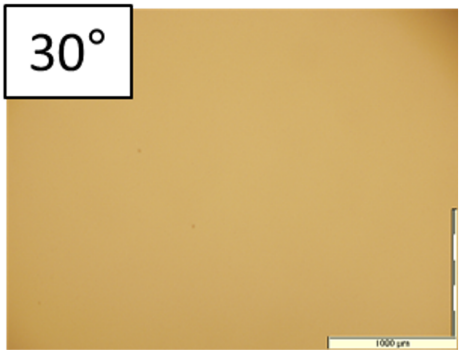


(c)

Figure 2.13: TiO_2 spots with butterfly valve at an angle of (a) 90° (b) 60° and (c) 30°. Note there are no visible spots for an angle of 30°.

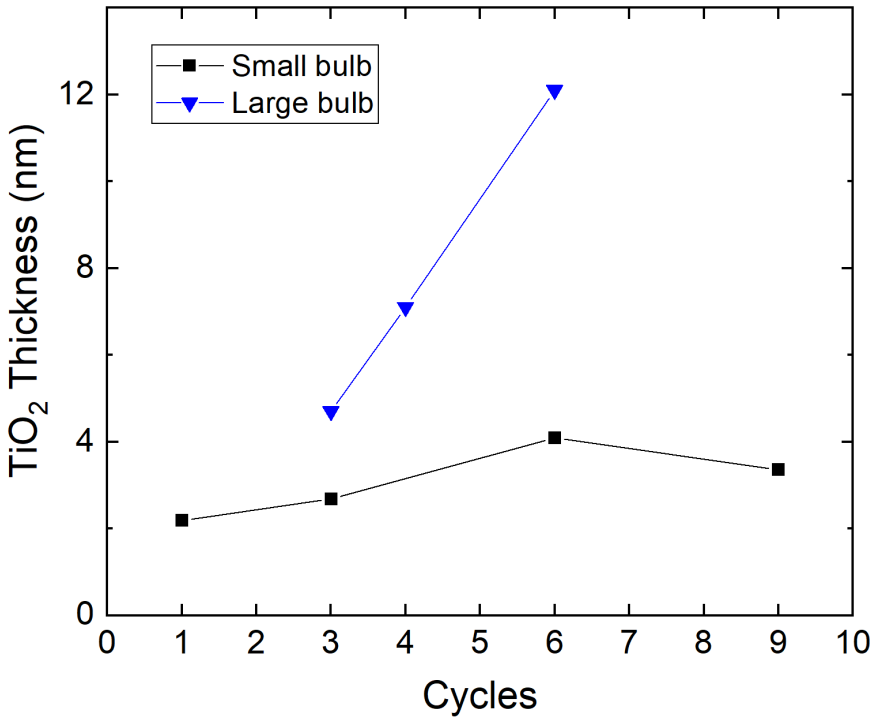


Figure 2.14: TiO_2 thickness versus number of cycles, for both the small glass bulb and the large glass-steel bulb, indicating larger bulb is effective at growing thicker TiO_2 layers

2.3 Characterization of TiO_2 layer

2.3.1 Surface Morphology

Figure 2.15 shows an atomic force microscopy (AFM) image taken of a 12 nm thick TiO_2 layer on top of silicon. The RMS value is 0.84 nm, indicating a very smooth layer. One can imply the layer is amorphous as no visible grain boundaries can be seen.

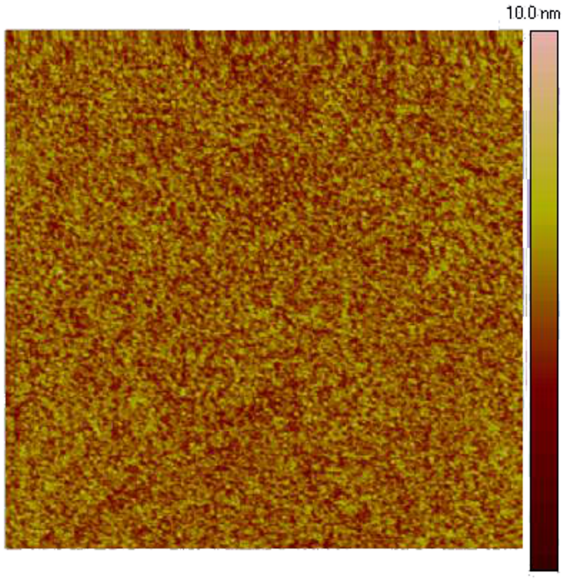


Figure 2.15: AFM image of TiO_2 surface

2.3.2 Stochiometry

X-ray photoelectron spectroscopy (XPS) was used (in collaboration with Gabriel Man) to test if the deposited layer is indeed TiO_2. Experiments were conducted with an Al kα radiation source (1486.6 eV), 0.5 eV resolution, on a highly-doped p^+ Si (100) wafer (< 0.005 Ohm cm) coated with 3 nm thick TiO_2 film [34, 35].

The Ti 2p3/2 peak for TiO^{4+} in TiO_2 generally lies in the range of 458.6 - 459.2 eV, while the Ti 2p3/2 peaks for TiO^{2+} and TiO^0 lie in the ranges 454.9 - 455.2 eV

and 453.7 - 454.2 eV respectively [9]. The Ti 2p3/2 peak location in Figure 2.16 is at 459.7 eV, demonstrating it corresponds to TiO^{4+}. Additionally, a Ti 2p1/2 peak location is at 465.3 eV, implying a spin-orbit splitting of 5.6 eV, a value which lies much closer to the spin-orbit splitting of TiO^{4+} (5.5 eV) than to the spin-orbit splitting of TiO^{0} (6.2 eV) [9]. The intensities of the peak at 459.7 eV and 465.3 eV have a ratio of 2.2:1, close to the branching ratio of 2:1 expected for the 2p lines. Overall, the Ti 2p spectrum confirms the presence of TiO^{4+} species (from TiO_2) on the silicon surface.

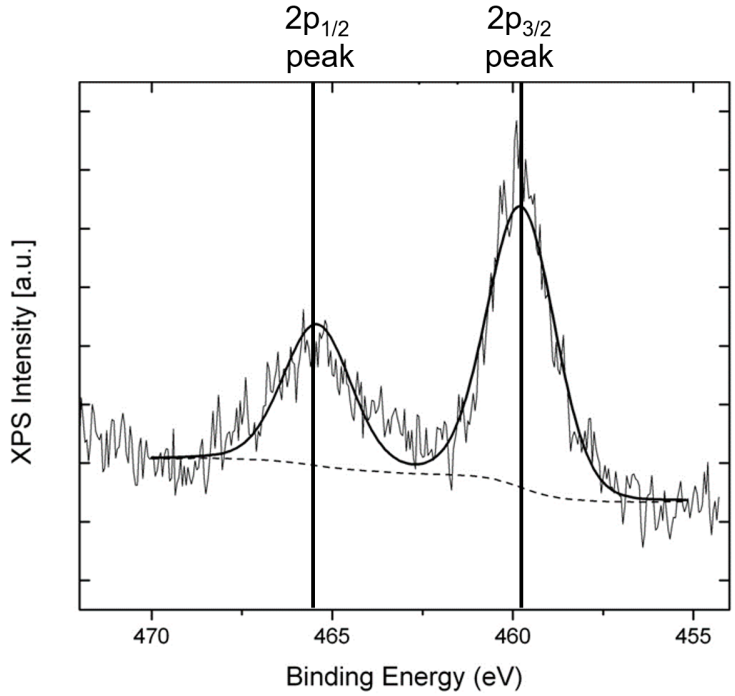


Figure 2.16: XPS Ti peaks with Ti 2p3/2 peak location at 459.7 eV and Ti 2p1/2 peak location is at 465.3 eV. Reproduced from [19], with the permission of AIP Publishing.

2.3.3 UPS/IPES - Bandgap

TiO_2 tends to be an n-type material, due to doping by oxygen vacancies (deep donors) [36, 37] and/or doping by titanium interstitials (shallow donors) [38, 39].

It is crucial to know the positions of the TiO_2 valence and conduction band edges relative to silicon, in order to ensure an electron-selective contact can indeed be formed. To establish these numbers, photoelectron spectroscopy (PES) techniques were used (in collaboration with Gabriel Man).

The valence band edge location and workfunction are determined utilizing ultraviolet photoemission spectroscopy (UPS). UPS works on the basis of exciting electrons from the material. The kinetic energy and number of excited electrons are measured and from that data, the binding energies of said excited electrons is determined. The binding energies in turn give information on the electron states in the material, allowing one to find the valence band edge.

Inverse photoemission spectroscopy (IPES) is used to measure the conduction band. In contrast to UPS however, electrons of known kinetic energy are targetted to the material. The electrons occupy previously unoccupied states and as they decay from higher to lower states, photons are emitted and measured. From these emitted photons, one can construct the energy levels of empty states and find the conduction band edge.

Figure 2.17 shows the combined UPS and IPES scans. This is confirmed here by the position of the Fermi level (E_F) close to the conduction band minimum $E_C(TiO_2)$. The work function of as-deposited TiO_2, $\phi(TiO_2)$, measured from the photoemission cut-off (not shown here), is 4.0±0.1 eV. The valence band maximum $E_V(TiO_2)$ is at 3.2 eV below E_F, giving an ionization energy of 7.2 ±0.2 eV. Conversely, E_C (TiO_2) is at 0.2±0.2 eV above E_F, giving an electron affinity (E_A) of 3.8±0.3 eV and a band gap of 3.4±0.3 eV

The band offsets vis-a-vis silicon is shown in Figure 2.18. As can be seen, there is a very small (< 0.2 eV) δE_C, and a large (approximately 2.1 eV) δE_V, leading one to conclude the band offsets are what one would hope for a electron-selective heterojunction contact.

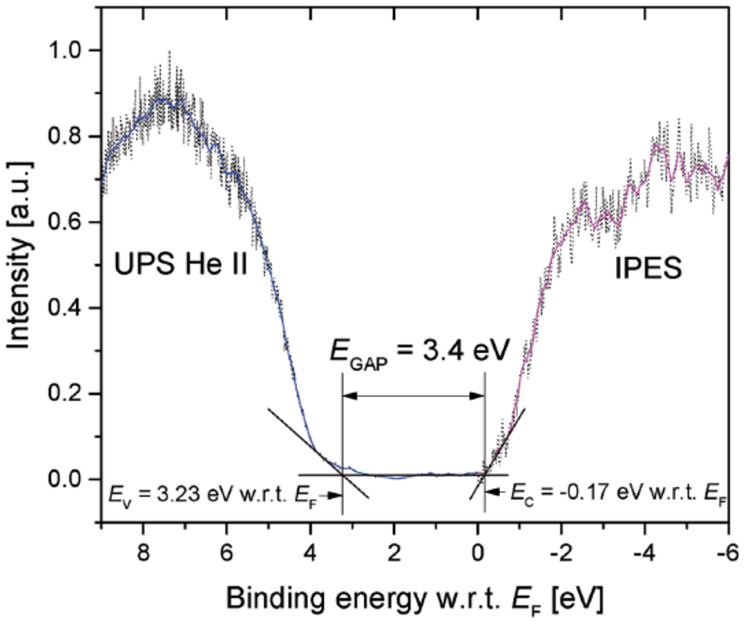


Figure 2.17: Combined UPS/IPES scans, showing a bandgap of 3.4eV. Reprinted with permission from [40]. Copyright 2016 John Wiley and Sons.

2.3.4 Voltage-Current Characteristics

Now that there is confirmation of a very small conduction band offset, a large valence band offset, stochiometric and amorphous TiO_2, the next step would be to test current-voltage (I-V) characteristics to see if TiO_2 on Si indeed forms an electron-selective contact or not. TiO_2 on p-Si would block the majority carrier current component (holes) and one would expect a diode-like behavior. TiO_2 on n-Si, on the other hand, would allow the majority carrier current component (electrons) to travel without impediment from silicon to metal and one would expect ohmic behavior.

TiO_2/Si diodes were fabricated, both on n-type and p-type silicon (doping for both of $1x10^{15}$ cm^{-3}). The device structure in shown in Figure 2.19. The top and bottom electrodes are deposited by thermal evaporation. The top electrode was made of Al. The bottom electrode was an ohmic Ag/Si contact. The device area was $3.14x10^{-2}$ cm^2. As can be seen in Figure 2.20, TiO_2 on p-Si indeed forms a diode, while TiO_2

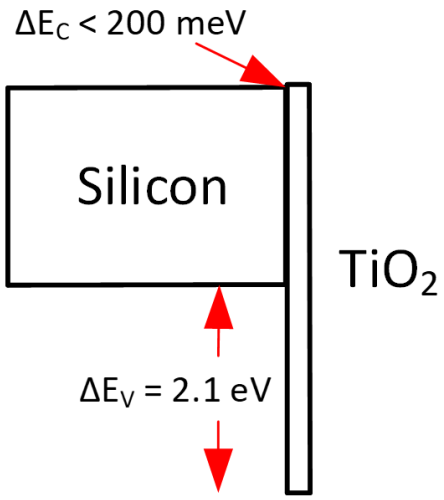


Figure 2.18: TiO_2/Si band offsets based on UPS and IPES measurements. Ideal interface with no dipoles are assumed.

on n-Si forms an ohmic contact. This implies that holes are being blocked, while electrons can pass through the TiO_2/Si interface. Additionally, a control device with no TiO_2 on p-Si was also fabricated. In contrast to the device with TiO_2, no TiO_2 on p-Si leads to an ohmic contact.

To further confirm the hole-blocking characteristics of the Si/TiO_2 interface, diodes were fabricated with TiO_2 layers 1nm, 2 nm and 4 nm thick and I-V characteristics were measured under dark and light. The Al top contact was kept intentionally thin (15 nm) so that 50% of the light can go through and be absorbed in silicon.

The I-V characteristics under dark are shown in Figure 2.21. As the TiO_2 layer gets thicker, the hole-blocking behavior becomes more effective and we see a more diode-like behavior.

The AM 1.5G response of these devices is shown in Figure 2.22. The device without a TiO_2 layer behaves as a resistor because of insufficient hole blocking - as Al/p-Si forms an ohmic contact. With a 1nm TiO_2 layer, holes from the p-Si are blocked, and we measure a short-circuit current and an open-circuit voltage.

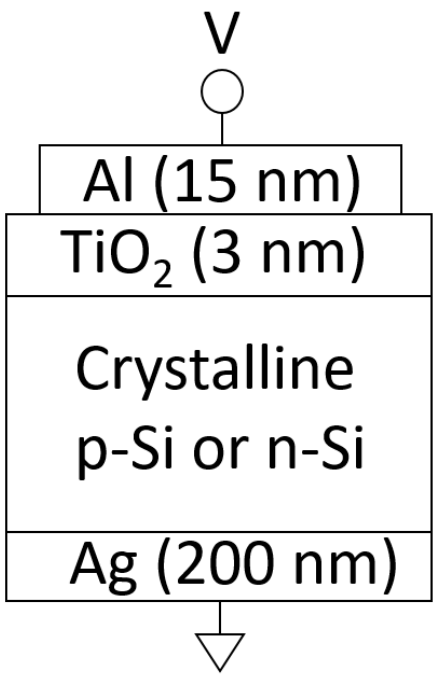


Figure 2.19: Device structure for TiO_2/Si device

By gradual increase in the TiO_2 layers thickness, from 2 to 4 nm, tunneling and pinholes are reduced, leading to more effective hole blocking, a lower J_0-value and thus resulting in higher values for V_{OC} and I_{SC}. At 4nm we obtain V_{OC} of 0.52 V, J_{SC} of 19.3 mA/cm2 and fill factor of 70%, which translates to a power conversion efficiency of 7.1% At this point, the efficiency is primarily limited by the absorption losses in the semi-transparent top metal.

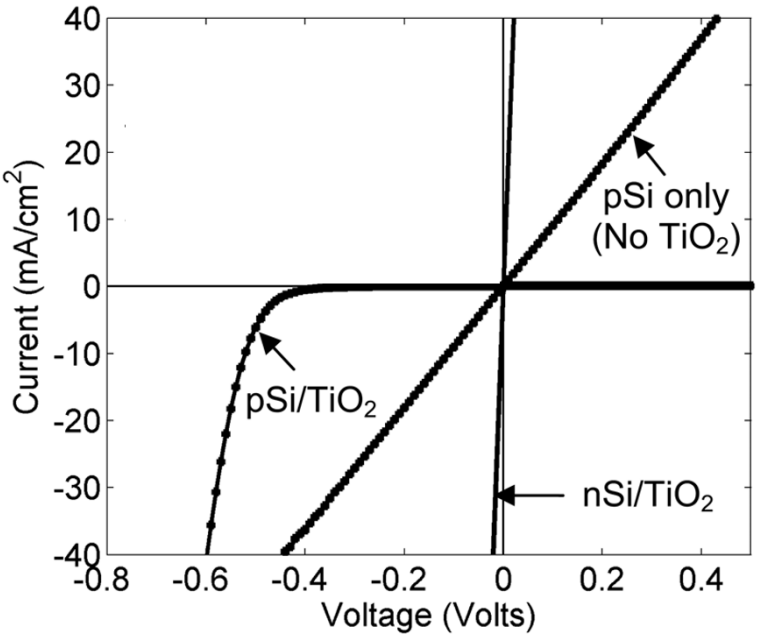


Figure 2.20: I-V TiO_2/pSi and TiO_2/n-Si devices. Reproduced from [19], with the permission of AIP Publishing.

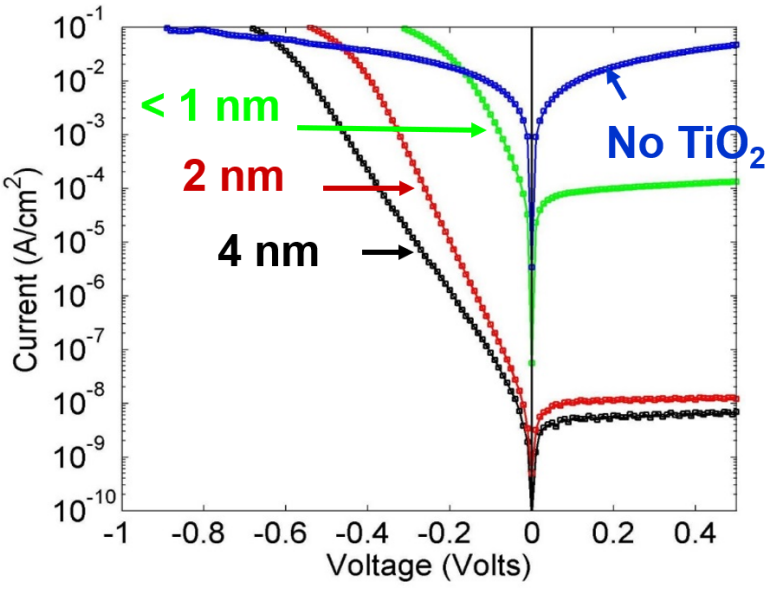


Figure 2.21: I-V under dark for TiO_2/p-Si for different thicknesses (courtesy of Sushobhan Avasthi)

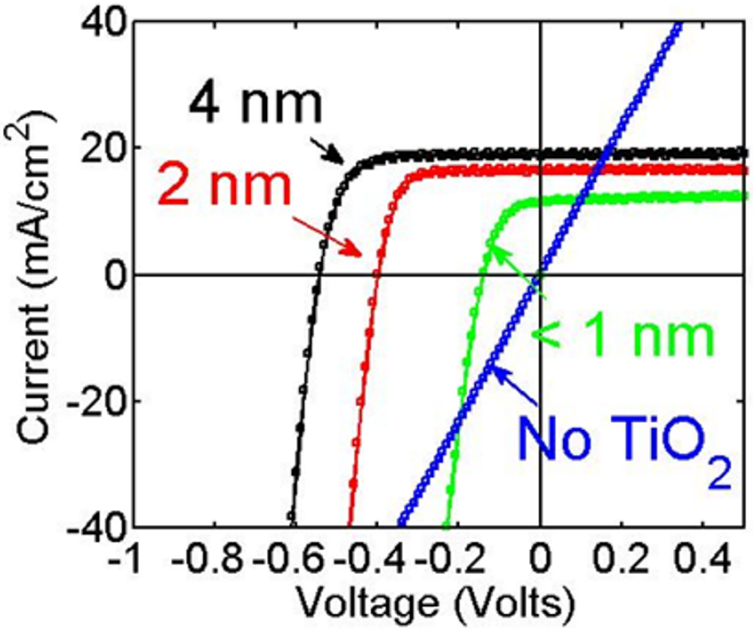


Figure 2.22: I-V under light (AM 1.5G) for TiO_2/p-Si for different thicknesses (courtesy of Sushobhan Avasthi)

2.4 Conclusion

In conclusion, a new method to deposit amorphous titanium dioxide was established: a modified CVD process, with only one precursor molecule (titanium tert-butoxide) consisting of two steps, an adsorption step at -10 °C and a thermolysis step at 100 °C. It was further determined that the bulb size has an effect on the ability to grow thicker TiO_2 layers (> 4nm).

In terms of characterization, it was determined the deposited material was indeed amorphous, stochiometric TiO_2. The bandgap was 3.4 eV, with a very small conduction band offset (< 0.2eV) and a large valence band offset (2.1 eV) for the TiO_2/Si interface. I-V measurements for TiO_2/Si devices showed that the heterojunction is a hole-blocking, electron-selective contact.

Chapter 3

Measurement and Optimization of TiO_2 Interface Properties

3.1 Introduction

So far a new deposition method has been demonstrated and the deposited TiO_2 has been characterized as having a small conduction band edge and a large valence band edge offset. The I-V characteristics of simple TiO_2/Si devices corroborated the band offsets. This chapter focuses on the TiO_2/silicon interface, in other words, specifically the number of silicon defect states at the silicon surface, how they affect interface recombination, and how to reduce the interface defect density by annealing.

The work in this chapter was largely published in [20, 41, 42]. Collaborators included Girija Sahasrabudhe (interface chemistry and XPS data) [43].

3.2 Modelled Effect of TiO_2/Si Interface Recombination on Solar Cell Performance

A single-sided PEDOT/Si device (with no TiO_2) is displayed in Figure 3.1. PEDOT, also known as PEDOT:PSS, is the organic polymer poly(3,4-ethylenedioxythiophene) poly (styrenesulfonate) (PEDOT:PSS) and is p-type doped. The PEDOT/Si interface, which replaces the front-side p+/n junction of a conventional Si solar cell, acts as a hole-selective contact, blocking electrons while being transparent to holes. Furthermore, due to the high work-function of the PEDOT, there is a depletion region in the silicon which collects photogenerated carriers. Because the electron dark current (majority carriers) is blocked by the PEDOT/Si interface, the dark current is now dominated by the hole dark current (minority carriers).

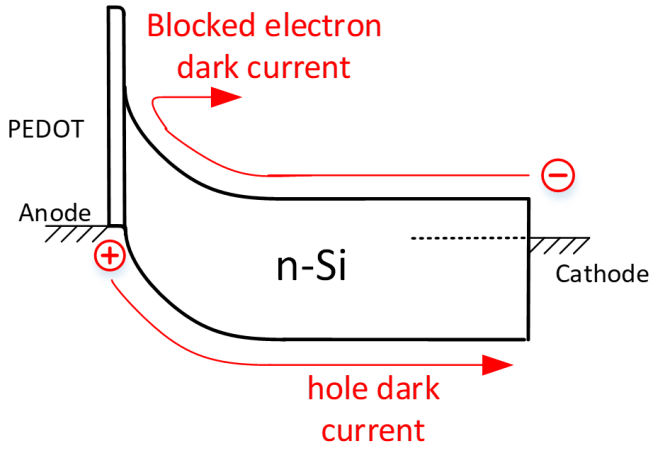


Figure 3.1: Single-sided PEDOT/n-Si device

One can get further improvement by creating a double-sided heterojunction: with the electron-selective TiO_2 deposited on the backside (Figure 3.2), replacing the backside n^+/n junction in a conventional solar cell, the hole dark current is blocked. This leads to a further reduction in the dark current and thus an increase in the open-circuit voltage.

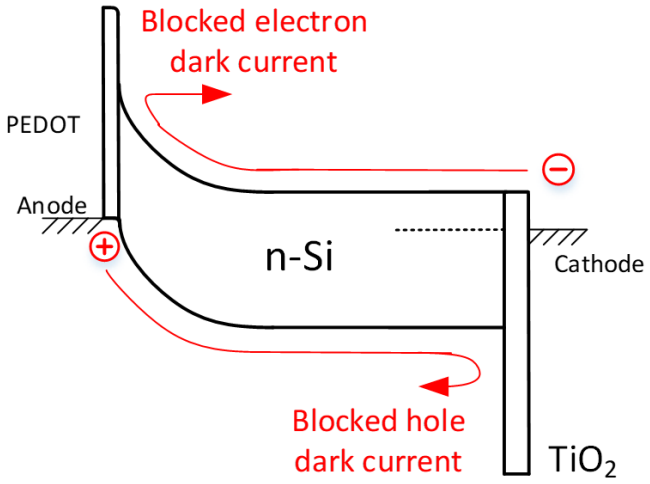


Figure 3.2: Double-sided PEDOT/n-Si/TiO_2 device

To obtain the highest possible efficiency for the crystalline-Si/TiO_2 heterojunction, a fundamental understanding of the interface quality is important. An unpassivated silicon surface has dangling silicon bonds, which lead to midgap defects and Fermi level pinning. The former degrades device performance by reducing the effectiveness of the hole-blocking TiO_2 layer - if holes can recombine at the Si surface then TiO_2 is no longer relevant. The latter degrades device performance by adversely affecting the open-circuit voltage. Hence it is critical to characterize surface defects and if necessary, reduce the number of defect states

Thus, in reality, the Si/TiO_2 interface will have defect states, allowing holes to recombine and thus negating the hole-blocking functionality of the Si/TiO_2 interface (Figure 3.3).

Recombination at an interface (as seen in Figure 3.4) can be described by the Shockley-Read-Hall (SRH) formalism [44, 45]. The initial equation for the recombination rate R is:

$$R = \frac{N_{it} v_{th} \sigma_n \sigma_p (p_s n_s - n_i^2)}{\sigma_p [p_s + n_i exp(\frac{E_i - E_{it}}{kT})] + \sigma_n [n_s + n_i exp(\frac{E_{it} - E_i}{kT})]} \tag{3.1}$$

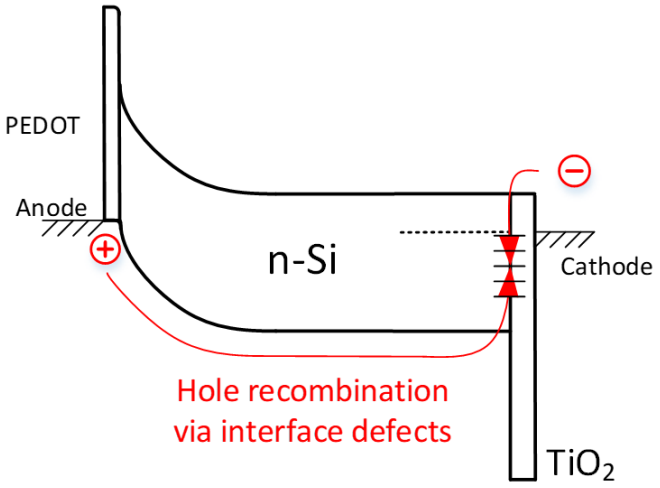


Figure 3.3: Double-sided PEDOT/n-Si/TiO_2 device with defects

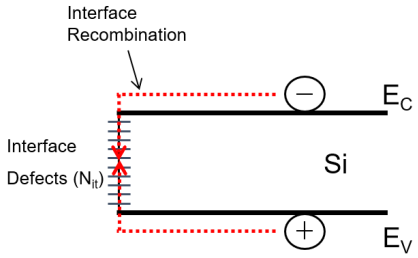


Figure 3.4: Recombination at silicon interface defects, defect density is N_{it}

σ_p and σ_n are the capture cross sections for holes and electrons respectively, p_s and n_s are the surface/interface hole and electron concentrations, N_{it} is the interface defect density, v_{th} is the thermal velocity of electrons, E_i is the intrinsic Fermi level, and E_{it} is the energy level of the interface defect recombination centers. If one assumes the capture cross sections are equal ($\sigma_p = \sigma_n = \sigma$) and the interface defects lie at midgap, one obtains the simpler form:

$$R = N_{it} v_{th} \sigma \frac{(p_s n_s - n_i^2)}{p_s + n_s + 2n_i} \tag{3.2}$$

The **surface recombination velocity** (cm/s) is represented by S_{eff} and is defined as:

$$S_{eff} \;=\; N_{it} v_{th} \sigma \tag{3.3}$$

Another term for S_{eff} is interface recombination velocity. Note that the recombination velocity is directly proportional to the number of interface defects.

If no barrier were present, the holes would recombine nearly instantly at the Si/metal interface, which has a very large defect density, and thus a near-infinite recombination velocity (found to be $\sim 10^6$ cm/s in practice). High quality Si/SiO_2 interfaces (from thermal oxide grown at 1000 °C) with forming gas annealing have Si-O-Si bonds (from SiO_2) and Si-H bonds (from forming gas anneal). These bonds significantly reduce the number of defects at the interface, such that a high quality Si/SiO_2 interface can have a recombination velocity $\sim$ 100 cm/s, with record low values $\sim$ 10 cm/s.

Simulations were done for a silicon solar cell using Sentaurus Device from Synopsys®. Sentaurus is a first-principles simulation package and solves for the Poisson equation and hole and electron continuity equations. The silicon substrate had a doping of $N_D = 2\text{x}10^{15}$ cm^{-3}, substrate bulk lifetime of 1 ms, and a thickness of 300 μm. Default parameters for silicon were used otherwise. Substrate temperature was 300 K. AM1.5G was simulated using the ASTM G173 reference solar spectrum data derived from SMARTS v. 2.9.2 [46].

The hole-selective contact at the front was set at a thickness of 5 nm, with a bandgap of 1.6 eV, both hole and electron mobilities were set at 20 $cm^2V^{-1}s^{-1}$ with the workfunction for the metal at the hole-selective contact set at 5.1 eV below vacuum.

The hole-selective contact at the front was set at a thickness of 5 nm, with a bandgap of 4.7 eV, both hole and electron mobilities were set at 1 $cm^2V^{-1}s^{-1}$ with the workfunction for the metal at the hole-selective contact set at 4.3 eV below vacuum.

The recombination velocity at the front interface was set at 0 cm/s, while the back interface recombination velocity was varied. Figures 3.5 and 3.6 shows the

effect of this back interface recombination on maximum cell efficiency (by affecting the dark current) and on the AM 1.5G current-voltage characteristics for the simulated silicon solar cell. As the recombination velocity is increased from 0 cm/s (perfectly passivated) to 10,000 cm/s, V_{OC} is reduced by 0.15 V. A small decrease in J_{SC} (due to recombination of excited photocarriers at the back interface) is also observable as s increases. Figure 3.6 shows the resulting effect on power conversion efficiency. The efficiency drops from over 24% for S_{eff} = 10 cm/s to less than 19% as s approaches 10,000 cm/s. To achieve a minimum power conversion efficiency of 20%, an S_{eff}-value of 1000 cm/s or less is desirable for the n-Si/TiO_2 interfaces. Note that lighter substrate doping requires a lower S_{eff}, whereas higher substrate doping makes the S_{eff} less critical. Surface recombination velocities less than 100 cm/s are clearly desired, with 10 cm/s as an ultimate target.

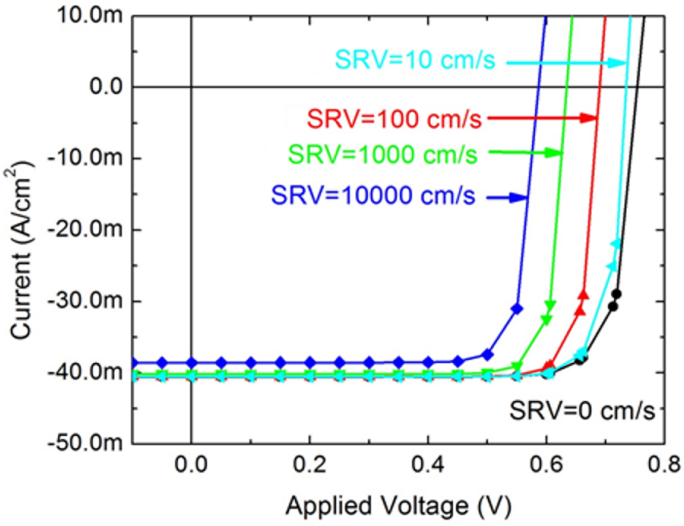


Figure 3.5: Simulated AM 1.5G I-V for different S_{eff}-values. (SRV in plot = surface recombination velocity)

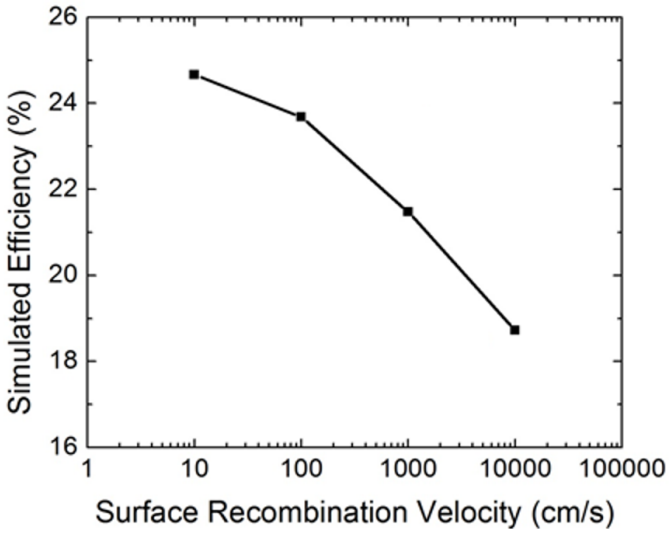


Figure 3.6: Simulated cell efficiency for different S_{eff}-values

3.3 Lifetimes and Recombination Velocities

The interface recombination velocity can be calculated by measuring the **effective minority carrier lifetime** as given by the following equation.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{S_{front}}{W} + \frac{S_{back}}{W} \tag{3.4}$$

τ_{eff} is the actual measured effective lifetime of the minority carriers, τ_{bulk} is the bulk minority carrier lifetime of the silicon substrate (for FZ wafers typically larger than 1 ms). S_{front} and S_{back} are the interface recombination velocities at the front and back Si interface respectively. W is the width of the substrate. This equation only applies if the minority carrier diffusion length is much longer than the substrate width. Or in other words, if the effective lifetime is larger than $W^2/2D$, where D is the diffusion coefficient.

Lifetimes were measured using the Sinton Instruments WCT-120 quasi-steady state photoconductance decay (QSSPCD) system. Measurements were done on 300-μm thick 2x10^{15} cm^{-3} n-type Silicon FZ wafers, with bulk lifetimes larger than 1 ms.

QSSPCD is a photoconductance decay technique that allows for the measurement of minority carrier lifetimes without the need for metallization and contacts. This enables one to quickly test minority carrier lifetimes without having to make complete devices. The WCT-120 has a Xe bulb, which generates a light flash with a slow decay time of 5 to 10 ms. The light generates photocarriers, which in turn increase the conductivity of the sample being measured. The conductivity is inductively measured using a sensor below the sample - the sensor has an area approximating a circle with a diameter of 1 inch, thus one needs to ensure a large enough sample (1 inch x 1 inch square suffices as a minimum). This setup is shown in Figure 3.7. A calibrated diode measures the flash, enabling one to measure the photogeneration rate in the sample. As the flash decays, so does the photogenerated carrier rate and thus the conductivity (Figure 3.7). From the decay of the conductivity (given by $\Delta p'/\Delta t$) and the photogeneration rate over time (G) measured from the calibrated diode, an effective minority carrier lifetime (τ_{eff}) is extrapolated for each point of measurement, which corresponds to the average excess minority carrier density (p') determined from the conductivity at that point..

3.3.1 250 °C N_2 Anneal

The standard TiO_2 deposition used was a 3-cycle deposition using the small glass bulb, unless stated otherwise. TiO_2 thickness, as stated before, was $\sim$ 4 nm for this 3-cycle deposition. The large glass-steel bulb was used for TiO_2 thicknesses larger 4 nm.

First, a high-quality thermal oxide was grown on both Si wafer surfaces at 1050 °C, with a post-oxidation forming gas anneal (FGA) at 400 °C, to passivate the surface. From the measured effective lifetime, a worst-case value (assuming an infinite τ_{bulk} and no Auger recombination at low excitation densities) of S_{eff} of 20 cm/s was extracted for both top and bottom Si/SiO_2 interfaces at an excess minority carrier density of

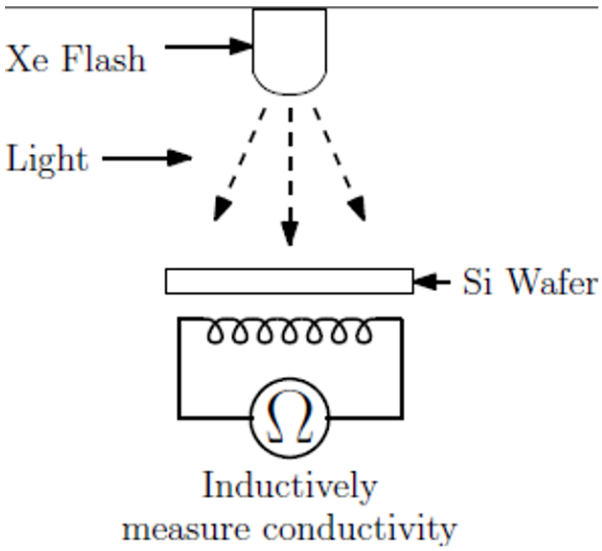


Figure 3.7: Diagram of Sinton WCT-120 indicating the Xe bulb, the Si sample and the inductive conductivity measurement setup

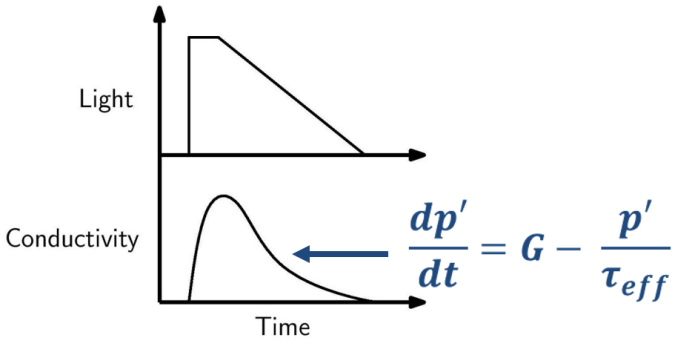


Figure 3.8: Light and conductivity response over time for a QSSPCD setup. The conductivity response is dependent on the photogeneration rate over time, given by G.

$5x10^{15}$ cm^{-3}. Then the oxide on the top was etched off and a native oxide was allowed to grow on the top surface. The effective lifetime was measured again. As expected from the high number of interface defects on the top surface, a low effective lifetime of 10 μs was measured. Next, TiO_2 was deposited at room temperature and the

lifetime was measured once more. The measured lifetime slightly improved to 18 μs, arguably due to reduction of surface defects. From the measured lifetime values we extract an interface recombination velocity of $> 10^6$ cm/s at the as-deposited Si/TiO_2 interface. Lifetimes and effective recombination velocity for SiO_2-passivated silicon, bare silicon and TiO_2-passivated silicon for different excess minority carrier densities are shown in Figures 3.9 and 3.10 respectively. Note that the data for unpassivated silicon does not extend beyond an excess carrier density of 4x10^{15} cm^{-3} due to the high recombination rate.

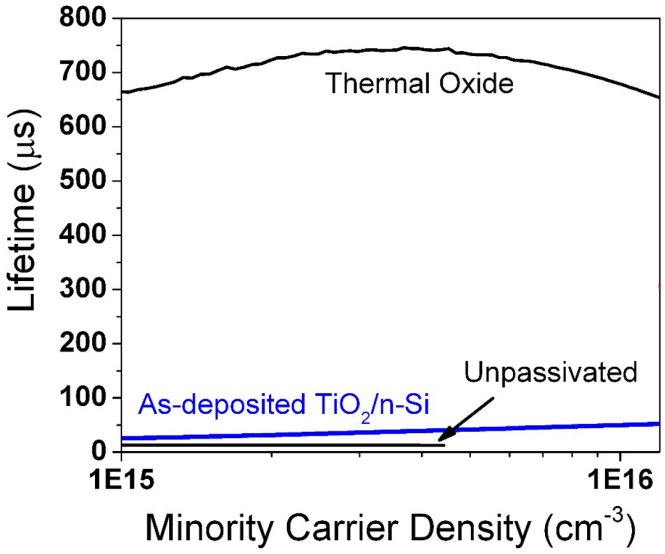


Figure 3.9: Effective lifetime of SiO_2, bare, and TiO_2-passivated silicon for different excess minority carrier densities

Annealing was done in the AG rapid thermal annealer (RTA). Due to the nature of the RTA, annealing times were limited to 2 minutes (longer annealing times would cause the cooling water lines to overheat and flood the lab). Figure 3.11 shows recombination velocities for different temperatures for TiO_2/n-Si and TiO_2/p-Si. The p-type silicon wafers were 645 μm thick, with a doping of N_A of 2x10^{15} cm^{-3}.

After annealing at 250 °C for 2 minutes, for n-Si/TiO_2 the effective lifetime increased to 275 μs at an excess minority carrier density of 1x10^{15} cm^{-3}, which cor-

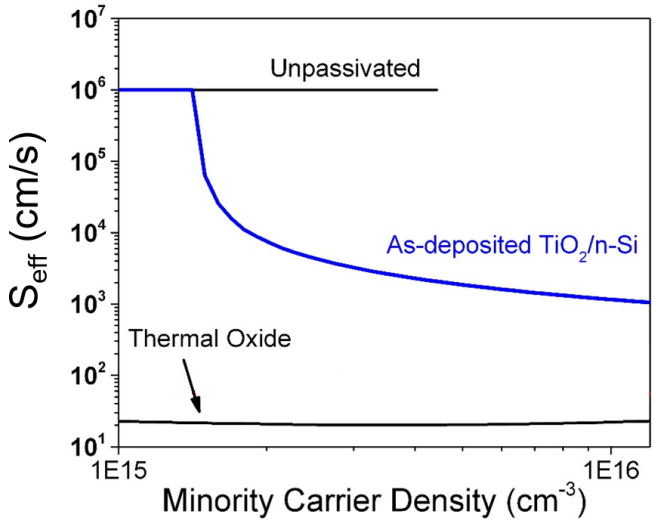


Figure 3.10: Effective recombination velocity of SiO_2, bare, and TiO_2-passivated silicon for different excess minority carrier densities. S_{eff} of 10^6 cm/s is the maximum possible recombination velocity which can be measured.

responds to an S_{eff}-value of 54 cm/s. Similarly, for p-Si/TiO_2 an effective lifetime increased to 640 μs was observed at an excess minority carrier density of 1x10^{15} cm^{-3}, which corresponds to an S_{eff}-value of 50 cm/s.

The S_{eff} reaches a minimum at an annealing temperature of 250 °C. It then rises with higher temperatures. One possible reason is that the TiO_2 is starting to go through a phase transition to a more crystalline phase - anatase TiO_2 forms at 450 °C [47].

Thus, an important result has been achieved: for 250 °C annealed TiO_2 on n-Si and p-Si substrates, recombination velocities as low as 54 cm/s and 50 cm/s respectively are obtained.

For practical applications, stability of the interface is critical. The stability of the interface (by measuring defect density changes) at the Si/TiO_2 heterojunction in response to exposure to the ambient air and humidity was observed. As commercial solar cells are expected to last for 20 years, it is important to investigate if the

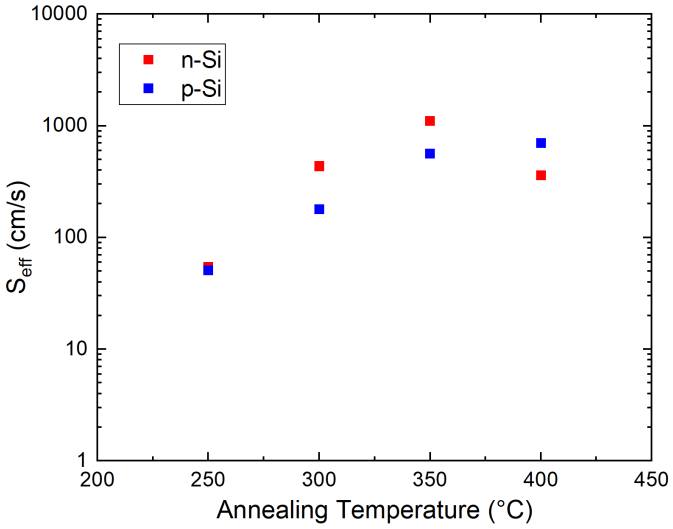


Figure 3.11: Surface recombination velocity (S_{eff}) versus anneal temperature for TiO_2/Si

hole-blocking interface is stable. Figure 3.12 shows S_{eff} for as-deposited and 250 °C annealed samples, exposed to air and ambient humidity for TiO_2/n-Si.

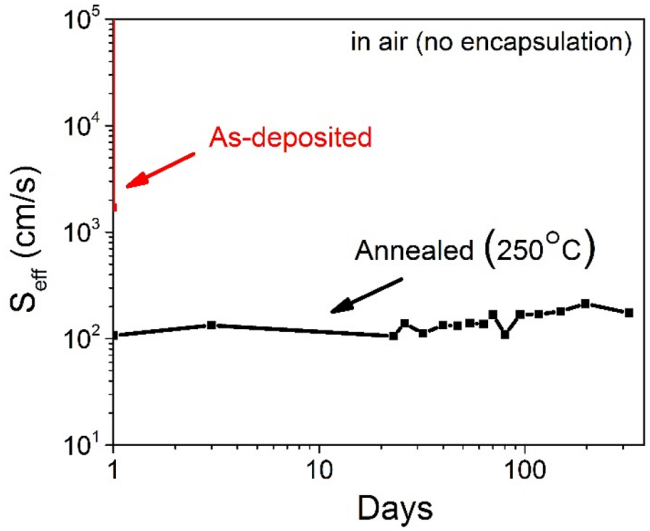


Figure 3.12: Surface recombination velocity (S_{eff}) versus time for TiO_2/n-Si for uncapsulated samples left in air

Annealing not only reduced the recombination velocity, but also made the interface more stable in air. The recombination velocity for the annealed sample slowly rises

to 200 cm/s within the span of 11 months, while the as-deposited interface degrades within a day (marked by the almost vertical red line on the left of the plot).

A stable trend has also been observed for annealed TiO_2/p-Si as well. As shown in Figure 3.13, TiO_2/p-Si has been measured to be modestly stable for over one year (S_{eff} slowly rises to 600 cm/s), while the best as-deposited TiO_2/p-Si degraded within 10 days. One explanation for the rise of the mean recombination is the degradation of passivation of the backside oxide/Si interface. Samples were prepared with a high quality passivating SiO_2 on the backside. However our control samples (SiO_2/p-Si/SiO_2) demonstrate an increase in recombination velocity over the span of months as well.

In summary, 250 °C annealing leads to a significant reduction in the interface recombination for TiO_2 deposited by CVD on n-Si and p-Si substrates, and the stability of S_{Eff}. A straightforward hypothesis is that the annealing reduces the electronic defect density at the interface. Models of this annealing chemistry will be presented later in the chapter.

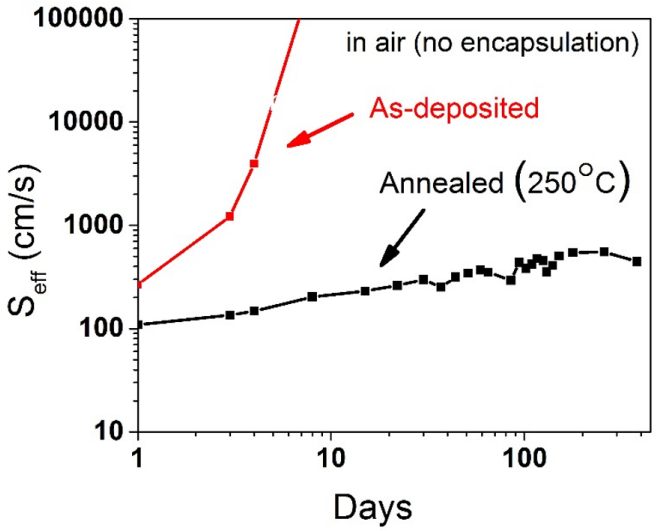


Figure 3.13: Surface recombination velocity (S_{eff}) versus time for TiO_2/p-Si for uncapsulated samples left in air

The quality of surface passivation does not appear to depend strongly on the thickness of the TiO_2 film, as seen in Figure 3.14. It appears there is a optimal thickness of about 3 to 6 nm.

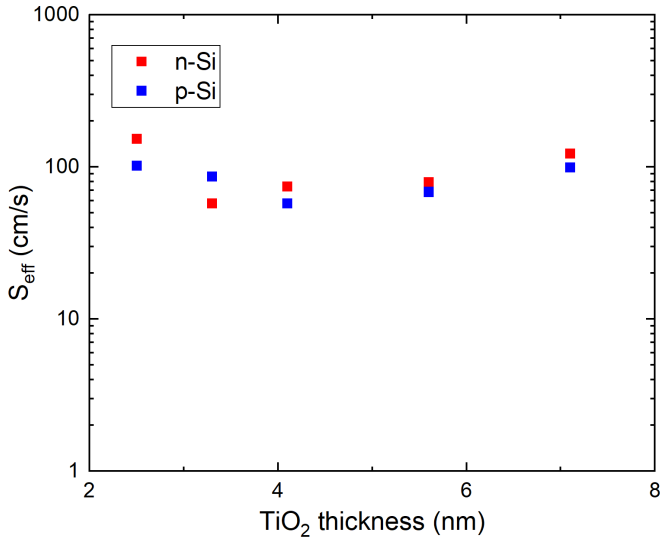


Figure 3.14: Surface recombination velocity (S_{eff}) versus TiO_2 thickness for 250 °C anneal

Note: annealing at 250 °C leads to a thickness reduction of the TiO_2 layer as shown in Figure 3.15. It is possible that the layer densifies. I-V characteristics performed on 250 °C annealed TiO_2/p-Si diodes were not promising, showing a significant degradation compared to as-deposited TiO_2/p-Si diodes (Figure 3.16). This significant degradation could be due to the layer densification, and/or interaction with O_2 or water vapor over time. Another possibility is that 250 °C annealing introduces negative charge [48], the effect of which will be explained in Chapter 5.

3.3.2 Room-temperature "Anneal"

Another approach to annealing was also attempted: room-temperature annealing, where instead of heating to elevated temperature, a sample was simply left inside a glove box with nitrogen ambient. Room temperature annealed significantly reduces

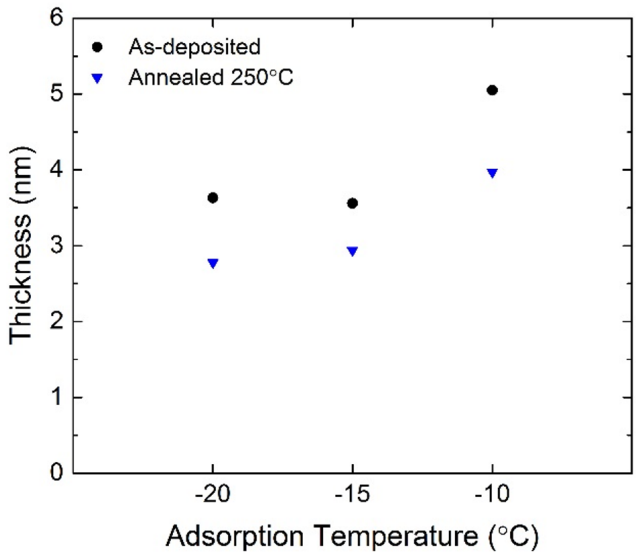


Figure 3.15: Reduction of TiO_2 thickness after 250 °C anneal.

the recombination velocity S_{eff} (down to 28 cm/s in a few days time). Figure 3.17 shows how as-deposited samples, after a few days in N_2 ambient see a marked drop in recombination velocity. The room-T anneal provides for stable recombination velocities, as long as samples remain in N_2. As can be seen in Figure 3.18, a sample exposed to air sees its S_{eff} rise to similar levels as 250 °C annealed samples left out in air for months. This indicates that room-T and 250 °C anneals utilize the same mechanism for surface passivation, as will be shown in subsection 3.3.3.

Meanwhile, samples left in the glovebox were unaffected, indicating it was really the air exposure that negatively impacts recombination velocities. To further confirm the negative impact of air exposure, samples annealed at 250 °C were left in the glovebox as shown in Figure 3.19. The recombination velocity actually improved slighty, instead of the degradation seen in Figures 3.12 and 3.13 for air-exposed 250 °C annealed samples. This further demonstrating a positive impact of the glovebox/nitrogen ambient.

Additionally, as Figure 3.20 demonstrates - unlike 250 °C annealing in N_2 ambient, room-T annealing does not degrade I-V characteristics. Ellipsometry measurements

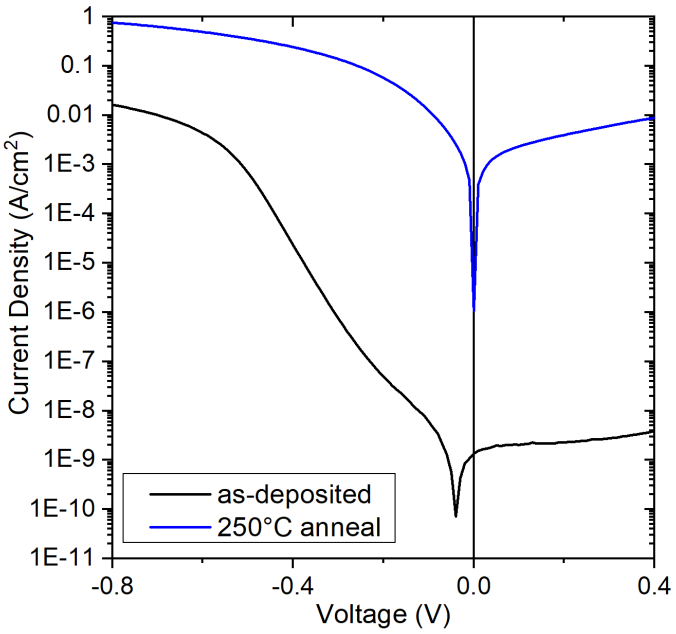


Figure 3.16: I-V characteristics for as-deposited, and 250 °C annealed TiO_2 on p-Si diodes, showing degradation for 250 °C annealed device

indicate that room-T annealing does not change TiO_2 thickness. Thus it appears room-T annealing has the surface passivation benefits of 250 °C annealing but not the drawback that the TiO_2 layer densifies and I-V characteristics degrade.

As a comparison to literature: the earliest report in literature shows an S_{eff}-values of 30 cm/s for 300 °C N_2-annealed TiO_2/Si [48]. Though this work was done on 60-70 nm thick TiO_2 using ALD and an annealing temperature of 300 °C. The lowest S_{eff}-values observed in literature is for 250 ° N_2-annealed TiO_2/Si, with values of 2.8 and 8.3 cm/s respectively for n-type and p-type silicon [49]. Though that work too was done with 60 nm of TiO_2 and using ALD.

At time of work, the S_{eff}-values for n-type and p-type silicon presented here for 250 ° N_2-annealed TiO_2 of 54 and 50 cm/s respectively were the lowest reported for thin TiO_2 films. [20, 41].

The S_{eff}-value of 28 cm/s for room-T annealed TiO_2/Si interfaces is the lowest to date for TiO_2 with a maximum fabrication temperature of 100 °C.

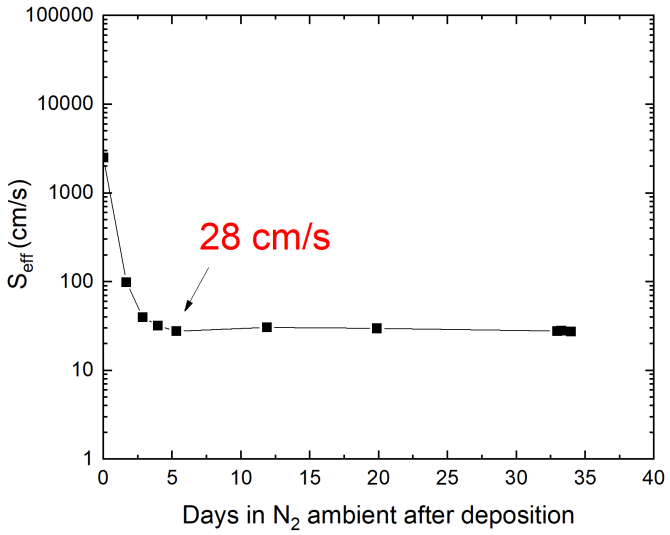


Figure 3.17: S_{eff}-values for room-T annealing. Samples were fabricated at different times, yet follow the exact same S_{eff} improvement pattern

3.3.3 TiO_2/Si Interface Chemistry

Now that we have two different approaches to improving surface passivation, it is time to investigate the chemistry and mechanism behind the deposition and annealing steps. One can break down the steps to "Before Deposition" (right after RCA clean and HF dip), Step A (after adsorption), Step B (after thermolysis), and Step C (after 250 °C or room-T anneal).

Figures 3.21 and 3.22 break down how the interface evolves chemically and the supporting XPS data respectively.

"Before deposition", Si(100) wafer substrates are cleaned using the standard RCA clean and dipped in HF to obtain hydrogen passivation (Figure 3.21a). The XPS spectrum in Figure 3(a) shows the usual bulk 2p1/2 and 2p3/2 Si peaks. A small interfacial Si peak is located at 101.5 eV. The precursor vapor is adsorbed in vacuum on the substrate held at -10 °C (Step A, Figure 3.21b and Figure 3.22a). This layer is then converted to 3 nm of TiO_2 by a thermolysis step at 100 °C (30 min) which cracks the precursor (Step B, Figure 3.21c and Figure 3.22b). At this stage, XPS (performed

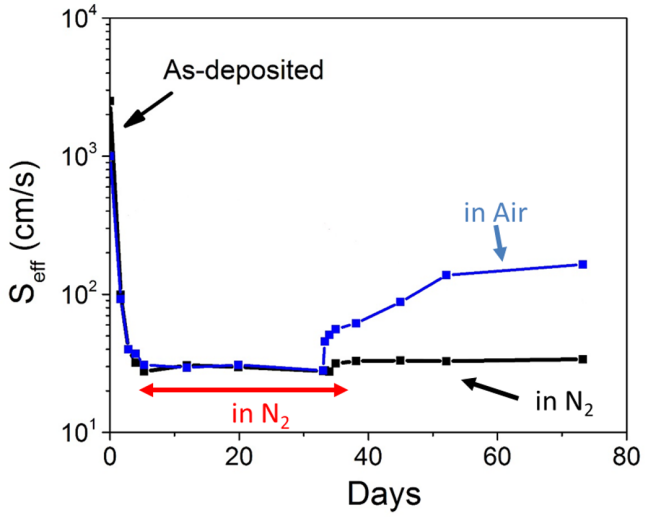


Figure 3.18: S_{eff}-values for room-T annealing after both (a) air exposure and (b) keeping in glovebox N_2 ambient. Air exposure leads to similar results as 250 °C annealed samples exposed to air, indicating the same passivation mechanism for both anneals.

on 1- nm thick films for interface sensitivity) shows the 101.5 eV peak is essentially unchanged (shifted by only 0.1 eV) compared to before the precursor was adsorbed, showing no reaction has occurred yet between the original Si:H surface and the TiO_2 film. The surface recombination velocity S_{eff} for TiO_2/n-Si after this thermolysis step is 5x10^3 cm/s, denoting a poorly passivated Si surface consistent with a lack of interface bonding. Furthermore, as mentioned before, S_{eff} for "as-deposited TiO_2" rises rapidly from 5x10^3 to 10^6 cm/s in air within a day, indicative that perhaps that some of the passivation was still provided by Si-H bonds, which are being oxidized in air.

After a 250 °C anneal in nitrogen (Step C, Figure 3.21d and Figure 3.22c), the interface is qualitatively different. The XPS spectrum in Figure 3.22c shows that the peak at 101.6 eV disappears and is replaced by a new structure with an energy of 102.0 eV. This annealing also led to S_{eff} dropping from 5x10^3 to 90 cm/s for the concomitant lifetime sample, with S_{eff} now remaining stable and low in air for months

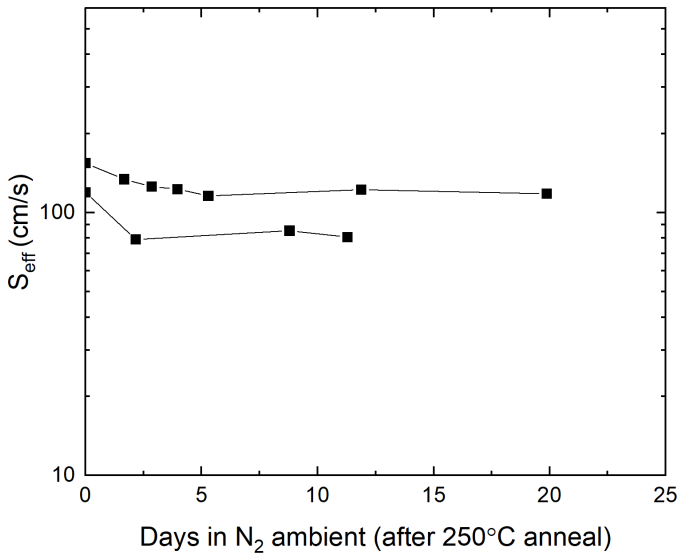


Figure 3.19: S_{eff}-values for 250 °C annealed samples left in glovebox N_2 ambient. The samples show a slight improvement in S_{eff} value.

(indicating the new Si surface bonds are stable in air). It is hypothesized that the structure associated with the 102.0 eV XPS Si peak is responsible for the high quality interface passivation, and that the Si surface has chemically reacted with the TiO_2 during the 250 °C anneal to form bridging Si-O-Ti bonds between the Si and TiO_2 film through transmetallization, similar to the structure of a well-passivated Si/SiO_2 interface. The peak at 102.0 eV implies a reduced Si species compared to SiO_2 (usual Si-O bonds are between 103.2 to 103.9 eV 4) The 102.0 eV peak can be attributed to Si-O-Ti bonds since the Si would be reduced in Si-O-Ti compared to Si-O-Si.

The same phenomenon was observed in XPS measurements done for room-T annealed samples, thus proving that 250 °C and room-T annealed TiO_2/Si interfaces have the same underlying mechanism for passivation.

So now that it has been shown that the TiO_2/Si interface is passivated, either with a 250 °C or room-T anneal, TiO_2/p-Si diodes are unaffected by the room-T anneal, and the interface chemistry is understood, let's see what happens when room-T TiO_2

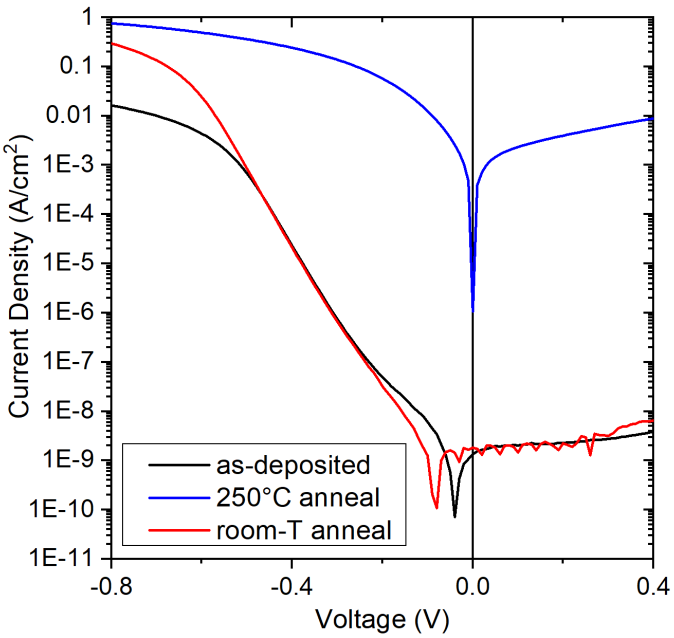


Figure 3.20: I-V characteristics for as-deposited, room-T and 250 °C annealed TiO_2 on p-Si diodes, showing degradation for 250 °C annealed device, but not for room-T annealed device. I-V were measured in air. Room-T annealed devices were taken out after 7 days in N_2 ambient.

is deposited on the backside of a PEDOT/Si heterojunction to form a double-sided heterojunction.

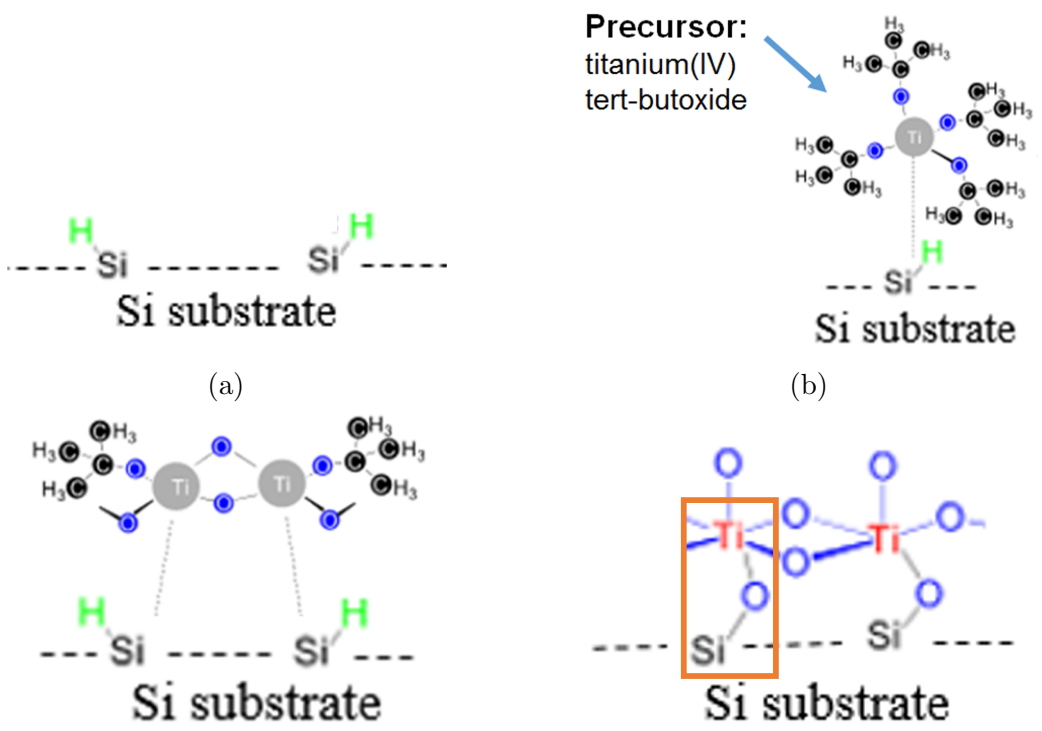


Figure 3.21: Mechanism steps for formation of Si-O-Ti bonds (a) before deposition - Si-H bonds are present, (b) After Step A - adsorption of precursor at -10 °C, (c) After Step B - thermolysis at 100 °C, inducing cracking of O-C bonds and condensation of precursor to TiO_2 film, (d) After Step C - annealing, causing transmetallization to form Si-O-Ti bonds. Courtesy of Girija Sahasrabudhe.

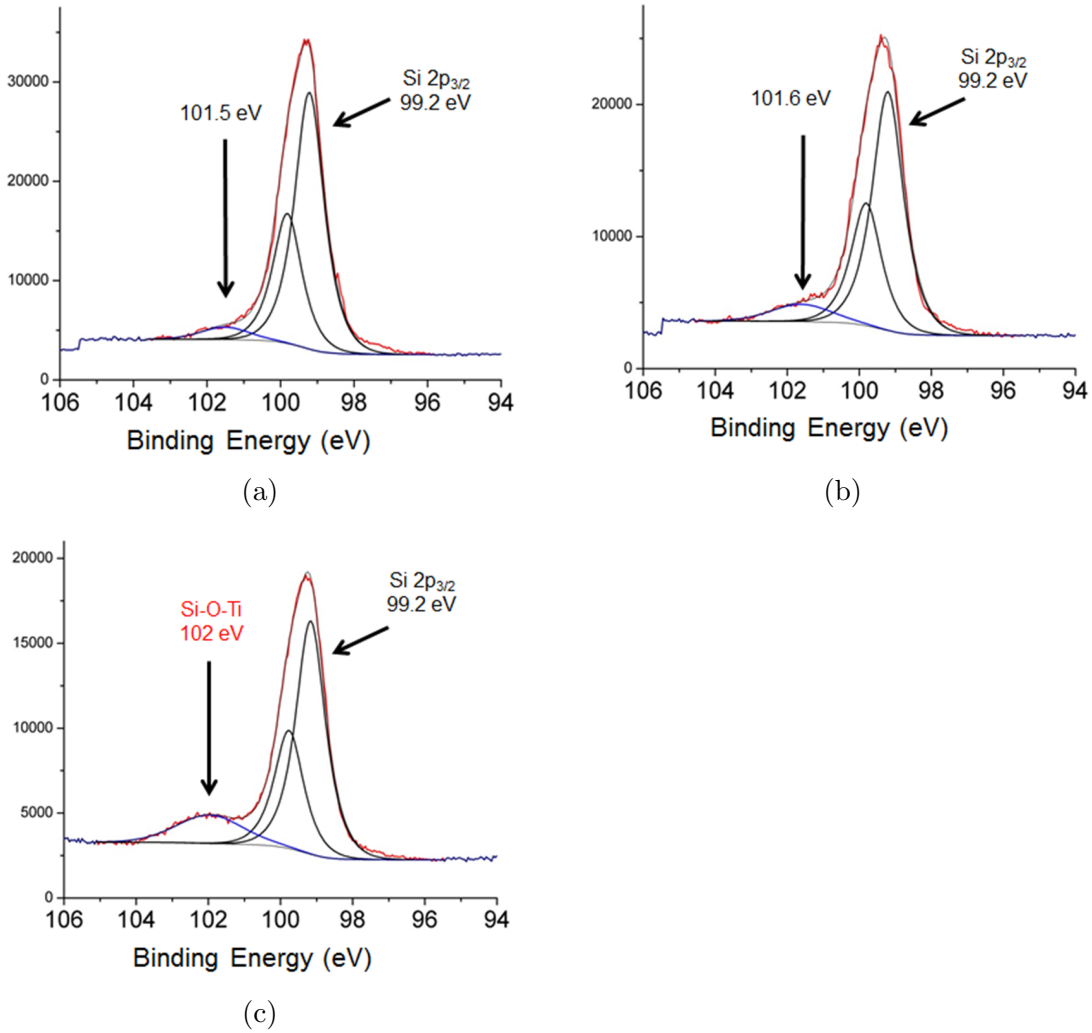


Figure 3.22: Mechanism steps for formation of Si-O-Ti bonds (a) before deposition - Si-H bonds are present, (b) After Step A - adsorption of precursor at -10 °C, (c) After Step B - thermolysis at 100 °C, inducing cracking of O-C bonds and condensation of precursor to TiO_2 film, (d) After Step C - annealing, causing transmetallization to form Si-O-Ti bonds. Reprinted (adapted) with permission from [43]. Copyright 2015 American Chemical Society.

3.4 PV Device and Its Dependence on Annealing Conditions

In previous work, a double-heterojunction crystalline silicon solar was demonstrated [50]. The band-alignment is shown in Figure 3.23 The front-side p^+/n junction of a conventional Si solar cell was replaced by a heterojunction formed between n-Si and PEDOT:PSS that blocks electrons but passes holes. The back-side n^+/n junction was replaced by the electron-selective Si/TiO_2 heterojunction. It was showed that the electron-selective "as-deposited" TiO_2 contact increased V_{OC} by 30 mV without degrading short circuit current or fill factor compared to a direct metal contact to the substrate. Using what is learned about annealing and Si surface passivation, V_{OC} is increased further through the reduction of TiO_2/Si interface recombination.

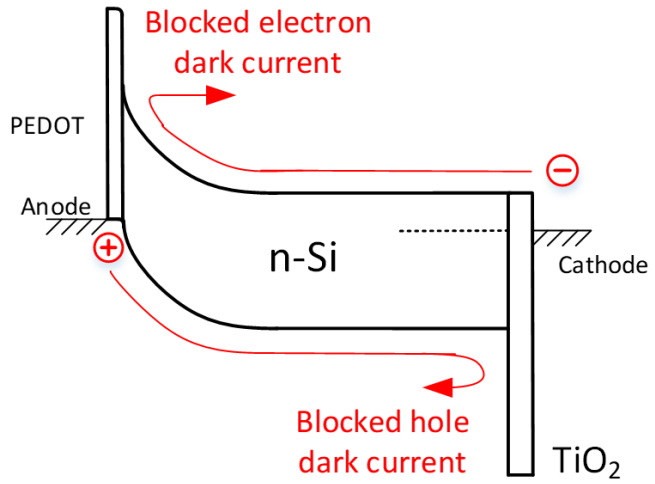


Figure 3.23: Double-sided PEDOT/n-Si/TiO_2 device

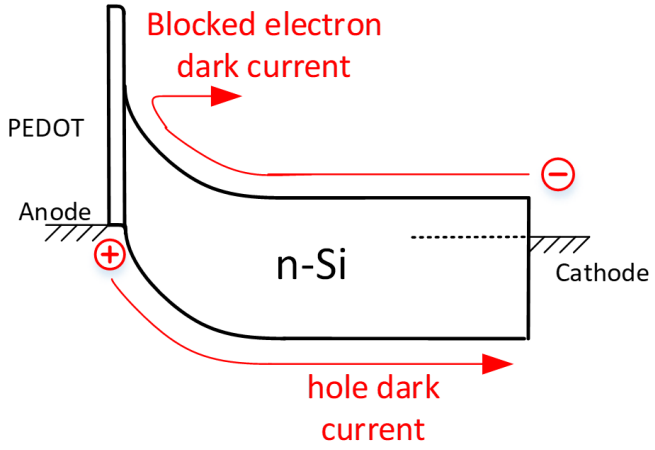


Figure 3.24: Single-sided PEDOT/n-Si device

3.4.1 Current-Voltage Characteristics

To demonstrate the effect of the passivated TiO_2 contact, the two structures from Figure 3.24 and Figure 3.23 - without and with TiO_2 respectively - were fabricated. First, TiO_2 was deposited on one sample, using the standard 3 cycle deposition with the small bulb. That sample was left in N_2 ambient at room temperature for 48 hours, i.e. the room-T anneal was performed. The top side TiO_2 layer was etched off, and 70 nm PEDOT was spuncoat on the top side for both samples. Silver contacts were deposited using a thermal evaporator for the anode (PEDOT) and Al/Ag contacts were evaporated for the cathode. J-V curves under dark are shown in Figure 3.25.

J-V curves under light (solar simulator at $\sim$ 110 mW/cm^2) are shown in Figure 3.26. The relatively low J_{SC} values (27.2 and 29.1 mA/cm^2 versus ideal 42 mA/cm^2) are due to the lack of an effective AR coating, PEDOT absorption, and the cathode metal coverage. A slight increase in short-circuit current due to the TiO_2 can be attributed to increased collection of long wavelength photons as the Si/TiO_2 interface is passivated and thus fewer photogenerated carriers recombine at the cathode [50].

The V_{OC} is 641 mV. At the time of work, it was a record V_{OC} for double-sided heterojunction solar cells with any sort of TiO_2/Si electron-selective contact at the cathode contact. Since then, further optimized solar cells with TiO_2/Si have achieved a V_{OC} of 681mV [51].

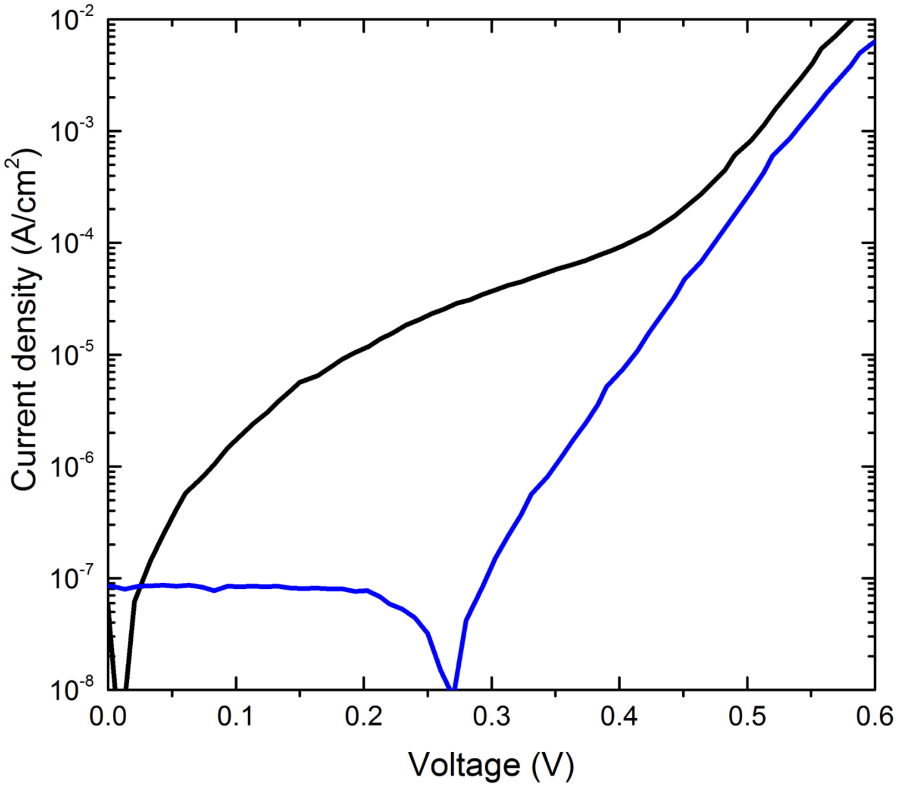


Figure 3.25: J-V characteristics of device without TiO_2 (black) and with TiO_2 (blue) respectively under dark

Table 3.1 shows the comparison of solar cell parameters between the "no TiO_2" and "room-T annealed TiO_2" devices. The 29 mA/cm^2 short circuit current was limited almost entirely by absorption in the PEDOT and surface reflection, with metal coverage (16%) also contributing. More relevantly, V_{OC} increase of 45 mV is observed. How can the V_{OC} increase be correlated to an S_{eff}-value to validate that indeed it is the room-T anneal that caused this improvement? The following subsection will go into this question.

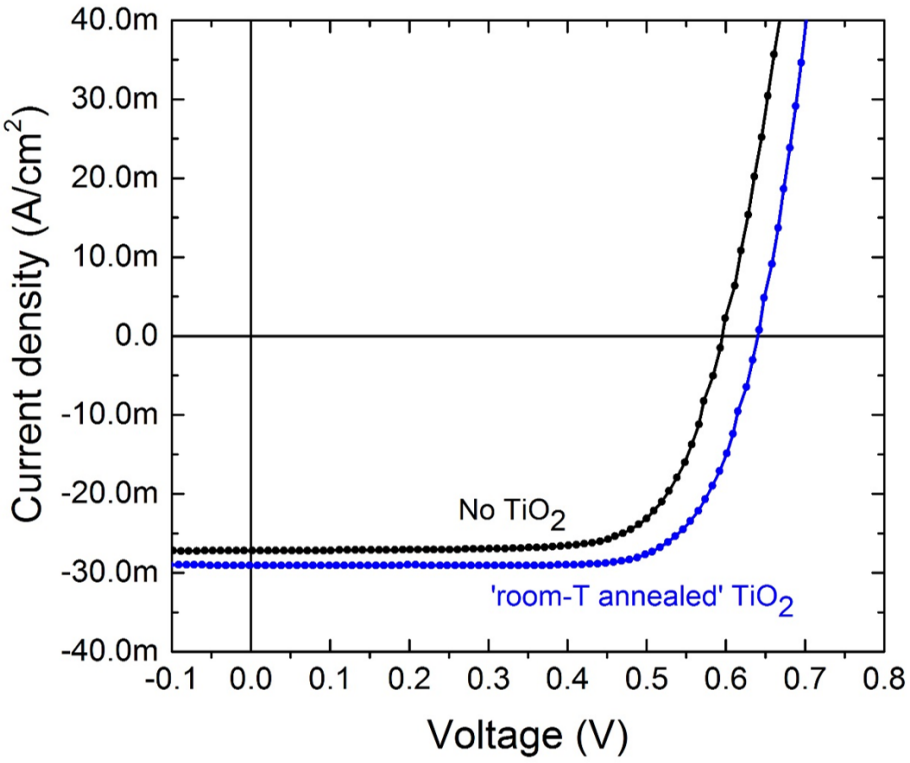


Figure 3.26: J-V characteristics of device without TiO_2 (black) and with 4 nm TiO_2 (blue) at the Al/n-Si interface under light. The device with TiO_2 had an open-circuit voltage of 641 mV, highest V_{OC} to date with a double heterostructure with a TiO_2/Si cathode contact.

	No TiO_2	with room-T TiO_2	change
V_{OC} (mV)	596	641	45
J_{SC} (mA/cm^2)	27.2	29.1	1.9
FF(%)	72.7	74.4	1.7

Table 3.1: Solar Cell Parameters of "no TiO_2" and "room-T TiO_2" double-sided PEDOT/n-Si/TiO_2 solar cells

3.4.2 Dependence of Hole Blocking Factor on S_{eff}

To elucidate the importance of interface recombination, one notes that the rate of hole transport in the substrate due to diffusion has to match the rate of recombination at the TiO_2 interface, which is proportional to the hole density at that interface. It

is straightforward to show that the hole current ($J_{0,h}$) is reduced from its short base value $J_{0,SB}$ (no TiO_2) by a blocking factor BF, where

$$BF = \frac{J_{0,noTiO2}}{J_{0,\ TiO2}} \tag{3.5}$$

From which follows that:

$$J_{0,h} = \frac{qn_i^2 D_p}{N_D W} * \ \frac{1}{BF} = J_{0,SB} * \ \frac{1}{BF} \tag{3.6}$$

with

$$BF \ = \ 1 \ + \ \frac{D_p}{W S_{eff}} \tag{3.7}$$

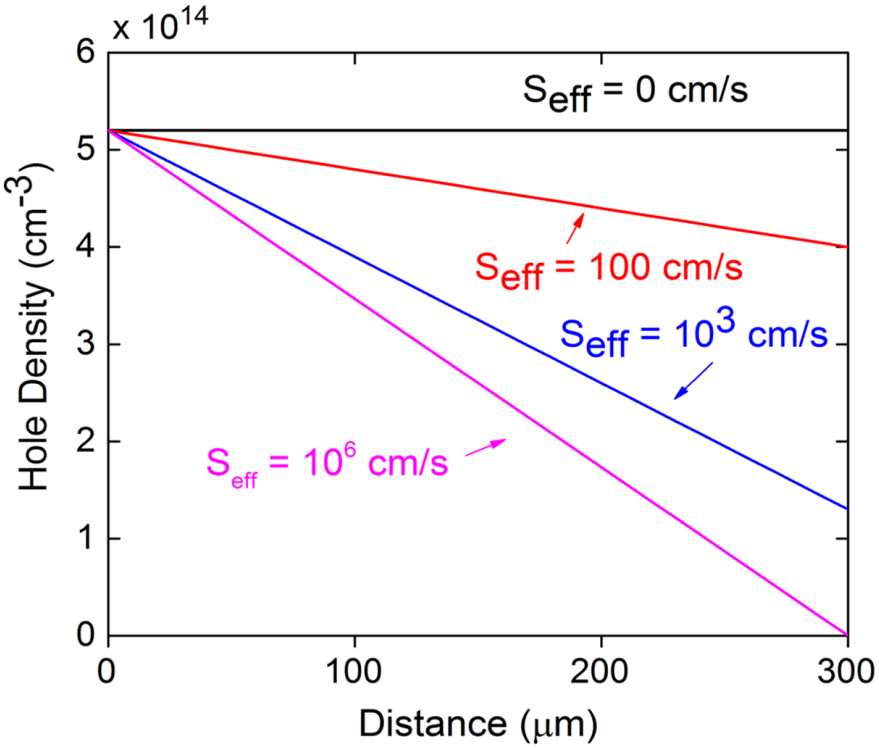


Figure 3.27: Simulated hole density profile for a 300 μm thick wafer under forward bias for different S_{eff} values. The applied bias is 0.60 V. Larger S_{eff} values lead to larger gradients.

The calculated hole density profile is plotted in Figure 3.27 for an applied bias of 0.60 V in dark (short-base scenario) for different S_{eff} values. A lower S_{eff} (smaller gradient) implies a higher BF and a smaller J_0. At $S_{eff} = 0$ cm/s, the gradient is completely flat. For an $S_{eff} > 1x10^3$ cm/s there is little effective blocking compared to a direct metal contact. Concomitantly, assuming (optimistically) that the PEDOT/Si functions as a perfect hole emitter with 100% injection efficiency, one can calculate an increase in V_{OC} from the reduced J_0 :

$$\Delta V_{OC} = kT * \ln\left(\frac{J_{0,noTiO2}}{J_{0,TiO2}}\right) = kT * \ln(BF) \tag{3.8}$$

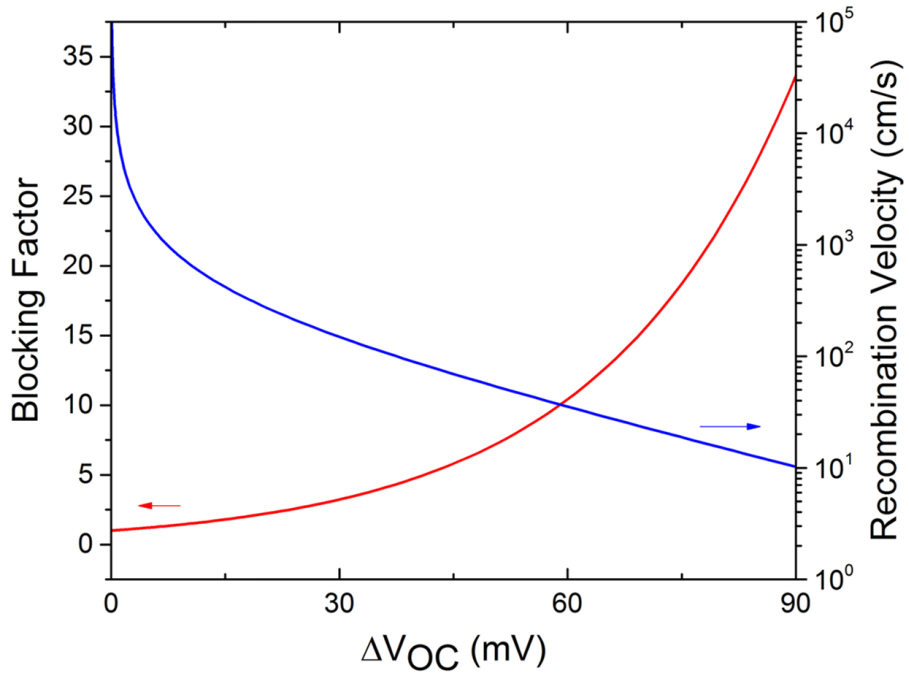


Figure 3.28: From ΔV_{OC}, and equations 3.7 and 3.8, one can calculate the blocking factor (reduction in J_0) and S_{eff} required to achieve said ΔV_{OC}.

Figure 3.28 shows the blocking factor as a function of V_{OC} (from equation 3.8) and S_{eff} from the observed V_{OC} (from equation 3.7). Based on the experimentally observed increase in V_{OC} of 45 mV, we find a BF of 5.4. Using W = 300 μm and assuming $D_p = 10$ cm^{2}s-1, we estimate S_{eff} to be 75 cm/s. This S_{eff} value is consistent

with calculated S_{eff} values from QSSPCD measurements of 65 - 85 cm/s at similar light levels on lifetime samples fabricated concomitantly with these double-sided devices.

The 29 mA/cm^2 short circuit current was limited almost entirely by absorption in the PEDOT and surface reflection, with metal coverage (16%) also contributing. Straightforward engineering to raise the short circuit current to 42 mA/cm^2 would raise the power efficiency to over 20%, consistent with that expected with S_{eff} = 80 cm/s in Figure 3.6.

The same consistency cannot be found for double-sided devices previously fabricated with 250 °C annealed TiO_2, as will be explained next.

3.4.3 Comparison of S_{eff} Extracted from QSSPCD and ΔV_{OC}

Figure 3.29 shows a comparison between $S_{eff}(V_{OC})$ and S_{eff}(PCD). $S_{eff}(V_{OC})$ was extracted from V_{OC} using equations 3.7 and 3.8. Meanwhile, S_{eff}(PCD) was determined from QSSPCD measurements of the TiO_2/Si interface left in N_2 ambient for 48 hours at room temperature (room-T stabilized TiO_2). Additionally, a comparison between $S_{eff}(V_{OC})$ and S_{eff}(PCD) is made for 250 °C annealed TiO_2 (annealed TiO_2) from previous experiments [41, 52]. 250 °C-annealed and room T-stabilized TiO_2 have similar S_{eff}(PCD) values. S_{eff} (V_{OC}) and S_{eff} (PCD) match for room-T anneal. However 250 °C-annealed TiO_2 has a large and high range for $S_{eff}(V_{OC})$.

This indicates that although the 250 °C annealing step reduces the recombination velocity measured by QSSPCD compared to as-deposited TiO_2, which typically has a S_{eff}(PCD) 5000 cm/s, the degradation in I-V performance seen for TiO_2/p-Si diodes also appears when 250 °C annealed TiO_2 is used on the backside of a PEDOT/n-Si diode.

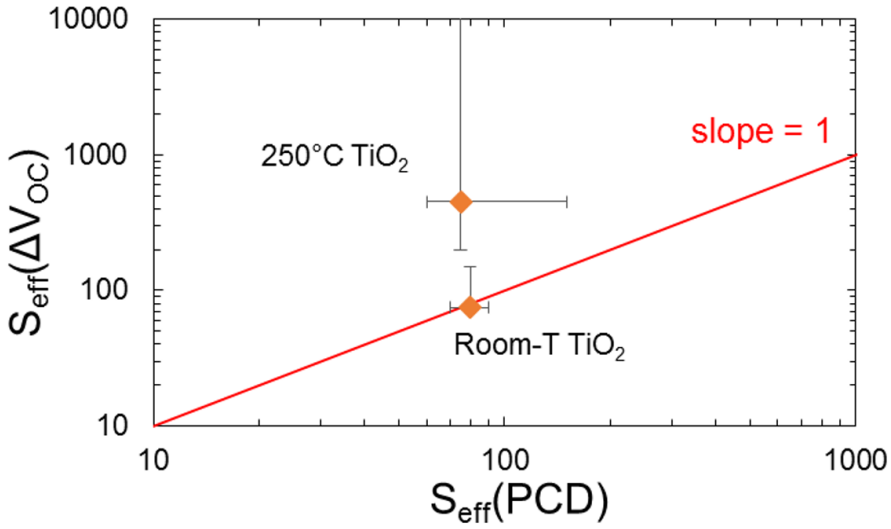


Figure 3.29: Comparison of recombination velocities calculated from improvement in V_{OC}, S_{eff}(delta V_{OC}), and from QSSPCD measurements, S_{eff}(PCD), for annealed TiO_2 (250°C anneal) and room-T TiO_2

3.5 Conclusion

The importance of passivating the TiO_2/Si interface was shown as surface defects have a dramatic effect on V_{OC} and PCE. Two annealing methods were demonstrated: a quick 2-minute 250 °C anneal in N_2 ambient, and a longer 2-day room-temperature anneal in N_2 ambient. Both observed the same interface chemistry, namely the formation of Si-O-Ti bonds, which led to higher minority carrier lifetimes, significantly lower recombination velocities (down to 28 cm/s) and thus a lowered defect density at the TiO_2/Si interface. Room-T annealing did not degrade TiO_2/p-Si diode I-V characteristics, unlike 250 °C annealing. Room-T annealing was further put to the test by fabricating and measuring a double-sided heterojunction device consisting of PEDOT/n-Si/room-T TiO_2. The improvement in V_{OC}, an increase of 45 mV, corresponded with an effective recombination velocity of 75 cm/s, consistent with QSSPCD measurements of lifetime samples measured concomitantly.

Chapter 4

Heterojunction Bipolar transistor with TiO_2/Si Emitter and Probing of Current Mechanisms in TiO_2/Si contacts

4.1 Introduction

In the previous two chapters, TiO_2 growth and TiO_2/Si interface conditions were optimized for low recombination at the Si/TiO_2 interface. As the previous chapter showed, a double sided device with room-T annealed TiO_2 as the backside electron-selective contact lead to a solar cell device with V_{OC} of 741 mV. In order to further improve V_{OC} and obtain the absolute best possible solar cells, the current mechanisms at the TiO_2/Si heterojunction need to be analyzed. This is difficult in practice because an I-V measurement measures the sum of the electron current in one direction and the hole current in the other direction.

In this chapter, we use the p-Si/TiO_2 electron-selective contact as the emitter in a heterojunction bipolar transistor (HBT). This allows one to measure the electron and hole currents separately. Of particular interest are the hole current components, i.e. holes travelling from the silicon into the metal, which are to be minimized for optimal solar cell performance.

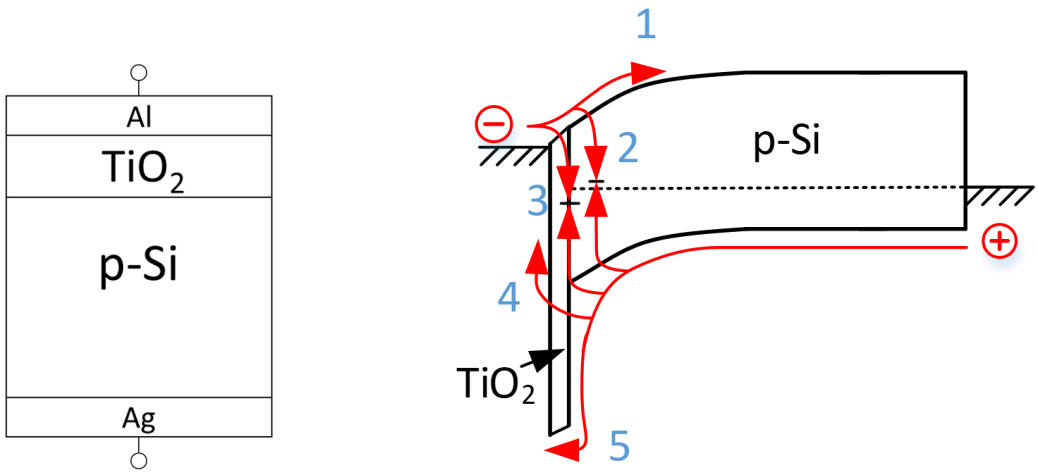
The work in this chapter was largely published in [53–55].

4.2 Possible Current Mechanisms at Al/TiO_2/p-Si Selective Contact

Figure 4.1 shows the structure and band diagram of the TiO_2/p-Si heterojunction. There are five possibilities regarding the current mechanisms across the heterojunction: (1) injection of minority carriers (electrons) from the cathode across the heterojunction into the p-type Si quasi-neutral region, (2) electron injection and subsequent recombination in the space-charge region, (3) electron transport through the TiO_2 to recombine at the TiO_2/Si interface, (4) holes tunneling through the TiO_2 layer, effectively exhibiting a Schottky-barrier-like majority carrier current, and (5) holes passing over the TiO_2/Si barrier. Only mechanism (1) functions as a minority carrier injector into the substrate; the other mechanisms are parasitic and undesirable for PV applications - and from a PV point of view these are the currents to be blocked by the electron-selective contact. The 5 current mechanisms are shown in Table 4.1. Mechanism (3), recombination at the TiO_2/Si interface, is of special interest in this thesis.

Figure 4.2 shows J-V characteristics for several thicknesses of the TiO_2 film on a CZ substrate doped 5x10^{15} cm^{-3}.

In I-V measurements for 4 nm of TiO_2 at different temperatures (Figure 4.3), two regimes are visible: a low-current regime at $< 10^{-6}$ A/cm^2 (disappears at higher



(a) (b)

Figure 4.1: (a) Device structure and (b) potential current mechanisms in forward bias. The Ag provides an ohmic back contact.

Current Mechanism	
1	injection of minority carriers (electrons) from the cathode across the heterojunction into the p-type Si quasi-neutral region
2	electron injection and subsequent recombination in the space-charge region
3	electron transport through the TiO_2 to recombine at the TiO_2/Si interface
4	holes tunneling through the TiO_2 layer, effectively exhibiting a Schottky-barrier-like majority carrier current
5	holes passing over the TiO_2/Si barrier

Table 4.1: Current mechanisms across Al/TiO_2/p-Si diode.

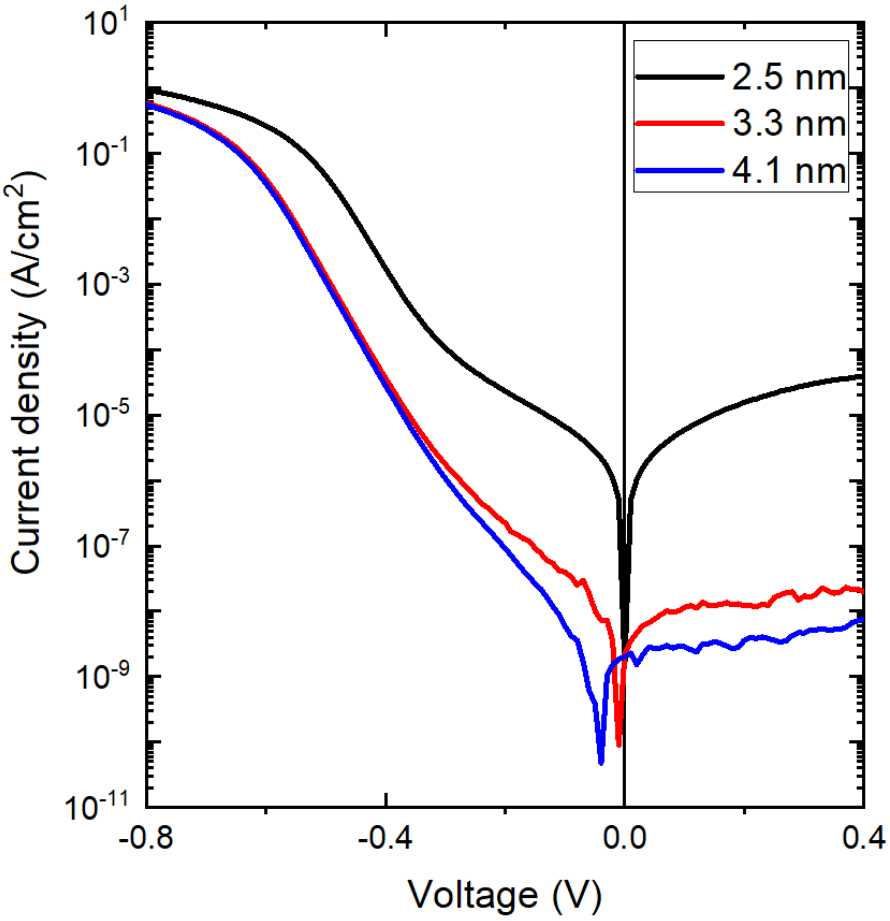


Figure 4.2: J-V characteristics TiO_2/p-Si for different thicknesses of TiO_2 for CZ substrates doped 5x10^{15} cm^{-3} at 298 K.

temperatures) and a high-current regime. Saturation current densities (J_0s) for both regimes plotted versus inverse temperature (Figure 4.3) yield an activation energy (E_A) for the low-current regime of 0.53 eV (Figure 4.4), indicating that this current regime is due to space-charge region recombination (current mechanism (2)). Thus current mechanism (2) is irrelevant for PV. The fact that the activation energy for the high-current regime is 1.12 eV is consistent with electrons being injected into the silicon (mechanism (1)):

$$J_{elec,\ inj} = \frac{qn_i^2 D_n}{N_A L_n}\left(e^{\frac{qV}{kT}} - 1\right) = J_{0,e} * \left(e^{\frac{qV}{kT}} - 1\right) \tag{4.1}$$

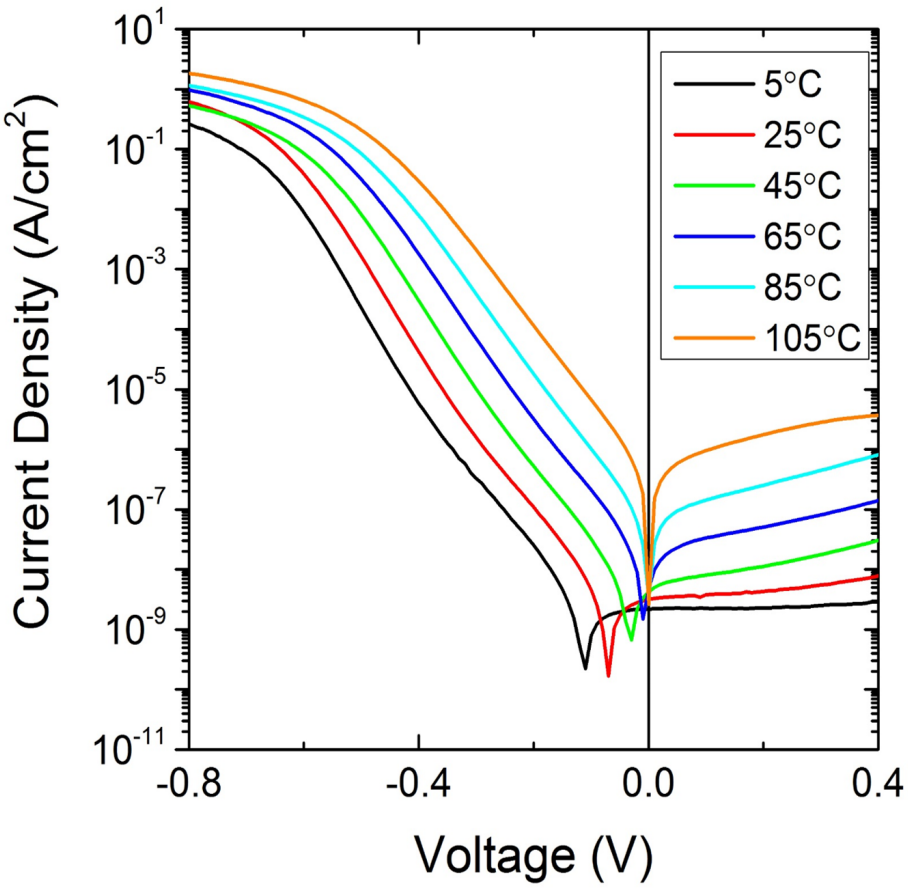


Figure 4.3: J-V characteristics TiO_2/p-Si for different temperatures. TiO_2 thickness was 4 nm for CZ substrates doped 5x10^{15} cm^{-3} at 298 K.

n_i is the intrinsic carrier density, D_n is the diffusion coefficient for electrons in p-Si, N_A is the doping of the p-Si substrate, V is the applied voltage across the TiO_2/p-Si junction (negative on Al/TiO_2 and positive on Si). An activation energy of 1.12 eV is obtained as in the long-base limit n_i^2 is proportional to exp(-E_G/kT) and E_G of silicon is 1.12 eV. The high-current and low-current regimes are consistent with the double diode model common in Si PV, with corresponding saturation current densities J_{01} and J_{02}, as shown in Figure 4.5.

However current mechanism (1) is not the only possibility for the high current mechanism. Current mechanism (4), Schottky barrier majority carrier current, and current mechanism (3), recombination at the interface, have an activation energy

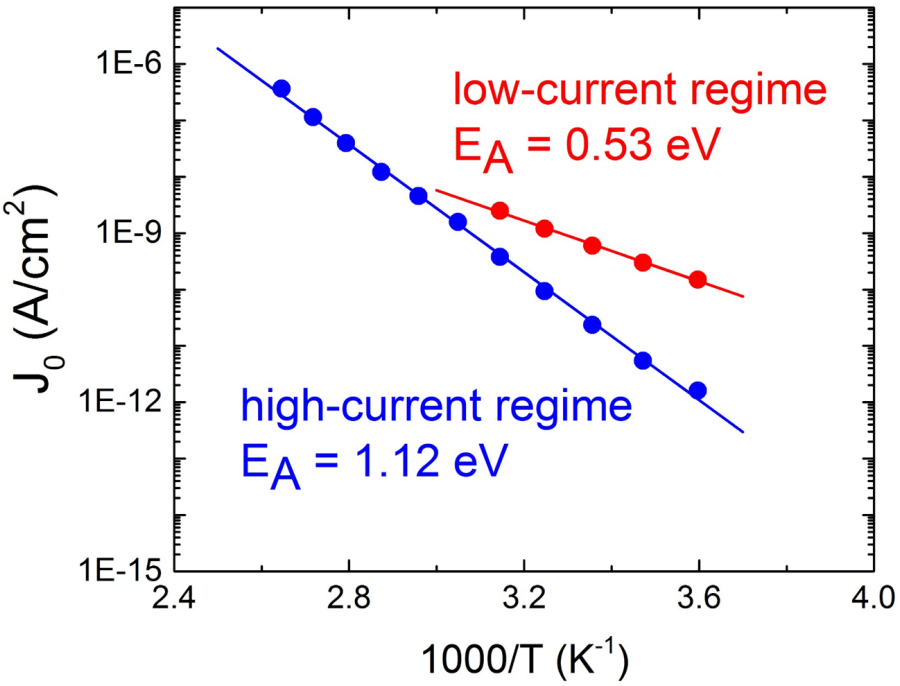


Figure 4.4: J_0 versus inverse temperature for the high-current and low-current regimes of Figure 4.3

equivalent to the Schottky barrier height. Figure 4.6 shows capacitance-voltage measurements for the TiO_2/p-Si heterojunction, with an extracted built-in voltage of 0.74 eV giving a Schottky barrier height of 0.99 eV. This implies that the combination of the low Al work function and thin nature of the TiO_2 set the Fermi level at the Si surface near the conduction band. The kink in the C-V data is from to a well-known effect of H-passivation of boron dopants at the Si surface due to RCA cleaning [56]. Assuming all current to be due to mechanisms (3) and (4), and using a $T^2\exp(-\Phi_B/kT)$ prefactor for Schottky barrier current, the high-current regime data in Figure 4.4 would be consistent with a Schottky barrier of 1.07 eV, close to that predicted by the C-V data (0.99 eV). Thus, with the data presented, we cannot clearly identify the major current component as injection of electrons into the substrate, current mechanism (1), or holes recombining at the TiO_2/S interface, current

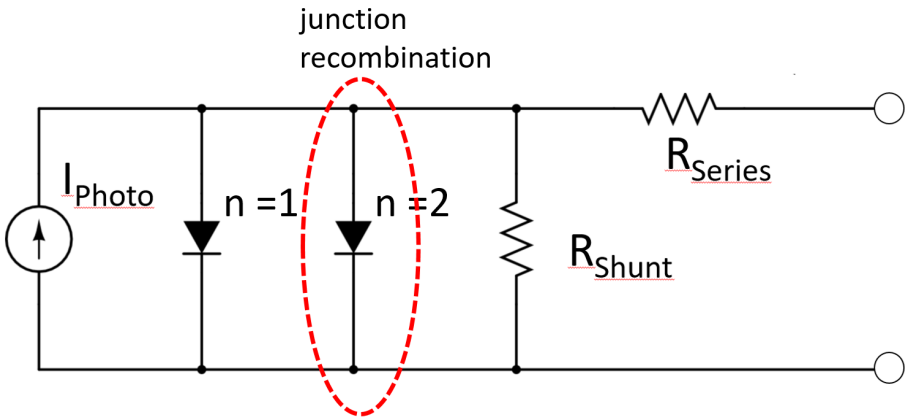


Figure 4.5: Double Diode Model for Si solar cell. Two mechanisms are active in standard p-n junction: space charge region recombination is behind "junction recombination" and n=1 corresponds to minority carrier injection in to the substrate bulk.

mechanism (3), or tunneling through or into TiO_2 defect states, current mechanism (4).

However, Figure 4.2 showed the TiO_2 barrier thickness > 3 nm had no effect on current, implying mechanism (4), which includes holes tunneling through the TiO_2, is unlikely to exist in the high-current regime. Mechanism (5), holes going over the TiO_2 barrier, is also unlikely to exist in the high-current regime, due to the large Si/TiO_2 band offset (2.1 eV). The remaining possible current mechanism, besides electron injection, would be interface recombination, mechanism (3).

Modelling current mechanism (1) based on equation 4.1 requires knowledge of L_n for CZ substrates. Modelling with the maximum L_n, equal to the subtrate width W $= 525$ μm underestimates the current (Figure 4.8). Thus the current is dominated by either ideal electron injection with $L_n \approx 200$ μm (giving a more closer match to the data in Figure 4.8) or interface recombination.

To resolve this uncertainty, the device in Figure 4.1 was reproduced with an FZ silicon wafer (doping 1.0×10^{15} cm^{-3}), which was measured to have a diffusion length $L_n = (\sqrt{D\tau}) > 1$ mm, in excess of wafer thickness, so equation 4.1 can be used with

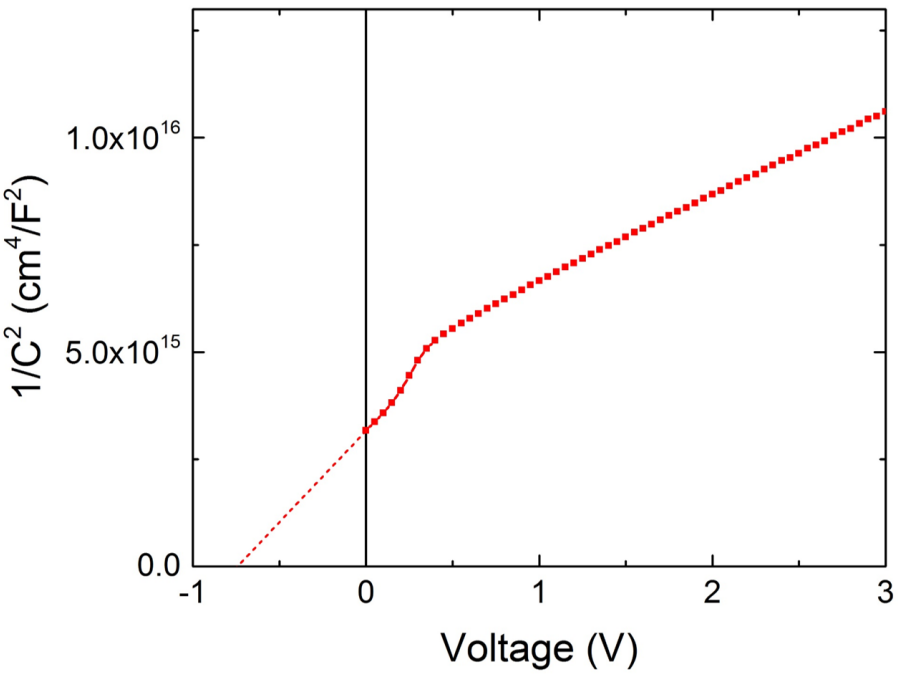


Figure 4.6: C-V characteristics of Al/TiO_2/CZ p-Si at 1MHz

the wafer thickness substituted for L_n (short base model). The very close fit between the ideal electron injection current and the actual J-V curve in Figure 4.8 indicates that current mechanism (1) is responsible for most of the current..

To further illustrate this point, we utilize the concept of minority carrier injection efficiency γ, shown in Figure 4.9. On the left, a typical n^+-p junction is shown, with both electron and hole currents. γ is the ratio of the electron current (minority carrier current) in the p-Si region divided by the total current across the junction. Similarly, on the right is shown the TiO_2/p-Si junction. Here as well, γ can be described as the electron current divided by the total current. Thus γ represents how much of the total current is the injected electron current. In other words, a γ-factor of 1 implies all the current is due to current mechanism (1), while a γ-factor of 0 would imply none of the current is due to minority carrier injection.

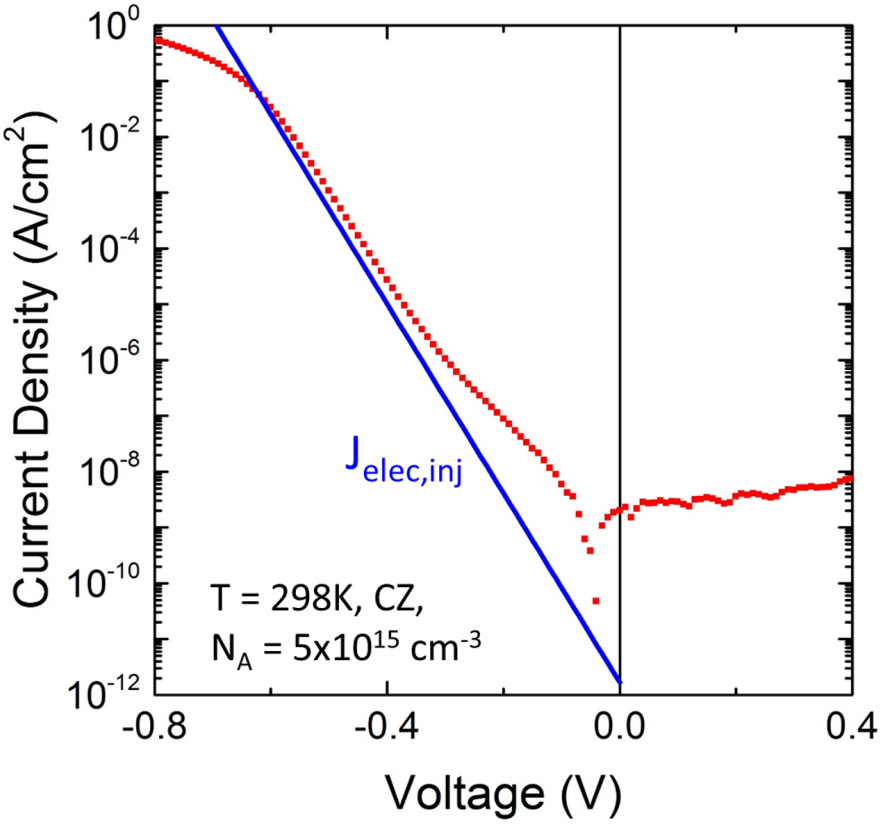


Figure 4.7: J-V characteristics of Al/TiO_2/CZ p-Si (red) and using equation 4.1 using the maximum possible L_n of the wafer thickness (525 μm), which as expected underestimates the current. TiO_2 thickness is 4 nm.

In Figure 4.10, we show total current for $\gamma = 0.1$ and $\gamma = 1$. As can be seen, the actual γ-factor is close to unity, implying an ideal minority carrier injection.

As an aside, The J-V curves in our experiments are well over 10 times lower than those in similar structures shown in Chapter 2 for the same substrate doping and TiO_2 thickness (Figure 2.21). The higher currents in earlier work may be due to a lower Schottky Barrier height formed when Al/TiO_2/p-Si diodes were made or higher interface recombination, i.e. current mechanism (3). We think current mechanism (3) is not significant in the work presented here because of a refined cleaning procedure and improved deposition system, leading to a higher barrier and/or lower interface recombination (Chapter 5).

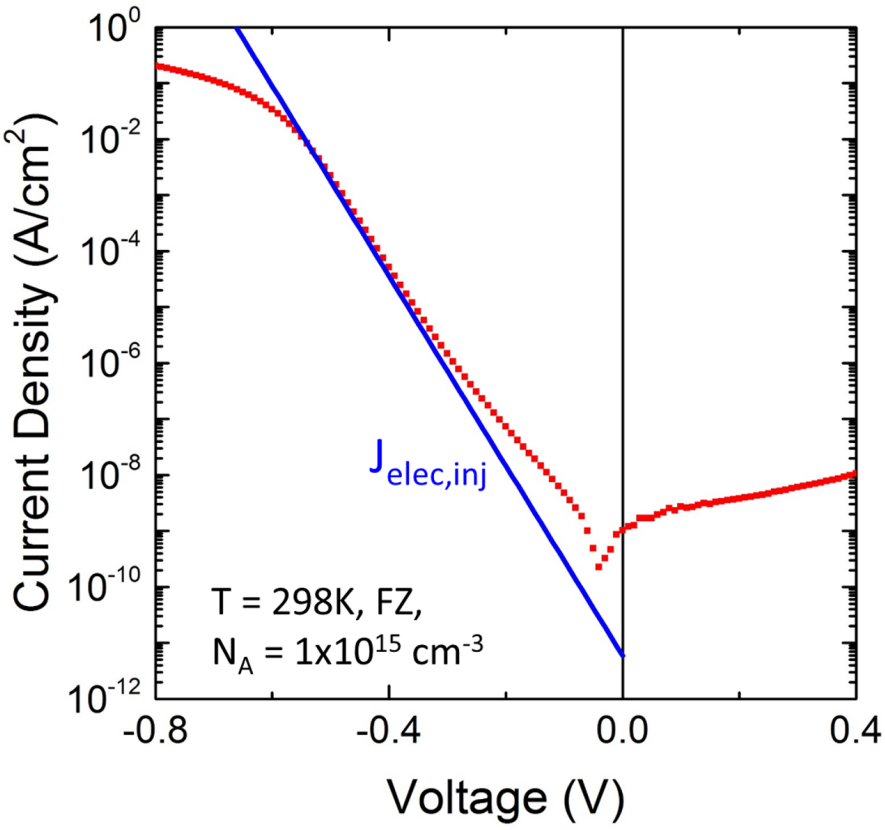


Figure 4.8: J-V characteristics of Al/TiO_2/FZ p-Si (red) and ideal J-V characteristics for injected electron current (blue) using Ln of the wafer thickness (675 μm). TiO_2 thickness is 4 nm. Note the good agreement in the high current region (before roll-off due to series resistance).

All the current mechanisms, their activation energy, and their ideality factor are shown in Table 4.2. Figure 4.11 also shows the relevant current levels for PV conditions (black oval). Furthermore, it is clear that while current mechanism (2) may dominate at lower current levels, current mechanism (1) dominates for PV relevant current levels.

The band diagram and current mechanisms of an Al/TiO_2/p-Si are reproduced in Figure 4.12. For this structure, it can be concluded that current mechanism (1) dominates, and current mechanisms (2) and (5) are irrelevant for PV. Knowing current mechanisms (3) and (4) is still crucial. If a double-sided device with TiO_2 as the frontside electron-selective contact and another material for the backside hole-

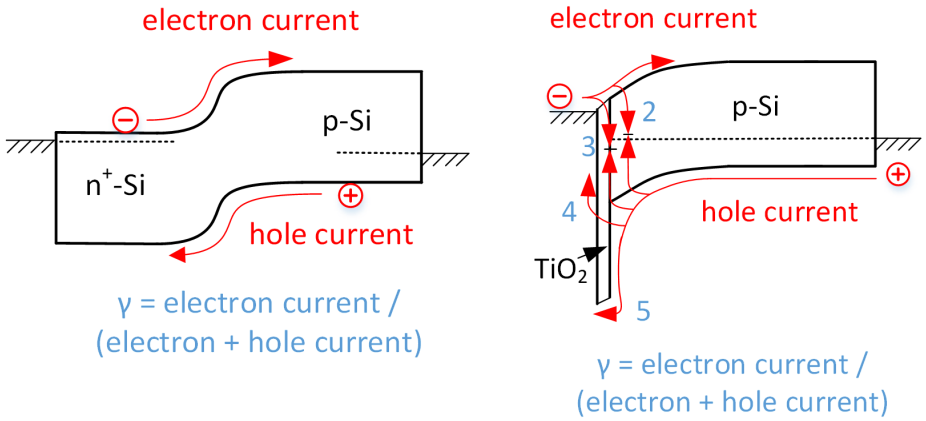


Figure 4.9: Minority carrier injection ratio for (left) n^+-p junction and (right) TiO_2/p-Si junction

Current Mechanism		Activation Energy	η
1. Minority carrier injection	Ideal	1.12 eV	1
2. Recombination in depletion region	Parasitic	0.56 eV	1-2
3. Recombination at interface	Parasitic	S.B. height	1
4. Holes tunneling through TiO_2	Parasitic	1.12 eV	1
5. Holes going over barrier	Parasitic	$>$ 2 eV	1

Table 4.2: Current mechanisms, and respective activation energies and ideality factors across Al/TiO_2/p-Si diode.

selective contact was attempted, the sum of current mechanism (3) and (4) would set an upper limit to V_{OC} by setting an lower limit to J_0 as seen in Figure 4.13. In this figure, it is assumed that current mechanism (1) is blocked completely by the backside hole-selective contact and thus J_0 is set by only current mechanisms (3) and (4).

4.2.1 Separating Minority and Majority carrier components

As the previous section concluded with, a TiO_2/Si diode with 4 nm of TiO_2 is dominated by the electron current component, current mechanism (1). Current mechanisms (2) and (5) are irrelevant for PV conditions (applied voltage of 0.6 V). Thus,

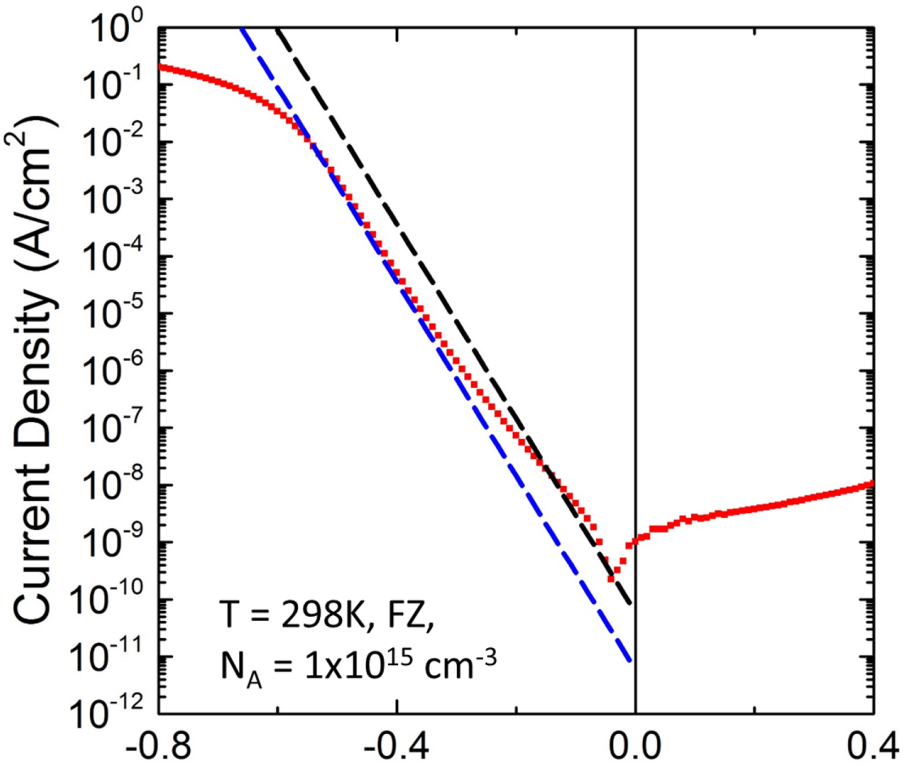


Figure 4.10: J-V characteristics of Al/TiO_2/FZ p-Si (red) and ideal J-V characteristics for injected electron current (blue) using Ln of the wafer thickness (675 μm). TiO_2 thickness is 4 nm.

a new picture emerges, with relevant mechanisms being (1), (3) and (4) as shown in Figure 4.14. Current mechanism (1) will henceforth be known as the electron current component (minority carrier component), while current mechanisms (3) and (4) will be referred to as the hole current component (majority carrier component).

How large are current mechanisms (3) and (4)? In this section, a new method is demonstrated to answer exactly that question.

To demonstrate the utility of this new method, we first start with Figure 4.15, which shows the dark J-V curve of an Al/TiO_2/p-Si diode on a high-lifetime FZ substrate, similar to Figure 4.8, but with a doping of $N_A = 7\text{x}10^{13}$ cm^{-3}. Also shown is the ideal injected electron current of electrons ($J_{elec,inj}$), calculated from 4.1 with L_n replaced by W, the wafer thickness (1000 μm for diode in Figure 4.15). We neglect

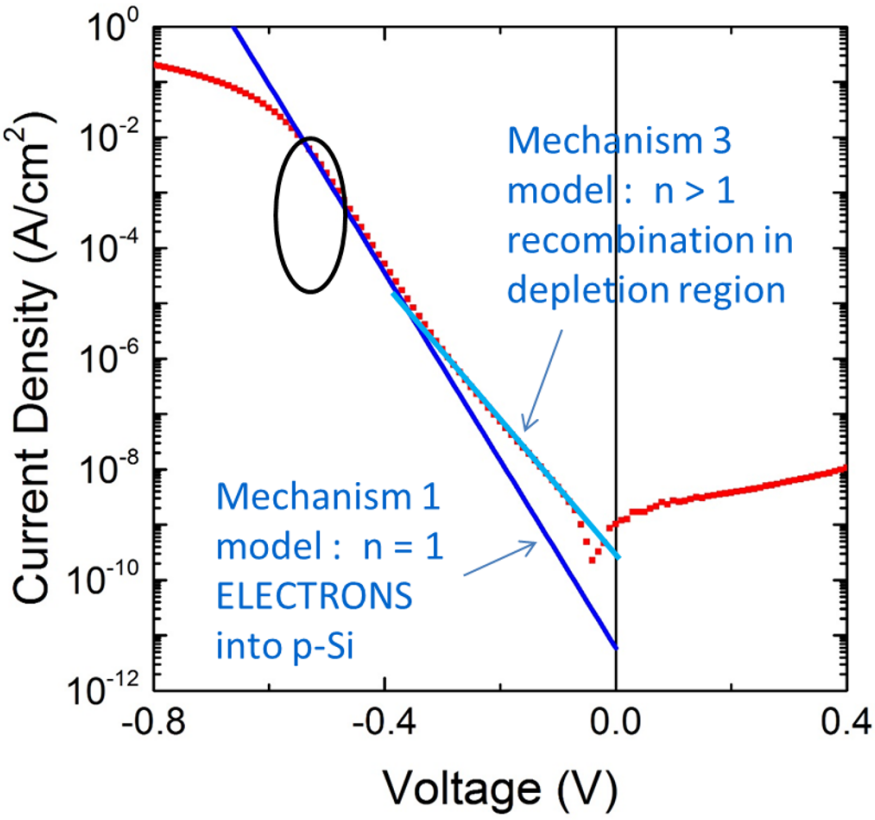


Figure 4.11: J-V characteristics of Al/TiO_2/FZ p-Si showing high-current and low-current regimes

recombination in the substrate bulk due to the high lifetime. With 4 nm 250 °C N_2-annealed TiO_2 deposited on both sides, an effective lifetime of 740 μs was measured using the quasi-steady-state photoconductance decay method. Independent experiments show the lowest interface recombination velocity at the p-Si/TiO_2 interface has a value of ∼50 cm/s, implying a lower bound for the bulk lifetime in the substrate of 2.8 ms. The transit time for an electron to cross the 1 mm base, $W^2/2D$ is 0.15 ms. Thus a short base model for electron current is appropriate.

The modelled injected electron current, which depends on the substrate doping level, is similar to the measured total current. Thus, the hole current, which is the difference between these two, is small. However, from this we can't learn the magnitude of the hole current. The hole current could be nearly as large as the electron current,

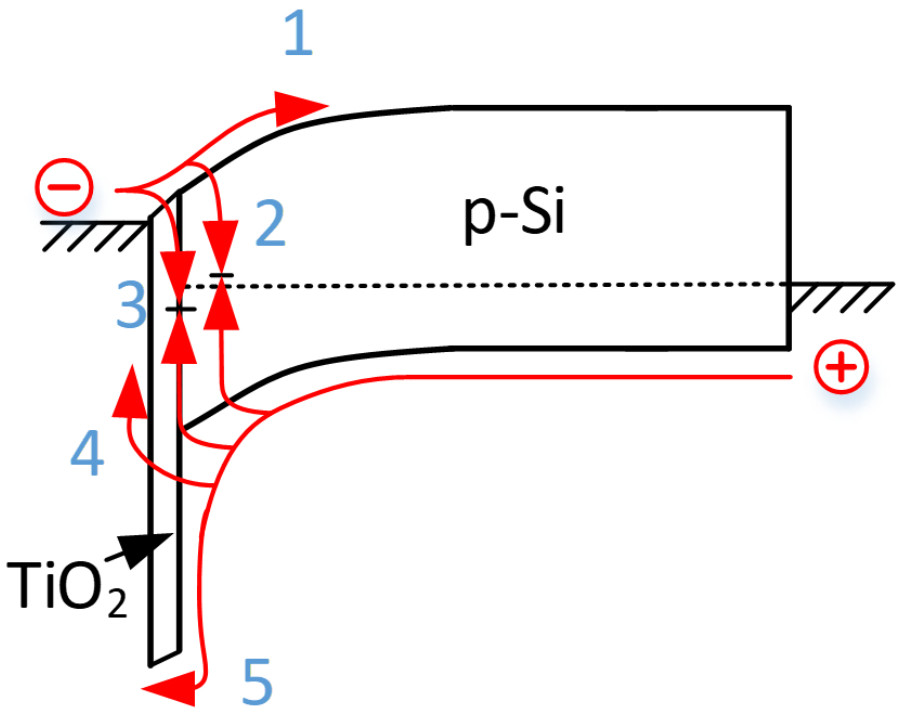


Figure 4.12: Potential current mechanisms in forward bias for Al/TiO_2/p-Si. The Ag provides an ohmic back contact.

or orders of magnitude smaller. In crystalline Si PV, for high lifetime substrates, the injected minority carrier can easily diffuse across the wafer and recombine at the rear contact. Thus, a barrier for the minority carriers (such as a back-side field) is often added at the rear contact to reduce this dark current and raise V_{OC}. This will be effective if the minority carrier current is dominant and other current sources are not significant. This once again highlights the importance of identifying the magnitude of the hole current at the p-Si/TiO_2 interface. To determine the magnitude of the hole current, a new measurement technique, the heterojunction bipolar transistor (HBT), was developed.

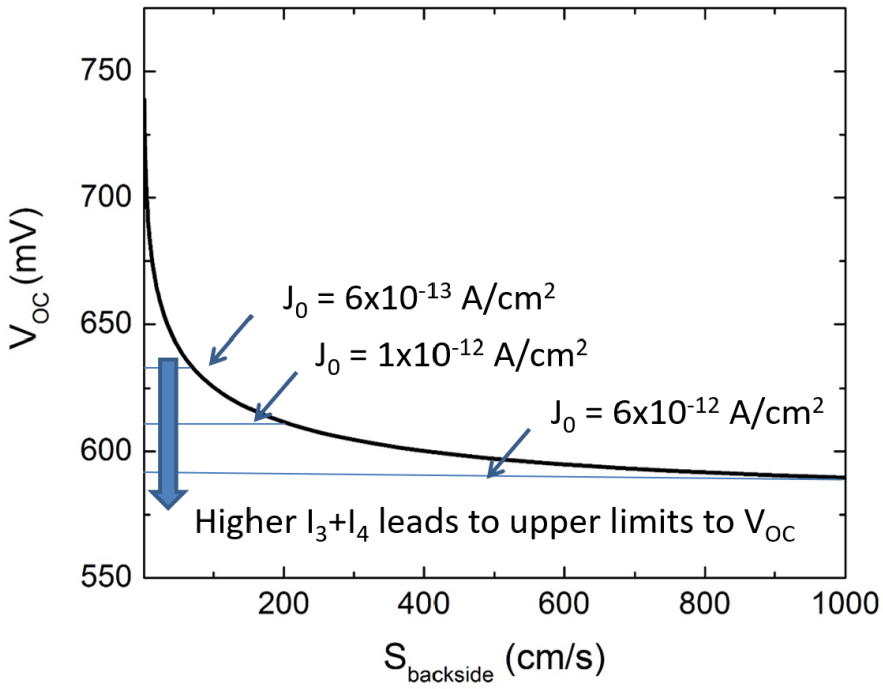


Figure 4.13: Upper limit of V_{OC} due to current mechanisms (3) and (4) for different S_{eff}-values of a backside hole-selective contact ($S_{backside}$. Current mechanism (1) is assumed blocked completely by the backside hole-selective contact

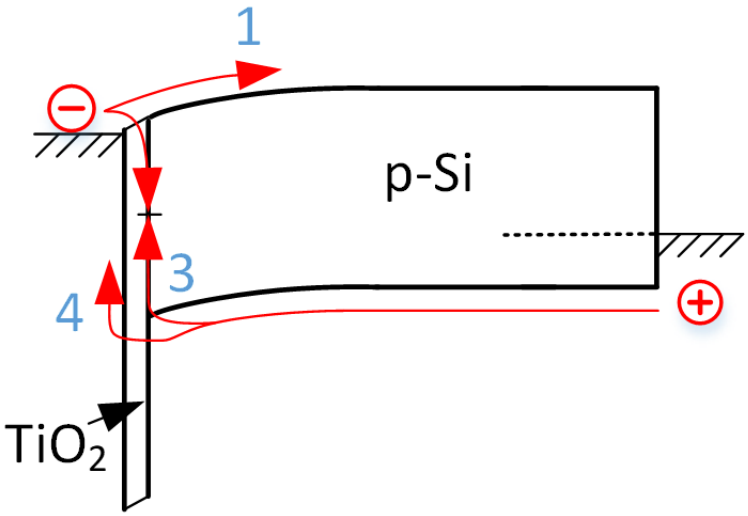


Figure 4.14: Relevant fundamental dark current mechanisms for p-Si/TiO_2/Al selective contact

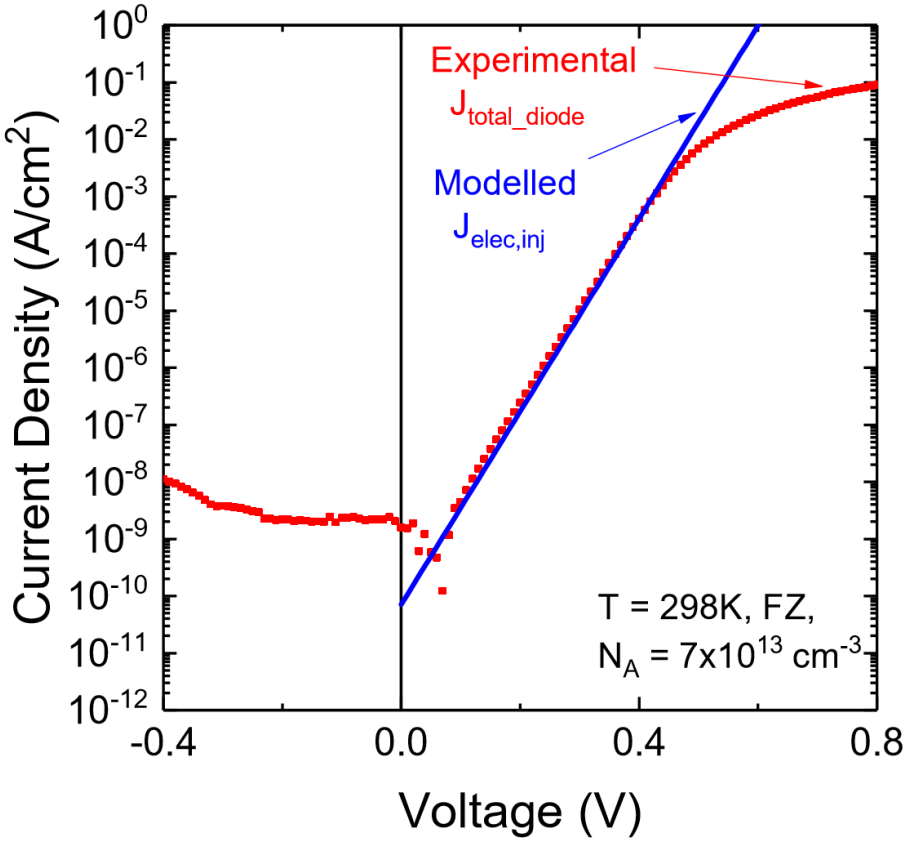


Figure 4.15: Measured J-V characteristics of FZ p-Si/TiO_2/Si (red) and modelled ideal J-V characteristics for injected electron current (blue). TiO_2 thickness is 4 nm.

4.3 Heterojunction Bipolar Transistor (HBT) Using Al/TiO_2/Si as the Emitter Contact

4.3.1 Heterojunction Bipolar Transistor Structure, Concept and Fabrication

We now demonstrate an npn HBT device using Al/TiO_2/Si as the emitter contact so that no n-type silicon region is required in the emitter at all. Thus, consider a heterojunction bipolar transistor where the n^+ emitter of a conventional n^+/p/n device (Fig. 3a) is replaced with an Al/TiO_2 selective contact (Fig. 3b). As in the conventional BJT device, under forward bias on the emitter-base and reverse or zero bias on the base-collector, electrons are injected into the p-type base, diffuse across the base, and are collected to become collector current (I_C). Hole current from base to emitter (I_B) originates from the base contact. The total current across the emitter-base junction, the emitter current (I_E), is the same as the total current across an Al/TiO_2/Si heterojunction device.

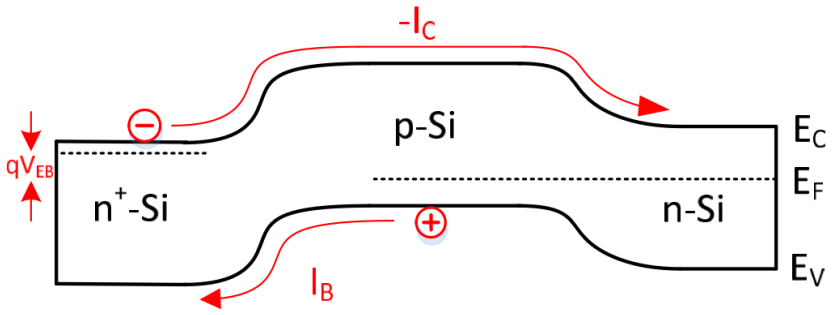


Figure 4.16: npn Bipolar Junction Transistor band diagram and current processes

Thus, the hole current, representing current mechanisms (3) and (4) in Figure 4.14 can be measured as base current I_B, independent of the electron current across the selective contact, assuming neglible leakage at the base-collector junction. I_B can

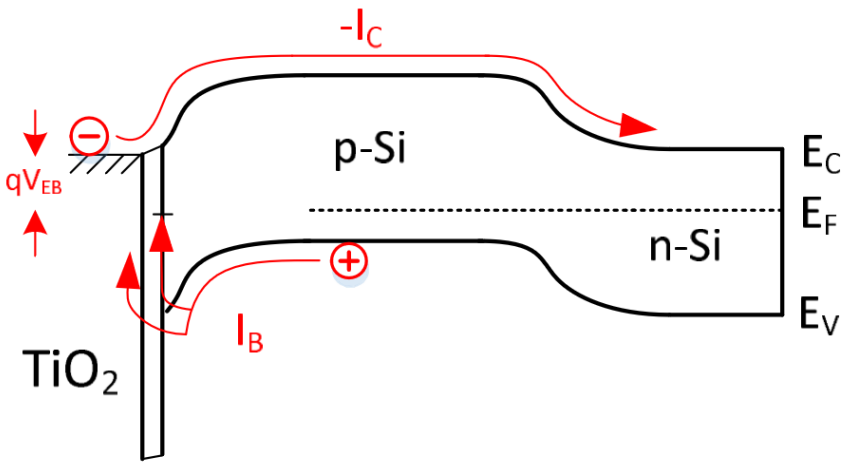


Figure 4.17: TiO_2/pn Heterojunction Bipolar Transistor Band diagram and current processes

also include base region recombination, an issue that will be addressed later in this chapter. Note that this independent measurement of electron and hole currents was not possible with the diode device of Figure 4.14.

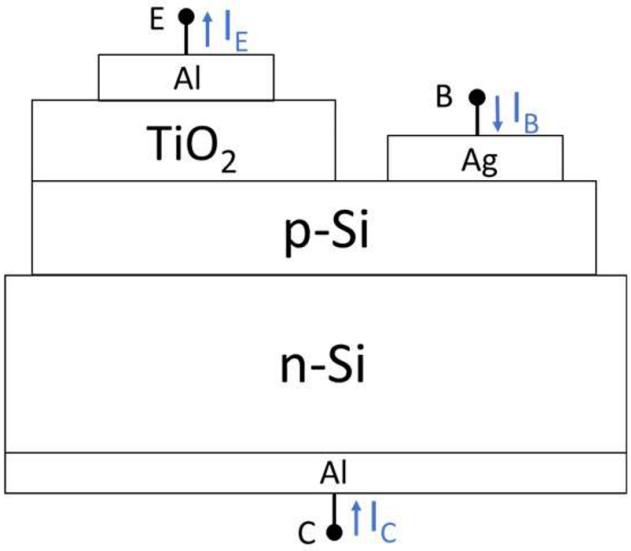


Figure 4.18: Cross section of HBT device with n-type Si substrate, p-type Si base and Al/TiO_2 electron-selective contact to the base as the minority carrier emitter.

The HBT device was fabricated by starting with an epitaxial p-type base (doping of 5x10^{14} cm^{-3}, width of 6 μm) on an n-type substrate (doping of 3x10^{18} cm^{-3}). Device structure is shown in Figure 4.18. The wafers were purchased from El-Cat, Inc. and SIMS measurements were performed by Evans Analytical Group to confirm both epitaxial p-type base and n-type substrate doping. The concentration of ^{11}B dopants versus depth (from top surface) is shown in Figure 4.19. The bulk lifetime of the epitaxial p-type region was unknown, however base recombination was found to be negligible in section 4.3.3. The area of the base-collector junction was isolated by mesa etching. Shadow masks were used to define the areas of the silver base contact, the TiO_2 deposition, and the Al emitter contact. The emitter area was 0.1 cm x 0.1 cm, and the base area 0.35 cm x 0.35 cm. Fabrication process conditions (step by step explanation) is given in Appendix A. The TiO_2 was deposited using the glass bulb for TiO_2 thickness of 4.1 nm and the large glass-steel bulb, with throttle valve at an angle of 30° for thicknesses greater than 4.1 nm. No annealing was done for these HBT devices (and concomitant diodes).

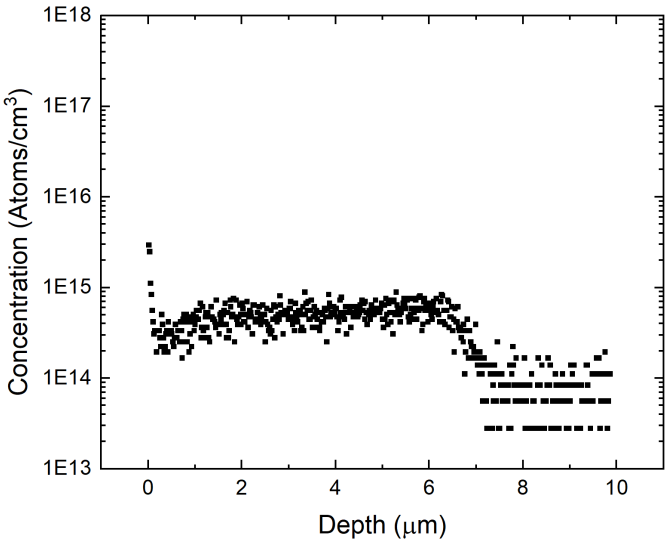


Figure 4.19: Concentration of ^{11}B dopants versus depth in HBT substrate, showing an average doping of 5x10^{14} cm^{-3} for a width of 6 μm. Past 6 μm, the measurement reaches its lower detection limit.

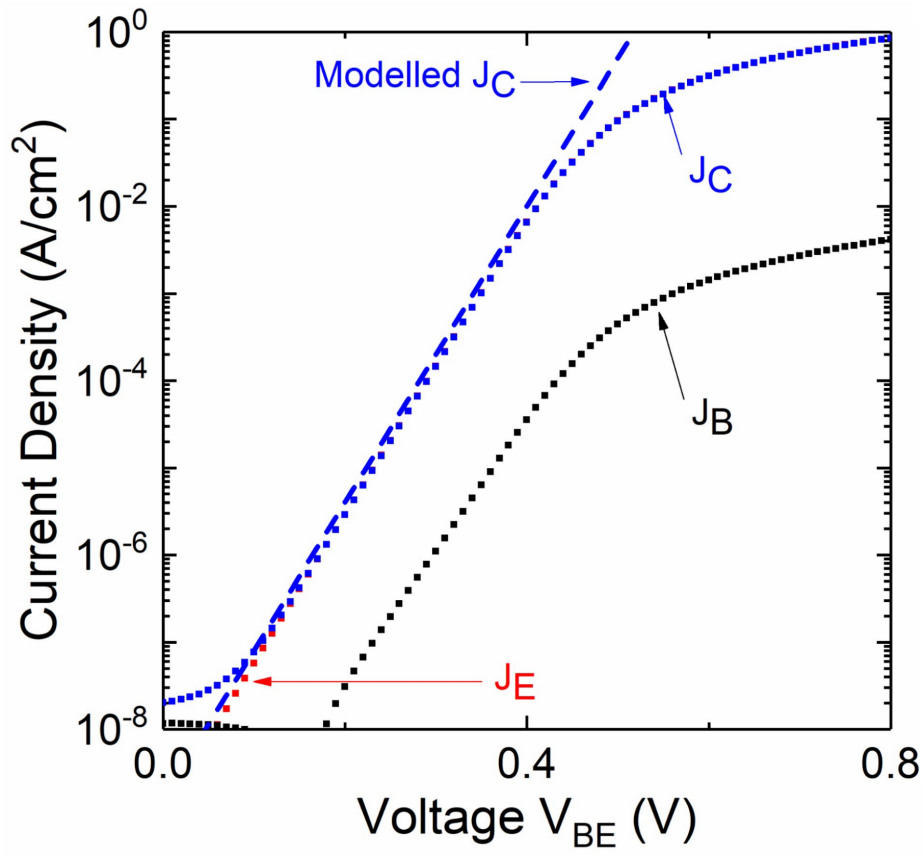


Figure 4.20: Gummel plot of J_C and J_B vs base-emitter bias for the HBT of Fig. 4, for $V_{BC} = 0$. J_E is show in red, J_C in blue and JB in black.

4.3.2 HBT Gummel Plots

HBT Gummel plots of J_C and J_B vs V_{BE} in forward-active mode ($V_{BC} = 0$ V) for TiO_2 thickness equal to 4.1 nm are shown in Figure 4.20. Before the effects of series resistance, the collector current has an ideal slope of ideality factor n = 1.0, while the slope of the base current reflects n = 1.12. The current gain (collector current /base current ratio) is as large as 220. As the base current is so small in comparison to the collector current, the emitter current matches the collector current for almost the entirety of the plot. However, the focus here is not to make a practical transistor, but rather to isolate different current mechanisms. The large collector current in Figure 4.20 represents electrons injected from emitter to base and diffusing across the

base. A dotted line is shown modeling this current with the classical equation for collector current (J_C), assuming 100% base transport factor:

$$J_C = \frac{qn_i^2 D_n}{N_A W_B}\left(e^{\frac{qV_{BE}}{kT}} - 1\right) = J_{0,c} * \left(e^{\frac{qV_{BE}}{kT}} - 1\right) \tag{4.2}$$

where N_A is the base doping (5x10^{14} cm^{-3}), and W_B is the neutral base width (6 μm). Note that replacing N_A and W_B with substrate doping and substrate thickness would give the diode electron current of 4.1.

4.3.3 Quantifying Base Recombination

The base current (J_B) of the device is far smaller than J_C, and represents the current of holes from the p-type base to the emitter contact (Si/TiO_2 selective contact mechanisms 3 and 4 in Figure 4.14), as well as any possible recombination of electrons in the base. To see if recombination is significant, Figure 4.21 shows the classic common-emitter curves for the HBT (I_C vs V_{CE} for base current steps of 0.1 μA.). A current gain of 50 is seen. (The reduction of I_C below V_{CE} 0.25 V is expected for a low common-base current gain in the reverse direction αR, caused by the large base-collector area vs. base-emitter area ratio.) I_C rises in reverse bias due to modulation of the base width by V_{CE} (Early Effect) [57].

This rise can have two origins: (i) as the base narrows (for a fixed V_{BE}), the collector current rises due to a higher electron concentration gradient in the base, and (ii) if the base current is dominated by recombination in the neutral base, reducing the base width will reduce the base current for fixed V_{BE}, causing a further increase in I_C.

To elucidate these two causes, in Figure 4.21, in addition to the usual curves of I_C for fixed I_B, we add one curve of I_C for fixed V_{BE} (0.25 V). In the case of a curve for fixed V_{BE}, as the fractional base width decreases, I_C increases by the same fraction.

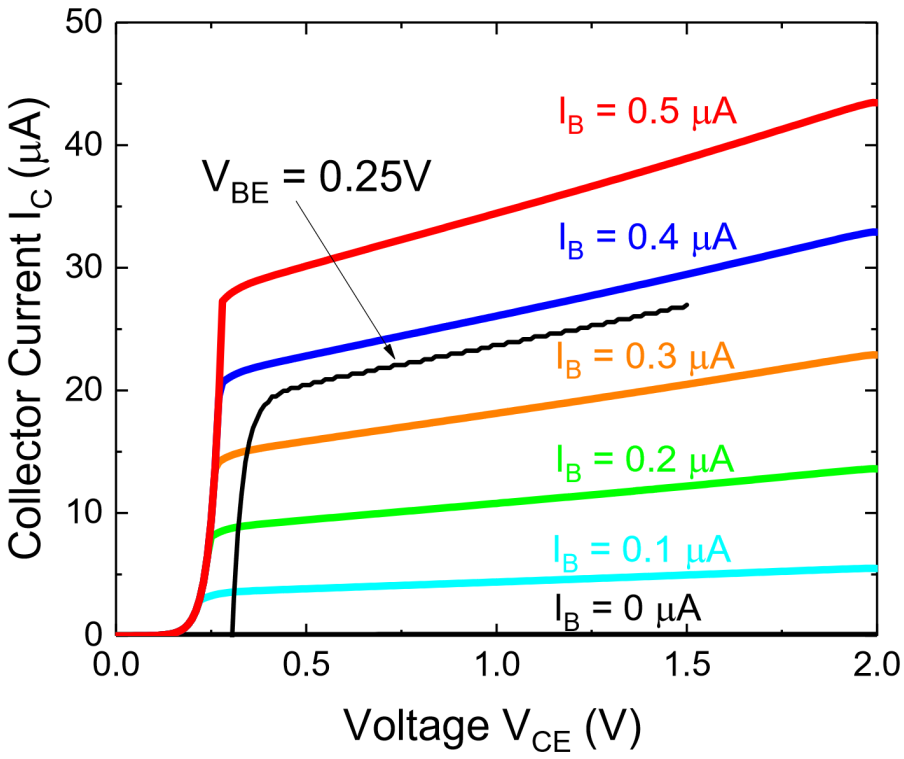


Figure 4.21: Common-emitter curve of TiO_2 HBT

For fixed I_B, there is a second effect if the base current is dominated by recombination in the base. The fractional decrease in the base width would cause the base current to decrease. V_{BE} must then increase to raise the electron concentration on the emitter side of the base by the same base width reduction fraction, to keep the base current fixed. This further increases I_C compared to the fixed V_{BE} effect. Thus one can determine the amount of base recombination ($I_{B,recomb}$) from comparing the fixed I_B and fixed V_{BE} curves.

It follows (formally derived in Appendix B) that the ratio of the slopes of I_C vs V_{CE} for fixed I_B vs fixed V_{BE} conditions for a given I_C is:

$$\left\{ \frac{\frac{dI_C}{dV_{CE}}|_{fixed\ I_B}}{\frac{dI_C}{dV_{CE}}|_{fixed\ V_{BE}}} \right\} = 1 + \frac{I_{B,\ recomb}}{I_B} \tag{4.3}$$

From the data of Figure 4.21, this ratio of the slopes is determined to be at most 1.05. From equation 4.3, this implies at most only 5% of the base current is due to recombination of electrons in the neutral base. Thus, we reach the important conclusion that the base current I_B represents hole current at the selective contact mechanisms (3) and (4). In other words, the sum of current mechanisms (3) and (4) can now be directly measured!

4.3.4 Comparing HBT and Diode J-V to Determine Current Mechanisms for Al/TiO_2/p-Si Diodes

Diodes (device structure in Figure 4.1) and HBT devices (Figure 4.18) were fabricated simultaneously, as to be able to make direct comparisons between diode and HBT data vis-a-vis fabrication conditions. The total diode current density is given by:

$$J_{total,diode} = (J_{p0} + J_{n0,diode}) \ * \ \left(e^{\frac{qV}{kT}} - 1\right) \tag{4.4}$$

where $J_{n0,diode}$ is the saturation current density in equation 4.1. The total HBT current density is given by:

$$J_E = (J_{p0} + J_{n0,HBT}) \ * \ \left(e^{\frac{qV_{BE}}{kT}} - 1\right) \tag{4.5}$$

where $J_{n0,HBT}$ is the collector current saturation density $J_{0,c}$ in equation 4.2. The base current density J_B is given by:

$$J_B = J_{p0} \ * \ \left(e^{\frac{qV_{BE}}{kT}} - 1\right) \tag{4.6}$$

Thus, from equations 4.4-4.6, we see that the base current of the HBT represents the hole current from substrate to the cathode of the diode device of Figure 4.15, specifically recombination at the p-Si/TiO_2 interface and/or tunneling into or through

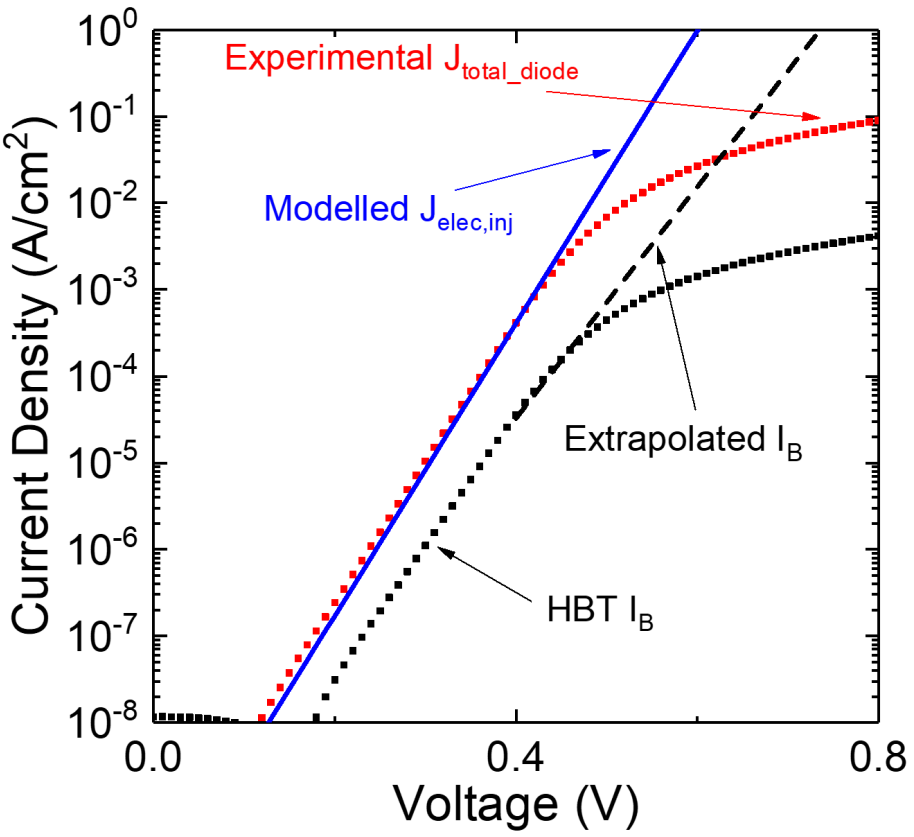


Figure 4.22: J-V of rectifying selective contact and modelled electron current of Figure 4.15, along with base current of HBT representing hole current at the p-Si/TiO_2/Al selective contact (4.1 nm TiO_2).

the TiO_2 layer (current mechanism 3 and 4). To show the utility of this approach for PV, in Figure 4.22 the HBT J_B is overlaid on the rectifying selective contact diode current of Figure 4.15. The roll-off of the HBT J_B above V_{BE} = 0.5 V is due to excessive lateral base resistance. Near V = 0.4 V, the HBT base current (hole current in the selective contact) is $\sim$ 12X smaller than the electron current.

Or in other words the hole current is 8% of the total current, thus a) proving TiO_2/Si is an electron-selective contact and b) quantifying the hole current component. Thus, considering the structure and device of Figures 4.1 as a PV device, to reduce dark current to raise V_{OC}, one needs to introduce an electron blocking selective contact (or a BSF p/p^+ junction) at the substrate ohmic contact, or use higher

substrate doping. If the device were so improve to reduce the electron dark current by $\sim$ 12X, the hole current and electron dark currents would be comparable. This implies an improved electron-blocking hole-selective contact to reduce hole current would be necessary for substantial further dark current reduction. And even with a perfect hole-selective contact, the resulting minimum of the dark current would be the hole current, thus highlighting the importance of isolating and characterizing the hole current.

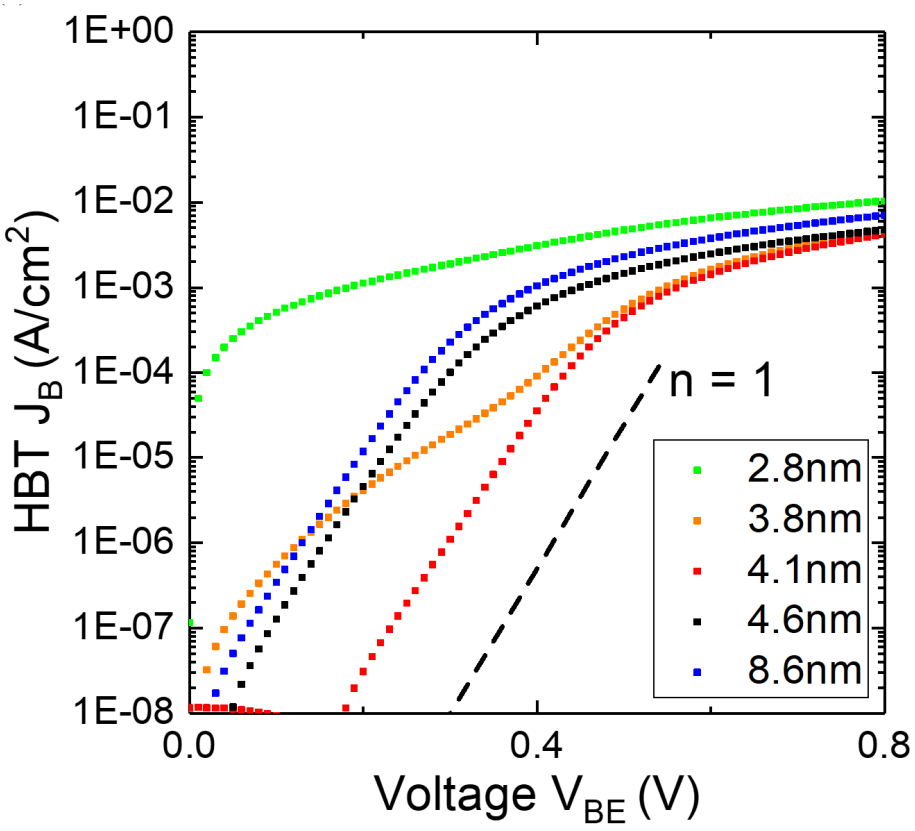


Figure 4.23: HBT base current J_B in forward-active mode, representing hole current at the p-Si/TiO_2/Al selective contact for different TiO_2 thicknesses (from 2.8 to 8.6 nm). The dotted line denotes a slope with an ideality factor of 1.

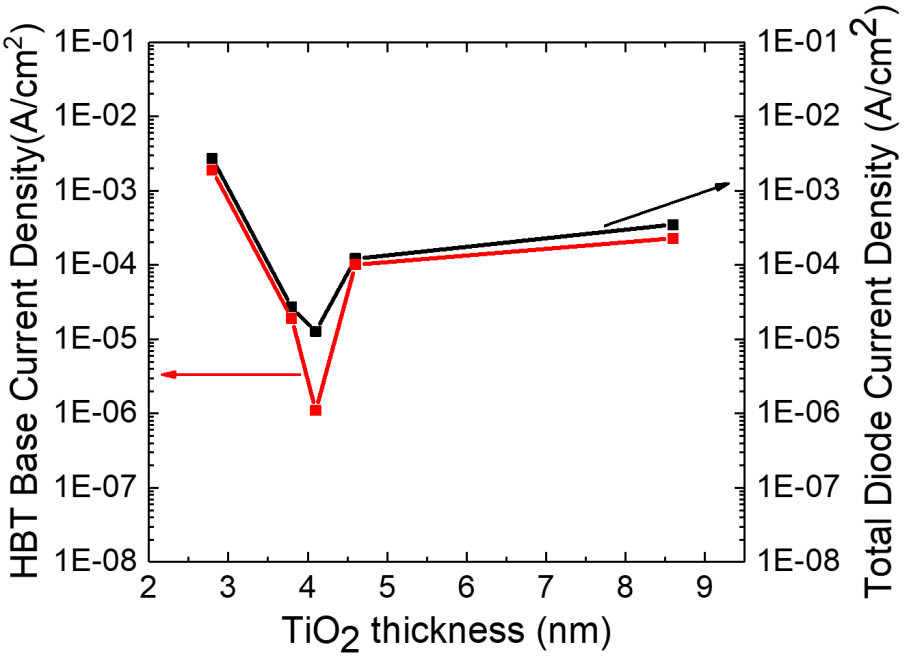


Figure 4.24: Comparison of hole current from p-Si to Al/TiO_2 emitter contact (HBT J_B from Figure 4.22) at $V_{BE} = 0.3$ V, and diode current in rectifying selective contacts (p-Si/TiO_2/Al) as in Figure 4.15 for forward bias = 0.3 V) for TiO_2 thicknesses from 2.8 to 8.6 nm.

4.3.5 Dependence of Hole Current at Al/TiO_2/p-Si Diode on TiO_2 Thickness

To further show the utility of the HBT approach for independently measuring hole current in an electron-selective contact, both HBTs and diodes were made with different TiO_2 thicknesses (2.8 nm to 8.6 nm). Figure 4.23 shows a HBT J_B current vs V_{BE} for the different thicknesses. Initially, as the TiO_2 thickness increases, the hole current drops. This is to be expected as tunneling current is reduced (mechanism (4)) and/or as surface passivation is improved (mechanism (3)) [58,59]. For the diode with TiO_2 thickness of 3.8 nm, space-charge region combination dominates at low current levels (the second diode in the double diode model as shown in Figure 4.5), similar to the diode data shown in Figures 4.2,4.3,and 4.4. The HBT J_B data comparison with diode total current data (at applied voltage V = 0.3 V) is shown in Figure 4.24.

For TiO_2 thickness below 4.1 nm, the diode current matches the HBT base current, showing that the diode is dominated by the hole current. At 4.1 nm, note the hole current is at its minimum, and the PV device is dominated by electron current. For TiO_2 thicknesses above 4.1 nm, the base current (hole current) and the diode current rises quickly again, and again the diode device is dominated by hole current. This shows there is a narrow TiO_2 thickness window for the performance of a p-Si/TiO_2/Al selective contact from a PV point of view.

The perhaps counter-intuitive increase of hole current at high TiO_2 thickness will be explored in Chapter 5. In brief however, one possible explanation for the rise of the hole current is the presence of fixed negative charge in the TiO_2 layer which has been observed in the literature [48]. Negative charge would push the silicon bands up at the TiO_2/Si interface, thereby reducing the barrier holes see and thus increasing the hole current component caused by mechanism (3) (a lower barrier would enable more holes to get to the interface where they could recombine at interface states). To test this hypothesis, current-voltage-temperature (I-V-T) measurements were done on the HBTs with TiO_2 thickness 4.1, 4.6 and 8.6 nm. Figure 4.25 shows I-V-T data for 4.1 nm. From these I-V-T measurements of the HBT I_B current, we were able to extract a Schottky barrier height of 1.01, 0.83 and 0.78 eV respectively for devices with TiO_2 thickness of 4.1, 4.6 and 8.6nm, thus validating the hypothesis that with thicker TiO_2 the silicon bands are being pushed up.

Finally, a comment on the practical utility of using an Al/TiO_2/p-Si structure to replace an n^+-p junction in a solar cell. A key figure of merit is the hole current in such a strucutre, as it sets a lower limit to the dark current and thus the upper limit to V_{OC}. From figure, we observe this minimum to occur at a TiO_2 thickness of 4.1 nm with a J_0 of 7.4x10^{-12} A/cm^2. By equation 1.9, this would limit V_{OC} to 0.58 V (low-level injection conditions). High quality diffused n^+-p junctions have hole saturation current levels below 10^{-13} A/cm^2. Thus an Al/TiO_2/p-Si emitter needs a further

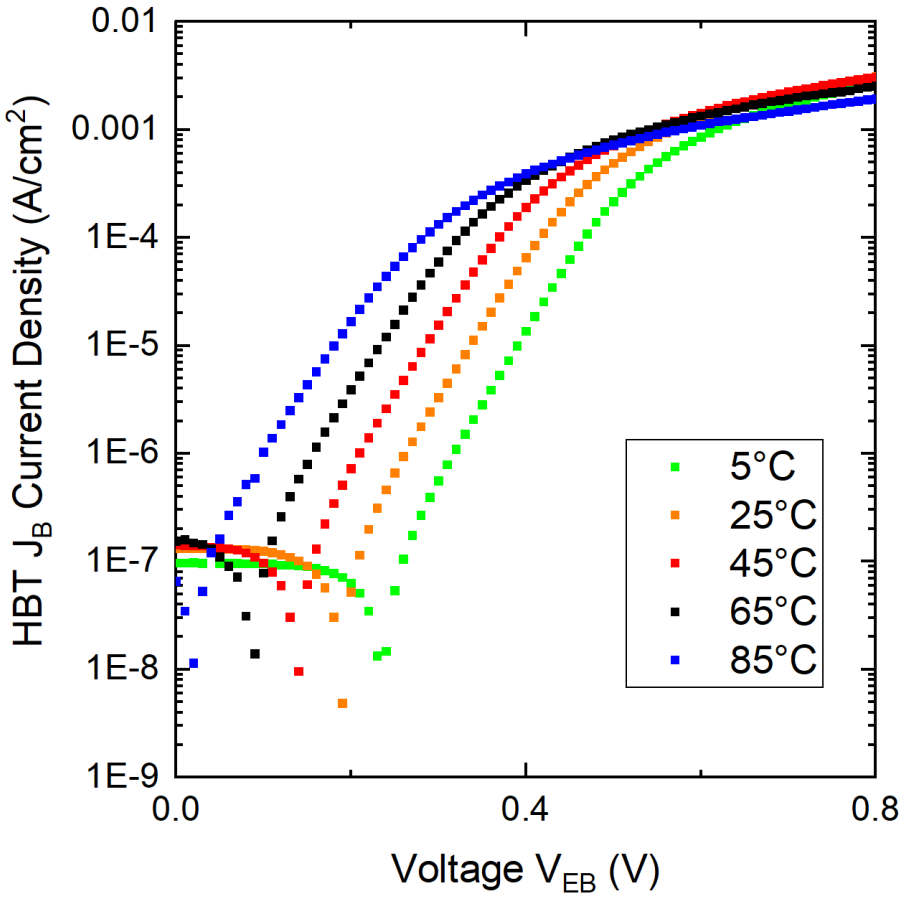


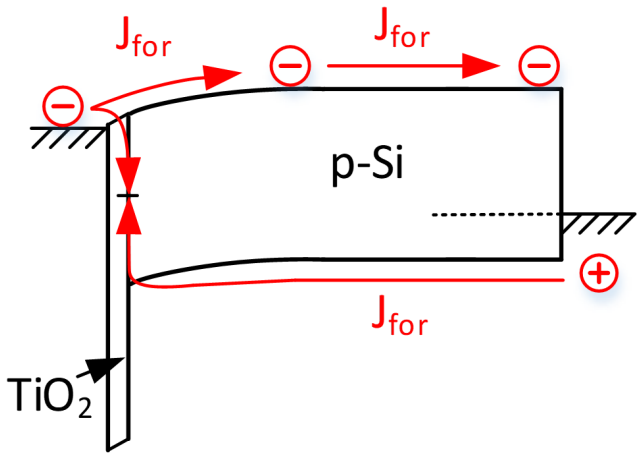
Figure 4.25: J-V characteristics for 4.1 nm TiO_2/p-Si HBT JB for different temperatures.

reduction in hole current (probably current mechanism (3), interface recombination current) to match the state-of-the-art cells.

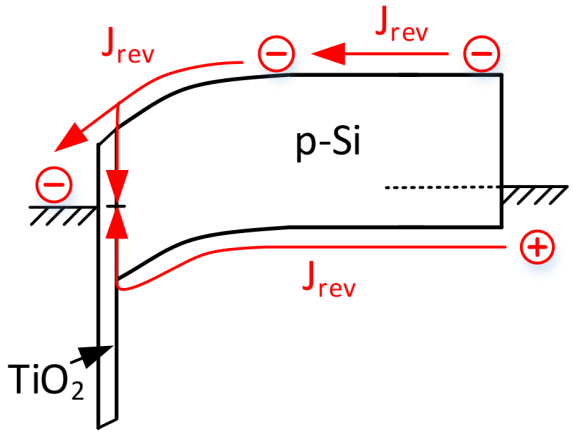
4.3.6 Reverse-Recovery Experiments

To provide independent confirmation that the current of the 4.1 nm TiO_2/p-Si diode is dominated by electron current, reverse recovery experiments were conducted. In a reverse recovery experiment, after steady state in forward bias, the voltage of a diode in series with a resistor is switched from positive to negative. In forward bias, electrons accumulate Figure 4.26a, leading to a particular excess electron profile, which in turn determines the electron current. When the applied voltage is rapidly

switched to reverse bias, the excess electron profile initially supports a reverse current many orders of magnitude higher than the device reverse-saturation current as the excess carriers are recovered (Figure 4.26b), with the current level set by the applied bias and the resistor [60, 61]. However, in time, the stored electrons are depleted, and the current decreases. From these measurements and modelling, one can infer the total number of electrons in the substrate in forward bias [62]. A characteristic parameter for reverse recovery experiments is the recovery time (t_R), which is the time at which the reverse current begins to decrease from its initial value.



(a)



(b)

Figure 4.26: Reverse recovery experiment: (a) Device under forward bias (b) Device under reverse bias

The minority carrier injection ratio (commonly known as γ), mentioned previously, is the ratio between minority carrier (electron) current and total current. In forward bias, recombination of electrons in defects at the Si/TiO_2 interface would cause γ to be reduced: the current of electrons injected into the substrate would be less than that of the total current, and the recovery time would be reduced for a fixed initial forward current. During the recovery phase, interface recombination would further reduce the recovery time (Figure 4.26b). Figure 4.27 shows our recovery time data for different ratios of forward to reverse bias current. Using numerical models [16], one can fit the data to the minority carrier injection ratio γ. Shown in Figure 4.27 are also modeled recovery times for three values of γ: 0.8, 0.9 and 1. Given the quality of the fitting, γ probably lies between 0.85 and 0.95, implying the ratio of hole current (current mechanisms 3 and 4) is 5% to 15% of the total current. This is in excellent agreement with the HBT-extracted result of the hole component being 8% of the total current as inferred from the data of Figure 4.22.

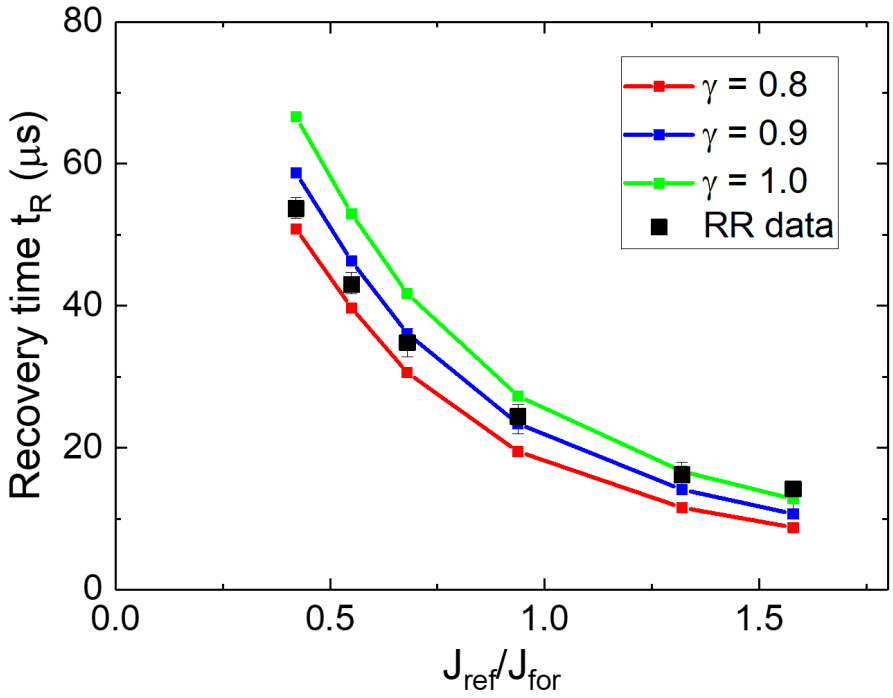


Figure 4.27: Recovery time versus the ratio between forward and reverse current with modelled fitting lines with γ equal to 0.8, 0.9 and 1.0.

4.4 Conclusion

In this chapter, the five current mechanisms across an Al/TiO_2/p-Si heterojunction (Table 4.2) were explored. It has been shown that the dominant current mechanism in an optimized Al/TiO_2/p-Si heterojunction (4 nm TiO_2 layer) is the minority carrier electron injection into the silicon (current mechanism (1)). Current mechanism (5) is negligible due to the large valence band offset between TiO_2 and Si. Current mechanism (2) appears at low applied voltage values, and is not applicable for PV-relevant applied voltage values. Current mechanisms (3) and (4), recombination at the TiO_2/Si interface and tunneling through the TiO_2 layer, are relevant.

To measure the magnitude of the sum of current mechanisms (3) and (4), a heterojunction bipolar transistor (HBT) method was developed. The HBT was utilized to distinguish the hole and electron current across carrier selective contacts, thereby

demonstrating an avenue to elucidate current mechanisms for further PV silicon engineering. Using the HBT technique on a p-Si/TiO_2/Al electron-selective contact, for a 4.1 nm TiO_2, the electron current in a typical PV device is, without an hole-selective contact at the back, more than an order of magnitude larger than the hole current. Reverse recovery experiments confirm the ratio between hole and electron currents. It is also shown that 4.1 nm is the optimal thickness for CVD-deposited TiO_2. However, the resulting hole current is still a factor of 10 higher or more than in high performance Si solar cells, fabricated using traditional "high temperature" technology vs. our approach with a maximum temperature of 100 °C.

Chapter 5

Model of TiO_2/Si Selective Contact as Schottky Contact with Finite Interface Recombination Velocity

5.1 Introduction

In Chapter 2, a new deposition method for amorphous titanium oxide was developed. Chapter 3 optimized the TiO_2 layer for recombination velocity. Chapter 4 looked into the current mechanism across the TiO_2/Si interface and determined that mechanism (1) - ideal minority carrier injection dominates. A new measurement technique was developed to determine the absolute magnitude of mechanisms (3) and (4), recombination at the TiO_2/Si interface and tunneling across the TiO_2 layer. The focus of this chapter is: what determines current mechanism (3) and how can one optimize for it, i.e. reduce it further such that a double-sided heterojunction with TiO_2/p-Si at the front interface would see the maximum V_{OC} increase possible if a hole-selective contact was placed at the backside, replacing a metal contact? Furthermore, what causes the degradation of the I-V characteristics for 250 °C annealed devices, and

why does the current increase for TiO_2 layers thicker than 4.1 nm? These questions will be answered in this chapter by developing an analytical model for the TiO_2/p-Si interface. The key parameters will be identified and the model will be correlated with the data presented so far in this thesis and new data presented in this chapter, tying everything together in a cohesive argument.

5.2 Analytical Model

5.2.1 Schottky Barrier Model

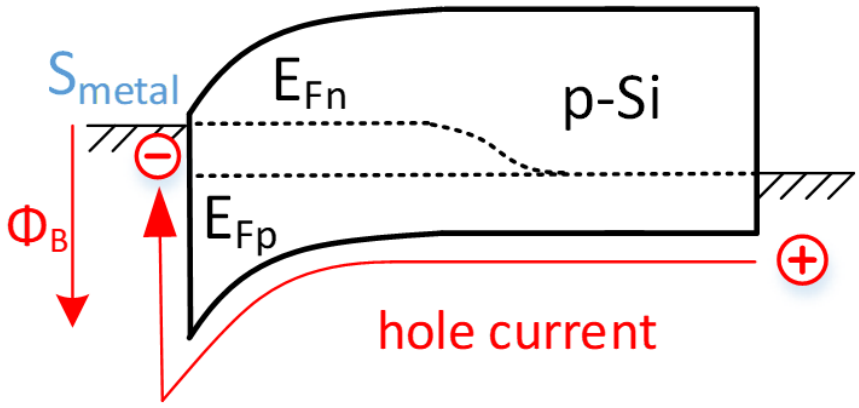


Figure 5.1: Band diagram of metal/p-Si Schottky barrier device and current mechanism under forward bias.

Figure 5.1 shows the well-known band diagram for an Al/p-Si Schottky barrier. The hole current going across the barrier (recombination current at the metal/Si interface) is given by:

$$J = qS_{metal}p' \tag{5.1}$$

where S_{metal} is the recombination velocity for excess majority carriers p' at the Si/metal interface (on the order of 1x10^6 cm/s) [63]. Expanding equation 5.1, one obtains:

$$J = qS_{metal}(p - p_0) \tag{5.2}$$

where p is given by:

$$p = N_V e^{\frac{E_v(x=0)-E_{Fp}(x=0)}{kT}} \tag{5.3}$$

N_V is the effective hole density of states in silicon. p can be expanded to:

$$p = N_V e^{\frac{E_v(x=0)-E_{Fp}(x=0)+E_{Fn}(x=0)-E_{Fn}(x=0)}{kT}} \tag{5.4}$$

Let's assume that at the interface (x=0), $E_{Fn}(x=0) - E_{Fp}(x=0) = qV_A$. Also:

$$E_{Fn}(x=0) - E_v(x=0) = q\Phi_B \tag{5.5}$$

Φ_B is the Schottky barrier height. Thus one obtains for p:

$$p = N_V e^{\frac{-q\Phi_B}{kT}} e^{\frac{qV_A}{kT}} \tag{5.6}$$

and p_0 is given by:

$$p_0 = N_V e^{\frac{E_v(x=0)-E_{Fn}(x=0)}{kT}} \tag{5.7}$$

And p_0 becomes through eq. 5.5:

$$p_0 = N_V e^{\frac{-q\Phi_B}{kT}} \tag{5.8}$$

Combining eqs. 5.6 and 5.8, **one obtains for J**:

$$J = qS_{metal}N_V e^{\frac{-q\Phi_B}{kT}}(e^{\frac{qV_A}{kT}} - 1) \tag{5.9}$$

Another form for J can also be expressed. First, if one writes:

$$qS_{metal}N_V = A^*T^2 \tag{5.10}$$

where A* is the effective Richardson's constant and T is the temperature of the substrate, then one obtains the more well-known classic thermionic emission model:

$$J = A^*T^2 e^{\frac{-q\Phi_B}{kT}}(e^{\frac{qV_A}{kT}} - 1) \tag{5.11}$$

Thus, the two models are equivalent.

5.2.2 Double Schottky Barrier Model

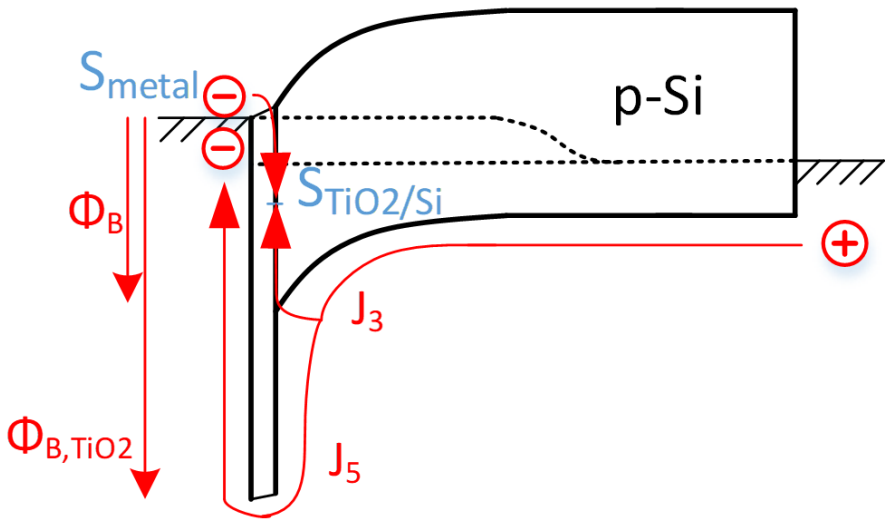


Figure 5.2: Band diagram metal/TiO_2/p-Si double Schottky barrier device

Figure 5.2 shows what happens when we insert a TiO_2 layer in between the metal and the p-Si layer. What we have in effect done is create a "double Schottky barrier",

with the first Schottky barrier being determined by S_{metal} and $\Phi_{B,TiO2}$, while the second Schottky barrier is determined by $S_{TiO2/Si}$ and Φ_B. Also note that in this double Schottky barrier model, the first Schottky barrier is current mechanism (5), while the second Schottky barrier is current mechanism (3).

For the regular Schottky barrier of Figure 5.1, to experimentally reduce J_0 you could only change the metal workfunction and thereby the Schottky barrier height Φ_B. The recombination velocity for a direct metal/Si interface, S_{metal}, is extremely high (1x10^6 cm/s) and cannot be changed substantially. With a TiO_2 layer inserted between the silicon and metal, we now separate the two variables, Φ_B and S_{metal}, into two Schottky barriers. The saturation current density of the first Schottky barrier can in theory (and practice) be reduced by changing the Schottky barrier height $\Phi_{B,TiO2}$ itself - by changing the metal oxide used (with differing E_V offsets), while not having to deal with the tricky issue of a very high metal interface recombination velocity. This was the key thrust to choosing TiO_2 in the first place. The very large valence band offset ensures that this Schottky barrier current is negligible, despite the 1x10^6 cm/s recombination velocity.

The saturation current density for the second Schottky barrier meanwhile can be reduced by passivating the TiO_2/Si interface, $S_{TiO2/Si}$, the key thrust of chapter 3. Note, once again, reducing the recombination velocity is not an option for a direct metal/Si Schottky barrier. But it is an option here due to the fact that a metal oxide/silicon interface can in theory be passivated, and in practice has been passivated.

Let us assume the band bending in the silicon is large enough such that holes are the minority carriers at the TiO_2/Si interface. Thus, in terms of equations, one obtains for J_5:

$$J_5 = qS_{metal}N_{V,TiO2}e^{\frac{-q\Phi_{B,TiO2}}{kT}}(e^{\frac{qV_A}{kT}} - 1) \tag{5.12}$$

where $N_{V,TiO2}$ is the effective hole density of states in the TiO_2 layer, and the prefactor before ($e^{qV_A/kT}$-1) is $J_{5,o}$ is the saturation current density for current mechanism (5). J_3 is given by:

$$J_3 = qS_{TiO2/Si}N_V e^{\frac{-q\Phi_B}{kT}}(e^{\frac{qV_A}{kT}} - 1) \tag{5.13}$$

where the prefactor before ($e^{qV_A/kT}$-1) is $J_{3,o}$, the saturation current density for current mechanism (3). The Schottky barrier height for current mechanism (5), $\Phi_{B,TiO2}$ can be written in terms of Φ_B and $\Delta E_V(TiO_2/Si)$:

$$\Phi_{B,TiO2} = \Phi_B + \Delta E_V(TiO_2/Si) \tag{5.14}$$

Thus the sum of J_3 and J_5 can be written as:

$$J_{3,5} = q(S_{TiO2/Si}N_V + S_{metal}N_{V,TiO2}e^{\frac{-q\Delta E_V(TiO_2/Si)}{kT}})e^{\frac{-q\Phi_B}{kT}}(e^{\frac{qV_A}{kT}} - 1) \tag{5.15}$$

With saturation current density $J_{3,5,o}$ given by:

$$J_{3,5,o} = q(S_{TiO2/Si}N_V + S_{metal}N_{V,TiO2}e^{\frac{-q\Delta E_V(TiO_2/Si)}{kT}})e^{\frac{-q\Phi_B}{kT}} \tag{5.16}$$

The valence band offset between TiO_2 and Si is quite large (2.1 eV), and so one can safely ignore J_5, as was done in Chapter 4. However, as a thought experiment, let us assume we did not know the valence band offset. What would then be the minimum $\Delta E_V(TiO2/Si)$ required for an electron-selective contact such as TiO_2/Si. The next subsection briefly explores this question.

5.2.3 The Relative Importance of $\Delta E_V(TiO2/Si)$

Figure 5.3 shows what happens if there is an infinitely large valence band offset between silicon and TiO_2. The saturation current density $J_{3,5,o}$ is plotted versus the Schottky barrier height Φ_B for different values of $S_{TiO2/Si}$. N_V of 1x10^{19} cm^{-3} was used for silicon. An $S_{TiO2/Si}$-value of 100 cm/s (achievable with room-T annealing) and a Schottky barrier height of 1 eV would give a $J_{3,5,o}$ below 1x10^{-14} A/cm^2, leading to a V_{OC} of 744 mV. A second important fact to note: Φ_B has a greater impact than $S_{TiO2/Si}$. Thus, for device engineering, one should maximize Φ_B first, by choosing an appropriate low workfunction metal before attempting to improve interface passivation.

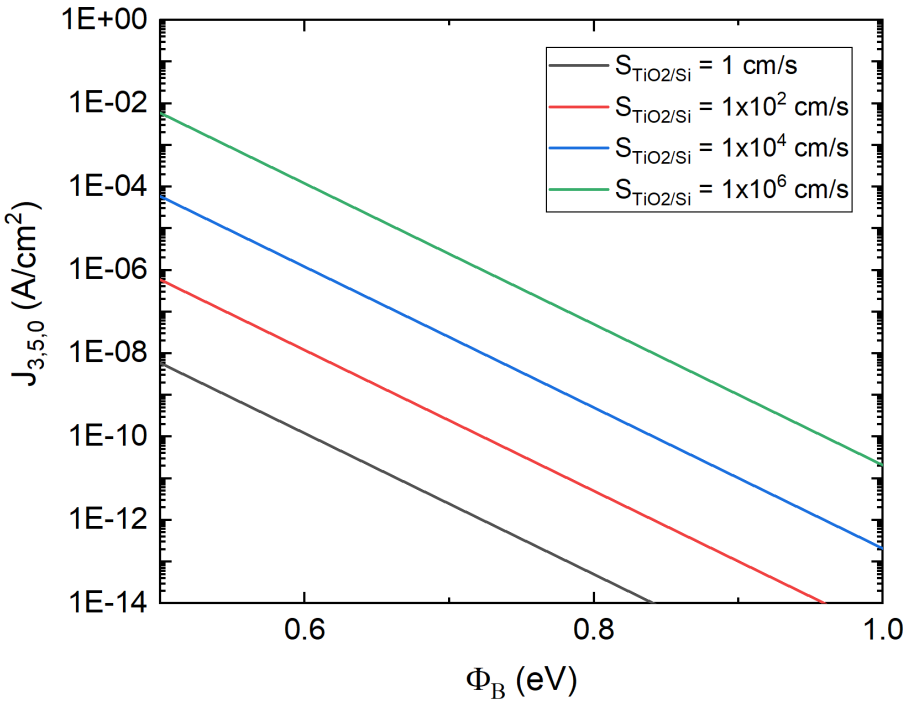


Figure 5.3: Saturation current density $J_{3,5,o}$ versus Schottky barrier height Φ_B for different $S_{TiO2/Si}$-values, with $\Delta E_V(TiO2/Si) = \infty$ eV

Figure 5.4 in contrast shows what happens if there is a small valence band offset of 0.3 eV. The plot is almost the same as that shown in Figure 5.3, except the curve for

$S_{TiO2/Si} = 1$ cm/s has shifted up. The other curves have not shifted at all. What this indicates is that as $\Delta E_V(TiO2/Si)$ gets smaller, J_5 starts to play a role, especially for small $S_{TiO2/Si}$-values. The question now becomes: for small $S_{TiO2/Si}$-values, what is the value of $\Delta E_V(TiO2/Si)$ at which $J_{3,o} = J_{5,o}$. In other words, what is the "minimum" $\Delta E_V(TiO2/Si)$ required for a certain $S_{TiO2/Si}$-value. This is plotted in Figure 5.5, showing $\Delta E_V(TiO2/Si)$ at which $J_{3,o} = J_{5,o}$ for different $S_{TiO2/Si}$-values. A value of 9x10^{19} cm^{-3} for $N_V(TiO_2)$ [64] was used for J_5.

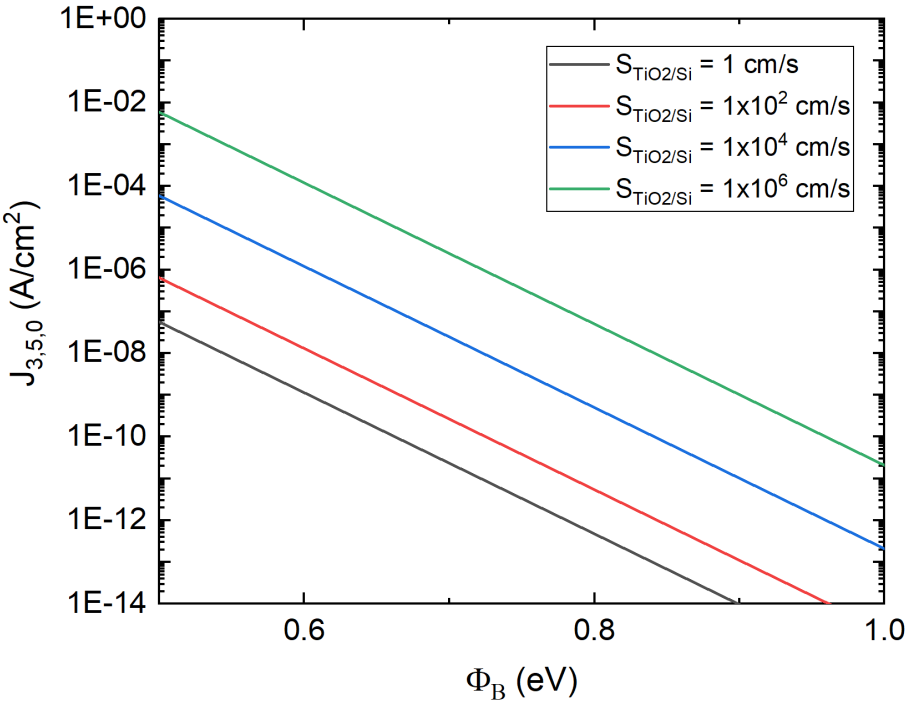


Figure 5.4: Saturation current density $J_{3,5,o}$ versus Schottky barrier height Φ_B for different $S_{TiO2/Si}$-values, with $\Delta E_V(TiO2/Si) = 0.3$ eV

A key finding: A $\Delta E_V(TiO2/Si)$ of slightly larger than 400 meV is enough for even an $S_{TiO2/Si}$-value of 1 cm/s. Thus one does not require a significantly large valence band offset (on the order of multiple eVs). For an $S_{TiO2/Si}$-value of 10 cm/s, $\Delta E_V(TiO2/Si) = 350$ meV will suffice. **And so, J_5 will be ignored moving forward.**

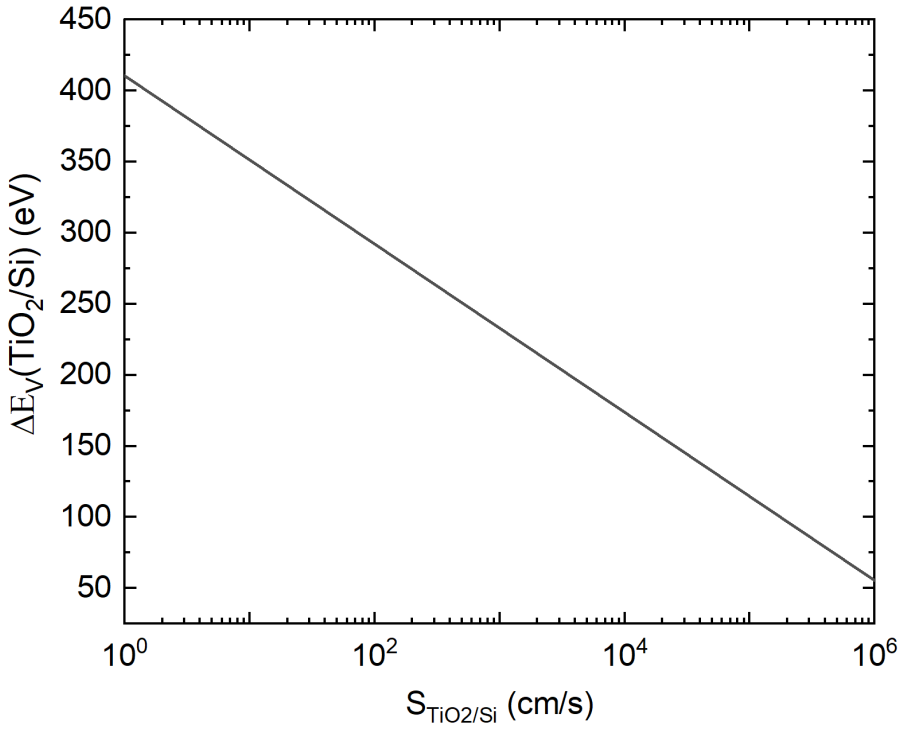


Figure 5.5: $\Delta E_V(TiO2/Si)$ for different $S_{TiO2/Si}$-values at which $J_{3,o} = J_{5,o}$ - showing the minimum valence band offset needed for $S_{TiO2/Si}$-values. For $\Delta E_V(TiO2/Si)$ greater than the value shown for a given $S_{TiO2/Si}$, one can ignore current over the barrier (J_5) relative to the current due to recombination at the interface(J_3).

5.3 "Thermionic-Emission-Diffusion Model" for Hole Current at TiO_2/Si

The equation for J_3 is slightly more complicated than shown in equation 5.13, which only takes into account interface recombination, but not the change in the hole quasi-Fermi level across the depletion region. Equation 5.13 assumes the hole quasi-Fermi level is flat across the depletion region. This cannot be true because a flat quasi-Fermi level implies no hole current across the depletion region. Thus the hole quasi-Fermi level must be higher at the TiO_2/Si interface than in the bulk, and thus E_{Fn}-E_{Fp} at the interface will be smaller than the applies bias V_A, and the hole density p' will be lower and thus the interface recombination current J_3 will be smaller as well.

A more accurate model would be similar to the thermionic-emission-diffusion Theory by Crowell and Sze [65]. The figure describing the key elements of the thermionic-emission-diffusion model is shown in Figure 5.6. This figure shows the TiO_2/Si heterojunction under an applied bias V_A. Under forward bias, one gets Fermi-level splitting in the depletion region, with E_{Fn} and E_{Fp}, the difference being equal to V_A at x = W_D, the edge of the depletion region. At the silicon interface (x = 0), the difference is defined as ΔE_F. E_{Fn} does not change at the silicon interface, while E_{Fp} is the variable. Finally, Φ_B is the Schottky barrier height for current mechanism (3).

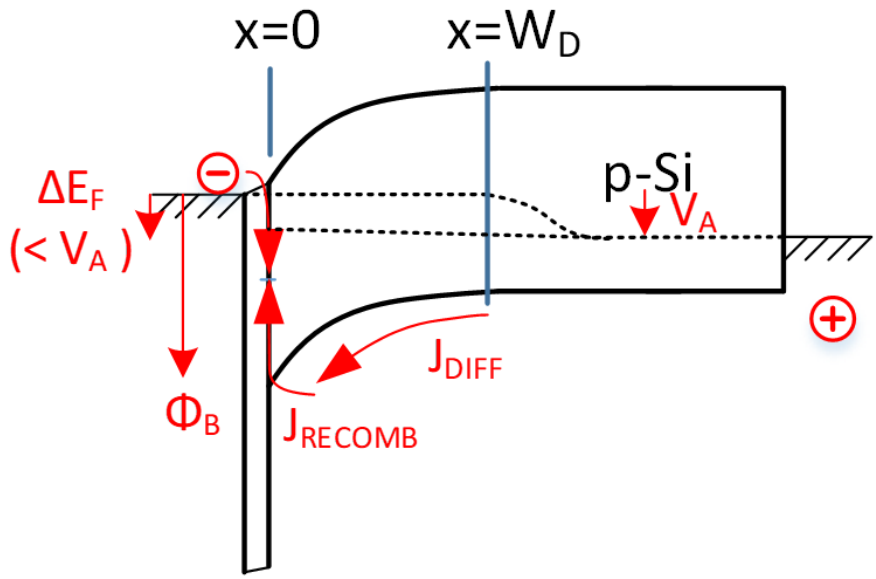


Figure 5.6: metal/TiO_2/Si diode, showing Fermi-level splitting at interface and across depletion region. Note that, in contrast to Figure 5.2, the hole quasi-Fermi level must rise from the bulk to the TiO_2/Si interface to supply holes from the bulk to the interface. This transport of holes across the depletion region is commonly referred to as J_{DIFF}, since it is driven by diffusion.

This section explores the analytical derivation of the equation for current mechanism (3), recombination at the TiO_2/Si interface. This current mechanism could be potentially diffusion-limited. This means that such a large change in E_{Fp} is needed to supply holes to the interface that the lower Fermi-level splitting at the interface

reduces the current from that where no change in E_{Fp} across the depletion region is assumed. As such, one needs find the change in E_{Fp} so that the interface recombination current (J_{RECOMB}) is equal to the hole supply across the depletion region (J_{DIFF}).

To do so, first a new term, ΔE_F, is defined. Next, both J_{RECOMB}, and J_{DIFF} are defined, and finally both currents are set equal to each other to find closed-form equations for both ΔE_F and J_3.

5.3.1 Defining ΔE_F

Thus one gets the following two equations:

$$E_{Fn}(x = 0) - E_{Fp}(x = 0) = \Delta E_F \tag{5.17}$$

$$E_{Fn}(x = W_D) - E_{Fp}(x = W_D) = V_A \tag{5.18}$$

5.3.2 Solving for $\mathbf{J}_{RECOMB}$

The recombination current at the TiO_2/Si interface is given by:

$$J_{RECOMB} = qS_{TiO2/Si}p' \tag{5.19}$$

where S is the recombination velocity for excess majority carriers p'. The derivation of this current has already been done for the simple Schottky barrier case. The only change would be to to use equation 5.17 for the Fermi level splitting at the interface. Thus **one obtains for $\mathbf{J}_{RECOMB}$**:

$$J_{RECOMB} = qS_{TiO2/Si}N_v e^{\frac{-q\Phi_B}{kT}}(e^{\frac{\Delta E_F}{kT}} - 1) \tag{5.20}$$

5.3.3 Solving for $\mathbf{J}_{DIFF}$

The diffusion current in the depletion region (x=0 to x=W_D) is given by:

$$J_{DIFF} = p\mu_p \frac{\partial E_{Fp}}{\partial x} \tag{5.21}$$

Substituting 5.3 for p, we obtain:

$$J_{DIFF} = \mu_p N_V e^{-\frac{E_{Fp}-E_v}{kT}} \frac{\partial E_{Fp}}{\partial x} \tag{5.22}$$

which can be re-arranged to:

$$e^{-\frac{E_{Fp}}{kT}} \partial E_{Fp} = \frac{J_{DIFF}}{\mu_p N_V} e^{\frac{-E_v}{kT}} \partial x \tag{5.23}$$

First, let us add $e^{\frac{E_{Fn}}{kT}}$ to each side to obtain:

$$e^{-\frac{E_{Fp}-E_{Fn}}{kT}} \partial E_{Fp} = \frac{J_{DIFF}}{\mu_p N_V} e^{\frac{E_{Fn}-E_v}{kT}} \partial x \tag{5.24}$$

Integrating both sides from x=0 to x=W_D:

$$\int_{x=0}^{x=W_D} e^{-\frac{E_{Fp}-E_{Fn}}{kT}} \partial E_{Fp} = \frac{J_{DIFF}}{\mu_p N_V} \int_0^{W_D} e^{\frac{E_{Fn}-E_V}{kT}} \partial x \tag{5.25}$$

Solving the integral on the right side gives:

$$-\frac{1}{kT}\left[e^{\frac{E_{Fn}-E_{Fp}(x=W_D)}{kT}} - e^{\frac{E_{Fn}-E_{Fp}(x=0)}{kT}}\right] = \frac{J_{DIFF}}{\mu_p N_V} \int_0^{W_D} e^{\frac{E_{Fn}-E_V}{kT}} \partial x \tag{5.26}$$

Substituting in 5.17 and 5.18:

$$\frac{1}{kT}\left[e^{\frac{\Delta E_F}{kT}} - e^{\frac{qV_A}{kT}}\right] = \frac{J_{DIFF}}{\mu_p N_V} \int_0^{W_D} e^{\frac{E_{Fn}-E_V}{kT}} \partial x \tag{5.27}$$

with $D_p = \mu_p \frac{kT}{q}$:

$$\left[e^{\frac{\Delta E_F}{kT}} - e^{\frac{qV_A}{kT}}\right] = \frac{J_{DIFF}}{qN_V D_p} \int_0^{W_D} e^{\frac{E_{Fn}-E_V}{kT}} \partial x \tag{5.28}$$

As per Taylor and Simmons [66], a new parameter v_h can be defined as:

$$v_h \equiv D_p \left[\int_0^{W_D} e^{\frac{E_{Fn}-E_V}{kT}} \partial x\right]^{-1} \tag{5.29}$$

The exact value of v_h will depend on the form of the barrier (Φ_B). This integral cannot be calculated analytically. Substituting 5.29 into 5.28, **we obtain for J_{DIFF}**:

$$J_{DIFF} = q v_h N_V e^{\frac{-q\Phi_B}{kT}} (e^{\frac{qV_A}{kT}} - e^{\frac{\Delta E_F}{kT}}) \tag{5.30}$$

5.3.4 Finding Expression for ΔE_F

In case of $\Delta E_F = 0$ (no recombination at Si interface), the entire voltage drop (V_A) occurs across the depletion region and the current is completely dominated by the diffusion current. One thus obtains:

$$J_3 \;=\; J_{DIFF} = q S_{TiO2/Si} N_V e^{\frac{-q\Phi_B}{kT}} (e^{\frac{qV_A}{kT}} - 1) \tag{5.31}$$

In case of $\Delta E_F = V_A$, the entire voltage drop occurs at the interface and the current is completely dominated by the recombination current. One thus obtains:

$$J_3 \;=\; J_{RECOMB} = q v_h N_V e^{\frac{-q\Phi_B}{kT}} (e^{\frac{qV_A}{kT}} - 1) \tag{5.32}$$

But what about in between these two conditions? Now that equations have been found for both J_{recomb} and J_{diff}, by setting them equal, one can find a closed form solutions for J_3 and ΔE_F for all conditions. So from:

$$J_{RECOMB} \;=\; J_{DIFF} \tag{5.33}$$

One obtains out of 5.9 and 5.30:

$$q\ S_{TiO2/Si}\ N_V\ e^{\frac{-q\Phi_B}{kT}}\left(e^{\frac{\Delta E_F}{kT}}-1\right) = q\ v_h\ N_V\ e^{\frac{-q\Phi_B}{kT}}\left(e^{\frac{qV_A}{kT}}-e^{\frac{\Delta E_F}{kT}}\right) \tag{5.34}$$

Eliminating common factors on both sides, equation 5.34 simplifies into:

$$S_{TiO2/Si}(e^{\frac{\Delta E_F}{kT}} \;-\; 1) \;=\; v_h(e^{\frac{qV_A}{kT}} \;-\; e^{\frac{\Delta E_F}{kT}}) \tag{5.35}$$

$$S_{TiO2/Si}e^{\frac{\Delta E_F}{kT}} \;-\; S_{TiO2/Si} \;=\; v_h(e^{\frac{qV_A}{kT}} \;-\; e^{\frac{\Delta E_F}{kT}}) \tag{5.36}$$

$$(S_{TiO2/Si} \;+\; v_h)e^{\frac{\Delta E_F}{kT}} \;=\; v_h e^{\frac{qV_A}{kT}} \;+\; S_{TiO2/Si} \tag{5.37}$$

$$e^{\frac{\Delta E_F}{kT}} \;=\; \frac{v_h e^{\frac{qV_A}{kT}} \;+\; S_{TiO2/Si}}{S_{TiO2/Si} \;+\; v_h} \tag{5.38}$$

And thus one gets an equation for ΔE_F as:

$$\Delta E_F \;=\; kTln(\frac{v_h e^{\frac{qV_A}{kT}} \;+\; S_{TiO2/Si}}{S_{TiO2/Si} \;+\; v_h}) \tag{5.39}$$

Substituting 5.38 into 5.9, one obtains for J_3:

$$J_3 = qS_{TiO2/Si}N_v e^{\frac{-q\Phi_B}{kT}}(\frac{v_h e^{\frac{qV_A}{kT}} + S_{TiO2/Si}}{S_{TiO2/Si} + v_h} - 1) \tag{5.40}$$

From which, one gets:

$$J_3 = q\frac{S_{TiO2/Si}N_v e^{\frac{-q\Phi_B}{kT}}}{S_{TiO2/Si}+v_h}(v_h e^{\frac{qV_A}{kT}} + S_{TiO2/Si} - S_{TiO2/Si} - v_h) \tag{5.41}$$

And thus one finally obtains an equation for J_3 as:

$$J_3 = q\frac{S_{TiO2/Si}v_h}{S_{TiO2/Si}+v_h}N_v e^{\frac{-q\Phi_B}{kT}}(e^{\frac{qV_A}{kT}} - 1) \tag{5.42}$$

Figure 5.7 compares J_{DIFF} and J_{RECOMB} for a ΔE_F ranging from 0 eV to a qV_A of 0.6 eV. A Φ_B of 1.01 eV was used based on experimental data (Section 5.4.1). A maximum recombination velocity of 1x10^6 cm/s was used. The crossing point determines the actual value of ΔE_F, and is shown to be almost exactly the same as qV_A of 0.6 eV. This is to be expected as v_h is on the order of 1x10^7 cm/s [67], thus significantly higher than any real value of the TiO_2/Si interface recombination velocity. In other words, for all intents and purposes, equation 5.13 may be used to describe current mechanism (3).

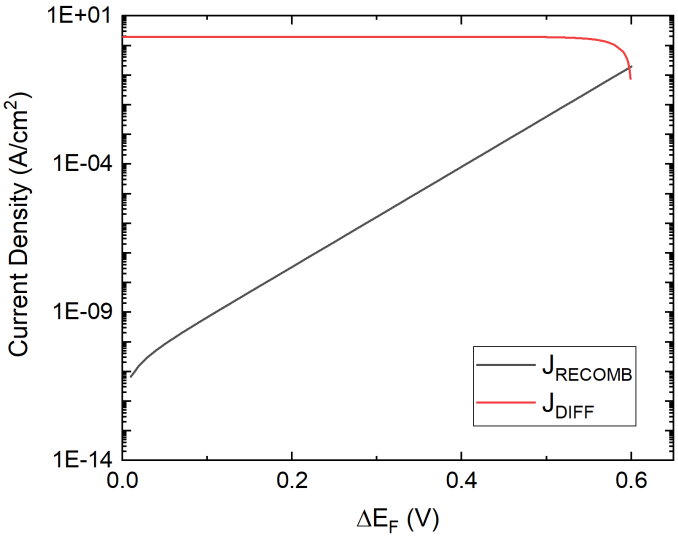


Figure 5.7: J_{DIFF} and J_{RECOMB} versus ΔE_F for an applied voltage of 0.6V, Φ_B of 1.01 eV and v_h of 1x10^7 cm/s - the cross point at 0.598V shows the actual value of ΔE_F, indicating that the change in hole quasi-Fermi level across the depletion region has a negligible effect on current mechanism (3). And thus equation 5.13 accurately describes hole interface recombination.

In Chapter 4, the sum of $J_{3,0}$ and $J_{4,0}$ was determined to be 7.4x10^{-12} A/cm^2 for HBT J_B for 4.1 nm TiO_2. Ignoring $J_{4,0}$ (tunneling current), and with a Φ_B of 1.01 eV for said device from I-V-T measurements in Section 4.3.5, an $S_{TiO2/Si}$ of 4x10^5 cm/s is extracted. This $S_{TiO2/Si}$-value is within the expected range as per lifetime measurements for "as-deposited TiO_2", which degrades rapidly in air, and is almost that of 10^6 cm/s expected for an unpassivated metal/Si contact!

For room-T annealed devices, with an $S_{TiO2/Si}$-value of 28 cm/s, and assuming the same Φ_B of 1.01 eV, one could achieve $J_{3,0}$ of 4x10^{-16} A/cm^2, well below saturation current density levels of high-efficiency silicon solar cells.

In summary, the two key parameters, looking at equation 5.13, are Φ_B, the Schottky barrier height and $\mathbf{S}_{TiO2/Si}$, the recombination velocity at the TiO_2/Si interface (addressed in Chapter 3). Shown in Figure 5.8 is a hypothetical J_0 with known Φ_B and $S_{TiO2/Si}$ (indicated by star). Two pathways are possible to reduce $J_{3,0}$ as shown by the orange arrows - one can either increase Φ_B or reduce $S_{TiO2/Si}$.

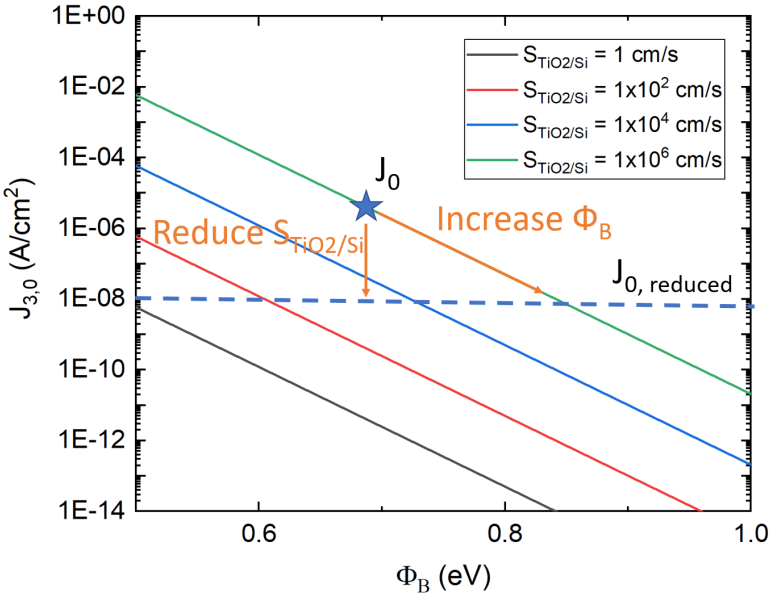


Figure 5.8: Saturation current density $J_{3,o}$ versus Schottky barrier height Φ_B for different $S_{TiO2/Si}$-values. Two pathways (in orange) are shown to reduce a hypothetical J_0, namely increase Φ_B or reduce $S_{TiO2/Si}$.

5.4 Experimental Data

5.4.1 Schottky Barrier Height Extraction from HBT J_B I-V-T

In this section, experimental data are used to corroborate the model previously discussed. As mentioned, the band-bending in the silicon and the corresponding Schottky barrier height ($\Phi_{B,Si}$) is ultimately critical to understanding hole current. Let us first look at I-V-T data from HBT J_B's from Chapter 4. Figure 5.9 shows I-V-T data for 4.1 nm TiO_2/p-Si. One can extract a Schottky barrier height from I-V-T measurements. For increasing TiO_2 thicknesses of 4.1, 4.6 and 8.6 nm, a Schottky barrier height of 1.01, 0.83 and 0.78 eV was obtained.

So what causes the change in Schottky barrier height for thicker TiO_2 layers? One possible explanation could be charge formation.

5.4.2 The Relative Importance of Charge

As mentioned above, the deciding parameter is the Schottky barrier height for holes recombining at the TiO_2/Si interface. This barrier height is normally set by the difference between the metal workfunction and the Si valence band edge. However, the introduction of fixed charge can change the barrier height and the corresponding band-bending in the silicon. Negative charge (as shown in Figure 5.10.a) would lead to silicon bands being pushed up, and thus a smaller Φ_B. Positive charge (as shown in Figure 5.10.b), on the other hand, would lead to silicon bands being pushed down, and thus a larger Φ_B would result.

The effect of positive and negative charge on J_3 is modelled in Figure 5.11. A doping of 1x10^{15} cm^{-3}, and a Φ_B of 0.8 eV is used for this modelling. As one can see, the effect of charge can be quite significant (relative to the case with no charge). A

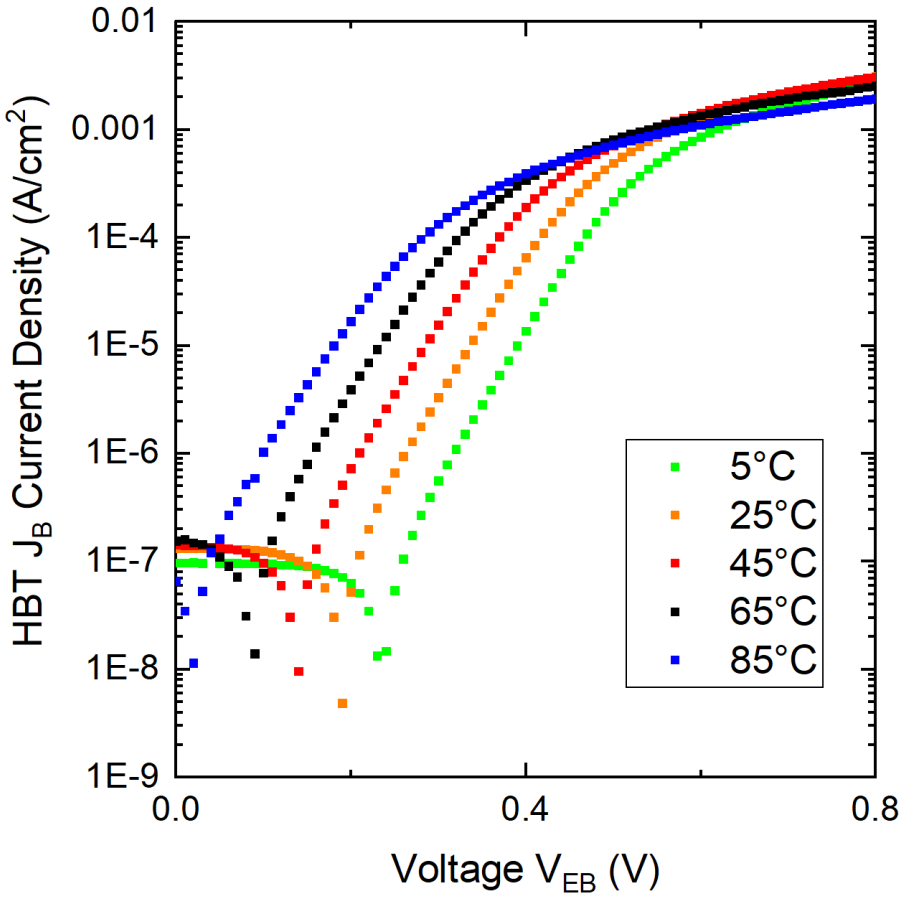


Figure 5.9: I-V-T data for 4.1 nm TiO_2/p-Si diode

charge of 1x10^{10} C/cm^2 reduces $J_{3,o}$ by a factor of 180. Further, as the plot shows, as the amount of positive charge increases, the impact increases as well.

5.4.3 TiO_2/Si Diodes versus Thickness

This is further corroborated with thickness data for TiO_2/p-Si and TiO_2/n-Si devices in Figures 5.12 and 5.13. For TiO_2/p-Si, as discussed in Chapter 4, initially as the thickness increases, the current gets reduced. Possible explanations are reduction of tunneling current, current mechanism (4) and possible increase in Schottky barrier height as the silicon gets Fermi-depinned with thicker TiO_2 layers, implying a reduced current mechanism (3). (Note the extreme variation in I-V characteristics versus

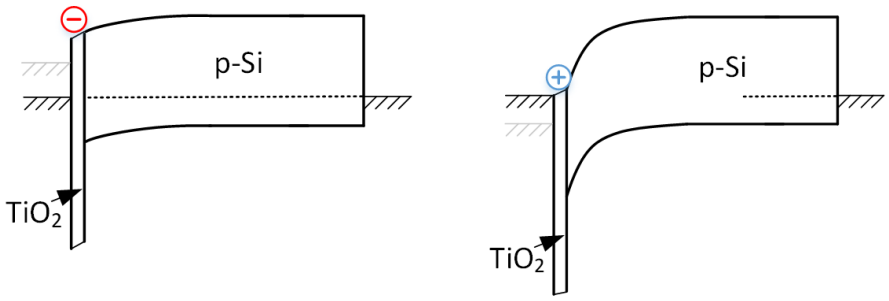


Figure 5.10: Effect of (a) negative and (b) positive charge on metal/TiO_2/Si diode and Φ_B. In gray is shown where the metal would be relative to the TiO_2 if there was no charge.

thickness around 4.1 nm). However as the I-V-T data shows, once the TiO_2 layer get thicker than 4.1 nm, the Schottky barrier for current mechanism (3) decreasing, implying a larger current mechanism (3). This matches what is seen in the TiO_2/p-Si diode data in Figures 5.12, the diodes with 4.6 and 8.6 nm TiO_2 have increasingly higher currents than the 4.1 nm TiO_2/p-Si diode.

Similarly, for TiO_2/n-Si, it shows in Figures 5.13 that 4.6 nm and 8.6 nm TiO_2/n-Si increasingly look more like a Schottky barrier device. This is to be expected if there is indeed negative charge for thicker TiO_2 layers: negative charge would push the silicon band up at the TiO_2/Si interface, leading to a barrier for electrons, the majority current carriers, thus exhibiting a Schottky barrier-like behavior.

Annealing at 250 °C too appears to create negative charge. Negative charge for 250 °C annealed TiO_2 has been shown in literature. As mentioned in Chapter 3, for TiO_2/p-Si, we see a degradation for 250 °C annealed devices, as seen in Figure 5.14. Thus it appears that both thicker TiO_2 than 4 nm and 250 °C annealing degrades device performance. The negative charge lowers the effective Schottky barrier height on p-type substrates. It is also possible that the aluminum could be penetrating the TiO_2. Further annealing with thicker TiO_2 would be useful.

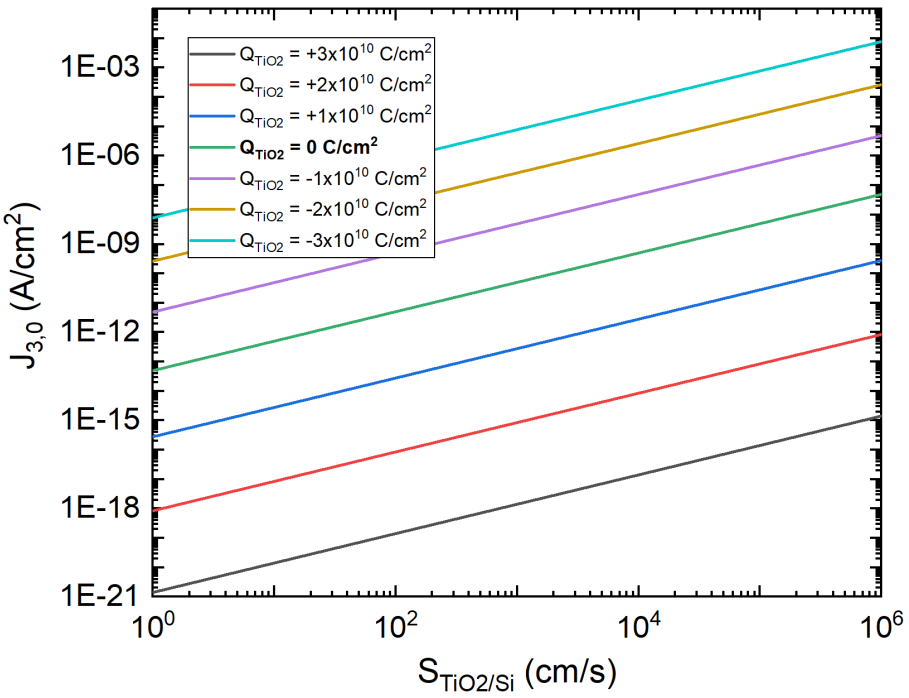


Figure 5.11: Effect of positive and negative charge of $J_{3,o}$ for different S-values. As the amount of charge increases (from negative to positive charge), the impact also increases.

5.4.4 Current Multiplication in Al/TiO_2/p-Si Diode

Finally, a peculiar phenomenon appears for optimized TiO_2/p-Si diodes (i.e. TiO_2 thickness layer of 4.1 nm). In reverse bias, as can be seen in Figure 5.12, there is a "kink" effect. This effect has been reported in MIS solar cells consisting of an Al/SiO_2/p-Si structure [68–71]. It is a phenomenon known as **current multiplication** as it multiplies the reverse bias current, more easily seen in Figure 5.15. This occurs only when there is an inversion layer, i.e. when there is already a large band-bending downwards in p-Si. This further confirms that 4.1 nm TiO_2/Si has a large band-bending at the Si interface (due to the large Schottky barrier height). In reverse bias, electrons accumulate and an inversion layer forms. The negative charge of the additional electrons increases the magnitude of the electric field at the semiconductor interface, leading to a larger field in the TiO_2 as well. A larger voltage drop across

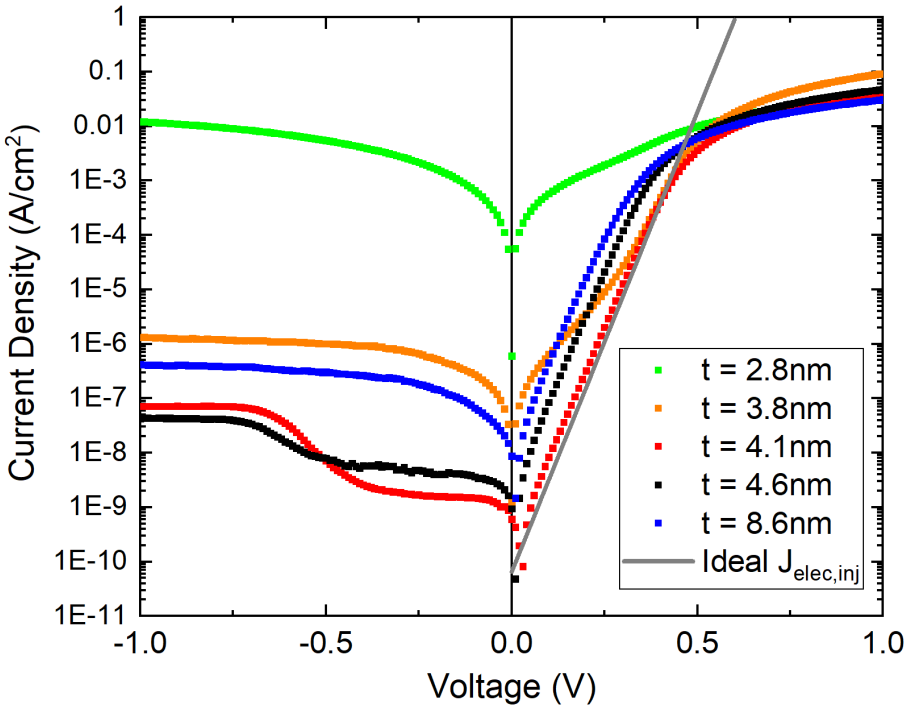


Figure 5.12: J-V data for TiO_2/p-Si diodes for different TiO_2 thicknesses

the TiO_2 layer follows, leading to a reduced applied voltage across the semiconductor depletion region. A smaller negative bias across the depletion region implies a smaller Schottky barrier height for holes, causing the current to suddenly increase (current multiplication). In order to achieve a current multiplication phenomenon and an excess formation of electrons, a conduction band offset is necessary - otherwise the excess electrons can simply recombine at the metal and no current multiplication would occur. The small conduction band offset (< 200 meV) measured through IPES in Chapter 1 appears to be large enough to enable current multiplication, yet small enough to allow for ohmic conduction for electrons (4.1 nm TiO_2 or thinner as seen in Figure 5.13)!

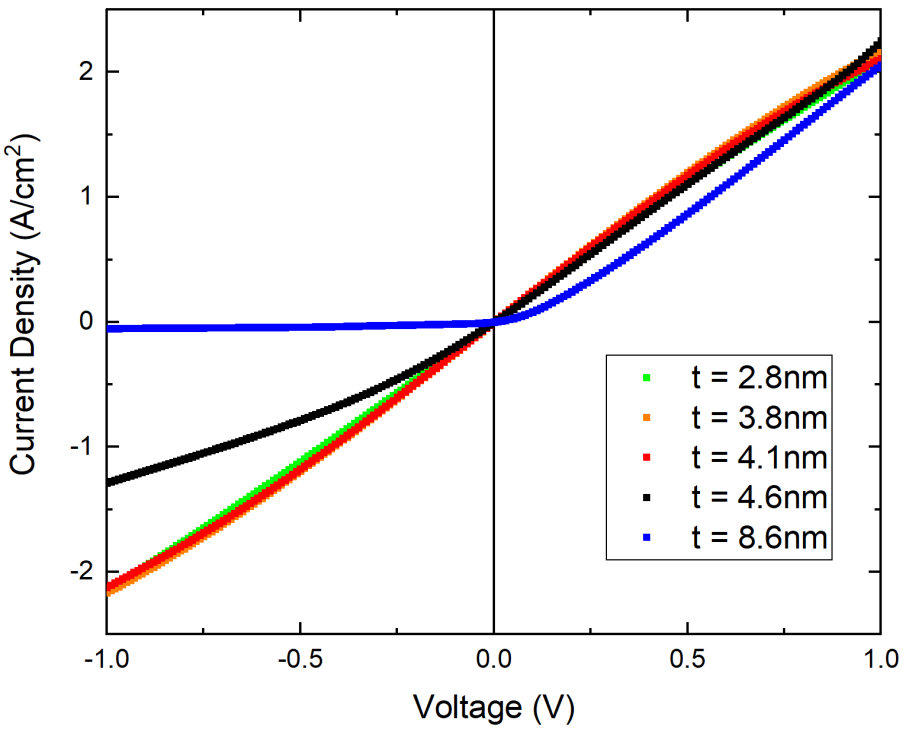


Figure 5.13: J-V data for TiO_2/n-Si diodes for different TiO_2 thicknesses

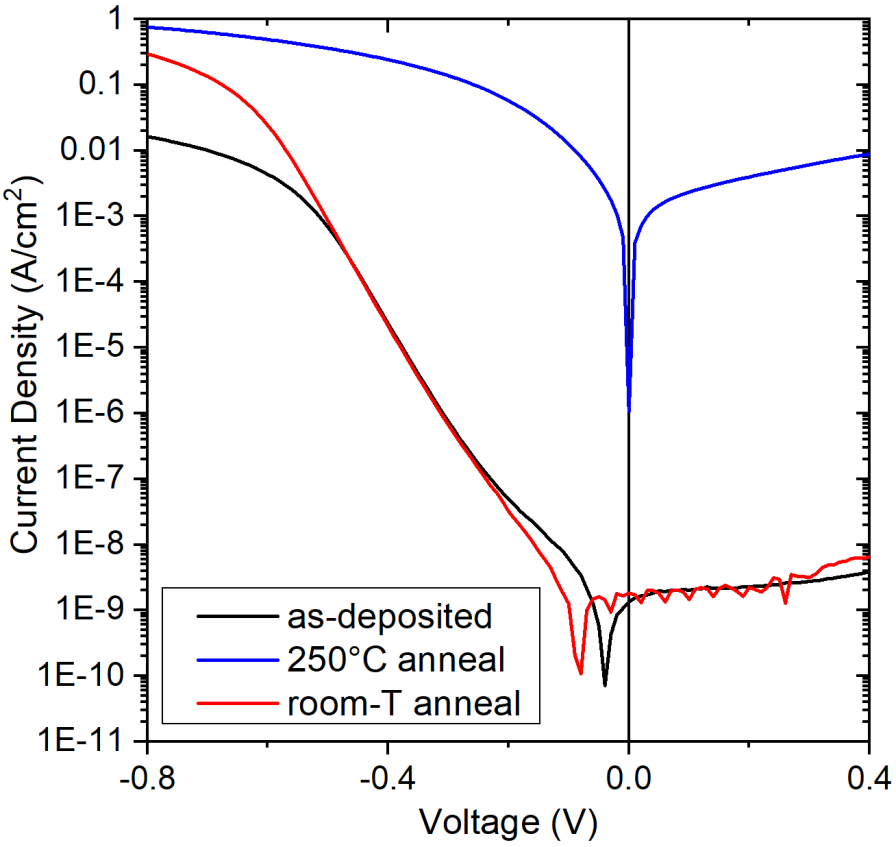
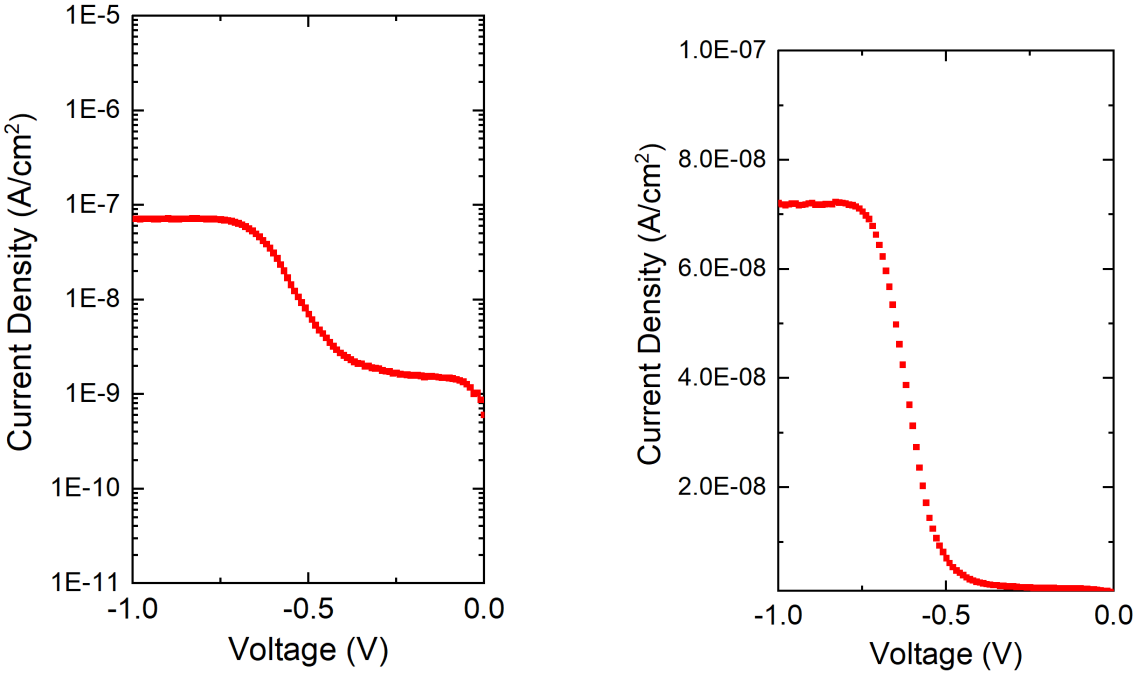


Figure 5.14: J-V data for TiO_2/p-Si diodes for as-deposited versus 250 °C annealed, showing degradation for 250 °C annealed



(a) (b)

Figure 5.15: J-V data for 4.1 nm TiO_2/p-Si diode in reverse bias, on both (a) log and (b) linear y-scale - showing current multiplication phenomenon

5.5 Impact of the Schottky Barrier Model on Hole-Blocking Mechanism

Our early work (Figures 2.21 and 2.22) interpreted the reduction of the current at an Al/TiO_2/Si junction versus an Al/Si junction as the effect of the valence band offset between TiO_2 and silicon.

The models of this chapter have conclusively demonstrated that current mechanism (3) in an Al/TiO_2/Si junction is exponentially dependent on the hole Schottky barrier height. Thus, we may propose that an increase in the Schottky barrier height is the main mechanism reducing hole current, not the valence band offset $\Delta E_V(TiO_2/Si)$.

At an ideal Al/p-Si interface, with an Al work function of 4.08 eV, one might expect a Schottky barrier height of 1.09 eV. In practice, often a very low barrier, or even an Ohmic contact results. The low barrier is thought to be due to interaction of the Al with the p-type Si, pinning the barrier height at a very low value. It has been established that a TiO_2 interlayer between the Al and the Si unpins the barrier height, possibly from preventing direct Al-Si chemical interaction. [72, 73].

This is observed in our own data, where for a TiO_2 thickness of 4 nm, a barrier height of 0.99 eV was measured by C-V (section 4.2), whereas without the TiO_2 the device did not rectify. Using the Schottky model, we earlier showed an effective barrier height of 1.01 eV from temperature dependent measurements for a TiO_2 thickness of 4.1 nm, almost perfectly matching the C-V extracted barrier height.

This supports the idea that the Schottky barrier height is a key parameter in determining the hole recombination current at the TiO_2 /Si interface, and that the main effect of the TiO_2 is unpinning of the Schottky barrier height.

5.6 Conclusion

In conclusion, in this chapter an analytical model was developed for current mechanism (3). Once $\Delta E_V(TiO_2/Si)$ is large enough (400 meV), the two key parameters are the Schottky barrier height and the recombination velocity at the TiO_2/Si interface. The Schottky barrier height is dependent on a) the metal workfunction as TiO_2 Fermi-depins the silicon surface and b) any charges in the TiO_2 - with negative charge degrading performance, and positive charge improving performance. From an experimental point of view, I-V data for TiO_2/p-Si and TiO_2/n-Si for different TiO_2 thicknesses indicate the existence of negative charge for TiO_2 layers thicker than 4.1 nm. I-V-T data performaned on HBT devices, looking specifically at current mechanism (3), further corroborate this as thicker TiO_2 layers (from 4.1 nm to 4.6 nm to 8.6 nm) lead to ever smaller Schottky barrier heights (1.01 to 0.83 to 0.78 eV). 250 °C annealed TiO_2/p-Si also indicate the presence of negative charge. As such, both thicker TiO_2 layers and TiO_2 layers annealed at higher temperature appear to cause the formation of negative charge.

An interesting phenomenon, seen in Al/SiO_2/p-Si MIS diodes, called current multiplication, was also seen in Al/TiO_2/p-Si, but only in optimized devices. Current multiplication is only seen in devices which have a large band-bending downwards, thus further proving that a large Schottky barrier height exists for optimized Al/TiO_2/p-Si diodes.

Chapter 6

Summary and Future Work

6.1 Summary

This is a summary of the key results of Chapters 2, 3, 4 and 5.

In Chapter 2, a new deposition method for amorphous titanium oxide was developed. This modified chemical vapor deposition (CVD) method uses only one precursor, titanium(IV)-tertbutoxide and the deposition itself is done through cycles consisting of an adsorption step at -10 °C and a thermolysis step at 100 °C. The precursor bulb size was the main limiting factor to growing thicker TiO_2 layers. Spectroscopy showed that indeed, stochiometric TiO_2 was deposited. The TiO_2 had a bandgap of 3.4 eV, a very small conduction band offset relative to silicon (< 200 meV), and a large valence band offset relative to silicon (2.1 eV), making it suitable as an electron-selective contact as seen by the current-voltage data for TiO_2/p-Si and TiO_2/n-Si devices.

Chapter 3 addressed the key issue of surface passivation. Annealing TiO_2/Si interfaces at 250 °C in nitrogen ambient led to high minority carrier lifetimes and low recombination velocities (down to 50 cm/s). However 250 °C annealing also led to degradation of I-V characteristics of TiO_2/p-Si. It was discovered that annealing

in nitrogent ambient, but at room temperature and for a longer time period (2 days) led to similar and even better recombination velocity values (down to 28 cm/s), with the added benefit of no I-V degradation. Furthermore, the mechanism behind these annealing techniques was investigated and the formation of an Si-O-Ti bond, similar to Si-O-Si in SiO_2, was found. Double sided PEDOT/n-Si/room-T TiO_2 devices were made, and an increase in V_{OC} of 45 mV was seen. The V_{OC} increase was correlated to a recombination velocity value of 75 cm/s, consistent with lifetime measurements done concomitantly.

Chapter 4 looked into the current mechanism across an optimized TiO_2/p-Si diode and determined that mechanism (1) - ideal minority carrier injection dominates. Mechanism (2), recombination in the depletion region, is not important at PV-relevant conditions. Current mechanism (5) is too small as the TiO_2/Si valence band offset is $>$ 2 eV. The remaining two mechanisms, (3) and (4), recombination at the TiO_2/Si interface and tunneling, are relevant. In order to predict how much dark current can be further minimized (and thus V_{OC} and η maximized), the sum of mechanisms (3) and (4) need to be known. A new measurement technique, the heterojunction bipolar transistor (HBT), was developed to determine the absolute magnitude of mechanisms (3) and (4) (hole current). For the TiO_2 thickness of 4.1 nm, it was found that the hole current is 8% of the total current. It was further established that past 4.1 nm, degradation of I-V characteristics occured, hence 4.1 nm is the optimal TiO_2 thickness.

In Chapter 5, an analytical model was developed for mechanism (3). It was shown that the two key parameters for minimizing current mechanism (3) are the Schottky barrier height for holes recombining at the TiO_2/Si interface and the recombination velocity at that interface.. The barrier height is dependent on a) the metal workfunction as TiO_2 Fermi-depins the silicon surface and b) any charges in the TiO_2 - with negative charge degrading performance, and positive charge improving performance.

The surface recombination velocity can be optimized as per the work in Chapter 3. This is assuming the TiO_2/Si valence band offset is at least 0.4 eV. Thus this new model states that the hole-blocking mechanism is due to band-bending induced by TiO_2 charge and unpinning of the Al/Si interface, as opposed to due to the TiO_2 valence band edge. From an experimental point of view, I-V data for TiO_2/p-Si and TiO_2/n-Si for different TiO_2 thicknesses indicate the existence of negative charge for TiO_2 layers thicker than 4.1 nm. I-V-T data performaned on HBT devices, looking specifically at current mechanism (3), further corroborate this as thicker TiO_2 layers (from 4.1 nm to 4.6 nm to 8.6 nm) lead to smaller and smaller Schottky barrier heights (1.01 to 0.83 to 0.78 eV). 250 °C annealed TiO_2/p-Si also indicate the presence of negative charge. As such, both thicker TiO_2 layers and TiO_2 layers annealed at higher temperature appear to cause the formation of negative charge.

Finally, this thesis concludes with this chapter, which will now discuss a few avenues for future work to successfully incorporate TiO_2/Si heterojunctions in high-efficiency solar cells.

6.2 Future Work

Future work can be split into two broad categories: 1) further engineering of TiO_2/Si heterojunction and 2) incorporation of TiO_2/Si heterojunction into solar cells

6.2.1 Further Engineering of TiO_2/Si Heterojunction

1. **Further chemical passivation of TiO_2/Si interface**: Si-O-Ti bonds appear to be important for the chemical passivation of the TiO_2/Si interface as shown in Chapter 3. As Chapter 5 demonstrated, further reduction of S_{eff} would be beneficially to reducing dark current. One possible avenue for further chemical passivation could be the formation of Si-H bonds at the remaining

dangling bonds. One could, for example, apply a low-temperature H_2-plasma to the TiO_2/Si interface [74], similar to how 400 °C forming gas anneal is used to form Si-H bonds after the formation of SiO_2 and its resultant Si-O-Si bonds [75,76]. This process may even altogether replace the 250 °C/room-T anneal used to form Si-O-Ti bonds, depending on how effective Si-H passivation is. Literature shows HF-passivated silicon (Si-H bonds) can achieve an S_{eff}-value of 0.25 cm/s [77]. The HBT method will be critical in measuring if any further passivation techniques results in a reduction in current mechanism (3).

2. **Development of positive charge in Al/TiO_2/Si stack**: As mentioned in chapter 5, negative charge increases current mechanism (3), while positive charge reduces current mechanism (3). Thus one approach to improved performance could be the introduction of positive charge. This may already be in existence as TiO_2/SiO_2/Si stacks have shown to improve performance relative to TiO_2/Si stacks [59, 78]. A V_{OC} of 676 mV for TiO_2/SiO_2/Si (compared to 638mV for TiO_2/Si) was achieved.The underlying mechanism may be the interfacial positive charge commonly found in SiO_2/Si [79–81]. The SiO_2 used in these stacks is a **tunnel oxide** - a thin enough oxide to allow carriers to tunnel [82]. However it is also possible that a SiO_2/TiO_2/silicon stack may yield even better results as the TiO_2 can be used for chemical passivation, while the SiO_2 layer could provide a field passivation effect due to positive charge. Other materials which exhibit positive charge, such as SiNx [83, 84], are also worthy candidates for investigation, especially if deposition conditions can be achieved at low cost.

3. **Surface Texturing**: The work described in this thesis used planar silicon surfaces. Yet, for optimal light absorption, textured surfaces are preferred [85]. Initial lifetime measurements for annealed TiO_2/textured silicon showed poor

lifetime values, similar to "as-deposited" TiO_2 and very high S_{eff}-values. Further work is needed to obtain high-quality passivation of TiO_2/textured silicon. The previous two points (further chemical passivation and positive charge) may suffice. Though further investigation is necessary.

4. **Development of transparent contact**: Aluminum, due to its low workfunction, provides for a large band-bending in the silicon. Unfortunately, as a metal, it absorbs light and thus cannot be used as the top contact for silicon SCs. A transparent contact, in a similar form as ITO [86], will have to be found. Furthermore, this transparent contact will need a low workfunction, and not react adversely with the TiO_2 layer. Examples of adverse effects are the formation of negative charge at the transparent contact/TiO_2 interface and the formation of a new material at the transparent contact/TiO_2 - with the new material having adverse conduction band or valence band offsets (for example - a large $\Delta E_C(TiO_2/Si)$).

6.2.2 Incorporation of TiO_2/Si Heterojunction into SCs

1. **TiO_2/p-Si/hole-selective contact SC**: Assuming a transparent contact is developed, surface passivation is optimized (on planar or textured silicon), the next step will be to develop a double heterojunction device consisting of TiO_2 (electron-selective contact)/p-Si/hole-selective contact, as seen in Figure 6.1. Many hole-selective contact materials already exist, including PEDOT (utilized in this thesis) [87], molybdenum oxide (MoO_x) [88, 89] and nickel oxide (NiO_x) [90, 91]. It remains to be seen which material will be best suited as a backside hole-selective contact.

2. **TiO_2 in IBC SC**: In Chapter 1, two high-efficiency silicon SC structures were discussed, namely the PERL and the HIT structure. Another high-efficiency

structure in the interdigitated back contact (IBC) solar cell [92], as shown in Figure 6.2. In an IBC solar cell, both electron- and hole-selective contacts are on the backside (hence the name). The top surface is typically textured and passivated, the metal contacts themselves are small and localized (reminiscent of the PERL device structure). In recent years, the IBC and HIT structures have been combined to obtain a world-record $> 26\%$ power conversion efficiency for monocrystalling silicon solar cells [93,94]. TiO_2, due to its potential low cost fabrication process, could be well situated to be incorporated into an IBC solar cell. The **selective deposition** and contact resistance of TiO_2 however must be further investigated and developed.

3. **TiO_2 as interlayer between silicon and perovskite**: TiO_2 can also be utilized as an interlayer between silicon and other solar cell materials, for example perovskites. Preliminary work in this field is promising [95], though with the developments in this thesis, one could further improve silicon/TiO_2/perovskite SCs and also use TiO_2 as an interlayer for other solar cell architectures.

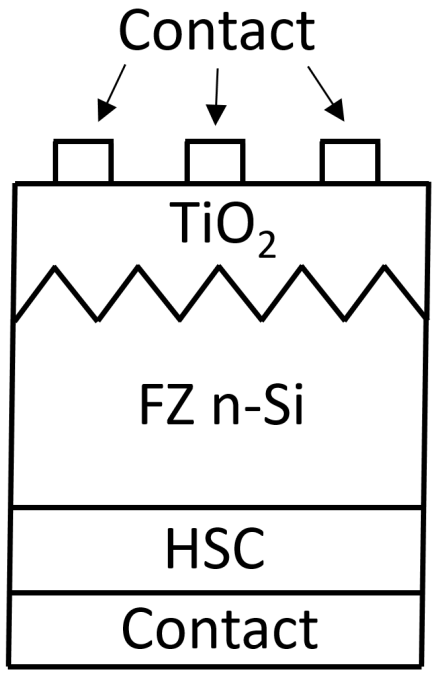


Figure 6.1: Device structure for TiO_2/p-Si/hole-selective contact (HSC) double-heterojunction device.

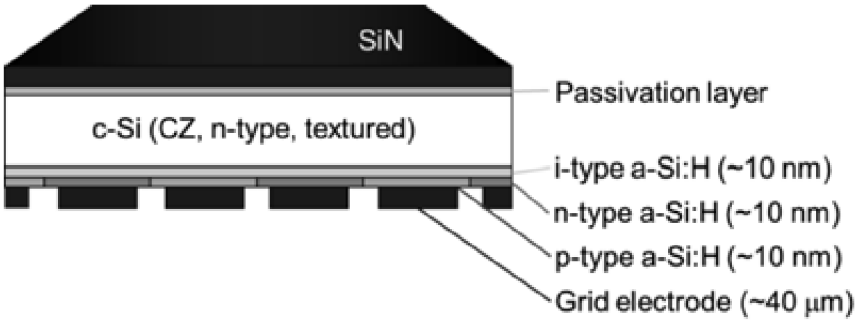


Figure 6.2: HIT-IBC cell structure. © 2014 IEEE. Reprinted, with permission, from [93].

Appendix A

Notes on HBT Fabrication

A.1 Masks

Figure A.1 shows the layout of the heterojunction bipolar transistor (HBT) device used in this work. The size of each device is 4 mm x 4 mm, and consists of 4 emitter contacts (the 4 red contacts in the middle) and 2 base contacts (top and bottom blue contacts).

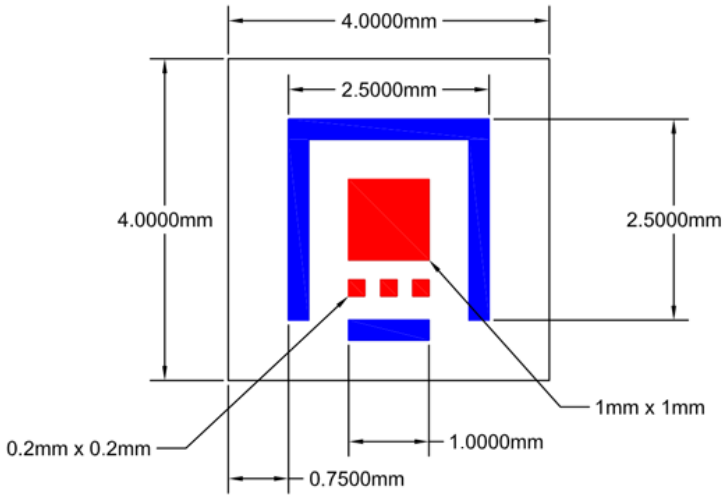


Figure A.1: HBT device layout

Data were collected in this work utilizing the top base contact and the large emitter contact. The other contacts were used as sanity checks: a) base-to-base I-V measurements were performed to ensure ohmic contacts, b) the smaller emitter contacts were tested for area dependency by comparing J_B and J_C for the smaller and larger emitter contacts.

Figures A.2 and A.3 show the shadow masks used to deposit metal utilizing a thermal evaporator (Edwards Auto 306) respectively for emitter and base contacts. The samples used in this work were 16 mm x 16 mm, thus each sample consisted of 16 devices.

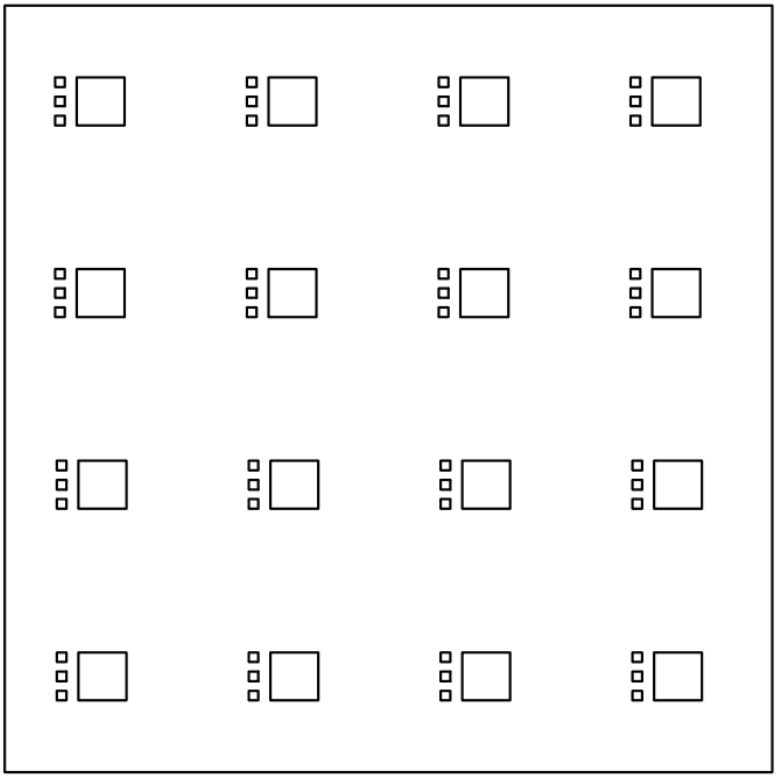


Figure A.2: Emitter contact shadow mask

And finally, Figure A.4 shows the mask used to physically separate the devices on a sample. Each device was etched (10-14 microns in depth) for 0.25 mm in width

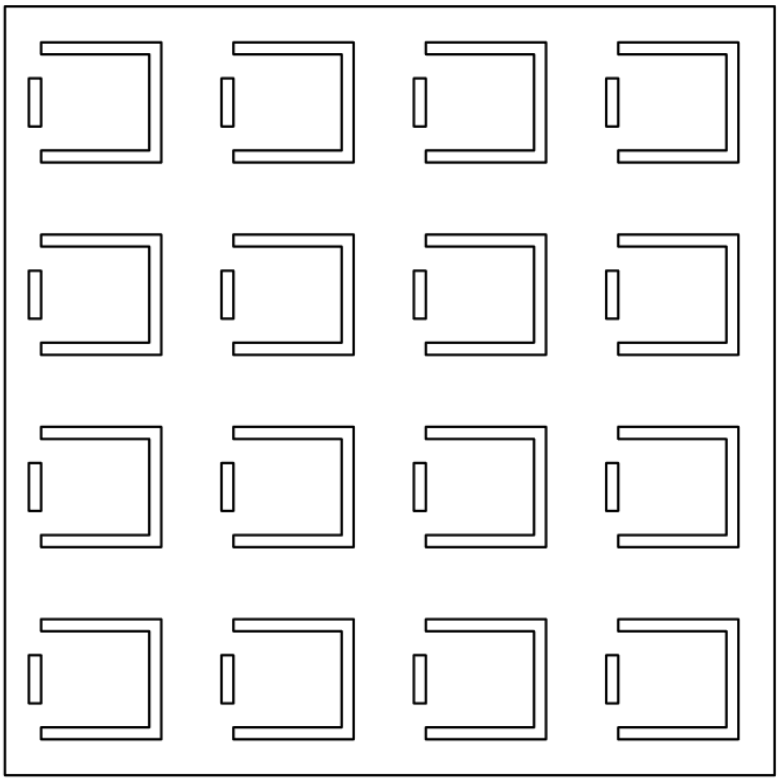


Figure A.3: Base contact shadow mask

across its perimeter. This etching ensures the base region is defined for the device, and not the entire sample.

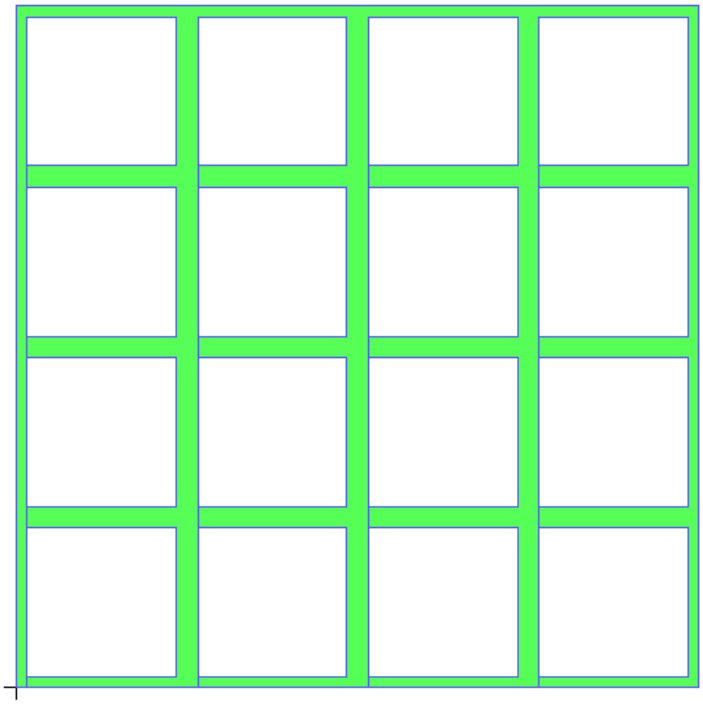


Figure A.4: Mask for etching and separating Base region

A.2 Fabrication Process

1. Prepare Sample

   (a) Dice silicon wafer into 16 mm x 16 mm square pieces

   (b) Spincoat AZ5214 photoresist

   (c) Use base region etch mask in Figure A.4 in Karl Suss MJB4

   (d) Expose for 10 seconds

   (e) Develop pattern in AZ 300 MIF

   (f) Rinse in DI water

   (g) Place dummy wafer on hotplate at 121 °C

   (h) Use Crystalbond 509 (melting temperature of 121 °C) to stick samples onto dummy wafer

(i) Load samples in RIE800iPB

(j) Etch using Bosch recipe, modified to only do silane step - for 2 min 40 s

(k) Unload samples

(l) Check etch depth - typically 10-14 μm

(m) Remove sample from dummy wafer on hotplate at 121 °C

(n) Rinse off photoresist using acetone

2. Deposit Base Contact

(a) Solvent clean:

(b) 5 min acetone

(c) 5 min methanol

(d) 5 min IPA

(e) End of solvent clean

(f) 5 second dip in 10:1 BOE

(g) RCA clean:

(h) RCA1: 5:1:1 H_20:H_20_2:NH_4OH

(i) 1 min dip in 20:1 H_20:HF

(j) RCA2: 5:1:1 H_20:H_20_2:HCl

(k) End of RCA clean

(l) 1 min dip in 20:1 H_20:HF

(m) Place samples with top surface covered by B mask (Figure A.3) in Edwards evaporator

(n) Deposit 20 nm Al

(o) Deposit 150 nm Cr (Cr is resistant to HF etch)

(p) Unload samples

3. Deposit TiO_2

   (a) 10 second dip in 100:1 H_20:HF (to clean exposed surface)

   (b) Put samples in TiO_2 deposition chamber

   (c) Pump down

   (d) Lower temperature to -10 °C

   (e) 10 min adsorption step

   (f) Ramp up temperature to 100 °C

   (g) 10 min thermolysis step

   (h) Repeat TiO_2 deposition cycle as often as required

   (i) Ramp down to 25 °C

   (j) Unload samples

4. Deposit Emitter Contact

   (a) Place samples with top surface aligned and covered by E mask (Figure A.2) in Edwards Evaporator

   (b) Deposit 20 nm Al - **note: Pressure must be less than 1x10^{-6} mb for high-quality Al/TiO_2 contact**

   (c) Deposit 150 nm Ag

   (d) Unload samples

5. Deposit Collector Contact

   (a) Scratch back surface for diamond-tip scribe - for proper contact between metal and Si, as TiO_2 is also coated on back surface

(b) Place samples with bottom surface (no shadow mask) in Edwards Evaporator

(c) Deposit 150 nm Ag

(d) Unload samples

Appendix B

HBT Base Recombination

Figure B.1 shows the banddiagram of a TiO_2/Si heterojunction bipolar transistor (HBT). Besides I_C, the diagram also shows the three relevant components of I_B - current mechanism 3 (recombination at the TiO_2/Si interface), current mechanism 4 (tunneling through the TiO_2) and $I_{B,recomb}$ (holes recombining with injected electrons in the base).

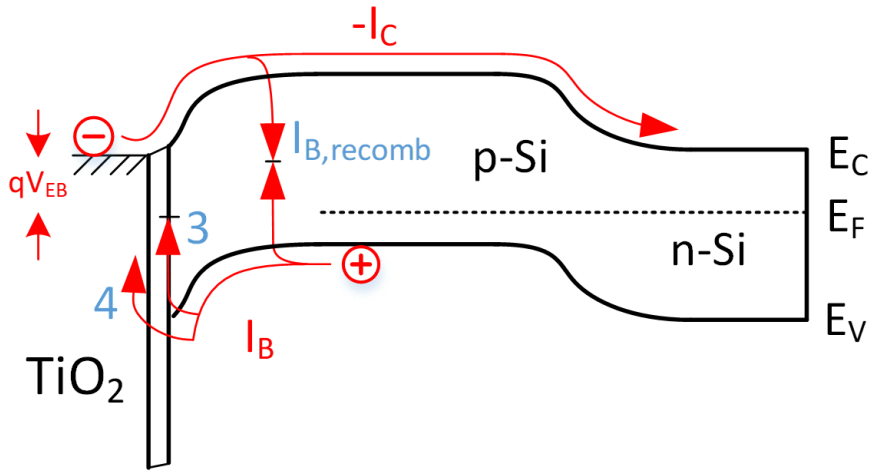


Figure B.1: HBT showing I_C and the three components of I_B - current mechanisms 4,5 and $I_{B,recomb}$

We examine the effect of $I_{B,recomb}$ on the dependence of I_C in bipolar transistors on V_{CE} due to base-width modulation in the common-emitter configuration (the Early effect). This effect is typically ignored.

B.1 Collector and Base Currents

Beginning with the classical equations, where W_B is the neutral base width, we obtain for I_C:

$$I_C = \frac{qn_i^2 D_n}{W_B N_A} e^{\frac{qV_{BE}}{kT}} \tag{B.1}$$

For I_B we obtain:

$$I_B = I_{B3,4} + I_{B,recomb} = \left[I_{B3,4,o} + \frac{qn_i^2 W_B}{2N_A \tau} \right] e^{\frac{qV_{BE}}{kT}} \tag{B.2}$$

$I_{B3,4}$ represents holes injected from base to emitter (Processes 3 and 4 in Figure 4.14), with its pre-exponential constant $I_{B3,4,o}$. τ is the electron lifetime in the base, and the other terms have their usual meanings.

If we take the derivative of I_C relative to V_{CE}, we find that the dependence of I_C on V_{CE} comes from possible changes in W_B and in V_{BE}:

$$\frac{dI_C}{dV_{CE}} = I_C \left[\frac{-1}{W_B} \frac{dW_B}{dV_{CE}} + \frac{q}{kT} \frac{dV_{BE}}{dV_{CE}} \right] \tag{B.3}$$

We now look at two different conditions, namely (a) when V_{BE} is held constant and (b) when I_B is held constant.

B.2 Fixed V_{BE}

If V_{BE} is held constant, then the Early effect is described by

$$\frac{dI_C}{dV_{CE}}|_{fixed\ V_{BE}} = -\frac{I_C}{W_B}\frac{dW_B}{dV_{CE}} \tag{B.4}$$

B.3 Fixed I_B

If I_B is held constant, the Early effect depends on whether the source of the base current depends on W_B. W_B itself depends on V_{CE}. Lets differentiate (B.2) and set the left side $dI_B = 0$ for a fixed I_B condition.

$$dI_B = 0 = \frac{dI_{B3,4}}{dW_B}\left[\frac{dI_{B2,3}}{dW_B} + \frac{dI_{B,recomb}}{dW_B}\right]dW_B + \frac{dI_B}{dV_{BE}}dV_{BE} \tag{B.5}$$

leading to

$$0 = \left[\frac{dI_{B3,4}}{dW_B} + \frac{I_{B,recomb}}{W_B}\right]dW_B + \frac{q}{kT}I_B dV_{BE} \tag{B.6}$$

Note in (B.5) I_B is the total base current. The holes injected to the emitter or recombining at the base-emitter interface (processes (3) and (4)) have no physical dependence on neutral base width, so we can set $dI_{B3,4}/dW_B = 0$. Then

$$\frac{dV_{BE}}{dW_B} = -\frac{I_{B,\ recomb}}{I_B}\ \frac{kT}{q\ W_B} \tag{B.7}$$

Physically, this means that under a fixed I_B condition, when base recombination dominates the base current, if W_B is decreased, V_{BE} must increase to keep the amount of electron charge in the base constant. Using (6) to substitute for the dependence of V_{BE} on V_{CE} in (3) gives for the fixed base condition:

$$\frac{dI_C}{dV_{CE}}|_{fixed\ I_B} = -I_C\left[\frac{1}{W_B}\frac{dW_B}{dV_{CE}} + \frac{q}{kT}\ \frac{I_{B,\ recomb}}{I_B}\ \frac{kT}{q\ W_B}\frac{dW_B}{dV_{CE}}\right] \tag{B.8}$$

leading to

$$\frac{dI_C}{dV_{CE}}|_{fixed\ I_B} = -\frac{I_C}{W_B}\left[1 + \frac{I_{B,\ recomb}}{I_B}\right]\frac{dW_B}{dV_{CE}} \tag{B.9}$$

B.4 Extracting $\mathbf{I}_{B,recomb}$

So we then know the ratio of the slopes of I_C vs V_{CE} for fixed I_B vs. fixed V_{BE} conditions. It depends on the fraction of the base current is due to recombination in the base, with the ratio of slopes varying between 1 and 2.

$$\left\{\frac{\frac{dI_C}{dV_{CE}}|_{fixed\ I_B}}{\frac{dI_C}{dV_{CE}}|_{fixed\ V_{BE}}}\right\} = 1 + \frac{I_{B,\ recomb}}{I_B} \tag{B.10}$$

Thus, experimentally the ratio of base recombination to total base current can be found through:

$$\frac{I_{B,\ recomb}}{I_B} = \left\{\frac{\frac{dI_C}{dV_{CE}}|_{fixed\ I_B}}{\frac{dI_C}{dV_{CE}}|_{fixed\ V_{BE}}}\right\} - 1 \tag{B.11}$$

Appendix C

Publications and Presentations

C.1 Journal Publications

1. **Janam Jhaveri** and Sturm, James C. Sturm. "Model of TiO_2/Si Selective Contact as Schottky Contact with Finite Interface Recombination Velocity" (in preparation)

2. **Janam Jhaveri**, Alexander H. Berg, and James C. Sturm. "Isolation of Hole vs. Electron Current at p-Si/TiO_2 Selective Contact using an Heterojunction Bipolar Transistor Structure." IEEE Journal of Photovoltaics 8, no. 3 (2018): 726-732.

3. Girija Sahasrabudhe, Sara M. Rupich, **Janam Jhaveri**, Alexander H. Berg, Ken A. Nagamatsu, Gabriel Man, Yves J. Chabal, Antoine Kahn, Sigurd Wagner, James C. Sturm and Jeffrey Schwartz. "Low-temperature synthesis of a TiO_2/Si heterojunction." Journal of the American Chemical Society 137, no. 47 (2015): 14842-14845.

4. Ken A. Nagamatsu, Sushobhan Avasthi, Girija Sahasrabudhe, Gabriel Man, **Janam Jhaveri**, Alexander H. Berg, Jeffrey Schwartz, Antoine Kahn, Sigurd

Wagner, and James C. Sturm. "Titanium dioxide/silicon hole-blocking selective contact to enable double-heterojunction crystalline silicon-based solar cell." Applied Physics Letters 106, no. 12 (2015): 123906.

5. Ken A. Nagamatsu, Sushobhan Avasthi, **Janam Jhaveri**, and James C. Sturm. "A 12% efficient silicon/PEDOT: PSS heterojunction solar cell fabricated at $<$ 100°C." IEEE Journal of Photovoltaics 4, no. 1 (2014): 260-264.

6. James C. Sturm, Sushobhan Avasthi, Ken Nagamatsu, **Janam Jhaveri**, William E. McClain, Gabriel Man, Antoine Kahn, Jeffrey Schwartz, and Sigurd Wagner. "Wide Bandgap Heterojunctions on Crystalline Silicon." ECS Transactions 58, no. 9 (2013): 97-105.

C.2 Conference Proceedings

1. **Janam Jhaveri**, Alexander H. Berg, Sigurd Wagner, and James C. Sturm. "Measurement of TiO_2/p-Si Selective Contact Performance using a Heterojunction Bipolar Transistor with a Selective Contact Emitter." In Photovoltaic Specialists Conference (PVSC), 2017 IEEE 44th. IEEE, 2017.

2. **Janam Jhaveri**, Alexander H. Berg, Sigurd Wagner, and James C. Sturm. "Al/TiO_2/p-Si heterojunction as an ideal minority carrier electron injector for silicon photovoltaics." In Photovoltaic Specialists Conference (PVSC), 2016 IEEE 43rd, pp. 2444-2447. IEEE, 2016.

3. **Janam Jhaveri**, Ken A. Nagamatsu, Alexander H. Berg, Gabriel Man, Girija Sahasrabudhe, Sigurd Wagner, Jeffrey Schwartz, Antoine Kahn, and James C. Sturm. "Double-heterojunction crystalline silicon solar cell with electron-selective TiO_2 cathode contact fabricated at 100°C with open-circuit voltage of

640 mV." In Photovoltaic Specialist Conference (PVSC), 2015 IEEE 42nd, pp. 1-4. IEEE, 2015.

4. **Janam Jhaveri**, Sushobhan Avasthi, Ken Nagamatsu, and James C. Sturm. "Stable low-recombination n-Si/TiO_2 hole-blocking interface and its effect on silicon heterojunction photovoltaics." In Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th, pp. 1525-1528. IEEE, 2014.

5. Sushobhan Avasthi, Ken A. Nagamatsu, **Janam Jhaveri**, William E. McClain, Gabriel Man, Antoine Kahn, Jeffrey Schwartz, Sigurd Wagner, and James C. Sturm. "Double-heterojunction crystalline silicon solar cell fabricated at 250°C with 12.9% efficiency." In Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th, pp. 0949-0952. IEEE, 2014.

6. **Janam Jhaveri**, Sushobhan Avasthi, Ken A. Nagamatsu, and James C. Sturm. "Wide bandgap HBT on crystalline silicon using electron-blocking PEDOT: PSS emitter." In Device Research Conference (DRC), 2013 71st Annual, pp. 77-78. IEEE, 2013.

7. **Janam Jhaveri**, Sushobhan Avasthi, Gabriel Man, William E. McClain, Ken Nagamatsu, Antoine Kahn, Jeffrey Schwartz, and James C. Sturm. "Hole-blocking crystalline-silicon/titanium-oxide heterojunction with very low interface recombination velocity." In Photovoltaic Specialists Conference (PVSC), 2013 IEEE 39th, pp. 3292-3296. IEEE, 2013.

C.3 Conference Presentations

1. **Janam Jhaveri**, Girija Sahasrabudhe, Gabriel Man, Ken A. Nagamatsu, Sigurd Wagner, Antoine Kahn, Jeffrey Schwartz, and James C. Sturm. "Structure of Low-Temperature TiO_2/Si Interface and Impact on Surface Recombination

for Low-Cost Si-based PV." Presented at the 45th IEEE Semiconductor Interface Specialists Conference (SISC), San Diego, CA, 2015.

2. **Janam Jhaveri**, Sushobhan Avasthi, Gabriel Man, Ken A. Nagamatsu, William E. McClain, Jeffrey Schwartz, Antoine Kahn, and James C. Sturm. "Effect of Annealing on Stability of Low Interface Recombination Velocity at TiO2/p-Silicon Interface." Presented at the MRS Spring 2014 Meeting, San Francisco, CA.

3. Sushobhan Avasthi, William McClain, Yasmin Afsar, Gabriel Man, **Janam Jhaveri**, Ken A. Nagamatsu, Antoine Kahn, Jeffrey Schwartz, Sigurd Wagner, and James C. Sturm. "Hole-Blocking Metal-Oxide/Crystalline-Silicon Heterojunctions with Recombination Velocity of <100 cm/s." Presented at the MRS Spring 2014 Meeting, San Francisco, CA.

4. Sushobhan Avasthi, William McClain, Gabriel Man, **Janam Jhaveri**, Ken A. Nagamatsu, Antoine Kahn, Jeffrey Schwartz, and James C. Sturm. "Growth Mechanism and Carrier Transport in Hole-Blocking TiO2/Silicon Heterojunctions. Presented at the MRS Spring 2014 Meeting, San Francisco, CA.

5. Gabriel Man, Sushobhan Avasthi, **Janam Jhaveri**, William E. McClain, Jeffrey Schwartz, James C. Sturm, and Antoine Kahn. "Chemical Composition and Electronic Structure of Titanium Dioxide / Silicon Heterojunctions." Presented at the MRS Fall 2013 Meeting, Boston, MA.

C.4 Other Work

1. Cleo B. Chou, **Janam Jhaveri**, Jane W. Baldwin, Phillip M. Hannam, Kyle Keller, Wei Peng, Sam Rabin, Arvind P. Ravikumar, Annette M. Trierweiler,

Xingchen T. Wang and Robert Socolow. "Fusion Energy." Princeton University Andlinger Center Distillate.

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