System Building, Two Ways: Development and Application of ZnO TFT Technology in Large-Area Hybrid Sensing Systems

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Abstract

In this thesis, we provide a material-based approach to mitigating a perennial problem in large-scale hybrid sensing systems.

While the purpose of these sensing systems is varied, the foundational belief of this work is that signals from the physical world have inherent value, and so long as the infrastructure for capturing this data can be built efficiently and scalably, new applications will flow freely. This work focuses on enabling the construction of robust sensing system infrastructures from the bottom up, starting with development of a deposition system for growth of thin-film metal oxides, moving next to material, device, and thin-film circuit development and characterization, and concluding with a new system architecture for highly-scalable large-scale sensing systems and system demonstration, using zinc-oxide thin-film transistor circuits.

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To my many teachers.

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Chapter 1

Introduction

Large area electronics (LAE) is a field predominantly divided into two subcategories, bridged by their mutual dependence on electronics devices (transistors, diodes, sensors) that can be fabricated on large, meter-scale substrates at low temperatures ($< 350°C$). The first subcategory, flat panel displays, is of enduring commercial value, and marches onwards to thinner, more luminous/sensitive/energy-efficient products via material, device, and circuit improvements. The second subcategory, although amorphous, is best described as "sensing systems," and with the exception of commercial X-ray imagers, resides purely in a number of academic laboratories scattered across the world [45]. While displays and sensing systems share a common technological toolset, their aims for now remain distinct – in this work we focus solely on the latter.

1.1 Objective: LAE Sensing Systems

Our goal is to create LAE sensing systems that harvest information from our surrounding environment by distributing sensors and access circuits across large, flexible substrates that can physically conform to the source of the signals of interest. Maximum processing temperatures are ultimately restricted by the glass transition temperatures of flexible sub-

strates, described in Table 1.1 [46–49], and more conservatively restricted by the softening temperatures, which fall even lower.

Table 1.1: Temperature ranges set by various LAE substrate materials

Substrate Material	**Temperature Limitation**
PET (polyethylene terephthalate)	70 – 100°C (T_g)
PEN (polyethylene naphthalate)	120°C (T_g)
PI (polyimide)	360°C (T_g)
Chemically-strengthened glass (< 500 μm)	550°C (annealing point)
Borosilicate glass	560°C (annealing point)

In particular, the desire to enable low-cost, extremely thin (< 50 μm), durable polymer substrates restricts practical maximum process temperatures in LAE to < 350°C. This reduced thermal budget conveniently makes integration of a variety of (often polymer-based) sensors possible [11–13, 50, 51] – some examples can be found in Figure 1.1.

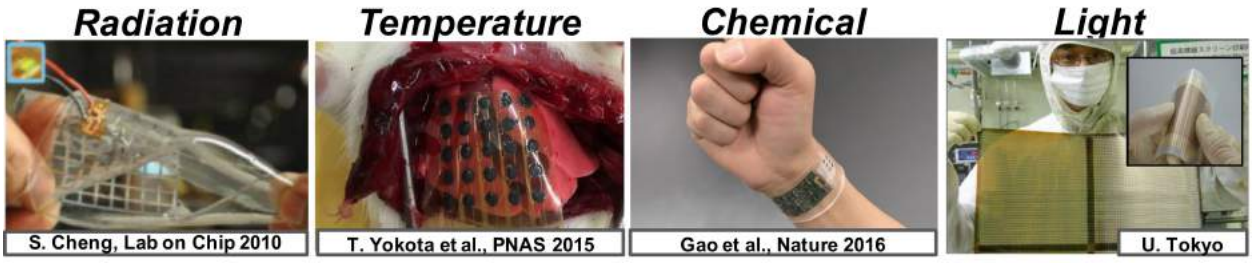


Figure 1.1: A wide range of LAE sensors is available; here, from left to right: radiation sensors, temperature sensors, chemical sensors, and photodetectors [11–13]. Fourth image unpublished, courtesy of Prof. Takao Someya.

Of course, there is a critical drawback to this temperature restriction. In order to accomplish our goal of full sensing systems, we need a way to incorporate not only sensors and substrates, but also additional functionality, such as instrumentation, computation, and power management. Thin-film transistors (TFTs) (and thin-film diodes) could provide this functionality in LAE, as recent work demonstrating various TFT circuit blocks has shown [51–56].

However, LAE requires semiconductors that can be deposited on materials such as borosilicate glass and polyimide that cannot withstand high temperatures. Low temperature deposition results in semiconductors with a high degree of disorder, regardless of deposition method, which bestows material properties on the thin-film semiconductor that can be far worse than those of the single-crystal semiconductor. Accordingly, the performance and energy efficiency of TFTs is typically orders-of-magnitude lower than those of silicon CMOS transistors, as shown in Table 1.2. For example, silicon-CMOS transistor f_T values fall between 200-300 GHz, while those of LAE TFTs are typically 1-10 MHz [44, 57].

Table 1.2: Thin-film transistors in LAE have parameters far worse than crystalline silicon CMOS counterparts.

	TFT (LAE)	**c-Si CMOS**
Mobility μ (cm^2/Vs)	0.1 – 100	300+
Supply Voltage (V)	5 – 20	1
Channel Length (μm)	1 – 5	< 0.1
Cutoff Frequency f_T (MHz)	0.1 – 100	200,000 – 300,000

To enable complete systems, hybrid systems have emerged [14–16, 58] in which LAE is combined with silicon-CMOS ICs in architectures that selectively delegate functionality between both technology domains. In many system functions, namely sensing, self-powering, communication, and computation, LAE serves to complement CMOS, and this partitioning arises naturally. In sensing, LAE offers diverse transducers and substrates for sensing a wide range of signals over large areas, while CMOS offers precision instrumentation for amplifying those signals. For self-powering, LAE offers physically large energy harvesters capable of collecting significant ambient waste energy, while CMOS offers dynamic control, DC/DC conversion, and regulation needed to use harvested energy resources within the sensing system. For communication, LAE provides physically large antennae and long, low loss metal interconnects, while CMOS offers wired/wireless transceivers for on/off-sheet communication. Computation, an energy- and performance-critical function, remains an area

best implemented in CMOS: as stated, active devices compatible with the LAE temperature range have $f_T s$ orders of magnitude lower than high-temperature technologies (e.g. mobilities/capacitances orders of magnitude lower/higher), which result in higher supply voltages and consumed power in LAE. For these reasons, computation is best delegated to silicon CMOS alone, while sensing, power management, and computation can efficiently split tasks between CMOS and LAE. A summary of LAE/CMOS system function division can be seen in Table 1.3.

Table 1.3: Aside from computation, LAE and CMOS can serve complementary roles in several system-level functions.

	CMOS	**LAE**
Computation	Dense, high performance, energy efficient devices	Slow, large, energy-intensive devices
Power	Efficient power management circuits	Physically-large energy harvesters and thin-film batteries
Communication	Control, regulation, DC/DC conversion	Low-loss interconnects and large, high Q antennae
Sensing	Precision instrumentation, limited direct sensing	Diverse transducers and conformal, large substrates

Several prototype systems have been constructed within this framework [14–16,58]; block diagrams and photos of these systems can be seen in Figures 1.2, 1.3, and 1.4.

1.1.1 Giving Hybrid Systems a Materials Advantage

In these prior systems, the semiconductor technology chosen for LAE-compatible TFTs was amorphous silicon (α-Si). While amorphous silicon TFTs have many strengths – they are robust, reproducible, extensively studied, mass-produced in the display industry, and compatible with large-area glass and polyimide – they exhibit a very modest field-effect

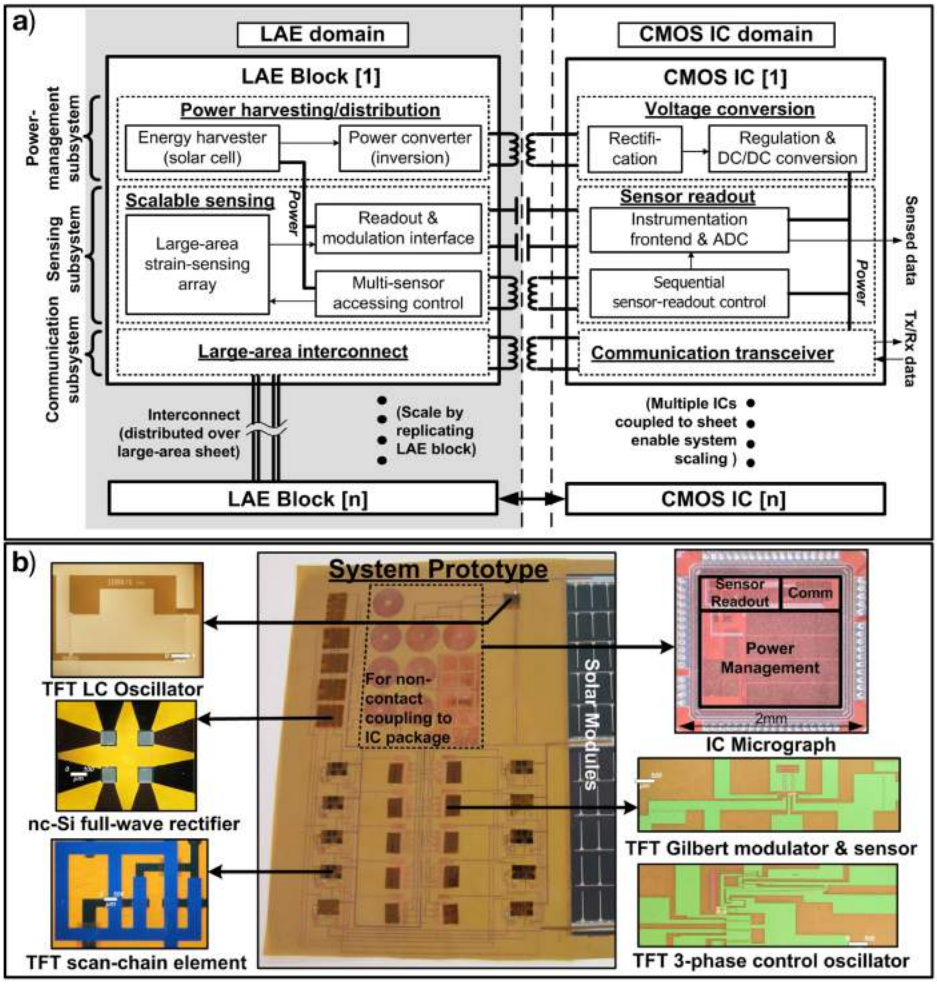


Figure 1.2: Hybrid system for structural health monitoring uses LAE for high density, large-area strain sensing, but also for efficient power harvesting and sensor accessing: a) system block diagram; b) system photo and components [14].

mobility of ~ 0.5 cm^2/Vs. This limited mobility can reduce the performance of LAE circuit blocks within the hybrid architecture, which can in turn limit system-level performance and restrict future applications. In our α-Si hybrid system work, there are several examples of circumstances where an improvement in LAE materials could result in system level advances:

1. In a strain sensing system for structural health monitoring [14], strain sensors are accessed by TFT switches that are addressed one-by-one with an α-Si scanning circuit. The scan circuit engages a TFT switch connected to the strain sensor. In order to meet a certain current requirement, the low-mobility α-Si TFT switches must be made

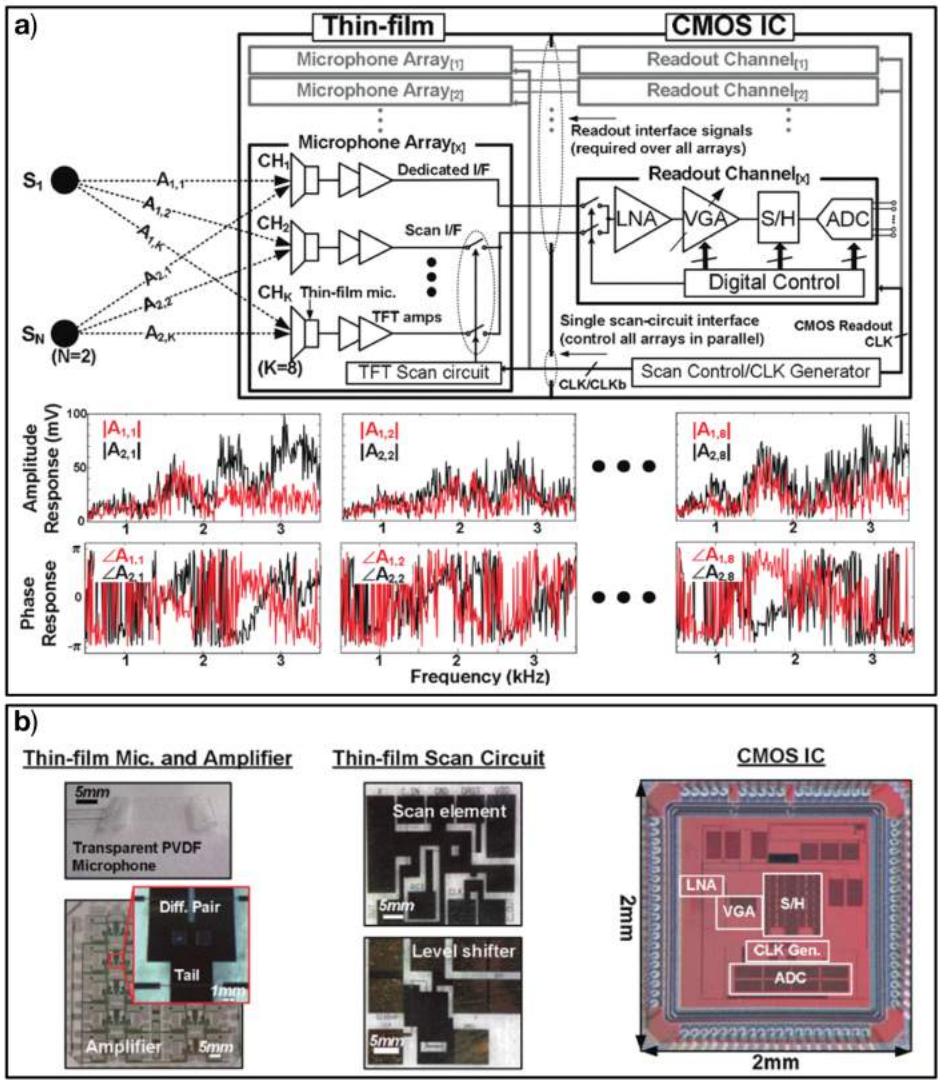


Figure 1.3: Hybrid system for multiple speaker separation implements microphone array, local amplification, and microphone access circuits in LAE, and delegates other functions to CMOS [15].

very wide; large switches in turn have large capacitance, which places a limitation on sensor readout speed and/or number of sensors in the array. Higher mobility TFTs can mitigate this issue because they can be made smaller, reducing switch capacitance.

2. In a system that harvests solar energy and wirelessly transmits harvested power to a load [59], power transfer efficiency is limited by the quality factor (Q) of the inductively-coupled system. An inductor's Q can be enhanced by operating at higher frequencies;

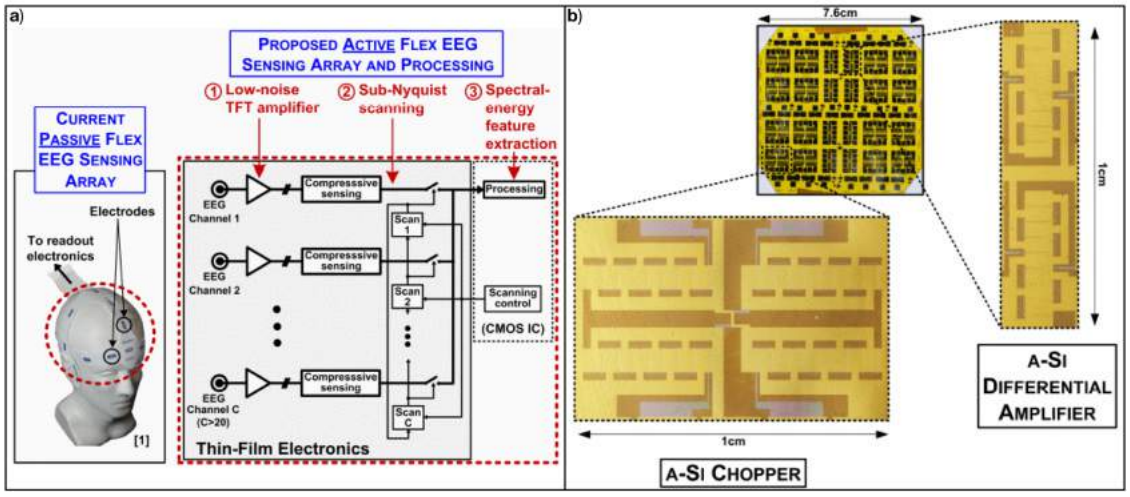


Figure 1.4: Hybrid system for EEG signal acquisition implements electrode array, amplification and sensor sampling in LAE domain, and delegates spectral feature extraction to CMOS [16].

hence, energy harvesting could be made more efficient by using a higher frequency TFT oscillator, which higher transconductance (e.g. higher mobility) TFTs would allow.

3. A system incorporating a large array of microphones for advanced human-computer interfaces [15] incorporates a TFT scanning circuit to sample each sensor; because voice signals include frequency content up to 5 kHz, to avoid aliasing, a scanning circuit would have to sample each sensor at a rate of at least 10 kHz. The low mobility and large sizes (high capacitances) of α-Si TFTs make this sampling speed unfeasible, and acquired signals are aliased. Low scanning speed furthermore reduces the number of speaker sources that can be separated in this system. While signal processing methods are used to resolve this issue, faster scanning circuits – via faster TFTs with low capacitance – could also be used to address this problem.

4. EEG signals fall between 1-500 Hz. A system to acquire EEG signals using TFT circuits to reduce LAE-CMOS interconnections [16] must overcome TFT $1/f$ noise, which is significant within this frequency band. TFT $1/f$ noise is commonly reduced by scaling up devices in width and length; in α-Si this is limited by the minimum pinhole density

resulting from the PECVD process. Creating an improved gate-dielectric technology with reduced susceptibility to pinholes could hence directly reduce $1/f$ noise. To bypass $1/f$ noise in this prior work, a chopper-stabilized approach is used, where acquired signals are up-modulated to 50 kHz to bypass $1/f$ noise. This requires operating the α-Si TFTs at very high overdrive voltages because of the limited f_T of α-Si TFTs, resulting in poor power efficiency. A higher-f_T TFT technology could also benefit the power-efficiency of this system.

These limitations and others underscore that materials-level development – in particular, TFT enhancement via higher mobility semiconductors and improved gate dielectrics – bears enormous promise for enabling next-generation hybrid sensing systems. There are several candidate technologies for LAE TFTs, each of which has its own advantages and drawbacks which must be considered critically. For this purpose, the next section provides an introduction to alternative TFT technologies for large area electronics, describing briefly for each (after a brief historical tangent) the basic physics of conduction, defects and doping, available deposition methods, and common instabilities. At the conclusion of this summary, we contrast attributes of these different technologies, and provide reasoning for how we arrived at the choice of material and deposition method used in this work.

1.2 LAE Foundations: Thin-Film Transistors

Thin-film transistors (TFTs) are field-effect transistors formed at low temperature ($< 350°C$) on physically-large, low-cost substrates, that form the basis for all large-area electronics. Early TFT development proceeded in parallel with integrated circuits in the 60s and 70s – initial TFT efforts focused on cadmium sulfide and selenide, culminating in the first CdSe TFT active-matrix LCD demonstration in 1975 (Figure 1.5) [17]. However, stability, reproducibility, and processing compatibility concerns surrounding CdSe resulted in limited enthusiasm until the development of silicon-based TFTs such as hydrogenated amorphous

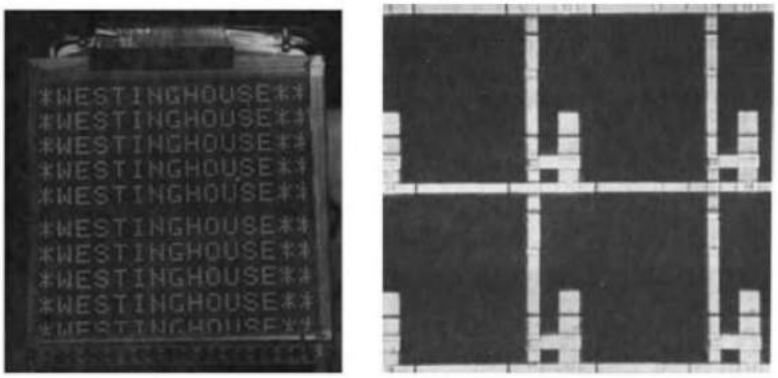


Figure 1.5: Photograph and microscope image of the first active matrix display demonstration in 1975, which incorporated CdSe TFTs [17].

silicon in 1979 [60]. Amorphous silicon's potential for flat-panel displays was immediately recognized, and the first commercial α-Si TFT LCDs followed soon after in the 1980s [19]. Today, the TFT field has a few more players. Amorphous silicon remains popular, but also prominent are metal oxide semiconductors based on ZnO and low-temperature polysilicon (LTPS) (these three have achieved commercial success), and organic semiconductors. More exotic TFTs based on graphene, carbon nanotubes, silicon nanomembranes, perovskites, and chalcogenides are also reported (for example, [61–70]); these candidates will be omitted in our discussion as they are generally considered far from systems integration.

1.2.1 Amorphous Silicon

Physical and Electronic Structure

Amorphous silicon departs from crystalline silicon most significantly in its bonding disorder and high defect density, and conduction in α-Si depends on both properties. While α-Si possesses short range order, with 1st and 2nd nearest neighbor distances that are on average the same as in c-Si, at longer range this order vanishes, and asymmetry in bond angles and bond lengths appear, resulting in a structure called a continuous random network (illustrated for hydrogenated α-Si in Figure 1.6 [18]). Asymmetry in bond angles and lengths distort the conduction and valence band edges, resulting in states extending from the band edge into

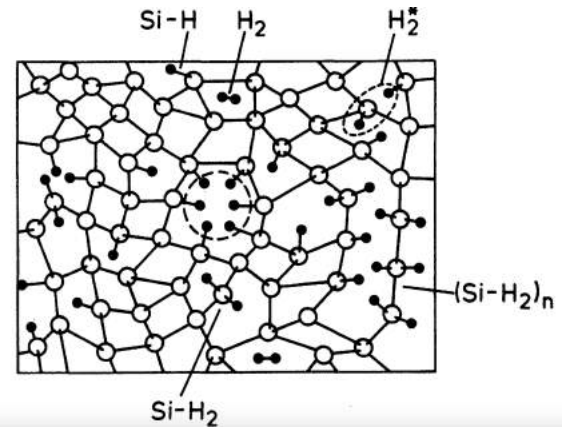


Figure 1.6: a-Si:H structure, showing disorder and availability of different hydrogen-related bonding configurations, e.g. Si–H, Si–H_2, $(Si–H_2)_n$, interstitial H_2, mobile hydrogen, and hydrogenated vacancies [18].

the band gap in which electron wave functions are highly localized. The density of these states decays exponentially as their energies approach mid-gap, resulting in a tail-like shape. The disordered α-Si also contains a high density of material defects, such as dangling silicon bonds. These defects manifest as traps deep within the band gap. A cartoon depicting extended states, localized tail states, and dangling bonds in amorphous silicon is shown in Figure 1.7 [19].

Conduction

Depending on temperature and defect density, the conduction mechanism may be dominated by hopping between localized states in the band tails (low-to-intermediate temperature) or transport in extended states for carriers thermally activated above the mobility edge (multiple-trapping-and-release/mobility edge model), although the last is only visible in state-of-the-art, low-defect α-Si [19, 71]. In all cases, mobility is hindered by the absence of long range order, which results in frequent collisions between carriers and silicon atoms that occur on average every $\sim$10 – 15 $\mathring{A}$ [18]. Because the valence band tail is very broad in α-Si, hole mobility is typically a fraction of electron mobility, making realization of n-channel α-Si TFTs much easier than realization of p-channel TFTs. Typical mobility val-

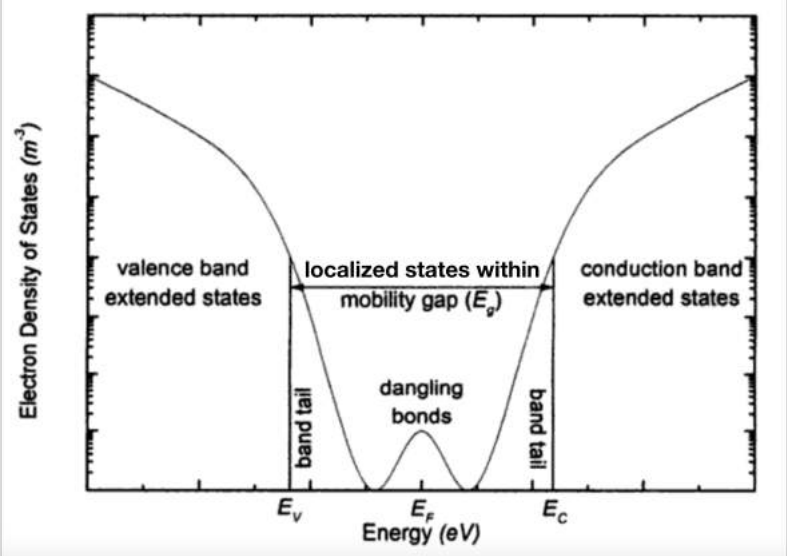


Figure 1.7: a-Si density of states, showing extended (delocalized) states in valence and conduction bands, exponential distribution of tail states (localized) and trap states formed by dangling bond at mind-gap [19].

ues for n- and p-channel α-Si TFTs are 0.3–1 and 0.005 –0.1 cm^2/Vs, respectively (Table 1.5).

Doping and Defects

While mobility for holes is far worse than mobility of electrons in α-Si, both n- and p-type doping is available. The efficiency of α-Si doping is low, since the random network of tetravalent silicon atoms, unlike the crystalline solid, can easily accommodate atoms of various coordination numbers, making substitutional doping challenging – only a small fraction ($\sim$ 10%) of incorporated dopants will demonstrate tetravalent (i.e., active) configuration [18, 72]. Nonetheless, the capability for both n- and p- type doping is of great value in and of itself as it enables fabrication of doped contacts, n- and (modest) p-channel TFTs, photodiodes, and solar cells.

In non-hydrogenated amorphous silicon, the dangling Si bond density is typically $\sim 5 \times 10^{19}/cm^3$, and serves to restrict transport and promote rapid oxidation at external and internal surfaces [73]. Depositing a-Si:H from a hydrogen-containing atmosphere results in a hydrogen concentration of 5-10 at.%, and a dangling bond density many orders of

magnitude lower than in non-hydrogenated α-Si – $10^{15}/\text{cm}^3$ [74, 75]. Because hydrogen will desorb from α-Si films between 300 – 600°C, low temperature deposition processes are key to growing quality α-Si:H films.

Deposition Options

While α-Si can be deposited by thermal evaporation, sputtering, or decomposition of Si-H compound gases, only the latter two methods are compatible with this temperature range [18]. Chemical vapor deposition (CVD) methods (plasma-enhanced, thermal decomposition, etc.) became most popular for reasons of uniformity, yield across large substrates, and potential for high throughput. Plasma-enhanced CVD – wherein an RF discharge is sustained between two parallel plates under constant chamber pressure and gas flow (diagram shown in Figure 1.8) – is the most common method today [18].

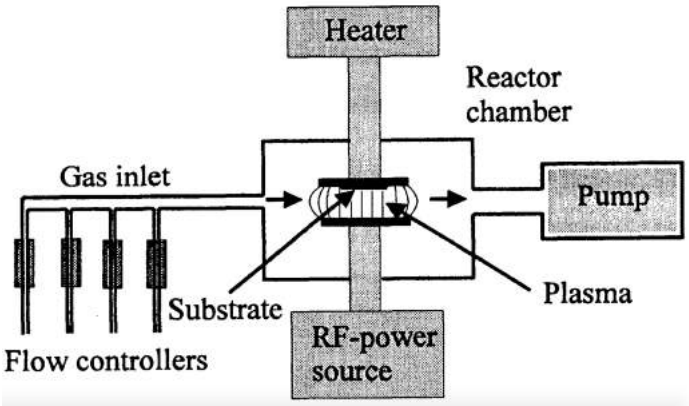


Figure 1.8: PECVD schematic diagram [18].

Instabilities

As with many thin-film semiconductors, α-Si is not without its faults, and has two prominent instabilities. First, the photoconductivity and dark conductivity of undoped α-Si:H decrease by ~ 1 order of magnitude under intense illumination. These effects result from an increase in defect density upon illumination (Figure 1.9) [18].

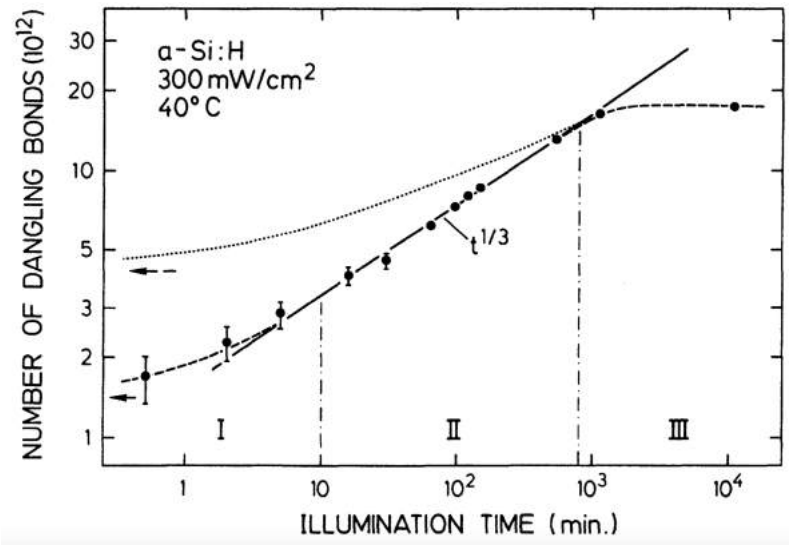


Figure 1.9: a-Si dangling bond density increases as function of illumination time [18].

Although this effect can be reversed by annealing at temperatures $> 150°C$, in practice strategies must be taken to prevent this situation; for example, α-Si TFTs in display backplanes incorporate a light-shielding coating. A second significant instability is that the threshold voltage of α-Si TFTs under constant positive bias increases over time. A two-stage degradation mechanism is responsible for this behavior, and stems from both charge-trapping within the gate dielectric and the formation of new broken bonds within the amorphous silicon [76]. To bypass this instability, applications requiring a stable current source (e.g., OLED display or X-ray imager pixel circuits, etc.) must incorporate multi-TFT compensation circuits, at the cost of circuit complexity and physical area [77].

1.2.2 Low-Temperature Polysilicon

Structure and Conduction

Unlike amorphous silicon, polysilicon retains many of the strengths of single-crystalline silicon because it consists of $\sim$ 100 nm+ crystalline grains separated by grain boundaries, visible in Figure 1.10 [20] (silicon with grain size on the order of 10 nm is technically considered microcrystalline, but distinctions often blur). As shown in Figure 1.11, the larger

the grain size in the polysilicon, the higher the mobility [21].

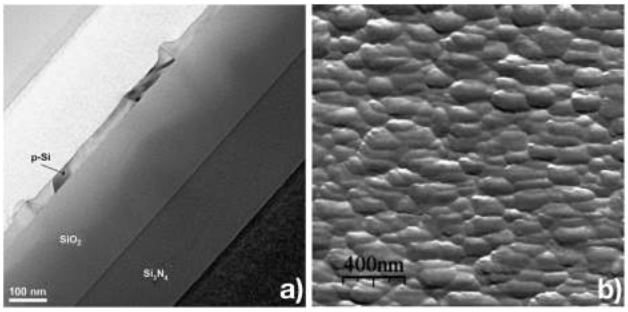


Figure 1.10: Polysilicon (here recrystallized via excimer laser) a) TEM cross section and b) AFM images indicate large grain size [20].

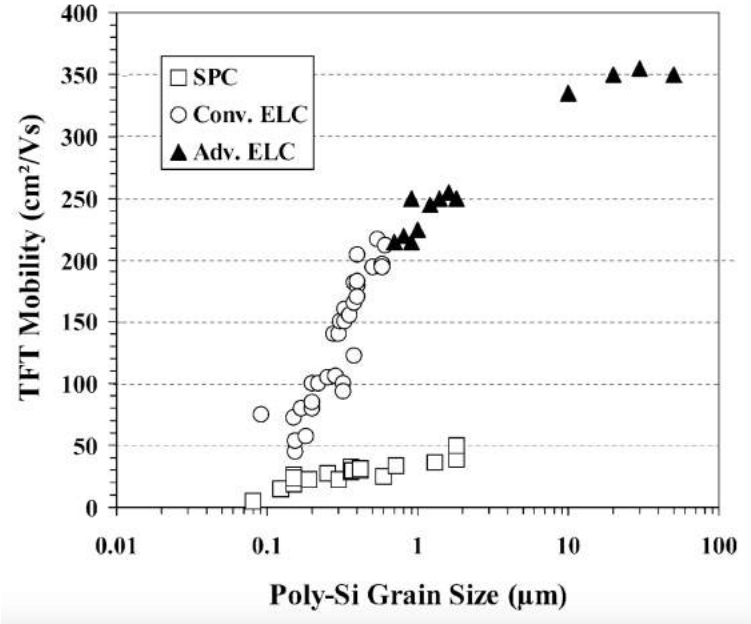


Figure 1.11: Polysilicon mobility is a clear function of grain size. Here we see this relation for polysilicon crystallized by conventional and advanced excimer laser methods (ELC), and also by solid phase crystallization for reference [21].

Doping and Defects

Grain boundaries are a perennial headache for polysilicon TFT designers, as they harbor high densities of material defects (e.g., dangling silicon bonds and oxygen impurities); these pose

problems for solar cells. For TFTs, the main problems are the potential barriers associated with grain boundaries. They are irregularly spaced and of varying heights; this makes the effective mobility vary between TFTs [78]. As in α-Si, dangling silicon bonds can be passivated with hydrogen, commonly in the form of a plasma post-treatment [78, 79]. In the simplest model, transport in polysilicon is determined by thermionic emission across potential barriers at grain boundaries (illustrated in Figure 1.12 [22]).

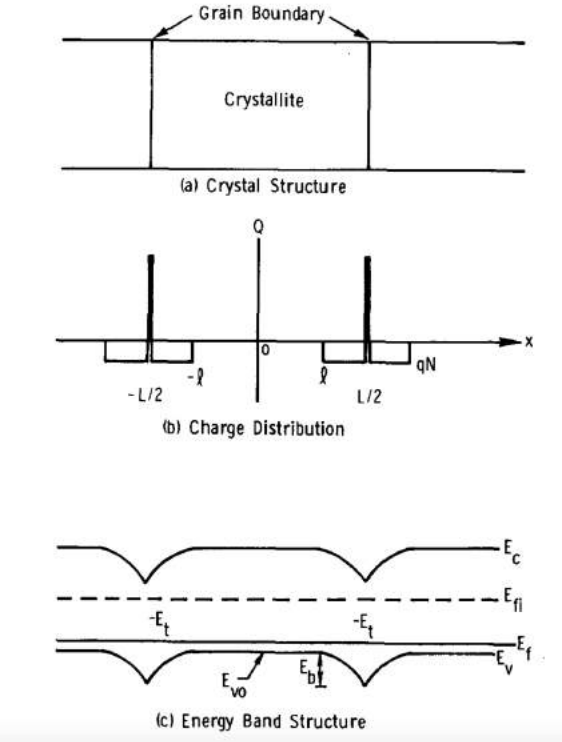


Figure 1.12: Grain boundaries in polysilicon form potential barriers for carriers – in this case, holes [22].

An essential feature of polysilicon conduction is its doping dependence; at low doping densities ($< 10^{18}/\text{cm}^3$), energy barriers between grains are large; at a critical doping density, energy barriers greatly reduce (Figure 1.13 [22]) [78]. Typical field-effect mobilities in polysilicon, including other standard TFT parameters, are provided in Table 1.5.

As in α-Si, polysilicon can be doped either n- or p-type, but unlike α-Si, complementary circuits are easily realized because hole mobility is relatively close to electron mobility.

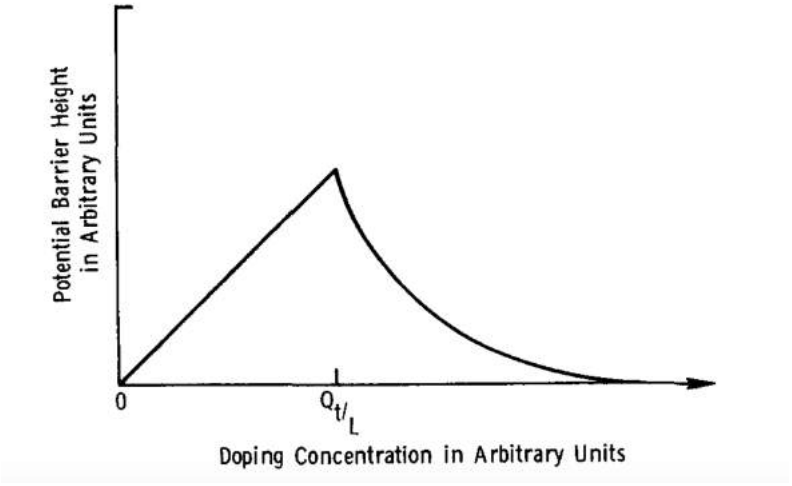


Figure 1.13: Barrier height is a function of doping in polysilicon [22].

Doping is thought to be less efficient than in monocrystalline silicon, because the high concentration of defects at grain boundaries act as traps for free carriers generated by doping. However, once these traps have been filled, the crystalline grains can be doped with much higher efficiency than α-Si [22]. Reported n- and p-channel low-temperature polysilicon TFTs have mobilities of 50–200 and 10–60 cm^2/Vs, respectively (Table 1.5).

Deposition Options

Polysilicon can be deposited directly at temperatures $> 540°C$; extensive literature exists describing how to precisely engineer polysilicon films via low-pressure CVD (LPCVD), and also via PECVD, where for the latter suppressing ion energy via high (~ 70 MHz) frequency plasmas, heavy dilution gas (e.g., deuterium vs hydrogen), and/or electrode configuration (triode, biased-wall) is key to creating highly crystalline materials [24, 78, 80]. However, to ensure compatibility with glass and plastic substrates, polysilicon for use in TFTs is typically laser-crystallized from dehydrogenated PECVD α-Si films (Figure 1.14 [81]), which reduces both the maximum process temperatures for the substrate to 300 – 400°C and film defect density compared to alternative recrystallization methods (e.g., thermal crystallization is

another common method, but requires temperatures of $\sim 600°C$ and soak periods of several hours: the product is known as low-temperature polysilcon (LTPS)) [20, 24, 79, 81].

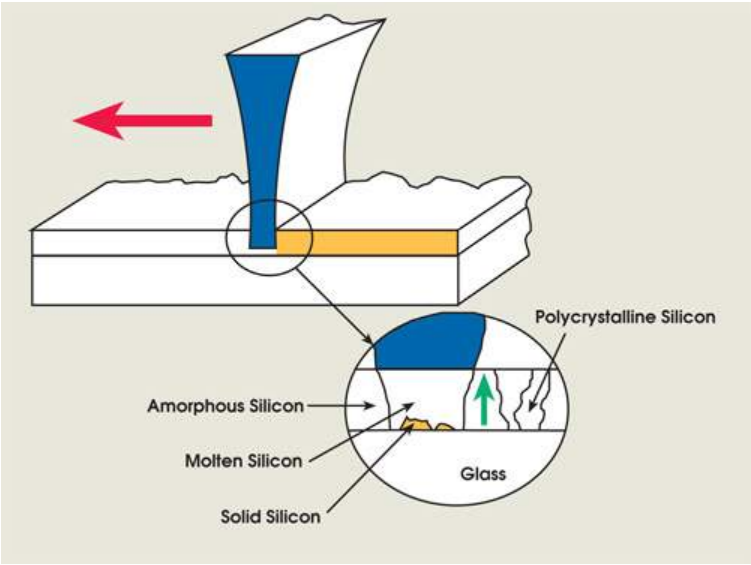


Figure 1.14: Excimer laser annealing process, showing thermal buffer layer and scanning beam [23].

Crystallization via laser heating is generally identified as such in order to distinguish the technique from LTPS. These processes most commonly exploit short (10 – 30 ns) excimer laser pulses of ~ 100 mJ/cm^2 intensity, which have wavelengths (~ 200 – 300 nm) that are readily absorbed within the first several nanometers of silicon. A ~ 100 nm thick silicon film and ~ 200 nm thick SiO_2 buffer layer ensure that the temperature of the underlying glass substrate can be kept below 400°C for these short pulses [20]. Nonuniformity of these films (and ultimately LTPS TFTs) stems from two sources: grain boundaries, and laser nonuniformity. While the former cannot be fully eliminated, the later can be ameliorated via multiple laser passes, and continues to improve as laser technology advances [21].

Instabilities

When LTPS was first incorporated into TFTs, the off current was found to be generally high and strongly gate-bias dependent – highly undesirable features for most circuit applications

which demand low static power. Both high off-state current and LTPS defect density can be reduced by hydrogen passivation (Figure 1.15 and Figure 1.16), suggesting that defects in grain boundaries act as carrier generation centers [24].

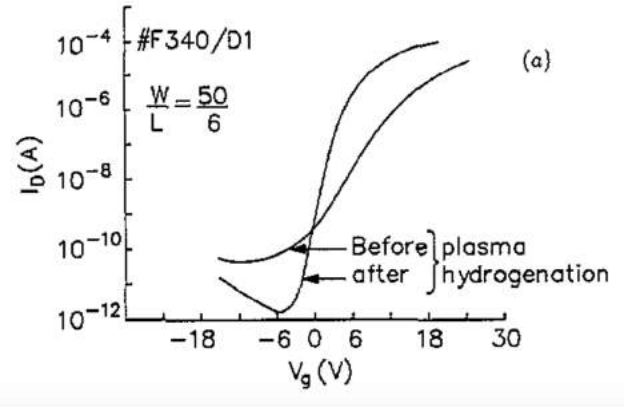


Figure 1.15: Current-voltage characteristics in a polysilicon TFT before and after hydrogenation [24].

High electric fields in the drain region of the TFT also contribute to large off currents at large negative gate bias (gate-induced drain leakage) due to band-to-band tunneling in the gate-drain overlap region. High electric fields near the drain also result in hot-carrier-related instabilities can result in disfiguration of the I_D – V_{DS}. Both bias-related problems can be reduced by lightly doping the drain region of the TFT (LDD) to increase the distance over which the bias is dropped, so long as the increase in series resistance can be managed [82]. While much progress has been made, off-currents remain higher in LTPS than in amorphous silicon or oxide TFTs. Unlike amorphous silicon TFTs, polysilicon TFTs demonstrate excellent stability under intense illumination [78].

1.2.3 Metal-Oxides

Metal oxide semiconductors are a broad class of materials containing certain binary, ternary, and quaternary oxides of transition and post-transition metals. While semiconducting metal oxides have been explored for at least 90 years [83], they have enjoyed renewed interest

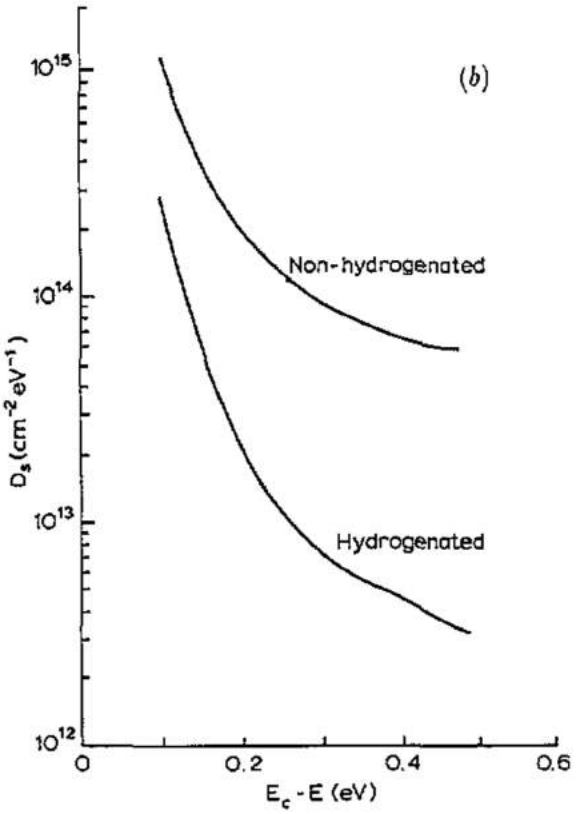


Figure 1.16: Defect density in polysilicon before and after hydrogenation [24].

within the past 20, culminating most recently in commercial realization of oxide-TFT LCD displays in 2012 [84]. Within the TFT community, ZnO-based metal oxides (including indium-gallium-zinc-oxde or IGZO) are most popular.

Structure and Transport

ZnO single crystals have a Wurtzite lattice structure (Figure 1.17 [25]), but at LAE-compatible deposition temperatures, ZnO is typically polycrystalline [85].

Concerns about both the uniformity of polycrystalline ZnO over large areas (rooted in experiences with LTPS TFTs) and mobility reduction via trap states at grain boundaries drove TFT materials developers to introduce additional metal atoms (with different cation coordination numbers) into the ZnO structure to disrupt crystal formation and produce an amorphous structure. Because the conduction band of ZnO consists of spherically symmet-

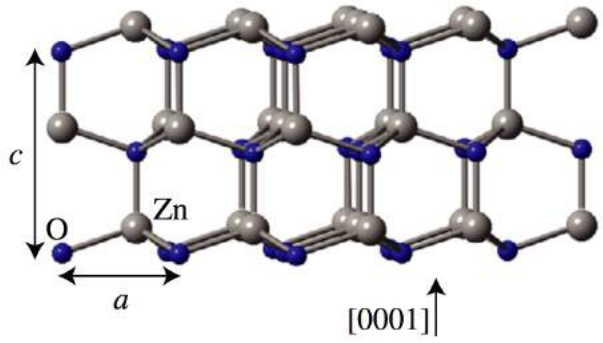


Figure 1.17: Wurtzite structure of ZnO [25].

ric Zn 4s orbitals (conduction bands of Ga2O3, In_2O_3, Al_2O_3, and SnO_2 are also s-orbital based [86]), structural disorder is thought to have less influence on electron mobility than in materials like silicon, and mobilities of polycrystalline and amorphous ZnO-based materials are similar – an illustration of this intuition is shown in Figure 1.18, and Hall mobilities for amorphous and single crystal IGZO are shown in Figure 1.19 [26]. Metal oxide TFT mobilities fall in range of 10–50 and 0.5–1 for n- and p-channel devices, respectively; additional parameters can be found in Table 1.5.

In contrast, the ZnO valence band is defined by highly electronegative oxygen, whose 2p orbitals do not maintain orbital overlap in the presence of structural disorder and remain highly localized. Furthermore, the valence band maximum is positioned so low in metal oxides that hole injection forms an additional challenge [86]. Both factors result in poor hole conduction in ZnO. Addition of indium or tin can further enhance mobility for electrons; their large 5s orbitals enhance orbital overlap in the conduction band [85]. P-type metal oxides usually rely on copper-containing oxides such as $CuAlO_2$ and $SrCu_2O_2$, whose 3d energy levels, which lie slightly above the 2p levels in oxygen, may hybridize with 2p levels, raising the position of the valence band maximum and making hole injection feasible [87]. An additional approach is to use introduce chalcogens into copper oxides, whose p orbitals could hybridize with copper d orbitals to become less localized than oxygen p orbitals [88].

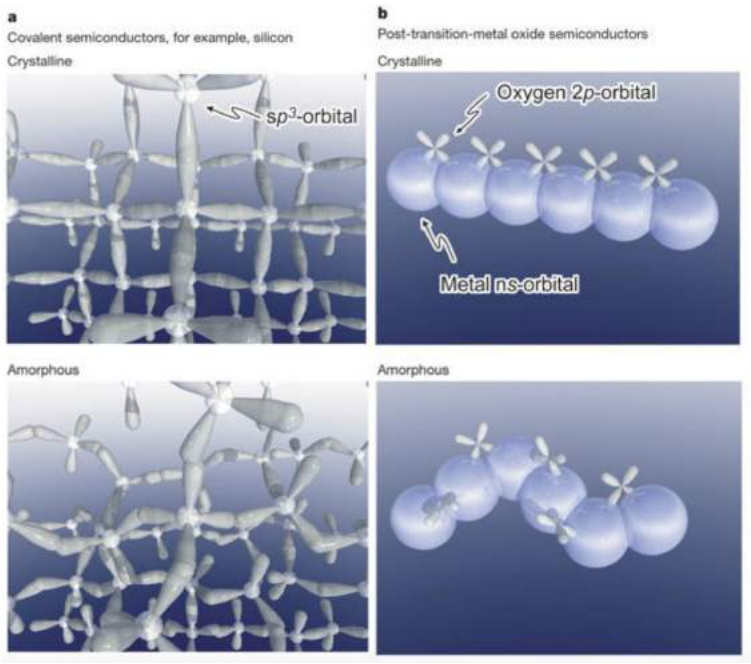


Figure 1.18: Large, symmetric s-orbitals form the conduction band in most metal oxides, resulting in less sensitivity to disorder compared with silicon's sp^3 orbitals [26].

P-type oxide semiconductors remain an area of active research, and focus on strategies to increase valence band dispersion.

In literature, several attempts have been made to describe transport phenomena in zinc-based metal oxides (namely, a strong Hall effect and a mobility that increases with free-electron density and temperature) using existing models; MTR [89] and percolation [90], compared conceptually in Figure 1.20 [27], cannot provide an adequate match across a broad gate voltage and temperature range individually, and variable range hopping is largely considered irrelevant in the presence of the observed Hall effect [27, 91, 92].

The most sophisticated attempts combine and/or extend these models. Bhoolokam et al. find that combining percolation (which matches well at high V_{GS}) with MTR (which matches well at RT) and additionally considering scattering mechanisms results in a model that fits I-V characteristics broadly across temperatures from 120 – 300°C [27]. Germs et al. find that extending the MTR model to include (simultaneously) variable range hopping

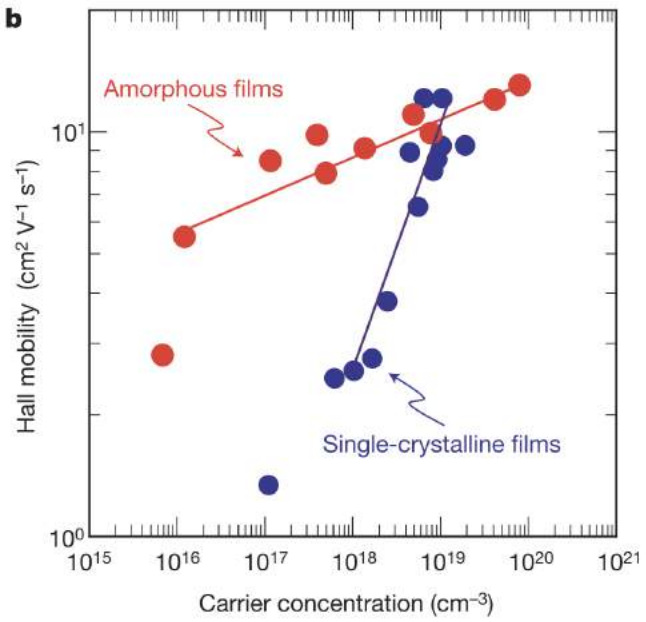


Figure 1.19: Hall mobilities in amorphous and single-crystal metal oxide (in this case, IGZO) films are similar [26].

in localized states provides a clear improvement over the percolation model, matching not only I-V behavior across a range of gate biases and temperatures, but also matching experimentally measured Seebeck coefficients and the DOS as determined by Kelvin probe [92].

Doping and Defects

Doping in metal oxide semiconductors is typically performed by adjusting material stoichiometry, particularly by controlling the concentration of oxygen vacancies. While a positive correlation between conductivity and oxygen vacancies was long observed in ZnO-based semiconductors, confusion arose because the position of oxygen vacancies is deep within the band gap, and hence unlikely to contribute dopants in and of itself. Theoretical calculations of formation energies indicate that both interstitial and substitutional hydrogen (H_O) are the most likely sources of shallow donors in ZnO, resulting in ZnO's typical unintentional n-type doping (Figure 1.21 and Figure 1.22 [25]); of these two options, substitutional hydrogen has a larger diffusion barrier and is more stable [86].

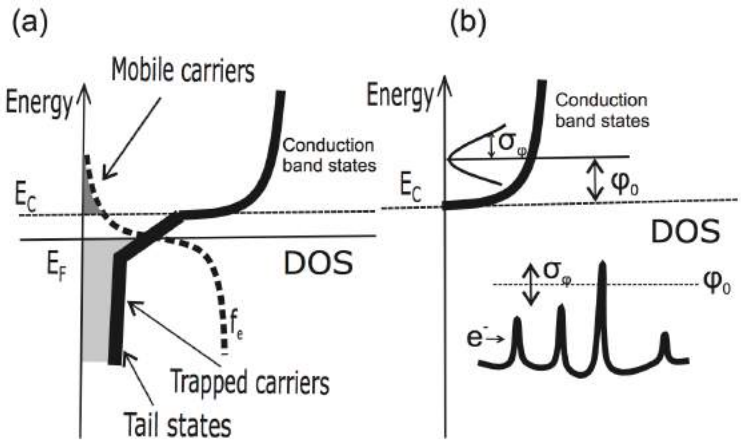


Figure 1.20: a) MTR model: Fermi level E_F determines amount of trapped and mobile carriers. b) percolation model: Gaussian distribution of barriers in conduction band hinder charge transport [27].)

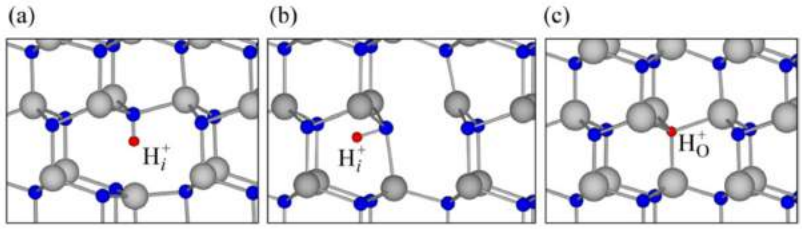


Figure 1.21: Different configurations in which hydrogen may incorporated into a zinc oxide lattice: a) and b) depict interstitials, c) depicts substitution of oxygen [25].

Interestingly, hydrogen has also been used recently to passivate defects in grain boundaries of polycrystalline ZnO, indicating additional benefits to incorporation of H in ZnO-based films [93]. Acceptors in ZnO can be introduced as substitutional nitrogen (N_O), although the position is too far from the VBM to result in useful hole concentrations. The higher the position of the Fermi level in ZnO, the lower the formation energy for N_O; hence, N_O can play a role as a compensating acceptor in ZnO [86]. Extrinsic doping is also available; a large survey can be found in [94]. In copper-based p-type oxides, copper vacancies and oxygen interstitials are considered the source of holes [88]. Doping can further be altered in metal oxides with more constituent atoms. For example, indium incorporation results in higher electron density because oxygen vacancies are formed more readily. Conversely,

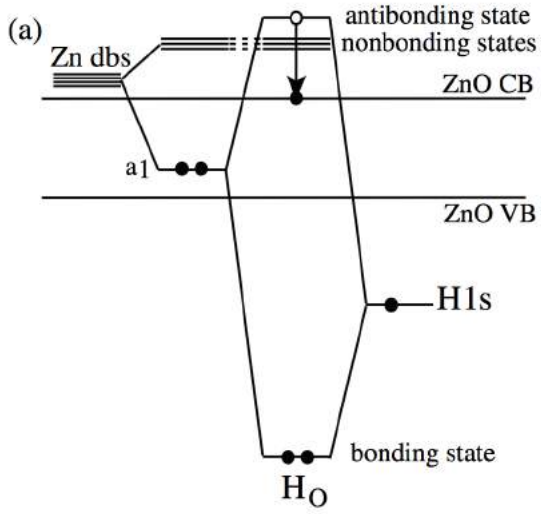


Figure 1.22: Hydrogen occupying an oxygen site results in antibonding states in the conduction band of ZnO; hence H_O acts as a shallow electron donor [25].

gallium is typically introduced into amorphous metal oxide films as a carrier suppressor, as it bonds more tightly to oxygen than Zn or In, preventing the formation of oxygen vacancies; many other materials, e.g. La, Ti, W, have been shown to serve a similar role [95]. A summary of mobility and carrier concentration for varying ratios of In_2O_3, GaO_3, and ZnO is shown in Figure 1.23 [28].

Deposition Methods

A range of large-area-compatible deposition methods are available for metal oxides. Most commonly reported is sputtering [96] (in part because it is a high-throughput technique that promotes transfer to industry), but pulsed laser deposition [97–99], atomic layer deposition [100–102], MOCVD [103, 104], and solution-based [105] methods are also available. Aside from solution-based methods, all other processes result in comparable TFT mobilities (pulsed laser deposition plus 400°C post-processing on silicon substrate has provided the low temperature ZnO TFT mobility record of 60 – 100 cm^2/Vs, but PLD at

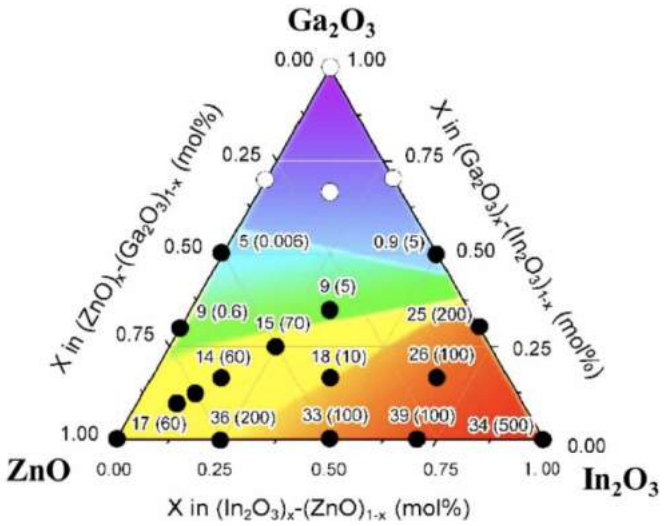


Figure 1.23: By altering the stoichiometry of IGZO films, a range of material properties can be achieved. At each dot on the diagram, mobility in cm^2/Vs and carrier concentration (in parenthesis, in $10^{18}/cm^3$) are shown [28].

lower temperatures does not boast comparably high results). As mentioned, sputtering is an industry-favored technique and a wealth of literature on sputtered IGZO TFTs is now available. However, thickness control in sputtered metal oxide films [106], and conformal step coverage – of particular value for TFTs on rough plastic substrates – remain limited. PLD has limited scalability to large areas. MOCVD can improve conformality, uniformity, and throughput, but work thus far is at temperatures $\sim 400°C$, acceptable for glass but not for plastic substrates. Solution-based methods focus on throughput and cost reduction, but increasing mobility and controlling uniformity remain significant obstacles. ALD-based deposition, which offers layer-by-layer deposition, provides a compelling means to address these uniformity and conformality, at the cost of deposition throughput. A summary of oxide deposition tradeoffs is listed in Table 1.4.

Instabilities

As metal oxide TFTs have been pushed to commercialization, a host of instabilities (largely those in IGZO) have emerged and undergone intense scrutiny. First, sensitivity to moisture

and atmospheric hydrogen (as metal oxides have been used routinely for gas sensing) necessitates the use of an effective passivation layer [107–109]. Second, positive (negative) gate bias stress on TFTs results in a positive (negative) shift in threshold voltage; these effects have been attributed to charge trapping at the semiconductor/dielectric interface [85, 97]. Third, oxides have also been shown to be sensitive to both visible and UV illumination, exhibiting a very large negative threshold shift in the presence of light and negative bias, attributed to photo-generated holes trapped at the gate-dielectric interface [107, 110, 111]. Efforts to mitigate these effects focus on interface improvement via innovative device structures, gate insulator development, post treatment with annealing and plasma, and light shielding [85, 112, 113].

Table 1.4: Summary of LAE-compatible metal oxide deposition methods.

Process	**Pros**	**Cons**
PLD	⊕ Highest-performance devices ⊕ Stoichiometric transfer	⊖ Reduced throughput ⊖ Limited large-area scalability (rastered laser and gradient heating of substrate required)
Sputtering	⊕ Area-scalable ⊕ Industry-compatible ⊕ Fast deposition ⊕ Room-temp. deposition ⊕ Enables stoichiometric experimentation	⊖ Poor uniformity control ⊖ Poor step coverage
ALD	⊕ Layer thickness control ⊕ Excellent step coverage ⊕ High density films with low defect/pinhole density	⊖ Poor industry compatibility ⊖ Slow (except spatial ALD),
MOCVD	⊕ Fast growth rate ⊕ Large-area uniformity	⊖ Reduced reaction control ⊖ Limited capability to reduce temperature $< 350°C$
Solution	⊕ Highest potential for low-cost	⊖ Poor uniformity control

(Continued on next page)

Table 1.4: (continued)

Option	Description	
	and roll-to-roll processing	⊖ Poor device performance

1.2.4 Organics

Structure and Transport

Organic semiconductors are based on small molecules (e.g., oligoacenes like rubrene, tetracene, pentacene, and derivatives) and polymers (e.g., polyparaphenylene, polythiophene, polyfluorene, etc.) that are highly conjugated. Figure 1.24 shows several of the most studied organic semiconductors [29].

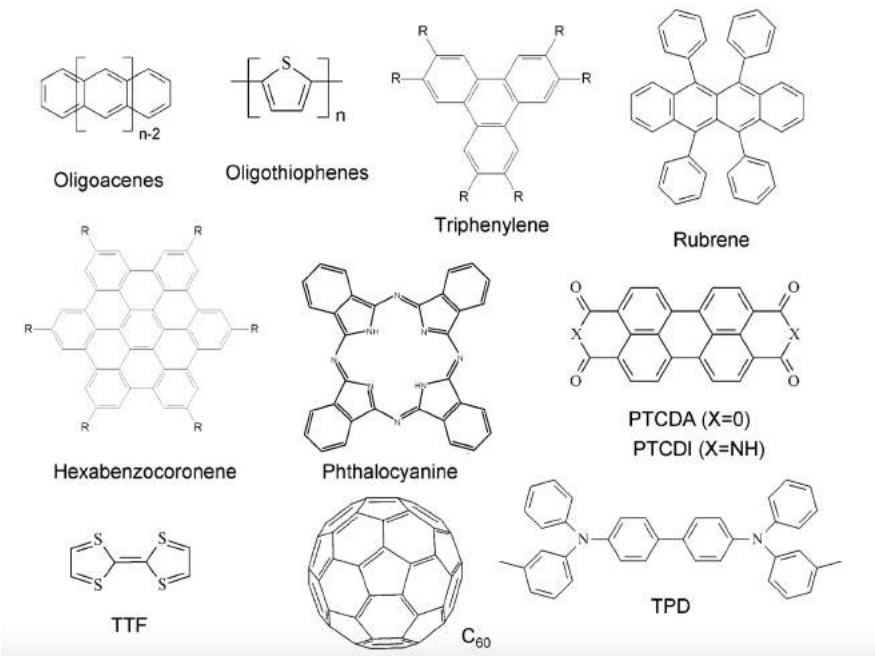


Figure 1.24: Some of the most studied small-molecule and polymer organic semiconductors [29].

Overlap between electron wavefunctions (typically p-orbitals, which form a π-bonding network as visualized in Figure 1.25 [30]) form the "valence" (highest occupied molecular orbital, or HOMO) and "conduction" (lowest unoccupied molecular orbital, or LUMO) bands

for organics. If the degree of overlap is large, these molecules can exhibit high mobilities, which can be as high as 400 cm^2/Vs in single-crystal organic semiconductors at cryogenic temperatures [30] (and even $\sim$ 10 cm^2/Vs at room temperatures [29, 114]).

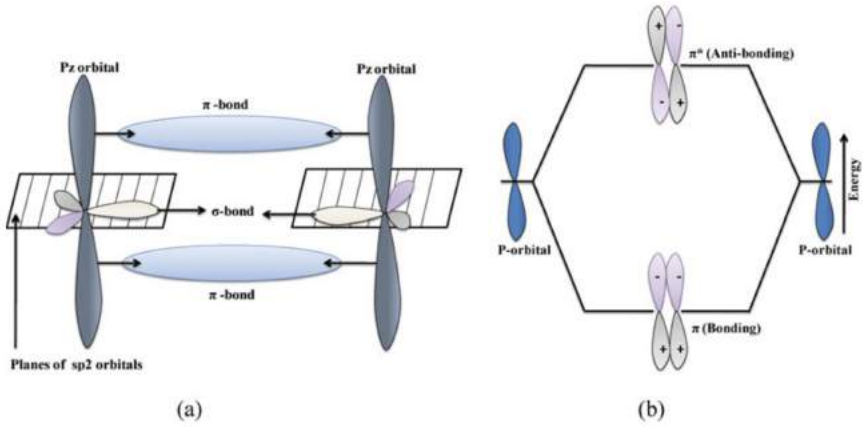


Figure 1.25: π bonding network form bonding and anti-bonding levels in organic semiconductors, which ultimately determine HOMO and LUMO levels [30].

In disordered organic semiconductors, mobility is degraded by the presence of defects (typically impurities) between crystal grains, localization of states, lattice vibrations, and for TFTs, interactions with the gate insulator. Mobility is strongly temperature- and gate-voltage dependent; typical values for organic TFTs are shown in Table 1.5. Transport is often modeled as variable range hopping (for highly disordered semiconductors), multiple trapping and release (e.g., thermal activation out of tail states over mobility edge into delocalized states), or via a polaron-based model, which becomes relevant in inorganic systems where electron-phonon coupling is dominant [29, 30, 115]. In crystalline organic semiconductors, mobility decreases with temperature and electric field, while in disordered organics, the opposite behavior is observed [29, 114].

Measurements in single crystal organic materials in inert environments indicate that mobilities for electrons can be as high as for holes; nonetheless, extrinsic factors (e.g., 1) rapid oxidation of low work function metals (Al, Mg, Ca) that could provide low electron injection barriers and 2) the small electron affinities ($<$ 3 eV) of available organic semiconductors

that result in rapid reaction with atmospheric moisture) result in very limited availability of n-type semiconductors [29, 114]. At present, only p-type organic TFTs are considered viable, precluding complementary circuits [114]. Demonstrated organic TFT mobilities are typically 0.1–10 and 0.005–2 cm^2/Vs for p- and n-channel devices, respectively (Table 1.5).

Doping

Doping is available in organic semiconductors, but is not substitutional: to p-(n-)dope, oxidizing(reducing) materials are added, such that the lowest unoccupied(highest occupied) states in the dopant match the energy in the highest occupied(lowest unoccupied) states in the undoped material (as in Figure 1.26 [31]).

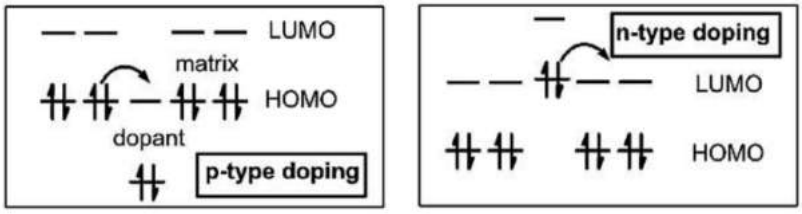


Figure 1.26: Positioning of dopant HOMO and LUMO levels relative to those of the doped material for n- and p-type doping [31].

Deposition Methods and Limitations

Since only weak Van-der-Waals forces hold these molecules together, the orientation of the π-electron system is dependent on material structure, which can depend on deposition method [114, 116]. While small-molecule organics are often evaporated, they can also be made soluble by attaching ligands to acene groups, making solution-processed methods like spin-coating, stamp-printing, blade coating, ink-jet printing, gravure-printing, and even self-assembly accessible [116–118]. Crystallization in these systems can then be controlled by controlling parameters like evaporation, shear rate, etc. Solution processing bears promise as a potentially low-cost deposition technique, and is arguably the most compelling feature of

organic TFTs. Ongoing challenges for organic semiconductors include enhancing uniformity over large areas, reducing material impurities that limit mobilities, and improving air- and bias- stability [30, 119–121].

1.3 TFTs for Hybrid Systems: Summary

We have now seen that there are many large-area compatible TFT technologies; each has its advantages and drawbacks. A summary of condensed TFT parameters for each of the four technologies discussed is provided is Table 1.5. Upon inspection of this table, we can see that polycrystalline silicon and metal oxide TFTs have the most impressive device characteristics. Between these two candidates, recall that recrystallization processes for LTPS are still limited in scalability because uniformity of devices across increasingly large areas remains a great technical challenge. Furthermore, note that LTPS requires the most lithographic steps – up to 11 masks for complementary circuits– and is accordingly the most expensive technology of the four presented. In contrast, metal oxides are readily scaled and have a similar lithographic process for TFT fabrication to amorphous silicon. These factors (in addition to the aforementioned strong electronic characteristics) make metal oxides most appealing for deployment in hybrid systems. Of metal oxides, zinc-based oxides have repeatedly shown the highest promise.

However, as seen in Figure 1.23, there are many stoichiometric options even within the category of zinc-based oxides. In hybrid systems, our priority is moderate mobility that is uniform over broad areas. Unadulterated ZnO provides the simplest starting material, requiring the minimum amount of stoichiometric experimentation as a binary material, but has been considered unattractive because it is typically a polycrystalline material with grain boundaries. Grain boundaries are considered to have two disadvantages. First, it is presumed that mobilities in polycrystalline material will suffer due to trap states within grain boundaries. However, it is clear from literature that ZnO TFTs have mobilities in the 10–

45 cm^2/Vs range – fully comparable to amorphous metal oxide TFTs like IGZO [93, 100]. The second concern assumes non-uniformity in ZnO grains and grain boundaries will inhibit large-scale uniformity. However, if the grain size is much less than the TFT channel length, it is not clear that grain boundaries would impact TFT uniformity over large areas. In hybrid systems, typical TFT channel lengths are in the 2 –15 μm range. Literature on ZnO TFTs indicates that grain size depends on deposition conditions, but is typically in the range of 15 – 50 nm [122–124]. For this reason, we do not consider poly- (e.g., nano-) crystalline ZnO to present serious drawbacks within hybrid sensing systems applications, while its stoichiometric simplicity remains a distinct advantage.

Returning to Table 1.4, we see that there are many options for metal oxide deposition; of these, it is evident that sputtering and ALD are the strongest candidates. In this work, we choose an ALD deposition process because 1) it provides the largest degree of control of thickness across broad areas, 2) it creates very dense, stoichiometric films, which is important in ZnO for controlling unintentional doping, 3) it is a naturally conformal process, capable of covering thick gate metal steps and rough plastic substrates, and 4) it can be used to deposit high-quality Al_2O_3, which can be used as both a dielectric layer and passivation/barrier layer, enabling a process in which dielectric, semiconductor, and passivation can be deposited without breaking vacuum, thereby protecting the (highly-ambient-sensitive) semiconductor from ambient contamination. In particular, we use a weak-oxidant plasma-enhanced ALD process (PEALD) pioneered by the Jackson group [100], which will be discussed in detail in Chapter 2.

1.4 Contents of this Thesis

As the title hints, this thesis begins with one kind of system-building (construction of a thin-film deposition system), and concludes by describing realization of a very different kind

Material	$\mu_n(cm^2/Vs)$	$\mu_p(cm^2/Vs)$	$V_{TH}(V)$	$SS(V/dec)$	I_{on}/I_{off}	Masks
Poly-Si	50–200	10–60	1.5–8	0.1–0.5	10^8	5–11
α-Si	0.3 -1	0.05–0.1	3	0.5–0.75	10^7–10^8	4–5
Metal oxide	10–50	0.5–1	0–3	0.12–0.4	10^7–10^{10}	4–5
Organic	0.005–2	0.1–10	-0.1– -10	0.1–1	10^3–10^8	–

Table 1.5: Summary of TFT properties of 4 major LAE-compatible technologies, including field-effect mobilities for n- and p-channel devices, threshold voltages, subthreshold slopes, on/off ratios, and number of masks required in a lithographic process. V_{TH}, SS, I_{ON}/I_{OFF} provided for n-channel devices, except for organic semiconductors, where parameters are from p-channel devices.

of system (a large-area force sensing system). The intermediate chapters describe all the steps required to make this journey.

Chapter 2 provides an introduction to ALD as a material deposition method, focusing on the particular advantage that plasma-enhanced ALD can provide for thin-film systems on plastic. It then describes in detail the design of the PEALD system used in this work, including a basic discussion of plasmas, chamber designs, and other components in deposition systems that informed design decisions. Lastly, Chapter 2 gives construction details and other practical considerations for all elements of the PEALD.

Chapter 3 focuses on materials and TFTs. It begins with basic material characterization needed to validate PEALD operation. Next, materials are built up into TFTs, and recipe development for several types of TFT configurations and associated challenges are described. The bulk of the section consists of TFT characterization, including DC and high-frequency TFT performance, behavior under mechanical and temperature stress, and TFT variation on large-area substrates.

In Chapter 4, the discussion shifts to circuits based on ZnO TFTs. As described in this section, several TFT circuits act as building blocks for LAE systems. We describe in particular the advantages and drawbacks of shifting from amorphous silicon-based TFTs to ZnO TFTs in two kinds of circuit blocks where we expect the largest benefit from ZnO– scan circuits and oscillators.

Chapter 5 builds upon previous chapters, and describes the realization of a full ZnO-TFT sensing system, which as described is the driving force behind this work. This system uses a unique architecture that allows for highly-scalable LAE systems with very large numbers of distributed sensors. This architecture is based on high-frequency ZnO TFT oscillators, that enable sensor signals to hop between several frequency channels in unique patterns; although sensor signals are summed in a single differential interface, these unique patterns enable faithful sensor signal reconstruction with extremely low error.

In Chapter 6 we provide conclusions, and point to directions for future work (of which there are many).

Chapter 2

Design and Construction of a Plasma-Enhanced ALD System

Atomic layer deposition (ALD) is a method for growing thin-films from vapor-phase reactants that are sequentially input into a deposition chamber separated by a purge step, in contrast to CVD, in which reactant gases (often identical to those in ALD) are simultaneously present in the deposition chamber. In thermal ALD, two individual surface reactions occur per deposition cycle, resulting in a binary compound film. Because the sites for these surface reactions are finite (e.g., hydroxyl groups at the substrate surface, etc.), the reactions are typically self-limiting. This results in a film-growth method with 1) Angstrom-level thickness control, 2) pinhole-free films, and 3) excellent step coverage, so long as reactants are given sufficient time to reach deep into troughs (as in Figure 2.3). Figure 2.1 provides a helpful schematic illustrating the impact of temperature on the ALD process window.

ALD growth is also possible on polymer substrates, and in fact ALD films can serve as excellent vapor barriers on hygroscopic polymer films. Figure 2.2 shows a cartoon describing thin-film nucleation by ALD on a polymer; ALD precursors diffuse into polymer substrates and react, filling up gaps between polymer chains until a uniform surface is produced. For

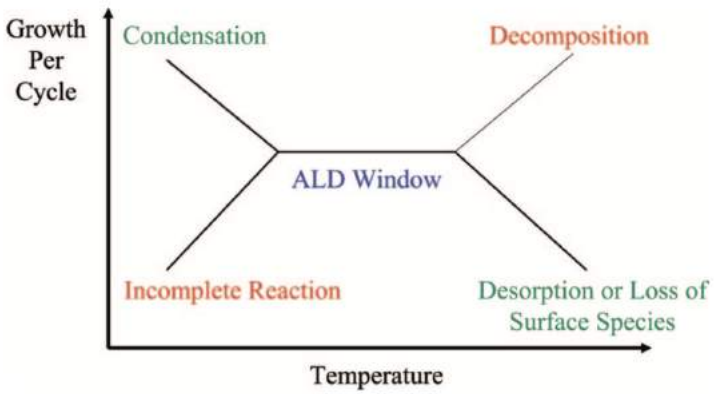


Figure 25. Schematic of possible behavior for the ALD growth per cycle versus temperature showing the "ALD" window. (Adapted from ref 12.)

Figure 2.1: Schematic showing process window for ALD, including irregular growth patterns outside of window from [32], adapted from [33].

this reason, layers of ALD Al_2O_3 just 10 nm thick can reduce the water vapor transmission rate through PI and PEN substrates by more than 3 orders of magnitude [34].

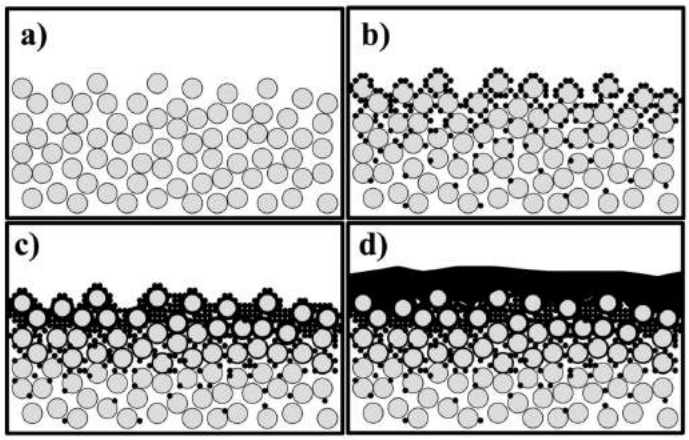


Figure 2.2: Aluminum oxide growth on a substrate consisting of large polymer chains (a) commences with cluster formation within the substrate (b); clusters coalesce and fill gaps between polymer chains (c), ultimately allowing dense films to grow (d) [34].

The most prominent drawback to ALD is that it is slow compared to other thin-film deposition methods. However, although the large-area display industry has yet to adopt ALD, it is worthwhile to point out the semiconductor industry has embraced it – e.g.,

Intel has relied on ALD for high-k dielectrics (HfO_2) since 2007 [38]. Hence, there is some precedent for high-volume ALD, should the display industry warm up to the technology in the future.

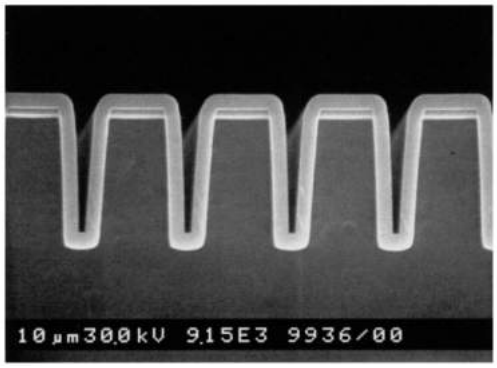


Figure 2.3: TEM showing cross-section of 300 nm Al_2O_3 on silicon structure [35].

ALD is commonly used to deposit oxide films, in addition to nitrides, phosphides, and sulfides – as a result, a wealth of literature exists describing ALD of ZnO and Al_2O_3, the materials of interest in this work [125–129]. While thermal ALD is a robust and versatile technique, there are several instances in which incorporation of plasma into an ALD process (i.e., plasma-enhanced ALD, or PEALD) can enable or significantly enhance material growth. In PEALD, alternating precursor and reactant doses are replaced by a cyclic sequence of precursor release and plasma initiation – for comparison, this difference is illustrated in Figure 2.4 [36].

For some materials for which thermal ALD deposition is not available, highly-reactive radicals in PEALD create a new reaction pathway, enabling ALD growth of single-element metals like Ti and Ta. For this work, we were primarily drawn to PEALD because it allows growth of higher density and higher purity films at lower temperatures than those afforded by thermal ALD [32, 129]. Hence, PEALD is doubly beneficial – it first promises ZnO with a lower density of oxygen vacancy than thermal ALD ZnO (and hence lower as-grown conductivity) and second, by enabling deposition at reduced temperature, it increases the types of large-area substrates at our disposal. Plasma also provides the TFT designer

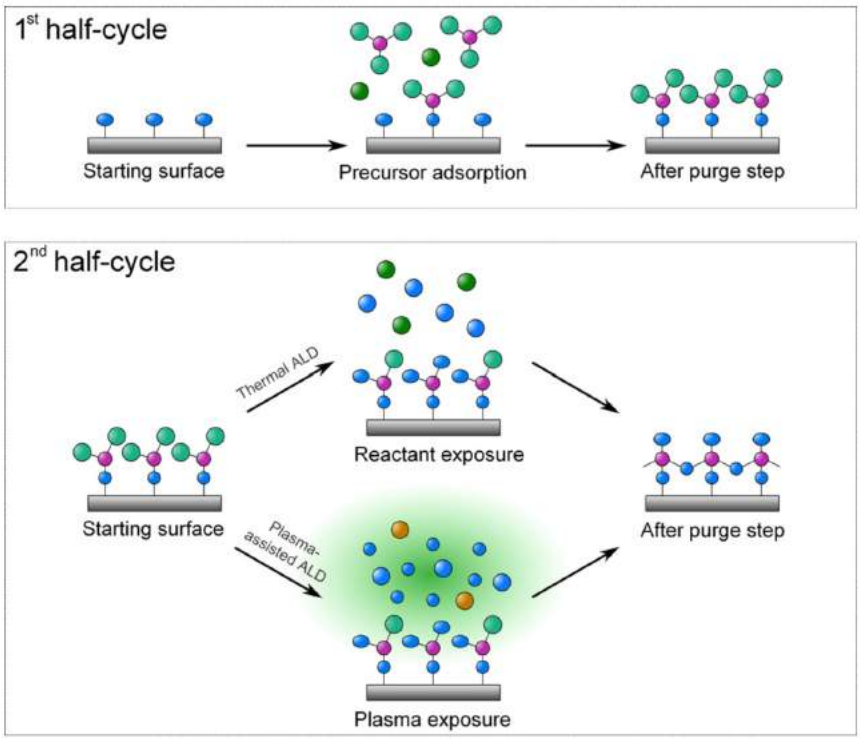


Figure 2.4: ALD and PEALD differ in their second half-cycle; in thermal ALD, precursor and reactant alternately adsorb onto the substrate, while in PEALD, the precursor adsorbs, but the reactant adsorption is replaced with plasma activation of the reactant to complete the reaction cycle [36].

additional parameters (choice of gas, plasma power, plasma pressure) that can be used to tune film properties that are not available in a thermal ALD system.

A photograph of the PEALD system we built is shown in Figure 2.5. Our system is based on a PEALD system pioneered by Prof. Jackson's group at PSU (described in [130] and many other works), and their guidance (particularly from Drs. Israel Ramirez and Yuanyuan Li) during our design process was of immeasurable value. As described in the labels, our PEALD consists of many parts: plasma generation and management, deposition chamber, pressure management, gas delivery (including precursors, oxidants, and gas manifold), and overall deposition automation via computer control. In the following sections, we describe each of these major parts of the system in detail, discussing design choices for each part, and providing relevant background material as needed. Building this deposition sys-

tem was the result of a close collaboration: primary responsibility for design of each of these system components was split between the author (gas delivery, pressure and temperature measurement, system automation, and integration), Dr. Bhadri Visweswaran (plasma generation and management, pump, throttle valve, and exhaust), and Dr. Sushobhan Avasthi (deposition chamber design). Drs. Visweswaran and Avasthi further taught the author many valuable details of high-vacuum system design.

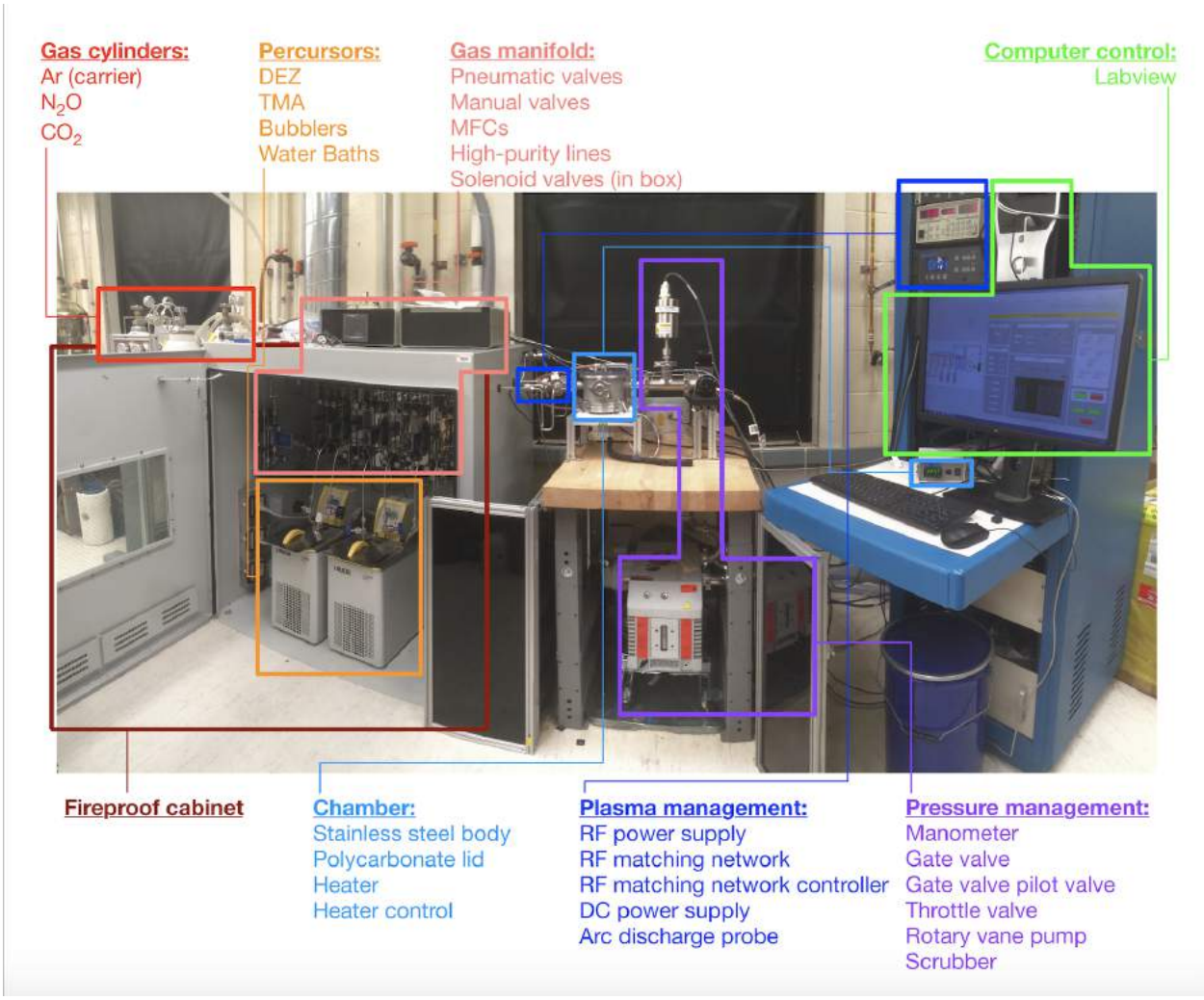


Figure 2.5: Photograph of PEALD built in this work, identifying all major components.

2.1 Plasma

2.1.1 Plasma Basics

Building a plasma-enhanced ALD naturally requires some general familiarity with the basic principles of plasma physics; we attempt a brief summary of information that we found useful during system construction here.

A plasma is a gas that is ionized by a strong electric field. High-energy electrons generated from initial ionization excite other molecules to produce many species within a plasma, including electrons and positively-charged ions, but also neutral plasma radicals and photons. Electrons move through the plasma at a much higher frequency than the larger, heavier ions. As a result, when a plasma comes in contact with a conducting surface (for example, the electrodes, the stainless-steel substrate holder, or the walls of a deposition chamber,) incident electron flux is much higher than incident ion flux. High electron loss at these surfaces results in an accumulation of negative charge with respect to the plasma. The electric field set up by this charge density difference generates a space charge region between the surface and the plasma bulk where electron density is very low and ion density is large (See Figure 2.6, [37]); this region is called the "plasma sheath" because it is visually dark in appearance.

Because the fraction of species that are ionized in the plasma is very low (10^{-6} –10^{-3}), the surface reactions that result from plasma processes are usually driven by the plasma radicals [36]; however, because ions can be accelerated within the plasma sheath, they can still produce surface damage. In low-pressure plasmas, the ion's mean free path can be large, and this acceleration can be significant. At higher pressures, the ions will undergo many collisions within the plasma sheath, and energy of ions incident on the substrate surface will be reduced. Hence, introducing a plasma into an ALD process is a complex business, and chamber/plasma generator geometry, plasma power, pressure, and gas species can all play a role in film quality.

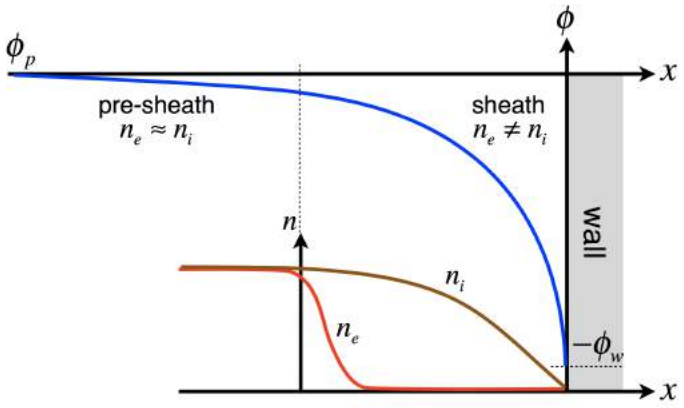


Figure 2.6: Electron density (n_e) and ion density (n_i)are roughly equal with a plasma, but electron density rapidly diminishes close to conducting surfaces, resulting in a"plasma sheath". Plasma potential is higher than the potential of the conducting surface [37].

2.1.2 Types of PEALDs

Many varieties of plasma-enhanced ALD have been previously demonstrated, and each funnels different numbers of radicals and ions to the substrate. Schematics for four methods are shown in Figure 2.7, which we describe briefly below [38]. A thorough review of plasma-ALDs can be found in [36].

In radical-enhanced ALD, a thermal ALD chamber is outfitted with an adjacent plasma source. Because the plasma is some distance from the reaction chamber, plasma species undergo many collisions before reaching the substrate; many ions and electrons recombination on various surfaces. Reactive plasma radicals–typically radicals with the longest lifetime, often the least aggressive radicals – can still reach the substrate in high density so long as tubing and chamber materials are carefully chosen to have low recombination probabilities with the radicals of interest. For example, metal chambers are often a poor choice compared to materials like quartz.

Direct plasma ALDs are effectively modified PECVD chambers, and consist of radio-frequency (generally 13.56 MHz, for practical rather than scientific reasons) parallel-plate-style capacitively-coupled plasmas, where one electrode (typically the grounded electrode)

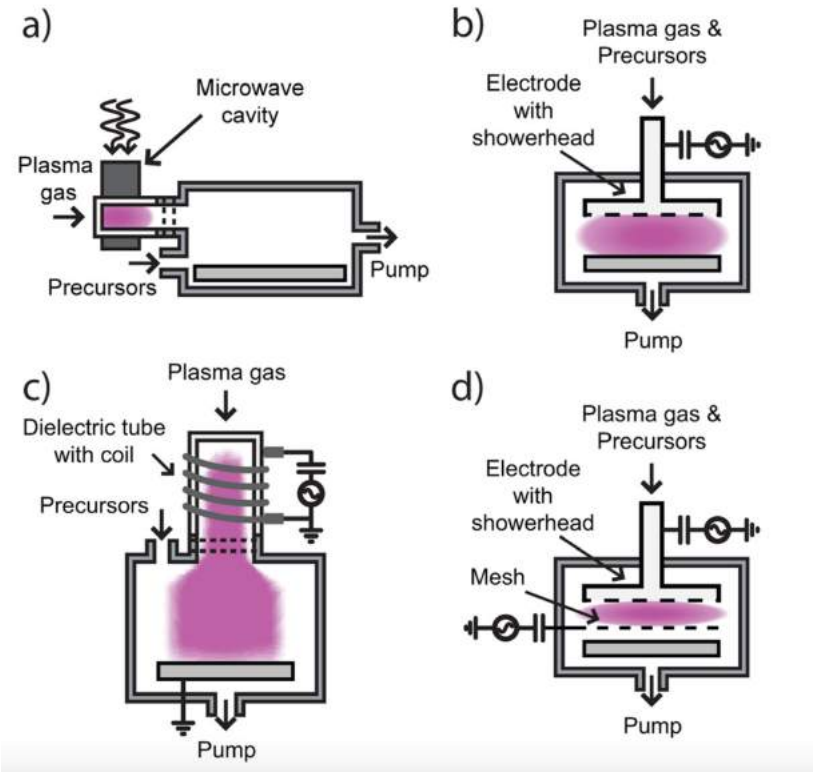


Figure 2.7: Radical-enhanced (a), direct (b), remote (c), and triode (d) plasma ALD configurations [38].

doubles as the substrate holder. Because the substrate is positioned on an electrode, it experiences a high flux of plasma radicals and ions at its surface. While this results in uniform, rapid deposition, the energy of the ions (depending on the plasma's pressure and voltage), and emitted UV radiation can be sufficiently high to induce material damage.

Unlike direct plasma ALD, in remote plasma ALD the substrate holder does not play a role in plasma generation; the most common method is inductive-coupling (ICP), which has been extensively studied and industrialized for etching applications. Because the plasma fills the chamber (as in a direct plasma), the sample experiences a direct flux of ions and electrons, and can achieve higher radical flux than a remote plasma. However, because the substrate is decoupled from the plasma, other factors (such as substrate temperature, etc.) that might cause fluctuations in plasma parameters become far less significant than in a

direct plasma. Remote plasma also reduces the likelihood that aggressive radicals with short lifetimes will reach the substrate,

One interesting hybrid of direct and remote plasmas is a triode system, wherein a perforated metal layer lies between a substrate holder and a capacitively-coupled plasma electrode; the plasma is confined between the top electrode and the mesh, and results in a plasma with some of the advantages of both direct and remote plasmas.

For our system, we use a direct plasma because it is analogous to a PECVD system and because it is straightforward to machine a parallel plate reactor. In this configuration, damage from incident ions is something that can be managed to a degree with low plasma power density and high gas pressure, but for this reason it is possible that a remote plasma or triode-style chamber could confer advantages in a future system design.

2.1.3 Plasma in this System

A schematic showing the components in our plasma generation setup is shown in Figure 2.8. Our plasma is confined between two parallel plate electrodes. The upper electrode is embedded into the insulating chamber lid, and the lower, grounded electrode doubles as the substrate holder. The plasma is generated by an RF (13.56 MHz) power supply, which is fed through a matching network and then to the chamber (power supply, matching network, and matching network controller all supplied by Kurt Lesker, part of a KJLC R-Series package).

The matching network is required because the plasma acts as a combination of capacitors, resistors, and diodes (see Figure 2.9). Since RF generators are designed to deliver power to a 50 Ω load, a matching network, which consists of an inductor and a variable capacitor, serves to dynamically drive the impedance of the system to 50 Ω and thereby minimize reflection of power back to the source. Each matching network is rated to match a particular range of impedances. In our case, the system impedance was at first just barely in range; as a result, the two variable capacitors (called “load” and “tune” capacitors) had to move to extreme

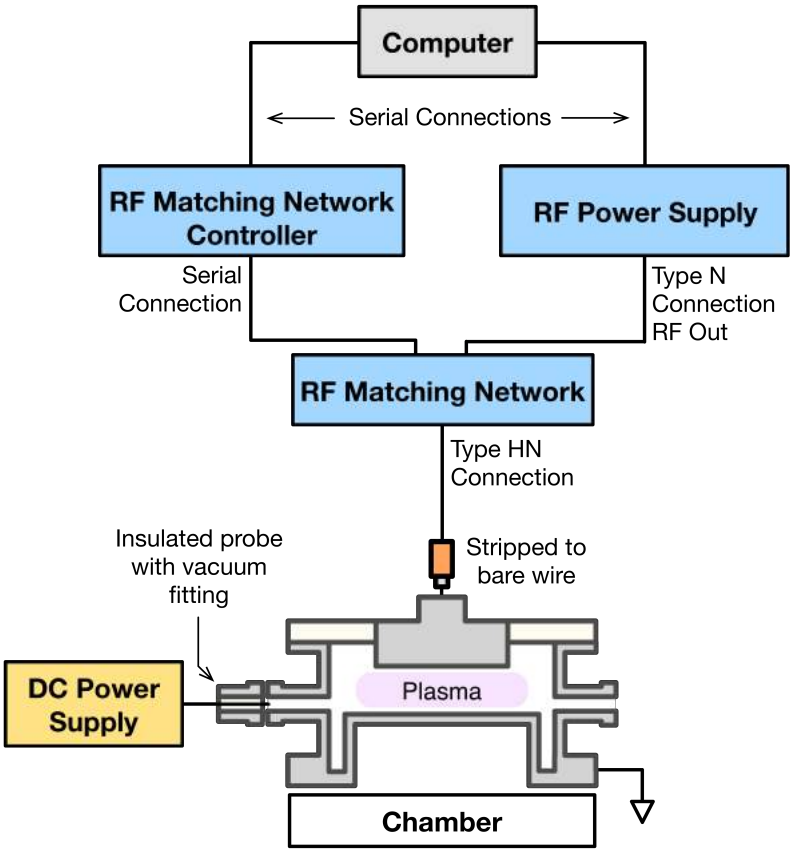


Figure 2.8: RF and DC components used for plasma generation and connections.

positions to provide a suitable match. To increase the range of the matching network, a larger inductance is needed. This can be provided (for minor adjustments) by squeezing together the rings of the spiral inductor inside the matching network. In our case, this minor adjustment provided some benefit, but ultimately Seren IPS replaced the inductor with a larger one. After this replacement, the load and tune capacitors could match the system impedance easily.

In our PEALD, we ionize our oxidizing gases, N_2O and CO_2. We prefer these oxidants to O_2 and H_2O because they are weak oxidants that will not freely-react with the metal-organic precursor. This produces a couple of benefits: 1) the weak oxidant gases are able to double as purge gases, reducing system complexity and increasing throughput, and 2) we are able to minimize parasitic thermal-ALD reactions, both in the deposition lines and on the

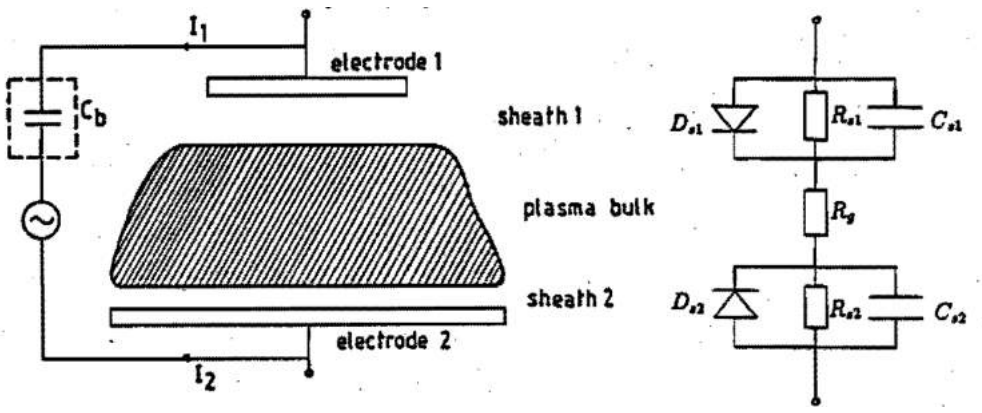


Figure 2.9: An RF capacitively-coupled plasma can be modeled as a combination of resistors, capacitors, and diodes. The resistor R_g represents the plasma glow, the plasma sheaths are represented by a parallel combination of capacitors $C_{s1,2}$, resistors $R_{s1,2}$, and diodes $D_{s1,2}$ – the diodes indicate that the plasma glow has a higher potential than the electrodes [39].

substrate, resulting in a cleaner system and a process that is more responsive to intentional changes. Photographs of N_2O and CO_2 plasmas, taken through the transparent portion of the chamber lid, are shown in Figure 2.10.

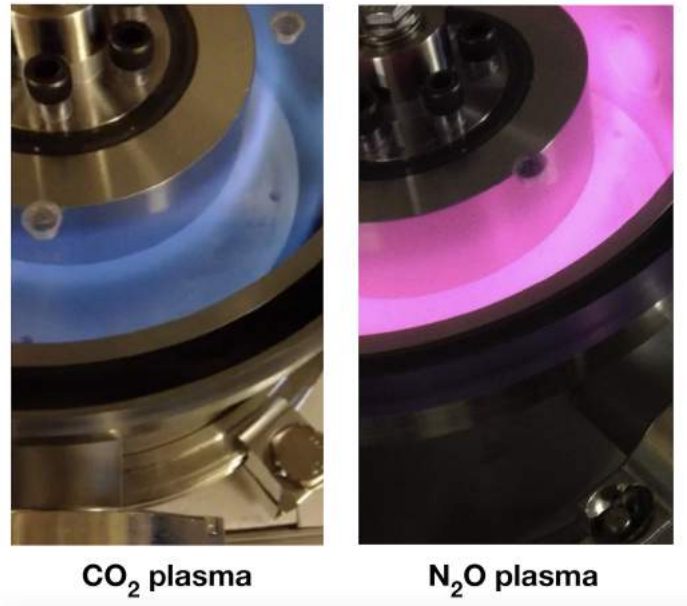


Figure 2.10: Images of CO_2 and N_2O plasmas in our PEALD.

As mentioned, it is important to reduce energy of incident ions in a direct-plasma ALD, especially for ZnO films that readily form oxygen vacancies. Hence, the operating plasma power should be as low as possible. The minimum voltage for parallel-plate plasma ignition depends on the product of the chamber pressure and the plate separation, and typically occurs when this value is $\sim 0.1 - 1$ Torr-cm, depending on the type of gas [40, 131]. This behavior is illustrated in Figure 2.11 for an RF Ar plasma, from [40]. For our plate spacing, 0.1 – 1 Torr-cm corresponds to a chamber pressure of $\sim$ 40 mTorr – 400 mTorr.

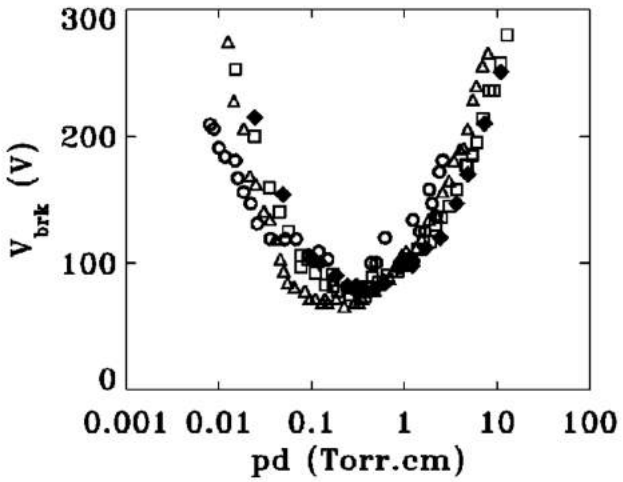


Figure 2.11: Voltage required to initiate plasma (V_{brk}) is a function of the product of pressure in distance *pd*, and obtains a minimum value around the same *pd* value; we see this behavior in this plot, where 2 cm (circles), 5 cm (triangles) and 10 cm (squares) electrode spacings demonstrate very similar breakdown patterns [40].

In practice, the minimum power at which we can reliably strike a plasma is 15 W (power density of 0.1W/cm^2), corresponding to a pressure of 100 mTorr. However, to reduce the possibility of oxygen-deficient ZnO growth ([130]) a deposition pressure of 690–700 mTorr is used in practice; however, with the assistance of a DC electrode "pilot light" for plasma initiation, described below, we can operate at this elevated deposition pressure without further increasing plasma power. We note that operating at this combination of pressure and power (700 mTorr, 15 W) results in a visibly dimmer plasma than when operating at 100 mTorr and 15 W.

In our system, many deposition cycles are required to build up a film of appreciable thickness. In each cycle, the plasma duration is kept short with the aforementioned goal of minimizing ion damage. However, because the matching network adjusts its values using servo motors to physically move plates in variable capacitors, response time is relatively slow ($\sim$ 1 s – although this can be adjusted to some degree by performing phase and magnitude calibration, as stated in the tool manuals). Furthermore, the impedance of the initial gas differs from the impedance of the ultimate plasma – so, one set of matching network values is optimal for plasma ignition, while a different set of values is best for plasma maintenance. In a PECVD system where a plasma would be continuously on for tens of minutes, this adjustment would occur in just a few seconds and would therefore be insignificant compared to the length of the deposition. In our rapidly switching ALD system that has many cycles lasting only a few seconds each, this matching time becomes a concern. In particular, if the matching network parameters needed for steady state maintenance are far from the parameters for plasma ignition, the matching network will have to constantly readjust and oscillate between these two sets of optimal values, making deposition cycles lengthy and possibly inconsistent. To mitigate this problem, an electrode connected to a DC high-voltage (10 kV) power supply (Stanford Research Systems PS300 Series) is introduced in the chamber far from the substrate (to minimize deposition on the probe), where it serves as a source for electrons by producing an arc discharge. Including this high-voltage source dramatically shortens plasma ignition time and consistency, and hence cycle time. The DC discharge components used are also shown in the schematic in Figure 2.8. A photograph showing the exterior connections for the DC and RF plasmas is shown in Figure 2.12.

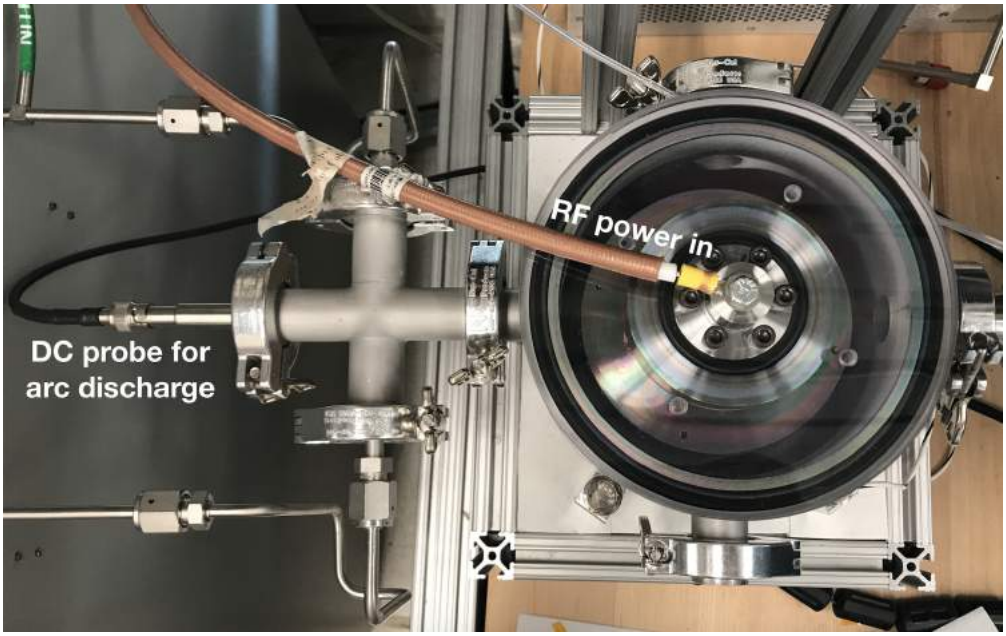


Figure 2.12: Electrode for DC discharge probe and RF power input to chamber.

2.2 Chamber

2.2.1 Types of Deposition Chambers

Chamber design plays an important role in the 1) interaction between the gases and the substrate and 2) ALD cycle duration. Design includes chamber type, heating, and geometry.

There are three common types of single-sample ALD chamber designs – cross-flow, single-hole top-injection, and multi-hole top-injection (see Figure 2.13) [32, 41].

In a cross-flow chamber, precursors and gases are introduced through one port of the chamber (gas inlet) and forced laterally across the sample towards the exhaust line (gas outlet). The chamber height is narrow, and the lateral chamber size is slightly larger than the sample; this ensures that flow is convective and gases are transported rapidly (e.g., in 0.1 s) across the chamber. A drawback to a cross-flow design is that portions of the sample closer to the inlet will be exposed to fresh precursor and oxidant, while areas closer to the outlet will be exposed to gases that have been partially depleted, which can result in film nonuniformities.

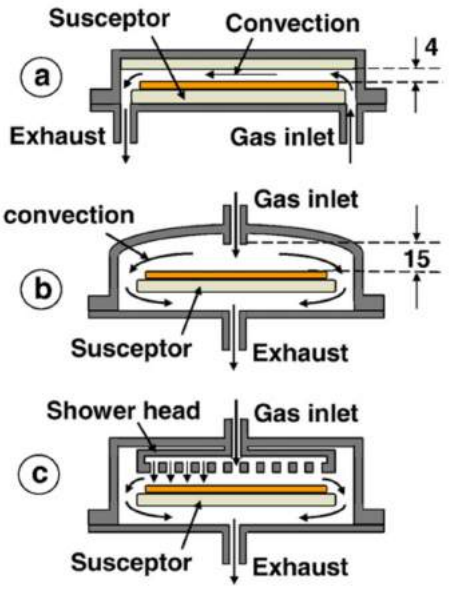


Figure 2.13: Chamber designs include (a) cross-flow (b) single-hole top-injection, and (c) multi-hole top-injection [41].

Top-injection chambers aim to avoid this scenario by exposing the whole surface of the sample simultaneously to fresh precursor and oxidant. Top-injection can be either single-hole, where the gas inlet is above the sample and the exhaust is below, or multi-hole (also called "shower head"), where the gas inlet is above the sample, but it is filtered through a large, perforated nozzle that diffuses the gas evenly over the substrate area. Because the gas outlet is underneath the sample and the gas flows through a very non-uniform cross section, the drawback of this approach is that transport is often diffusive, and purge times are much longer than in the cross flow design. From a practical perspective, a showerhead design may also require more aggressive and frequent cleaning, as narrow openings in the nozzle can easily clog with accumulated layers of deposited film.

In addition to chamber type, heating is another import component of chamber design. When hot-walled, all surfaces are heated; when cold-walled, only the substrate is heated. Cold-walled chambers result in more condensation and deposition on chamber surfaces compared to hot-walled systems.

Lastly, chamber geometries must be considered. Since we use a direct plasma, some features of chamber geometry will determine plasma characteristics– for example, electrode spacing, separation from the walls, and electrode size. Electrode spacing is typically made to be a few hundred times the mean free path, so electrons undergo many collisions to activate neutral gas molecules. Electrode size should be larger than the sample size to reduce edge effects. If the driven electrode is the top electrode and the substrate holder (and in fact, the bulk of the chamber) is the grounded electrode, the spacing from the driven electrode to the walls is important. If this spacing is kept larger than the inter-electrode spacing, the plasma can be confined mostly between the substrate and the top electrode. One final general consideration for chamber geometry is to keep the overall system volume as small as possible, such that pump-out times can be kept short.

2.2.2 Our Deposition Chamber

Diagrams and photos of the chamber we built can be seen in Figures 2.14 and 2.15. Full CAD renderings of the design with all dimensions specified can be found in Appendix A.

Because we have a direct plasma ALD with a capacitive discharge, it is most straightforward to build a cross-flow style chamber such that the top of the chamber can be reserved for the top electrode. Other groups have worked to implement a shower head design, but no significant difference in TFT performance was realized [132]. Because we use 3" square glass samples, the top electrode is 3.5" in diameter. The top electrode is embedded in an insulating polycarbonate lid (an inexpensive and effective alternative to glass) with an O-ring and several screws. The physical gap (in the z-direction) between the substrate holder and the top electrode is 1" – hence, the difference between the top electrode outer radius and the chamber inner radius (chamber wall) is $>$ 1" (1.167"). The chamber and top electrode are manufactured from 304L stainless steel. The chamber ports and fittings are all quick-connector type for easy assembly and disassembly during cleaning. The RF signal is input to the chamber using a stripped type HN cable that is fitted with a crimp-on spade connector

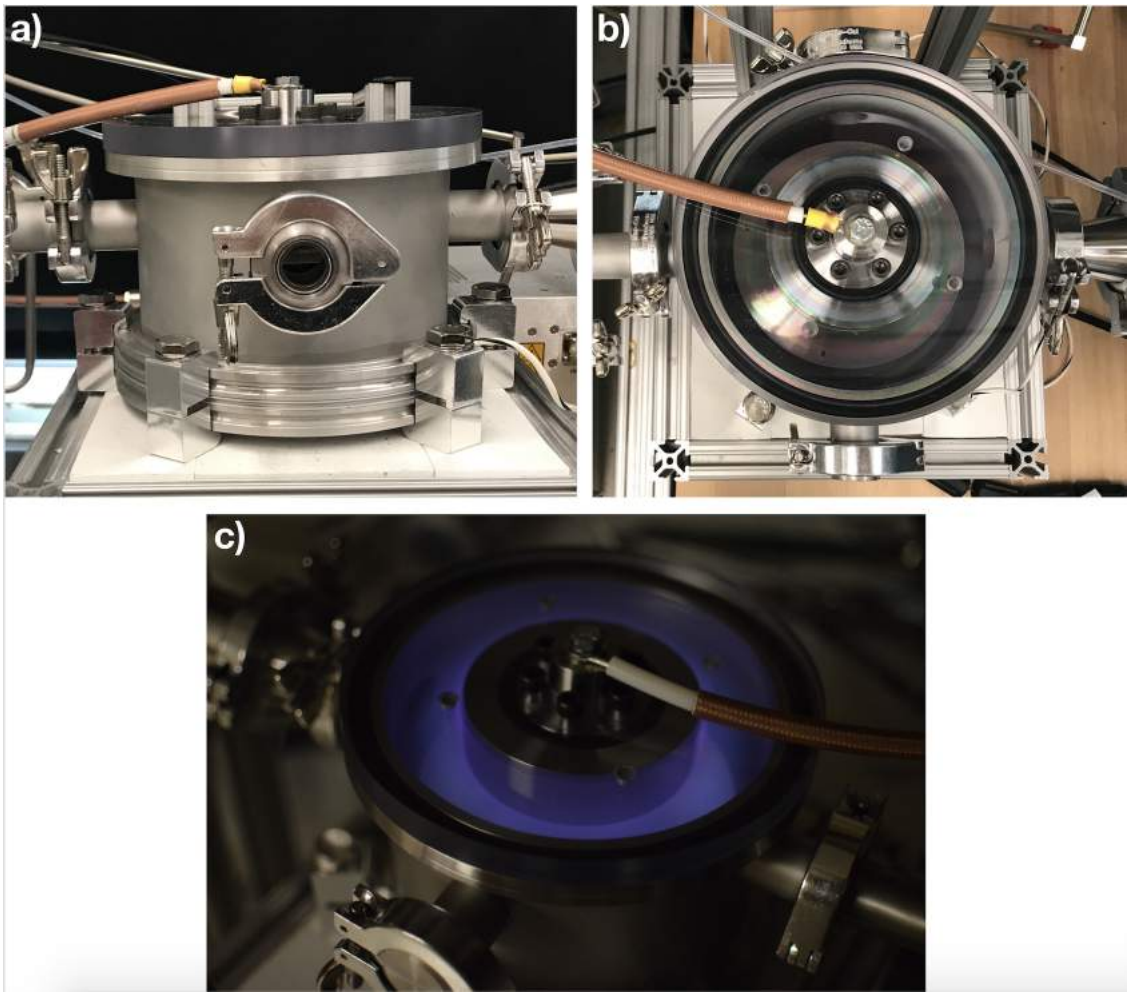


Figure 2.14: Side (a), top (b), and three-quarters view of our deposition chamber (c).

and clamped to the chamber lid so that it can be removed easily, and a braided wire is used to ground the chamber body. The chamber was custom-fabricated by A&N Corporation.

In order to avoid condensation of multilayers on the substrate, we heat the substrate holder externally, using a ring heater (Omega A-series ring heater) that is mounted beneath the outside surface of the sample holder and fastened with clips. We mount it externally to simplify construction and cleaning. In order to 1) facilitate more efficient substrate heating and 2) avoid heating the whole chamber (particularly the polycarbonate lid), we try to thermally isolate the substrate holder. To do this, we take advantage of the poor conductivity of stainless steel, making the thickness of the chamber wall connecting the substrate holder

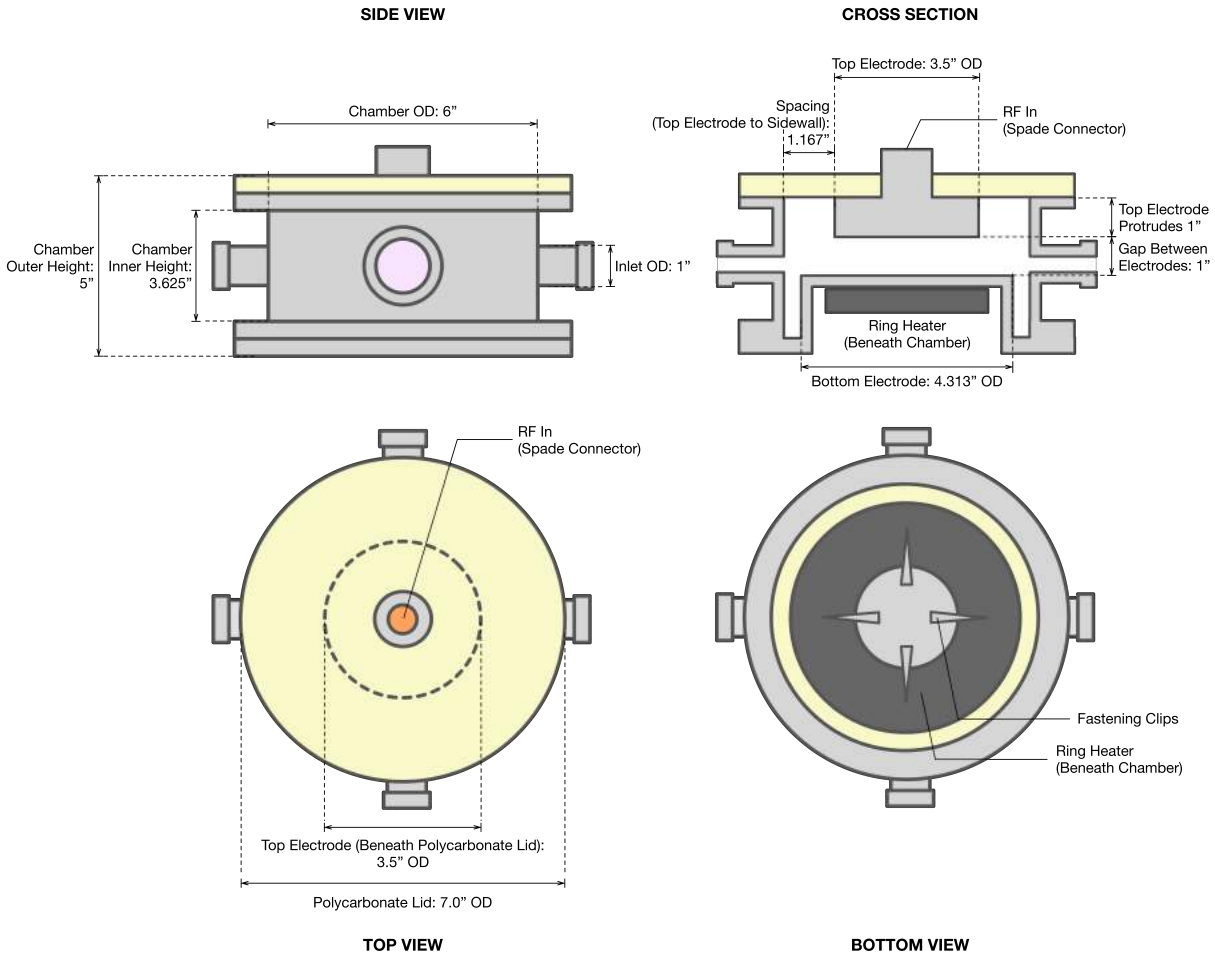


Figure 2.15: Schematic drawings of chamber (not to scale).

to the rest of the chamber narrow (0.065”). The heater is computer controlled via a PID controller (also from Omega). Because the heater control cable is unshielded, we cover the cable with commercially available clamp-on ferrite cores to isolate it from the nearby RF power lines; without the ferrite cores, the displayed temperature value rises rapidly when plasma is struck in the chamber.

2.3 Gas Delivery

As stated, many gases must be delivered to the chamber. These include 1) metal organic precursors diethylzinc (DEZ) and trimethylaluminum (TMA) (which are stored in liquid

form) and 2) the weak oxidant gases (N_2O and CO_2). A diagram showing the dosing of gases into the chamber and qualitative chamber pressure changes is provided in Figure 2.16. Schematics showing step-by-step ZnO and Al_2O_3 deposition processes are also provided in Figure 2.17.

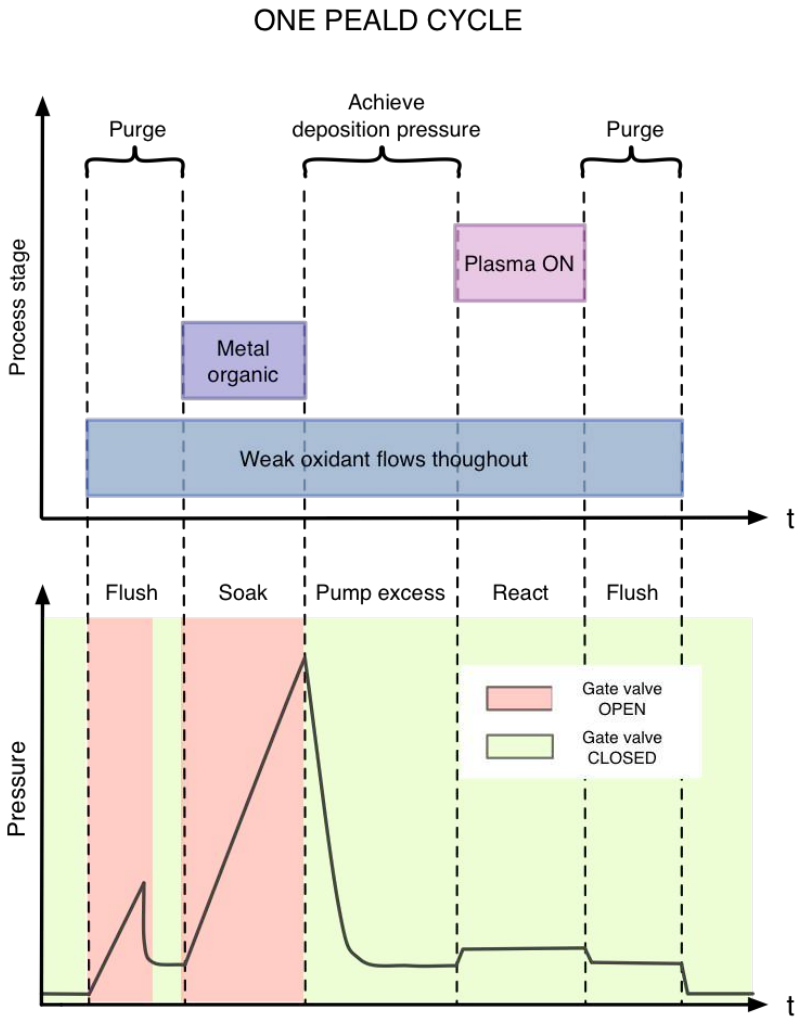


Figure 2.16: Schematic showing PEALD deposition phases and qualitative pressure changes throughout one deposition cycle.

Because the weak oxidant gases can double as purge gases, they are always flowing: they flush the chamber before the reaction, they flow while metal organic adsorbs, they form the plasma, and they flush byproducts out at cycle completion. Their flow rate (100 sccm) is controlled by MKS mass flow controllers. As a result of constant flow, the background

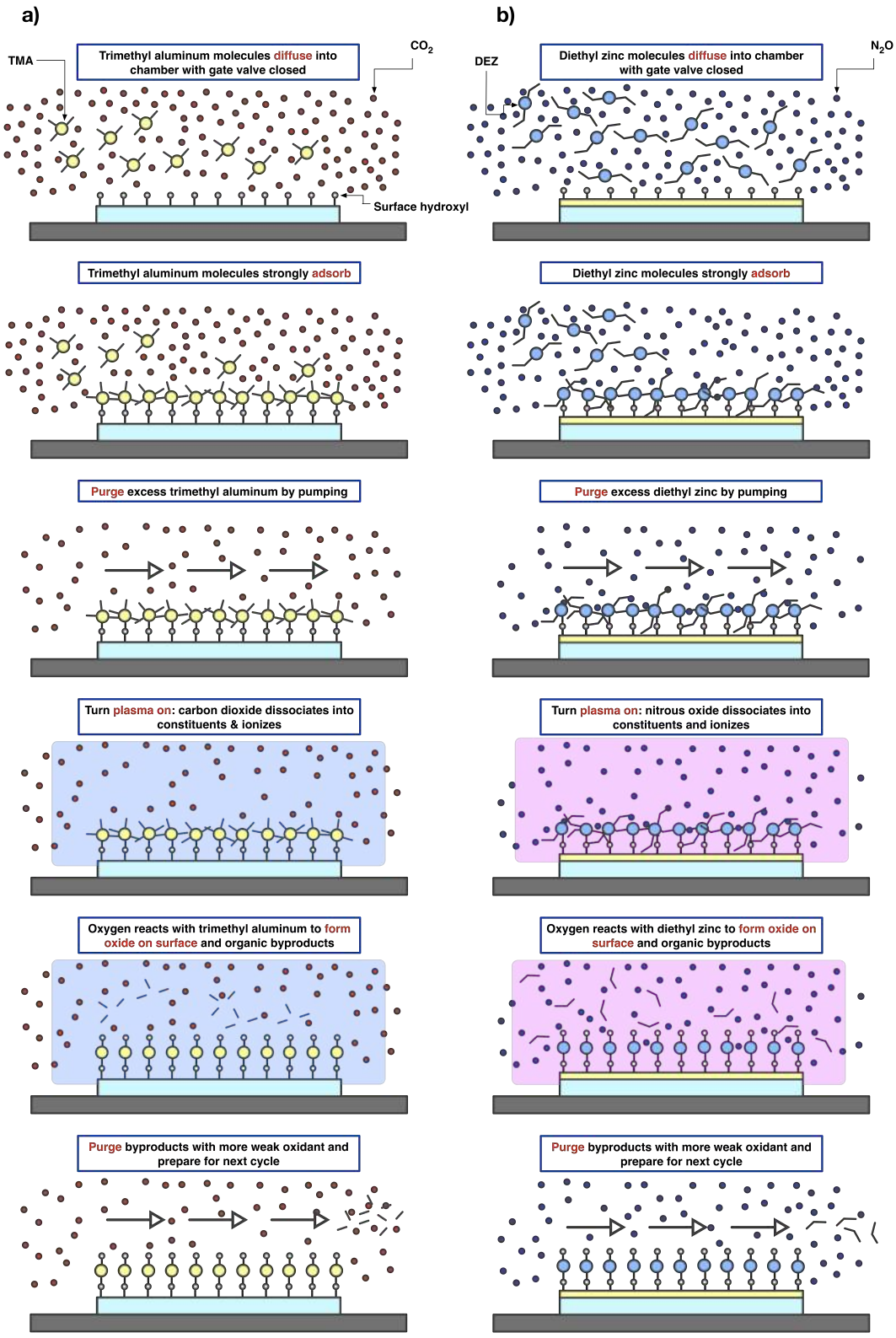


Figure 2.17: Schematic showing PEALD cycle from a layer-growth perspective for (a) Al_2O_3 (b) ZnO.

pressure in the chamber is always relatively high – 690 – 700 mTorr, but up to $\sim$ 6 Torr during soak periods where the gate valve is closed.

Metal organic precursor vapor must also be delivered to the chamber. The vapor pressures of TMA and DEZ at 20°C are about 9 and 12 Torr, respectively. Because this vapor pressure is higher than the chamber pressure, the precursor could be delivered by directly pumping precursor. However, this would result in 1) poor control of precursor delivery that would depend entirely on valve timing and 2) inefficient utilization of precursor, since only very small amounts are required for each cycle in which a monolayer or less of material is deposited.

To avoid these problems, we used a simple "fixed-volume" dosing scheme in which a small volume of tubing bounded on both sides by pneumatic valves is filled with precursor vapor and stored until it is dosed into the chamber once per deposition cycle [130]. A depiction of the fixed-volume process is shown in Figure 2.18.

The fixed-volume precursor delivery is further improved by storing liquid precursor in a bubbler. In a bubbler cylinder, a high-pressure carrier gas is introduced through a tube that extends to the bottom of the container. In our case, we choose Ar as the carrier gas because it is an inert gas that will not react with liquid precursor or impact oxidation in the chamber. The carrier gas bubbles through the volume of the liquid, saturating with precursor vapor, and releases a high-pressure mixture of carrier and precursor gases at the bubbler's outlet. Using a bubbler serves two purposes. First, because the carrier gas bubbles through the full volume of the liquid, it increases the effective surface area of the precursor liquid (e.g. equilibrium vapor pressure is achieved in every single bubble). For this reason, more precursor can be delivered to the chamber compared to relying on the vapor at the surface of the liquid alone. Second, the high-pressure carrier gas pressurizes all the gas in the cylinder – hence, the stored fixed volume of mixed carrier/precursor gas can be delivered much more rapidly to the deposition chamber than if it were just gaseous precursor at its vapor pressure (e.g, the Ar we use is at 25 psi/1293 Torr, more than 100$\times$ higher than the TMA/DEZ vapor pressure). This in turn reduces cycle duration by reducing the length of the soak

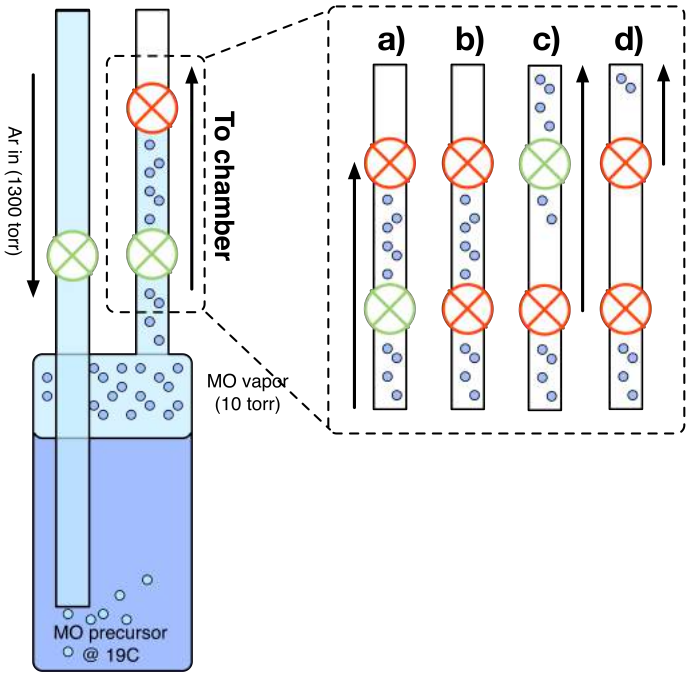


Figure 2.18: A fixed volume downstream of the metal-organic bubbler is cyclically filled and emptied of precursor by two pneumatic valves; one normally open (green) and one normally closed (red). The inset shows the cycle: a) the valves are in their default positions, and the fixed volume is full of precursor; b) the lower valve is closed, defining the fixed volume to be delivered; c) the upper valve is opened and precursor diffuses to the chamber; d) the volume is emptied, and the upper valve is closed before proceeding again to default state (a).

phase. In order to ensure consistency in this process, the vapor pressure of the precursor must be constant – hence, the bubblers are contained within temperature-controlled (0.1°C resolution) water baths set to 19°C. A photograph of the bubbler and the water bath can be seen in Figure 2.19.

Additionally, this method requires the system to be slightly heated to mitigate precursor condensation; because the baths generate large quantities of heat and the manifold is fully enclosed in a fireproof cabinet, the system is heated by default and additional heating tape is not needed.

To determine the desired value of fixed volume, we use values from literature to approximate the area occupied by each metal-organic molecule, calculate the number of moles of precursor required to coat the full surface area of the chamber, and use the ideal gas law

Figure 2.19: Bubbler cylinder for liquid precursor storage, immersed in circulating temperature-controlled water bath.

to identify the appropriate volume of 1/4" OD tubing [133, 134]. To provide a generous margin (allowing for non-idealities like multilayer coating etc.), we multiply this number by 10, yielding 1.8" for TMA and 3.7" for DEZ. Because of constraints in the fabrication process, the minimum separation between the two valves defining the fixed volume was 4.6"; for simplicity of fabrication a larger spacing was ultimately employed (6.34"). A table with parameters used for this calculation is provided in Table 2.1.

Table 2.1: Parameters for determining length of tubing needed in fixed-volume dosing.

Chamber surface area	1230 cm^2
TMA area	0.25 nm^2/molecule
DEZ area	0.12 nm^2/molecule
Argon pressure	1.68 atm
Temperature	292°K

A schematic of the overall gas manifold can be seen in Figure 2.20. An important feature of the design is redundancy – should any of the pneumatic valves cease to function, the manifold has been designed with many back-up manual valves that can isolate parts of the system from each other and minimize exposure of the manifold lines to atmospheric contaminants during a valve replacement. This serves the additional function of isolating manifold areas for leak-checking. Furthermore, VCR connections (rather than purely welded connections) enable some degree of modularity and user-end repair.

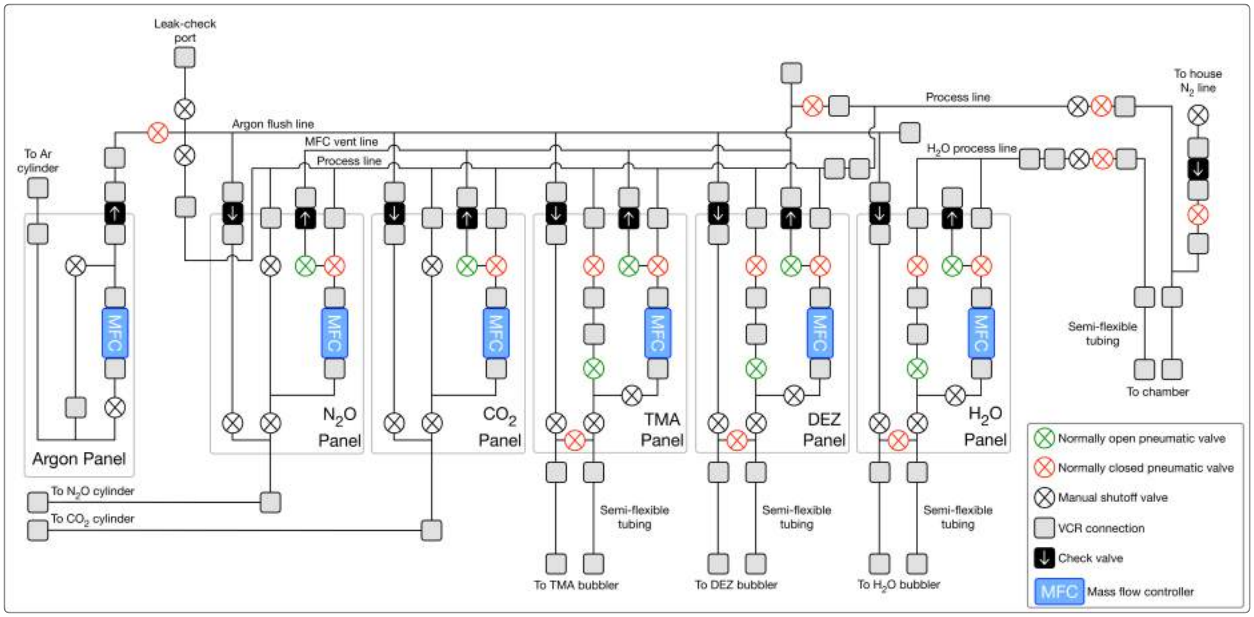


Figure 2.20: Schematic showing gas manifold design.

As seen in Figure 2.20 and also in a close-up of the precursor panel shown in Figure 2.21, there are three panels for precursor delivery – one for TMA, one for DEZ, and a third one intended for H_2O. This third panel enables the system to perform thermal ALD using water as a strong reactant. Its lines are kept separate from the main process line in order to prevent unintended oxide deposition in the process line. While in this work we largely do not use this panel, because it is isolated from the rest of the manifold, it could be adapted in the future for any other kind of liquid precursor that could contaminate the main process line.

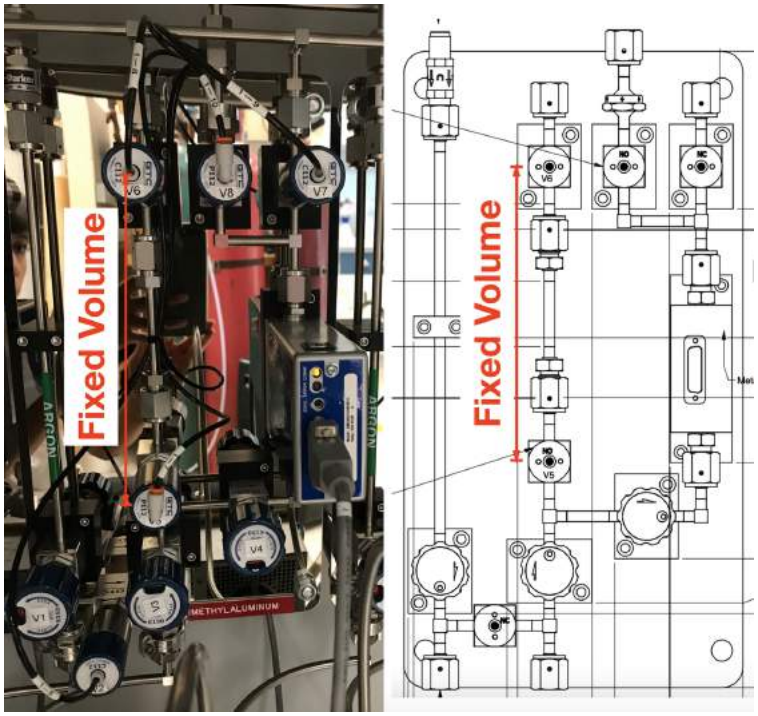


Figure 2.21: Photograph and CAD diagram of precursor panel.

Note also that in each precursor manifold, there is an argon inlet (for the bubbler), a fixed volume line (for fixed-volume dosing), and also a third line outfitted with a mass-flow controller. The MFC is not used in this work, but could allow the manifold to be used for a PECVD and is included for higher system modularity in future experiments.

Note also that each pneumatic valve is actuated by its own solenoid valve, which directs the flow of regulated house compressed air at 90 psig (housed in a box on top of the gas cabinet); the solenoid valves are all computer-controlled via Labview.

Before connecting the gas manifold to the rest of the system, each valve and VCR connection was leak-checked to ensure no damage during shipment; a base leak rate of 3 – 4 $\times 10^{-10} atm - cc/sec$ was measured.

2.4 Pressure Control and Exhaust

In order to perform the ALD cycle, measurement and control of the chamber pressure is required. To accomplish this in our system, we use a mechanical pump, a pneumatic gate valve, a manual throttle valve, a capacitive manometer, and a molecular sieve. A schematic showing these parts in shown in Figure 2.22.

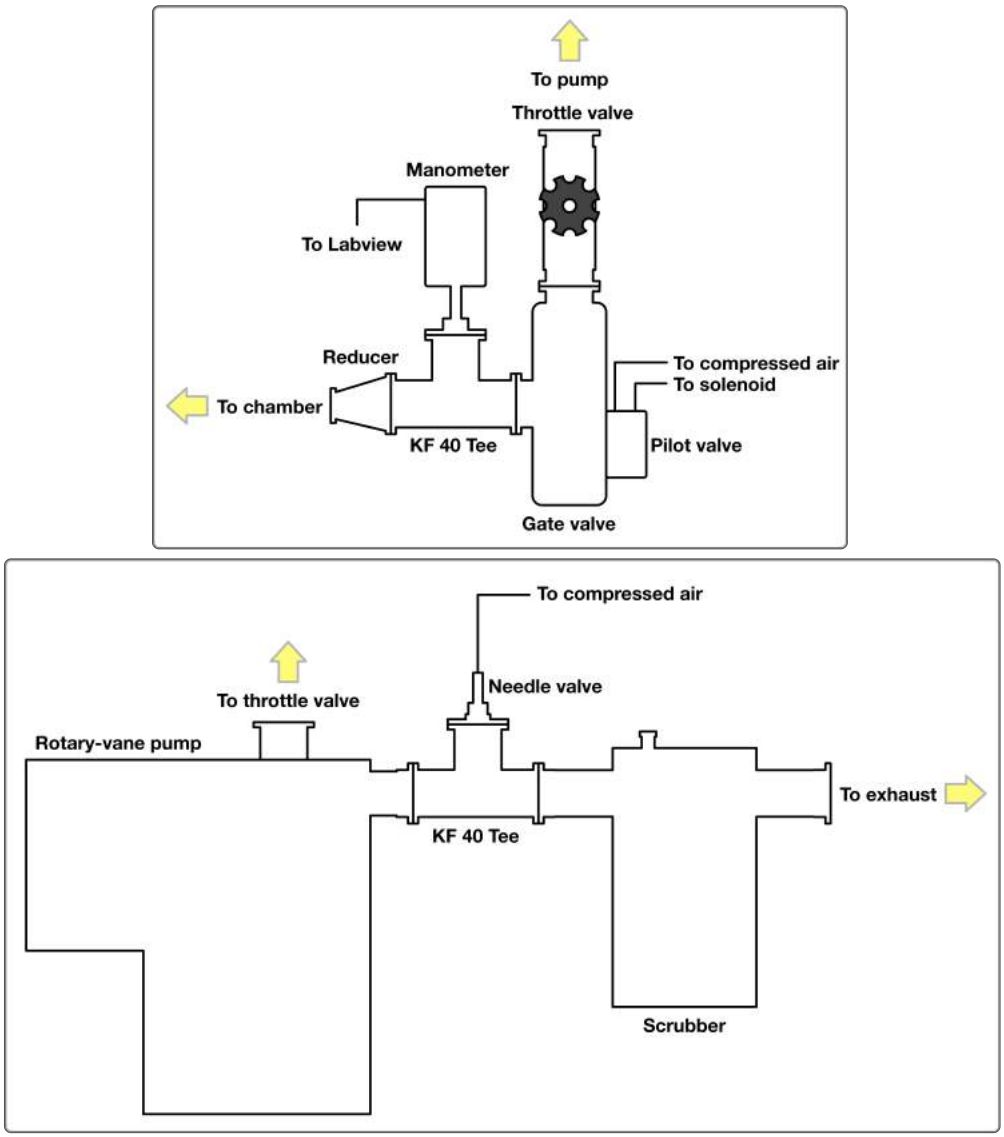


Figure 2.22: Schematic showing pressure management system design.

Chamber pressure is measured with a capacitive manometer (MKS 631C) that is placed at the chamber outlet, just before the gate valve. The sensor in this device contains a diaphragm. One side of the diaphragm is evacuated to much higher vacuum than the pressure measurement range; a getter helps maintain this low pressure over the life of the manometer. The manometer measures pressure by measuring changes in capacitance between the diaphragm and and an adjacent electrode. To prevent oxide deposition on the surface of the sensing element, we use a heated manometer (heated to 200°C).

Chamber pressure is modulated using both a high-cycle, spring-return, pneumatically-actuated, normally-closed gate valve (HCV-40-AK-CLV NW) and an inline, LowPro single-stage manual throttle valve (LPV1-40-IK-MNVS), both KF-40 sized from MKS. The throttle valve's position is set by a manual knob, and restricts pumping power. This is how we set the deposition pressure for the system. In a future implementation, a more-sophisticated butterfly valve could be used instead to provide dynamic pressure control.

The high-cycle gate valve can tolerate 10 million cycles – this is important as every deposition cycle requires a gate valve cycle, and each deposition requires $\sim 40 - 300$ cycles, depending on thickness. Initially, the gate valve was actuated by the same type of solenoid valve used for the small pneumatic valves in the gas manifold. However, this resulted in very slow actuation (~ 1 sec) and led to needlessly long cycle times. This slow actuation resulted from the large (KF-40) size of the gate valve, as a large volume must be displaced to actuate it; the solenoid valves flow rate is relatively low, so the gate valves actuates slowly when actuated directly by the solenoid. To address this, a "pilot valve" is used (3 Way In-Line Pilot Air Control Valve from Grainger), which has a small valve flow coefficient (C_v) similar the pneumatic valves in the gas manifold, and hence can be actuated easily by the computer-controlled solenoid valve. At the same time, the pilot valve can support a much larger flow rate, and directly supplies compressed air to the gate valve, resulting in $10\times$ faster actuation (e.g., 3 second open/close time can be shorted to a couple hundred milliseconds). A photo of the gate valve, throttle valve, and pilot valve can be seen in Figure 2.23.

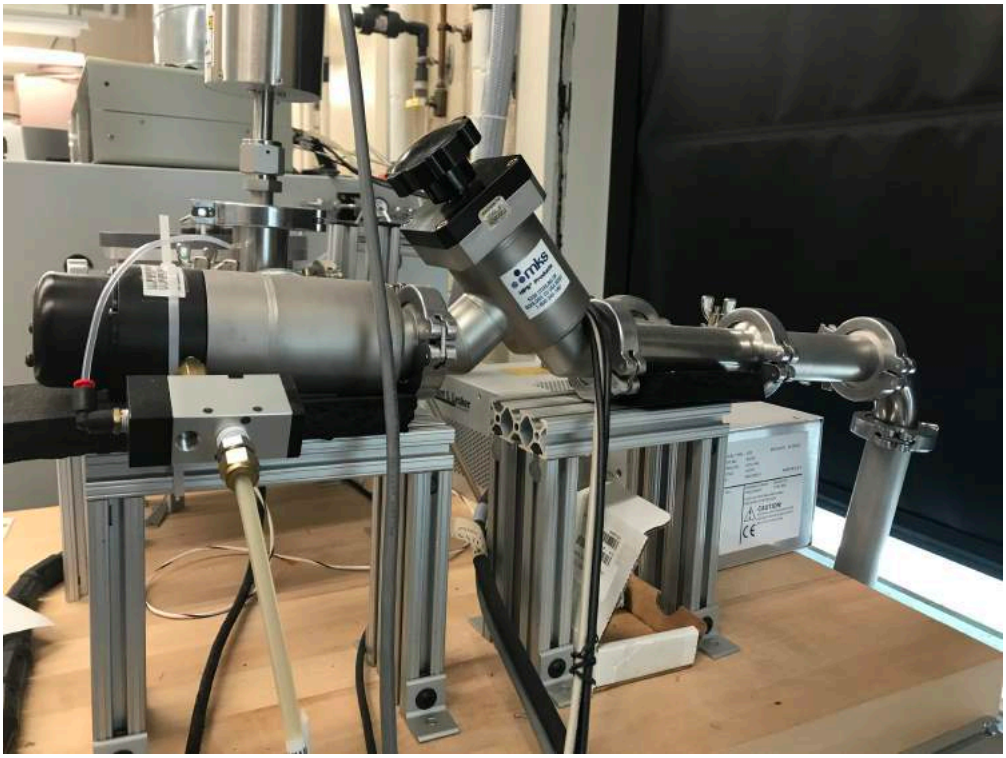


Figure 2.23: Gate valve attached to pilot valve and manual throttle valve. Manometer visible in background; pump beneath table.

The system is pumped by an oil-sealed two-stage rotary vane vacuum pump (Leybold TRIVAC 40 D BCS), which can achieve ultimate pressures below 10^{-4} mbar and operate in aggressive and corrosive environments. It operates using fomblin perfluoropolyether (PFPE) oil, which is inert and nonflammable – this leads to long oil lifetime, reduces the chance of fire, and allows us to place the scrubber after the pump.

The last physical component of the PEALD system is the scrubber, which eliminates chemical waste from the exhaust line. The scrubber consists of a molecular sieve (MDC Vacuum Products) that contains many small pebbles and hence has a high internal surface area. We use a needle valve to bleed a small amount of compressed air into the molecular sieve. Hence, if any of our highly pyrophoric precursor exits the deposition chamber without having reacted, it will react with compressed air in the scrubber, eliminating the possibility of a fire in the exhaust.

2.5 Computer Control

Labview was used to program all equipment in the PEALD (all valves in manifold, gate valve, manometer reading, temperature reading, RF power supple and matching network) via serial interfaces. Processes are fully automated, but users can easily input desired timings for plasma power, temperature, soak times, plasma durations, and pump out times. A picture of the user interface can be seen in Figure 2.24. Images of code I wrote can be found in Appendix A.

Figure 2.24: PEALD control station showing Labview interface.

In addition to automating processes, the Labview program also provides failsafes for several likely scenarios that are either harmful to the system or physically dangerous. In particular, the program prevents:

- Venting the chamber during a process run, which would release pyrophoric process gases to the air,
- Running a process without pumping the chamber, which would contaminate the gas manifold with atmospheric constituents, and
- Leaving valves open in the event a process is aborted.

2.6 Section Conclusion

In this section, we introduced ALD as a material deposition method, and motivated the used of PEALD for high-density, conformal thin-film growth at plastic-compatible temperatures required in LAE systems. We then described both the design process for building a PEALD, informed by an understanding of plasmas and chamber designs in deposition systems. Lastly, we provided construction details for all elements of the PEALD used throughout the remainder of this work. We will refer to the system design in the following section, where we discuss film growth and characterization and TFT development, both of which exhibit dependence on plasma parameters and cycle timing.

Chapter 3

Material and TFT Validation, Development, and Characterization

In this chapter, we use the PEALD system described in the prior chapter to grow and characterize films of zinc oxide and aluminum oxide, and to build different kinds of thin-film transistors that use zinc oxide as an active semiconducting layer and aluminum oxide as insulating and passivating layers. The results in this chapter were made possible because of training from other students; in particular, Warren Rieutort-Louis and Josh Sanz-Robinson together trained the author to build and characterize amorphous silicon TFTs, which helped form a basic skill set that could be extended to oxide TFTs; Sushobhan Avasthi trained the author to use the Edwards thermal evaporator and the cleanroom measurement and characterization tools; Christine Pappas trained the author to spin-cast thin polyimide films. Section 3.5.2 presents results from collaboration with undergraduate Jenny Tang, who defined strain limitations on ZnO TFTs on free-standing plastic as part of her thesis work. Some of the results from Sections 3.4.3, 3.3.3, and 3.5 were presented by the author at the International Thin Film Transistor Conference and the Society for Information Display Symposium [135–137]. Results in Section 3.5 were also published in the Journal of the Society for Information display [44].

3.1 Deposition, Material Assessment, and Etching

3.1.1 Deposition Recipe Development

After PEALD construction, recipes for growth of ZnO and Al_2O_3 were developed, where times for the various cycles stages, deposition pressures, and plasma power were tuned. The cycles stages include:

1. Flush chamber prior to deposition, once per deposition (open weak oxidant valve, close gate valve for soak, open gate valve for purge)
2. Soak metal-organic (close gate valve, then open and close MO top valve)
3. Purge excess metal-organic and achieve stable deposition pressure (open gate valve, wait for stable manometer reading)
4. Ignite and run plasma (turn RF power on and off)
5. Purge reaction byproducts (keep gate valve open after reaction)
6. Purge chamber post-deposition, once per deposition (ensure thorough purge of pyrophoric residual gas before venting to atmosphere)

To begin, long cycles stages (many seconds) were chosen to ensure each phase reached completion. While this results in undesirably long depositions, if cycles stage times are too short, many problems can arise. Examples of these problems can be found in Table 3.1. Initial stage timing is provided in the left-hand column of Table 3.2.

Table 3.1: Consequences of PEALD stages being too short in duration

Short PEALD Stage	**Undesirable Result**
Initial chamber flush	High background H_2O level in chamber: parasitic ALD reactions and increased film hydrogen content

(Continued on next page)

Table 3.1: (continued)

Short PEALD Stage	**Undesirable Result**
Metal-organic soak	Metal organic (in viscous flow) doesn't have time to reach chamber through narrow 1/4" OD tubes
Metal-organic purge	Residual metal organic in chamber; parasitic PECVD-type reactions
Plasma time	Reduced film growth rates
Post-reaction purge	Films contaminated by organic reaction byproducts
Post-deposition purge	Unreacted precursor in chamber exposed to air can result in fire

Once stable film deposition was observed, cycles stages were modified to improve device performance. In some cycle phases, a shorter duration is beneficial – e.g., for ZnO in TFTs, shorter plasma duration is preferred to longer plasma duration, which will be discussed in section 3.3. However, other cycle phases benefitted from increased duration; in particular, the post-reaction purge time and the metal-organic purge time were increased from 4 to 5 seconds for the reasons listed above. As mentioned, for ZnO growth, the metal organic precursor used was diethylzinc (DEZ) and the weak oxidant was nitrous oxide (N_2O). For Al_2O_3, the precursor used was trimethylaluminum (TMA) and the weak oxidant used was carbon dioxide (CO_2).

Aside from cycle timing, one additional pre-deposition step significantly enhanced device performance at the expense of cycle duration: a pre-deposition cyclic CO_2 purge after samples were placed in the chamber initially (CO_2 flow rate of 200 sccm, soak 5 s, purge 5 s, repeat 30×; N_2O would be appropriate to flush prior to ZnO deposition). We expect this helped to dilute and remove atmospheric H_2O from the chamber, reducing ALD-type growth. Initial and ultimate film cycle stage durations for both ZnO and Al_2O_3 are provided in Table 3.2; we believe there is still room for cycle timing optimization.

Table 3.2: Timing for all stages of PEALD cycle

Cycle stage	**Initial Duration**	**Ultimate Duration**
Pre-deposition flush	4 s	5 s
MO soak	5 s	5 s
MO purge	4 s	5 s
Plasma on	7 s	2.5 s
Post-reaction purge	4 s	5 s
Final chamber purge	20 s	120 s

Plasma behavior for N_2O and CO_2 was initially evaluated prior to film growth. In general, plasmas could ignite at lower power when chamber pressure was lower; this is expected, because high chamber pressures reduce particle mean free path, reducing the maximum acceleration of ionizing electrons. For a given plasma power (15 – 25 W), plasma can be maintained within a pressure window of 70 – 700 mTorr. Plasma brightness increases significantly as pressure is reduced, until the plasma becomes unstable and extinguishes at 30 mTorr. The increased plasma brightness at low pressure indicates an increased rate of photon generation from ionization and excitation events. Figure 3.1 summarizes these observations.

As mentioned, both high plasma power density and low plasma pressure play a role in ion damage, which we seek to minimize in our materials. It remains unclear which factor is most important on its own. We choose to operate at a relatively high pressure of 650 – 700 mTorr because we wish to increase the concentration of oxidants in during the PEALD reaction. Having decided upon this, the plasma power is then set to be the minimum power required to ignite plasma at this pressure (15 – 25 W). Because a plasma power of 15 W results in the best quality TFTs, this power is recommended; as mentioned, this power can consistently strike plasma in the presence of a DC arc discharge probe.

3.1.2 Material Assessment

Thick films for initial evaluation (90–120 nm) were grown on UV-ozone treated silicon substrates; film thickness and uniformity were determined by single-wavelength (632 nm) ellip-

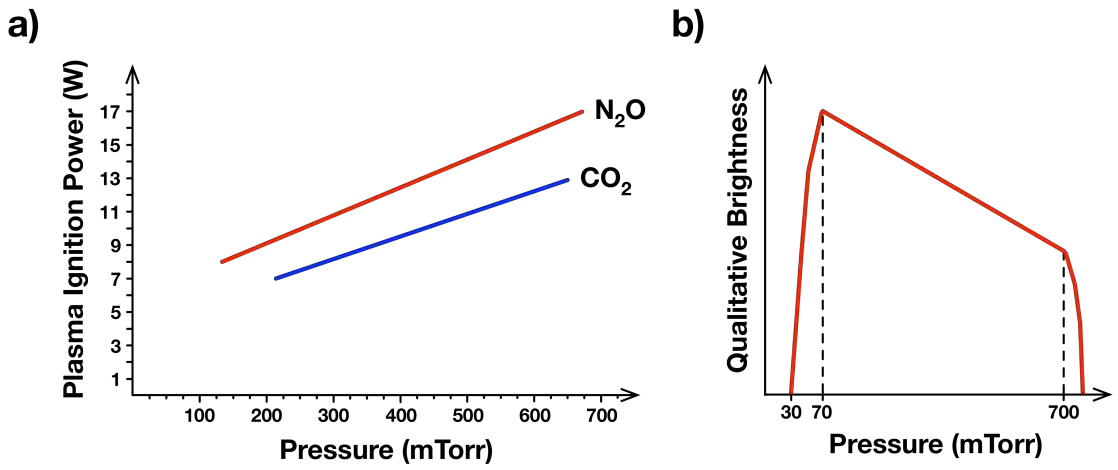


Figure 3.1: RF power required for plasma ignition for various gas pressures, left, and qualitative behavior of plasma brightness as a function of gas pressure at fixed plasma power, right.

sometry and confirmed by profilometry. Average growth rates per cycle were determined by taking the full measured thickness and dividing by the number of cycles. Depending on growth conditions, the growth rates for Al_2O_3 and ZnO are found to be 1.2–1.35 (lower for "Initial Duration" conditions and higher plasma power) and 2.7–3 $\mathring{A}$/cycle (higher for "Initial Duration" conditions and higher plasma power), respectively. These numbers are consistent with (though slightly higher in the case of ZnO) ALD growth rates for these materials in literature [138–145]. Note that this corresponds to sub-monolayer coverage each cycle; this is typical in ALD, where steric hindrance prevents all -OH sites from being occupied. Thickness variation across a 4" diameter wafer is found to be less than $\pm$ 2%.

Refractive indices of ZnO and Al_2O_3 derived from ellipsometry can serve as a measure of film density. We would like dense films because this suggests higher stoichiometry. "Ideal" ZnO and Al_2O_3, with no voids whatsoever, have refractive indices of 2 and 1.76, respectively, at 632 nm. Values in the literature for thin-films report (as expected) lower values in the ranges of 1.77–1.98 and 1.35–1.7, respectively [139–141, 143–148]. Measurements from our films produced refractive indices for ZnO and Al_2O_3 of 1.98 and 1.61, respectively. These

values are at or near the highest values reported in literature, indicating that PEALD has indeed produced dense films.

We perform grazing-incidence X-ray diffraction (GIXD) on our ZnO thin-films (100 nm films grown on (100) Si substrates) to assess their crystallinity. An XRD spectra is shown in Figure 3.2, and indicates the film is polycrystalline, with a dominant (002) peak corresponding to c-axis orientation, the most common ZnO orientation in literature [142,143,149]; while the preferred orientation for fast ZnO TFTs is not well understood, we note that the highest-performance ZnO TFTs in literature have a (002) orientation. From the width of the (002) peak, we use the Scherrer equation to estimate an average ZnO grain size of 25 nm, about 100× smaller than the minimum size used for TFT channel lengths in industry ($\sim$ 2 μm).

To measure the resistivity of the ZnO film, glass slides (1.1-mm-thick Corning 1737) were coated with 100 nm of PEALD Al_2O_3 and 100 nm of PEALD ZnO, and aluminum contacts were thermally evaporated through a shadow mask designed for TLM measurements (TLM described in more detail in Section 3.2). The measured ZnO resistivity was 6 kΩ-cm, corresponding to a sheet resistance of 600 MΩ/sq; we note this is several orders of magnitude higher than the resistivity of ZnO films grown by thermal ALD and more than one order of magnitude higher than ZnO grown by spatial and strong-oxidant plasma-enhanced ALD at ∼200°C, demonstrating the benefit of weak-oxidant plasma-enhanced ALD for TFT applications [141–143, 146, 150, 151]. Using the first-order approximation $\sigma = ne\mu$ to derive electron concentration and assuming a mobility of 10 cm^2/Vs gives n $\sim 10^{14}/cm^3$.

With help from (now Dr.) Gabriel Man in Prof. Antoine Kahn's group and Nick Davy in Prof. Yueh-Lin Loo's group, XPS, UPS, IPES, and UV-visible absorption spectroscopy measurements of 2.5- and 10-nm-thick ZnO films (deposited using "ultimate" conditions from Table 3.3) were performed. Elaborate results from these measurements can be found in Dr. Man's Ph.D. thesis; a brief summary of these results is included for reference below.

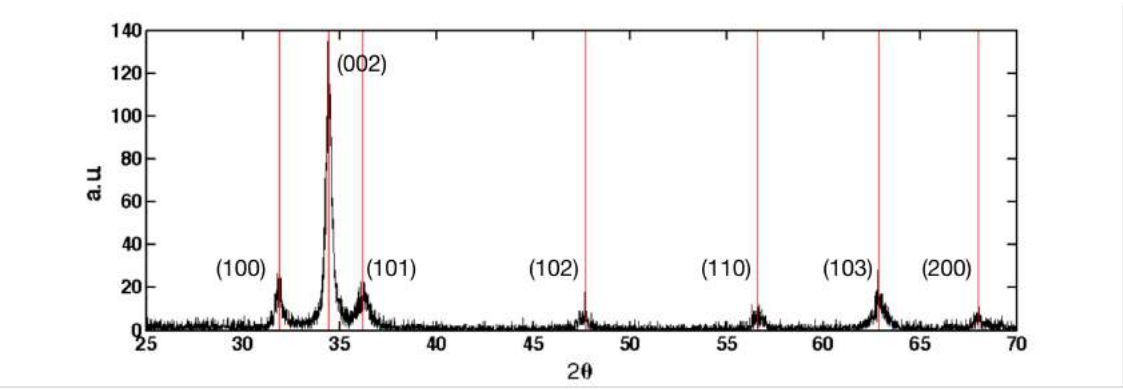


Figure 3.2: Grazing-incidence X-ray diffraction spectra for 100 nm of PEALD ZnO grown on a (100) Si substrate; red lines highlight peaks.

Table 3.3: Parameters of our PEALD ZnO measured by Gabriel Man and Nick Davy of the Kahn and Loo research groups using UPS, XPS, IPES, and absorption spectroscopy, compared to literature reports for single-crystal c-axis oriented ZnO [1–10].

ZnO Parameter	**PEALD**	**Single-Crystal**
E_g	3.2 eV ± 0.3 eV	3.3 – 3.4 eV
Electron affinity	3.2 eV ± 0.3 eV	3.7 – 4.6 eV
Ionization energy	6.4 eV ± 0.3 eV	7.8 eV – 8.1
$E_V - E_F$	- 2.5 eV ± 0.3 eV	- 3.2 – - 3.3 eV
$E_C - E_F$	0.7 eV ± 0.3 eV	0.1 eV
Zn:O Ratio	1.4	–
Optical Gap	3.04 – 3.24 eV	3.3 eV

To further asses Al_2O_3 quality, metal-insulator-metal capacitors were built using "Initial Duration" parameters, and breakdown voltage was measured. To avoid lithography, the capacitor structure included a blanket 100-nm-thick Cr, covered by a 120-nm-thick layer of Al_2O_3, over which a 100-nm-thick shadow-masked Cr layer was evaporated. Circular capacitors 2 mm in diameter exhibit breakdown at 45 MV, or 3.75 MV/cm (see Figure 3.3), which is low with respect to literature reports [138, 148]. However, improvements in this breakdown field have been observed since within TFT structures using lower deposition power and the "Ultimate Duration" parameters, where breakdown occurs at 8 MV/cm. It is likely that both the reduced area (300× less) of these later structures and the improved deposition conditions contribute to this improved breakdown performance.

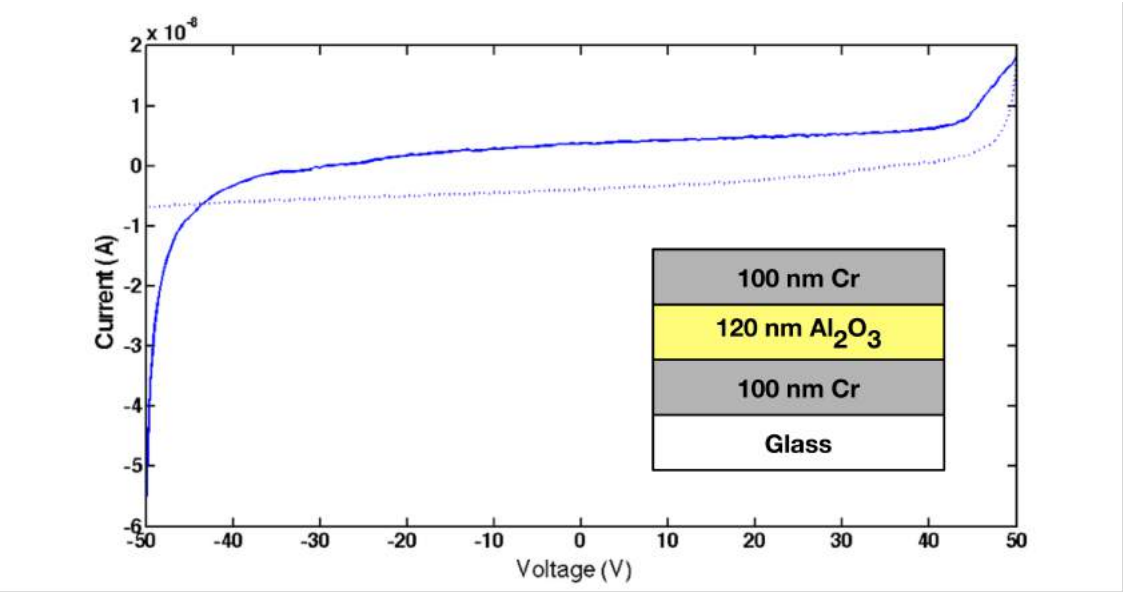


Figure 3.3: Metal-insulator-metal structure begins to show leakage current increase at +45 V.

From this initial material assessment, we moved directly to developing TFTs, so that device parameters could be related to deposition conditions directly.

3.1.3 Etch Recipe Development

The first step in TFT process development is identifying reliable etching recipes for both ZnO and Al_2O_3. In many TFT designs, the gate metal is deposited first, and then patterned and blanket-coated by the dielectric layer and semiconductor, so we must be able to controllably remove these layers in order to access the gate terminal (full process flows and TFT geometries will be introduced in the following sections). One challenge with ZnO-based materials is that they readily etch in most acidic and basic solutions (although ZnO is nearly insoluble in water). Furthermore, our insulator Al_2O_3 is also known to etch easily, and etches even in common alkaline developer solutions.

For ZnO, many wet etching recipes exist that use highly diluted acids to provide a controllable etch rate [152–155] – in this work, we used dilute hydrochloric acid for ZnO etching.

For some applications, it is desirable to have etch selectivity between ZnO and Al_2O_3. While etching ZnO preferentially over Al_2O_3 is easily achieved, the opposite can be more challenging. One approach is to consider the solubility of the two materials over a range of pH values. Because Al_2O_3 has maximum solubility in solutions of pH < 4.2 and > 9.8, while ZnO (while soluble at all non-neutral pH) has maximum solubility at pHs < 9.2 and $>$ 11.5 [156], solutions with pH between 10–11 should provide selective etching of Al_2O_3 with minimal attack of ZnO. A table of several wet etches is provided in Table 3.4.

Table 3.4: Etch rates (E.R.) in nm/min for ZnO and Al_2O_3 in various solutions

Solution	**pH**	**Temp (°C)**	**Al_2O_3 E.R.**	**ZnO E.R.**
2% TMAH in H_2O	13.3	55	5.5	2.5
2% TMAH in H_2O + NH_4Cl	10.5	55	1.6	19
2% TMAH in H_2O + NH_4Cl	10.5	110	4.75	36
25 mM NaOH in H_2O	12	55	7 – 12	< 1
85 % H_3PO_4	-	80	10 – 15	1800
1: 4000 HCl:H_2O	2.5	23	-	45

Because the 25 mM NaOH solution provides a 10× higher etch rate of Al_2O_3 over ZnO, it is our preferred selective etchant. However, as this pH is still out of the optimal 10–11 pH range, there is room for further etch recipe improvement – an example can be found in [157]. It may furthermore be advantageous to move towards a Na-free wet etching recipe to minimize the possibility of incorporating mobile sodium ions in our films. An additional feature of NaOH etching at the interface between Al_2O_3 and ZnO is that, while etching rates are still low, NaOH will preferentially attack ZnO grain boundaries [156]. A microscope image show the result of a 24-hour etch of ZnO in NaOH solution is shown in Figure 3.4; the many colors in the image indicate the ZnO is etched, but etching is visible only along narrow lines randomly distributed across the film surface.

Lastly, the careful grad student should note (as seen in Table 3.4) that TMAH – the active component in AZ 300 MIF developer – etches both Al_2O_3 and ZnO.

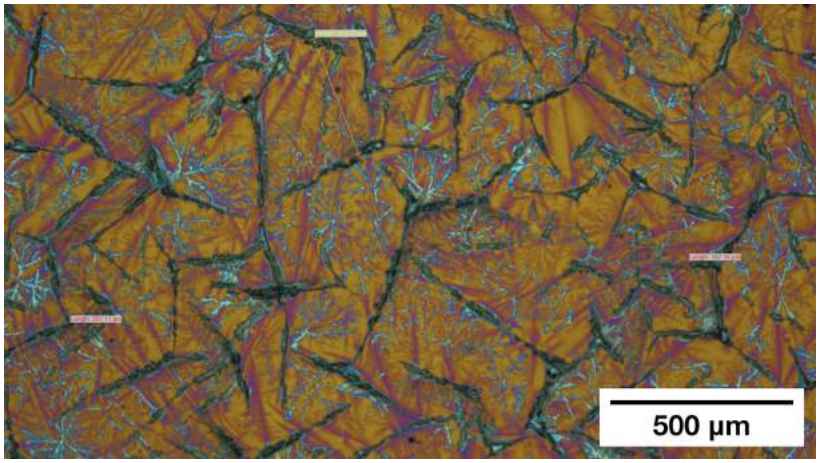


Figure 3.4: 15 nm of ZnO grown on top of 35 nm of Al_2O_3 on a silicon wafer with 100 nm of thermal oxide is left for 24 hours in heated 25 mM NaOH solution. ZnO film total thickness (judged optically by its color) does not reduce significantly, but grain boundaries appear to be strongly etched throughout the depth of the film.

3.2 TFT Basics

3.2.1 Basic Transistor Equations and Definitions

Before launching into TFT development, we briefly note a few equations used to describe DC TFT behavior and quantify TFT and material quality.

While ZnO TFTs operate in accumulation, not inversion like traditional MOSFETs, in practice the expressions developed to analytically describe MOSFETs also apply to TFTs. The current equations are then defined to first order by Equations 3.1 and 3.2. In linear operation, $V_{DS} < V_{GS} - V_T$ and

$$I_{DS,linear} = \frac{\mu W}{L} \frac{\epsilon_{Al_2O_3}}{t_{Al_2O_3}} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS} \tag{3.1}$$

When $V_{DS} > V_{GS} - V_T$, the TFT is considered to be in saturation, and the current expression is:

$$I_{DS,saturation} = \frac{\mu W}{2L} \frac{\epsilon_{Al_2O_3}}{t_{Al_2O_3}} (V_{GS} - V_T)^2 \tag{3.2}$$

where μ is the field-effect mobility, W and L are the channel width and length, $\epsilon_{Al_2O_3}$ and $t_{Al_2O_3}$ are the dielectric constant and thickness of the Al_2O_3 gate dielectric, V_T is the threshold voltage, and V_{GS} and V_{DS} are the gate-to-source and drain-to-source biases, respectively.

Mobility and threshold voltage of TFTs in this thesis are extracted by fitting a straight line to a plot of the square-root of Equation 3.2 versus V_{GS}. The slope of this line contains the mobility, and the intercept contains V_T. Several other methods for extracting mobility and threshold voltage exist; most common is the extraction of mobility in the linear regime. We choose to extract parameters in saturation because we will mostly be operating TFTs in saturation when incorporating them into circuits. We note that in TFTs, mobility exhibits a dependence on gate bias, and will typically increase continuously before saturating and reducing. Mobility extracted from saturation in literature is often reported as this peak value. However, as ZnO TFTs exhibit self-heating effects (as will be discussed in 3.3.3), the mobility typically does not peak; rather, it increases monotonically until the device is destroyed. For this reason, we generally extract mobilities conservatively, at low bias points where heating is less significant.

The subthreshold slope (SS) – the gate bias required to achieve a decade increase in drain current before the threshold voltage is reached – is extracted from the steepest 100-mV region of the $I_{DS,sat} - V_{GS}$ curve. Its steepness reduces when the oxide capacitance reduces or the density of interface states D_{it} (in units of $states/cm^2 - J$) increases, as seen in Equation 3.3 in the absence of a depletion capacitance:

$$SS = ln10\frac{k_B T}{q}\left(1 + \frac{q^2 D_{it}}{C_{Al_2O_3}}\right) \tag{3.3}$$

To simplify the construction of circuit models, the $I_{DS} - V_{GS}$ curves are often approximated using a small-signal model, which focuses on incremental changes to transistor currents from incremental changes in bias voltages. The total drain current i_D is the sum of DC (I_D) and small-signal (i_d) currents; likewise, the total gate bias v_{GS} is the sum of the DC bias

point V_{GS} and small-signal perturbations to this bias v_{gs}. A Taylor expansion of i_D around the DC operating point Q yields (to first order) 3.4:

$$i_D = I_D + \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q V_{gs} \tag{3.4}$$

The partial derivative term is called the transconductance g_m, which corresponds to the slope of the $i_D - v_{GS}$ curve in the vicinity of Q:

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q \tag{3.5}$$

Transconductance is a handy metric commonly used when describing TFTs in a circuit context that holistically includes all parameters that are at a circuit-designer's disposal – not only mobility, but also geometry, capacitance, and overdrive voltage. A large transconductance is generally desirable. Along with transconductance, the output resistance r_o of the TFT is another TFT metric used in circuit models; it quantifies the degree of saturation in the $I_D - V_{DS}$ curve and should be large. For bias point Q, r_o is defined by Equation 3.6:

$$r_o = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q \tag{3.6}$$

In addition to drain-current-related parameters, another parameter of interest is the current that leaks through the gate insulator, I_G. In the current–voltage plots in this work, we typically plot not only the drain current, but also the gate leakage current, to verify that it is low and does not interfere with the drain current behavior.

Lastly, we consider two parasitics in the TFT that are significant because they diminish on current and high-frequency performance: contact resistance and overlap capacitance.

Contact resistance is the resistance between the semiconductor and the source/drain metal in the TFT; when large currents flow through the TFT and/or if the contact resistance is significant, then the voltage drop across the contact region becomes large and the effective voltage dropped across the channel is much smaller than what is applied at the terminals.

This results in reduced on-current and a reduction in the apparent mobility of the TFT. To extract contact resistance, a variation of a traditional transmission line measurement (TLM) can be performed, where TFTs of increasing channel length and constant width are fabricated. If the TFT is biased comfortably within the linear regime, it can be accurately modeled as a resistor for a constant gate bias. Current can then be measured at a range of gate biases to determine the total TFT resistance R_{TOTAL}, described by Equation 3.7, which corresponds to a straight line:

$$R_{TOTAL} = 2R_{CONTACT} + R_{CHANNEL} \approx 2R_{CONTACT} + \frac{L}{\mu W C_i (V_{GS} - V_T)} \tag{3.7}$$

When resistance is then plotted versus channel length for a given gate bias, the intersection with the y-axis (i.e., channel length L = 0) gives the residual resistance that comes from the device contacts. In TFTs, contact resistance itself is also a function of gate bias [158], so it is important to characterize contact resistance at the gate bias appropriate for one's chosen application. An illustration of this process is shown in Figure 3.5.

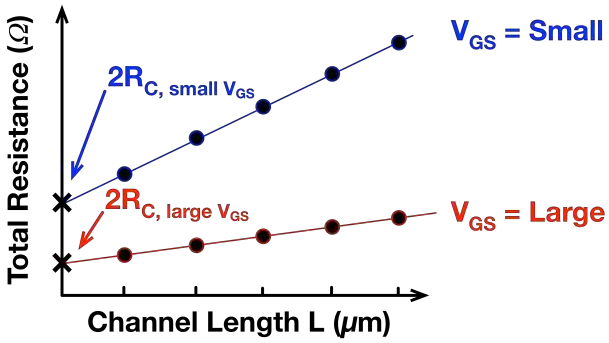


Figure 3.5: Contact resistance extraction idealization.

Overlap capacitance is another common parasitic TFT element that that can limit device performance at high frequency, which will be discussed at length in the next chapter. While for operation, the TFT benefits from a high capacitance between the conducting channel and the gate metal (C_i), in practice, there is also a non-zero overlap between the gate metal and

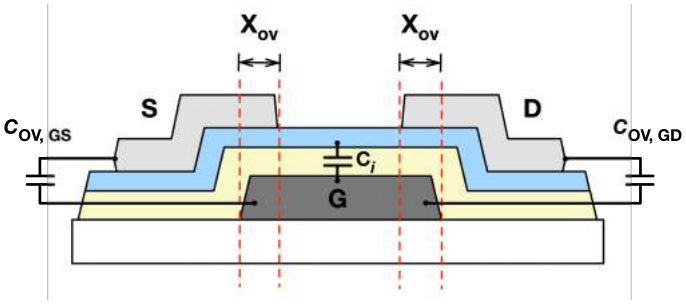


Figure 3.6: Physical overlap between the gate, source, and drain X_{OV} results in undesirable parasitic capacitance in the TFT.

the source and drain metals (identified in Figure 3.6) that contributes two additional parallel-plate capacitances $C_{OV,GS/D}$ that are proportional to the area of overlap. For high-frequency circuits, this dimension should be kept as small as possible.

3.2.2 TFT Geometries

Before settling on a particular TFT recipe, decisions must be made regarding device geometry, materials, and layer thicknesses. These decisions are driven by 1) device level goals, namely, high mobility, low threshold voltage, steep subthreshold slope, low off-current, and low parasitic resistances/capacitances, and 2) processing feasibility, namely protecting vulnerable layers from unwanted etching and/or defect generation and reducing the number of required masks.

Common TFT geometries differ in the order in which active layer, source/drain metal, and gate metal are stacked. The gate metal can be either at the bottom of the stack (bottom-gate) or at the top (top-gate), and the source and drain metal can be either on the same side of the semiconductor as the gate (coplanar) or on the opposite side (staggered or inverted). The four combinations of these can be seen in Figure 3.7, and each has its advantages and disadvantages [42]. In a staggered TFT, source and drain are separated from the channel by the thickness of the semiconductor. This results in a field-enhancement in the source/drain region that makes charge injection more efficient, but also results in an

additional parasitic resistance because the thickness of the semiconductor must be traversed. The coplanar structure circumvents this problem because the source and drain are in-line with the channel, but also does not have the benefit of field-enhancement. The bottom-gate structures reduce exposure of the active layer to chemicals and plasma processing (the bottom-gate coplanar structure more so than bottom-gate staggered). A top-gate structure can be advantageous in cases where the top surface of a semiconductor has better material properties compared with the initial few deposited layers at the bottom surface, because the channel will be formed at the top interface.

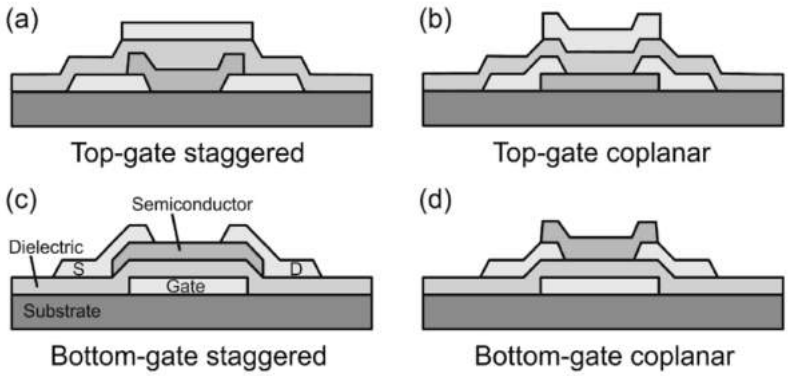


Figure 3.7: TFT geometries include: top-gate, staggered (a), top-gate, coplanar (b), bottom-gate, staggered (c), and bottom-gate, coplanar (d) [42].

In our case we choose a bottom-gate structure to protect the easily-etched ZnO. We decided to use a staggered source/drain configuration such that the gate dielectric and semiconductor could be deposited without breaking vacuum in the PEALD system in order to create a reproducible interface. In the following subsections, I will describe fabrication of bottom-gate staggered ZnO TFTs similar in structure to Figure 3.7c, followed by recipes for similar structures that are passivated and self-aligned. While we have not explored other geometries in this work, one particularly useful geometry is a double-gate structure, which in effect creates two conducting channels at the top and bottom interfaces [159].

3.3 Unpassivated ZnO TFTs

3.3.1 Process Development

Initial ZnO TFTs described in this section had no passivation layer, because this presented the most straightforward process. Below we describe considerations for the gate metal, oxide layer thicknesses and deposition conditions, and source/drain metal, followed by step-by-step schematics of the complete fabrication process.

Gate Metal

The choice of bottom-gate geometry requires a gate metal that can survive many processing steps. Aside from this more practical concern, the gate metal should also provide a work function that does not contribute a large threshold voltage offset, or ZnO circuits will require unneccessarily high supply voltages. Because ZnO TFTs operate in accumulation, the work function of the gate metal could also be used to create a condition where the channel is depleted in thermal equilibrium, resulting in very low off-state current.

We use chrome as a gate metal. It is deposited first in the bottom-gate structure, and subsequently exposed to oxidizers in the the PEALD process. Because Cr has a high melting point (1907°C), it is unlikely to exhibit creep deformation when exposed to the 200°C PEALD deposition (unlike, for example, Al).

From the values in Table 3.3, it is expected that a Cr-gate metal would produce a depleted channel at zero gate bias for a single-crystal ZnO transistor. While the parameters measured for our PEALD ZnO differ from those of single-crystal ZnO, we still expect a depleted channel in thermal equilibrium (see sketch in Figure 3.8), because the Cr work function (4.5 eV) is positioned deeper than the measured Fermi level of PEALD ZnO (3.9 eV). A depleted channel is desirable in thermal equilibrium because it would result in very low off-currents. Other refractory metals with work functions in the 4.3 - 4.5 eV range like Ti and Mo would likely also be good gate metal candidates. The Cr layer is sputtered onto

our glass substrates and patterned via wet etching.

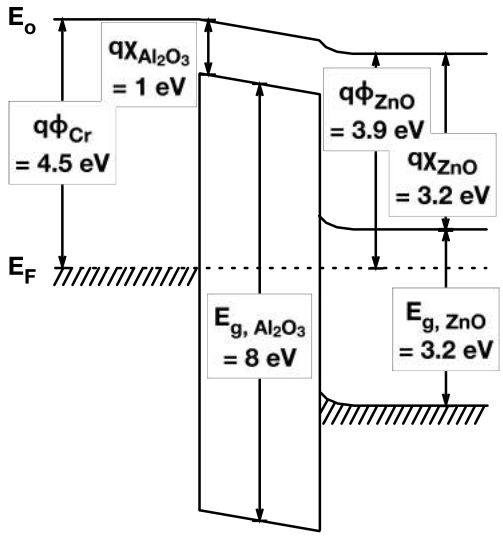


Figure 3.8: A sketch showing thermal equilibrium band diagram looking from the Cr gate metal to the ZnO layer ($V_{GS} = V_{DS} = 0$ V) for a ZnO transistor using values determined by UPS/IPES for our PEALD ZnO as in Table 3.3.

Al_2O_3 Gate Dielectric and ZnO

In the next step of the TFT process, ZnO and Al_2O_3 are deposited (on top of the Cr layer) in the PEALD without breaking vacuum. Suitable thicknesses for the ZnO active layer and Al_2O_3 dielectric must be determined. For a resistive semiconductor (like our ZnO) in a bottom-gate or top-gate structure, the active layer should be thin to minimize parasitic resistance contributions from the thickness of the semiconductor that charge carriers must traverse (although a thin active layer increases the influence of the back surface of the ZnO). The gate dielectric should also be thin, in order to reduce the TFT's subthreshold slope, but should be thick enough to provide uncompromised step coverage and low gate-leakage current.

We built TFTs using a range of thicknesses for ZnO and Al_2O_3 gate dielectric; measurements are shown in Figure 3.9. Ultimately, we find a 40-nm-thick gate dielectric and 10-nm ZnO channel provide the lowest subthreshold slope and threshold voltage. As dielectric

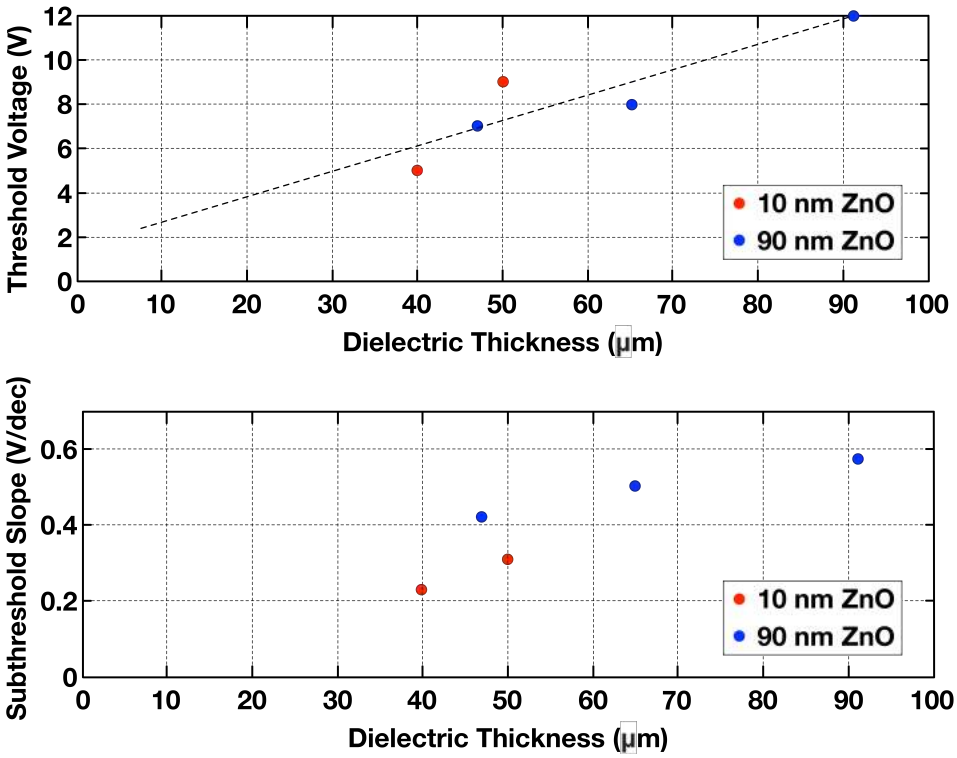


Figure 3.9: As expected, threshold voltage and subthreshold slope reduce with reduced PEALD Al_2O_3 gate dielectric thickness. In addition, subthreshold slope is steeper for thin (10 nm) versus thick (90 nm) PEALD ZnO.

thickness reduces, we note that the gate leakage does not increase, and typically remains 1–10 pA, even for gate metal 225-nm thick.

Furthermore, on-current for 10-nm ZnO is higher than for thicker ZnO layers, because the parasitic bulk resistance is minimized; histograms comparing TFTs with 10-nm and 20-nm thick ZnO layers illustrate this point (Figure 3.10).

We note that ZnO TFTs show a strong dependence on plasma parameters during PEALD. In Figure 3.11, we see unpassivated TFTs processed at (a) 0.2 W/cm^2 and (b) 0.1 W/cm^2 conditions. The degraded subthreshold slope in Figure 3.11a suggests that exposure to stronger plasmas increases interface trap density as described in Equation 3.3.

One additional tunable parameter of note is the substrate temperature during PEALD. As seen in the left of Figure 3.12, reducing the temperature setpoint from 225 to 200 to

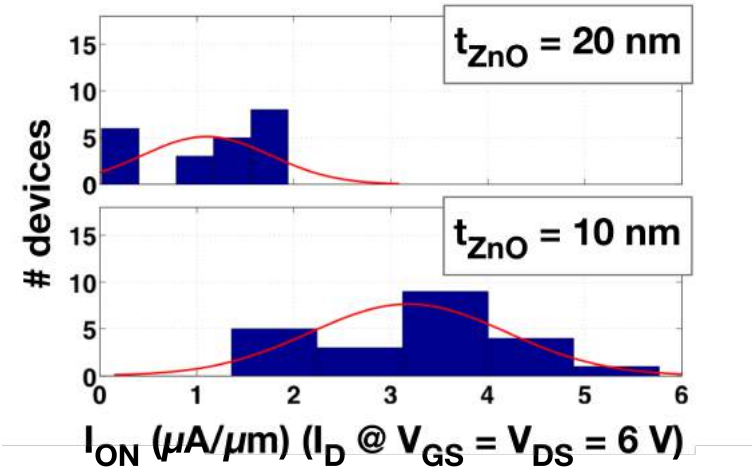


Figure 3.10: Histograms of on-current, defined here as the drain current at $V_{GS} = V_{DS} = 6$ V, is plotted for these TFTs with a 40-nm-thick Al_2O_3 gate dielectric and W/L of 20. In addition, subthreshold slope is steeper for thin (10 nm) versus thick (90 nm) PEALD ZnO. 10-nm ZnO results in higher on-current.

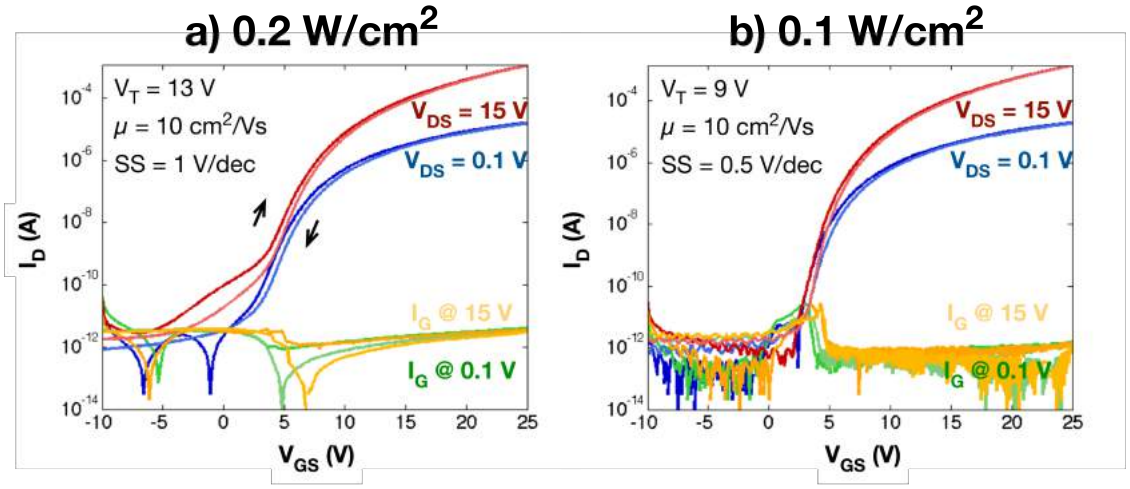


Figure 3.11: TFTs with 75 nm Al_2O_3 gate dielectric and 90 nm ZnO layer with different PEALD plasma densities during oxide deposition. TFT W/L is 600/80 μm.

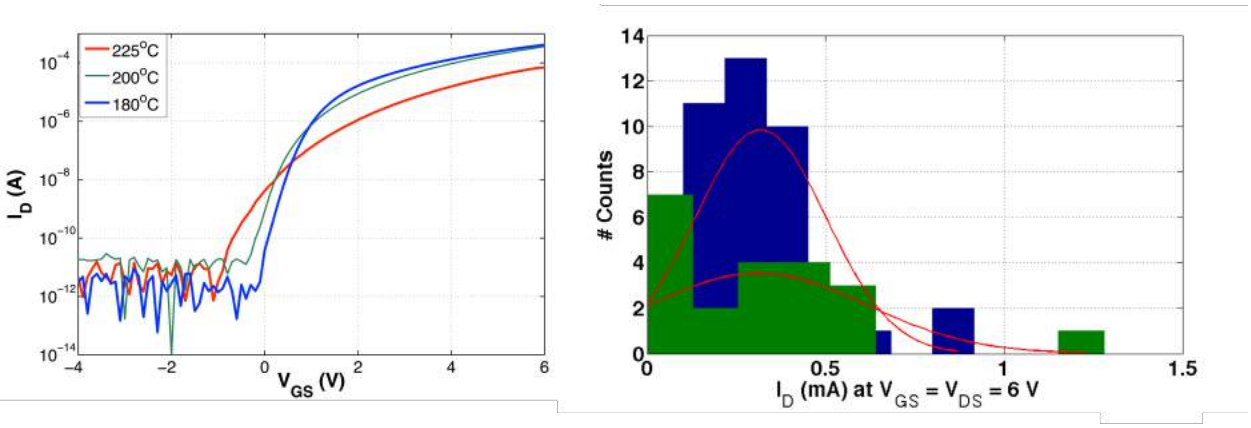


Figure 3.12: TFTs with 40 nm Al_2O_3 gate dielectric and 10 nm ZnO layer with different substrate temperatures during oxide deposition. TFT W/L is 200/10 μm and V_{DS} = 6 V. Note that these devices are in fact passivated, but included in this section for clarity; this is why the turn-on voltages are negative in this plot.

180°C results in TFTs with near-zero turn-on voltage, steep subthreshold slope, and higher on-currents. However, this occurs at the expense of variation control. The right hand side of Figure 3.12 shows that while the I–V curve for devices deposited at 180°C are the best, the spread in on-current (drain current at 6 V = V_{DS} = V_{GS}) is far worse than for devices deposited at 200°C. Hence, we choose to deposit oxides at 200°C.

After oxide deposition, the ZnO is etched with dilute HCl for device isolation. To minimize ZnO exposure to chemicals, the patterned Al_2O_3 area is larger than the ZnO area, and the source and drain metals, discussed next, are defined using lift-off.

Source/Drain Metal

The source/drain metal should provide an ohmic contact – i.e., it should be able to inject electrons into the ZnO channel, so its work function should ideally be slightly above the ZnO Fermi level. We use both aluminum and titanium, which have work functions of 4.06 – 4.26 eV and 4.33 eV. While the work function of single crystal ZnO (4.2 eV) is near these values, we note that for our PEALD ZnO (according to Table 3.3), we would actually expect an electron barrier to form between the ZnO channel and the source and drain in thermal

equilibrium (see sketch in Figure 3.13), because the Ti work function lies below the measured PEALD ZnO Fermi level (3.9 eV).

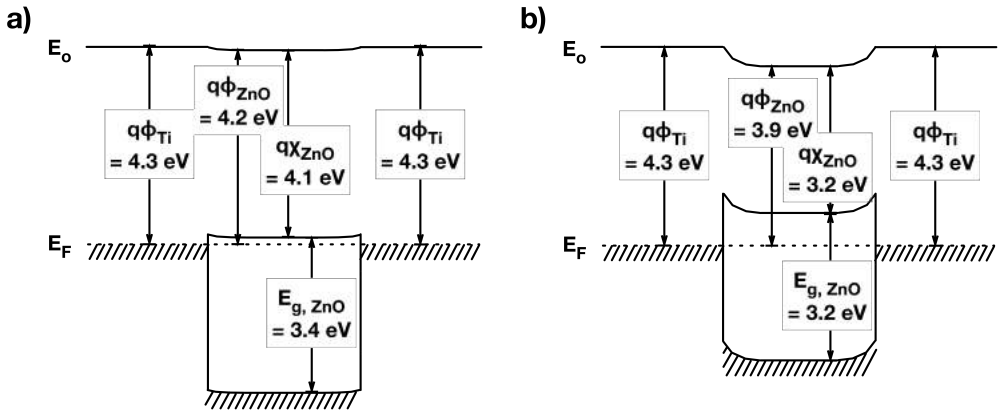


Figure 3.13: A sketch showing thermal equilibrium band diagram looking laterally across a ZnO transistor from Ti source to ZnO to Ti drain ($V_{GS} = V_{DS} = 0$ V) using values from Table 3.3 for a) single-crystal ZnO and b) PEALD ZnO.

This may not be surprising, especially given the gate-voltage dependent contact resistance behavior commonly observed. However, in practice ohmic contacts to ZnO and IGZO are commonly reported, and Ti, ITO, Cu, Mo, and Al have all been used successfully for this purpose in literature [160, 161] – although in several cases plasma treatment or an Al-doped ZnO layer have been used to further reduce contact resistance by increasing electron concentration in the contact regions [162, 163].

Contact resistances extracted from TLM measurements of 10-nm thick ZnO TFTs with a Ti S/D are shown in Figure 3.14, and indicate that while contact resistance is large at low gate bias (in accordance with the reasoning in Figure 3.13), upon application of gate bias, the metal/ZnO contact barrier is lowered, and the contact resistance becomes small at the bias point of interest ($\sim V_{GS} = 8$ V) compared to the channel resistance (e.g., $\sim 5\%$ of $R_{channel}$).

After deciding upon gate metal, oxide layer thicknesses, and source drain metal, the recipe for unpassivated ZnO TFT fabrication could be finalized. A process overview diagram

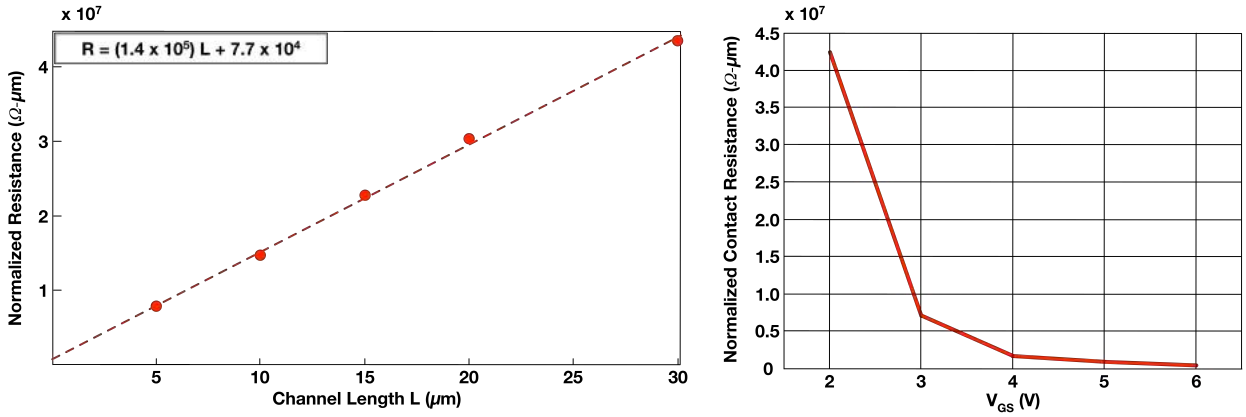


Figure 3.14: Extracted contact resistance at $V_{GS} = 8$ V (left) is a small fraction of total resistance, although contact resistance becomes large at lower V_{GS} (right).

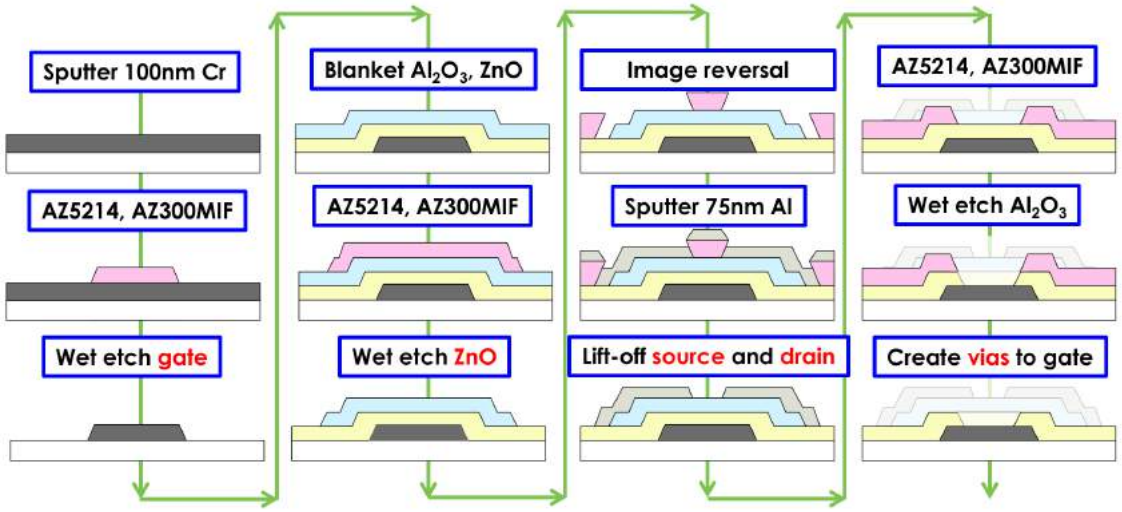
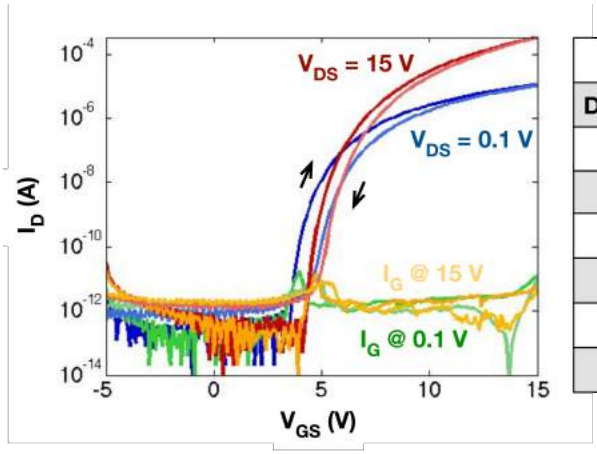


Figure 3.15: General process flow for unpassivated ZnO TFTs. Specific details in Appendix.

is shown in Figure 3.15 and the precise recipe can be found in the Appendix. Typical I-V characteristics and parameters for TFTs fabricated in this manner are shown in Figure 3.16.

3.3.2 Instability

Because ZnO is not stable in atmosphere, unpassivated ZnO TFT I–V characteristics will drift over time in ambient conditions (see Figure 3.17). There are two plausible culprits for this behavior: ambient exposure may allow further diffusion of atmospheric hydrogen into



ZnO thickness (nm)	10
Dielectric thickness (nm)	40
μ (cm^2/Vs)	15
V_{TH} (V)	7
SS (mV/dec)	200
Max g_m (mS)	0.49
W (μm)	800
L (μm)	60

Figure 3.16: Typical I–V characteristic (left) for unpassivated ZnO TFTs and important parameters (right). Deposition conditions correspond to "Ultimate Duration" parameters in Table 3.2, 0.1 W/cm^2 power density, and 200°C.

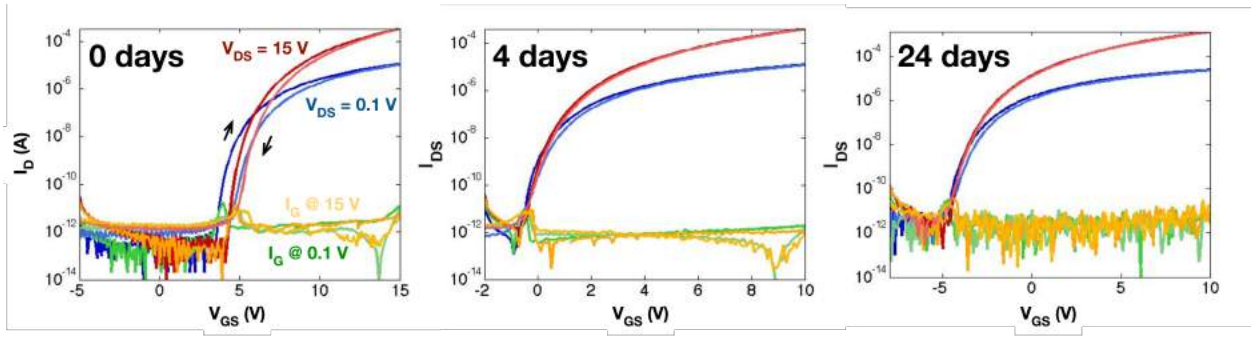


Figure 3.17: Unencapsulated TFTs (43 nm dielectric, 10 nm active layer) are unstable in atmosphere: the current–voltage characteristic is seen to drift negative over time. W/L is 800/60 μm.

the ZnO back channel, or adsorbed water vapor on the back channel could produce a layer of positive charge in the thin ZnO that shifts the threshold voltage negative over time.

To see if we could recover initial TFT behavior, we exposed unpassivated TFTs to a range of annealing conditions with the intent of driving out the unwanted water or hydrogen. A summary of these trials can be found in Table 3.5. No annealing treatment was capable of returning the TFTs to their initial state; hence, we moved quickly to strategies for TFT back-channel passivation as will be described in Section 3.4. However, we note that the annealing of thick (90 nm) ZnO TFTs in N_2O and ambient conditions produced some beneficial results

– the ambient anneal was able to largely return the TFTs to initial conditions after they had drifted - 35 V over the course of one month. Notably, the same annealing condition was severely detrimental to thin (10 nm) ZnO TFTs, suggesting that the effect of surface species at the back-channel is magnified in thin-ZnO TFTs compared to thick-ZnO TFTs.

Table 3.5: Annealing unpassivated thick (90 nm) and thin (10 nm) ZnO TFTs produces mixed results.

Gas	**Temp (°C)**	**Pressure (mTorr)**	**Time (min)**	**Effects**
UV – Ozone	25	Atm.	5	Thick ZnO: severe SS degradation
N_2O	200	700	120	Thick ZnO: 25% steeper SS
Ambient	250	Atm.	60	Thick ZnO: V_T shifts + 25 V, 30% steeper SS
Ambient	250	Atm.	60	Thin ZnO: V_T + 5 V; hysteresis 3 V
2% H_2 in N_2	220	Atm.	10	Thin ZnO: V_T + 4 V; hysteresis 2 V
H_2O	200	700	20	Thin ZnO: V_T + 3 V; hysteresis 1 V

3.3.3 Heat and Illumination

One feature of note for ZnO TFTs is their tendency to self-heat, as previously reported in [164]. This behavior is apparent when acquiring the $I_D - V_{DS}$ curve. As seen in Figure 3.18, the drain current is a function of acquisition method – the continuously swept sample exhibits much higher current (and significantly worse output resistance) than the curve generated by a pulsed V_{GS} (e.g., gate bias applied for 1 ms, then gate grounded for 1 s), allowing the device to cool between gate bias applications. The disparity increases at higher current densities. The dependence of extracted mobility on current density, shown in Figure 3.19, explicitly illustrates this effect.

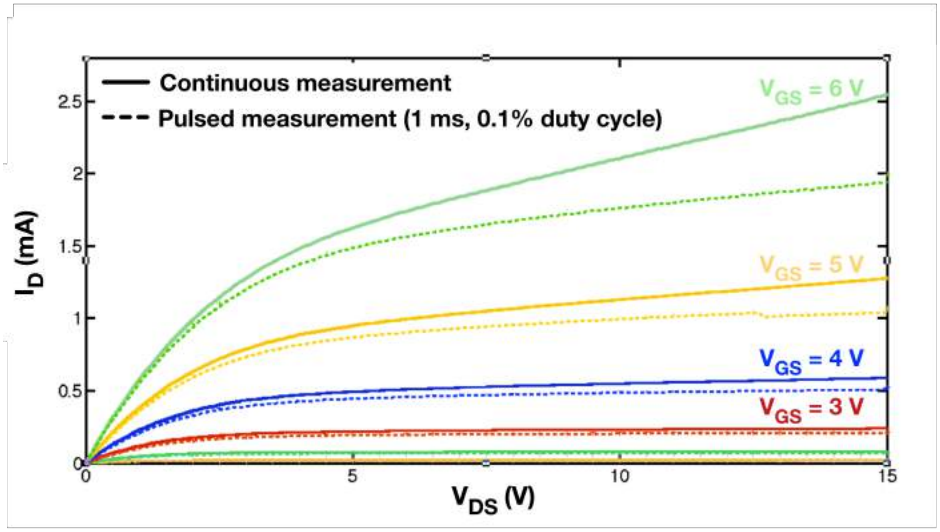


Figure 3.18: Current levels in ZnO TFTs are much higher when gate bias is applied continuously (solid lines) rather than pulsed (dashed lines), a result of self-heating effects. W/L = 500/5 μm

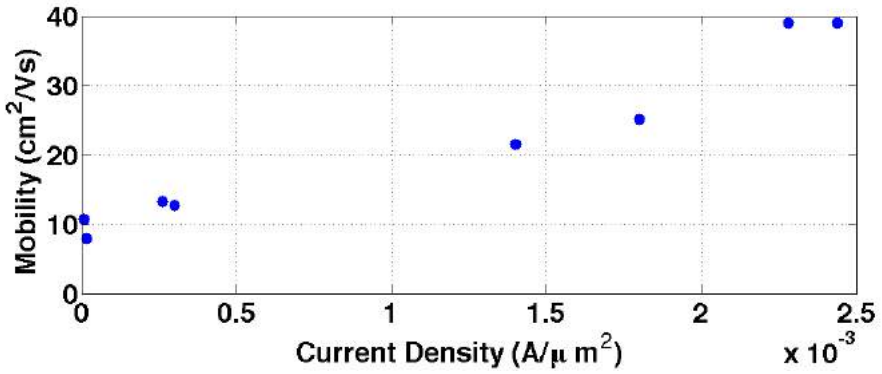


Figure 3.19: Mobility, extracted for V_{DS} = 15 V from a range of TFT sizes with constant ZnO thickness has a linear dependence on current density (e.g., TFT drain current divided by the channel surface area $W \times L$), which further emphasizes the impact of self-heating.

When ZnO TFTs are externally heated (in a probe station with a heated chuck) at bias points with minimal self-heating, the same behavior is observed (see Figure 3.20. Extracting mobility, threshold voltage, and contact resistance from curves of externally heated TFTs indicates that the extracted mobility increases, the threshold voltage shifts negative, and the contact resistance reduces upon heating (Figure 3.21). While all three result in increased current upon heating, the extracted mobility enhancement (145 %) changes most significantly

at the bias points of interest (contact resistance changes, while very significant at low bias, become very small above 5 V). Hence, as devices produce current, Joule heating enhances mobility, which results in an additional increase in current, which in turn produces more heating. At higher current densities (> 200 A/cm^2), this process results in device failure and effectively places an upper limit on ZnO TFT current densities and a lower limit to device scaling on thermally insulating substrates.

It may be surprising that our ZnO TFTs exhibit an extracted mobility that increases with increasing temperature. In fact, single-crystal ZnO exhibits Hall mobility that decreases with increasing temperature, similar to behavior seen in crystalline Si and other materials [165, 166]. However, in polycrystalline ZnO, the opposite behavior has been observed [167]. This behavior has been explained using Seto's analysis for polycrystalline silicon: thermally-activated carrier transport over potential barriers is enhanced as temperature rises, so long as doping levels are low enough such that tunneling is not the dominant transport mechanism [22, 167, 168]. We note that amorphous oxide and amorphous silicon TFTs also exhibit mobility that increases with temperature, although in these cases the physical mechanism must differ [169–171].

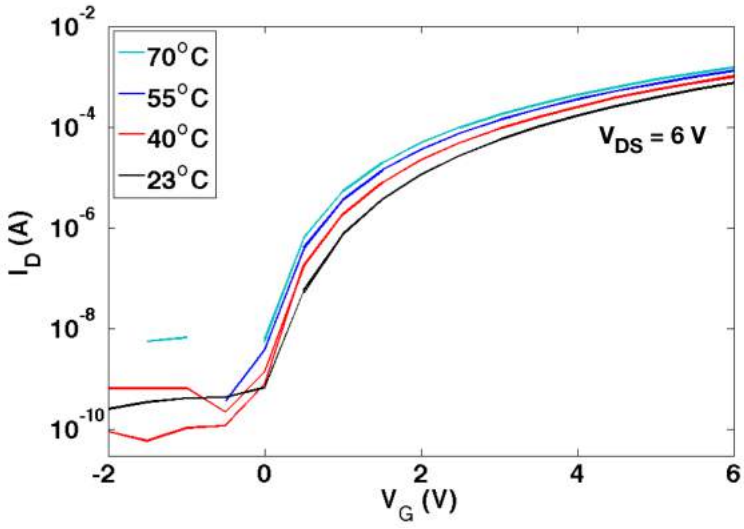


Figure 3.20: Pulsed I_D–V_{GS} curves (1 ms V_{GS} application, 0.1% duty cycle) for a standard ZnO TFT with W/L = 3000/30μm as a function of substrate temperature.

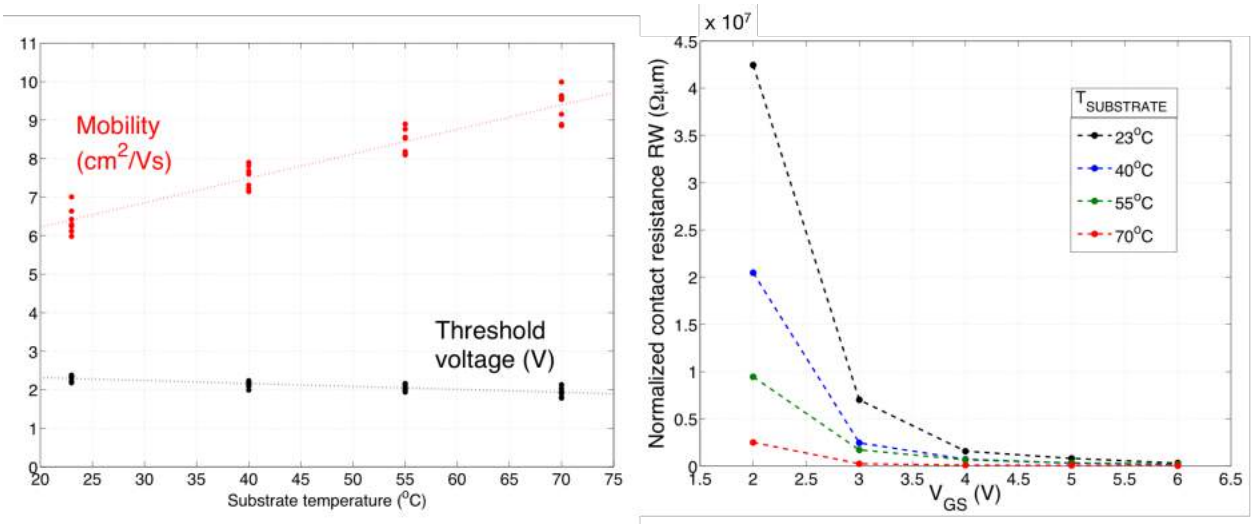


Figure 3.21: Extracted mobility and threshold voltage at $V_{GS} = V_{DS} = 6$ V as a function of substrate temperature (left) and width-normalized contact resistance as a function of substrate temperature and gate bias (left).

One final brief note is the effect of visible light on ZnO TFTs. As mentioned, IGZO TFTs are unstable in the presence of visible light and exhibit persistent photoconductivity; TFTs exposed to moderately bright (5 mW/cm^2) white light exhibit negative threshold voltage shifts [172]. Surprisingly, ZnO TFTs we tested did not exhibit a threshold voltage shift upon exposure to bright white illumination of similar intensity (Figure 3.22, left). While a 10× increase in drain current was observed upon light exposure for a negatively biased TFT (Figure 3.22, right), the current level dropped back to its baseline value once the light was turned off. This behavior is also visible in the negative portion of Figure 3.22 (left). Note that ambient indoor light, which is typically of much lower intensity ($\sim$ 25 μW/cm^2) [173], does not produce an increase in current in Figure 3.22. Under forward bias, any current increase is unobservable. Further experiments with light stress of longer duration should be done to investigate the robustness of this measured ZnO TFT light stability.

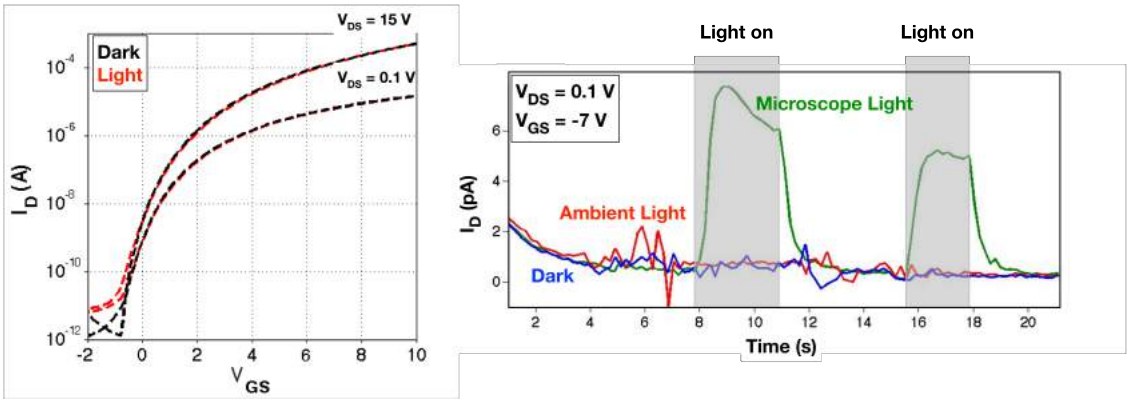


Figure 3.22: TFT (W/L = 800/60 μm) under bright microscope illumination and negative gate bias demonstrates an increase in current that disappears once the light source is removed. Note that ambient light (orders of magnitude dimmer) has no discernable impact on drain current.

3.4 Passivated ZnO TFTs

3.4.1 Passivation Materials

Because unpassivated ZnO TFTs drift over time, we sought out a suitable passivation layer to stabilize the back interface. First, we explored ex-situ passivation options; e.g., passivation layers that could be deposited and patterned on top of a functional, fully-fabricated unpassivated ZnO TFT. Prior work emphasized the importance of reducing plasma exposure of the back interface [174]. For this reason, a thermal ALD Al_2O_3 layer was deposited on top of our unpassivated TFTs in our PEALD system (operating in thermal-ALD mode), using alternating exposures of H_2O and TMA (1 s) separated by a 30 s purge time at 200°C. However, in our chamber, we were unable to replicate the success in [174]; instead, the TFTs upon passivation became completely conducting and could not be turned off (see Figure 3.23).

It is possible that hydrogen exposure from the water flushing in the thermal process resulted in an increase in ZnO conductivity; it is also possible that the top Al_2O_3 contained a high density of positive charge near the ZnO interface that shielded the back channel from the influence of the back bias, resulting in the devices being always "on". To investigate,

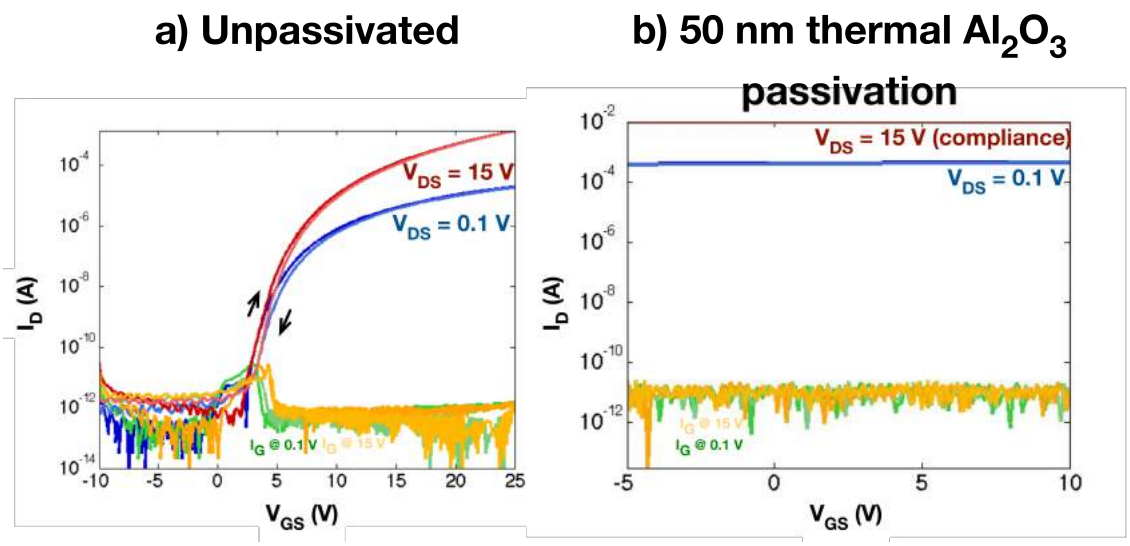


Figure 3.23: Functional unpassivated TFTs (90 nm active layer) (a) become completely conducting after a 50 nm of thermal Al_2O_3 is deposited on top (top oxide layer patterned to provide access to gate contacts). The same result is found for thin (10 nm) ZnO TFTs. W/L = 800/60 μm.

a second gate metal was deposited and patterned by lift-off on top of the passivation layer. As seen in Figure 3.24, while this structure resulted in some degree of channel control, the application of a bias of -20 V with respect to the source (at a front-gate bias of - 35 V) was still not sufficient to fully turn off these TFTs. This, combined with the very poor subthreshold slope in the curves in Figure 3.24, suggest that the second hypothesis may be more likely.

Another passivation material at our disposal was PECVD SiO_x; in contrast to the thermal ALD Al_2O_3, this SiO_x has been demonstrated to be very high quality. While [174] indicates that SiO_x deposited by PECVD will result in a threshold voltage shift, the shift is relatively small compared to other alternatives like SiN_x. The results of this experiment are shown in Figure 3.25: the TFTs I–V characteristic shifts negative by several volts and the subthreshold behavior degrades, once again suggesting a high density of positive charge at the ZnO-passivation interface. This is also an undesirable effect.

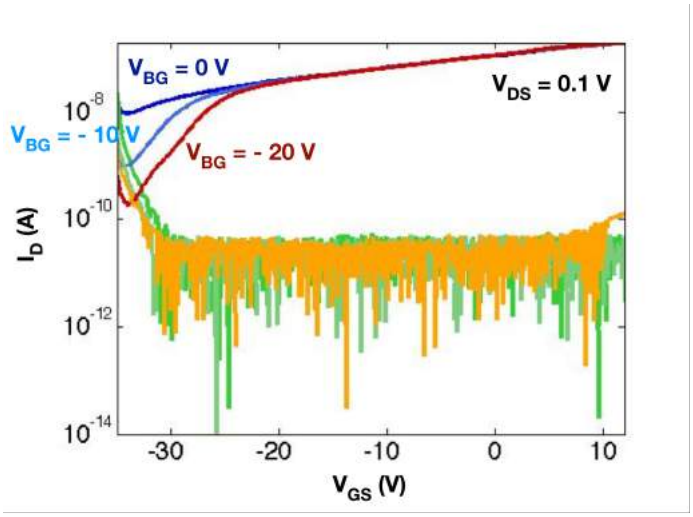


Figure 3.24: An aluminum back gate was deposited on top of the thermal ALD Al_2O_3 passivation layer, but applying bias to this back gate (V_BG) exhibits limited influence over drain current. W/L = 800/60 μm.

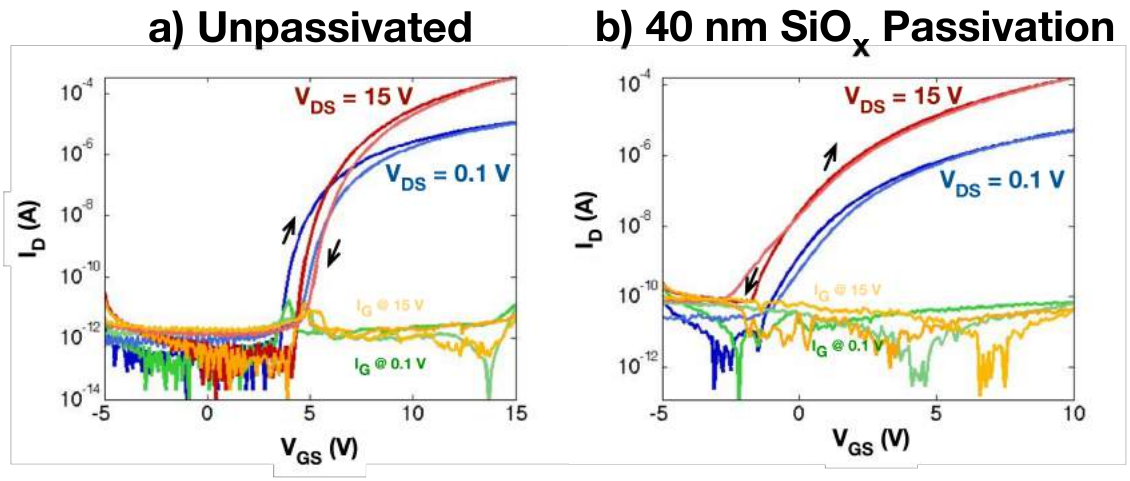


Figure 3.25: PECVD SiO_x results in a negative shift of the I–V curve and a degradation of subthreshold slope when used to passivate ZnO TFTs. W/L = 800/60 μm.

With the assistance of Dr. Israel Ramirez from Penn State University, we were able to also passivate some of our ZnO TFTs with thermal ALD Al_2O_3 using the same equipment as in [174]. This process results in a negative curve translation and subthreshold degradation (seen in Figure 3.26), but is an improvement over SiO_x.

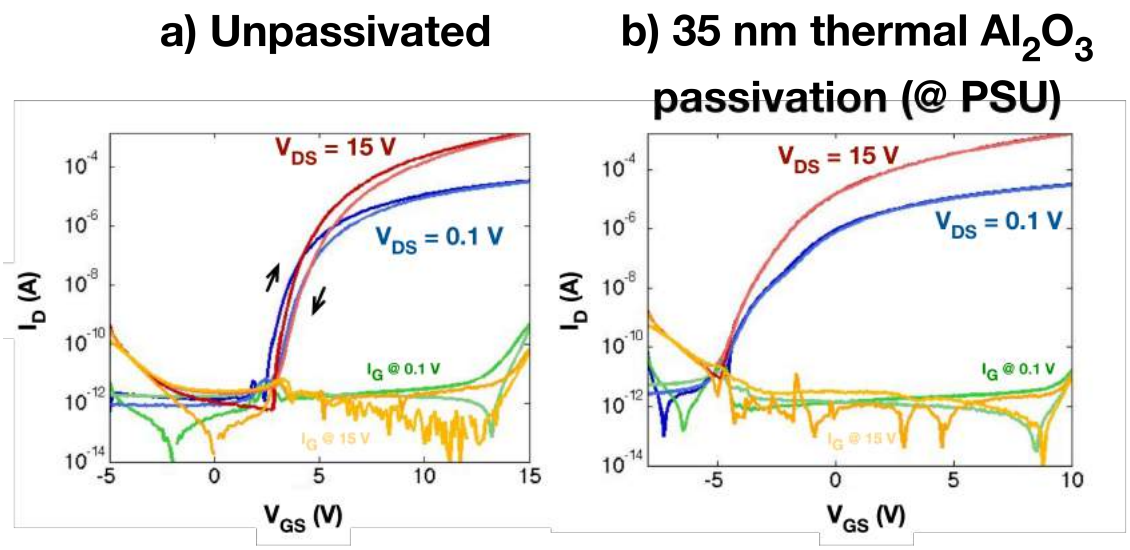


Figure 3.26: Al_2O_3 deposited by thermal ALD at Penn State University provides useable TFTs, and promised that there is hope for a thermal ALD passivation layer at Princeton with substantial process investigation. W/L = 800/60 μm.

3.4.2 Standard Passivated TFT Process

While the result from the PSU deposition was promising, ultimately it was desirable to invest time in a process that would result in a consistent ZnO – passivation layer interface to minimize process variation. For this reason, the passivated TFT process we use, based on [175], deposits dielectric, semiconductor, and passivation layer all without breaking vacuum, and makes vias to the underlying semiconductor using the NaOH selective etch process described above. We expect this process – "in-situ" passivation – to result in a more reproducible interface between the ZnO and the passivation because in this way, the ZnO will never be exposed to atmosphere. The process overview is shown in Figure 3.27, and details are provided in the Appendices.

Note that a bi-layer resist (PMMA and AZ5214 photoresist) must be used as AZ5214 is soluble in NaOH solution; PMMA is insoluble in developers like NaOH, and hence enhances adhesion between the AZ5214 and the Al_2O_3 during the selective etch process, at the expense of an additional spin-coat step and plasma descum step. Without said PMMA layer, because

both the Al_2O_3 and the AZ5214 are etching/developing, their interface is extremely weak and the narrow ribbon of resist protecting the channel region of the TFT will generally peel off the sample entirely, shorting the source and drain and making the TFT useless.

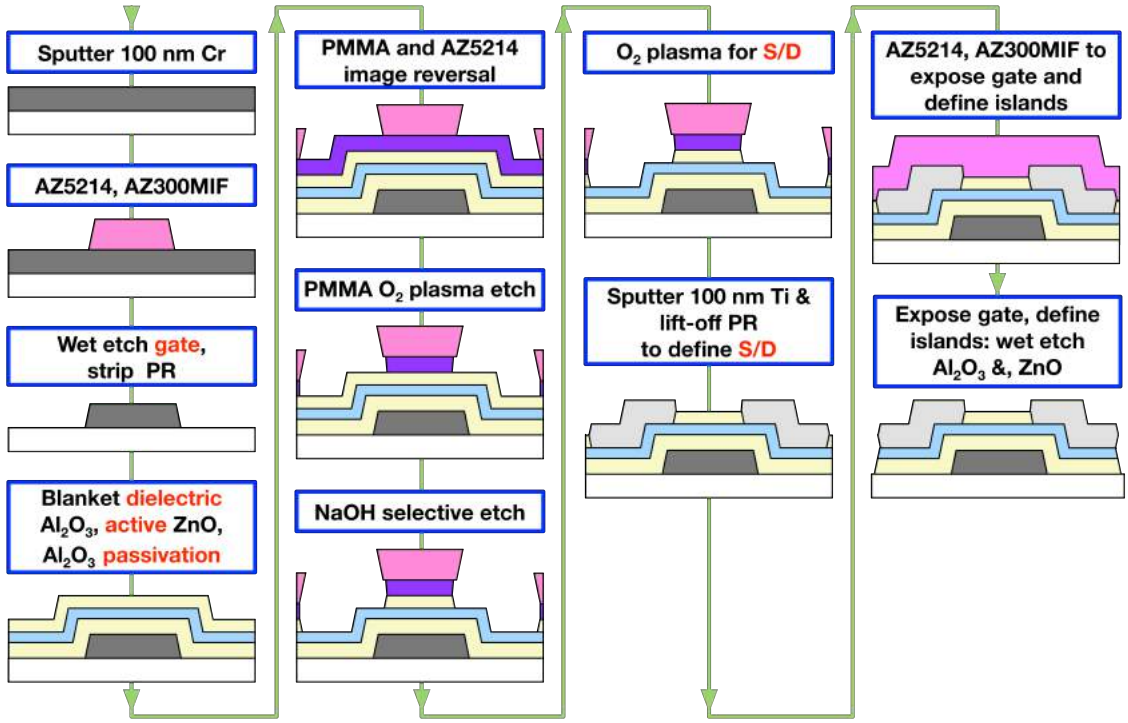


Figure 3.27: Typical passivated TFT process allows in-situ deposition of dielectric, semiconductor, and passivation. All details of fabrication presented in Appendices.

We note that even with this bi-layer resist, as W/L ratios for TFTs scale to large values ($>$ 100), the photoresist layer, which still develops in NaOH despite, tends to peel off. Because the PMMA on its own is too thin to provide enough step height for the lift-off process, once again the TFT will be shorted. To avoid this heartbreak, one can use a layout trick, shown in Figure 3.28, where larger resist "posts" strengthen the adhesion locally in the channel area. Making this modification enables TFTs with W/L values of at least 400.

Typical I-V curves and TFT parameters for passivated devices are provided in Figure 3.29. Note that the threshold voltage has been shifted several volts negative compared to Figure 3.16, but the curve is largely translated without subthreshold deterioration. This TFT recipe is our workhorse, and will be used throughout the following chapters. As discussed,

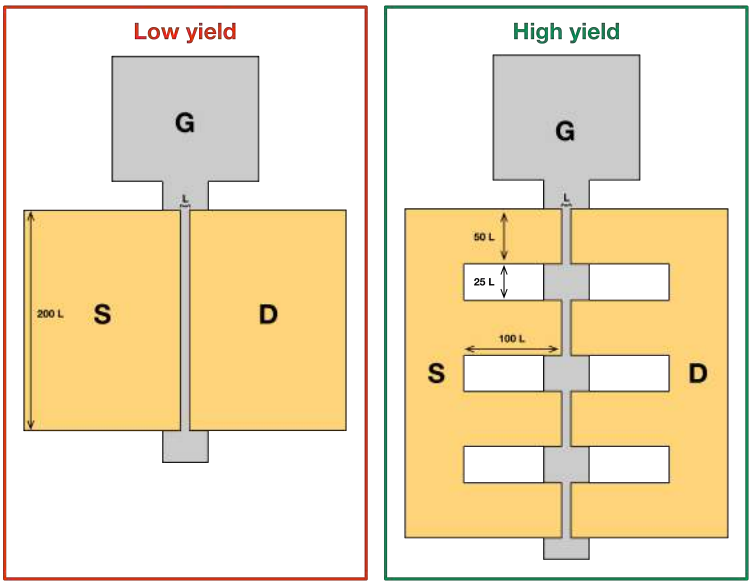
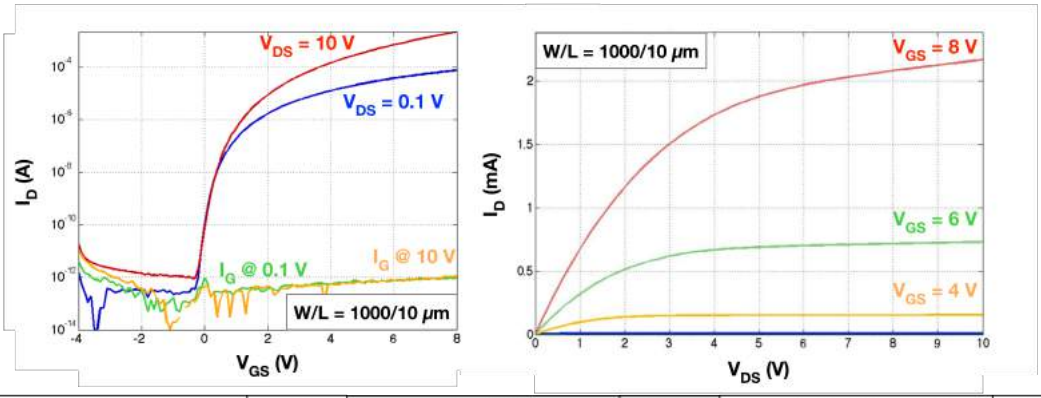


Figure 3.28: Fortifying the narrow piece of photoresist covering the TFT channel with large support posts (right) dramatically increases yield of wide TFTs, albeit increasing the overall area occupied by the TFT.



ZnO thickness (nm)	10	μ (cm^2/Vs)	10 - 15	g_m (mS) @ V_{GS} = 8 V	0.8 - 1
Dielectric thickness (nm)	40	V_{TH} (V)	2 - 4	r_0 (kΩ), V_{GS} = 8 V, V_{DS} = 10 V	25
Passivation thickness (nm)	35	SS (mV/dec)	150 - 350	$C_{OV, GD/S}$ (fF/μm)	20

Figure 3.29: Typical passivated TFT process allows in-situ deposition of dielectric, semiconductor, and passivation. All details of fabrication presented in Appendices.

all TFT recipes exhibit device variation, both within each sample and across samples. It is valuable to visually comprehend this variation; for this reason we show 22 TFT curves superimposed in Figure 3.30. Mean and standard deviation for TFTs resulting from this process are supplied in Table 3.6.

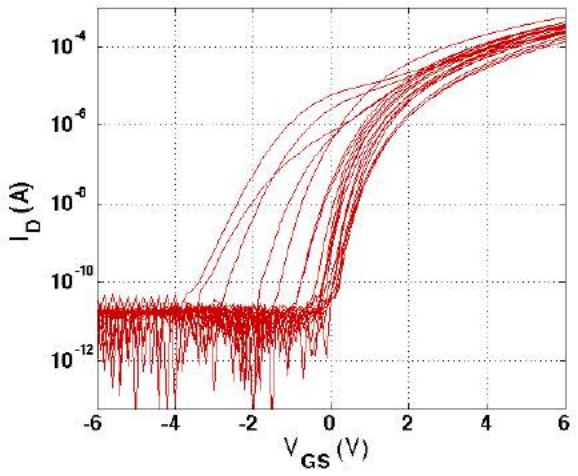


Figure 3.30: I–V curves for 22 ZnO TFTs of W/L = 200/10 μm with V_{DS} = 6 V.

3.4.3 Self-Aligned, In-Situ Passivated TFT Process

As will be discussed at length in the subsequent chapter, for fast circuits, we are interested in minimizing the overlap between the gate metal and the source and drain regions to minimize parasitic capacitance in the TFT. The processes described in the previous two sections rely on manual (i.e., visual, under an optical microscope) alignment of the gate to the source and drain, so the overlap region is typically made large (minimum 5 μm). Furthermore, when ported to a flexible substrate, this overlap region becomes essential to accommodate for thermal expansion and contraction of various layers during processing, and an overlap of 15 μm is required.

Self-aligned processes aim to eliminate this overlap with various lithographic techniques. We developed our own self-aligned process that is also compatible with the in-situ passivation from the previous section. As in previous self-aligned procedures (e.g., [176, 177]), this process utilizes a back-side exposure, where the gate metal acts as a mask for the channel region – this approach ensures very small overlaps even on plastic substrates. In our case, the optical transparency of the oxide layers in the TFT make backside alignment rela-

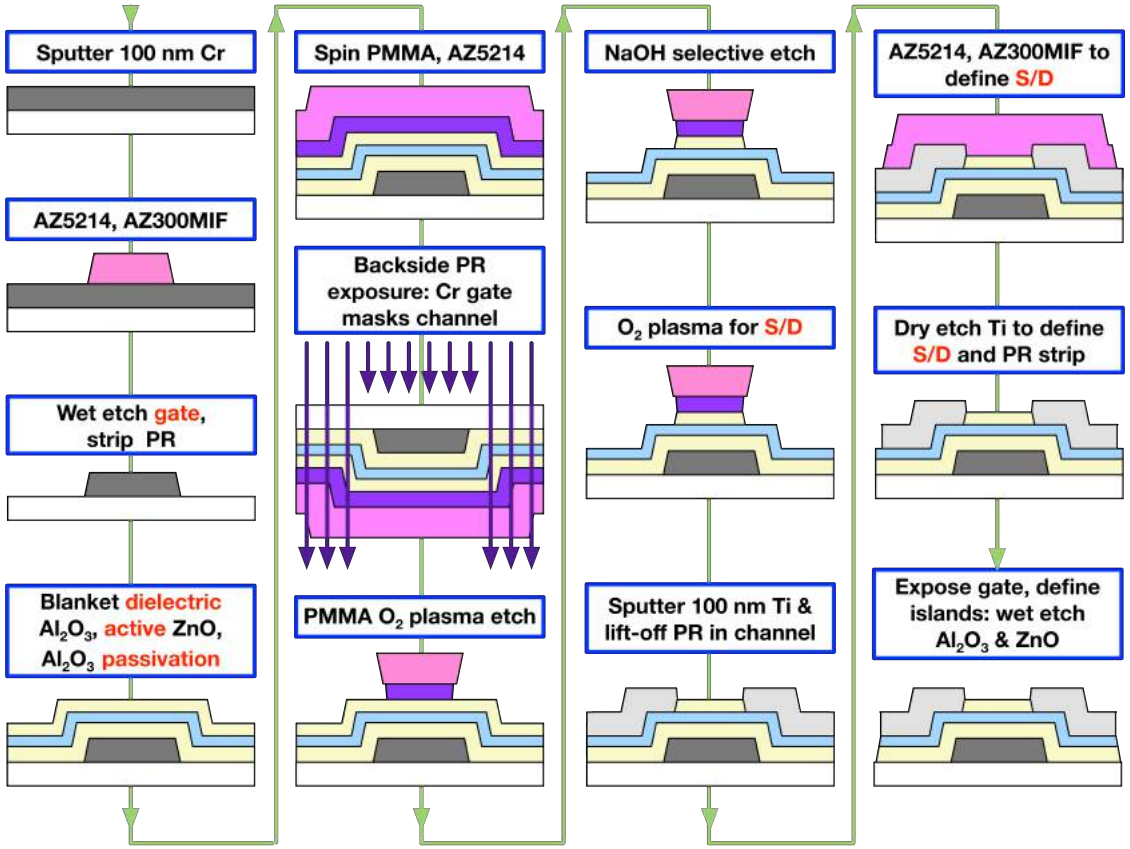


Figure 3.31: Typical in-situ passivated, self-aligned TFT process minimized overlap capacitances and simultaneously protects ZnO back channel. All details of fabrication presented in Appendices.

tively straightforward: exposure time is only increased by 25% compared with the standard procedure. The full process is shown in Figure 3.31 and further detailed in the Appendices.

As seen in the microscope image in Figure 3.32a, the physical overlap dimension X_{OV} of our self-aligned TFTs is reduced to $\sim$ 600 nm, essentially eliminating the parasitic overlap capacitance. The SEM image in Figure 3.32b confirms this overlap; the ridge seen corresponds to the Ti source extending over the top passivation covering the channel. Representative I–V curves for self-aligned ZnO TFTs are provided in Figure 3.33. Extracted mobility is 10 – 15 cm^2/Vs, threshold voltage is 3 V, subthreshold slope is 200 mV/decade, and hysteresis is negligible. We note that contact resistance for self-aligned TFTs is the same as contact resistance for standard TFTs.

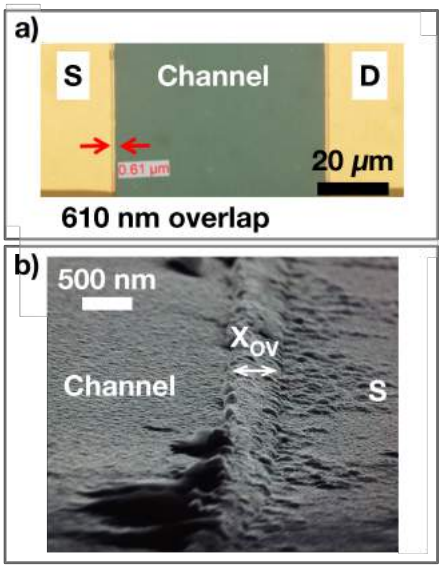


Figure 3.32: Optical microscope and SEM images of the overlap region in self-aligned ZnO TFTs indicates an X_{OV} dimension of 500 – 610 nm.

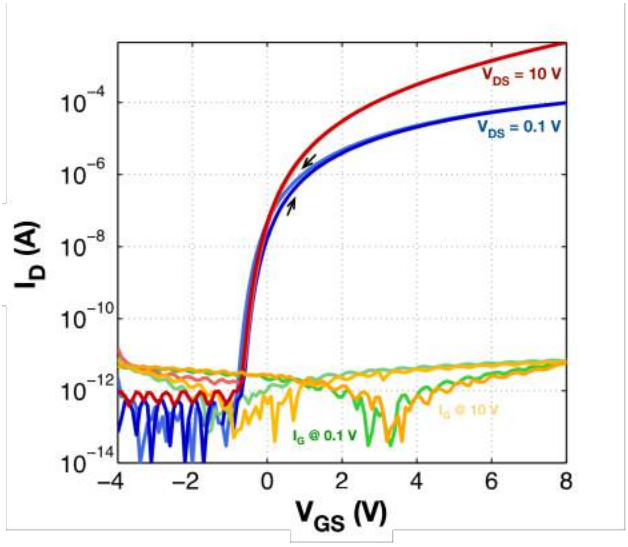


Figure 3.33: Typical I-V characteristics at V_{DS} of 0.1 and 10 V for self-aligned TFTs. W/L = 800/60 μm.

3.5 TFTs on Plastic

While TFTs are made most often on glass substrates, because process temperatures are kept below 200°C, it is relatively straightforward to move these processes to plastic substrates.

In this thesis, we build ZnO TFTs on 50-μm-thick freestanding polyimide foil and on 3.5-μm-thick polyimide that is spin-cast and cured on a silicon carrier before release. Although freestanding polyimide foil has a very rough surface with bumps 150 nm high (profile shown in Figure 3.34, from [43]), we note that the PEALD process results in devices with similar performance to TFTs on glass, suggesting that the effect of the uneven surface profile is reduced by the conformal deposition of the oxide layers. A comparison of extracted parameters for TFTs on glass, freestanding polyimide, and spin-cast polyimide is provided in Table 3.6. Representative I–V characteristics for TFTs on glass and polyimide can be seen in Figure 3.35.

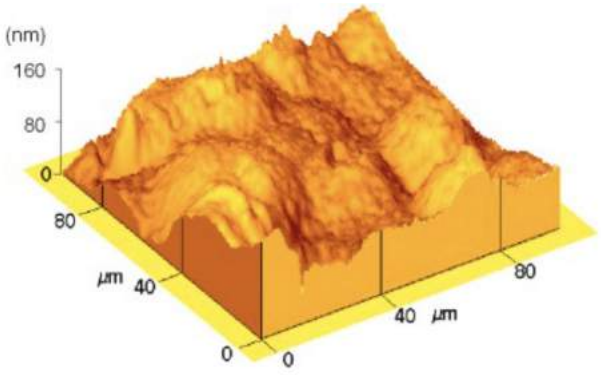


Figure 3.34: Surface of the inner side of a roll of Kapton-E film, as measured by. Prof. Cheng's thesis [43]

3.5.1 Process

For TFTs on plastic, two main process changes must be made for TFT fabrication. First, clean substrates contain moisture, which must be outgassed prior to gate metallization. We outgas in vacuum at 200°C (8 hours for thick polyimide, 2 hours for thin polyimide), then immediately transfer substrates to the metallization chamber. Second, because the compliant substrate is subject to mechanical strain during and after processing, it is essential to replace the brittle Cr gate metal with a composite Cr-Al-Cr gate metal. The first layer of Cr (in contact with the polyimide) serves as an adhesion promoter, and can be as thin as 5 nm. The

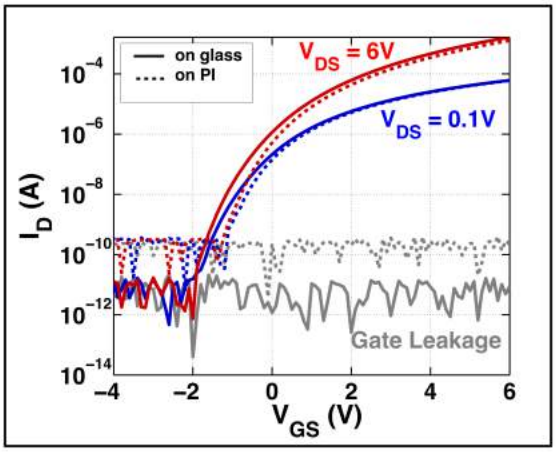


Figure 3.35: TFT transfer characteristics for V_{DS} of 0.1 and 6 V for devices on glass (solid) and 3.5-μm polyimide (dashed) after delamination. W/L = 500/5 μm.

intermediate aluminum layer has a Young's modulus about 1/4 that of Cr – hence, it serves as a conductive, mechanically compliant layer far more robust to cracking than Cr. This layer provides an additional benefit of high conductivity – Al is about 10× more conductive than Cr, which we exploit later on in this thesis. This Al layer, depending on application, is made 50 – 200 nm thick. The third layer of metal is again Cr, which will be the surface exposed to chemical processing and plasma deposition at elevated temperature – once again, we use Cr here because it is a refractory metal. This Cr layer should be at least 20 nm thick, or the underlying Al will migrate under the thermal stress induced by PEALD and form hillocks that puncture the Al_2O_3 dielectric.

Table 3.6: Extracted ZnO TFT parameters on different substrates

	Glass	**50-μm PI**	**3.5-μm PI**
μ (cm^2/Vs)	13.4 ± 2.0	8.3 ± 1.1	11.3 ± 1.2
V_T (V)	2.0 ± 0.4	2.9 ± 0.2	2.2 ± 0.3
C_{GD}/W (fF/μm)	10	30	10
X_{OV} (μm)	5	15	15

To process TFTs on freestanding polyimide (Dupont Kapton-E), we temporarily affix the substrates to glass carriers using the surface tension provided by a few drops of water.

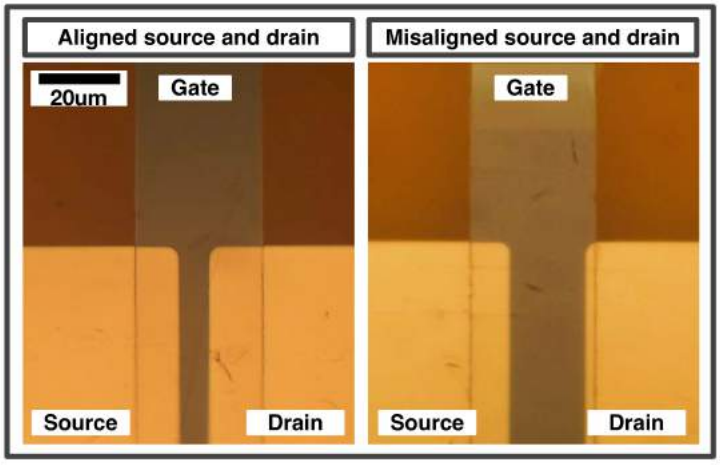


Figure 3.36: Because of expansion and contraction of the polyimide substrate during processing, gate-source/drain overlaps X_{OV} on freestanding 50-μm-thick polyimde must be made large. Even the 10 μm overlaps shown here are problematic, resulting in well-aligned devices (left) and poorly aligned devices (right) in different parts of the same sample [44].

This bond is sufficient for lithographic alignment and UV-exposure, but the substrate will delaminate from the carrier as soon as it is immersed in developer or other liquids. As mentioned, freestanding substrates expand and contract during processing. This requires that the overlap dimension X_{OV} be made large (15 μm) to enable alignment over a 4" substrate (see Figure 3.36).

For spin-cast polyimide substrates, one layer of PI2611 is spin cast using onto a solvent-cleaned silicon wafer with a native oxide. Because this polyimide precursor is extremely viscous, the ramp rate for spin coating must be very gradual or the resulting surface will be uneven. The substrates are baked briefly on a hotplate before being placed in nitrogen oven to cure at 350°C for 3 hours. A full recipe for thin polyimide substrates is provided in the Appendices, and is based on the process in [178].

Processing TFTs is then straightforward – the adhesion of the polyimide to the silicon carrier wafer is sufficiently strong that the two remain bonded throughout the fabrication process. Because substrate-carrier adhesion is strong, the substrate is also unable to expand and contract during processing; this allows us to build TFTs with small gate-source/drain

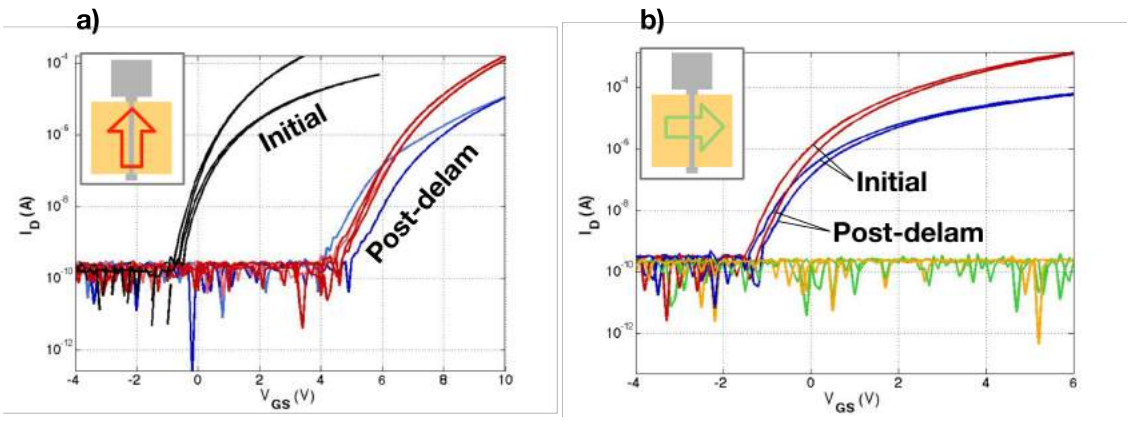


Figure 3.37: (a) Mechanical peeling along the channel width results in a +5 V I–V curve translation, (b) peeling along the channel length results in a +170 mV curve translation. W/L = 500/5 μm, V_{DS} = 0.1 and 6 V.

overlaps X_{OV}, as on glass (5 μm). After fabrication, TFTs are delaminated mechanically by defining a cut in the PI with a razor blade and gently peeling the substrate from the carrier. Delamination should proceed laterally across the TFT, from source to drain; delamination along the gate axis results in severe degradation of the I–V characteristic, as seen in Figure 3.37. For applications where easier delamination is desired, a gold layer can be grown on the carrier surface prior to spin-coating with PI2611.

Because the oxide layers we grow are quite thin and are deposited at low temperatures, they do not impart enough strain to the surface of the polyimide substrate to result in curling, as seen in amorphous silicon TFTs on polyimide where layers are 10× thicker. In amorphous silicon TFTs, a silicon nitride layer is grown on the top and bottom surfaces of the polyimide to compensate for this strain build-up; while we can omit this step for ZnO TFTs, there may be some benefit to growing a thicker layer of Al_2O_3 on the polyimide surface to prevent moisture absorbed by the substrate from seeping into the active area. Since we did not encounter this problem in this work, we have not explored this direction here.

3.5.2 Mechanical Limits of Flexible TFTs

In addition to electrical characterization, it is useful to characterize mechanical behavior of TFTs fabricated on flexible substrates. In particular, defining the maximum strain TFTs can endure before the onset of irreverseable performance degradation is of practical value – once this information is known, applications for flexible TFTs can be identified.

For very thin materials on thin, compliant substrates, uniaxial strain can be applied in a straightforward way by bending materials of interest around cylinders of decreasing radius. The strain on the top surface of the substrate can then be estimated by Equation 3.8 [179]:

$$\left(\frac{d_f + d_s}{2R}\right)\left(\frac{1 + 2\eta + 2\chi\eta^2}{(1+\eta)(1+\chi\eta)}\right) \tag{3.8}$$

where d_f, d_s are the film and substrate thicknesses, R is the bending radius, $\eta = d_f/d_s$ (the ratio of film-to-substrate thicknesses), and $\chi = Y_f/Y_s$ is the ratio of the Young's moduli of the film and the substrate.

To establish the strain limits of TFTs on flexible substrates, TFTs were bent into cylinders of decreasing radius in both convex (with the TFT on the outer surface of the substrate) and concave (with the TFT on the inner surface of the substrate) configurations, with the TFT channel length perpendicular to the axis of the cylinder, as shown in Figure 3.38. The convex configuration corresponds to the application of tensile strain, while the concave configuration corresponds to the application of compressive strain.

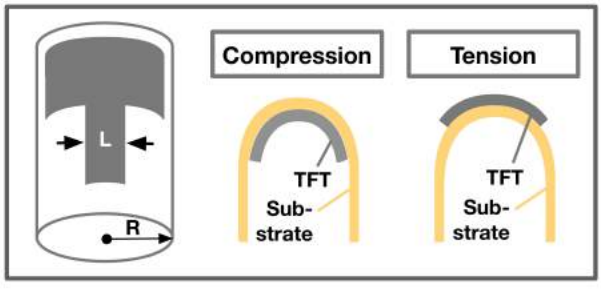


Figure 3.38: Schematic indicating (leftmost) bending direction and (right) cross-sectional views of compressive and tensile strain configurations for TFTs.

For tensile (convex) bending, TFTs were bent around metal drill bits. For compressive (concave) bending, custom plastic half-pipes were laser cut to ensure that the thin TFT layers would not be abraded by contact with a drill bit surface, and TFTs were curled inside the half-pipes. Current–voltage sweeps were performed before and after the strain was applied to the TFTs: the TFTs were measured initially, bent to the desired radius, flattened, and then measured again.

Thin-film transistors on 50-μm-thick, freestanding polyimide foil exhibit electrical changes when bent around cylinders of decreasing radius in both tension and compression. The percent change in mobility and threshold voltage as a function of inverse bending radius (= curvature) is plotted in Figure 3.39. We see that the extracted mobility steadily reduces in both tensile (blue) and compressive (red) cases and that the threshold voltage increases slightly, even at large bending radii. Even at a bending radius of 3.5 mm in compression, extracted mobility has reduced by about 30% from its initial value. Surprisingly, extracted mobility decreases for both tensile and compressive strain. At the smallest radii (a range of 2–3 mm), the gate dielectric suddenly fails, and catastrophic gate leakage results in total device failure. The TFT W/L was 500 μm/5 μm. Assuming that the TFT thin-film layers have total thickness 300 nm and Young's modulus 100 GPa, and using 5 GPa as the Young's modulus for the polyimide substrate, the TFTs break catastrophically between 0.7% and 1.1% strain in compression and tension, although they show signs of degradation much earlier.

Microscope images of TFTs that failed in tension (left) and compression (right) are shown in Figure 3.40 and suggest that physical damage for bending the TFTs on thick polyimide results in electrical degradation and ultimate device failure. We observe that the transparent 40-nm-thick gate dielectric cracks and flakes off in the immediate vicinity of the 100-nm gate metal step (gray line). In many areas of the sample, the gate metal itself shows significant cracking. These observations indicate that for robust flexible TFTs on freestanding polyimide, the gate metal thickness must be reduced even though this results in

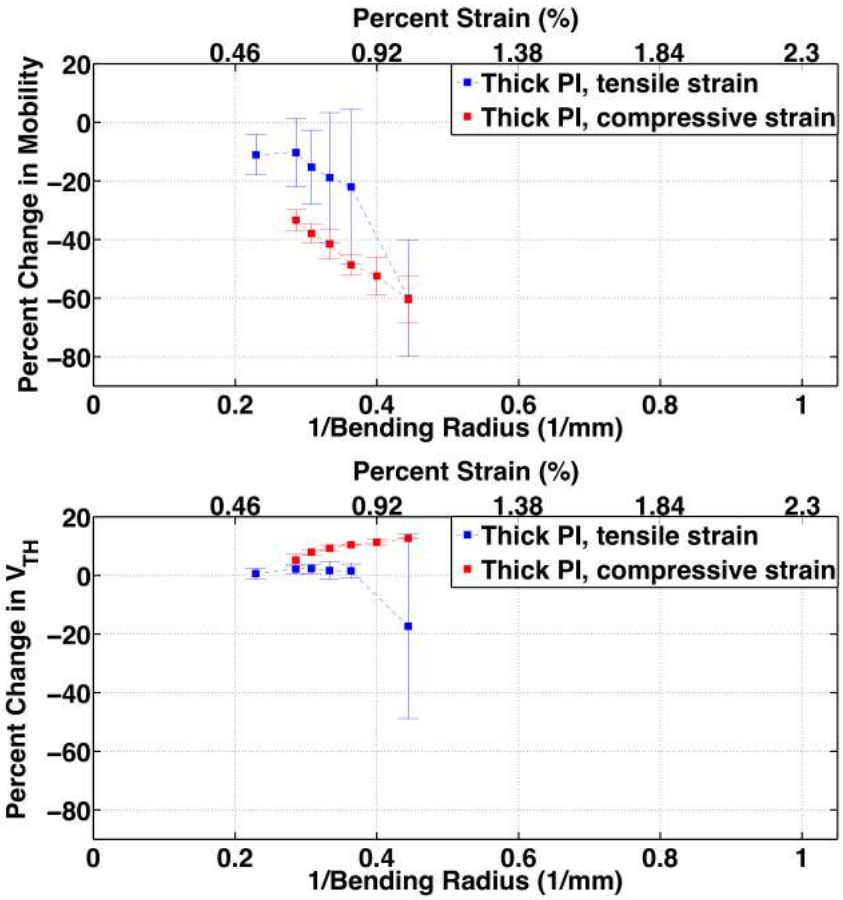


Figure 3.39: Percent change in mobility (top) and threshold voltage (bottom) from initial flat values after application of tensile (blue) and compressive (red) strain for ZnO TFTs on 50-μm freestanding polyimide. Mobility degradation is notable even at a bending radius of 3 mm. For each bending radius and each strain configuration, four TFTs were tested.

increased gate resistance. In these images, we see again the alignment challenge with TFTs on freestanding polyimide, which limits the value of the gate-source/drain overlap X_{OV} to 15 μm.

In contrast, ultrathin spin-cast substrates offer distinct advantages for flexible TFTs, as other works have shown [102, 180]. We demonstrate that for the same bending tests performed on TFTs on freestanding substrates described above, TFTs on ultrathin spin-cast substrates exhibit very little change in mobility or threshold voltage even down to bending radii of 1 mm in both tension and compression, as shown in Figure 3.41. This is different

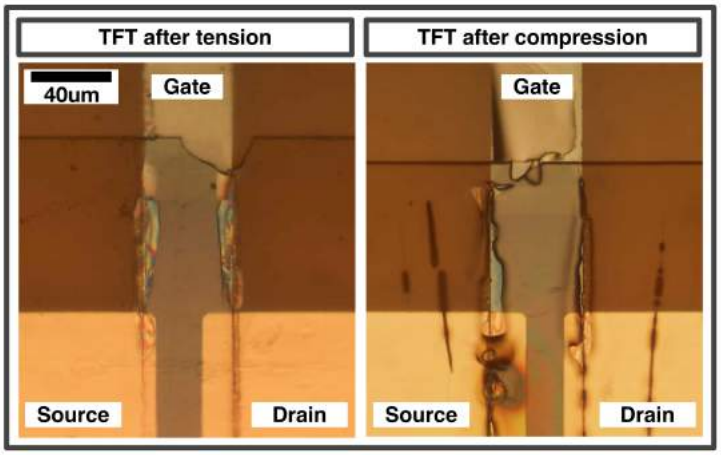


Figure 3.40: ZnO TFTs on 50-μm-thick freestanding polyimide after applying tensile strain (left) and compressive strain (right). In both cases, we observe that the transparent oxide layers crack and flake off, particularly along the gate metal step.

from the result found in [102], which concludes that ZnO is unsuitable for flexible TFT applications.

Strained TFTs on ultrathin substrates furthermore show no visual signs of fatigue. For this reason, we are able to employ a gate metal up to 120 nm thick for TFTs on spin-cast substrates without limiting the bending capability of the TFTs. Because the ultrathin substrates are 3.5 μm thick, the substrate thickness is only about 10$\times$ thicker than the total TFT layer thickness. This reduces the strain experienced by the whole structure. Via Equation 3.8, the strain corresponding to a 1-mm bending radius is only $\sim$0.09%, so it is not surprising that the electrical parameters of the TFT are relatively constant.

Below this radius, testing becomes challenging. "Folding" the substrate on top of itself, directly across a TFT, causes a sharp (but undefined) bending radius $\leq$ 500 μm (Figure 3.42). The TFT characteristics remain unchanged, however, after release of the fold (Figure 3.43), demonstrating the clear superiority of ultrathin substrates for applications in which the substrates must be deformed.

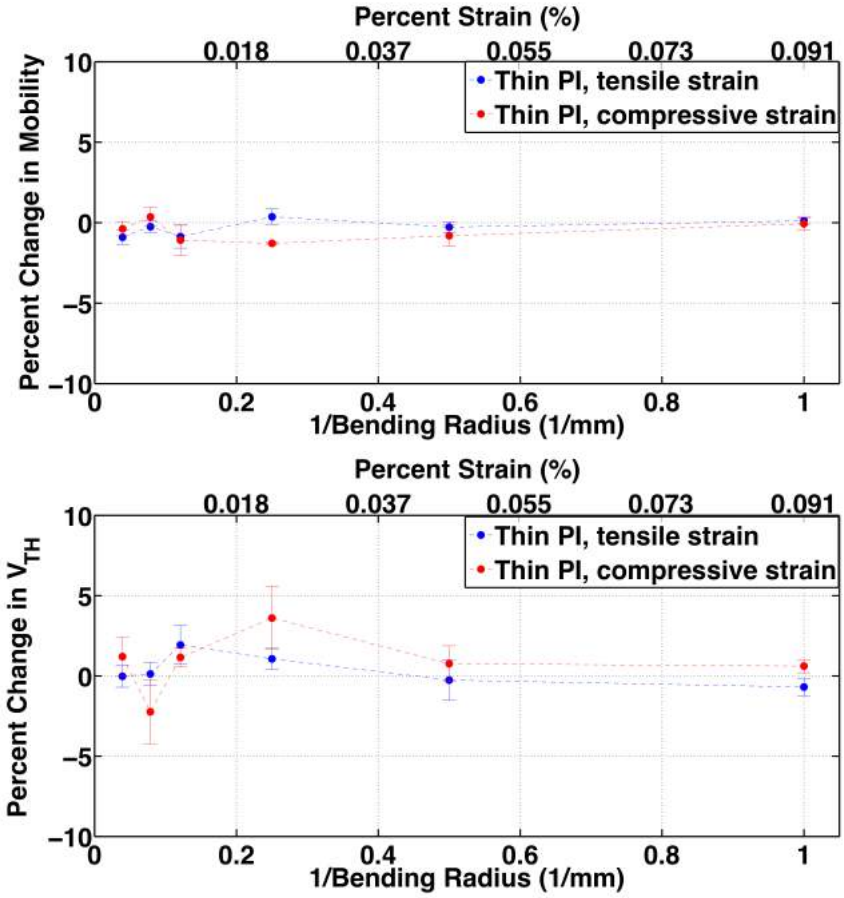


Figure 3.41: Percent change in mobility (top) and threshold voltage (bottom) after application of tensile (blue) and compressive (red) strain for ZnO TFTs on 3.5-μm polyimide. Mobility and threshold voltage change very little down to a bending radius of 1 mm. Each data point corresponds to five TFTs.

3.6 Section Summary

In this chapter, details regarding TFT materials, TFT design, and TFT measurements and anomalous effects were reported. Properties of ZnO and Al_2O_3 deposited in our PEALD were measured, indicating that PEALD produced dense oxides and a polycrystalline ZnO material. Etch recipes for ZnO and Al_2O_3 were developed. Recipes for ZnO TFTs began as simple, unpassivated structures. Instability in atmosphere (and the inability to resuscitate shifted I–V curves with annealing treatments) motivated a transition to a passivated ZnO

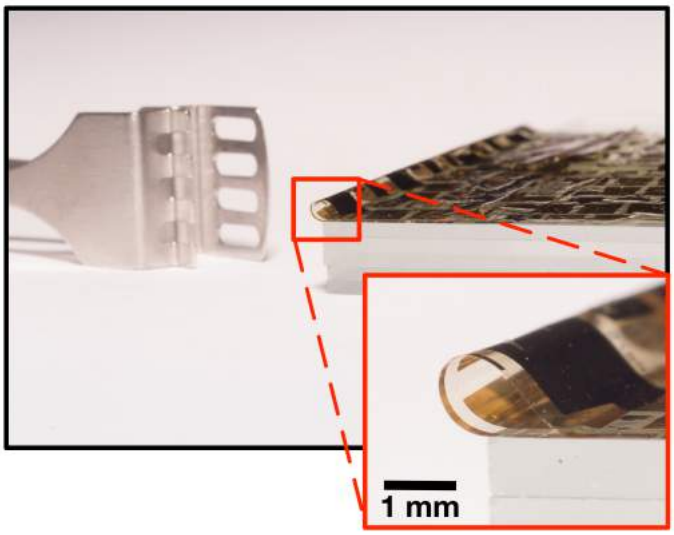


Figure 3.42: ZnO TFTs on 3.5-μm-thick delaminated polyimide folded over itself with TFTs on the inside experience a $\leq$500-μm bending radius but little electrical change. Inset shows fold radius close up.

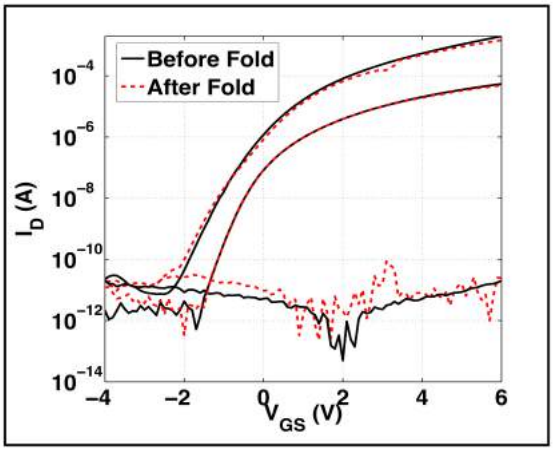


Figure 3.43: TFT transfer characteristics before (black) and after (dashed red) folding in half in compressive configuration. Fold corresponds to a $\leq$500-μm bending radius. Top to bottom: I_D for $V_{DS} = 6$ V, $V_{DS} = 0.1$ V, and I_G.

TFT structure, and I–V changes under heat and light were observed. While a range of passivation materials was explored, ultimately a PEALD passivation performed in-situ, enabled by selective etching techniques, was the most reproducible. A self-aligned structure, with the benefit of low parasitic capacitance, was demonstrated. ZnO TFTs were also fabricated

on plastic substrates, with only small differences compared with TFTs on glass. In addition to electrical characterization of these TFTs, flexible TFTs were subjected to mechanical bending tests to establish strain tolerance. This toolset of reproducible TFT recipes for a range of circumstances now lays a foundation for ZnO TFT circuits, the subject of the next chapter.

Chapter 4

ZnO TFT Circuits

As discussed in Section 1.1.1, ZnO's 10–20× mobility advantage over amorphous silicon promises a significant speed advantage for the circuit blocks used in hybrid sensing systems. Scan circuits, oscillators, and certain amplifier circuits stand to benefit from a speed enhancement – faster scan circuits enable systems with many more sensors and/or signals with higher frequency content, faster oscillators promise efficient inductive transfer of power and/or information, and faster amplifiers can have improved power efficiency. These circuit blocks may also benefit from other properties of the ZnO TFT; for example, its high-quality, conformal ALD dielectric could enable a large gate area for low-noise amplifiers, or enable thicker, lower-resistance gate metallization.

In this chapter, we first introduce TFT metrics relevant for circuit development – the cutoff frequency f_T, the unity-power gain frequency f_{MAX}, and transconductance efficiency – and provide measurements of these parameters for our TFTs. We then discuss development of a model for ZnO TFTs that is used extensively for circuit design. Lastly, for the bulk of this chapter, we describe design and implementation of our demonstrated ZnO circuits: scan circuits and oscillators.

Many group members contributed to the work in this chapter. Warren Rieutort-Louis taught the author to use the Vector Network Analyzer to perform cutoff frequency mea-

surements for amorphous silicon TFTs. Tiffany Moy designed the scan chain discussed in Section 4.3 in amorphous silicon, and provided valuable guidance as the author set about creating an oxide version of this circuit, as well as practical instruction as to how to use the Pattern Generator. For results in Sections 4.4.2, Warren Rieutort-Louis and Liechao Huang, as experts in amorphous silicon oscillators, provided initial guidance for building cross-coupled oscillators; Warren Rieutort-Louis provided amorphous silicon TFTs for the f_T, f_{MAX}, and oscillator comparisons in Sections 4.1 and 4.4.5. Yingzhe Hu helped debug ZnO Colpitts oscillators in Section 4.4.3.

Results from Sections 4.1, 4.3, 4.4.2, 4.4.4, and 4.4.5 were presented by the author at the Materials Research Society Meeting in 2014 and the International Thin-Film Transistor Conference, the International Workshop on Zinc Oxide and Related Materials, the Materials Research Society Meeting in 2015, the Society for Information Display Symposium, and the 15th Annual Flexible and Printed Electronics Conference, respectively [136, 137, 181–184]. Results from Section 4.4.4 were published in the Journal of the Society for Information Display [44].

4.1 TFT Metrics for Circuit Design

4.1.1 The Cutoff Frequency f_T

Circuit designers use a range of metrics to benchmark transistors. Most common among these is the so-called "cutoff frequency" f_T. A more descriptive definition of f_T is the unity current gain frequency. As the MOSFET (unlike a BJT) is a voltage-controlled device, the value of this figure of merit may seem somewhat unclear. While at DC, essentially no current passes through the gate dielectric, at high frequencies, the displacement current into the gate increases, ultimately surpassing the current into the transistor's drain. The cutoff frequency defines the point where the two currents equal, beyond which the transistor fails to produce current amplification.

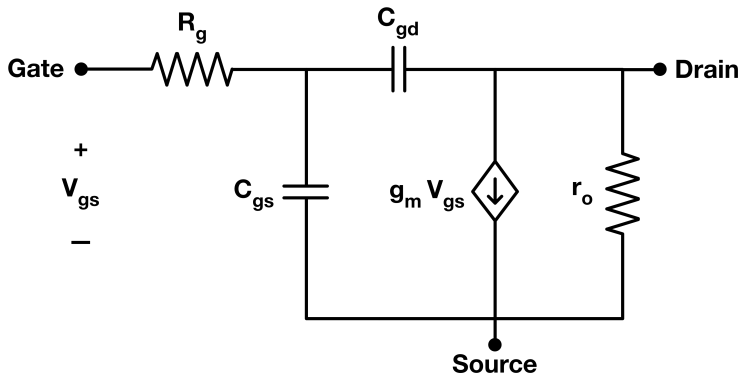


Figure 4.1: The small signal model for a TFT is like that of a MOSFET, but without a body terminal.

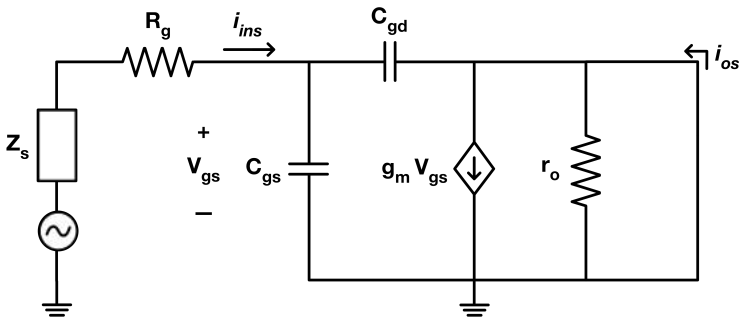


Figure 4.2: To derive f_T, we take the small signal model for a TFT and apply a short at the output. Based on the excellent lecture notes in [185]

An analytical expression for f_T can be derived using the small-signal model (Figure 4.1). The small signal model of the MOSFET can be applied to the TFT by removing the body terminal, and then proceeding with the same analysis.

Recalling that the f_T is defined in the case of an output short and referring to Figure 4.2, we see that the current to the output from the source i_{os} and the current to the input to the source i_{ins} are:

$$i_{os} = g_m V_{gs} - i_{gd} = g_m V_{gs} - sC_{gd}V_{gs} \tag{4.1}$$

$$i_{ins} = sV_{gs}(C_{gs} + C_{gd}) \tag{4.2}$$

The current gain is the ratio of these currents; assuming that $g_m >> sC_{gd}$ gives:

$$A_I = \frac{i_{os}}{i_{ins}} = \frac{g_m - sC_{gd}}{s(C_{gs} + C_{gd})} \sim \frac{g_m}{s(C_{gs} + C_{gd})} = \frac{g_m/(C_{gs} + C_{gd})}{j\omega} \tag{4.3}$$

Setting $\mid A_i \mid = 1$ for unity current gain then leaves us with the well-known expression for f_T:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{4.4}$$

We measure f_T for our ZnO TFTs using a vector network analyzer to perform a two-port measurement; the 0-dB crossing of the H21 curve corresponds to the f_T. A schematic and photo of the measurement setup is shown in Figure 4.3. A f_T measurement at the maximum suggested bias point for this technology is provided in Figure 4.4, showing an f_T of 12.8 MHz. The H21 plot derived from a TFT-level Spectre simulation (discussed later in this chapter) is plotted on top in the dashed blue line, showing good agreement.

For a given TFT technology (e.g., for a given mobility), f_T can be enhanced by either boosting transconductance g_m or by reducing capacitance. Transconductance g_m is a function of the gate overdrive voltage $V_{OV} = V_{GS} - V_T$ and channel length L (e.g., $g_{m,sat} = \frac{\epsilon_i \mu W}{t_i L} V_{OV}$) and capacitance is a function of channel length and overlap capacitance (e.g., $C_{gs} + C_{gd} = \frac{\epsilon_i}{t_i} W(L + 2X_{OV})$; hence, we expect to see changes in each of these parameters to be reflected in f_T measurements. In particular, as expected, a reduction in L will have the most dramatic impact on f_T because it is represented in both g_m and C. By expressing f_T slightly differently we can see this directly:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{\mu(V_{GS} - V_T)}{2\pi L(L + 2X_{OV})} \tag{4.5}$$

We can see the impact of both L scaling and overlap capacitance reduction on cutoff frequency in Figure 4.5. In blue, we we see HF measurements of standard ZnO TFTs with a large overlap dimension ($X_{OV} = 15$ μm) compared with f_T calculated from measured values of $g_m/2\pi C_T$ for the same TFTs, where g_m is measured from the DC I–V curve, and C_T (the

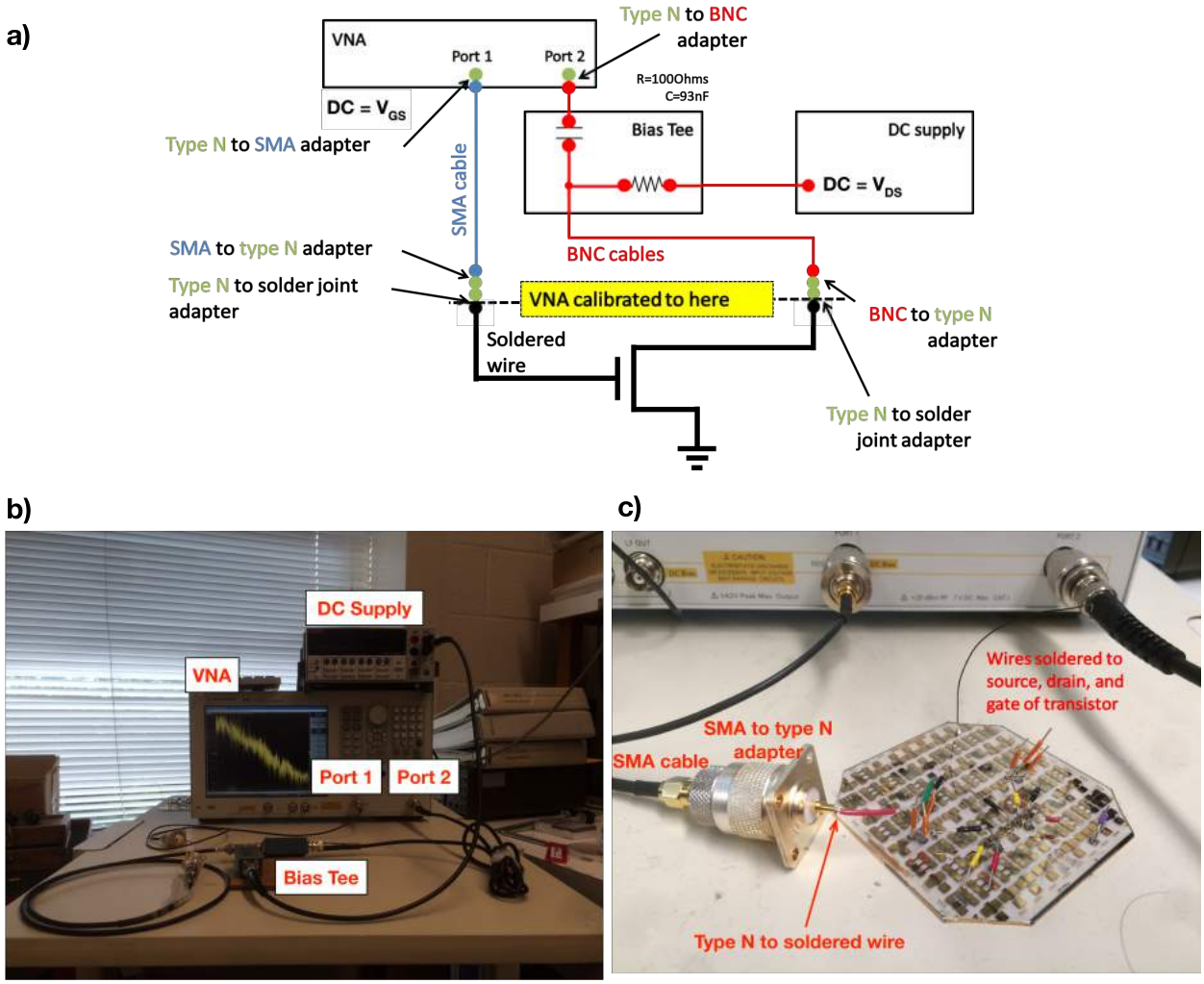


Figure 4.3: Schematic (a) and photograph (b) of the setup we use for high-frequency measurements. Parasitics are calibrated out using a full-two port calibration up until the solder joint shown in (c).

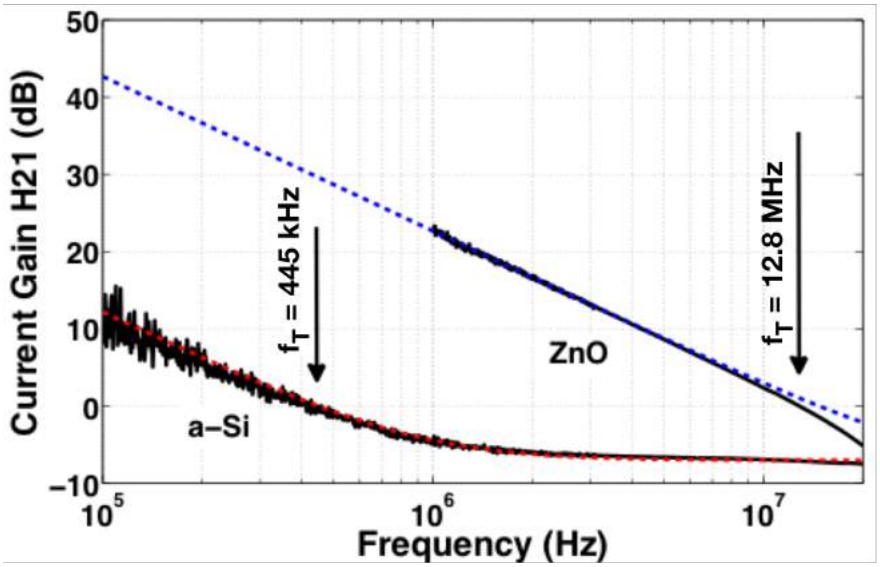


Figure 4.4: H21 measurements from a ZnO TFT (L = 5 μm, X_{OV} = 5 μm) biased at a $V_{GS} = V_{DS}$ =9 V, the highest recommended bias point for this technology. Simulated H21 plot for ZnO TFTs shown in blue. The 0 dB crossing shows the f_T is 12.8 MHz. For comparison, a measured for our standard amorphous silicon TFT (L = 6 μm, X_{OV} = 15 μm) at its standard bias point $V_{GS} = V_{DS}$ =12 V is shown (with α-Si simulation in red also shown), illustrating the benefit of metal oxide TFTs.

total TFT capacitance) is measured in a standard C–V sweep at the same bias points used in the HF measurement. The two are largely in agreement. The expected increase from reducing channel length from 30 μm to 10 μm for these TFTs (using Equation 4.5) is 4.5 – which is in agreement with what is measured. Because a self-aligned process minimizes X_{OV} for a given channel length, it is also an effective tool for f_T maximization, as seen in the red curves. For L = 30 μm, eliminating the overlaps halves the capacitance, and (via Equation 4.5) should double f_T – which once again agrees well with what is measured. While f_T does not exhibit a dependence on channel width W, we note that all TFTs measured have the same W/L.

Lastly, we can see the effect of overdrive voltage on f_T in Figure 4.6, which plots f_T calculated from I–V measurements (at DC) and capacitance measurements versus overdrive voltage. We note that while the dependence is expected to be linear (from Equation 4.5), in our case we typically see a superlinear dependence because of self-heating effects. For this

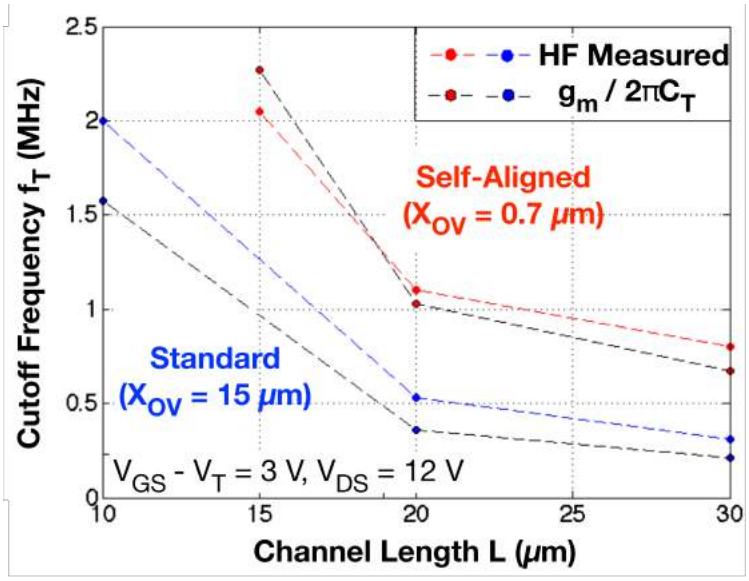


Figure 4.5: Impact of channel length and gate-source/drain overlap dimension on cutoff frequency.

reason, solid curves in Figure 4.6, extracted from pulsed I–V measurements, are linear at low drain bias, while dashed curves, extracted from continuous I–V plots, are highly nonlinear. We have shown f_T derived from I–V and C–V measurements in this case because the HF measurement setup (VNA) does not allow for pulsed application of the gate bias, and hence we cannot decouple HF f_T measurements from self-heating effects.

Because f_T is a relatively unambiguous metric that is readily measured, it has become a very popular metric of comparison between technologies. However, it is important to acknowledge that the cutoff frequency defines only a first-order upper limit for most circuits. In practice, device parasitics not included in this simple small signal model further reduce this frequency, limiting circuit operation to frequencies far below f_T. Another serious drawback of f_T as a primary HF metric is that, because it is defined for the case of infinite output conductance, is fails to account for input resistances of the transistor. Hence, it can be the case that a high-f_T transistor cannot provide useable power gain near f_T. To address this failure of f_T as a metric, it is important to consider another high-frequency metric simultaneously: f_{MAX}.

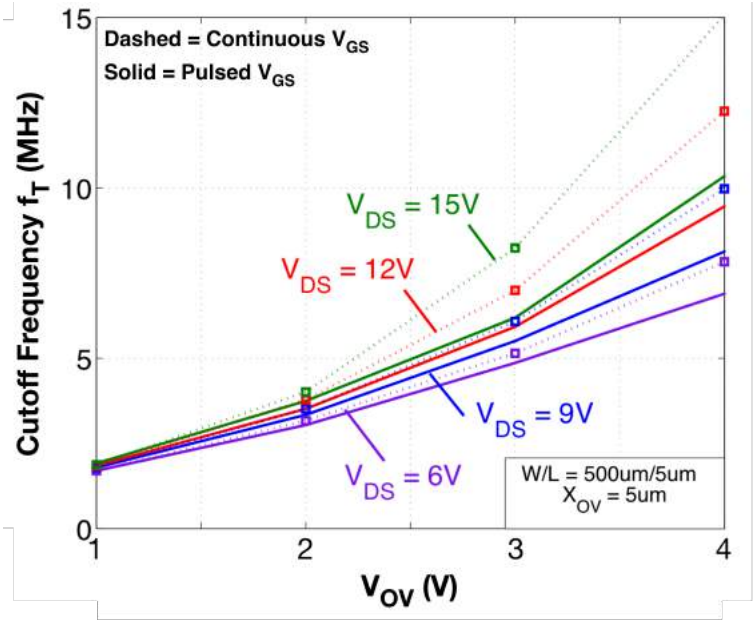


Figure 4.6: Impact of gate bias on cutoff frequency. Self-heating effects are evident when gate bias is applied continuously through sweep (dotted lines), resulting in apparent super-linear dependence of f_T on V_{OV} that largely disappears when gate bias is intermittent (solid lines). Because drain bias also increases heating, the effect is more pronounced at high V_{DS}. Because the HF measurement setup does not allow for pulsed application of the gate bias, these f_T values are calculated from DC I–V measurements and C–V measurements according to Equation 4.4.

4.1.2 The Unity-Power Gain Frequency f_{MAX}

While f_T presents an upper bound for high-frequency operation of most circuits, it is also possible to build circuits that operate above f_T; one strategy is to tune out parasitic transistor capacitances via resonant circuit topologies. These circuits are limited by f_{MAX}, defined as the unity-power gain frequency (f_{MAX} is also commonly known as the maximum oscillation frequency, because it is the maximum frequency at which at transistor can oscillate with passive feedback). Although device capacitances can be tuned out by using an appropriate inductance, because f_{MAX} depends on other TFT parasitics not included in f_T, it is possible for f_{MAX} to be below or above f_T, depending on device design.

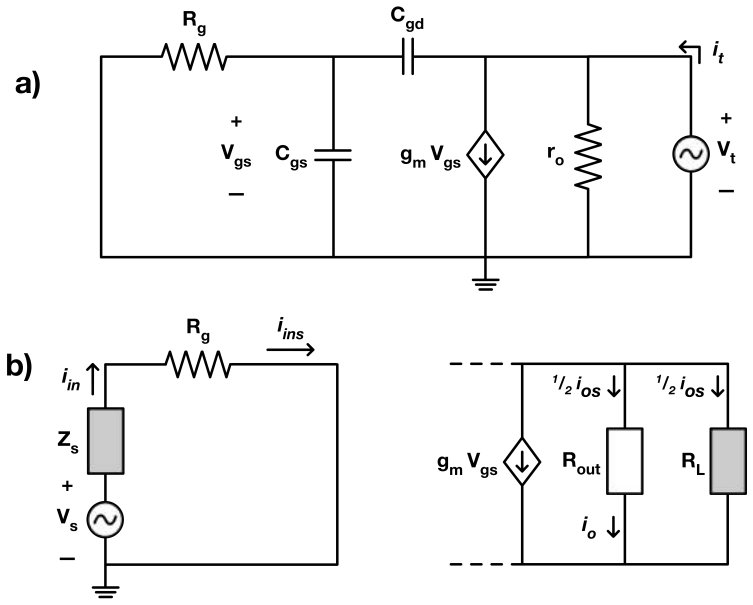


Figure 4.7: To derive f_{MAX}, we look at the small signal model for a TFT. In (a) V_t and i_t are Thevenin voltage and current. In (b), which shows input (left) and output (right) conjugate matching, Z_s and V_s are the source impedance and voltage. Figure is based on the excellent lecture notes in [185]

To derive an analytical expression for f_{MAX}, we return to the small signal model. For maximum power transfer, the input and output ports must be conjugate matched. First, the input and output impedance are determined (from Figure 4.7a) to be:

$$Z_{in} = R_g + \frac{1}{j\omega C_{gs}} \sim R_g \tag{4.6}$$

$$Z_{out} = \frac{1}{\frac{1}{r_o} + \frac{g_m C_{gd}}{C_{gd}+C_{gs}}} \tag{4.7}$$

Next, input and output are conjugate matched in accordance with Figure 4.7b:

$$Z_s = R_g \Rightarrow i_{in} = i_{ins} = V_s/2R_g \tag{4.8}$$

$$R_L = R_{out} \Rightarrow i_o = i_{os}/2 \tag{4.9}$$

We can then define the power gain G_p:

$$G_p = \frac{\frac{1}{2}i_o^2 R_{out}}{\frac{1}{2}i_{in}^2 R_{in}} = \frac{1}{4}\left(\frac{i_{os}}{i_{ins}}\right)^2 \frac{R_L}{R_g} = \frac{1}{4}\left(\frac{f_T}{f}\right)^2 \frac{R_L}{R_g} \tag{4.10}$$

So, for $\mid G_p \mid = 1$, $f = f_{MAX} = \frac{1}{2} f_T \sqrt{\frac{R_L}{R_g}}$. Subbing in our expressions for R_L and f_T, this yields our final expression for f_{MAX}:

$$f_{MAX} = \frac{1}{2} \frac{f_T}{\sqrt{2\pi f_T C_{gd} R_g + \frac{R_g}{r_o}}} \tag{4.11}$$

We note that in most cases, $r_o >> R_g$, such that the last term in the denominator can be ignored.

To measure f_{MAX}, we use a vector network analyzer configured as shown previously and measure the maximum available power gain (MAG). The 0-dB crossing of the MAG curve provides the f_{MAX}. Measurements of f_{MAX} for standard ZnO TFTs at the maximum recommended bias point are provided in Figure 4.8, with measured data in black and the result simulated in Spectre in blue. At these high frequencies, there is some small discrepancy, with measurement showing an f_{MAX} of 34 MHz, while simulation shows an f_{MAX} of 40 MHz, suggesting that there could be some parasitics in the measurement setup that remain uncalibrated. Later in this chapter we describe the operation of ZnO TFT circuits $>$ 34 MHz; this fact also points to a slightly higher f_{MAX} than what is measured.

In Equation 4.11, we see that the expression for f_{MAX} exhibits dependence on f_T, so reduction in channel length is expected to also enhance f_{MAX}, although this dependency is less clear than in the case of f_T. This is seen in Figure 4.9, which plots measured f_{MAX} as channel length is reduced.

Similarly, other TFT optimizations that benefit f_T, like reducing C_{gd}, will also enhance f_{MAX}. However, present in the expression for f_{MAX} (Equation 4.11) is also a new, explicit dependence on the gate resistance R_g. Because this parameter – unlike mobility, threshold voltage, channel length, and capacitance – is not considered by the metric f_T, it is typically

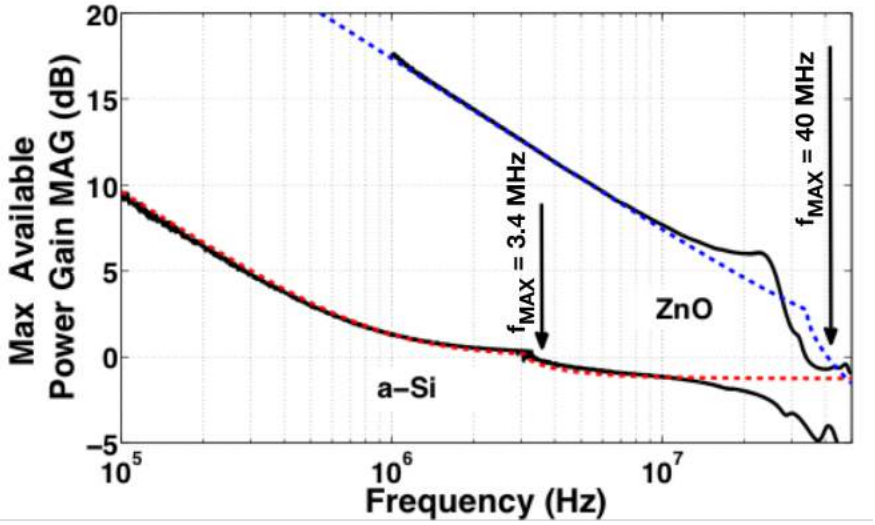


Figure 4.8: Maximum available power gain (MAG) measurements from a ZnO TFT ($L = 5$ μm, $X_{OV} = 5$ μm) biased at a $V_{GS} = V_{DS}$ =9 V, the highest recommended bias point for this technology. The 0 dB crossing shows the f_{MAX} is 34 MHz for the measurement, and 40 MHz for the simulation (in blue). For comparison, a plot for a standard amorphous silicon TFT ($L = 6$ μm, $X_{OV} = 15$ μm) at its standard bias point $V_{GS} = V_{DS}$ =12 V is shown (along with α-Si simulation, in red), illustrating the benefit of metal oxide TFTs.

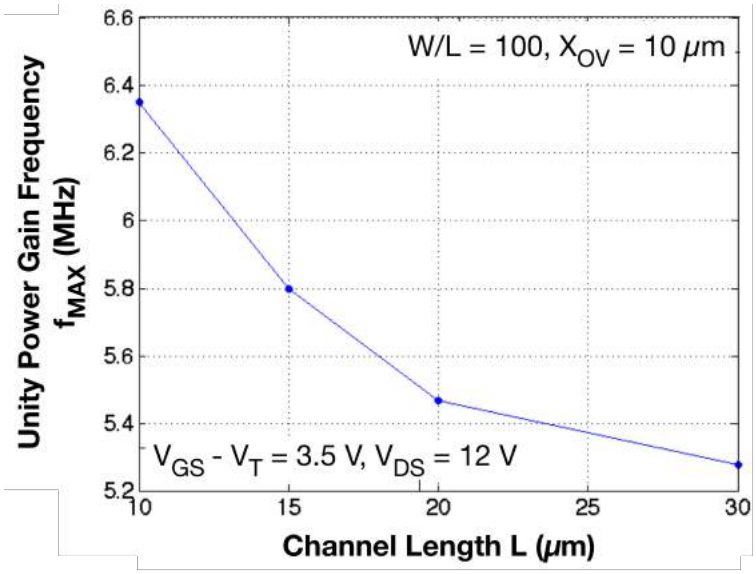


Figure 4.9: Reducing channel length increases measured f_{MAX} for ZnO TFTs, as expected. Note these TFTs have large overlap X_{OV} and lower overdrive voltage than the measurement in Figure 4.8.

ignored by TFT developers. We find gate resistance optimization to be a very straightforward and powerful tool for f_{MAX} enhancement.

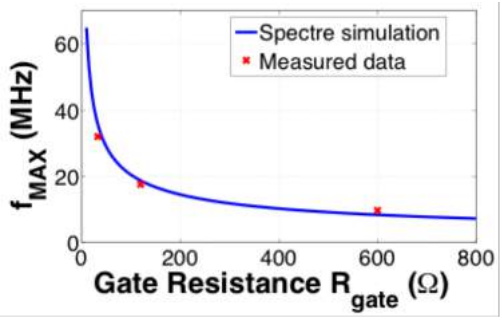


Figure 4.10: Gate resistance can be reduced 20 × by switching to a composite Cr/Al/Cr gate, significantly enhancing f_{MAX} for identically sized devices (W/L = 500 / 5 μm and X_{OV} = 5 μm, $V_{GS} = V_{DS}$ = 6 V).

We reduce the gate resistance in our non-self-aligned TFTs by introducing an aluminum layer into the otherwise Cr gate metal, and gradually increasing its thickness, as we have done for TFTs on plastic (discussed in Section 3.5.1). We can see the effect of this gate resistance reduction in Figure 4.10. Aside from the composite material approach used here, wide TFTs can also be broken into "multi-finger"-style gates; this approach is also effective, but results in an increase of overall device area compared to a single-gate device. We note that self-alignment, a boon to f_T, is not as straightforward for f_{MAX} because reducing the overlap dimension corresponds directly to increasing the gate resistance (e.g., for a given W, L, X_{OV}, metal thickness t, and metal resistivity ρ, gate resistance will be reduced from $\frac{\rho(L+2X_{OV})}{Wt}$ to $\frac{\rho L}{Wt}$).

4.1.3 Transconductance Efficiency

As discussed, TFT circuits, due to limited mobility and high operating voltages, consume much more power than CMOS circuits. Transconductance efficiency g_m/I_{DS} is a transistor-level metric that quantifies these differences in power efficiency between TFT and CMOS technologies. In particular, transconductance efficiency describes the TFT current (and by

extension, power expenditure) required to achieve a level of transconductance; since circuit designers focus on transconductance as a performance metric rather than mobility, this is in effect a performance – power ratio.

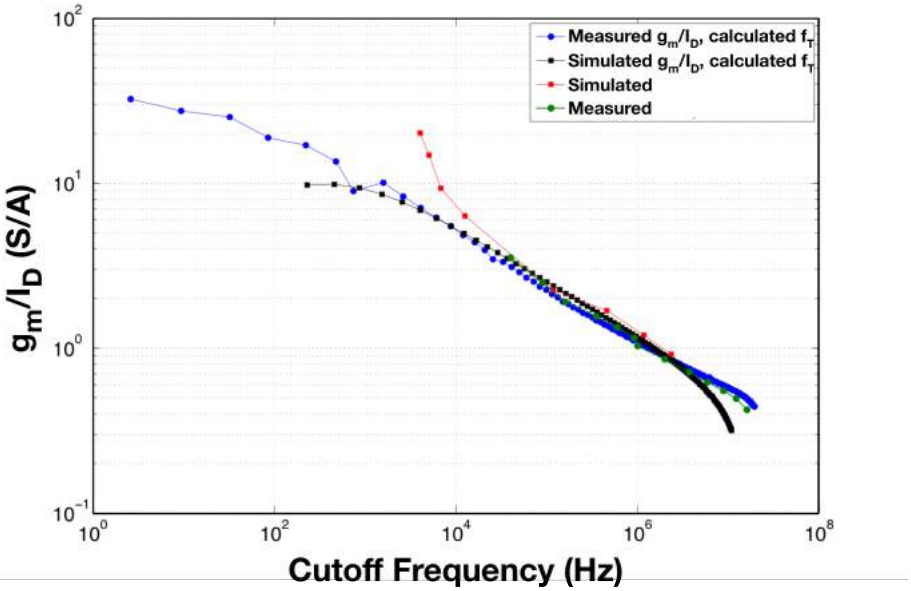


Figure 4.11: Transconductance efficiency for ZnO TFTs versus cutoff frequency f_T; at each point, the gate bias on the TFT changes. TFT dimensions are W/L = 500 / 5 μm and X_{OV} = 5 μm.

It is important to note that transconductance efficiency is actually highest in the subthreshold regime, for all transistor technologies. In TFTs, this value is 1 – 20 V^{-1} in subthreshold, while in CMOS it is about 40 V^{-1}. While the CMOS transistor will vastly outperform the TFT in transconductance efficiency as the applied bias is increased and the TFT (or CMOS transistor) is driven into stronger accumulation (inversion), the interesting possibility remains of building TFT circuits (for instrumentation etc.) that have energy-efficiency quite close to CMOS counterparts, as long as the TFTs are operated near subthreshold. So long as the bias point can provide sufficiently high-frequency operation for the desired application (e.g., sufficiently high f_T), sub-and/or near-sub-threshold operation presents an interesting TFT circuit design space. Our group has previously taken advantage of this to build chopper-stabilized low-noise amplifiers from amorphous silicon [16]. We have

characterized transconductance efficiency as a function of f_T for ZnO TFTs for future circuit applications that may also wish to take advantage of the above (Figure 4.11). Because the VNA cannot measure frequencies below 100 kHz, we plot simulated results as well at lower frequencies. To account for the possibility of AC simulation errors at low frequencies, we also calculate results based on both measurements and simulations and plot them alongside.

4.2 ZnO TFT Modeling

We have mentioned in passing the existence of a ZnO TFT model, that we use in the previous sections to verify our high-frequency measurements. This model is based on a Level 61 SPICE TFT model (originally developed for amorphous silicon) that uses 28 parameters to approximate DC and AC TFT performance. We are able to adjust these parameters to fit ZnO TFT behavior. While some of these parameters can be directly measured (for example, device capacitances and resistances), other parameters are fitting parameters that must be adjusted to suit the TFTs in question. A full description of the original model, developed at RPI, is available online [186]. Figure 4.12 lists the parameters that we have used with success.

Figure 4.13 demonstrates that this TFT model can accurately mimic both $I_D - V_{GS}$ and $I_D - V_{DS}$ curves of our ZnO TFTs. As shown in the previous sections, we have also verified that this model results in H21 and MAG curves that agree well with experiment, indicating that both DC and AC TFT properties can be accurately described. We use this model extensively as a circuit design tool, typically determining circuit dimensions in simulation prior to designing lithographic masks and fabricating samples.

Some degree of caution should be exercised when working with TFT models. First, the Level 61 model does not accommodate for TFT variation; hence, it may be worthwhile for designers to fit models for best- and worst-case devices to avoid unpleasant surprises. Furthermore, when adjusting parameters, it is important to ensure that new simulations

```
.MODEL ModTFT61ZnO nmos Level=61
+ alphasat = .4 cgdo = 17.5e-9 cgso = 17.5e-9 def0 = 1.11
+ delta = 4.5 el = 0.1 emu = 0.02 eps = 11
+ epsi = 8 gamma = 2.3 gmin = 1e23 iol = 1.5e-13
+ kasat = 0.006 kvt = -0.01 lambda = 0.0001 m = 2.1
+ muband = 0.00030 rd = 142 rs = 142 sigma0 = 2e-14
+ tnom = 27 tox = 4e-8 v0 = 0.8 vaa = 5.8
+ vdsl = 7 vfb = -1.4 vgsl = 7 vmin = .1 vto = 0
```

Figure 4.12: Level 61 SPICE model parameters for ZnO TFTs with $X_{OV} = 10$ μm. For self aligned devices, reduce cgso and cgdo to 1.25e-9.

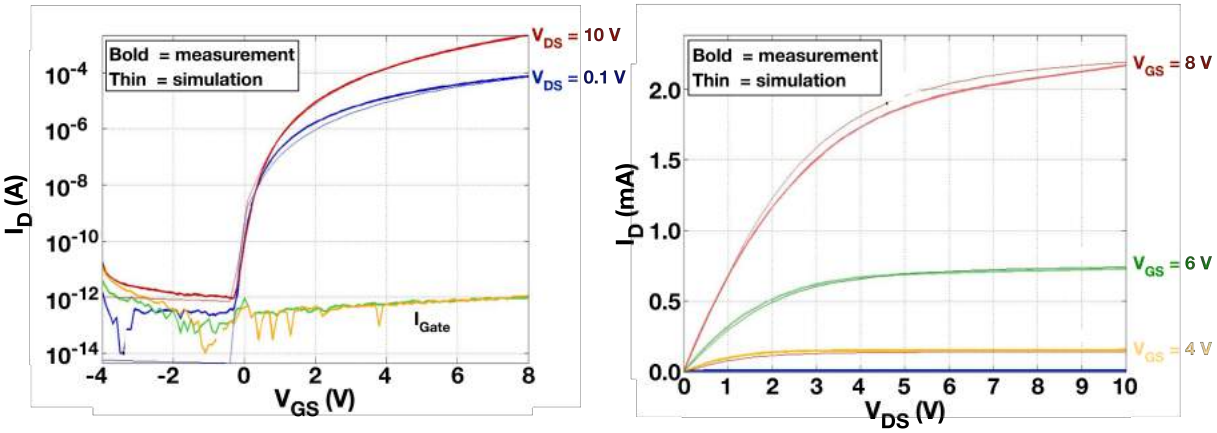


Figure 4.13: Measured current-voltage curves (bold lines) for ZnO TFTs (W/L = 500 / 5 μm) match well with simulated curves (thin lines) across all regions of operation: subthreshold, linear, and saturation.

match all regions of TFT operation, even at high frequency, as there are enough parameters to arrive at similar simulation results (for one type of curve) in multiple ways, not all of which are necessarily accurate. Additionally, model deviations become more pronounced at large biases, as self-heating effects cannot be accounted for accurately within this model. Nonetheless, for providing first-order insight into circuit operation, this model has been an invaluable tool.

4.3 ZnO Scan Circuits

4.3.1 General Considerations

As mentioned, hybrid systems combine strengths from very different technologies– e.g., flexible polyimide sheets with embedded thin film sensors interact with the external world, but rely on a CMOS IC for control and computation of the signals they gather. The scan circuit provides an interface between these two realms, sampling the numerous sensors in the large area domain according to control signals from the CMOS IC.

The scan circuit is a superior interfacing method for hybrid systems compared to direct interconnections or active matrices, mainly because it allows the number of connections to the IC to remain fixed while we scale the number of elements in the large area sensing array. This means we can scale large area systems as needed to suit different applications. A schematic illustrating the scan circuit's role in hybrid systems is shown in Figure 4.14 – as shown, each circuit sends an "ENABLE" signal to access one sensor, and the circuits are strung together into a sequential "scan chain" (Figure 4.15).

However, because the scan chain must sample all of the N sensors in a system, it must operate at a speed equal to the number of sensors N times the sensor bandwidth. Hence, the scan circuit must be the fastest thin-film component of the hybrid system. Faster scan circuits can enable hybrid systems with more and/or higher bandwidth sensors, resulting in richer large-area sensing applications – for this reason, ZnO is a strong candidate material for scan circuit TFTs, compared to amorphous silicon etc.

4.3.2 Implementation

Our group previously reported an amorphous silicon scan circuit that, using three control signals from the CMOS domain, could be scaled to an arbitrary number of sensors without scaling static power consumption [187]. As previously mentioned, a key challenge with LAE TFTs is that they typically present only unipolar devices. In order to preserve full-swing

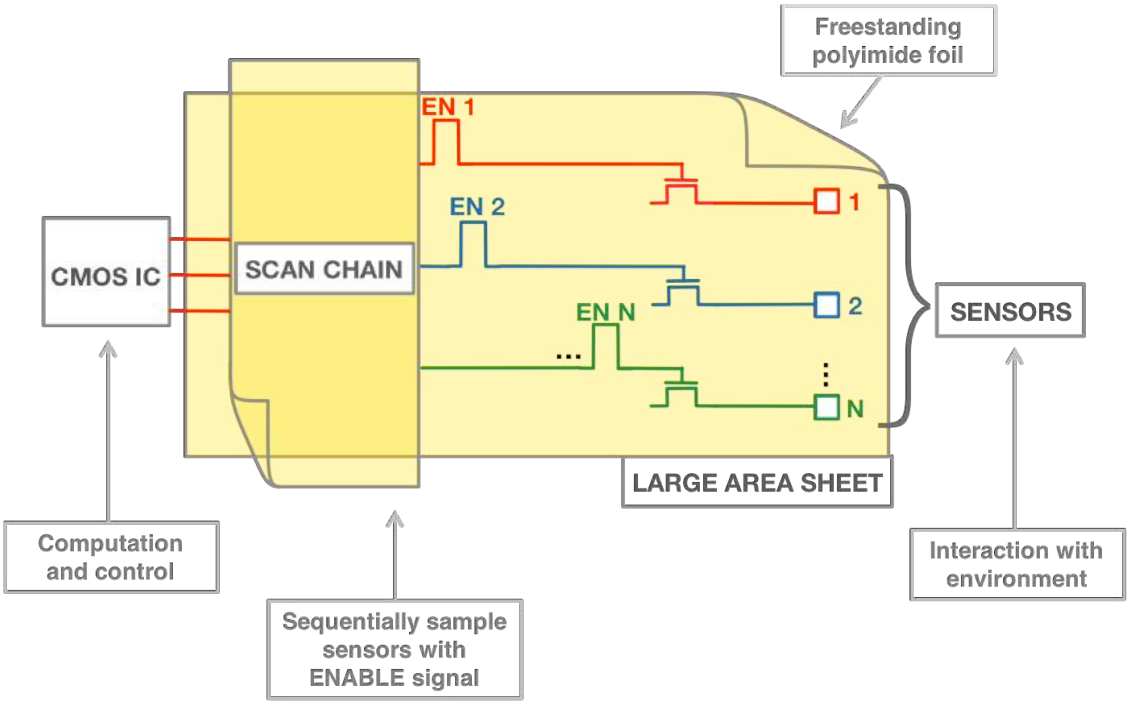


Figure 4.14: Scan circuits take a control signal from CMOS and generate a sequence of signals used to sample from sensors in array. This reduces the number of interconnections required between LAE and CMOS domains and provides a means to increase the number of sensors in a system.

voltage levels (> 6 V) through the scan chain, this circuit operates using three-phase control: three scan circuits are asserted in a round-robin manner, forming a three-phase control signal for stepping through the chain. Specifically, the use of three-phase control allows us to create a dynamic pass-transistor topology, enhanced by bootstrapping. While amorphous silicon is a robust platform for these circuits, as discussed, its low mobility results in relatively low scan speeds ($\sim$ 1 kHz, i.e., 1 ms per sensor) and large operating voltages ($\sim$ 15–20 V). Replacing amorphous silicon with a higher-mobility semiconductor could greatly increase scan speeds and enable new applications that require faster sampling rates (e.g., audio applications, etc.). To this end, we fabricated and simulated variations of this scan circuit using ZnO TFTs for enhanced performance.

Figure 4.16 shows the details of the circuit design for each scan circuit within the four-element chain. It consists of 4 TFTs, a fixed resistor R, and a fixed capacitor C. For

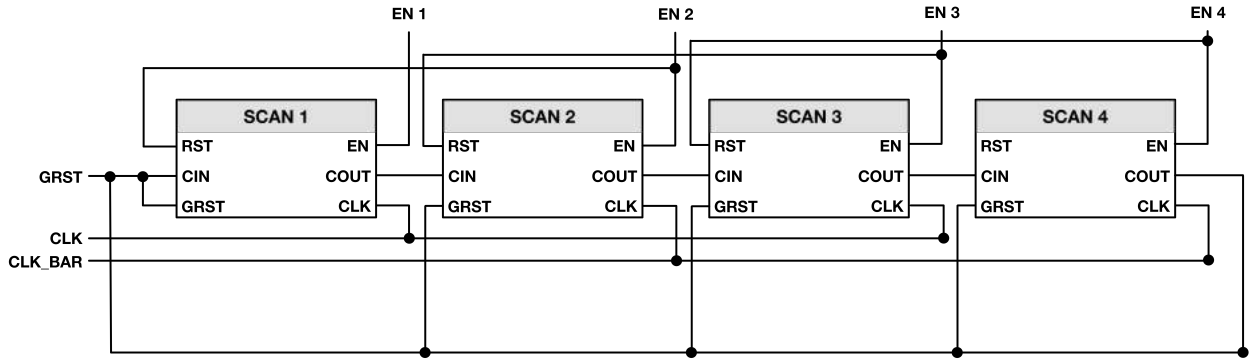


Figure 4.15: Scan chain consists of scan circuits connected together. The chain requires a two-phase clock signal (CLK and $CLKBAR$) and a global reset signal $GRST$ that come from CMOS, but all other signals are generated within the chain itself.

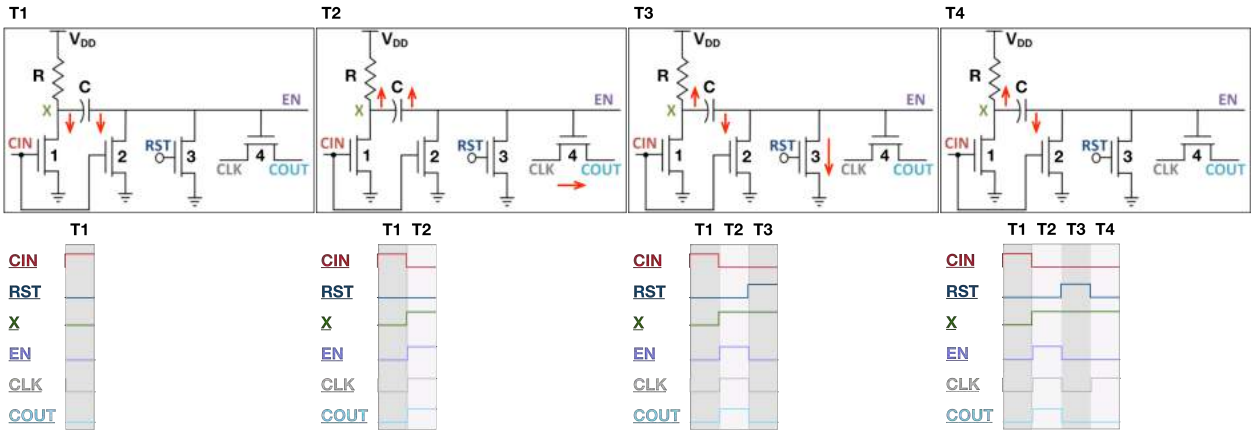


Figure 4.16: Scan circuit operation in four phases.

optimal circuit operation, we should size TFTs, R, and C such that 1) the swing of the "ENABLE" signal is close to the supply voltage V_{DD} as possible, such that when circuits are chained together the Nth ENABLE signal is comparable to the first, and 2) the duration of these "ENABLE" pulses is as short as possible, so that the number of sensors accessible in a given time is maximized. Unfortunately, these two constraints have conflicting optimal circuit designs. Observation of the circuit in action (Figure 4.16) helps clarify these opposing constraints.

As we will see, the values of R and C limit the speed of the scan circuit, and the lower limits on R and C themselves are determined by the TFT properties of on-resistance and device capacitance. These limits are determined by two voltage dividers.

In phase $T1$ of circuit operation, CIN goes high, turning TFTs 1 and 2 on with the aim of discharging C. To fully discharge C, node X must be pulled as close to ground as possible. This must be accomplished in the presence of the resistive voltage divider between R and $R_{ON,TFT1}$. This requires that R should be much much bigger than the on-resistance of TFT 1.

In phase $T2$ of circuit operation, CIN goes low, turning off TFTs 1 and 2. Because $R_{OFF,TFT1} >> R$, node X goes high. Because C has been discharged, the other side of C, EN, follows X and also goes high. In this stage, we access the sensor associated with this scan circuit. The extent to which EN is able to rise is set by a second voltage divider between capacitor C and the load capacitances imposed by TFTs 2-4. To make sure that the voltage at this node is as close to the voltage at node X as possible, the value of C should be much larger than the capacitances of TFTs 1-4. Because the clock signal from CMOS CLK also goes high in $T2$, the on-resistance of TFT 4 is very low and $COUT$ follows CLK, triggering the CIN signal for the next scan circuit in the chain.

In phase $T3$, the reset signal RST goes high (triggered by the EN signal from the next scan circuit in the chain), discharging the EN node down to ground and disconnecting the sensor. Because CIN remains low, this step allows charge to build on C: while X briefly follows EN, as current through R charges up C, X rises. The time required for X to charge fully – set by the time constant RC – sets the speed of the scan circuit. $COUT$ and CLK both go low.

In phase $T4$, charge is maintained across C. $COUT$ no longer follows CLK, since EN is low. Then the cycle repeats.

Hence, while the two voltage dividers suggest that R and C should be made large so that X and EN can swing from rail to rail, the overall speed of the circuit is set by how quickly C charges through R, suggesting that R and C should be as small as possible.

These two constraints are best satisfied by 1) making the on-resistance on the TFT as small as possible by maximizing TFT transconductance, and 2) reducing the sizes of TFTs 2-4 as much as possible (although TFT 4 must still be able to drive the load of the sensor) to mitigate the effect of the capacitive divider. A TFT with a lower R_{ON} for a given C_{TFT} is fundamentally a TFT with a higher cutoff frequency, and for this reason we expect that ZnO should deliver a significant speed enhancement to this scan circuit compared to amorphous silicon.

Figure 4.17 shows a functional ZnO scan element at work at a speed of 10 kHz (corresponding to a 100 μs minimum pulse), using a waveform generator for the RST signal (this is why its voltage only rises to 6.5 V, the max output from the generator). Node X rises fully to VDD (10 V), and is also pulled down to ground, maintaining as large a voltage swing as possible. The EN signal rises to 7.5V – this is sufficient to reset the next scan circuit, but will limit the number of circuits that can be chained together because it is greater than the RST voltage of 6.5 V. EN is prevented from rising further due to the capacitive divider between C and the capacitances of TFTs 2–4.

We note that the basic functioning of the circuit is clearly evidenced, with a clear advantage demonstrated: the speed of 10 kHz is already 10 times higher than our previous efforts with amorphous silicon scan circuits, and the supply voltage of 10 V is half as large as what amorphous silicon scan circuits require.

We can begin to optimize our circuit using our device model to tune the TFT sizing for improved circuit performance. The result of this optimization is shown in Figure 4.18; it shows that by resizing the TFTs (but maintaining the same channel length and overlap) to reduce parasitic C in the capacitor divider, we can eliminate the EN loss seen in Figure 4.17.

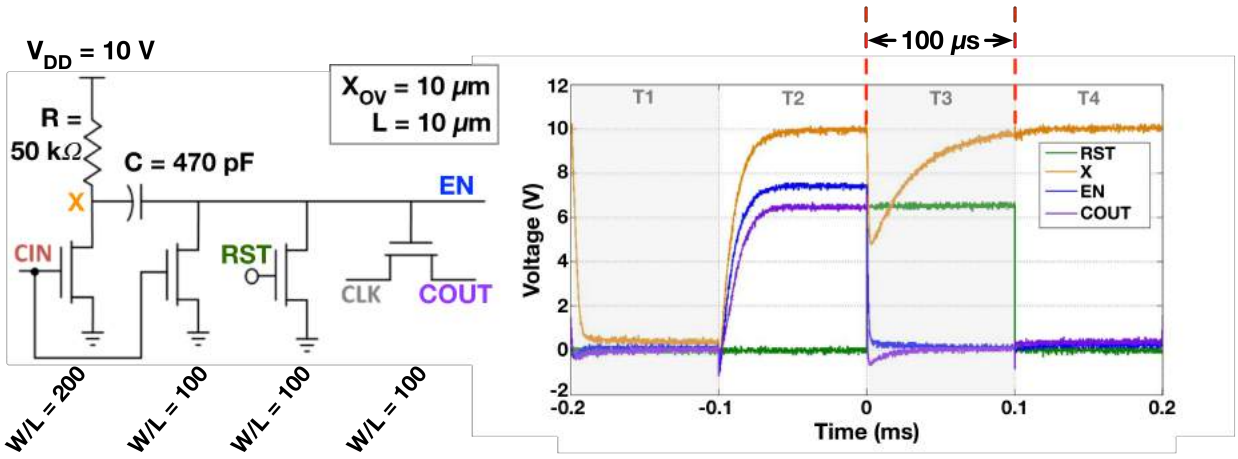


Figure 4.17: Demonstrated scan circuit using ZnO TFTs.

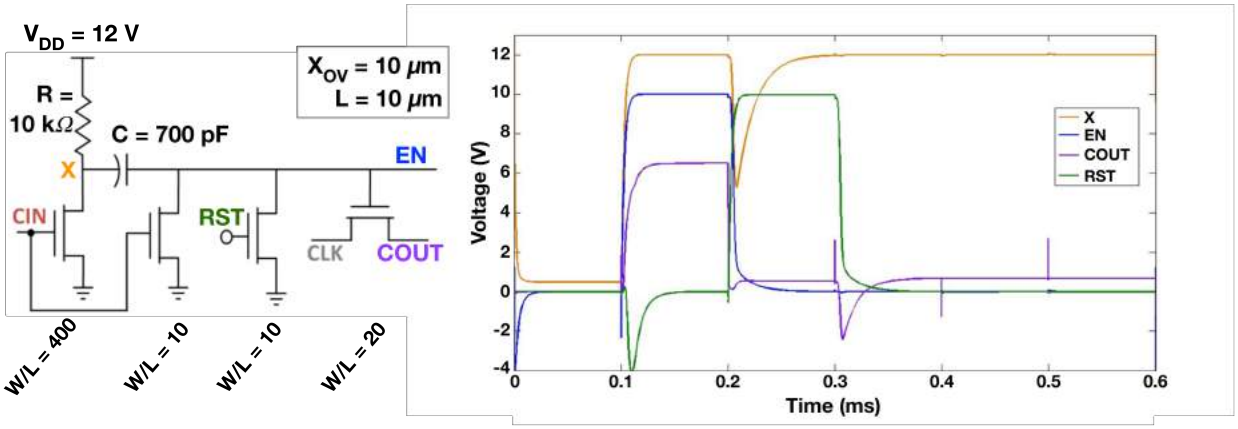


Figure 4.18: Simulated ZnO TFT scan circuit that improves upon measured result by resizing TFTs.

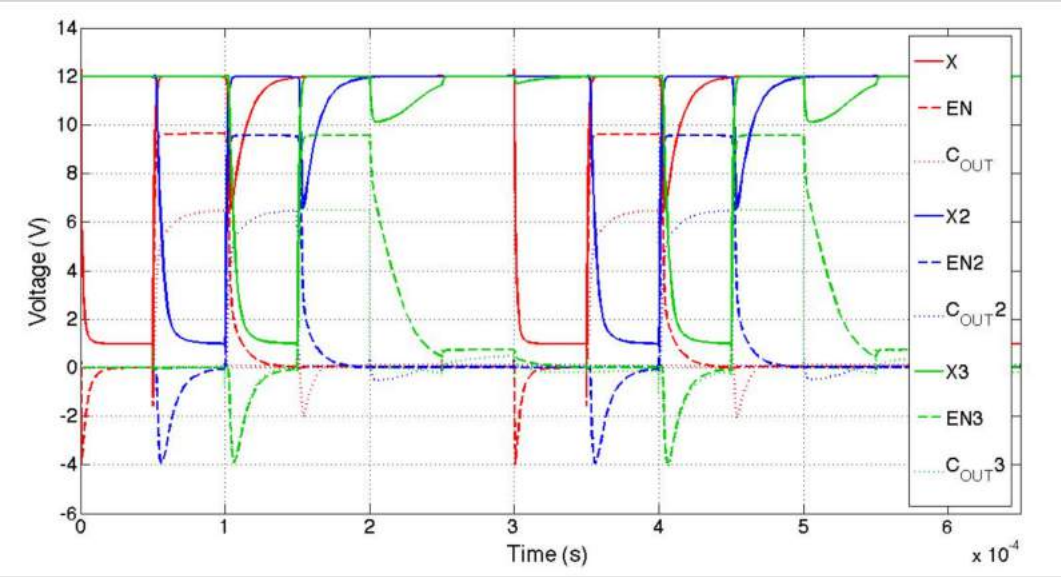


Figure 4.19: Simulated ZnO TFT scan chain that improves upon measured result by using self-aligned TFTs to reduce capacitance. Operation frequency is 20 kHz. TFT dimensions are as Figure 4.18, but X_{OV} has been reduced to 700 nm to account for self-aligned TFTs.

A primary obstacle to higher-frequency operation is the large parasitic capacitance from the large gate-source/drain overlaps. This necessitates a very large "hold" capacitor C to overcome the capacitor divider created by the capacitive parasitics and generate enable signals that approach V_{DD}. This issue is aggravated when scan elements are connected together into scan chains. Simulations indicate that reducing capacitive parasitics through TFT self-alignment will allow scan chains with sampling rates of 20 kHz (while driving a very conservative 100 pF load). The result of this simulation for a three-element scan chain is shown in Figure 4.19.

Scan chain optimization depends heavily on the nature of the load being driven. Further optimizations based on this work that more aggressively scale-down TFT channel length and assume down-scaling of the capacitive load have been performed using our PEALD technology in [188], and fully demonstrate the value of ZnO for TFT scan circuits, achieving frequencies as high as 30 kHz.

4.4 ZnO Oscillators

As introduced in Chapter 1, generation of AC signals in the LAE domain via TFT oscillator circuits raises several important capabilities in hybrid systems. If generated AC signals can be sufficiently high-frequency, then it becomes feasible to inductively- or capacitively-couple different sheets in an LAE system together, as illustrated conceptually in Figure 4.20, using mating sets of inductors or capacitors fabricated on the respective sheets. This coupling – which we call a "non-contact interface", enables a range of applications, including wireless power delivery, simplification of hybrid system integration, and radios for off-sheet communication [189–191]. A cross section of a non-contact interface between a CMOS carrier and an LAE sheet is shown in Figure 4.21, showing the typical separation between sheets. At the right of Figure 4.21 we see (for the case of power transfer) how transfer efficiency increases as a function of signal frequency in both inductive and capacitive interfaces. However, from Figure 4.21 it is clear that inductive interfaces become efficient only above 10 MHz. Inductively-coupled interfaces offer two advantages over capacitively-coupled interfaces: 1) they have previously been shown to be far less susceptible to misalignment between mating layers in non-contact interfaces than capacitively-coupled interfaces, and 2) inductors provide a straightforward means to step voltages and currents up and down as needed between CMOS and LAE technologies; for these reasons, efficient inductive interfaces have become an important goal in LAE hybrid systems.

LAE gives us the ability to build physically-large inductors that can have high quality factor Q (e.g., wide traces for low resistance, many turns for large inductance); this is a promising first step for low-loss non-contact interfaces. However, because LAE TFTs are limited by relatively low f_T, it becomes challenging to actually generate signals in excess of 10 MHz that are needed for efficient coupling. Many TFT-based ring oscillators have been demonstrated in literature (e.g., [155, 176, 192–198]), but these generally face low f_T limitations and hence never come close to 10 MHz. TFT oscillators reaching frequencies as high as 100 MHz have been demonstrated, but typically use higher temperature (300

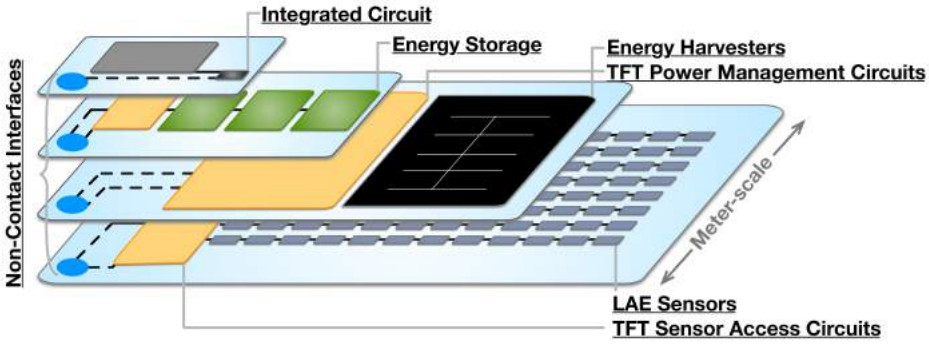


Figure 4.20: One application of oscillator circuits in LAE hybrid systems is to simplify system integration through non-contact interfaces that connect sub-systems fabricated on different sheets.

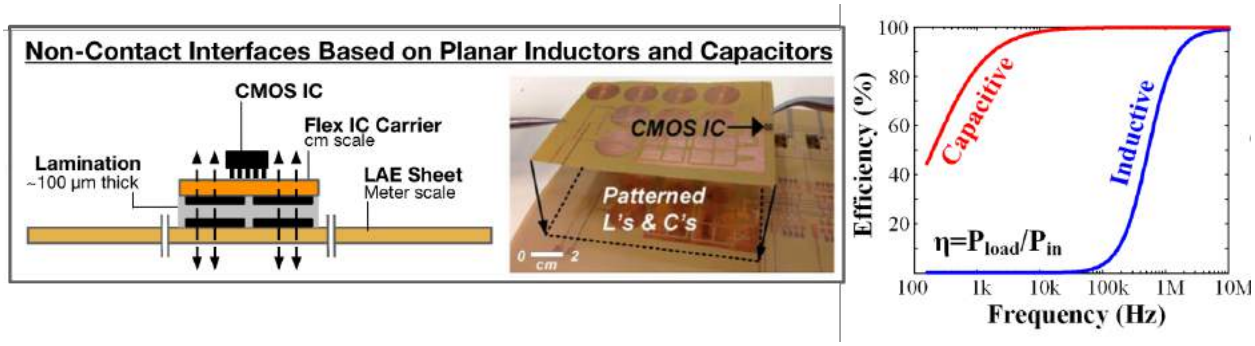


Figure 4.21: Non-contact interfaces are created by laminating together mating sets of inductors or capacitors on different sheets. The frequencies at which capacitive and inductive coupling become efficient are different [58].

°C) processing where LTPS CMOS topologies can be exploited ([199–201]). One example exists of very fast (75 MHz) IGZO TFT oscillators, but the channel length is scaled down to 500 nm, and the process temperature is still too high for many plastic substrates at 300 °C. We address the challenge of high-frequency, low-temperature compatible TFT oscillators in this section, using both higher-mobility ZnO and circuit strategies to overcome previous limitation.

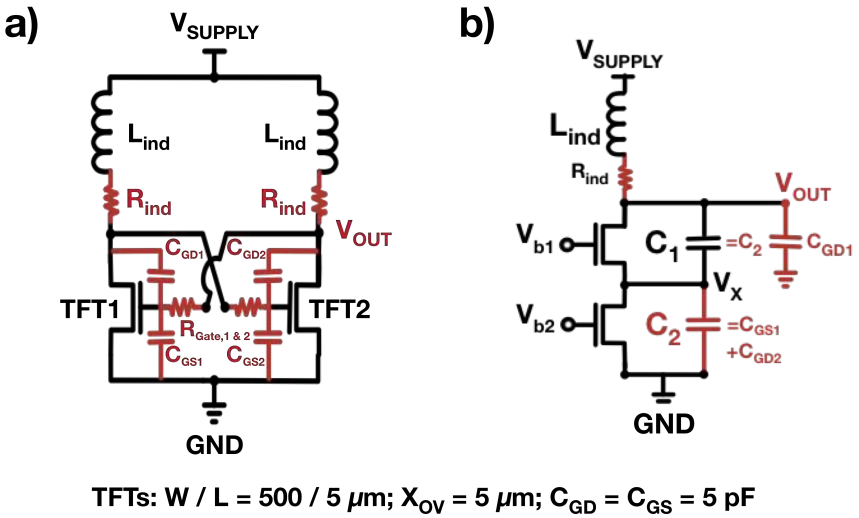


Figure 4.22: Schematics of (a) cross-coupled and (b) Colpitts resonant oscillators, with parasitic elements highlighted in red.

4.4.1 Design Considerations

As mentioned in Section 4.1.2, we can use resonant circuits to overcome the low f_Ts in TFT circuits. This is essential to creating TFT oscillators that operate $>$ 10 MHz. Resonant circuits tune out large TFT capacitances using high-quality passives – in this case, high-Q inductors – to achieve oscillation frequencies that are limited by f_{MAX}, not f_T. In this section, we discuss two common types of resonant oscillators – the cross-coupled oscillator and the Colpitts oscillator. We note that for oscillations to occur, it is not sufficient for the ZnO TFTs to have high f_{MAX} – each circuit must also satisfy its positive-feedback condition, which depends on TFT parameters, but also on parameters of the passive circuit components. If both of these conditions are met, then the circuit will oscillate at a frequency set by the effective capacitance C_{par} and inductance L_{ind} of its resonant tank:

$$f_{osc} = \frac{1}{(2\pi\sqrt{L_{ind}C_{par}})} \tag{4.12}$$

4.4.2 Cross-Coupled Oscillators

Using non-self-aligned ZnO TFTs with optimized f_{MAX} (reduced R_{gate}, minimal channel length and overlaps), we construct cross-coupled LC oscillators according to the schematic in Figure 4.22a. For a given inductor and TFT, the resonant frequency will be constant. Hence, to approach the frequency limitation (f_{MAX}) set by the TFTs, we employ a range of planar, spiral inductors on plastic with varying values of L_{ind}, all with low-resistance (low R_{ind}) 25-μm-thick copper traces, and downsize the inductors (in discrete steps, by using inductors with fewer turns) until it is no longer possible to achieve oscillations. As TFTs are fabricated on glass, while inductors are on plastic, soldered external wires are used to form interconnections. The positive feedback condition for the circuit, which depends heavily on parasitic capacitors and resistors in the circuit, must be satisfied for oscillations to occur:

$$g_m R_{TANK} = \frac{\mu C_i \frac{W}{L}(V_{GS} - V_T \times WL) L_{ind}}{C_{par}(R_{ind} + R_{gate})} > 1 \tag{4.13}$$

Optimization of R_{gate} (and other TFT parameters) thus allows the positive-feedback condition to be met with smaller L_{ind} values. This is turn results in higher oscillation frequencies in accordance with Equation 4.12. Figure 4.23 shows the oscilloscope-measured output of a cross-coupled oscillator with $L_{ind} = 1.5$ μH. The circuit oscillates at $f_{OSC} = 35.3$ MHz, just below the simulated f_{MAX} of the TFTs (40 MHz), and is the fastest thin-film circuit fabricated entirely below 200 °C published to date [1].

We note that one drawback of this circuit is that the TFT gate-to-drain capacitances experience a Miller multiplier effect, making the total capacitance of the resonant tank C_{par} – which sets the resonant frequency according to Equation 4.12 – about 2× higher than just the device capacitances for our device sizing:

[1] In fact, by designing inductors that downsized in smaller increments, we were able to build cross-coupled oscillators that oscillated at frequencies as high at 39 MHz, but the USB storing the waveform data has long since vanished!

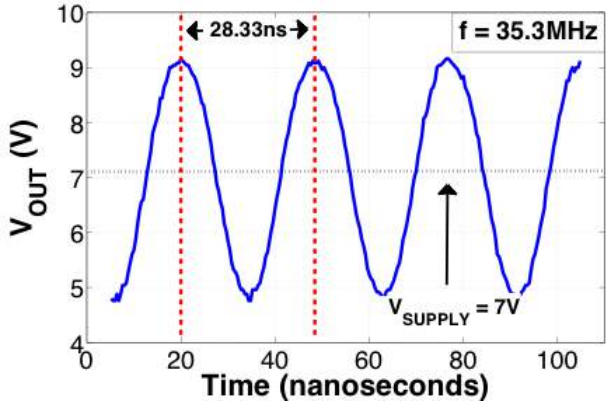


Figure 4.23: For the cross-coupled topology, 35.3 MHz oscillations with peak-to-peak voltage of 4.3 V are achieved at a supply voltage of 7 V. ZnO TFTs have dimensions W/L = 500 / 5 μm and X_{OV} = 5 μm. L_{ind} = 1.5 μH, I = 10.1 mA, P = 70.7 mW.

$$C_{par} = 2 \times (C_{GD1} + C_{GD2}) + C_{GS1,2} + C_{ox} \sim 5 \times C_{OV} + C_{ox} \sim 6C_{OV} \tag{4.14}$$

As a final aside that is most relevant when considering the next chapter, we mention that for systems applications, oscillators may need to operate continuously for extended times; conveniently, ZnO oscillators under continuous operation show far less (∼2-3%) current degradation over 1800 seconds than ZnO TFTs under constant bias stress (nearly 20%), as seen in Figure 4.24. This result most likely stems from the fact that TFTs in cross-couple oscillators undergo rapid transitions from saturation to linear and back, and therefore only *intermittently* experience strong bias voltage stress, compared to a TFT biased constantly. This suggests that ZnO TFT oscillators can serve as a robust circuit block for our LAE hybrid systems.

4.4.3 Colpitts Oscillators

Because non-self-aligned TFTs present exhibit large C_{GS} and C_{GD} overlap capacitances, in principle Colpitts oscillators (schematic shown in Figure 4.22b) present an advantage: by eliminating the Miller effect, they result in substantially lower C_{par} and thus possibly

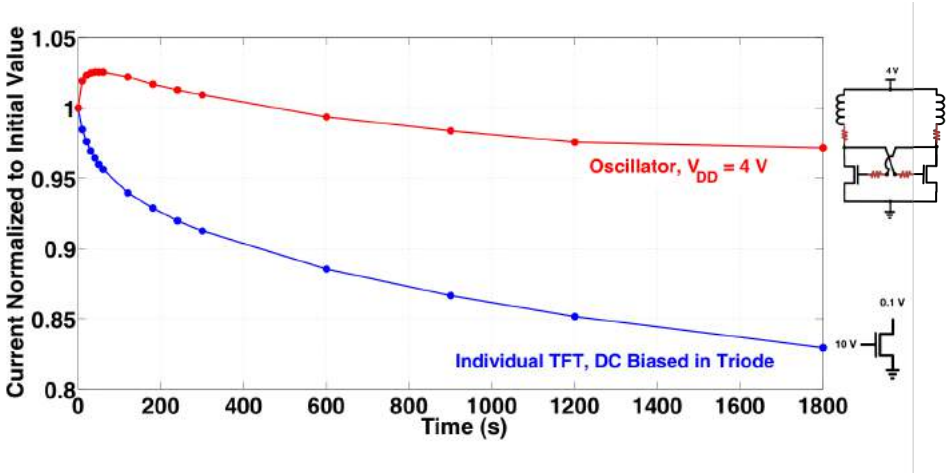


Figure 4.24: For the cross-coupled topology, current degradation from the initial value is far less than for an individual TFT biased in the linear regime.

higher oscillator frequencies via Equation 4.12. The challenge, as seen in Figure 4.22b, is that Colpitts oscillators achieve positive feedback via a capacitor-divider connection between drain and source nodes; capacitive division results in a more stringent positive-feedback condition, minimized when $C_1 = C_2 = C_{TFT}$:

$$g_m R_{TANK} > (C_1 + C_2) L_{ind} \omega_R^2 = \frac{(C_1 + C_2)^2}{C_1 \times C_2} = 4 \tag{4.15}$$

We used our non-self-aligned, f_{MAX}-optimized ZnO TFTs to build various Colpitts oscillators. These achieve oscillation frequency f_{OSC} up to 31.25 MHz with $L_{ind} = 2.7$ μH. This oscillation frequency is 50% higher than the frequency we achieved for ZnO cross-coupled oscillators with the same inductance, because C_{par} has been reduced by elimination of the Miller effect. Despite the C_{par} benefit, the higher required g_m – and hence higher V_{SUPPLY} and biasing current – in practice leads to greater power consumption.

For all topologies and all device optimizations, we expect that the oscillator frequency can be increased at the cost of increased power consumption; for a given TFT, reducing L_{ind} increases f_{OSC} (via Equation 4.12) but makes oscillation more difficult (via Equations 4.13 and 4.15). Boosting g_m (by increasing V_{GS}) is the only way to make oscillation easier,

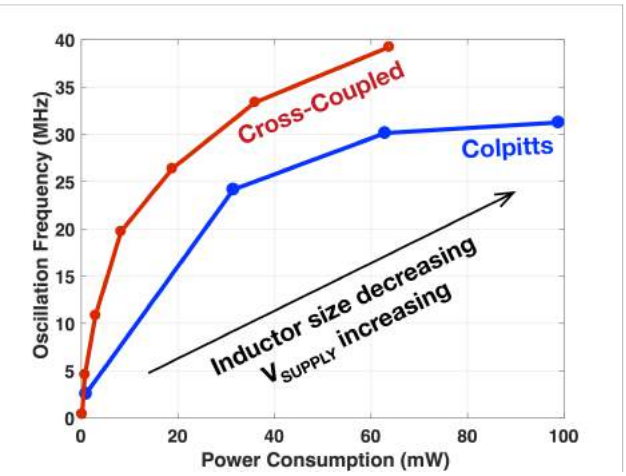


Figure 4.25: While the Colpitts oscillator topology can achieve higher oscillation frequencies for a given L_{ind} than the cross-coupled topology, its more stringent positive-feedback condition requires biasing the TFTs for higher transconductance to achieve oscillation, resulting in higher power consumption for a given frequency. In this plot, TFT sizing is held constant (W/L = 500/5μm, X_{OV} = 5μm). Moving to the right requires reducing inductor size and boosting the supply voltage applied to the circuit.

but requires higher V_{SUPPLY}, which consumes more power. Thus, it is useful to look at power consumption and frequency together. Figure 4.25 shows frequency versus power for the cross-coupled and Colpitts topologies in ZnO technology.

This figure highlights that the cross-coupled oscillator gives higher frequencies at lower power than the Colpitts topology. For example, in the case of the 31.25 MHz oscillator, V_{SUPPLY} = 19 V, V_{b1} = 19 V, and V_{b1} = 10 V, resulting in an average current of 5.2 mA. For comparison, the highest supply voltage required for the fastest cross-coupled oscillators in Figure 4.25 is just 8.5 V (resulting in an average current of 7.5 mA).

4.4.4 Flexible Cross-Coupled Oscillators

Because cross-coupled oscillators provide higher oscillation frequencies at lower power than Colpitts oscillators, we next fabricated cross-coupled oscillators on plastic substrates (3.5-μm polyimide) using non-self-aligned ZnO TFTs with optimized f_{MAX}. We choose to build flexible oscillators on the ultra-thin, 3.5-μm-thick polyimide in order to minimize the gate-

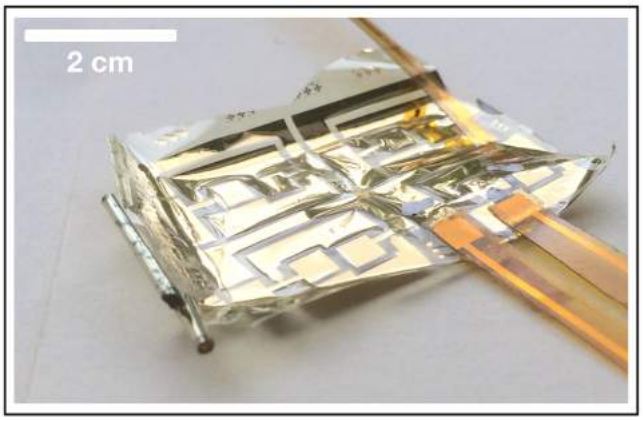


Figure 4.26: Flexible oscillator sample with cross-coupled TFTs is connected to off-sheet Cu spiral inductors using flexible Au interconnects.

source drain overlap dimension to 5 μm (recall, for freestanding polyimide, 15 μm overlaps are required) and thereby reduce C_{par} as much as possible. In order to interconnect the copper inductors (designed in-house but fabricated commercially) to the flexible TFT sample, flexible, reusable Au interconnect traces are fabricated and cut to size. These are then laminated to the inductor contact pads and the TFT contact pads with anisotropic conducting tape (3M), that conducts only in the z-axis. Because these in-house fabricated connectors cannot be thicker than 200 nm, they contribute an additional resistance to the circuit of 10 Ω per connector, which is much higher than the resistance contribution of the soldered copper wires in the previous subsections. A picture of these flexible interconnects laminated to a cross-coupled TFT sample can be seen in Figure 4.26.

Figure 4.27 shows the oscilloscope-measured output waveform of a cross-coupled oscillator on a 3.5-μm polyimide substrate with $L_{ind} = 3.7$ μH. At a V_{SUPPLY} of 9 V, the circuit oscillates at $f_{OSC} = 17$ MHz, which significantly above the TFT's f_T of 12.9 MHz, but lower than the peak oscillation frequencies for TFT oscillators on glass because of the contribution of interconnect resistance, which serves to increase the effective R_{gate}.

The reduced performance of the flexible oscillators is visible also when observing the plot of the tradeoff between frequency and power across different cross-coupled oscillators with

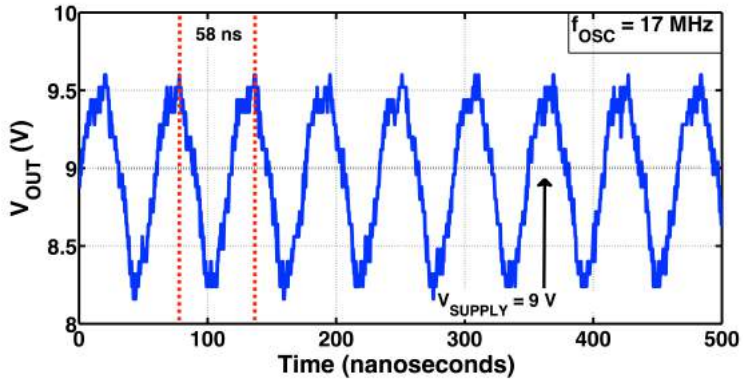


Figure 4.27: Cross-coupled ZnO TFT oscillators achieve frequencies as high as 17 MHz. W/L = 500/5μm, X_{OV} = 5μm.

identically sized TFTs but different R_{gate} values (Figure 4.28). The reduced performance – lower frequencies and higher power consumption – for the flexible oscillators, in green, falls on a spectrum corresponding to different R_{gate} values. This is because its effective R_{gate} is increased to 52 Ω because of high-resistance thin-film metal interconnects. With improved interconnects, we expect the results for oscillators on polyimide to approach the result for glass. Figure 4.28 illustrates the practical advantage to TFT R_{gate} optimization – not only do low-R_{gate} TFTs result in faster oscillators, they also result in circuits that consume less power – and all these benefits can be harvested readily by simply changing the gate metal, a much easier feat than building a better semiconductor.

Because flexible oscillators may be used in applications that require mechanical deformation, we measured the oscillation frequency while bending the plastic substrate into a cylinder, with the TFT channel length perpendicular to the direction of axis of the cylinder, and with TFTs on the outside of the cylinder (e.g., the same way as in Section 3.5.2, corresponding to tensile strain). The change in oscillation frequency as a function of bending radius of the TFTs in the circuit is provided in Figure 4.29. When the entire oscillator (TFTs and inductors) is bent to the same radius, the frequency changes measurably. This change could result from changes in the TFT upon bending, or from changes in the inductors upon

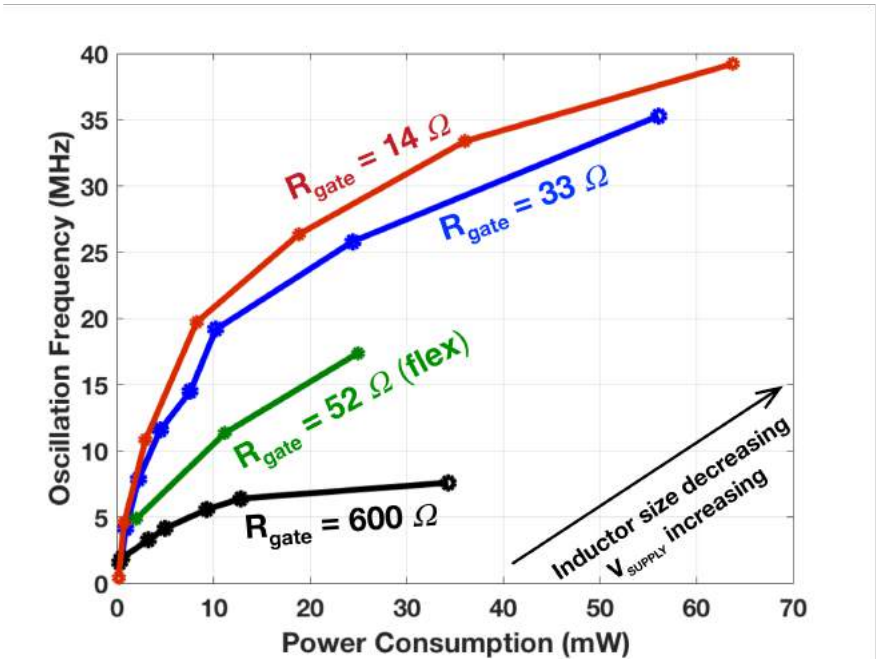


Figure 4.28: Oscillation frequency versus consumed power for identically-sized ZnO TFT cross-coupled oscillators (W/L = 500/5 μm, X_{OV} = 5 μm) with varying R_{gate} values.

bending, or both. Because the circuit is laminated together and not monolithically fabricated, it was possible to decouple these two elements and tease out the culprit, by flattening the TFTs and the inductors individually while keeping the other component flat. We find that when the inductors are flattened, but the TFTs remain bent, the oscillation frequency returns exactly to its unbent value.

This behavior is explained as follows: the inductance L_{ind} of the planar inductors decreases as their bending radius increases, as shown in Figure 4.30. This causes the oscillator frequency to shift upwards upon bending. Inductors with very different inductances but identical outer radius (i.e., different numbers of turns) have nearly identical bending behavior, which suggests that inductor geometry plays a role in this effect. For the inductor used in the oscillator measured while bending in Figure 4.29, we see a 10% reduction in inductance at an inverse bending radius of 0.08 inverse millimeters. Equation 4.12 predicts a 5% increase in oscillation frequency as a result of a 10% inductance decrease, which is exactly the result we see in Figure 4.29. This change in oscillation frequency as a function

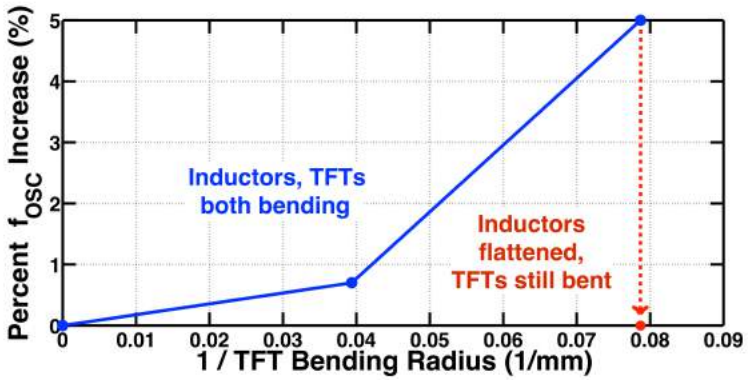


Figure 4.29: Upon bending, flexible oscillators (cross-coupled TFTs and inductors) exhibit an increase in oscillation frequency. When the inductors in the circuit are flattened while the TFTs remain bent, the oscillation frequency returns exactly to its unbent value.

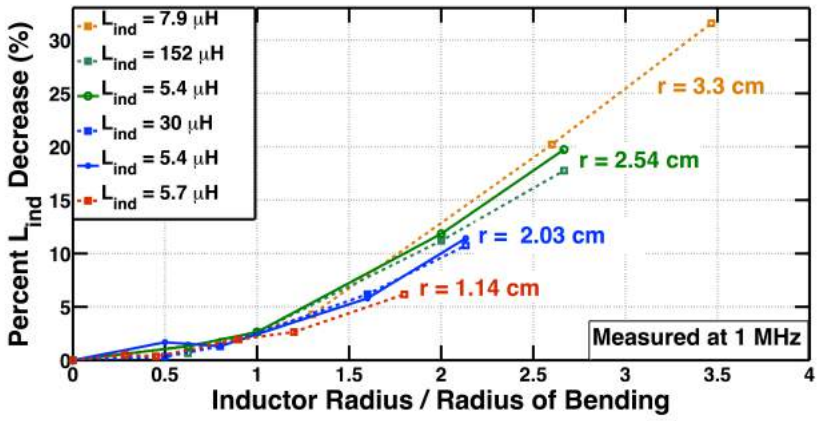


Figure 4.30: In this VNA measurement, planar spiral inductors of various inductances L_{ind} and outer radii (r) exhibit reduced inductance as bending radius is reduced (e.g., as more strain is applied). The relationship between bending radius and inductance decrease appears to depend more on inductor outer radius than on inductance, suggesting that inductor geometry plays a role in this behavior.

of bending radius is important to consider in large-area flexible systems employing resonant LC oscillators.

4.4.5 Comparison with Amorphous Silicon

Lastly, let's examine the advantage that ZnO oscillators give compared to amorphous silicon predecessors by looking at the frequency-power tradeoff across technologies. It can be challenging to compare oscillators from different technologies; for example, amorphous silicon TFTs have such low transconductance that very large inductors are required to satisfy the condition for positive feedback (Equation 4.13). Because these inductors have many more turns than the inductors used for ZnO TFTs, they have much higher resistance, diminishing the impact of TFT R_{gate} reduction observed for ZnO oscillators in this chapter. Furthermore, large inductors exhibit greater parasitic self-capacitance, which can also reduce the effect of TFT overlap capacitance reduction on the value of C_{par} and necessitates wider TFTs for amorphous silicon oscillators than in ZnO oscillators.

With these caveats in mind, we compare the frequency-power plot for ZnO and amorphous silicon cross-coupled TFT oscillators in Figure 4.31. The plot compares ZnO oscillators with optimized Cr/Al/Cr gate metal and 100-nm thick Cr-only gate metal (as shown in Figure 4.28) with α-Si oscillators with 100-nm thick Cr-only gate metal. The sizing for the TFTs is as typical for each technology: W/L = 500 / 5μm for ZnO, and 3600 / 6 μm for α-Si. The overlap sizes also differ – X_{OV} is 5 μm for ZnO and 15 μm for α-Si (which results in higher capacitance but lower R_{gate}).

Despite these geometric differences, we can draw a few important conclusions from Figure 4.31. First, ZnO oscillators without gate metal optimization barely outperform amorphous silicon oscillators, despite their 20× mobility advantage! In this case, high gate resistance masks ZnO's material advantage, underscoring the value of taking a holistic approach to TFT design in which parasitics are given as much weight as more popular parameters like mobility. Second, after gate resistance reduction, ZnO oscillators achieve a $>$ 60× reduction

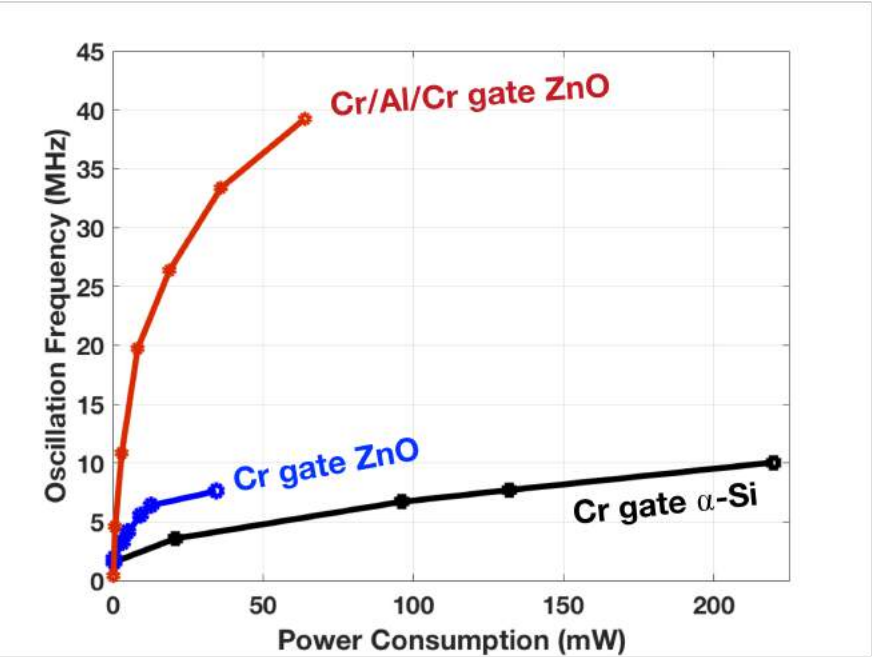


Figure 4.31: Comparison of Cr-Al-Cr gate ZnO, Cr-gate ZnO, and Cr-gate amorphous silicon TFT cross-coupled oscillators. ZnO TFTs have W/L = 500 / 5 μm and X_{OV} = 5 μm, while α-Si TFTs have W/L = 3600 / 6 μm X_{OV} = 15 μm.

in power for a given frequency compared with α-Si; e.g., At 10 MHz, ZnO oscillators consume 3.5 mW (from 3 V supply), while α-Si oscillators consume 220 mW (from a 30 V supply), although we expect this disparity would be reduced somewhat upon reduction of X_{OV} and L for α-Si oscillators, combined with α-Si TFT R_{gate} reduction.

4.5 Section Summary

In this chapter, we established the importance of certain TFT-level metrics that are most relevant when building circuits, and provided measurements of these parameters for ZnO TFTs: f_T, f_{MAX}, and g_m/I_D. In particular, we highlight the importance of the f_{MAX} for circuit design, a metric that is largely unknown in the materials and TFT community, and optimized ZnO TFTs for high f_{MAX} by emploing a composite, low-resistance gate metal. We described the development of a ZnO TFT model that serves as an invaluable tool for

circuit design prior to circuit layout and fabrication that matches well with measured TFTs measured under DC conditions (I–V curves) and also at AC conditions (H21 and MAG curves). Lastly, we demonstrated ZnO scan circuits and resonant oscillators, characterizing their behavior and quantifying their benefits compared with amorphous silicon predecessors. Resonant oscillators on flexible substrates were also shown, and behavior under application of mechanical strain was measured. The resonant circuits in this section are the highest frequency low-temperature (< 200 °C) TFT circuits reported, because they exploit not only the material advantages of ZnO, but also because they employ circuit solutions to the unavoidable problem of high TFT capacitance.

The next chapter will build upon this chapter, using these high-frequency resonant ZnO TFT oscillators to build a hybrid sensing system.

Chapter 5

Highly-Scalable Large-Area Sensing System Using ZnO TFT Oscillators

In this chapter, we build upon the results from the previous chapters to create the first ZnO-silicon CMOS hybrid sensing system.

We have discussed in prior chapters how a hybrid architecture that combines the strengths of large-area electronics with silicon CMOS is an effective strategy for building full sensing systems. However, when building systems that accommodate very large numbers of sensors, a new challenge emerges that is specific to hybrid architectures: how can we physically interconnect a large number of distributed LAE sensors with the CMOS domain in a way that is efficient and scalable? Research in hybrid systems has shown that, in the absence of a high-volume, mechanically flexible wire-bonding technology, these LAE–CMOS interconnections form the primary bottleneck to system scalability [58]. As illustrated in Figure 5.1, specialized TFT architectures can overcome this; TFT active matrices have been effective in reducing CMOS-LAE interconnects in large-area, flat-panel displays and imagers. However, active matrices yield only a square-root reduction in the number of LAE-CMOS interconnections and are most conducive to tight, highly-regular arrangements of sensors due to the impact of gate-/data-line capacitances [202]. Other interfacing approaches like scan circuits

aim to address this challenge, but are ultimately limited in scalability (by "EN" degradation from capacitive voltage division) and speed (by the RC time constant). Envisioning future systems capable of scaling to very large numbers of distributed sensors, in this chapter we develop a TFT architecture that aims to 1) maximize the number of accessible sensors for a given number of of physical CMOS–LAE interconnections and 2) minimize the time needed to access all sensors in an LAE hybrid sensing system, despite low TFT performance.

Section 5.1 describes the overall architecture, which uses an array of amplitude-modulated, frequency-hopping ZnO TFT oscillators to enable much greater scalability of sensors for a given number of connections than existing technology interfacing methods [203]. Section 5.2 focuses on the circuit-level implementation, which exploits high-Q, digitally-controlled LC oscillators to substantially increase the signal-processing bandwidth compared to typical TFT circuits. Section 5.3 presents the system prototype, wherein the architecture is applied to a large-area force-sensing system that exhibits extremely low acquisition error. Finally, Section 5.4 provides conclusions.

The architecture and system presented in this chapter were the result of a particularly close collaboration between the author and Tiffany Moy. Tiffany Moy was responsible for 1) sensor signal reconstruction and system error evaluation, 2) system-level simulations based on frequency variations, 3) architecture-level simulations, 4) probe card layout and component soldering, and 5) characterization of the force-sensor PCB. The author was responsible for 1) design, analysis, simulation, and iteration of the digitally-controlled oscillator circuits, 2) layout, fabrication, and testing of the ZnO circuit samples, 3) transfer-function measurement, frequency analysis, and variation characterization, 4) simulation and implementation of injection-locking and tuning of locking range, 5) inductor design, layout, and assembly 6) weight design and construction, and 7) system integration and measurement automation. Further assistance in this project was provided by undergraduate Nicholas Brady, who designed of the sensor array, and Lung-Yen Chen, who helped the author upload arbitrary waveforms to the waveform generator. The results from this chapter were presented by

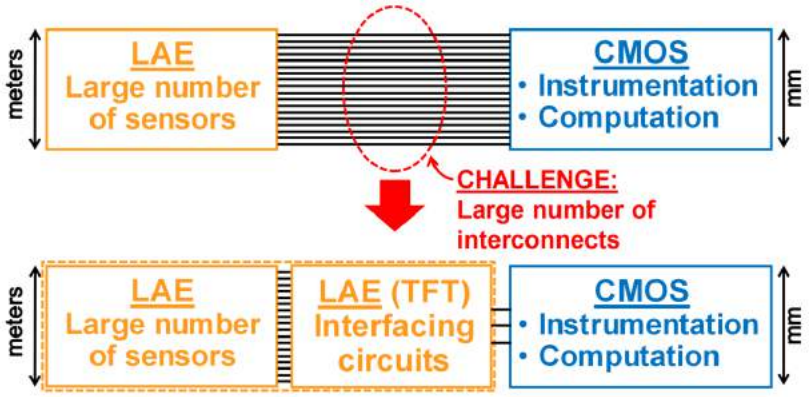


Figure 5.1: Hybrid systems combine complementary strengths of LAE and CMOS, but the physical interconnections between technology domains limit sensor scaling. This challenge has motivated specialized TFT architectures, including active matrices, scan circuits, and the architecture presented in this chapter.

the author at the 2017 International Solid State Circuits Conference, and published in the Journal of Solid State Circuits [203, 204].

5.1 System Architecture

5.1.1 Overview

The goal of this architecture is again to maximize access to LAE sensors (number of sensors accessed in a given time) while minimizing the number of interconnections between distributed sensors and the CMOS IC. To accomplish this, we propose an architecture that leverages the high f_{MAX} of our ZnO TFTs (compared to α-Si) and the high demonstrated oscillation frequencies of our ZnO TFT oscillators discussed in the previous chapter. The system architecture shown in Figure 5.2 as a block diagram (left) and as a conceptual sketch of a fully-realized system (right). The LAE domain consists of an array of M sensors, where each sensor is connected to one TFT-based digitally-controlled oscillator (DCO). The DCO outputs are then summed, resulting in a *single differential interconnection* to the CMOS domain, despite the large number of sensors in the array. Instrumentation and signal processing

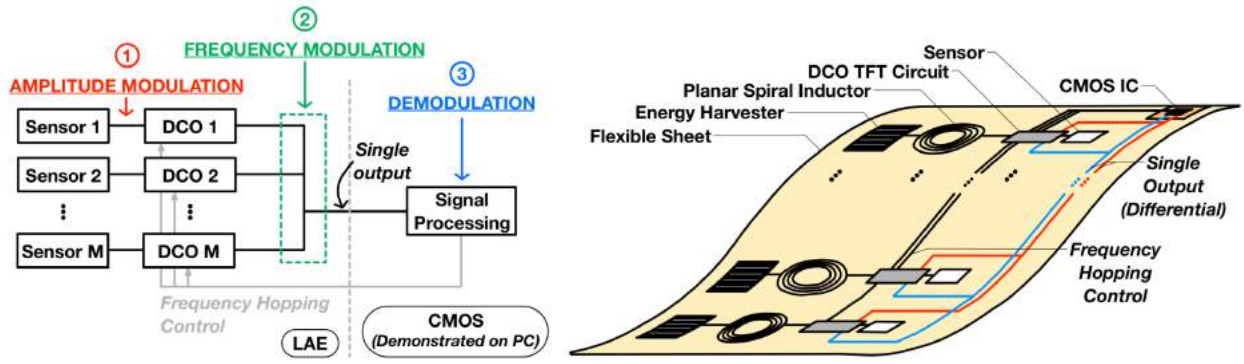


Figure 5.2: System architecture (left) and conceptual implementation (right). System presented consists of an array of sensor-DCOs pairs, where DCO amplitude is modulated by sensor signal and frequency is modulated by CMOS frequency-hopping control signal, yielding a single differential interface to CMOS. The conceptual drawing shows how a fully-realized system would incorporate a CMOS IC, solar cells for self-powering, large, planar, spiral inductors, interconnects, and TFT circuits.

for demodulating the many sensor signals are then performed in the CMOS domain (using a PC in this system demonstration). Each sensor signal value modulates the *amplitude* of the output waveform from its associated DCO. Meanwhile, a frequency-control signal from CMOS (labelled the "Frequency Hopping Control" signal) modulates the *frequencies* of the output waveforms from all the DCOs, in a way that enables all the sensor-modulated DCO outputs summed on the single interconnection to CMOS to be separated, and allows the sensor signal data to be recovered. Figure 5.3 provides a simple illustration of the impact of the sensor signal value and the frequency hopping control code on the DCO output waveform.

As seen, each DCO has N frequency-control bits that mate with the N frequency-hopping control code bits from CMOS. Depending on which of these bits is engaged/disengaged (e.g., at the supply voltage or at ground), the DCO will then output into one of 2^N frequency channels. While standard frequency multiplexing would yield a linear increase in the number of sensor signals with the number of frequency channels, a frequency-hopping scheme can yield a much greater increase, and accordingly a much greater reduction of interconnections. While the sensor density is limited by the physical area occupied by the LAE circuitry,

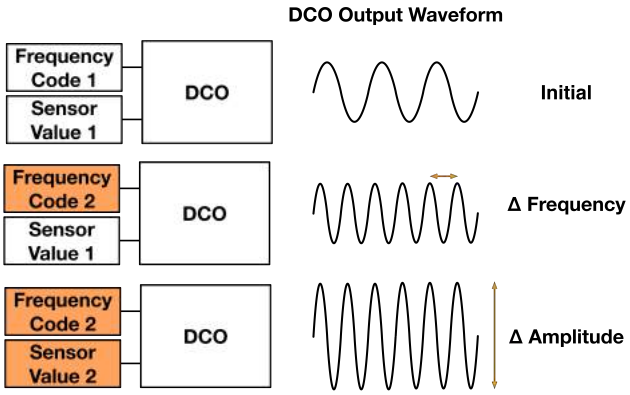


Figure 5.3: When frequency code switches from 1 to 2, the DCO output waveform frequency changes. When the sensor value changes from 1 to 2, the amplitude of the DCO output changes.

(which is largely dominated by the area occupied by the DCO inductors, as seen in Figure 5.2), this architecture makes access to a very large number of distributed sensors possible.

For our demonstration, we choose to set the number of frequency control bits N to 3, which means each DCO can output into one of $2^3 = 8$ frequency channels. Figure 5.4 (top) shows the frequency-hopping scheme employed with $N = 3$. The frequency-hopping control code $H[N-1:0]$ from CMOS provides N bits to the array of DCOs (in the $N = 3$ case shown, $H[2:0]$ is the 3-bit code). Critically, each of these frequency control bits is hardwired *differently* to the frequency-control inputs $X[N-1:0]$ of each of the M DCOs in the array. For example, in Figure 5.4, we see that DCO 1 receives as inputs $H[1]$, $H[0]$, and $H[0]$, while $DCOM$ receives as inputs $H[1]$, $H[2]$, and $H[2]$. For readout, all the DCO outputs are coupled through capacitors C_C to a single differential interconnection to CMOS, as shown.

Figure 5.4 (bottom) shows how scanning through the different values of the hopping-control code (e.g., 001, 010,...) causes each DCO to follow a unique frequency-hopping pattern through all the different frequency channels. The patterns are shown for two DCOs. Note that the sensor signals are assumed to be constant while we cycle through all permutations of the frequency hopping control code (e.g., 001, 010, 100, ..., 011 for $N = 3$), setting a limitation for sensor signal frequency – this scenario is known as "fast frequency hopping".

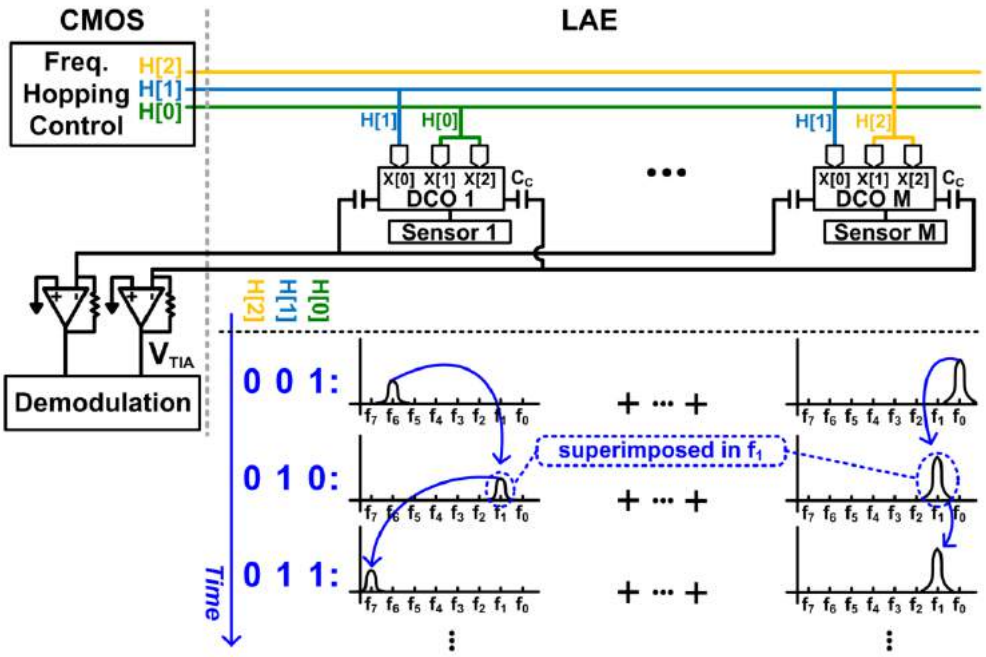


Figure 5.4: Unique hardwired connections (in yellow, blue, and green) between CMOS hopping control-code bits (H[2:0]) and frequency-control bits (X[2:0]) for each DCO in the array, as shown at top, give each DCO-sensor pair a unique, predetermined hopping pattern as the hopping code values are scanned through in time (e.g., 001, 010, ... , 011), as shown at bottom for two DCOs in an N = 3 system. The unique patterns are used to recover sensor data. DCO outputs are summed by differential TIAs in the CMOS domain for signal processing.

As shown, all the DCO outputs are summed by transimpedance amplifiers (TIAs) in the CMOS domain for readout. Starting with $H[2:0] = 001$, we see that the frequency-control connections cause DCO 1 to output in frequency-channel 6, and DCO M to output in frequency-channel 0 (note that the output levels of the DCOs are shown to be different, since the DCO output amplitudes depend on the sensor signal values, here assumed to be different). Next, with $H[2:0] = 010$, both DCOs output in frequency-channel 1, resulting in a temporary superposition of the two sensor signals. But subsequently, with $H[2:0] = 011$, the DCOs again output in different frequency channels. Hence, although the DCO outputs may overlap and end up in the same channel at certain points in the hopping code cycle, each DCO takes a unique *path* through all the frequency channels because of the unique configuration of its frequency control bits.

Most importantly, these unique hopping paths over the course of the hopping-code scan are *predetermined*, since the control bit configuration is hardwired in advance. We can then use these unique hopping patterns to identify each DCO, separating all of the sensor signals on the single interconnection to CMOS, despite the sensor superpositions observed above.

We can use these unique hopping patterns to construct a mathematical relationship that will readily allow sensor signal reconstruction. The mapping of sensor signals to frequency-channels can be represented by a "hopping matrix" $\mathbf{T}$, and separation can be achieved by using the matrix equation shown in Figure 5.5 for the $N = 3$, 8 frequency channel case. In $\mathbf{T}$, each group of 8 rows forms a submatrix, corresponding to a particular hopping-code value (e.g., 001, etc.). Each row within a submatrix corresponds to a particular frequency channel f. Thus, each column of $\mathbf{T}$ corresponds to a particular sensor-DCO pair m. The entries $t_{f,DCOm}$ in this matrix are only non-zero if DCO m outputs in the corresponding frequency channel f during the corresponding hopping-code value; for this reason, most matrix entries are seen to be zero.

$\mathbf{T}$ multiplies with a vector $\vec{s}$, whose elements represent the values of the M sensor outputs – this is the information we would like to tease out. The resultant vector $\vec{y}$ consists of elements $y_{f,H[2:0]}$ that correspond to voltages summed by the CMOS transimpedance amplifier in each frequency channel f, for each hopping-code value $H[2:0]$. Using the example from above, during $H[2:0] = 001$, DCO 1 outputs in frequency channel 6 and DCO M outputs in frequency channel 0, corresponding to the non-zero entries shown in $\mathbf{T}$.

With this matrix relationship, the sensor data can now be easily recovered by inverting the hopping matrix: $\vec{s} = \mathbf{T}^{-1} \times \vec{y}$. However, it is only possible to invert $\mathbf{T}$ if it is a full-rank matrix – for this reason, the rank of $\mathbf{T}$ sets the maximum number of sensors M that can be accessed via the architecture. This is in turn a function of the number of frequency channels, which is set by the number of DCO frequency-control bits N, equal to the number of hopping-code bits from CMOS. In this way, the number of interconnections from CMOS (N) ultimately sets the number of sensors M. Figure 5.6 shows this relationship

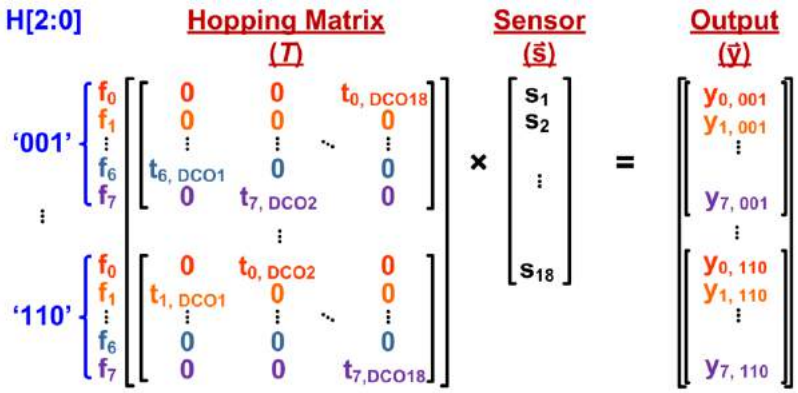


Figure 5.5: DCO hopping patterns for all values of the CMOS hopping code H[2:0] are represented in a matrix $\mathbf{T}$, giving a mathematical relation representing sensor signals $\vec{s}$ and CMOS-TIA outputs $\vec{y}$.

for the proposed architecture; note that to our knowledge there is not a simply analytical expression for the rank of the matrix $\mathbf{T}$, so in this figure each value has been computed in Matlab. The many different ways in which the hopping-code bits can be connected to DCO frequency-control bits leads to rapid combinatorial scaling, allowing the proposed frequency-hopping architecture to outpace active-matrix and even binary-addressing schemes, shown in Figure 5.6 for comparison. For example, even for just $N = 5$, frequency-hopping can access 351 sensors, a greater than 10× improvement over other possible hybrid system interfacing methods like active matrices (25 sensors) and binary addressing (32 sensors). As mentioned, our prototype system employs a 3-bit hopping code ($N = 3$), resulting in a hopping-matrix rank of 19, enabling up to 19 accessible sensors. We choose to prototype a system with $N = 3$ because this corresponds to the first point for which the frequency-hopping scheme shows an advantage over the other approaches. In the demonstrated system, we note that 18, rather than 19, sensors are employed ($M = 18$) for greater regularity in the sensor arrangement.

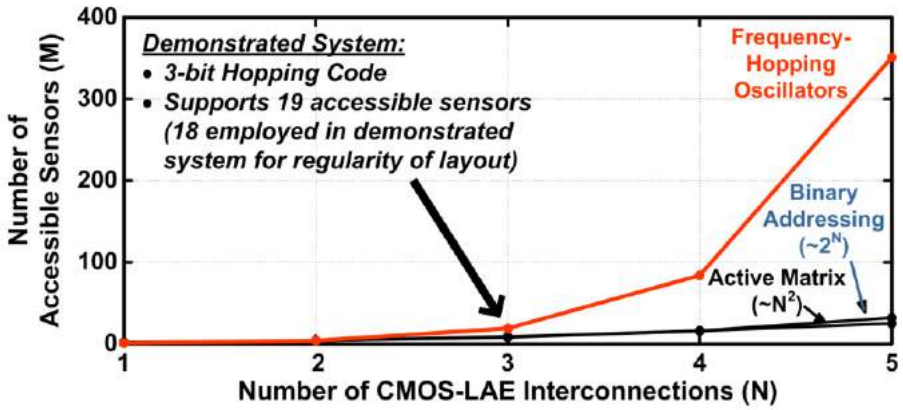


Figure 5.6: Comparison of number of sensors M versus number of CMOS-LAE interconnections N for the frequency-hopping architecture presented and also for existing architectures like active matrix and binary addressing. The presented architecture is able to access more sensors for a given N starting at $N = 3$, the design point chosen for the demonstrated system.

5.1.2 Architecture Design Tradeoffs

The presented architecture has the potential to greatly increase the scalability of hybrid systems, but also raises a number of other design tradeoffs related to dynamic-range requirements, sensor-acquisition rate, and circuit complexity.

For every hopping-code value, all DCO outputs corresponding to the M sensors are summed by a transimpedance amplifier in CMOS. This requires that the CMOS electronics support a large dynamic range, particularly as the number of sensors scales to very large numbers (which is of course the goal of the architecture). However, a key attribute of this architecture is that the increased dynamic range appears only in the CMOS domain, following current summation at the TIA outputs. Because CMOS circuits can have much higher energy efficiency and performance, and can take advantage of many available architectural enhancements for signal processing (e.g., baseline cancellation to only preserve incremental changes in DCO amplitude from sensor-signal modulation), this is a promising tradeoff.

Furthermore, because the summation of DCO outputs is performed across 2^N frequency channels, CMOS demodulation can take advantage of architectures that process frequency channels separately. This can substantially mitigate dynamic-range requirements, particu-

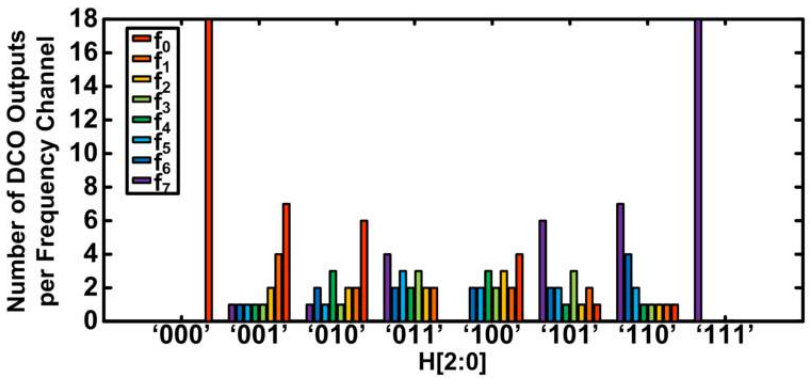


Figure 5.7: Distribution of DCO outputs across all frequency channels (for $N = 3$) for different hopping-code values. Both 000 and 111 are seen to result in outcomes that require the highest dynamic range; excluding these codes from the hopping-code cycle results in a less demanding dynamic range requirement.

larly if we only select hopping codes that result in smaller numbers of DCO outputs per frequency channel. Figure 5.7 shows a histogram of how DCO outputs distribute across frequency channels, for all values of the hopping code in the prototyped $N = 3$ system. Since using all hopping-code values results in many more rows (for N =3, $2^3 \times 8 = 64$) in the $\mathbf{T}$ matrix than its rank (for N =3, 19), many hopping codes can be omitted. In particular, we omit $H[2:0] = 000/111$, in which all DCO outputs appear in just one frequency channel (as seen in Figure 5.7). The remaining hopping-code values yield much more uniform DCO output distributions, reducing the required maximum dynamic range. Similar distribution characteristics are seen for systems with larger N.

The second tradeoff concerns acquisition rate. The presented system, as well as binary-addressing and active-matrix schemes, acquire data from all sensors over a certain number of access cycles, yielding a frame rate. Of course, we cannot consider scaling in sensor number only (as in Figure 5.6) – we must consider both the total number of accessible sensors in addition to the achievable frame rate, which together set the sensor bandwidth that can be supported. Figure 5.8 compares the number of access cycles between the different schemes. In the presented architecture, the number of cycles equals the number of hopping-code values that must be scanned through to provide an invertible hopping matrix. As

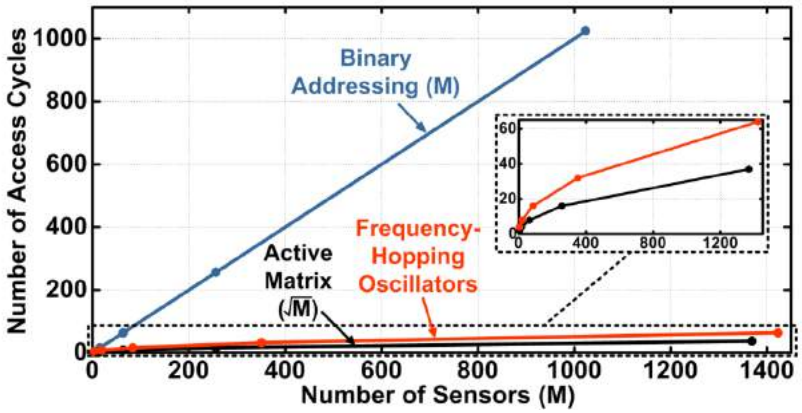


Figure 5.8: Comparison of access cycles required in different sensor-accessing schemes for a given number of sensors M. The presented frequency-hopping approach performs similarly to the active matrix approach, but as showing in Figure 5.6 gives access to far more sensors for a given number of LAE-CMOS interconnection.

shown, while this cycle number is close to the number of cycles required in an active matrix approach, our proposed architecture maintains far fewer interconnections per sensor. As seen, one-by-one sensor accessing with binary addressing yields a very large number of cycles. Furthermore, the presented system could require less time per access cycle, since the DCO output capacitance is absorbed in a resonant tank and no explicit capacitance of a data line needs to be driven; rather, the current is sensed through a TIA virtual ground node.

The complexity of the DCO circuit in our architecture must also increase as the system scales to accommodate more sensors. DCO complexity depends on the number of frequency channels supported. While the circuit implementation has significant potential to ultimately scale to many channels (which will be discussed in more detail in Section 5.2), the presented architecture actually supports scaling the number of sensors *without* scaling the number of DCO frequency channels. Specifically, even if the DCOs maintain 2^N frequency channels (i.e., N frequency-control bits), we can still increase the number of *CMOS hopping-code bits* beyond N. This means that while each DCO retains N frequency-control bits (just as in the original architecture), on the CMOS end, we have *more* than N hopping code bits. This yields more possible ways (e.g., more combinations) in which hopping-code bits can be uniquely

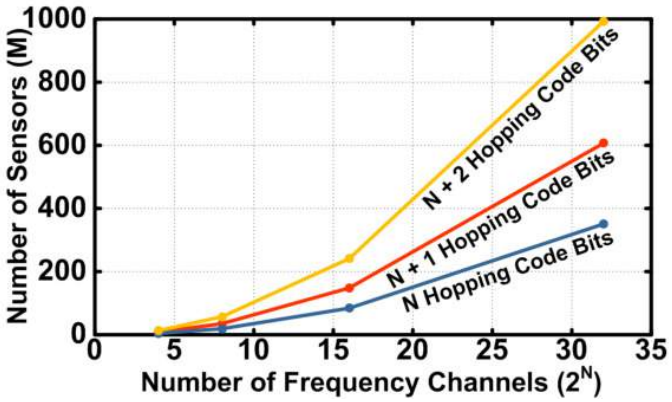


Figure 5.9: For a system with a given N (with 2^N frequency channels), the number of accessible sensors can be increased beyond the number in Figure 5.6 by increasing the number of CMOS hopping-code bits beyond N. This leads to more unique ways in which DCOs can be connected, and hence enables a system with more DCO-sensor pairs without compromising sensor signal reconstruction (e.g., Figure 5.5).

mated with the DCO frequency-control inputs. A larger number of possible unique hardwired connections enables a system that can accommodate more DCO-sensor pairs that all take their own unique frequency-hopping paths – in this way, increasing the number of hopping code bits increases the number of possible sensors M. Figure 5.9 plots the achievable rank of corresponding $\mathbf{T}$ matrices, showing significant potential for the architecture to support more sensors without actually increasing TFT-circuit complexity (e.g., without increasing the number of DCO frequency control bits).

5.2 System Implementation

5.2.1 TFT-Based LC DCO

To build TFT circuits that can demonstrate many distinct frequency channels (e.g., TFT DCOs), we return to the cross-coupled LC oscillator of Section 4.4.2. We showed in the previous chapter that cross-coupled oscillators using high f_{MAX} ZnO TFTs could achieve high frequencies (nearly 40 MHz) by resonating TFT capacitances with high-quality large-area inductors. We can leverage the high oscillator frequencies enabled by our ZnO TFTs

to create a very large number of channels for our frequency-hopping system – this is feat that would be unachievable with our previous lower performance, lower f_{MAX} amorphous silicon TFTs. We must take some additional steps to create digitally-controlled oscillators with many, well-separated channels.

To achieve many distinct channels, the DCO's maximum frequency should be as high as possible: then, many additional channels (separated by a suitable inter-channel spacing) can be added in below the maximum oscillation frequency, making the sensor scaling shown in Figure 5.6 possible. We note that while high f_{MAX} values have been shown in this work, additional TFT optimizations (reducing channel length and lowering overlap capacitances through self-alignment) show further promise for pushing f_{MAX} [205], potentially benefitting the presented architecture.

Once the highest frequency in the oscillator has been established, we introduce lower frequency channels by switching in different combinations of a bank of N binary-weighted capacitors. These capacitors increase the capacitance of the LC tank, modulating the free-running oscillation frequency to one of 2^N values, so long as the oscillation condition (Equation 4.13) is still satisfied for all modified tank capacitances. Figure 5.10a shows the basic DCO topology. The DCO's N binary-weighted capacitors are switched in and out via N TFT switches driven by digital frequency-control signals $X[N-1:0]$, which will ultimately be hardwired to the CMOS control signal $H[N-1:0]$.

Figure 5.10b shows the considerations for designing the TFT switches. Note that when the switch is 'ON', a high-pass filter appears, whose cutoff frequency is set by the TFT's deep-triode on-resistance $R_{ON,b}$ and the bank capacitance $C_{B,b}$. For the DCO to operate, it is essential that the corner frequency of this high-pass filter is well above the highest oscillation frequency of the DCO:

$$f_{HP} = \frac{1}{2\pi R_{ON,b} C_{B,b}} >> f_{DCO,MAX} \tag{5.1}$$

If the TFT's $R_{ON,b}$ is too large, this condition will not be met, and the TFT switch will be unable to pull the bottom plate of the bank capacitor to ground. Instead, the high-frequency

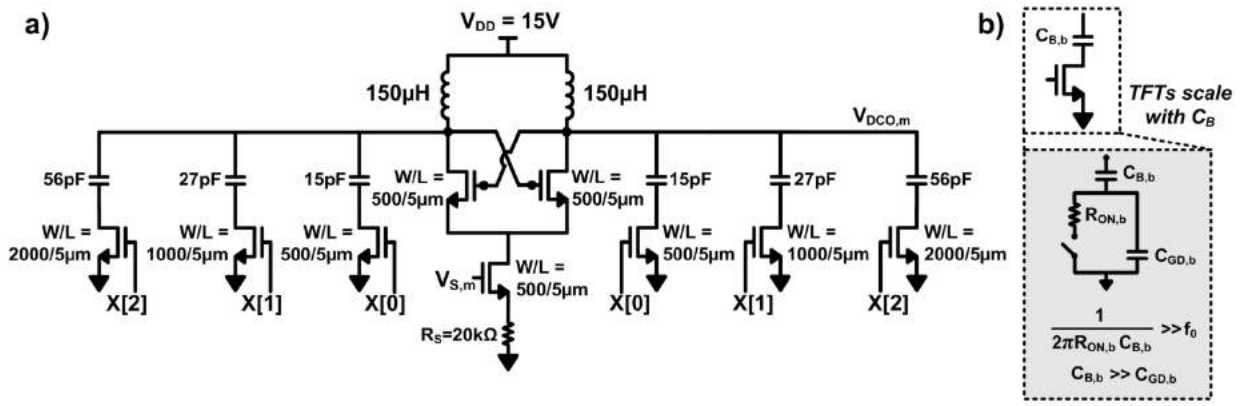


Figure 5.10: (a) DCO design, including all TFT, capacitor, and resistor sizes used in the system. X_{OV} was kept to 5 μm. The design incorporates a bank of switched, binary-weighted capacitors, each controlled by an appropriately-sized TFT switch. A source-degenerated tail TFT ensures a linear relationship between the sensor signal voltage $V_{S,m}$ and the DCO output amplitude. (b) The TFT switches are designed for appropriate on resistance $R_{ON,b}$ and drain capacitance $C_{GD,b}$.

oscillation at the DCO output node will pass through unfiltered and the capacitor will fail to charge, and will have no capacity to increase the tank capacitance and thereby reduce the DCO's oscillation frequency. We can see this effect in the simplified circuit measured in Figure 5.11, where (in a $N = 1$ DCO) we simulate the switch TFT as a resistor R_{ON}, and sweep its resistance for different widths of the cross-coupled TFTs (different widths correspond to different unperturbed tank capacitances and hence different DCO frequencies). In all three curves, only when R_{ON} is below ~ 1 kΩ do we see that the oscillation frequency is pulled down from its initial value (e.g., without C_0).

To ensure a TFT with small $R_{ON,b}$, we can make the width of the TFT large. However, increasing the TFT width results in a proportional increase in the parasitic gate-to-drain overlap capacitance $C_{GD,b}$. This parasitic TFT capacitance must be kept significantly smaller than the corresponding bank capacitor ($C_{GD,b} << C_{B,b}$), or the separation between "ON" and "OFF" frequency channels will be reduced, as seen for the $N = 1$ case in Equation 5.2:

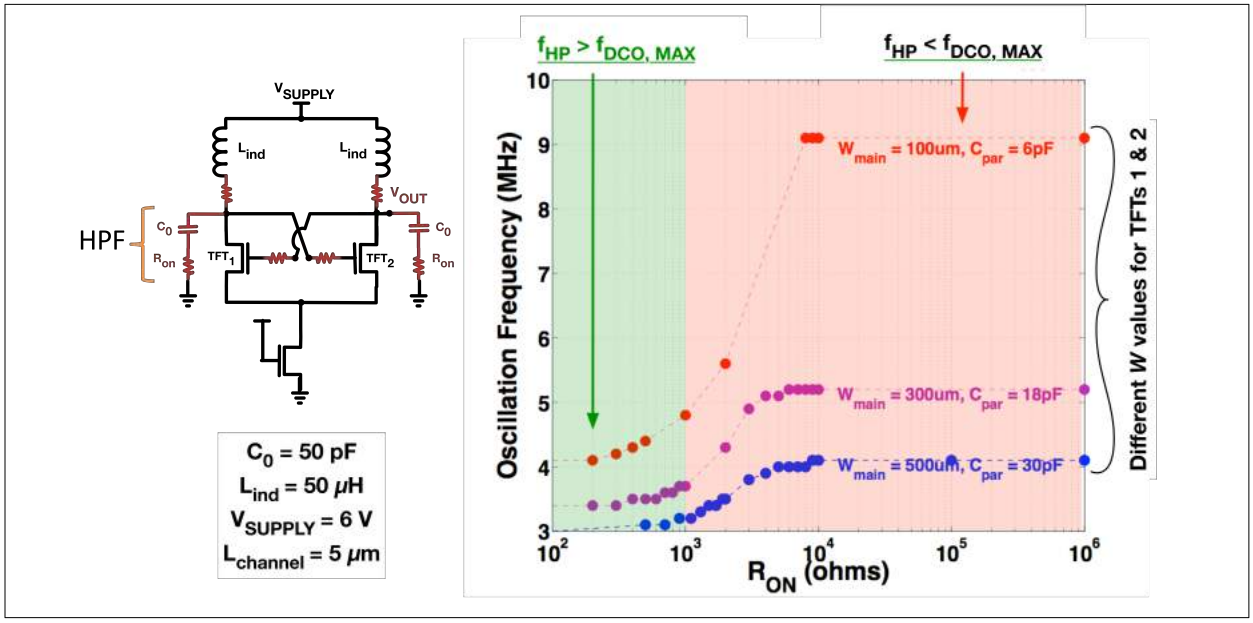


Figure 5.11: Simulation showing how oscillator frequency is unchanged by bank capacitor C_o for high values of switch TFT "R_{ON}", modeled here as a fixed resistor. This analysis indicates that a TFT R_{ON} in triode of 1 kΩ or less is required for circuit operation; above this on-resistance value, the DCO frequency is only partially reduced due to the HPF. W_{main} corresponds to the width of the cross-coupled TFTs; tail TFT width is 100 μm; channel lengths and overlap dimensions for all TFTs are 5 μm.

$$\frac{f_{ON}}{f_{OFF}} \propto \sqrt{\frac{C_{TANK,0} + \frac{C_{B,b}C_{GD,b}}{C_{B,b}+C_{GD,b}}}{C_{TANK,0} + C_{B,b}}} \tag{5.2}$$

where $C_{TANK,0}$ is the capacitance of the tank without the addition of bank capacitors and TFTs (e.g., capacitance of the cross-coupled TFTs and the parasitic capacitance of the inductors only). In other words, we will not be able to turn the TFT switch "OFF" because its own capacitance becomes comparable to the bank capacitor value. We note that since the gate and source of the switch TFT are grounded in the switch "OFF" state, this parasitic TFT capacitance comes from the TFT gate-to-drain overlap capacitance $C_{GDS,b}$ only, since there is no charge in the channel. We observe this effect in the simulation of oscillation frequency versus switch TFT channel width in Figure 5.12 and again in measured power spectral density plots (PSDs) from DCO outputs using four different switch TFT widths in

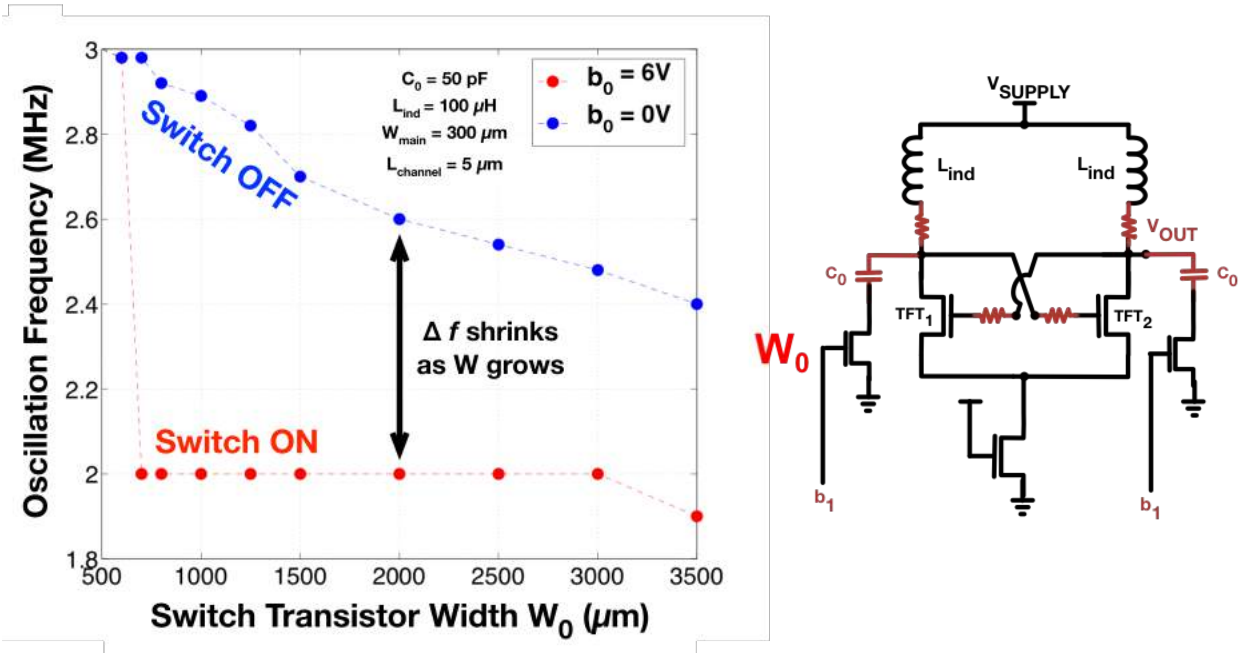


Figure 5.12: A simulation of ZnO TFT switches of increasing width W_0 shows that, for a C_o of 50 pF, all W_0 values above 600 μm can adequately "turn on" and charge the capacitor. However, the wider TFTs contribute extra capacitance that degrades the channel spacing between "on" and "off" conditions. W_{main} corresponds to the width of the cross-coupled TFTs; tail TFT width is 100 μm; channel length for all TFTs and overlap dimension are 5 μm.

Figure 5.13 for a simplified $N = 1$ DCO, where the separation between "ON" and "OFF" states is clearly reduced for larger switch TFT widths.

Hence, W should be made as small as possible while satisfying Equation 5.1 to maximize channel spacing. For the TFTs employed, deep triode $R_{ON,b} \approx 500$ kΩ/W and $C_{GD,b} \approx$ 0.01 pF$\times$W (where W is the TFT width in μm); this results in a HPF cutoff frequency of $\frac{1}{2\pi R_{ON,b} C_{GD,b}} \approx 30$ MHz. Based on these values, we (conservatively) design our DCOs to have 8 nominal channel frequencies of 1.36, 1.27, 1.20, 1.13, 1.07, 1.03, 0.99, and 0.95 MHz; the bank capacitor values, TFT sizes, and inductor values used are as shown in Figure 5.10a. This design point results in a value of 2–6 in the oscillation condition (Equation 4.13), ensuring robust oscillations.

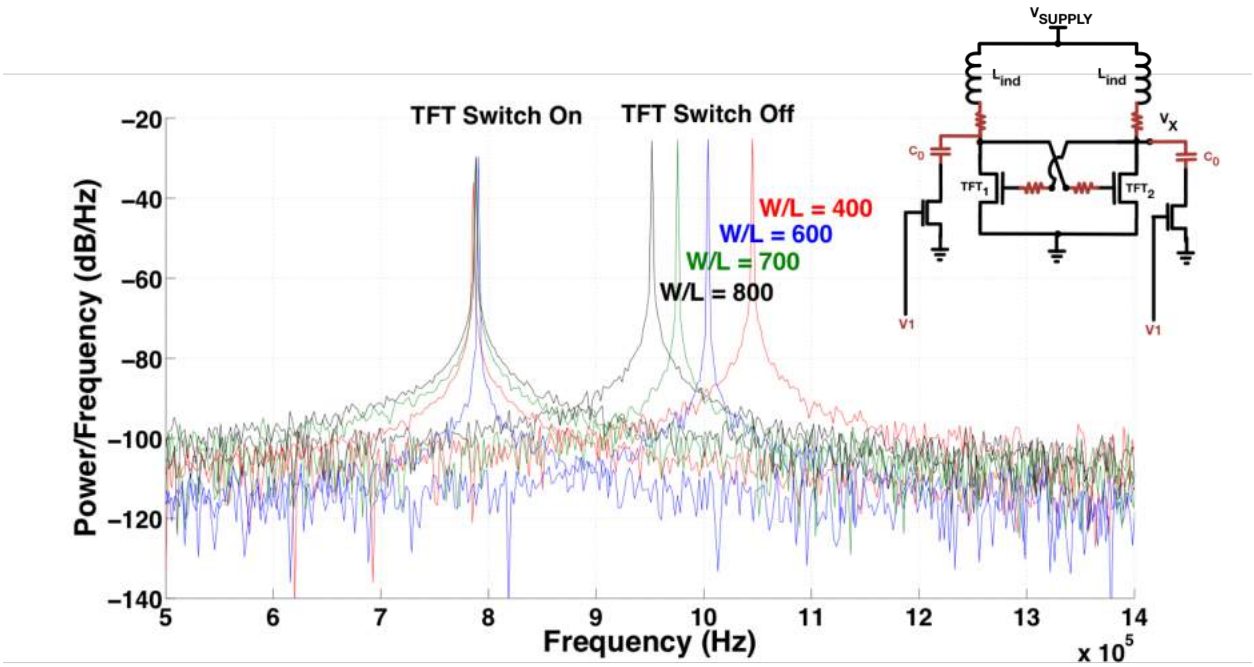


Figure 5.13: Measured oscillator output PSDs using ZnO TFT switches with four different W/L ratios show that, for a C_o of 100 pF, all W/L values can adequately "turn on" and charge the capacitor. However, the wider TFTs contribute extra capacitance that degrades the channel spacing between "on" and "off" conditions. Cross-coupled TFT width is 500 μm; channel length for all TFTs and overlap dimension are 5 μm; L_{ind} = 200 μH.

Figure 5.14 shows the measured power-spectral density plot for one DCO (dimensioned as in Figure 5.10a) for the different values of $X[2:0]$. Because the capacitance-to-frequency relationship is nonlinear ($f = 1/2\pi\sqrt{LC}$), the separation between frequency channels is also non-uniform. At the design point, the minimum nominal channel spacing is seen to be 40 kHz.

In order to use the sensor signal $V_{S,m}$ to modulate the amplitude of the DCO output, we connect $V_{S,m}$ to the gate of a tail transistor, as shown in Figure 5.10a. The tail transistor acts as a throttle valve for the oscillator, restricting current flow I_{DCO}. Because $I_{DCO} \propto V_{DCO}$ (the amplitude of the DCO output), changes in $V_{S,m}$ result in changes to V_{DCO}, leaving the oscillation frequency of the overall DCO unchanged to first order (recall its frequency is set by the tank capacitance and the inductor value, as in Equation 4.12). Some second order frequency variations do result from $V_{S,m}$; these will be discussed in Section 5.2.2.

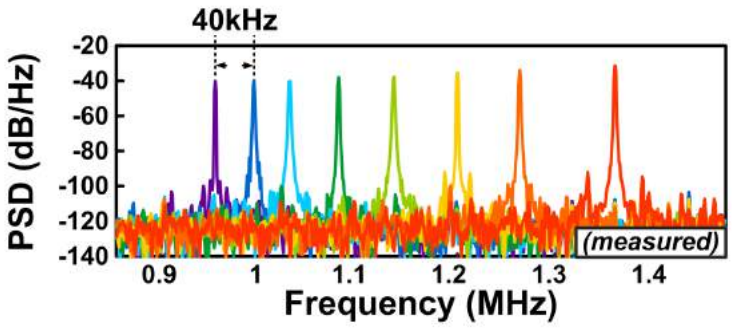


Figure 5.14: Measured power spectral density for one oscillator showing minimum inter-channel spacing of 40 kHz; measured by cycling through all 8 possible combinations of the 3 digital control signals. Circuit elements sized according to Figure 5.10.

In order to reconstruct $V_{S,m}$ via the matrix inversion discussed in Section 5.1, it is essential that the relationship between the sensor voltage $V_{S,m}$ and DCO output amplitude $V_{DCO,m}$ be linear; deviations from linearity will result in error in the reconstructed sensor signal.

We could use a tail transistor on its own to modulate V_{DCO}. Figures 5.15 and 5.16 show simulation and measurement results for the $V_{S,m}$ to oscillator-output transfer function for such a circuit, which indicate that a smaller-width tail TFT will be able to modulate the DCO current over a broader voltage range than a wider TFT. However, for all widths, we see that the $V_{S,m}$ range for which the output follows linearly is relatively small.

For this reason, we source-degenerate the tail TFT. Figure 5.18 shows the $V_{S,m}$-to-V_{DCO} transfer function with and without a 20 kΩ source-degeneration resistor (configured as in Figure 5.10a), and indicates that the maximum linear range for the sensor input doubles from 2 V (e.g., 6 V to 8 V) to 4 V (e.g., 8 V to 12 V) after source degeneration. We note that the maximum linear range for the source-degenerated case generally increases as the drain voltage on the tail TFT increases (Figure 5.17 shows a simulation), which requires increasing the supply voltage to the DCO at the cost of power consumption; for this reason, in the demonstrated system, we use a supply voltage of 15 V.

Figure 5.19a shows the change in the measured DCO output waveform in one of the frequency channels over a 4-V input range. To restrict our system to an even more linear

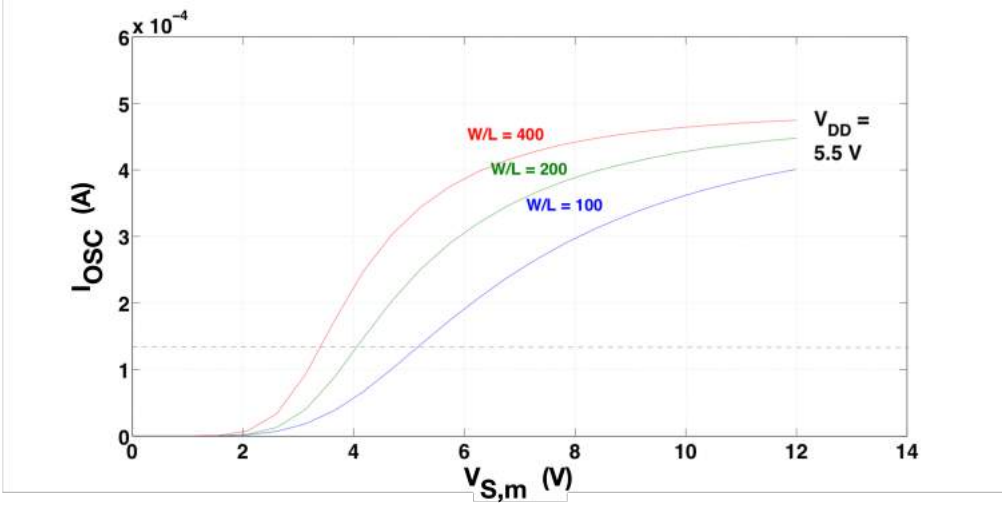


Figure 5.15: A simulation of a simple cross-coupled oscillator (W/L = 500/5 μm) with a tail transistor of varying width (for L = 5 μm) results in some degree of control over the oscillator current ($\propto V_{DCO}$), but the relationship between the tail bias $V_{S,m}$ and the oscillator current is generally nonlinear, even for the best-case, narrower tail TFTs.

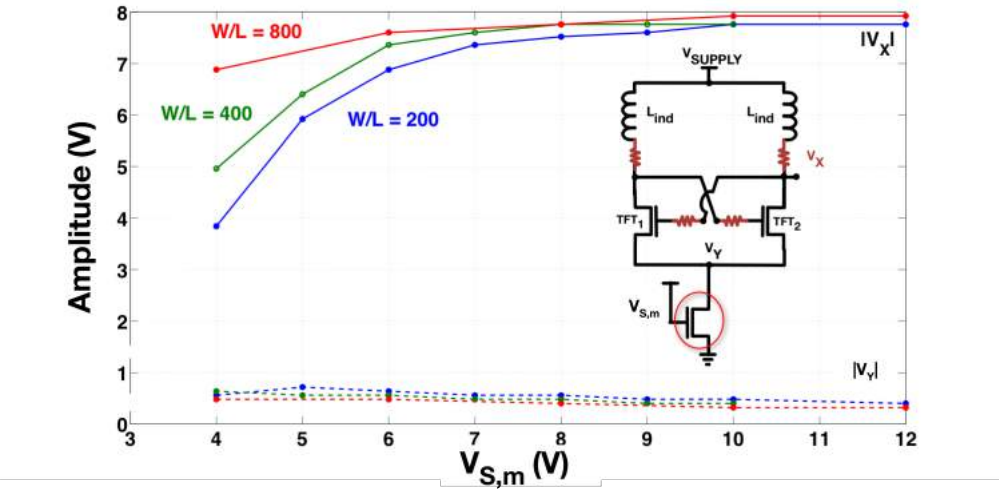


Figure 5.16: A measurement of a simple cross-coupled oscillator (W/L = 500/5 μm) with a tail transistor of varying W (L = 5 μm) results in some degree of control over the oscillator output amplitude, but the measured relationship between the tail bias $V_{S,m}$ and the output amplitude is generally nonlinear.

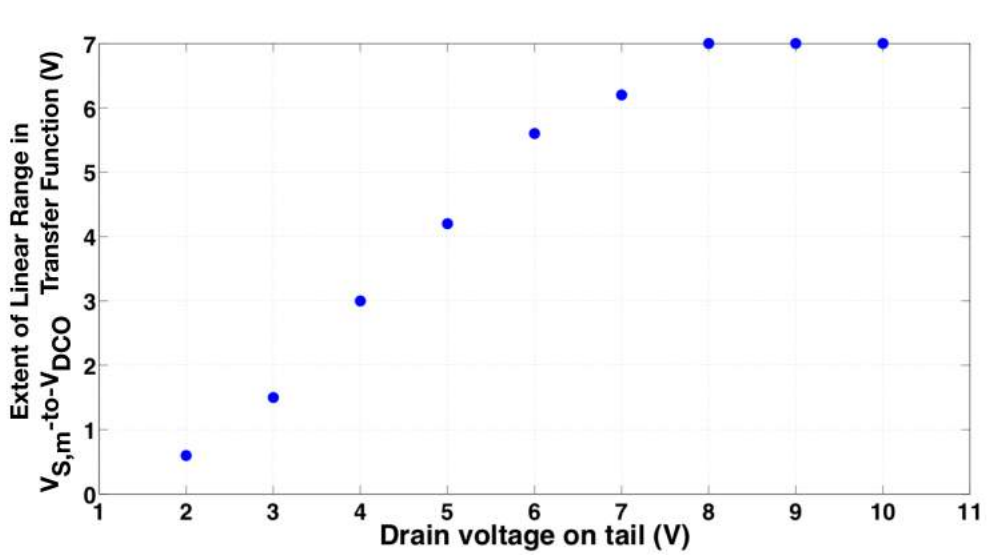


Figure 5.17: In this DCO simulation (sizes as in Figure 5.10), linear range in sensor voltage-to-DCO output increases when tail TFT drain voltage increases, necessitating an increase in DCO supply voltage.

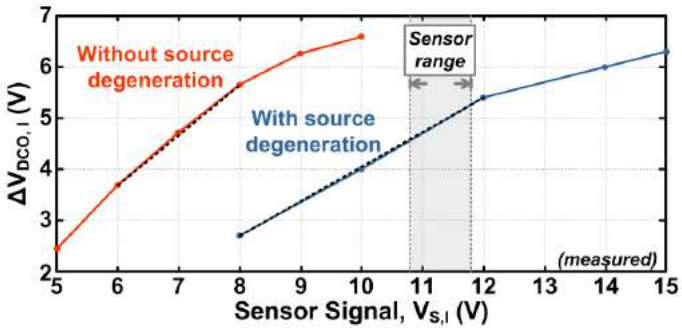


Figure 5.18: In this measurement of the $V_{S,I}$-to-$V_{DCO,I}$ transfer function with and without source degeneration of tail transistor (sizes as in Figure 5.10), we see that the linear region of the transfer function (identified with a dotted black line) is doubled with the use of a source-degeneration resistor. Linearity is essential for accurate signal reconstruction; having a large linear area increases the resolution of the sensing system.

portion of this curve, we design the sensor range in the demonstrated system to only be 1 V.

Figure 5.19b plots the source-degenerated transfer function, showing the linearity achieved.

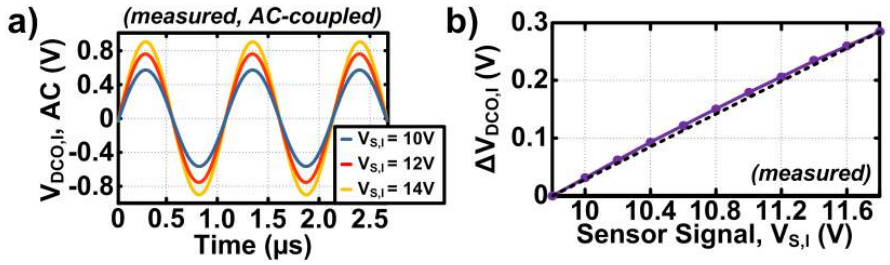


Figure 5.19: Measured amplitude modulation of a DCO output $V_{DCO,I}$ for changing values of the input sensor signal $V_{S,I}$ is visible in (a) the time-domain waveform, and (b) in the $V_{S,I}$-to-$V_{DCO,I}$ transfer function, shown in purple (linear fit in black) for one of the DCO frequency channels (f_7).

5.2.2 Designing a DCO Array to Minimize Variation

Thus far, we have described design and operation of one ZnO TFT DCO, demonstrating eight well-separated frequency channels and linear amplitude modulation. Of course, the system architecture requires fabrication of many such DCOs, all of which should ideally be identical so that sensor signals are projected into identical frequency channels. In practice, there are many sources of variation that must be controlled in order to build a functional system. Figure 5.20 shows power spectral density plots for 20 cross-coupled oscillators on one sample that have been designed to oscillate at the same frequency. Across these oscillators, a frequency spread of 250 kHz is observed – this is 6× our desired inter-channel spacing, which is highly undesirable!

Because the resonant frequencies of presented circuits are set by the capacitances of their tanks, it is essential first to ensure that C_{TANK} is consistent across different DCOs. We find that there are four practical sources of C_{TANK} variation; two can be mitigated through layout, while the other two require more sophisticated treatment that will be discussed in the following section.

First, as we fabricate our ZnO TFTs in a research cleanroom, we do not have access to state-of-the-art automatic aligner tools that guarantee perfect alignment between lithographic masks – most significantly, the gate and source/drain layers. This results in overlap

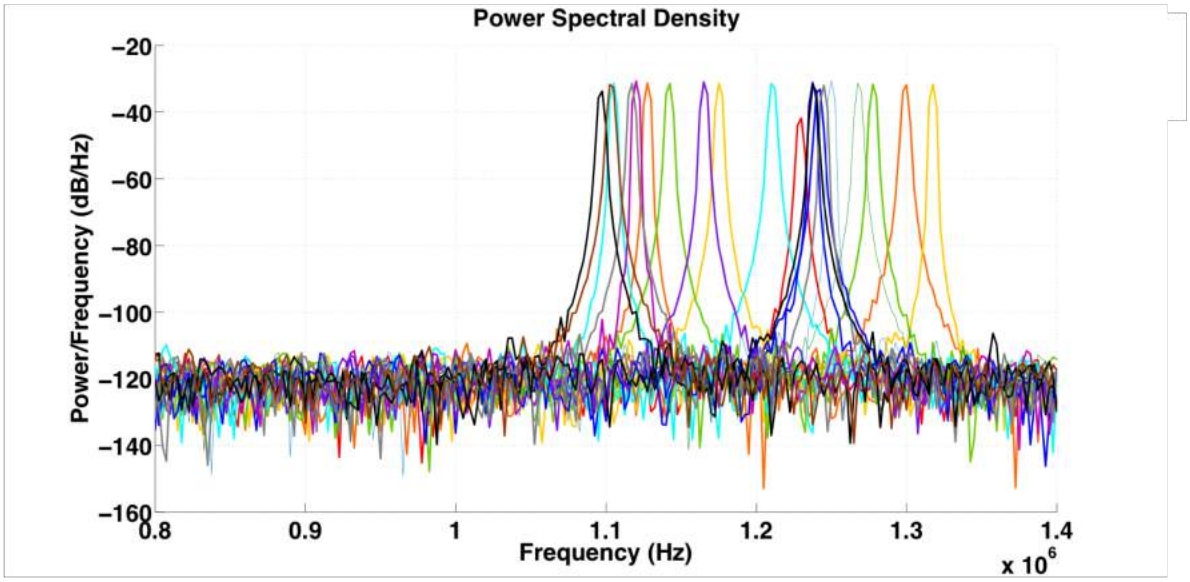


Figure 5.20: Asymmetric interconnect layout results in significant additional capacitances that create DCO frequency spread. Here we see power spectral density plots for 20 cross-coupled oscillators on one sample designed to oscillate at the same frequency, where a 250 kHz spread is observed due to asymmetric probe card PCB capacitances. Note that this is 6× our desired inter-channel spacing.

capacitance variation of up to 200% on a single sample. While this problem occurs on glass samples in a research setting, even industrial fabrication environments will experience this problem when handling freestanding flexible substrates, as discussed in Section 3.5.1. While self-alignment presents one means of bypassing this issue, a simple layout solution is also available when self-alignment is not an option: by splitting the channel into two legs, we can produce symmetric capacitances across the whole sample, as misalignment on one leg of the channel is compensated by the misalignment in the second leg of the channel, as shown in Figure 5.21.

Second, we must connect TFTs together to form circuits. As we generally like to optimize layouts for density, squeezing as many circuits onto one sample as possible to account for imperfect yield, the resulting interconnects are usually asymmetric. Of course, the metal interconnections themselves (especially in high-density layouts) will contribute their own parasitic capacitances (a few pF) to each DCO. So long as we can design the interconnect

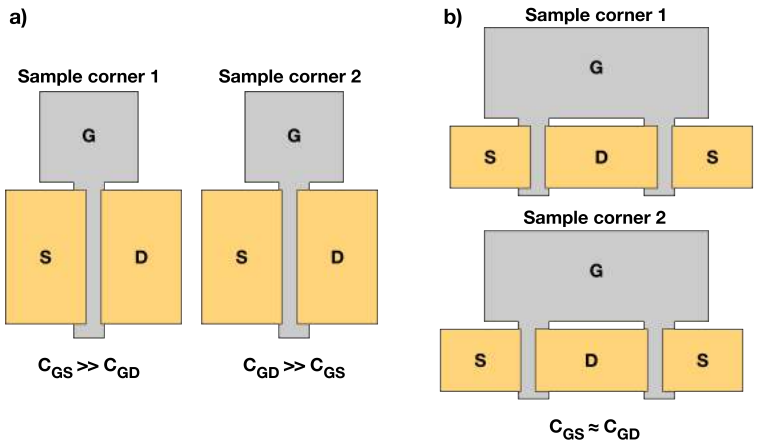


Figure 5.21: Mask layout strategy to control DCO tank capacitance variation due to alignment errors across samples. In (a), we see a standard TFT layout: when misalignment occurs, the source and drain overlaps are mismatched, resulting in overlap capacitance mismatch that changes DCO free-running frequencies. In (b), we see a two-legged gate design, in which misalignment in one leg of the TFT is compensated to first-order by the opposite misalignment of the second leg of the TFT.

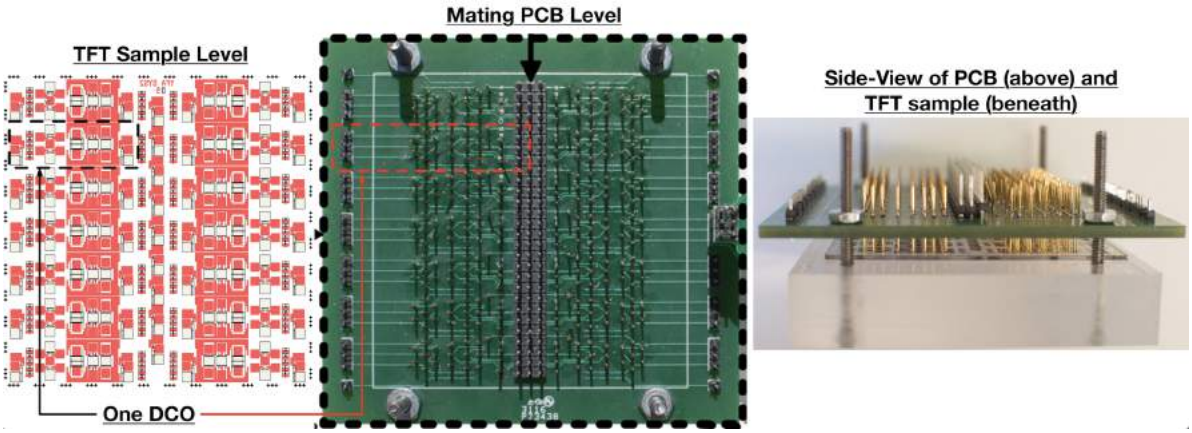


Figure 5.22: Mask layout (left) and PCB layout (middle) mate together and are designed to be identical and symmetric from DCO to DCO. They contact each other using gold pins, visible in the side view (right)

layout to be symmetric and identical from one DCO to the next, these parasitics can be accounted for and will remain consistent from DCO to DCO.

In our system demonstration, we replace thin-film interconnects with a custom PCB "probe card" for ease of testing. The probe card consists of an array of spring-loaded gold

pins that mate with large contact pads on our TFT sample. The interconnections can then be formed in the two-layer PCB. Hence, we co-design the TFT sample and the custom PCB to be as symmetric as possible, as shown in Figure 5.22.

By controlling layout-induced sources of capacitance variation, we are able to reduce oscillator frequency spread by a factor of ten from what we measured in Figure 5.20 – the remaining frequency spread can be seen in Figure 5.28 in the next section.

The remaining sources of DCO frequency variation are more difficult to avoid. The first stems from variations in the properties of the gate insulator material (thickness and/or dielectric constant) across the TFT sample. While this variation (shown in Figure 5.28 in the next section) can be more tightly controlled in an industrial fabrication environment, it will always exist in some capacity. The second observed source of variation is a reduction in oscillation frequency in all channels as the oscillator current is increased (e.g., as the tail TFT bias $V_{S,m}$ increases), shown in Figure 5.23 for one DCO. Because each sensor signal may be different, even DCOs that are identical in all of the above respects will still exhibit slightly different oscillation frequencies because their respective $V_{S,m}$ values will vary. This variation stems from small changes in TFT capacitance as the gate bias is changed (e.g., the C–V curve does not completely saturate in the bias range used). Though this last variation source is less significant than the other three sources, it must be considered. Thankfully, we can use the same strategy to overcome both of these unavoidable sources of frequency variation, as we discuss next.

5.2.3 Injection-Locked DCO Array

In order to accurately sum all sensor values in the LAE array by summing DCO outputs in the TIA, all DCOs in the array must be both phase and frequency synchronized. Otherwise, we will encounter a host of problems; for example, equal amplitude signals with identical frequency that are 180° out of phase will simply cancel each other out! Phase and frequency variation are expected in the DCO array: phase variation arises because the oscillators turn

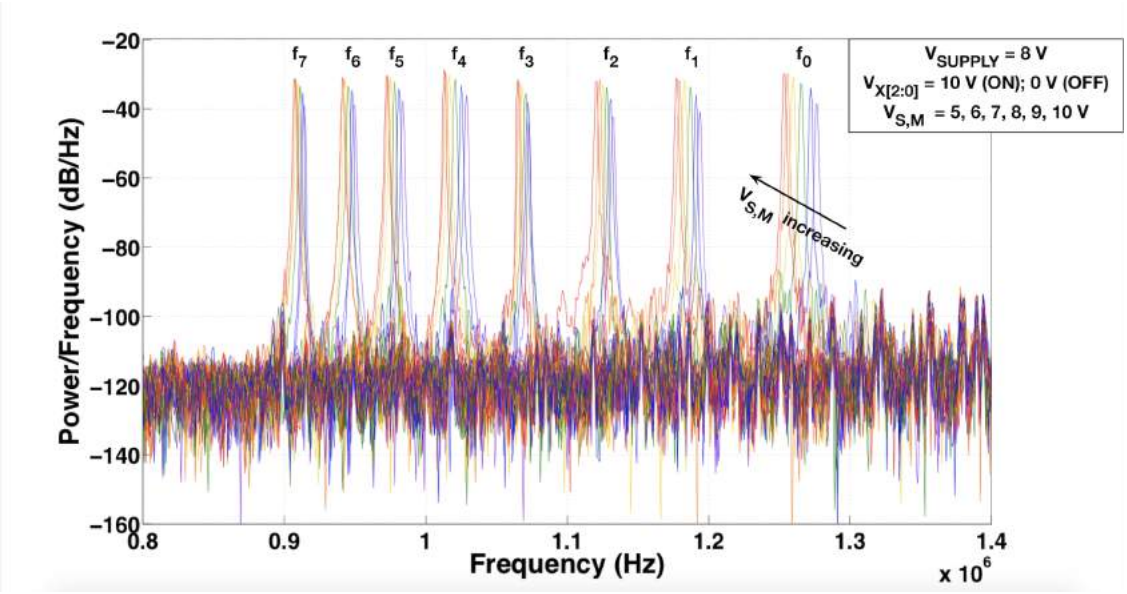


Figure 5.23: Changing the tail TFT bias (sensor signal) $V_{S,m}$ over a 6-V range results in measurable changes in oscillation frequency in all 8 DCO frequency channels, as seen in this power spectral density plot measured for one DCO. In practice, our tail voltage range is only 1 V, making this error source smaller than the other causes of DCO frequency spread.

on at different times, and frequency variation (aside from what can be controlled via layout as discussed) is a result of tank inductance and capacitance variations. In particular, the tank capacitance is set in part by TFT overlap capacitances (as described in Section 5.2.1), and is subject to variation in Al_2O_3 thickness and/or dielectric constant variation.

To achieve phase/frequency synchronization, we employ injection locking, as discussed at length by Prof. Razavi in [206]. As shown in Figure 5.24, this is done by introducing currents $I_{REF,0^\circ}/I_{REF,180^\circ}$ into the LC tank at a desired reference frequency. These reference currents then add with the TFT currents $I_{OSC,0^\circ}/I_{OSC,180^\circ}$, to give the tank currents $I_{TANK,0^\circ}/I_{TANK,180^\circ}$. If the reference frequency falls sufficiently near the free-running resonant frequency of the oscillator, we can pull the oscillator off of its resonant point and lock it to the reference signal. We note that in being pulled off its resonant point, the tank's voltage exhibits a phase offset with its current, set by its impedance, as shown schematically. Furthermore, because $I_{OSC,0^\circ}/I_{OSC,180^\circ}$ change with the value of the sensor signal $V_{S,m}$ (for DCO amplitude modulation), $I_{TANK,0^\circ}/I_{TANK,180^\circ}$ change in both their amplitude and

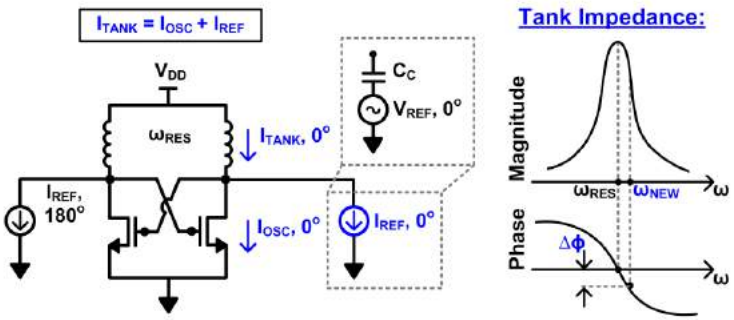


Figure 5.24: Injection-locking principle, based on [206]. A differential reference signal I_{REF} at the desired reference frequency ω_{NEW} is introduced into the oscillator (in our case, this signal is a CMOS-generated voltage, coupled via capacitor C_C). The oscillator can be pulled off its own resonant frequency ω_{RES} and locked at the new frequency dictated by the reference signal, depending on the magnitude of the reference signal. This results in a fixed phase offset between the reference signal and the oscillator.

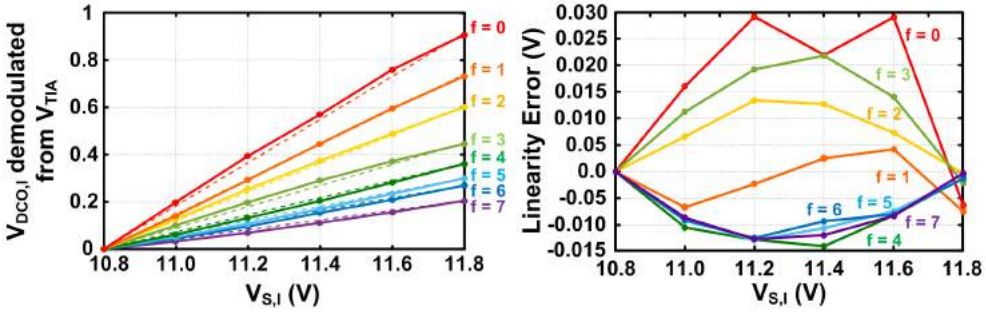


Figure 5.25: Measured relationship between sensor input voltage and output amplitude of a locked DCO in each frequency channel with linear fits in dashed lines (left) and linearity error (right). This transfer function is required for reconstruction, and its linearity enhances the reconstruction accuracy.

phase, with respect to the reference signal. Nonetheless, as seen in Figure 5.25 for a typical DCO, measurements of $V_{S,m}$-to-$V_{DCO,m}$ transfer functions (left) and linearity error (right) in each channel for locked DCOs show that good linearity is maintained over the sensor range, which is designed to be 10.8 – 11.8 V, although linearity degrades as this range is increased.

In the demonstrated system, we generate reference signals in the CMOS domain at each of our 8 desired reference frequencies. In our approach, all DCOs can be locked simultaneously in their respective frequency channels. This is possible because reference signals

sufficiently far from the oscillator's free-running frequency will have a negligible effect, because $I_{REF,0^\circ}/I_{REF,180^\circ}$ will be filtered out by the diminished tank-impedance magnitude response of the oscillator (as shown in Figure 5.24) for $\omega_{NEW} << \text{or} >> \omega_{RES}$. This means that there is a finite locking range for each DCO and each frequency channel. The extent of this lock range can be controlled via the magnitude of $I_{REF,0^\circ}/I_{REF,180^\circ}$ [206].

We exploit this fact to achieve simultaneous locking in all channels, as pictured in Figure 5.26 for the $N = 3$ system. The sum of $2^N = 8$ reference sinusoids (at the desired nominal channel frequencies) is applied to the reference node of the CMOS TIA. The TIA's feedback condition causes the sum to then appear at the virtual ground node, which couples back to all DCOs through the C_Cs. This is done differentially through the two TIAs, as shown.

The amplitude of each reference sinusoid is chosen to be large enough to ensure locking over all the DCOs (overcoming the frequency spread expected within each channel from Al_2O_3 capacitance variations), but small enough to ensure that adjacent channels experience negligible frequency pulling. Figure 5.27 illustrates how increasing the $V_{REF,f}$ amplitude increases the lock range in each frequency channel ($V_{S,m}$ is set to a value in the middle of the sensor range).

Figure 5.28 shows the measured power spectral density (PSD) for 11 DCOs, each configured to output in each of the eight frequency channels. The free-running DCOs (top) show substantial frequency spread, which corresponds with the measured variation of the TFT capacitances. The injection-locked DCOs (bottom) show that the frequency spread is eliminated. Furthermore, injection-locking is seen to enhance the spectral purity in all of the frequency channels, raising the possibility of reducing inter-channel spacing and increasing channel number to enhance the scaling in number of sensors in Figure 5.6.

In addition to process-induced TFT-capacitance variation, implementation of the system on flexible foils would introduce inductance variation upon bending. Based on our measurements of inductance variation upon bending in Section 4.4.4, the system is estimated to tolerate bending radii of up to ~25 mm (corresponding to < 1% frequency shift from nomi-

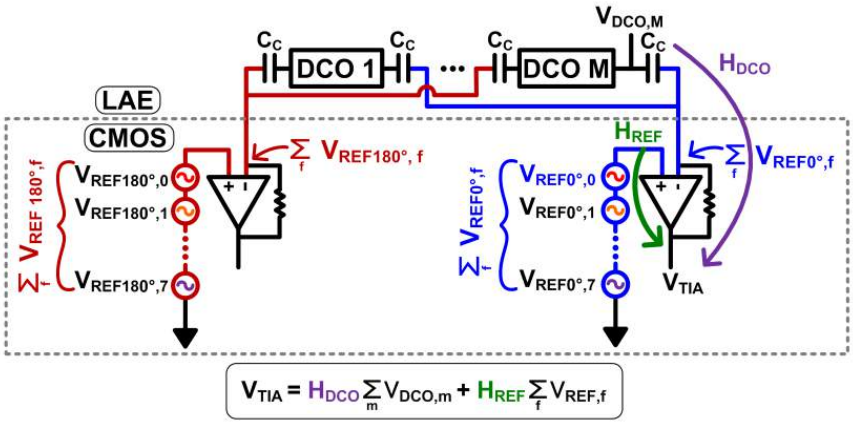


Figure 5.26: Injection-locking implementation: the sum of reference signals (e.g., one V_{REF} for each frequency channel in the system) is applied to the TIA's virtual ground node, where it couples via capacitors C_C to all of the oscillators throughout the array. The expression at the bottom describes the output of the TIA, which now contains a component from the reference signals in addition to the desired DCO output, which contains the sensor signal data.

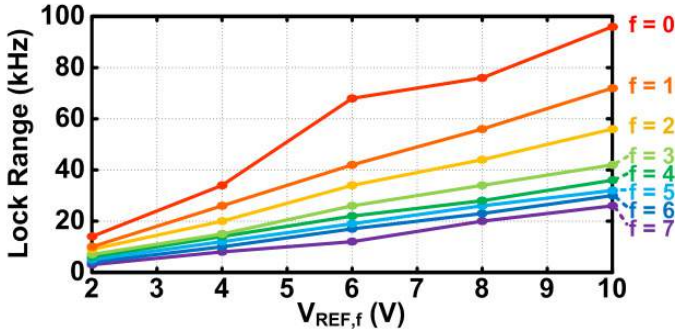


Figure 5.27: Simulated lock range versus reference-signal voltage amplitude for each of the 8 frequency channels in our demonstrated system indicates that the lock range can be tuned to accommodate for increased DCO frequency spread (from increased TFT variation), or reduced to enable narrower inter-channel spacings.

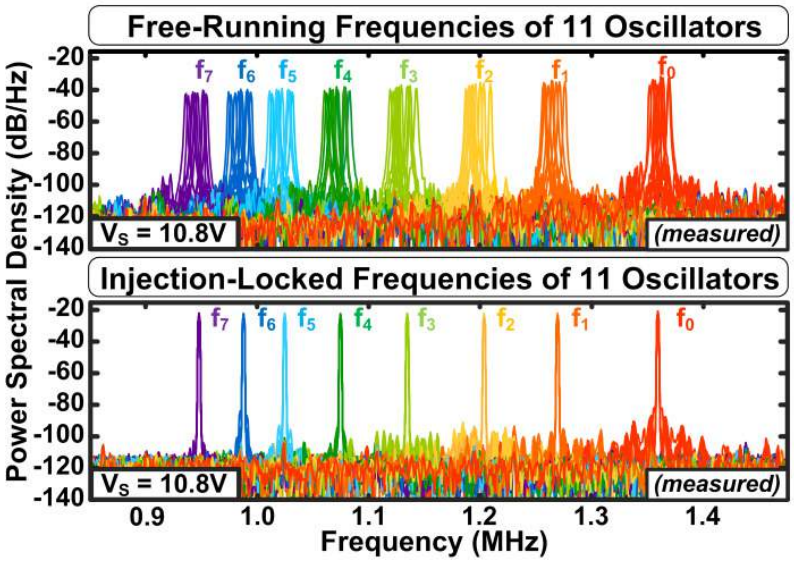


Figure 5.28: Measured PSDs for 11 free-running (top) and injection-locked (bottom) DCOs, configured to output in all 8 channels. The variation in DCO resonant frequencies in all of the 8 frequency channels (due to TFT variations), is visible in the top image, but is eliminated in the bottom image upon injection-locking.

nal values). Bending tolerance could be increased by reducing inductor size, which could be accomplished for example by using self-aligned TFTs.

5.2.4 Sensor Signal Demodulation

Recall that our goal is to reconstruct the sensor signals $V_{S,m}$, represented by the vector $\vec{s}$, by using the matrix relationship $\vec{y} = \mathbf{T} \times \vec{s}$, where $\mathbf{T}$ is the "hopping matrix" (described in Section 5.1), and $\vec{y}$ is a vector whose elements represent the sum of all the sensor signals in each frequency channel for each value of the hopping-control code.

Ideally, the elements of $\vec{y}$ could be retrieved by simply demodulating the output of the CMOS TIA V_{TIA} in each of the frequency channels. However, demodulation is complicated somewhat by injection locking. As shown in Figure 5.26, V_{TIA} consists of two components: (1) the sum of the DCO outputs, through the transfer function H_{DCO}, and (2) the sum of the injection-locking reference signals, through the transfer function H_{REF}. Thus, the

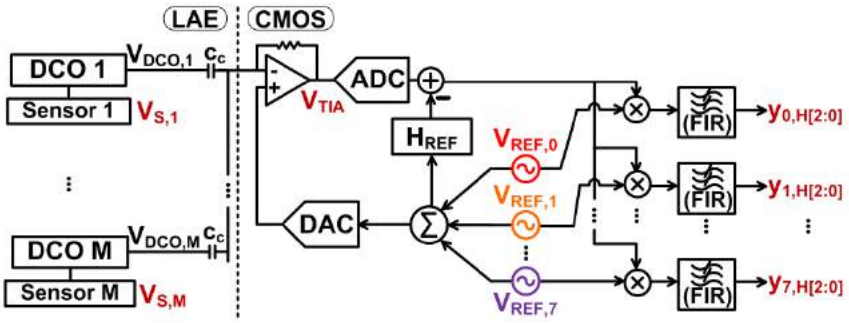


Figure 5.29: The output of the TIA contains sensor data and reference signal data. To separate the reference signal information from the desired output in each frequency channel $y_{f,H[2:0]}$, we perform demodulation in the CMOS domain. This involves 1) removal of reference-signal component, 2) mixing with the corresponding reference signal, and 3) low-pass filtering (FIR).

component of V_{TIA} due to the reference signals must be removed before the elements of $\vec{y}$ can be demodulated.

The demodulation process is shown in Figure 5.29. First, the sum of injection-locking reference signals is generated in CMOS. This is applied to the TIA reference node via a DAC, and also applied to the transfer function H_{REF}, where is subtracted from the digitized V_{TIA} output. The resulting signal is then demodulated, using each of the individual injection-locking reference signals. Lastly, low-pass FIR (finite impulse response) filtering is applied to each demodulated output to filter signals from other frequency channels, recovering only the sum of sensor signals in the corresponding frequency channel. The demodulated and filtered outputs from each frequency channel then form the elements of $\vec{y}$.

However, to complete reconstruction of the sensor data, we must still determine the values of the matrix $\mathbf{T}$. These matrix entries are derived from the linear transfer function from $V_{S,m}$-to-$V_{DCO,m}$, and then from $V_{DCO,m}$-to-V_{TIA} (H_{DCO}). Nominally, the non-zero matrix elements would all be equal. In practice, however, the transfer functions are different for each frequency channel, since $V_{S,m}$-to-$V_{DCO,m}$ depends on the tank Q and $V_{DCO,m}$-to-V_{TIA} depends on the impedance of C_C which will change for the different frequencies. To determine the transfer functions, we use a calibration stage, as shown in Figure 5.30. For each frequency

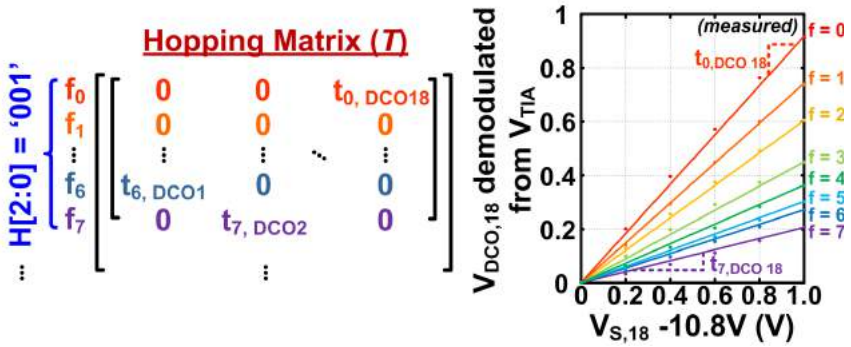


Figure 5.30: The entries of the hopping matrix **T** are derived from the $V_{S,m}$ to V_{TIA} transfer functions in each frequency channel: after a linear fit is performed for each channel's transfer function, the slope of this fit is the matrix entry for that frequency and that DCO.

channel, the sensor-voltage input for each DCO is swept through its full range (e.g., 10.8 V – 11.8 V), and the value of V_{TIA} is demodulated. A linear fit to the demodulated output values is then performed to establish the corresponding entry of the **T** matrix.

Aside from dependence on frequency channel, the transfer function associated with each DCO is also impacted by process variations. First, variation in the mobility and threshold voltage of the DCO tail TFT directly affects the conversion of $V_{S,m}$ to $V_{DCO,m}$, as is typical in a modulator, although this variation is not found to be significant (measurements provided in the following section). Second, injection locking introduces a new dependence on TFT capacitance variation: because all oscillators have their own free-running frequencies (set by their slightly different tank capacitances), each oscillator exhibits a different phase offset between its free running frequency and the reference frequency.

We can see this in the plot of the phase offset versus the difference between the free-running frequency and the reference frequency (Δf_{lock}) for 11 DCOs configured to output in one frequency channel (f_7) in Figure 5.31 – the relationship is seen to be roughly linear. This variation in phase offset is observed to cause sensor acquisition error in the demonstrated system by aggravating transfer function nonlinearity upon demodulation. Specifically, as seen in Figure 5.24, the tank impedance is a function of this phase offset. We analyze the impact of this on the presented system in simulation, as described next.

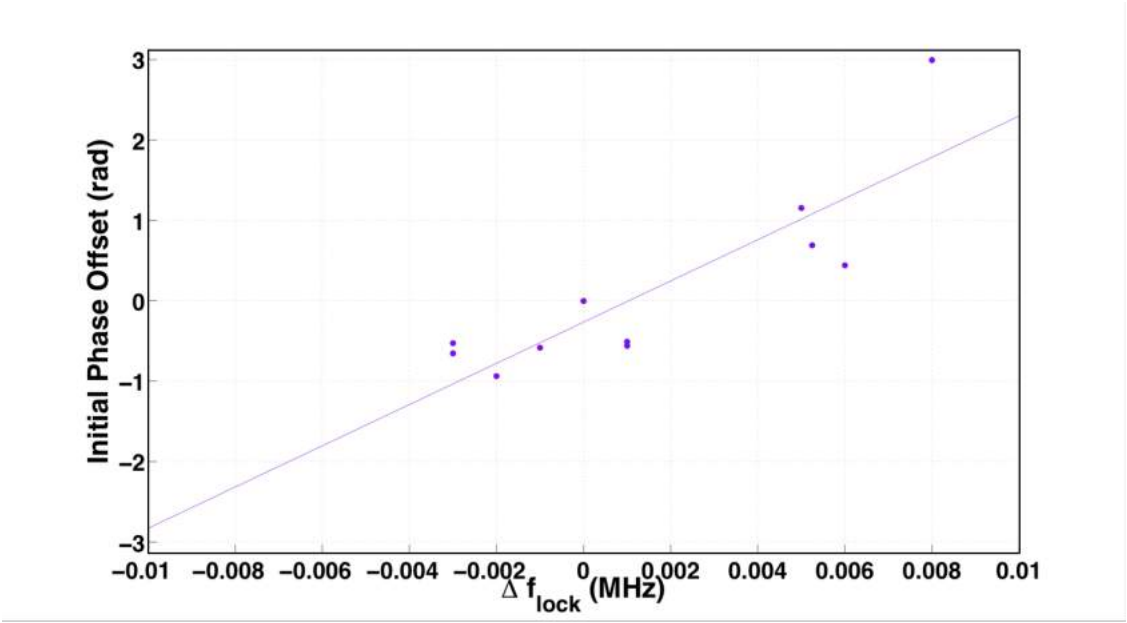


Figure 5.31: Each DCO has its own free-running frequencies, and hence its own frequency offsets from each of the reference signals. This results in a different phase offset for each DCO output with respect to the reference signal upon injection-locking. Plotted here are the measured phase offsets between the DCO output voltage signals (measured at the TIA output) and the locking signal for channel 7; we see that the phase offset varies linearly with the frequency offset (e.g., $\delta f_{lock} = f_{freerunning} - f_{REF}$) for all 11 DCOs. Linear fit superimposed in solid line.

To better understand the relationship between oscillator variation and reconstruction error, we use a simulation in which we assume that the set of free-running frequencies in each of the frequency channels for all the DCOs in the array can be described by Gaussian functions with a chosen standard deviation (kept constant across all channels) and a mean corresponding to the reference frequency. We then randomly sample from these Gaussians for 18 DCOs. By assuming a linear relationship between the free-running frequency-to-reference frequency difference (Δf_{lock}) and the phase offset (as indicated by Figure 5.31), we can assign a phase offset to each of the randomly sampled DCOs. We then use this phase offset to determine the sensor-voltage acquisition error for a system where all 18 sensor voltages $V_{S,1}...V_{S,18}$ are swept together over the input range of 10.8 V to 11.8 V. This process is repeated for distributions with standard deviations that increase from 0 kHz to 10 kHz;

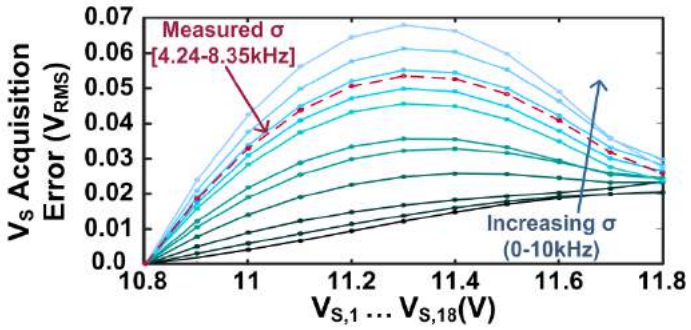


Figure 5.32: Simulated impact of TFT capacitance variation on sensor-acquisition error: each curve corresponds to a different value of free-running DCO frequency spread (ranging from 0 kHz to 10 kHz). The greater the spread, the greater the acquisition error. The transfer functions exhibit curvature, resulting from the demodulation process. This results in the shape of the error curve observed: since linear fits are performed constraining the first point in the transfer function, error is zero at $V_{S,i} = 10.8$, and error is maximal in the middle region of the plot.

Figure 5.32 shows the result. Also shown in Figure 5.32 is an acquisition error plot measured from in our demonstrated prototype ("Measured σ"), which (unlike the simulated data) has different standard deviation in each channel (hence we note the range of measured σ on the left hand side of the plot in red). We note that this measured error curve falls in the range predicted by our simulation, indicating that the DCO free-running frequency variation, not tail-TFT transconductance variation, is the dominant source of system acquisition error. Lastly, we observe that acquisition error can be notably improved beyond that of our prototype by controlling variation (e.g., reducing σ pushes the V_S acquisition error curve down in Figure 5.32); we expect this would be the case if these circuits were fabricated in industrial fabrication facilities.

5.3 System Prototype and Demonstration

To demonstrate and characterize our proposed architecture, we built a prototype large-area, force-sensing system application. The DCO array was fabricated in-house using our standard passivated ZnO TFTs. While mobility and threshold voltage variations are comparatively

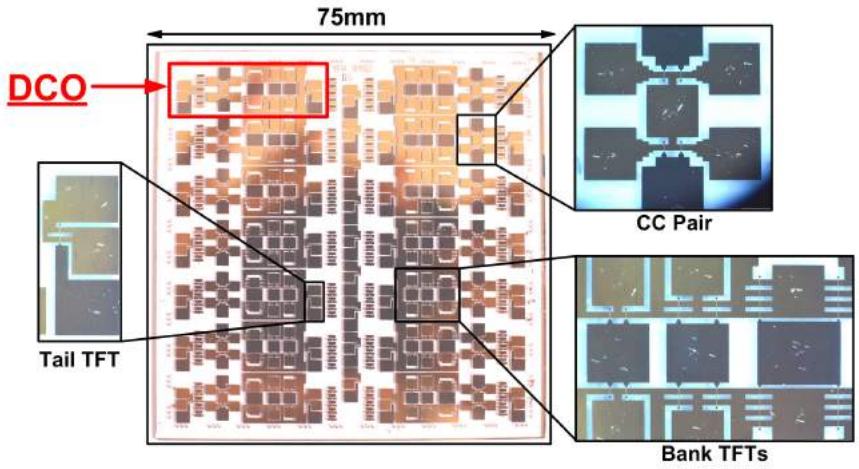
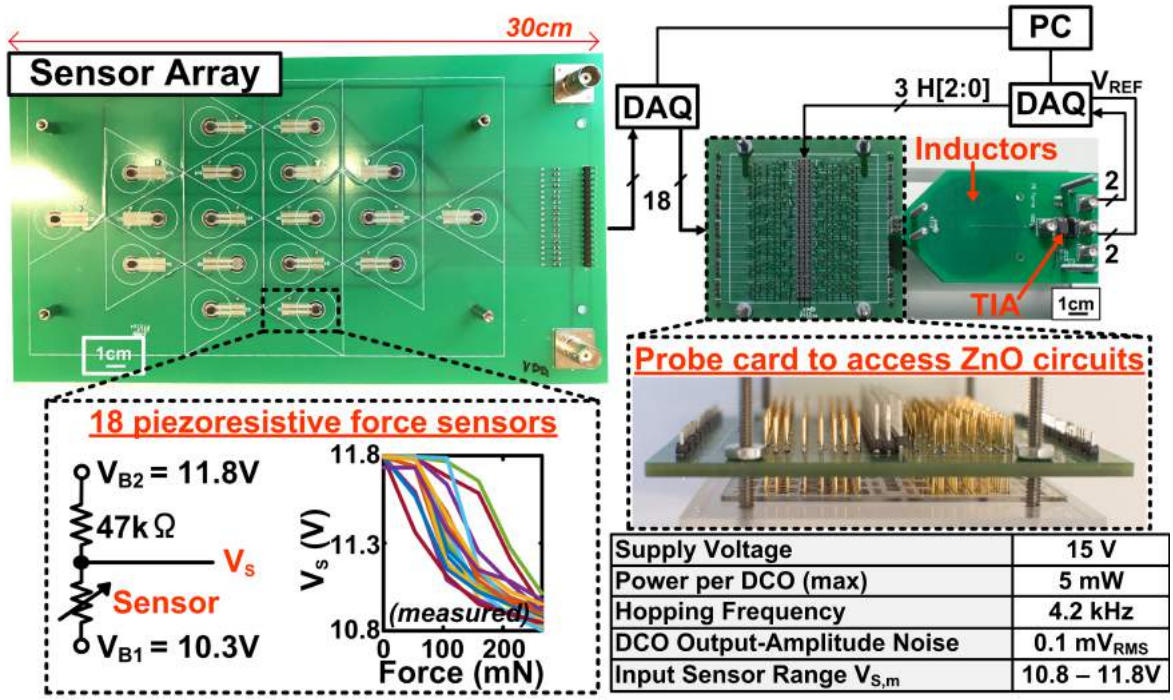


Figure 5.33: Photograph of DCO sample, highlighting DCO components.

small, capacitance variations cause errors as modeled in Section 5.2.4 and measured below. A fabricated DCO-array sample is shown in Figure 5.33; the system demonstration employs DCOs from multiple such samples as full circuit yield is ∼50%. Though we describe fabrication of oscillators on polyimide in Section 4.4.4, a glass substrate is employed for this system demonstration to simplify testing with the (sharp) PCB probe card.

The demonstrated system is shown in Figure 5.34. As discussed, the system uses a 3-bit hopping code (8 frequency channels) and 18 sensors. The sensor array consists of commercial, polymer-based piezoresistive force sensors [207], distributed across a 30-cm-long rigid PCB; sensors are connected electrically to the PCB using silkscreened silver paint. Each sensor forms one leg of a voltage divider, with the other leg being a fixed surface-mount resistor soldered to the sensor array PCB; the intermediate voltage provides the sensor voltage $V_{S,m}$, which is designed to be in the range of 10.8 – 11.8 V. This is then fed to the tail transistor of an associated DCO. The inset in Figure 5.34 shows how $V_{S,m}$ for all sensors decreases as weight is added. Significant variation in the commercial sensors is observed.

As shown in the system diagram, a data-acquisition system (DAQ) reads the sensor data, which is then provided to the DCO array for measurement. The DCO outputs are captured with a second DAQ through a single differential interface. The probe card PCB, shown



Supply Voltage	15 V
Power per DCO (max)	5 mW
Hopping Frequency	4.2 kHz
DCO Output-Amplitude Noise	0.1 mV_{RMS}
Input Sensor Range $V_{S,m}$	10.8 – 11.8V

Figure 5.34: Demonstrated system, showing sensor array (upper left), sensor voltage-divider configuration and resulting sensor signal measurements (bottom left), probe card for interfacing with TFT sample (right), as well as data-acquisition system (DAQ) for post processing and configuration. Important system-level measurements are provided in the table.

at the right, contacts the TFT sample and interconnects the TFT circuits. The PCB also contains the bank capacitors, which are implemented as surface-mount components for ease of testing. With one additional lithographic mask, the capacitors could be integrated onto the TFT sample; measurements of metal-metal capacitors with a 40-nm-thick aluminum-oxide dielectric give a capacitance density of $\sim 2\ fF/\mu m^2$. The DCO inductors are also fabricated on a PCB, and connect to the probe card via rigid header connections. We note that in an actual system realization (Figure 5.2), the DCOs would be distributed alongside the sensors, rather than separated, as done here for testability and characterization. Hence, the DCO area, dominated by the large-area inductor (50 cm^2) would likely set the sensor density.

The hopping frequency used (e.g., the inverse of the time interval between sequential hopping codes) was 4.2 kHz, set by the sample length for FIR filtering required for demod-

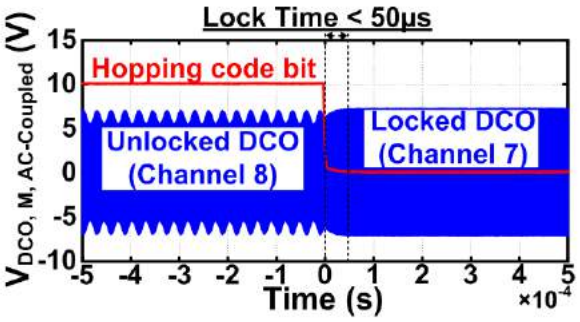


Figure 5.35: The time required for DCO to lock is $< 50\mu$s, and does not limit the acquisition speed of this system. One reference signal is applied for channel 7. At t ¡ 0, we see the output waveform from the unlocked DCO, configured to output in channel 8. It exhibits frequency pulling, visible in the waveform as amplitude variation (e.g., "beating") due to the reference signal at channel 7. At t = 0, we reconfigure the DCO to output in channel 7, and see the output amplitude stabilizing within 50 μs, indicating that the DCO has locked.

ulation. As this rate compares favorably with active matrix scan rates (shown in Figure 5.8), but the number of sensors that can be accessed is higher, cycling through the hopping codes at this rate still enables a high sensor access rate, which is our ultimate goal. The time required for injection locking to occur is less than this FIR window, and hence does not ultimately limit scan speed. Figure 5.35 shows a DCO output (in blue) changing from frequency channel 7 to 6. The reference signal is applied only for channel 6, with the reference signal for channel 7 explicitly turned off so that beating in channel 7 due to slight frequency pulling makes the locking transition time visually apparent. The left-hand side of the plot shows that before the least-significant bit (LSB) of the DCO frequency-control signal (red) is switched, the DCO does not lock to the reference for channel 6. Once the LSB switches, the DCO locks in < 50 μs.

The DCOs operate from a 15 V supply, which is sufficiently high to meet the oscillation condition for all capacitance values. At this supply voltage, each DCO consumes a maximum power of 5 mW, where the power depending on the value of the sensor signal $V_{S,m}$ and the DCO frequency. This raises an additional consideration for an eventual system (Figure 5.2). While previous work has shown TFT oscillators operating from thin-film photovoltaic (PV)

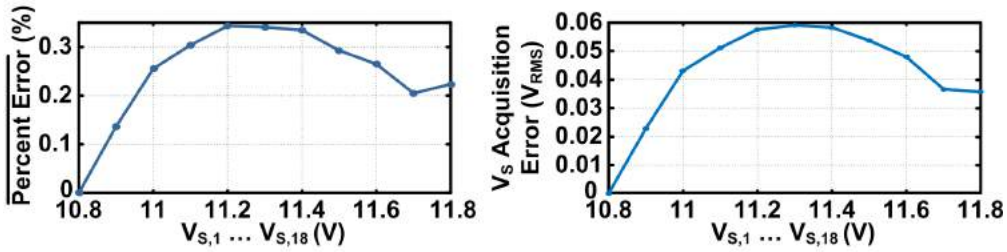


Figure 5.36: Average error as percentage of ground-referenced signal $V_{S,m}$ (left) and as absolute voltage (right) of DCO-based acquisition system as a function of sensor-voltage level.

harvesters [59], such PVs would occupy an additional area of 1-100 cm^2 per DCO (depending on lighting conditions), further reducing the sensor density. However, TFT improvements (such as work in [205] pushing the f_{MAX} of PEALD ZnO TFTs from 40 MHz to $>$ 1 GHz) offer substantial promise to reduce the power and PV area requirements.

Before reconstructing specific patterns by measuring the weight applied to the force-sensor array, we first characterize the acquisition error of the system itself over the entire sensor voltage range. To do this, all tail TFT input-voltages $V_{S,1}...V_{S,18}$ were swept for all DCOs in the array simultaneously: e.g., all tail TFT voltages, decoupled from the sensors, are set to 10.8 V, and then the voltage acquired by the system was compared to the applied 10.8 V, then all tail voltages were set to 11.0 V, etc., through 11.8 V. Figure 5.36 shows the maximum voltage acquisition error measured for each $V_{S,m}$ voltage level as 1) percent error of the ground-referenced input signal $V_{S,m}$ (left), and 2) as absolute error of the input signal $V_{S,m}$ (right). The maximum percentage error is 0.34% over the full sensor range. This percent error corresponds to a voltage error of at most 60 mV_{RMS}, which as noted in Figure 5.32, agrees well with simulation error predictions.

The sample-to-sample noise of the DCO output sinusoids is measured to be $<$ 0.1 mV_{RMS} (Figure 5.33), which is small compared to the $>$ 200 mV DCO amplitude change over the 1 V (e.g. 10.8 V – 11.8 V) sensor range. Thus, particularly after FIR filtering in the demodulation process, noise is not expected to be a prominent source of error compared to other sources (e.g., non-linearity, capacitance variations).

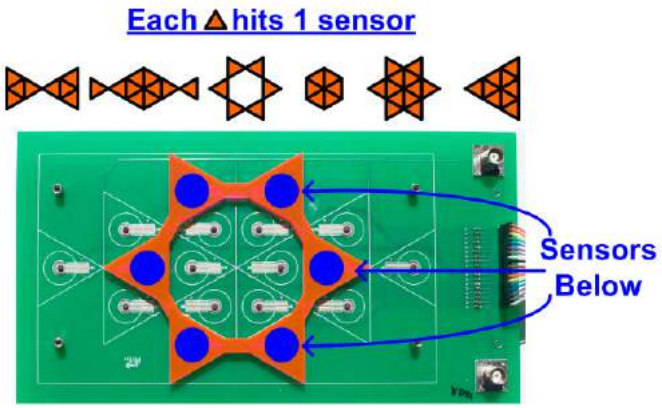


Figure 5.37: Force-sensor data obtained by placing shapes of calibrated weight on sensing plane. The test shapes are chosen such that each pattern puts a load on a different set of the 18 sensors, with up to 12 sensors depressed at once.

To generate force-sensor data, weights are cut from acrylic sheets into 6 different shapes, as illustrated in Figure 5.37. Each weight pattern is designed to contact a different set of sensors (and hence activates a different set of sensor-DCO pairs) to ensure that sensor signal reconstruction is robust across many different scenarios. The total weight of the pattern is increased in discrete steps by stacking multiple identical weights on the array; each shape applies a weight of 52 mN to each sensor it contacts. Generating calibrated weights in this way enables detailed characterization of acquisition data and error over the input range.

For each of the 6 weight patterns at each of the 5 weight levels, Figure 5.38 shows the measured results both for direct acquisition of the 18 sensor voltages through 18 interfaces (e.g. "Raw Sensor"), and for reconstruction of the sensor voltages via the system through the single differential connection from all the DCOs in LAE to the CMOS TIA (e.g., "System Output"). The data is displayed in heat-map form, where each triangle in each image corresponds to one sensor in the array, and the color of the triangle corresponds to the measured or reconstructed sensor signal voltage level. The "ideal" weight patterns are shown at the top of the figure, where black triangles demarcate the acrylic weight shape, and the white triangles indicate empty space where there is no weight. Hence, as the weight increases as more and more shapes are stacked on top of the sensor array, the patterns appear darker

and darker (corresponding to lower and lower voltage levels). When one sheet of acrylic is placed on the array, the weight pattern is scarcely visible, both for the raw sensor voltage data and for the sensor data acquired by the system. We note that there is variation in the gray level of the sensor voltages, even when acquired directly from the sensors, which causes acquired data to differ in appearance from the "ideal" shapes in the top row – this is because of the sensor variation, shown before in Figure 5.34. However, significantly, the voltage error between the raw sensor measurement and the reconstructed system output is quite small – at most 37 mV_{RMS} – e.g., the system reconstruction faithfully reproduces the observed sensor variation. As we add one more acrylic sheet on top of the array, increasing the weight on the sensors, the pattern becomes visible to the eye in both raw sensor and system output cases. Again, the error is low – at most 62 mV_{RMS}, corresponding to a ground-referenced percentage error of just 0.31%. Increasing the number of acrylic sheets on top of the array to 3, 4, and 5 yields similarly low error for all shapes.

5.4 Section Conclusion

In hybrid systems that combine LAE, for large-scale, distributed sensing, with silicon CMOS, for sensor-data processing, the interfaces required between the technologies present a dominant limitation to system scalability. In this chapter, we demonstrate a system that addresses this challenge, leveraging the inherent qualities of thin-film ZnO (improved mobility compared with amorphous silicon predecessors) along with TFT and circuit strategies (TFTs with low R_{gate} for high-f_{MAX} and a resonant LC oscillator topology) to enable a highly-scalable frequency-hopping architecture.

Our demonstrated system is based on amplitude-modulated, frequency-hopping PEALD ZnO TFT DCOs. The system architecture is designed to reduce the number of CMOS–LAE interconnections, while maintaining a rate of sensor access beyond what can be achieved with existing active-matrix and binary-addressing schemes. The primary tradeoff is increased

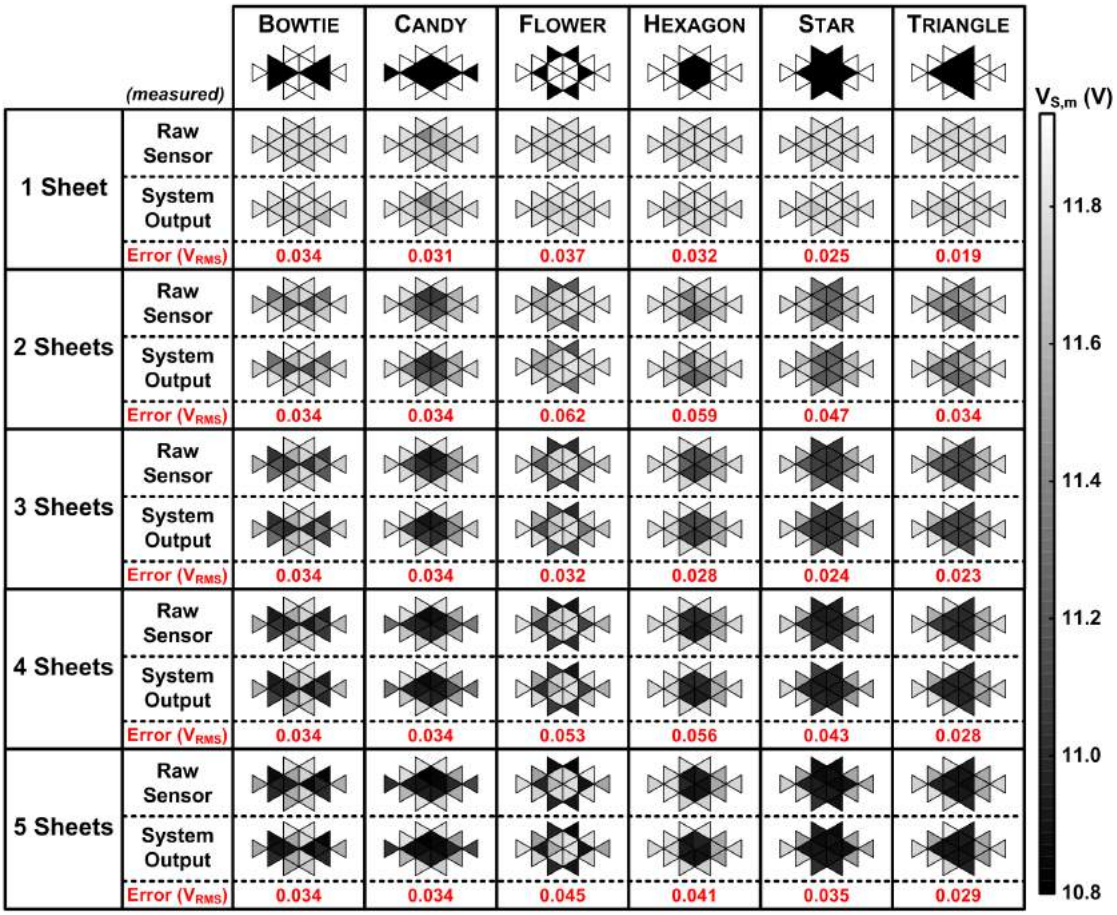


Figure 5.38: Results comparing sensor voltages acquired through the demonstrated system and those acquired directly from measuring each sensor output ("Raw Sensor") for 6 shapes and 5 weight levels. Voltage error between the voltage acquired by the raw sensors and the voltage reconstructed by the system output is shown in red beneath each shape/weight combination. Measurements are displayed in heat-map form, where darker triangles indicated more weight. Measurements are acquired for 5 different weight levels by stacking 1 to 5 sheets of shaped acrylic on the sensing array; hence more contrast is visible as the number of sheets is increased.

dynamic-range required for signal processing. However, this affects only the CMOS domain, where circuits can have much higher energy efficiency and performance thanks to the available transistors. For demonstration and characterization, an 18-element force-sensing system is prototyped, employing ZnO TFT DCOs. The system performs frequency hopping over the 18-DCO array at a rate of 4.2 kHz and achieves a maximum acquisition percentage error of just 0.31% over 30 weight patterns.

Chapter 6

Conclusions, Acknowledgements, and Future Work

6.1 Summary

In this thesis, we have covered a broad span of topics all unified by the theme of large-area electronics. Large-area electronics provides a unique opportunity to realize powerful sensing systems at a massive scale – the diversity of sensors it affords, coupled with the variety of large scale, compliant substrates, are enough to fill the pages of many a science fiction novel. In our approach, we aim to make these fantasies more concrete, using a bottom-up approach motivated by the practical constraints of system integration.

Approaches to LAE systems generally focus on building faster TFTs and more sophisticated sensors. This is very important work, but in order to result in rapid industry adoption of LAE for sensing, it is not sufficient to design TFTs and sensors in isolation: in our work, we find that it is most effective to develop these important components in the LAE system with full knowledge of systems architecture, as system-level needs may differ from device-level priorities

Our approach to LAE has been to build hybrid LAE-CMOS systems that divide system functionality based on the largely complementary strengths of the two technologies. This strategy has been effective, but faces a critical bottleneck in the interconnections between the two technologies. We would like to expand the sensing domain to very large numbers of sensors, but cannot do so without having a fundamentally scalable means of connecting these sensors back to CMOS for higher level signal processing.

Motivated by this high-level challenge, we turn again to TFTs with new priorities, hoping to identify a TFT suitable for incorporation into LAE-CMOS interfacing circuits.

In Chapter 1, we outlined our requirements for TFTs in hybrid systems: we need high-performance TFTs, but they must also be robust, uniform over vast areas, compatible with mass production, and compatible with low-temperature processing. These criteria brought our attention to metal oxide TFTs, because of their high performance relative to amorphous silicon and organic materials and their superior uniformity compared with polysilicon. PEALD ZnO in particular was chosen for its fundamentally high conformality and spatial uniformity.

From this point, the path became clear. First, build a PEALD system that has enough tuning parameters to optimize growth conditions, but is also designed with material reproducibility in mind. Second, build TFTs from the resulting materials on glass and plastic, understand their behavior under a host of conditions, and optimize TFTs not only for f_T, but also for parameters most relevant to the circuits you want to build. Third, explore ZnO TFT circuits that can benefit most from its material properties: enhanced mobility and conformality. Lastly, leverage the advantages provided by ZnO circuits to return to our large goal: robust, scalable hybrid systems.

In Chapter 2, we described the motivation for all aspects of the design of our plasma-enhanced ALD system, including the deposition chamber with its low-density capacitive plasma, the gas delivery system with its many failsafes and bubbler-based design, pressure

control and safe release of exhaust, and computer control, for recipe consistency and automation.

In Chapter 3, we developed recipes for ZnO and Al_2O_3 films that were high-density and formed with low plasma density and high oxidant pressure. We developed reliable etching recipes for these materials, including a selective etch for Al_2O_3 that does not attack the easily-etched ZnO. From here, TFT recipes were developed, including the first recipe for in-situ passivated, self-aligned ZnO TFTs, and TFT instabilities were examined, and TFTs on multiple kinds of plastic substrates were evaluated under tensile and compressive strain; ZnO TFTs were bent across radii as small at 500 μm without deterioration for the first time.

In Chapter 4, we characterize ZnO TFTs in terms of parameters most relevant to circuit development, and emphasize the importance of gate resistance as an easily modified, often-neglected parameter for optimizing TFTs for resonant circuits. We then use circuit-optimized TFTs to build two kinds of circuits aimed at system-level interconnection reduction: scan circuits and *LC* oscillators. The ZnO circuits demonstrated exhibit significant advantages in speed and/or power over amorphous silicon predecessors. These circuits include the fastest circuits built at low temperature ($< 200°C$).

In Chapter 5, we exploit the speed, conformality, and uniformity of our ZnO TFTs to develop a new hybrid system architecture that results in explosive system scalability. The architecture was prototyped into a functional force-sensing system that reconstruct sensor data from 18 distributed sensors with extremely high fidelity, all through a single differential CMOS–LAE interconnection.

This thesis has described a long and winding journey, but a rewarding one that provided ample opportunities to both understand challenges and contribute insight at every step of LAE system building, from machine development, to material and TFT assessment, to circuit design, to system architecture and integration.

6.2 Acknowledgements

I am grateful to have been part of a research group with such diverse talents. Because our work is fundamentally interdisciplinary, many projects only come to fruition because of intense collaboration and efforts from many students. As described, the PEALD system was built in collaboration with (now Prof.) Sushobhan Avasthi and (now Dr.) Bhadri Visweswaran. Measurements of TFTs on free-standing plastic were performed in collaboration with undergraduate Jenny Tang. The force-sensing system was built in close collaboration with Tiffany Moy, with additional support from undergraduate Nick Brady. I am also very grateful for less obvious mentorship and support from all group members, past and present, including the above but also Drs. Warren Rieutort-Louis, Josh Sanz-Robinson, Liechao Huang, Yingzhe Hu, and Ting Liu, and not-yet Drs. Levent Aygun, Yoni Mehlman, Can Wu, Hongyang Jia, and Lung-Yen Chen.

Lastly, none of this work would have been possible without generous support from the NSF Graduate Research Fellowship Program, the Princeton Program on Plasma Science and Technology Fellowship (DE-AC02-09CH11466), National Science Foundation Grant ECCS-1202168 and Grant CCF-1218206, Universal Display, Flextech Alliance, and MARCO and DARPA through the Systems on Nanoscale Information fabriCs (SONIC) project, one of the six SRC STARnet Centers. Thank you also to the Andlinger Center for Energy and the Environment, which provided the funds to build the PEALD system.

6.3 Future Work

There is ample room for continued work in each area touched upon in this thesis. Here are a few ideas.

6.3.1 PEALD Improvements

While the PEALD has been a trusty ally, faithfully pumping out film after film for nearly five years, there are several ways it could be improved. Some suggestions include:

- Placing an easily-removable diffuser in front of the gas inlet (or a small ridge before the first sample edge) to prevent precursor from depositing multilayers on the sample edge.
- Increasing the size of the chamber such that the top electrode could be much larger than the substrates used would increase sample uniformity at the outer edges. As a rule of thumb, the diameter of electrode should equal the diameter of the substrate plus two times (at least) the electrode-substrate spacing.
- Place a filter within a recirculating "shunt" line connected to the pump to ensure that any precursor that reacts inside the pump is removed from circulation.
- Place a backstream oil filter inside the exhaust line, between the throttle valve and the pump, to reduce the possibility of pump oil diffusing into the chamber if the gate valve is left open accidentally and no gas is flowing.
- Replacing the DC power supply with a simpler power source with no current limit so the arc discharge can remain continuously, rather than intermittently, on.

6.3.2 Material and TFT Improvements

- It is clear that reducing plasma power during oxide deposition has a huge impact on TFT performance. Currently, a plasma cannot be struck if the RF power is reduced below 15 W. By incorporating a DC power supply without a current limit (as I suggest in the last section), I think it we could overcome this limitation and reap TFT benefits.
- While the NaOH etch is highly selective, it could impart mobile sodium ions to the ZnO film. It would be worthwhile to perform heated I-V and/or C-V measurements

(as done long ago in Si transistors) to encourage Na diffusion and watch for changes in threshold and flatband voltage (using a sensitive ammeter and applying a constant dV/dt voltage ramp), and if these occur, to seek out a new etchant.

- I found the low photocurrent levels in ZnO TFTs (relative to IGZO) to be promising, and if subjected to more aggressive investigation, this could provide a strong argument for the superiority of ZnO over IGZO. I-V experiments using a calibrated single-wavelength light source while biasing TFTs in forward and reverse conditions would be very illuminating.

- Self-heating of TFTs is shown to be a significant limitation. Because TFTs are generally deposited on thermally insulating substrates, it would of use to characterize and compare self-heating effects for ZnO TFTs on glass and different plastic substrates of different thicknesses to identify the material most capable of dissipating generated heat. Furthermore, as pulsed measurements are seen to greatly reduce self-heating, it would be very interesting to design ZnO TFT circuits that take advantage of pulsed biasing – this would likely increase device lifetime and furthermore would increase power efficiency, at the expense of more complex biasing waveforms, that could be generated without much difficulty in the CMOS domain.

- Because single-crystal ZnO is piezoelectric, current-voltage sweeps of ZnO TFTs on flexible substrates should be performed *while strain is continuously applied*. We have evaluated this for large bending radii, in the flexible oscillator section, and find no change from the TFTs on the circuit level. However, it would be interesting to identify if effects emerged at higher strain levels.

- TFTs on spin-cast PI have superior properties compared with TFTs on free-standing polyimide. We suspect this is a result of the improved surface roughness of spin-cast PI substrates (which are spun on extremely smooth Si carriers). It would be interesting

to investigate this point further; if this is the case, perhaps TFTs on free-standing PI could be improved by incorporating a planarization layer.

- Nitrogen is known to act as an acceptor in ZnO, and can hence reduce electron concentration in ZnO films [208]. It is plausible then that nitrogen or N_2O plasma treatment after ZnO deposition (prior to encapsulation) could help further reduce ZnO conductivity and enhance subthreshhold slope.

- TFTs on spin-cast polyimide are very promising, but not readily compatible with a self-aligned process. Perhaps we could instead spin polyimide onto clear glass substrates (which should survive the 350°C cure temperature), so that we can again take advantage of transparency to perform self alignment.

- There have been great advancements in the realm of ultra-thin, ultra-strong glass in recent years. It would be interesting to build TFTs on thin, flexible glass – perhaps at higher temperature – to see how far we can push ZnO TFTs in temperature while still maintaining compatibility with a flexible substrate. 200°C is a temperature limit that makes a larger number of substrates available, but perhaps this is not a primary concern in many applications.

6.3.3 Circuit Improvements

- Self-alignment and channel downsizing are straightforward, if less easily realized, ways to improve TFT oscillator performance, so long as gate resistance can be reduced (using for example a multi-fingered gate).

- In LC oscillators, as frequency increases (e.g., as we reduce the size of the oscillator) the tank Q will degrade. It would be beneficial from a scaling perspective to quantify this degradation.

- We believe that PEALD materials have a very low occurrence of pinhole-related defects compared to PECVD films. Because $1/f$ noise of TFTs can be reduced by increasing TFT area (which is limited in amorphous silicon TFTs, which are deposited by PECVD) it would be valuable to define the extent to which we can increase the dielectric area before compromising yield of the gate dielectric. This optimization would require variation of dielectric thickness and area.

6.3.4 Future Systems

- Our ZnO TFTs show increased current as a function of temperature; this may be in part due to a higher level of carriers available, but could also stem from the fact that ZnO is a pyroelectric material. Depending on the reproducibility and sensitivity of this effect, we could use this fact to embed temperature sensors into our TFT circuits for biological sensing applications.

- Metal oxides have been used historically as gas sensors, which is why our TFTs require passivation for stable operation. Perhaps we could exploit this sensitivity to create a LAE gas sensing system using ZnO sensors.

- Because our oxide layer are thin, they are readily fabricated on ultra-thin substrates, as discussed. The natural motivation for such thin substrates is for biomedical application, where patient comfort (for applications external to the body) or successful implantation may be priorities. Two undergraduates that I have mentored worked extensively to develop robust electrodes patterned on perforated, ultra-thin polyimide sheets. Because the sheets are so thin and have perforations that allow fluids to pass through, the hope was to use implant them in Duragen, a collagen matrix developed by a local company that helps regenerate tissue in the brain. As we already have a process for ZnO TFT fabrication on ultra-thin plastic, it would be interesting to build

large, (and hence hopefully very-low noise) TFTs to amplify biological signals directly on these perforated sheets for more sophisticated sensing.

There is essentially no end to the work that remains. It is hence with a bittersweet feeling that I conclude this thesis, knowing I will not have the opportunity to pursue any of these musings myself!

Appendix A

PEALD Dimensioned Drawings and Code

A.1 Chamber Drawings

In this section you can find:

- Fully-dimensioned CAD drawings of the PEALD chamber body from A&N corporation: Figures A.1, A.2, A.3, A.4, A.5, A.6.
- Fully-dimensioned CAD drawings of the PEALD chamber lid from A&N corporation: Figures A.7, A.8, A.9.

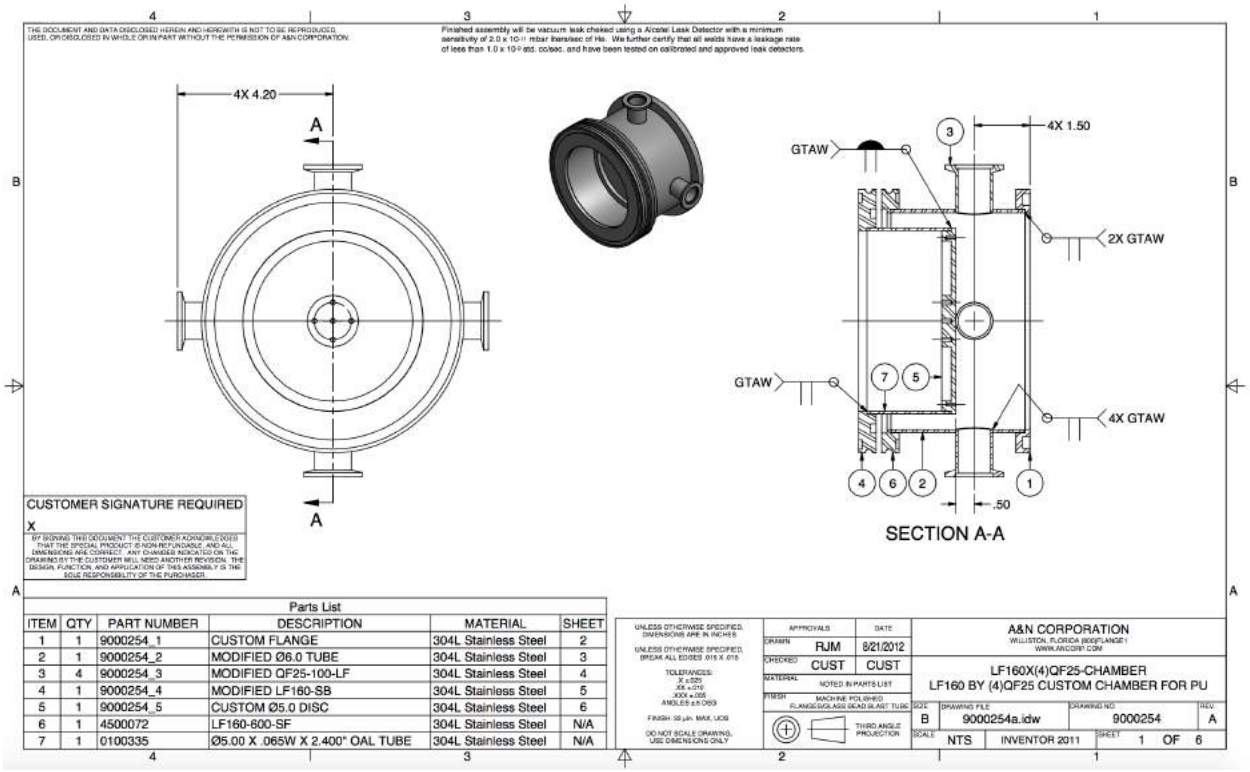


Figure A.1: Dimensioned drawings of chamber body (1 of 6).

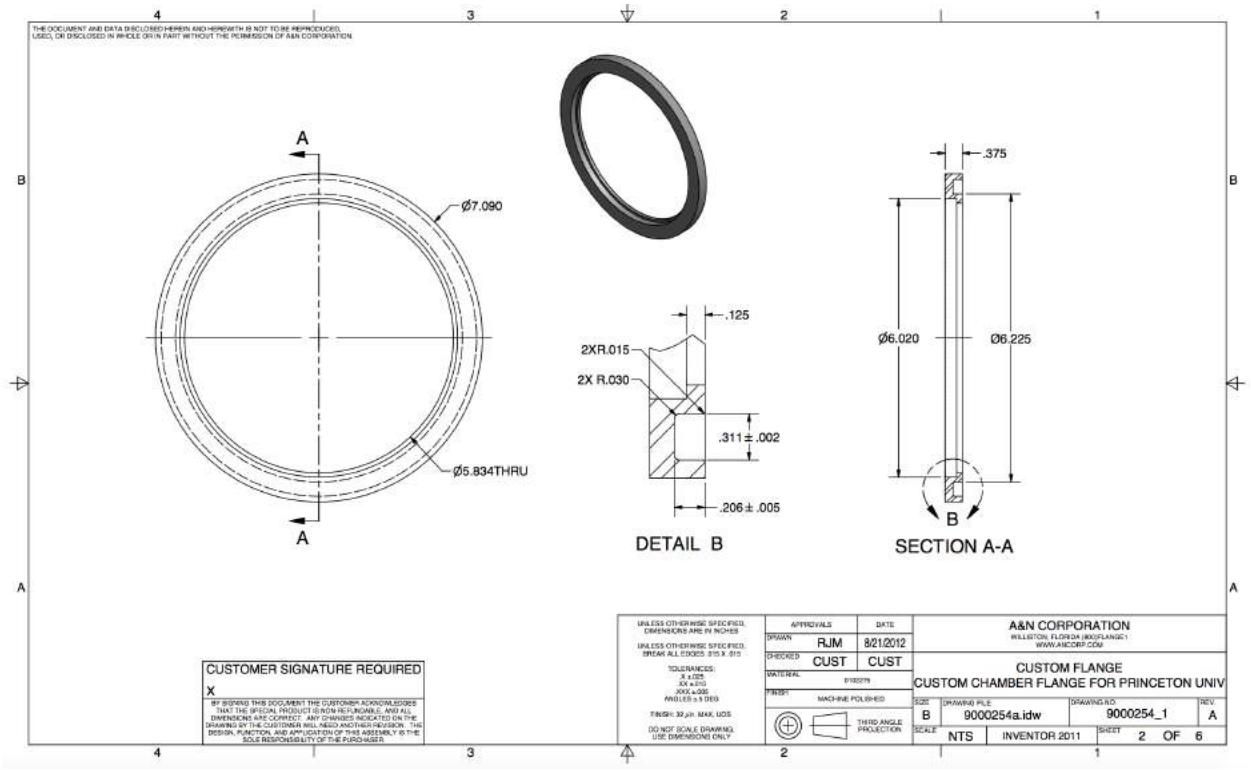


Figure A.2: Dimensioned drawings of chamber body (2 of 6).

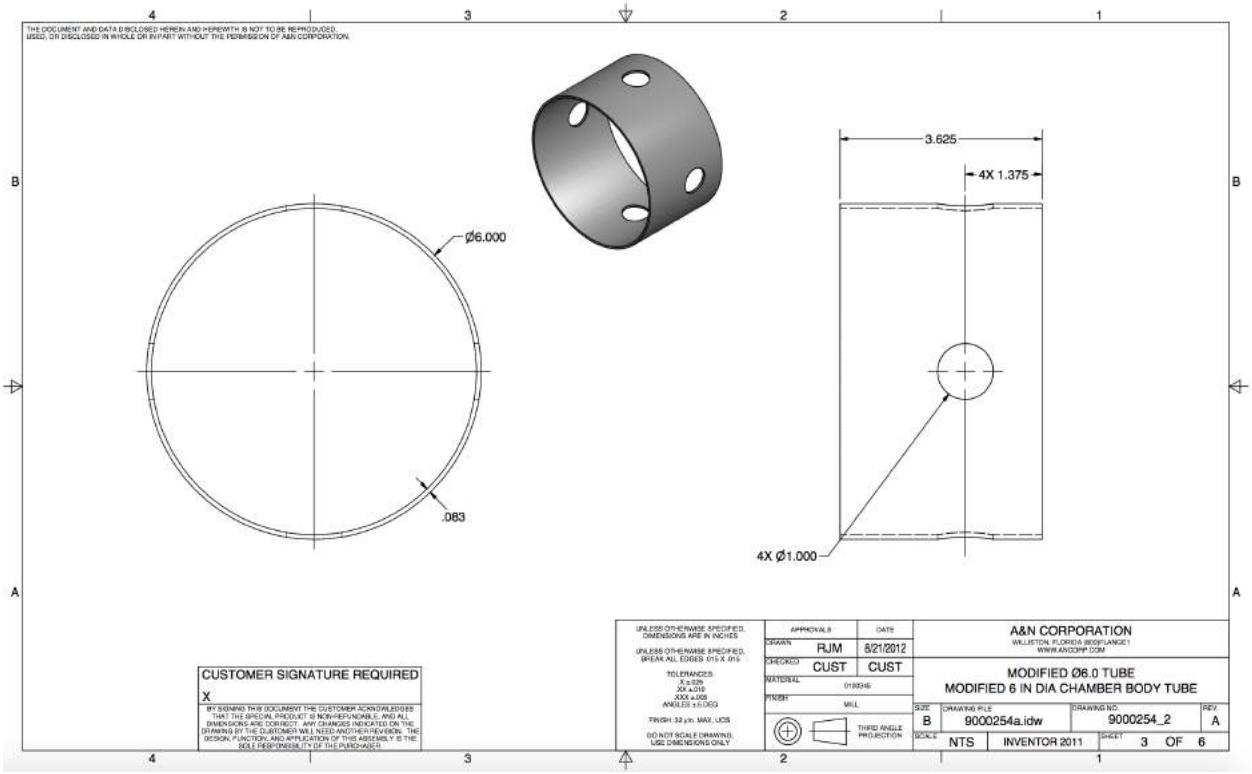


Figure A.3: Dimensioned drawings of chamber body (3 of 6).

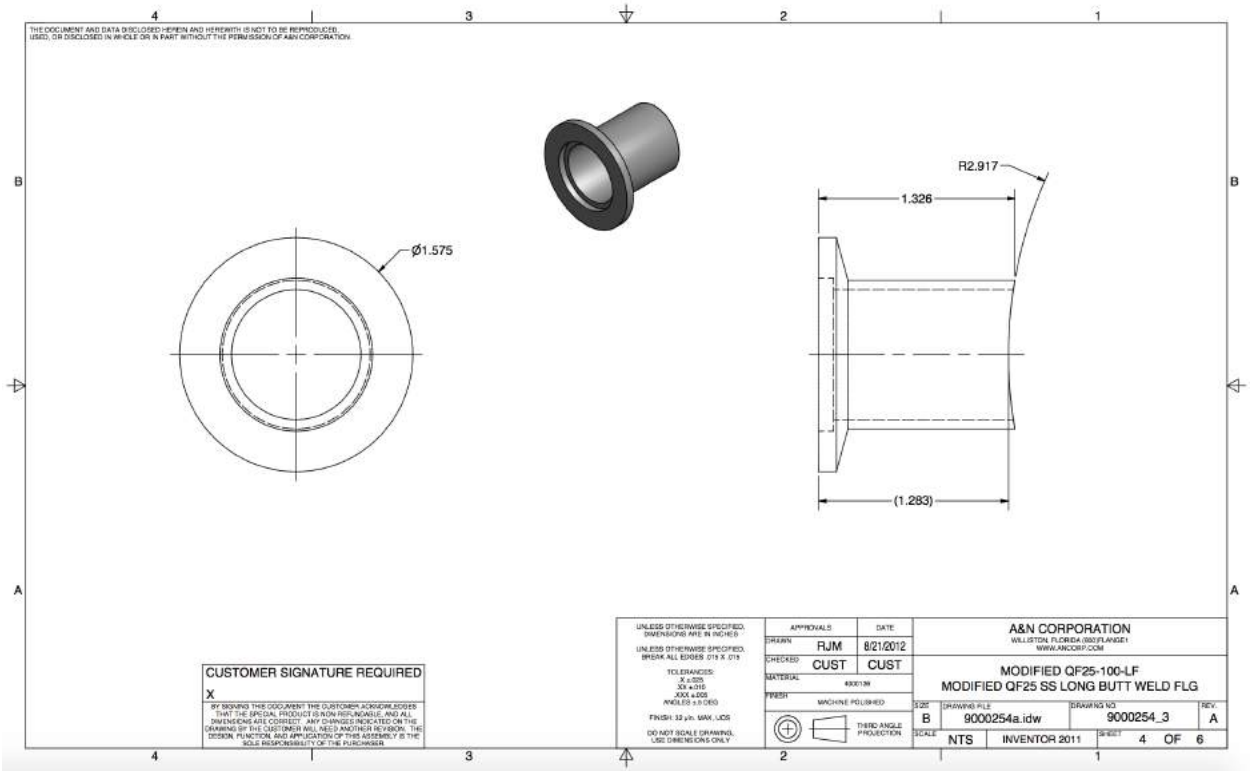


Figure A.4: Dimensioned drawings of chamber body (4 of 6).

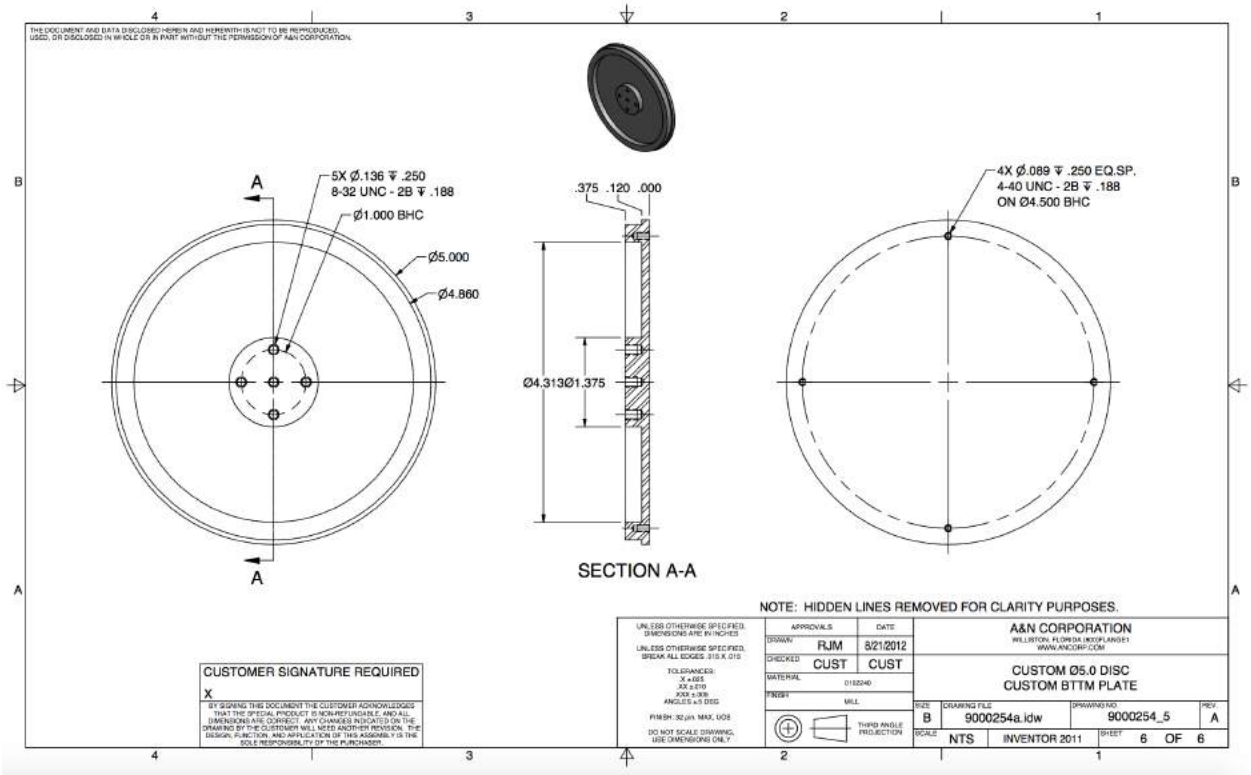


Figure A.5: Dimensioned drawings of chamber body (5 of 6).

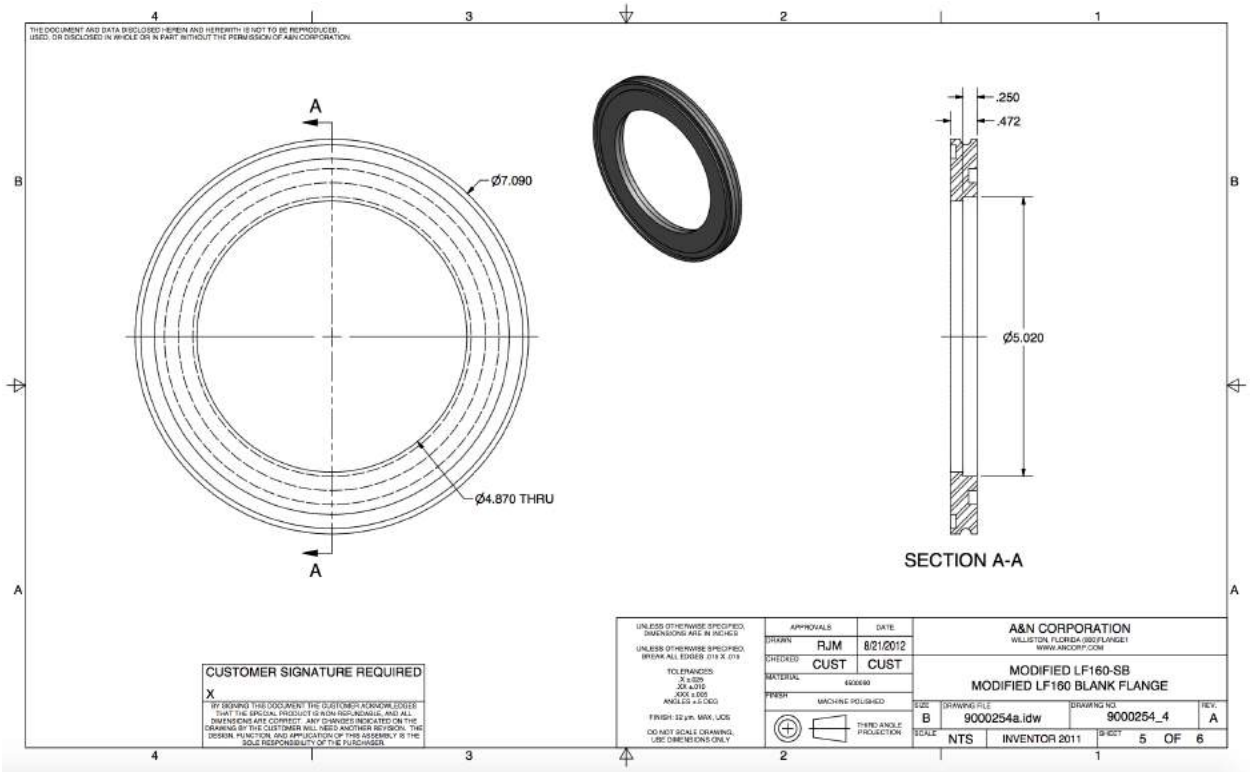


Figure A.6: Dimensioned drawings of chamber body (6 of 6).

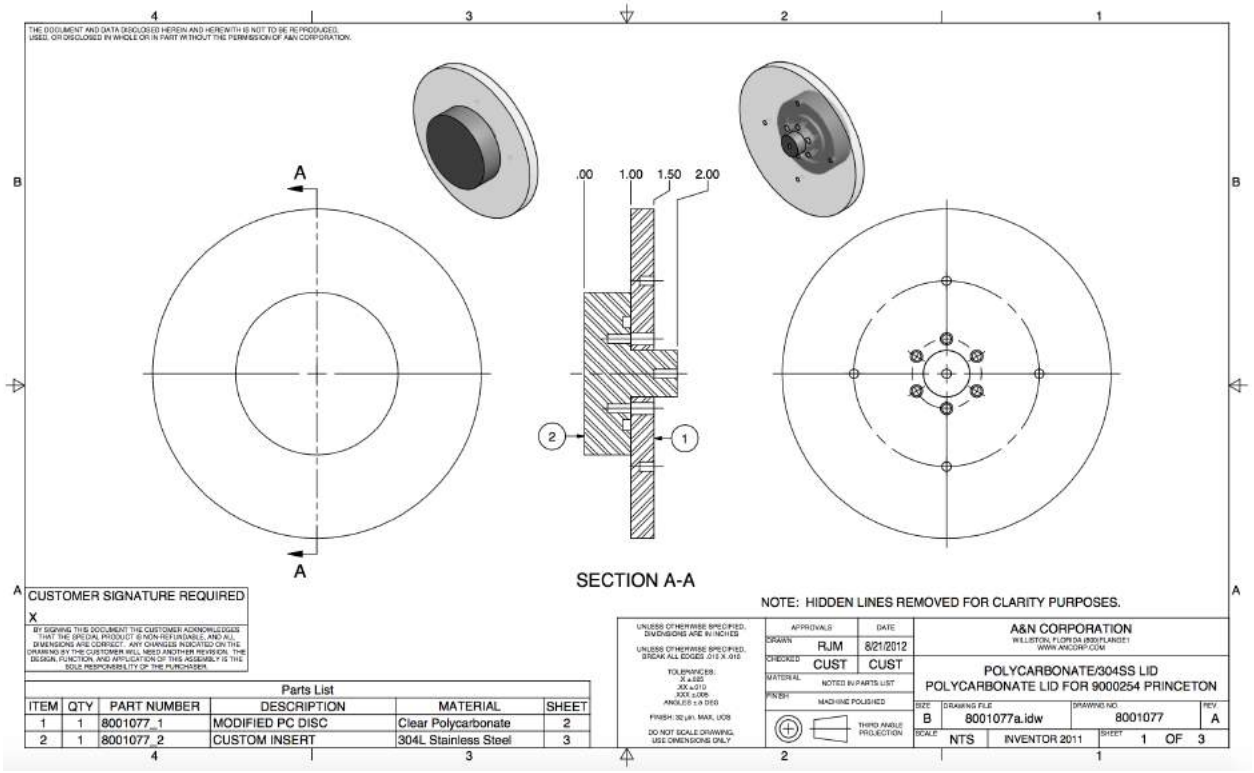


Figure A.7: Dimensioned drawings of chamber lid (1 of 3).

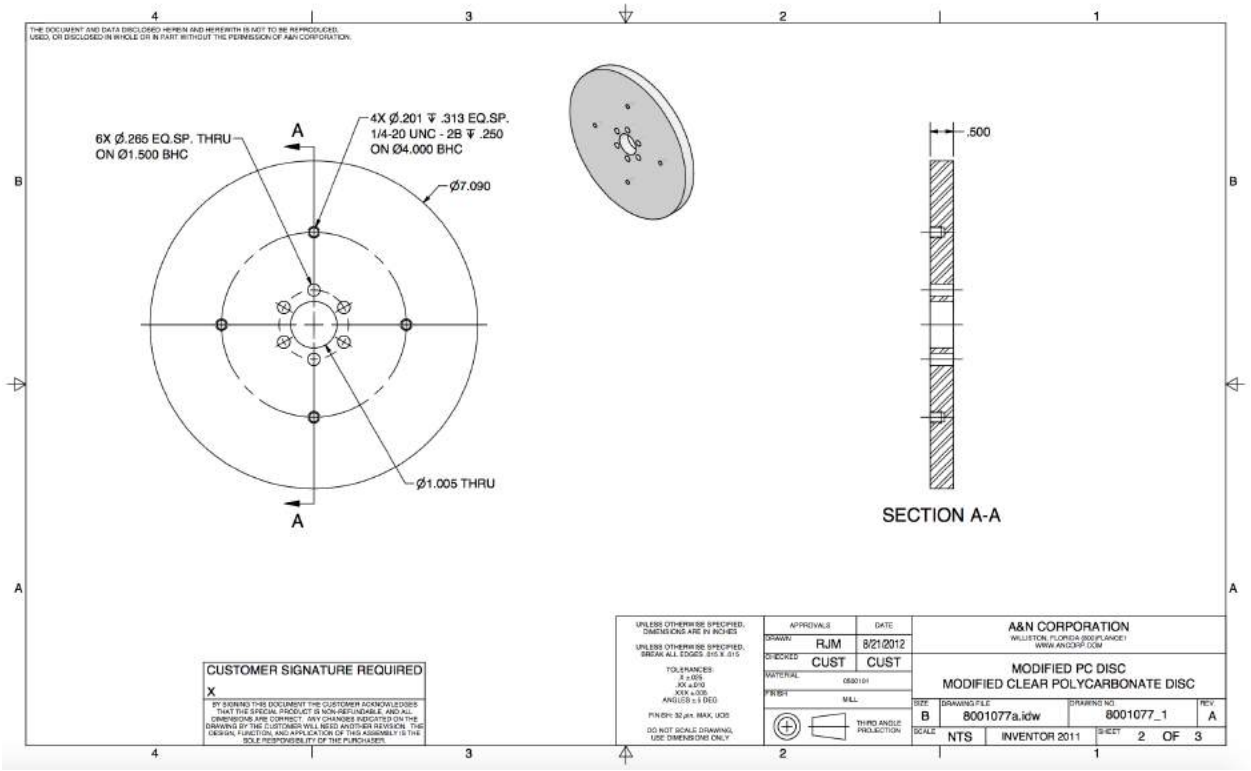


Figure A.8: Dimensioned drawings of chamber lid (2 of 3).

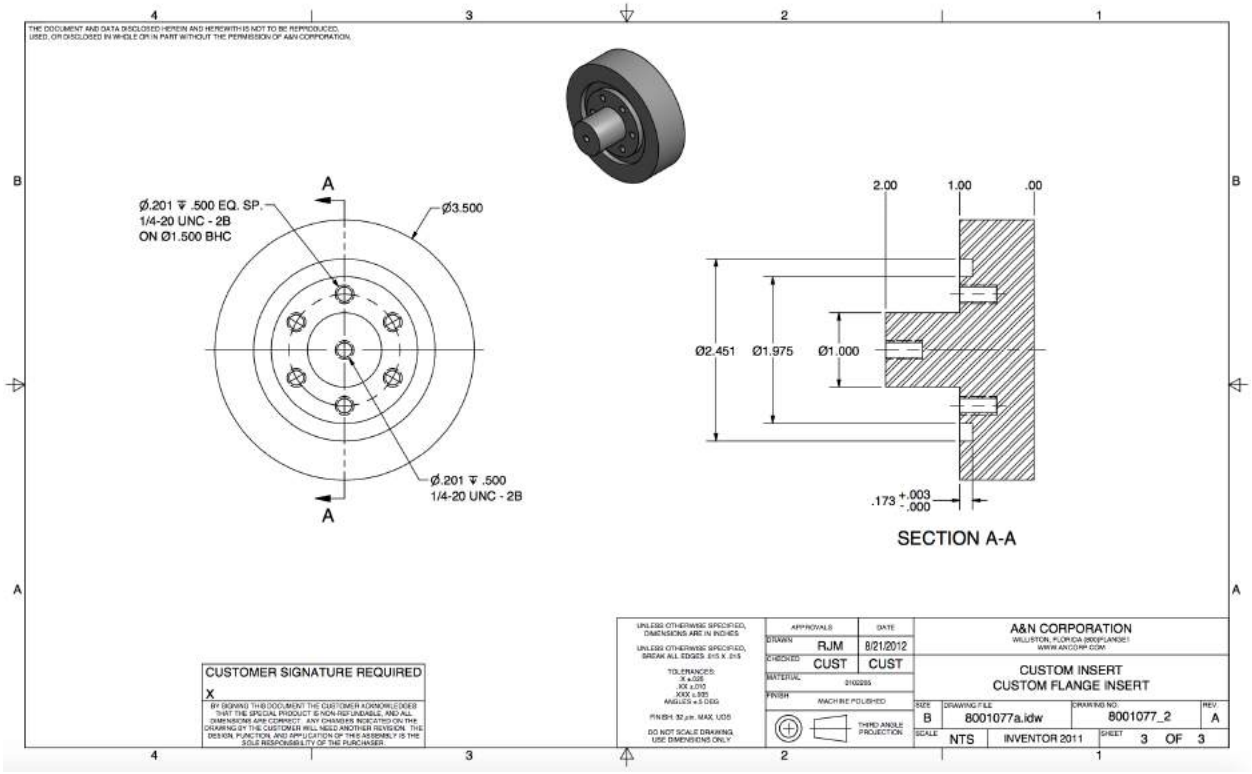


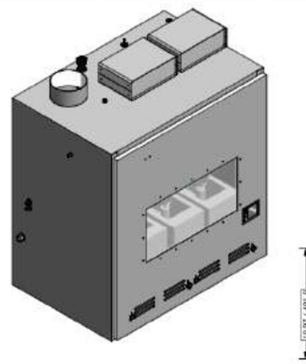
Figure A.9: Dimensioned drawings of chamber lid (3 of 3).

A.2 Gas Manifold Drawings

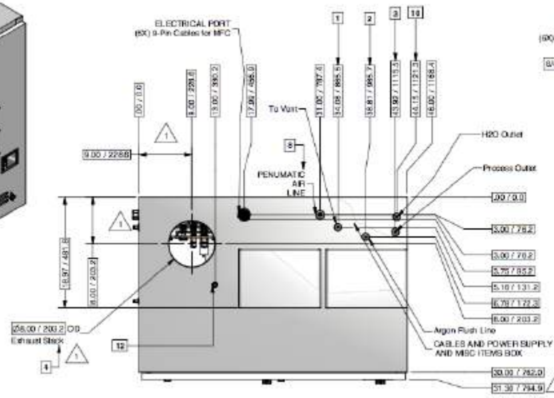
In this section you can find:

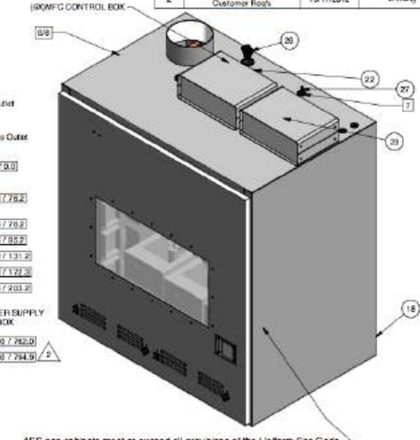
- Fully-dimensioned CAD drawings of the PEALD gas cabinet from Applied Energy (Malvern, PA): Figures A.10, A.11, A.12, A.13
- Fully-dimensioned CAD drawings of the individual gas panels for TMA, DEZ, and H_2O delivery from Applied Energy (Malvern, PA): Figures A.14, A.15, A.16, A.17, A.18, A.19
- A CAD drawing of the house nitrogen delivery line for chamber venting from Applied Energy: Figure A.20.

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
0	RELEASED FOR CUSTOMER REVIEW	9/25/12	L.WANG
1	Changed window, stack and slots size per customer request. Changed cabinet color to Light grey	10/8/2012	L.Wang
2	Updated Design Per Customer Roofs	10/17/2012	L.Wang

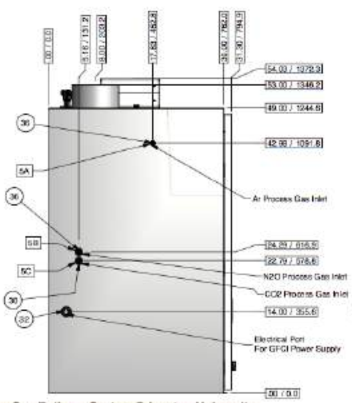


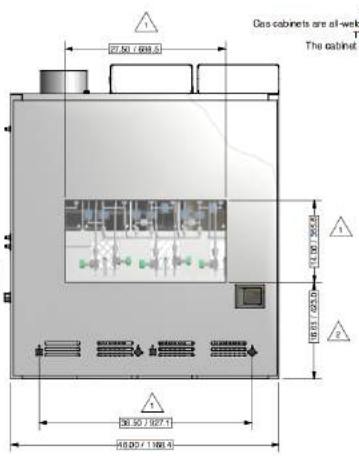
Door Closed Enclosure





AES gas cabinets meet or exceed all provisions of the Uniform Fire Code.
The outside dimensions of the **CABINET IS** 46" wide x 49" high x 30" deep.
There will be a 6" exhaust duct that extends 4 inches from the top of the gas cabinet.
Gas cabinets are all-welded, 11 gauge, cold rolled (CRS) steel, with powder coated paint. **Color - Light Grey**
The door is self-closing. Gaskets are provided on door and window to control airflow.
The cabinet is provided with wire window, automatic door closure and adjustable air inlet louvers.
A sprinkler head is mounted in the gas cabinet for connection to a water supply.





Custom Gas Delivery System Princeton University
CUSTOMER: PRINCETON UNIVERSITY
SALES ORDER: AES35182
PO: 0000487296
QTY: One

Legend:

1) Vent Outlet
Connection: 1/4" Male Face Seal within Enclosure

2) Ar Flush Lines Outlet
Connection: 1/4" Male Face Seal within Enclosure

3) Process Gas Outlet
Connection: 1/4" Male Face Seal within Enclosure

4) Enclosure Exhaust
Connection: 6.00" OD x 4" Tall Stack

5) Process Gas Inlet (6X)
Gas: Argon (A)
Connection: 1/4" Female Face Seal within Enclosure (Piping from Ar Cylinder to inside of CAB. To Be Provided by Customer)
Flowrate: 200 sccm Max
Inlet Pressure: 30/5 psig Max/Min
Outlet Pressure: 0 to 0.5 atmosphere

Gas: N2O (B)
Connection: 1/4" Female Face Seal within Enclosure (Piping from N2O Cylinder to inside of CAB, To Be Provided by Customer)
Flowrate: 200 sccm Max
Inlet Pressure: 30/5 psig Max/Min
Outlet Pressure: 0 to 0.5 atmosphere

Gas: CO2 (C)
Connection: 1/4" Female Face Seal within Enclosure
(Piping from CO2 Cylinder to inside of CAB. To Be Provided by Customer)
Flowrate: 200 sccm Max
Inlet Pressure: 30/5 psig Max/Min
Outlet Pressure: 0 to 0.5 atmosphere

Gas: TMA (D)
Connection: 1/4" Male Face Seal within Enclosure (From TMA Cylinder)
Flowrate: 200 sccm Max
Inlet Pressure: 30/5 psig Max/Min
Outlet Pressure: 0 to 0.5 atmosphere

Gas: DEZ (E)
Connection: 1/4" Male Face Seal within Enclosure (From DEZ Cylinder)
Flowrate: 200 sccm Max
Inlet Pressure: 30/5 psig Max/Min
Outlet Pressure: 0 to 0.5 atmosphere

Gas: H2O (F)
Connection: 1/4" Male Face Seal within Enclosure (From H2O Cylinder)
Flowrate: 200 sccm Max
Inlet Pressure: 30/5 psig Max/Min
Outlet Pressure: 0 to 0.5 atmosphere

6) MFC Control Box

7) Power Supply and misc Items Box

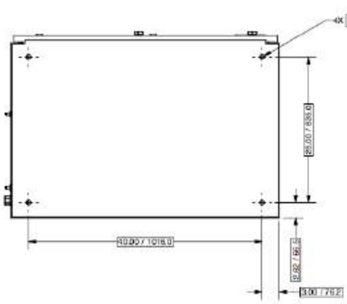
8) Pneumatic Gas Supply
Connection: 1/4" OD x 1/8" ID Polytubing Hose Barb Fitting
Gas: Nitrogen or CDA Filtered to <10 Micron
Pressure: 85-95 psig (6.0 - 6.7 kg/cm2)

9) Cabinet Mounting
This is a recommendation based on typical ratings. Consult your local authorities and codes to determine conformance with your seismic rating. The enclosures are not suitable for exterior installations.

10) H2O Process Gas Outlet
Connection: 1/4" Female Face Seal within Enclosure

11) Leak Test Port
Connection: 1/4" Female Face Seal within Enclosure

12) Spinkler
Connection: 1/2" Male NPT at Roof
Static (Non-Flowing) Pressure: 175 psig Max
Dynamic (Flowing) Pressure: 7 psig Max
Water Usage: 7 to 36 GPM (Depending Upon Supply Pressure)



NOTES:

1) Refer to Drawing PRIN-080412-001 through PRIN-080412-005.

2) Six gas panels are included and mounted as depicted on the sketch
An electrical conduit is provided to supply the three bubblers
All components will be front mounted on standoffs for
easy removal, and maintenance

3) MFC cabinets are included and will run to a bulkhead fitting in the gas cabinet. MFC cables to Princeton's computer are not included but can be added once the configuration is defined. There may be a price associated with this.

4) Kel-F seat material on the valves fro DEZ Gas Panel

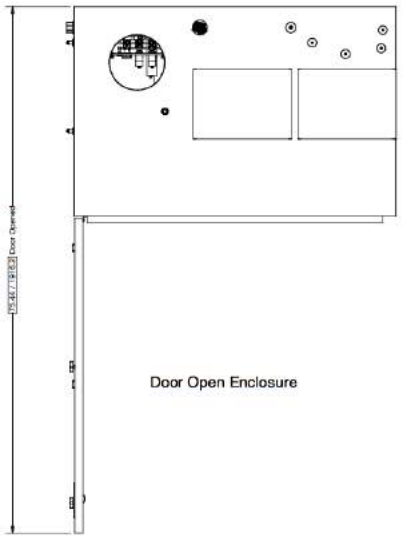
5) Bubbler Pigtails Size: 1/4 "OD Tubing

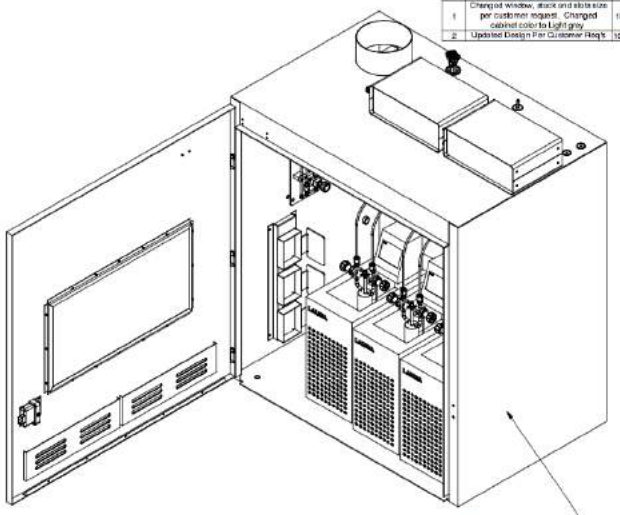
PARTS LIST			
ITEM	QTY	PART NUMBER	DESCRIPTION
1	3	Bath	PROVIDED BY CUSTOMER
2	2	2012100-20	Mfld, N2O,CO2 Custom Gas Delivery System
3	1	2012100-30	Mfld, H2O,Custom Gas Delivery System
4	1	2012100-10	Mfld, TMA Custom Gas Delivery System
5	1	2012100-40	Mfld, DEZ,With FFKM (Kalrez) Check Valve, Custom Gas Delivery System
6	1	2012100-50	Mfld, Ar Custom Gas Delivery System
8	1	2012100-60	Vlv Mod,Ar Header,Custom Gas Delivery System, Princeton Univ
9	5	0208-0002	Gasket, 1/4" VCR, Nickel, Unplated, Swagelok
10	1	2012100-70	Tbg Mod,Vent Header,Gas Delivery System, Princeton Univ
11	1	2012100-80	Tbg Mod,Process Header,Gas Delivery System, Princeton Univ
13	3	0403-0127	Panel Interface Connectors, 2X Outlets GFCI, 15A Max Power Supply
14	1	2012100-90	Tbg Mod, Ar outlet, 1/4 M/FVCR
15	1	2012100-100	Tbg Mod,N2O inlet, Gas Delivery System, Princeton Univ
16	1	2012100-110	Tbg Mod, CO2 inlet, Gas Delivery System, Princeton Univ
18	1	0010-0038	Custom Cabinet, 49" Tall, 46" x 33"
22	1	0401-0041	MFC CONTROL BOX
23	1	SOLENOIDS-0400-0123	ENCLOSURE, CABLES POWER SUPPLY
24	1	S014-0146	Kit, Sprinkler Sys, 155 Deg F, and
25	1	0010-0008-50	Bracket, GFCI, Power Supply
26	6	1420-0060	Cable Assy, DB9 Male x Female, Shielded, 10 ft
27	2	S405-0069	TUBE, MULTI-COLOR, 1/8"OD X 1/16" ID (8-TUBES), HARD95A DUR
28	1	0015-0001	Grommet, 1-1/2" ID, 1/8" X 1-3/4" OD Groove, Buna-N Rubber
29	6	0015-0005	014076
31	1	0015-0004	000895
32	1	0427-0029	Meyers Hub, 3/4" Conduit
33	3	2012100-120-L	Tbg Mod,PGT 3-loops, 1/4" FVCR, Princeton Univ
34	2	0207-0034	FITTING LOCKING CLAMP, 1/4" VCR
35	3	2012100-120-R	Tbg Mod,PGT 3-loops, 1/4" FVCR, Princeton Univ
36	3	0206-0079	Bulkhead Union, 1/4 MVCR, 2.23 Long, <10 Ra EP, Swagelok
37	1	2012100- 150	Tbg Mod,Ar inlet, Gas Delivery System, Princeton Univ
38	1	2012100-140	Vlv Mod,H2O to Chamber,Custom Gas Delivery System, Princeton Univ
39	1	S008-0789	BRKT, REG/PGT1 MTG

APPLIED ENERGY SYSTEMS, INC.
150 QUAKER LANE
MALVERN, PA 19355

TOLERANCES		COMPANY Princeton University	
MATERIAL	APPROVALS / DATE	TITLE Custom Gas Delivery System Princeton University	SIZE D
	DRAWN L.Wang 9/19/2012	TYPE / REQ № AES35182 / DWG № 2012100-00	REV 2
FINISH	CHECKED 9/21/2012	CONTROL Pending / SCALE N/A / SHEET 1 OF 5	

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
0	RELEASED FOR CUSTOMER REVIEW	9/25/12	LWANG
1	Changed Window, studs and slots size per customer request. Changed cabinet color to Light grey	10/8/2012	L.Wang
2	Updated Design Per Customer Req's	10/17/2012	L.Wang





AES gas cabinets meet or exceed all provisions of the Uniform Fire Code.
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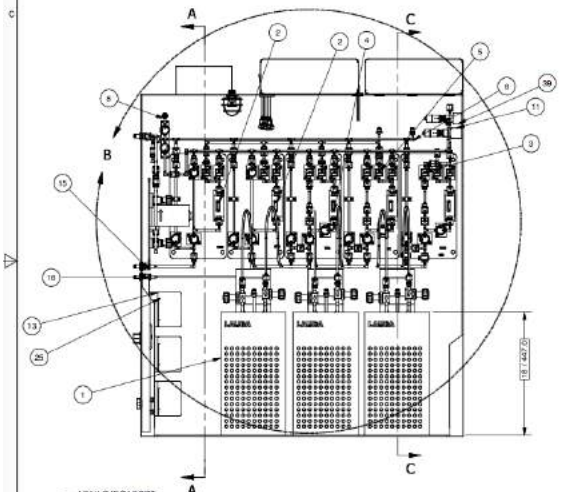
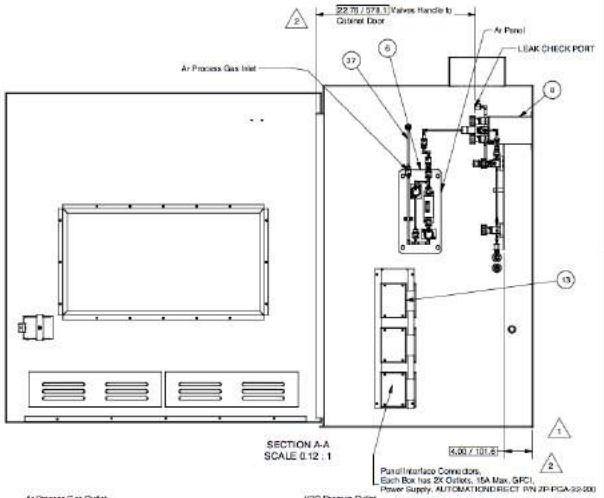
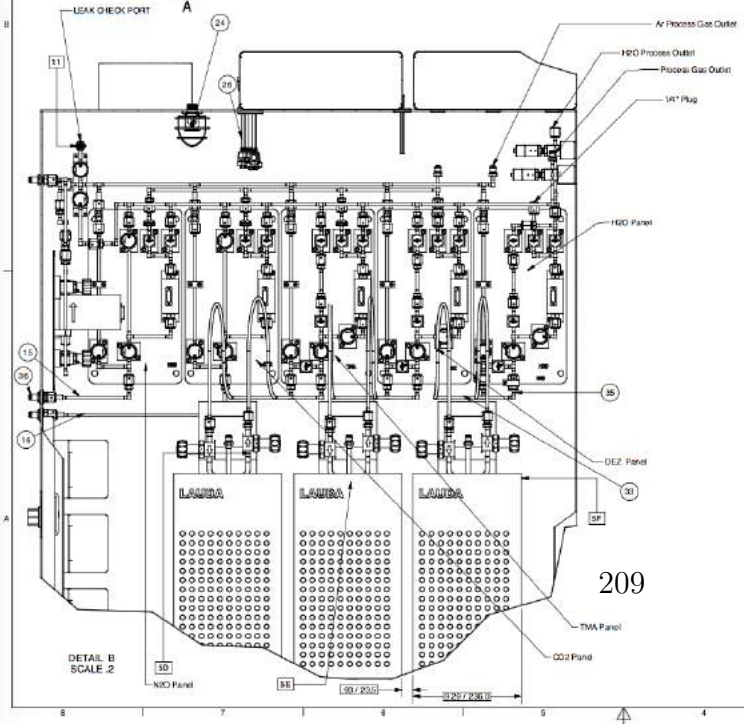
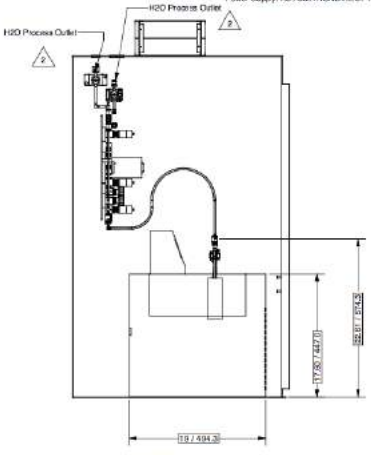
There will be a 6" exhaust duct that extends 4 inches from the top of the gas cabinet.
Gas cabinets are all-welded, 11 gauge, cold rolled (CRS) steel, with powder coated paint. **Color - Light Grey**
The door is self-closing. Gaskets are provided on door and window to control airflow.
The cabinet is provided with wire window, automatic door closure and adjustable air inlet louvers.
A sprinkler head is mounted in the gas cabinet for connection to a water supply.









APPLIED ENERGY SYSTEMS, INC.			
TOLERANCES	COMPANY Princeton University		
MATERIAL	APPROVALS	DATE	TITLE Custom Gas Delivery System Princeton University
	DRAWN L.Wang	9/19/2012	SIZE D
FINISH	CHECKED	9/21/2012	TYPE REQ No AES35182 DWG No 2012100-09 REV 2
	APPROVED		CONTROL Pending SCALE N/A SHEET 2 OF 5

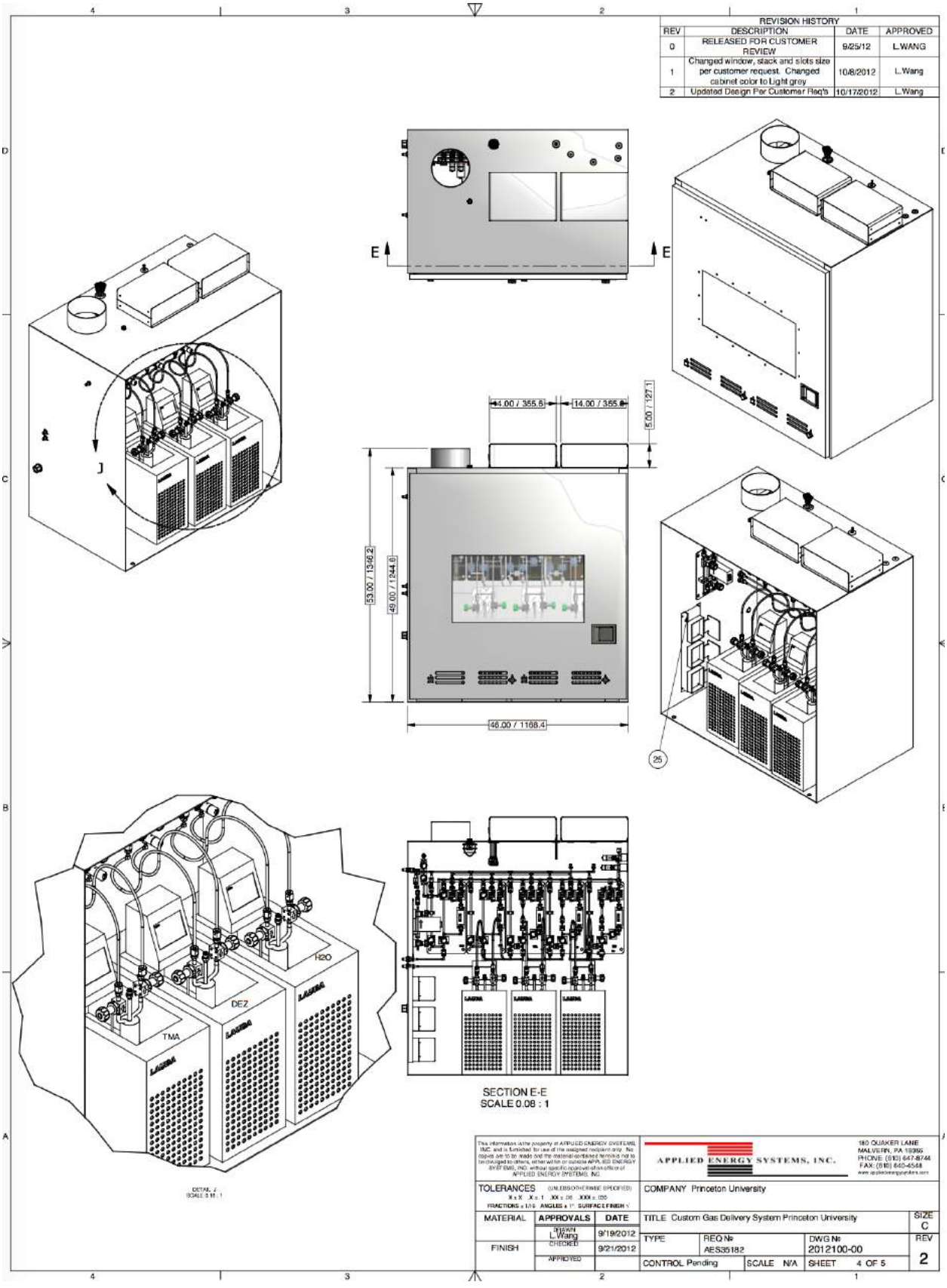
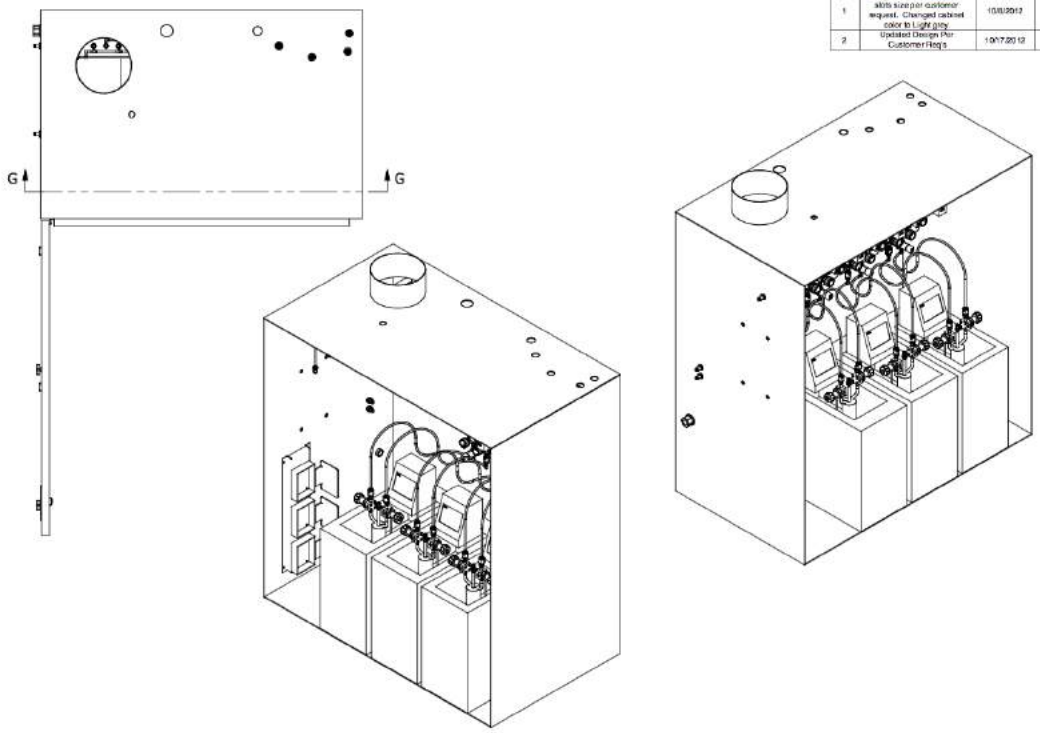
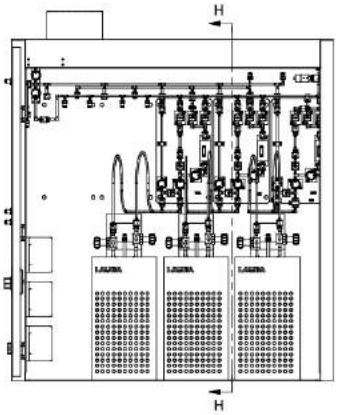
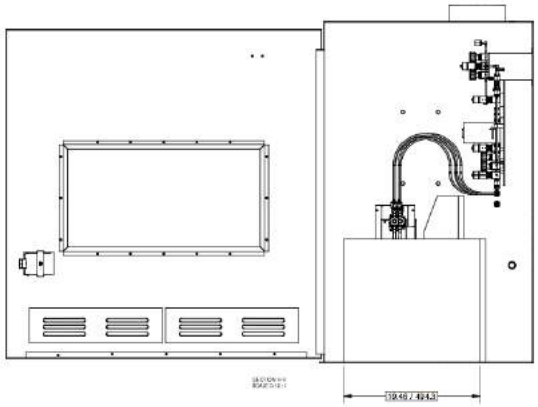


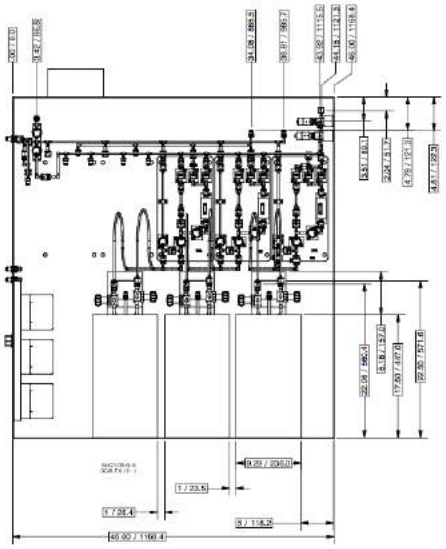
Figure A.12: Dimensioned drawings of gas cabinet (3 of 4).

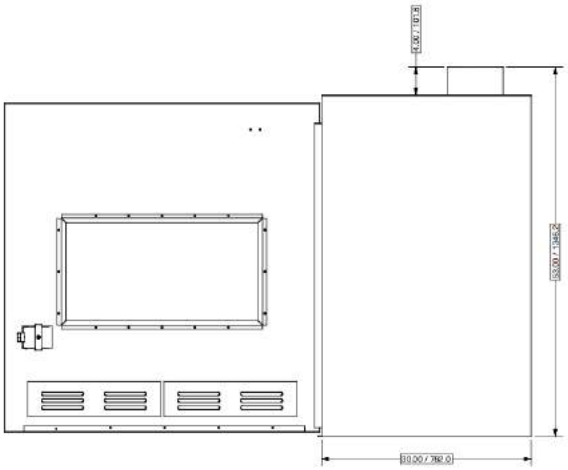
REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
0	RELEASED FOR CUSTOMER REVIEW	9/25/12	L.WANG
1	Changed window, dack and slots size per customer request, Changed cabinet color to Light grey	10/8/2012	L.Wang
2	Updated Design Per Customer Reqs	10/17/2012	L.Wang











APPLIED ENERGY SYSTEMS, INC.				
TOLERANCES	COMPANY Princeton University			
MATERIAL	APPROVALS	DATE	TITLE Custom Gas Delivery System Princeton University	SIZE D
	DRAWN L.Wang	9/19/2012		
FINISH	ENGINEER	9/21/2012	TYPE	REQ № AES35182
	APPROVED		DWG № 2012100-00	REV 2
			CONTROL Pending	SCALE N/A SHEET 5 OF 5

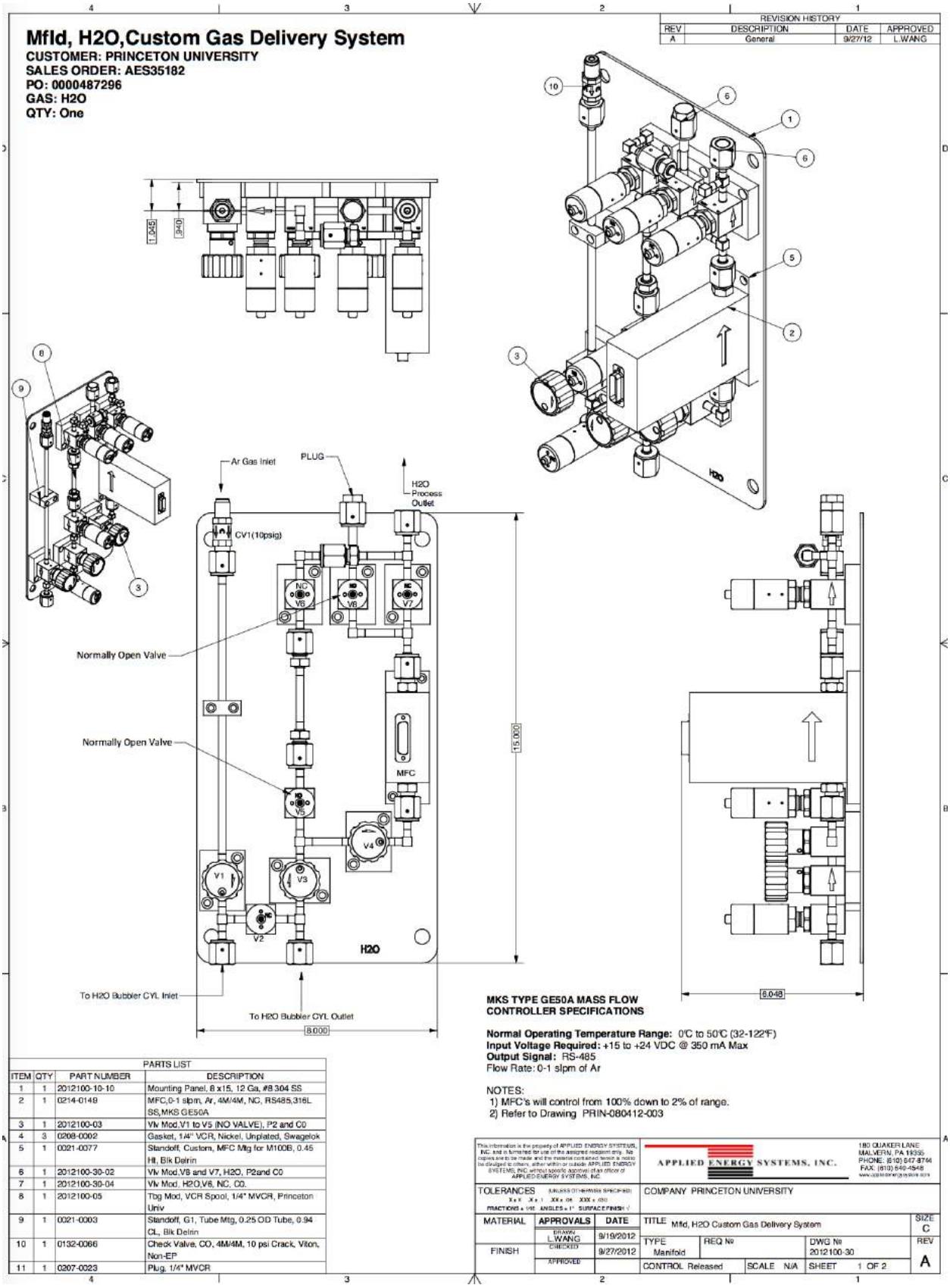


Figure A.14: Dimensioned drawings of H_2O panel (1 of 2).

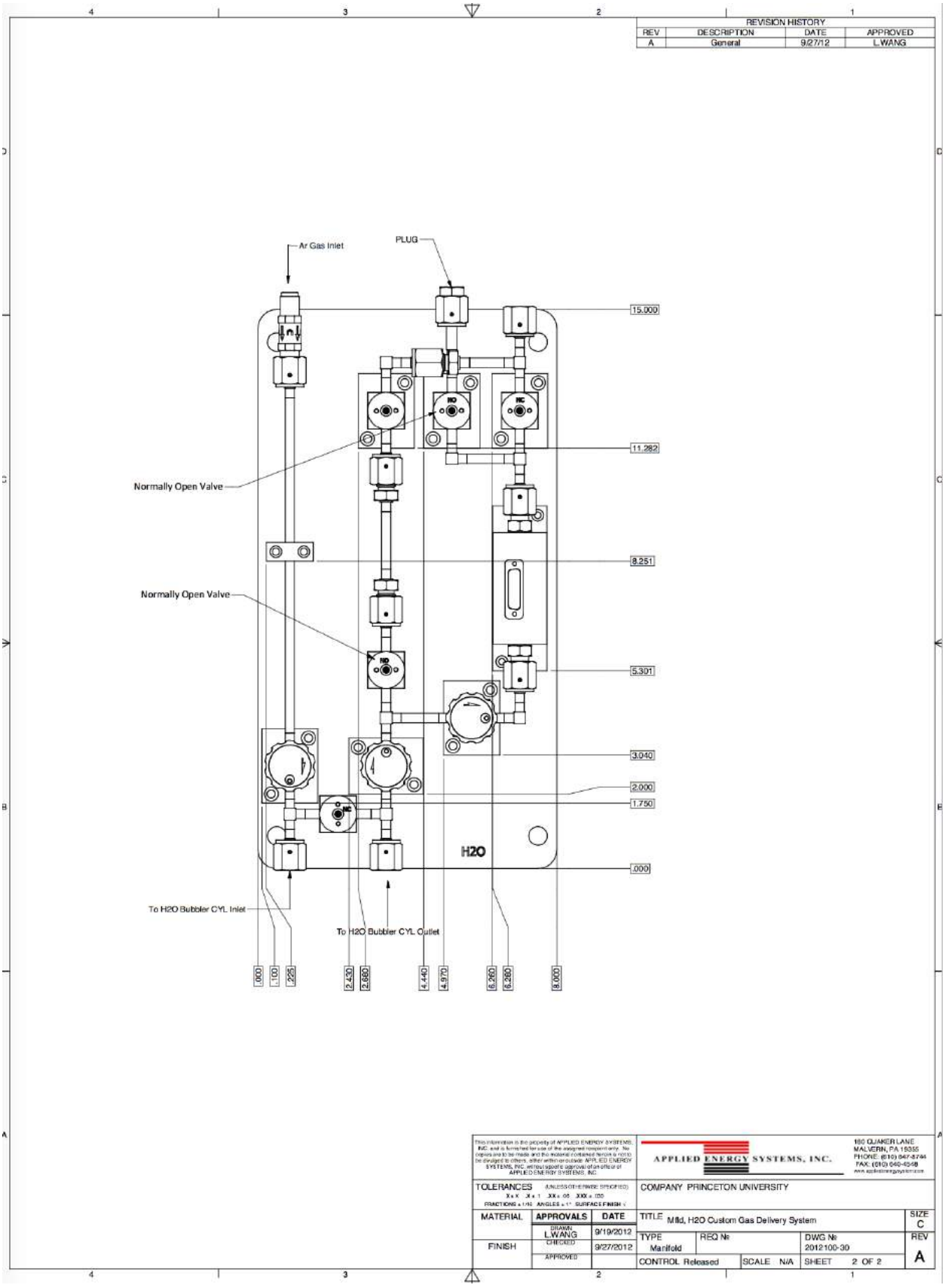


Figure A.15: Dimensioned drawings of H_2O panel (2 of 2).

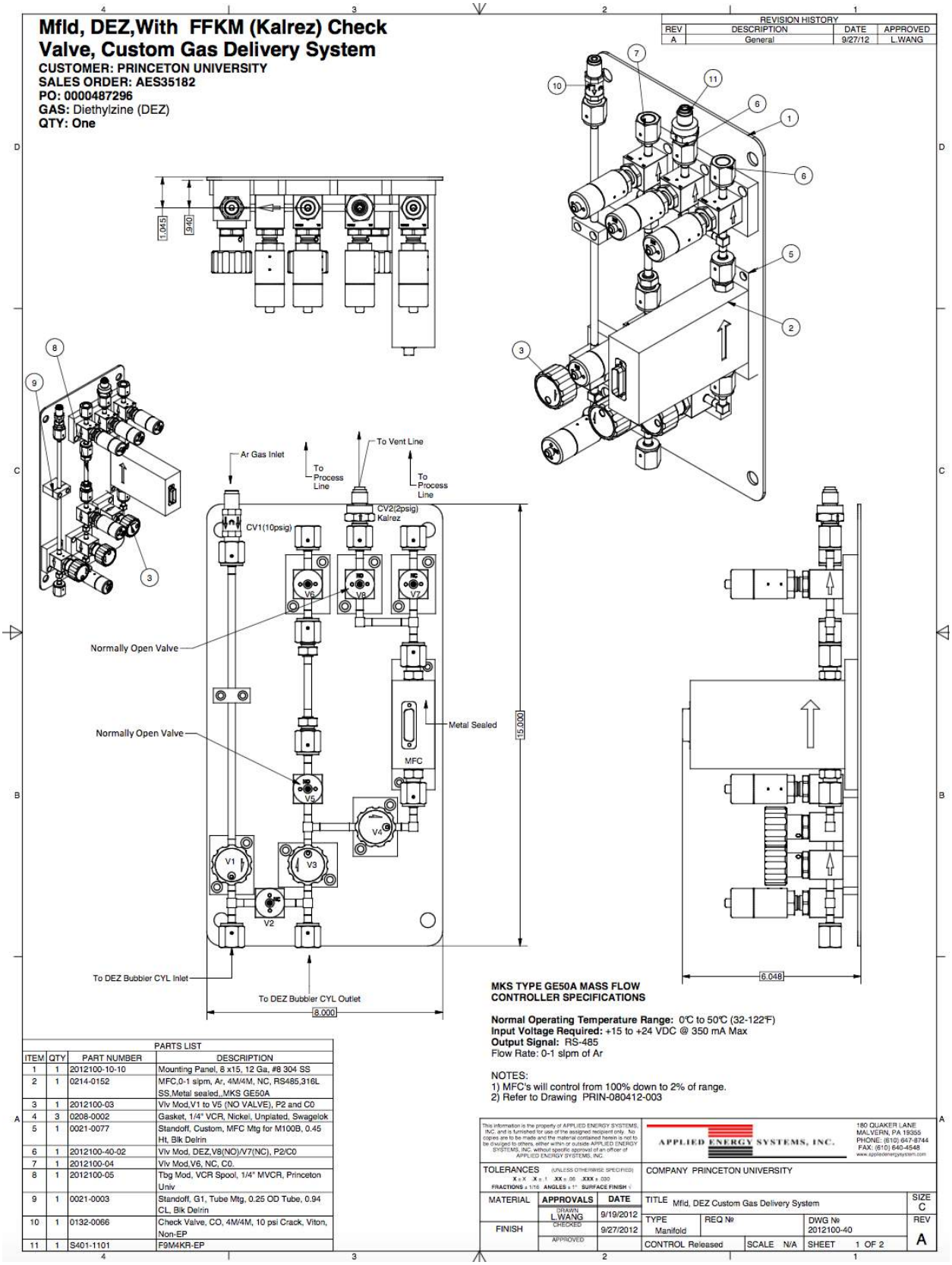


Figure A.16: Dimensioned drawings of DEZ panel (1 of 2).

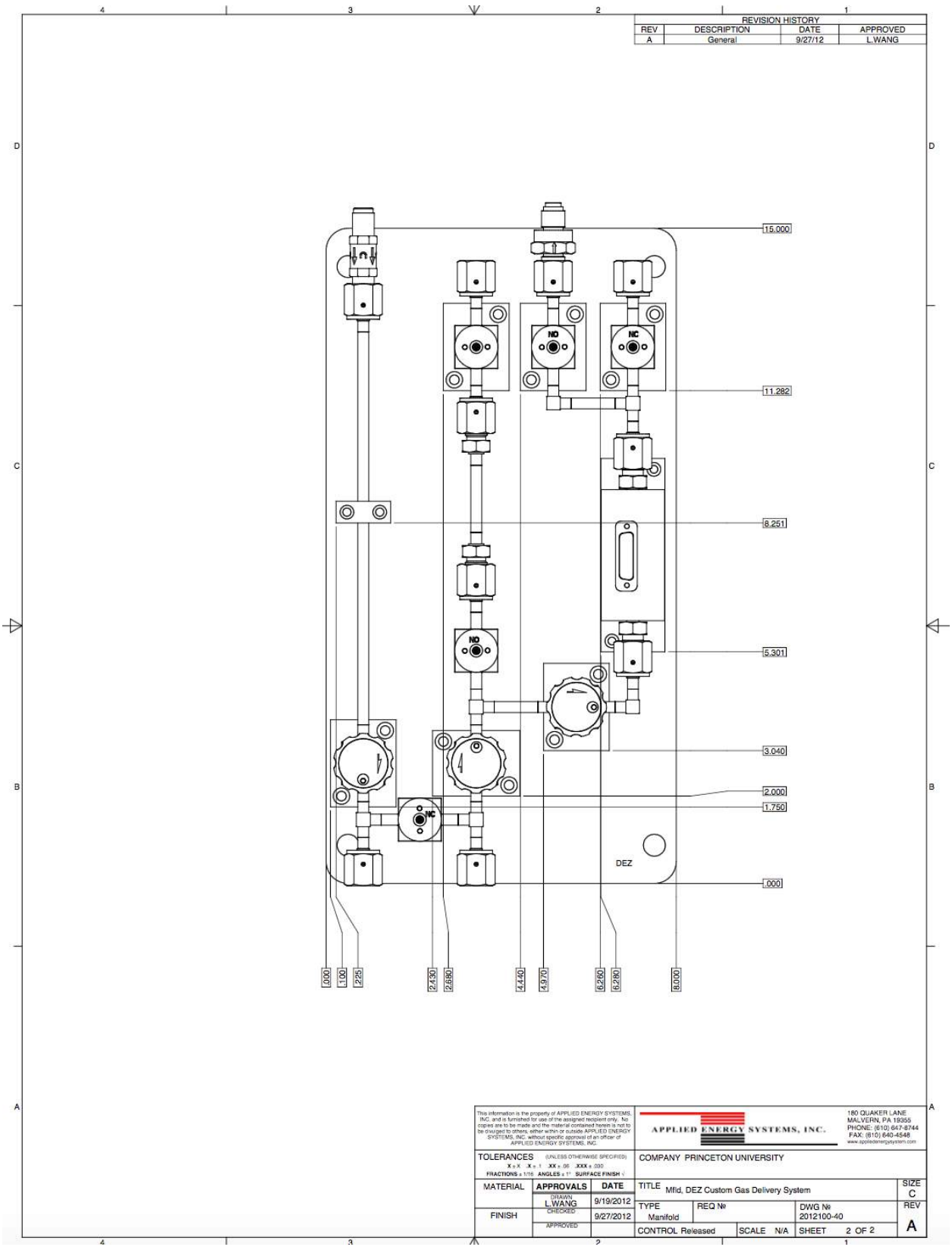


Figure A.17: Dimensioned drawings of DEZ panel (2 of 2).

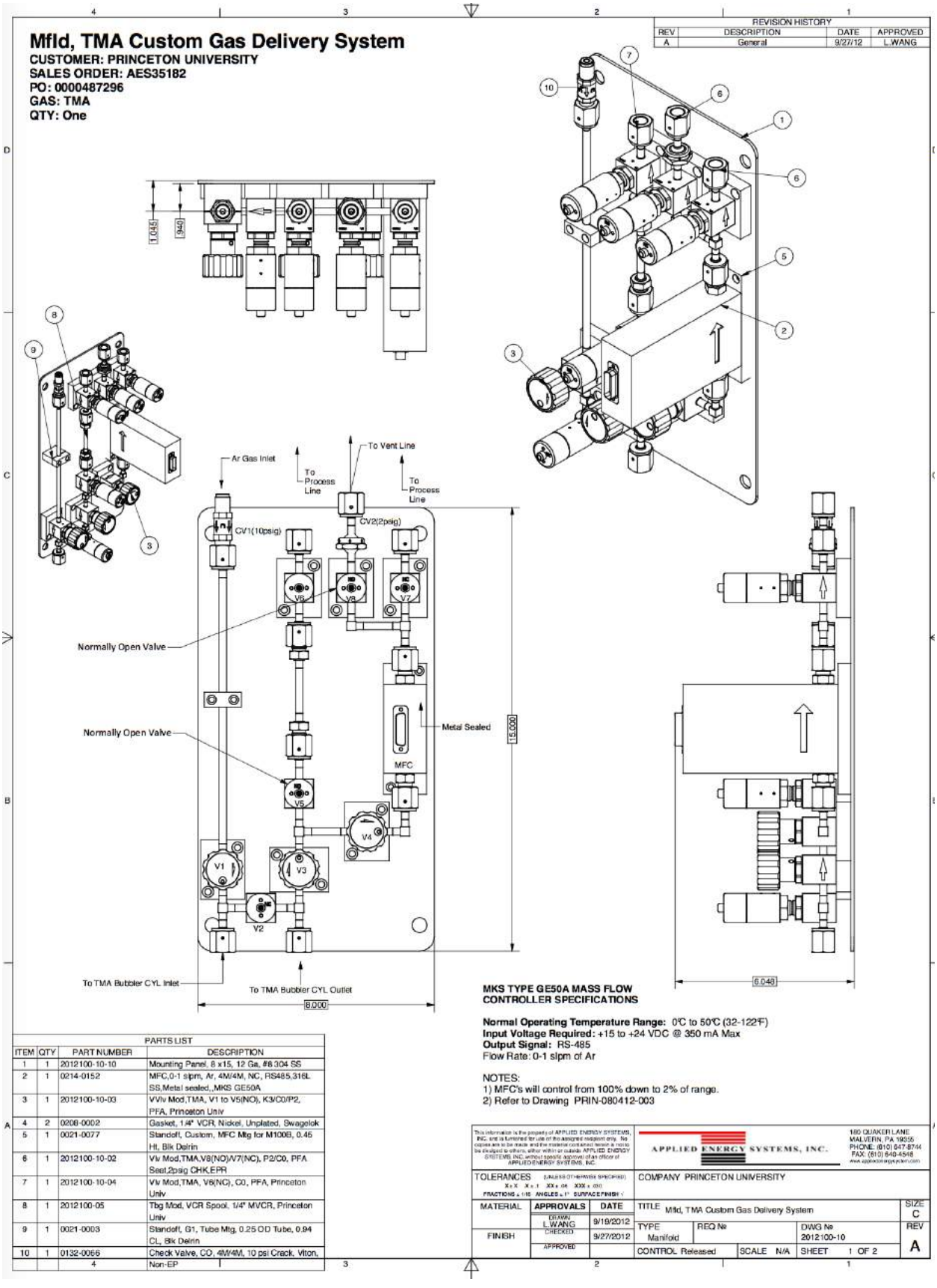


Figure A.18: Dimensioned drawings of TMA panel (1 of 2).

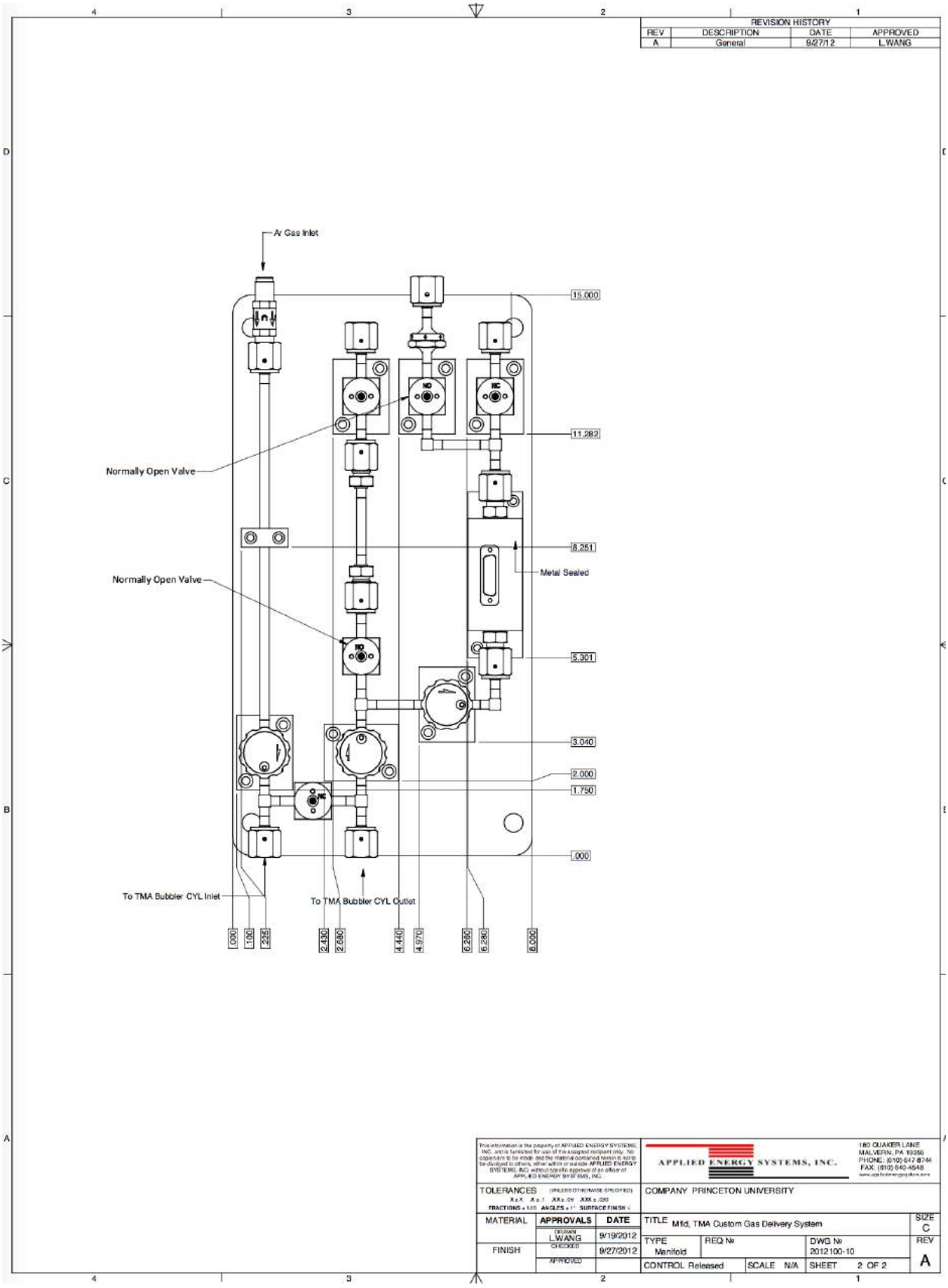


Figure A.19: Dimensioned drawings of TMA panel (2 of 2).

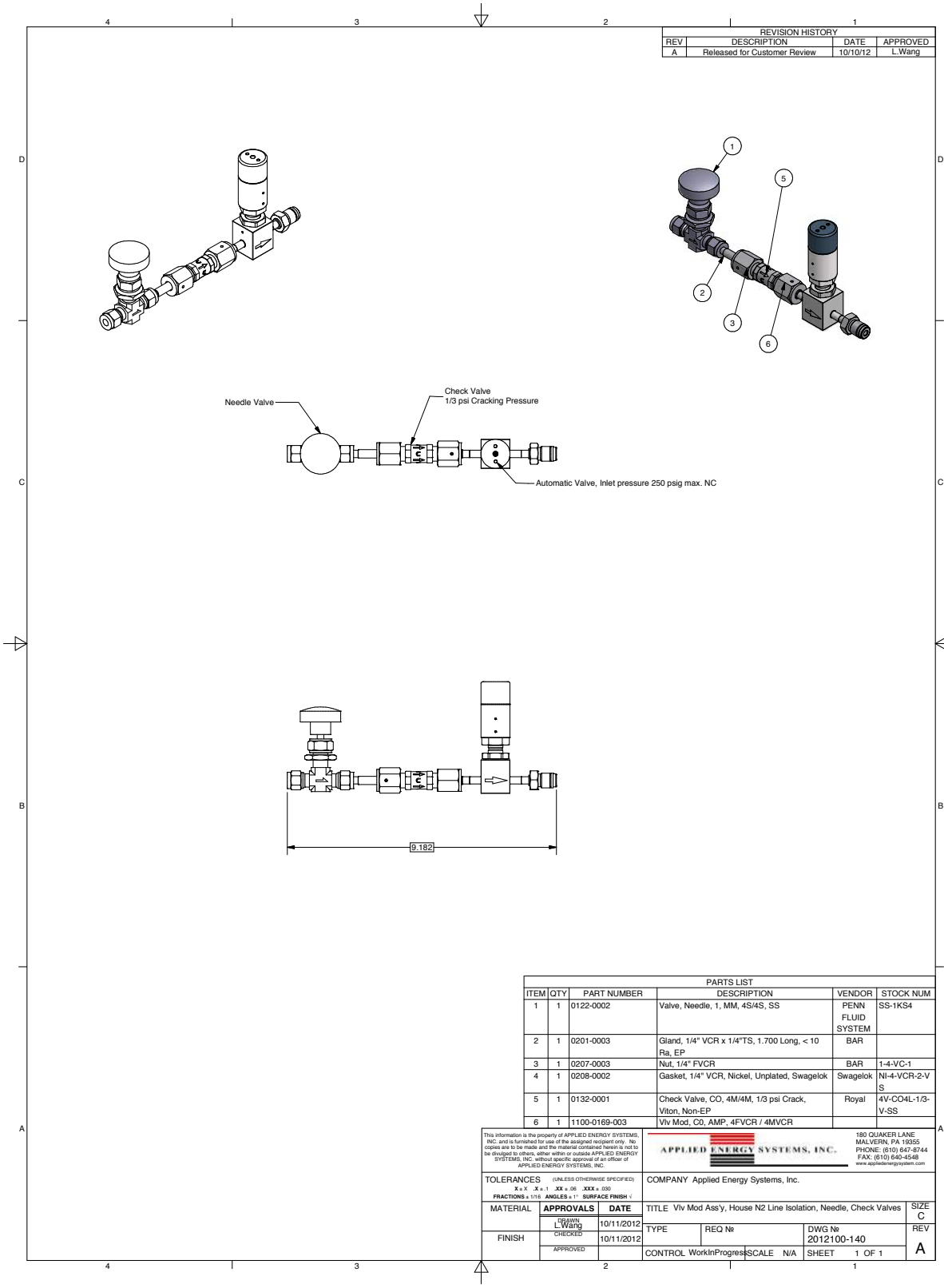
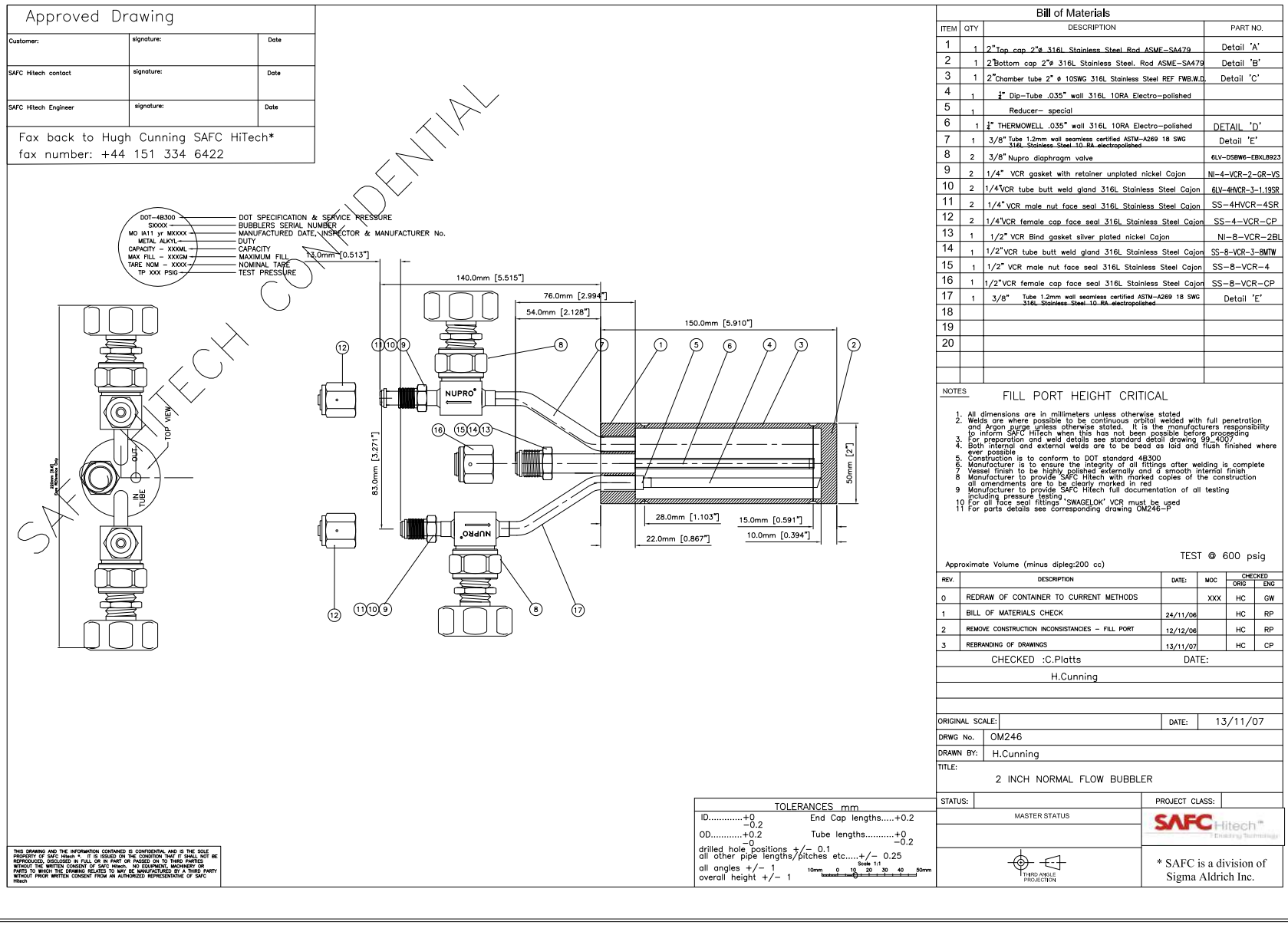


Figure A.20: Dimensioned drawing of N_2 panel (for house nitrogen).

A.3 Bubbler

This section shows the CAD drawing of the bubbler purchased from SAFC Hitech: Figure A.21.



Bill of Materials

ITEM	QTY	DESCRIPTION	PART NO.
1	1	2"Top cap 2"ø 316L Stainless Steel Rod ASME-SA479	Detail 'A'
2	1	2"Bottom cap 2"ø 316L Stainless Steel. Rod ASME-SA479	Detail 'B'
3	1	2"Chamber tube 2" ø 10SWG 316L Stainless Steel REF FWB.W.D.	Detail 'C'
4	1	¼" Dip-Tube .035" wall 316L 10RA Electro-polished	
5	1	Reducer- special	
6	1	¼" THERMOWELL .035" wall 316L 10RA Electro-polished	DETAIL 'D'
7	1	3/8" Tube 1.2mm wall seamless certified ASTM-A269 18 SWG 316L Stainless Steel 10 RA electropolished	Detail 'E'
8	2	3/8" Nupro diaphragm valve	6LV-DSBW6-EBXL8923
9	2	1/4" VCR gasket with retainer unplated nickel Cajon	NI-4-VCR-2-GR-VS
10	2	1/4"VCR tube butt weld gland 316L Stainless Steel Cajon	6LV-4HVCR-3-1.19SR
11	2	1/4" VCR male nut face seal 316L Stainless Steel Cajon	SS-4HVCR-4SR
12	2	1/4"VCR female cap face seal 316L Stainless Steel Cajon	SS-4-VCR-CP
13	1	1/2" VCR Bind gasket silver plated nickel Cajon	NI-8-VCR-2BL
14	1	1/2"VCR tube butt weld gland 316L Stainless Steel Cajon	SS-8-VCR-3-8MTW
15	1	1/2" VCR male nut face seal 316L Stainless Steel Cajon	SS-8-VCR-4
16	1	1/2"VCR female cap face seal 316L Stainless Steel Cajon	SS-8-VCR-CP
17	1	3/8" Tube 1.2mm wall seamless certified ASTM-A269 18 SWG 316L Stainless Steel 10 RA electropolished	Detail 'E'
18			
19			
20			

NOTES

FILL PORT HEIGHT CRITICAL

1. All dimensions are in millimeters unless otherwise stated
2. Welds are where possible to be continuous orbital welded with full penetration and Argon purge unless otherwise stated. It is the manufacturers responsibility to inform SAFC HiTech when this has not been possible before proceeding
3. For preparation and weld details see standard detail drawing 99_4007
4. Both internal and external welds are to be bead as laid and flush finished where ever possible
5. Construction is to conform to DOT standard 4B300
6. Manufacturer is to ensure the integrity of all fittings after welding is complete
7. Vessel finish to be highly polished externally and a smooth internal finish
8. Manufacturer to provide SAFC Hitech with marked copies of the construction all amendments are to be clearly marked in red
9. Manufacturer to provide SAFC Hitech full documentation of all testing including pressure testing.
10. For all Face seal fittings 'SWAGELOK' VCR must be used
11. For parts details see corresponding drawing OM246-P

TEST @ 600 psig

Approximate Volume (minus dipleg:200 cc)

REV.	DESCRIPTION	DATE:	MOC	CHECKED ORIG	CHECKED ENG
0	REDRAW OF CONTAINER TO CURRENT METHODS		XXX	HC	GW
1	BILL OF MATERIALS CHECK	24/11/06		HC	RP
2	REMOVE CONSTRUCTION INCONSISTANCIES – FILL PORT	12/12/06		HC	RP
3	REBRANDING OF DRAWINGS	13/11/07		HC	CP

CHECKED :C.Platts DATE:

H.Cunning

ORIGINAL SCALE: DATE: 13/11/07

DRWG No. OM246

DRAWN BY: H.Cunning

TITLE: 2 INCH NORMAL FLOW BUBBLER

STATUS: PROJECT CLASS:

MASTER STATUS

TOLERANCES mm

ID.....+0 −0.2 End Cap lengths.....+0.2

OD.....+0.2 −0 Tube lengths.....+0 −0.2

drilled hole positions +/− 0.1

all other pipe lengths/pitches etc.....+/− 0.25

all angles +/− 1

overall height +/− 1

Scale 1:1

10mm 0 10 20 30 40 50mm

THIRD ANGLE PROJECTION

SAFC Hitech™ Enabling Technology

* SAFC is a division of Sigma Aldrich Inc.

Figure A.21: Dimensioned drawings of bubbler cylinder.

A.4 Water Bath

This section shows CAD drawing of the water bath purchased from Lauda Brinkmann: Figure A.22.

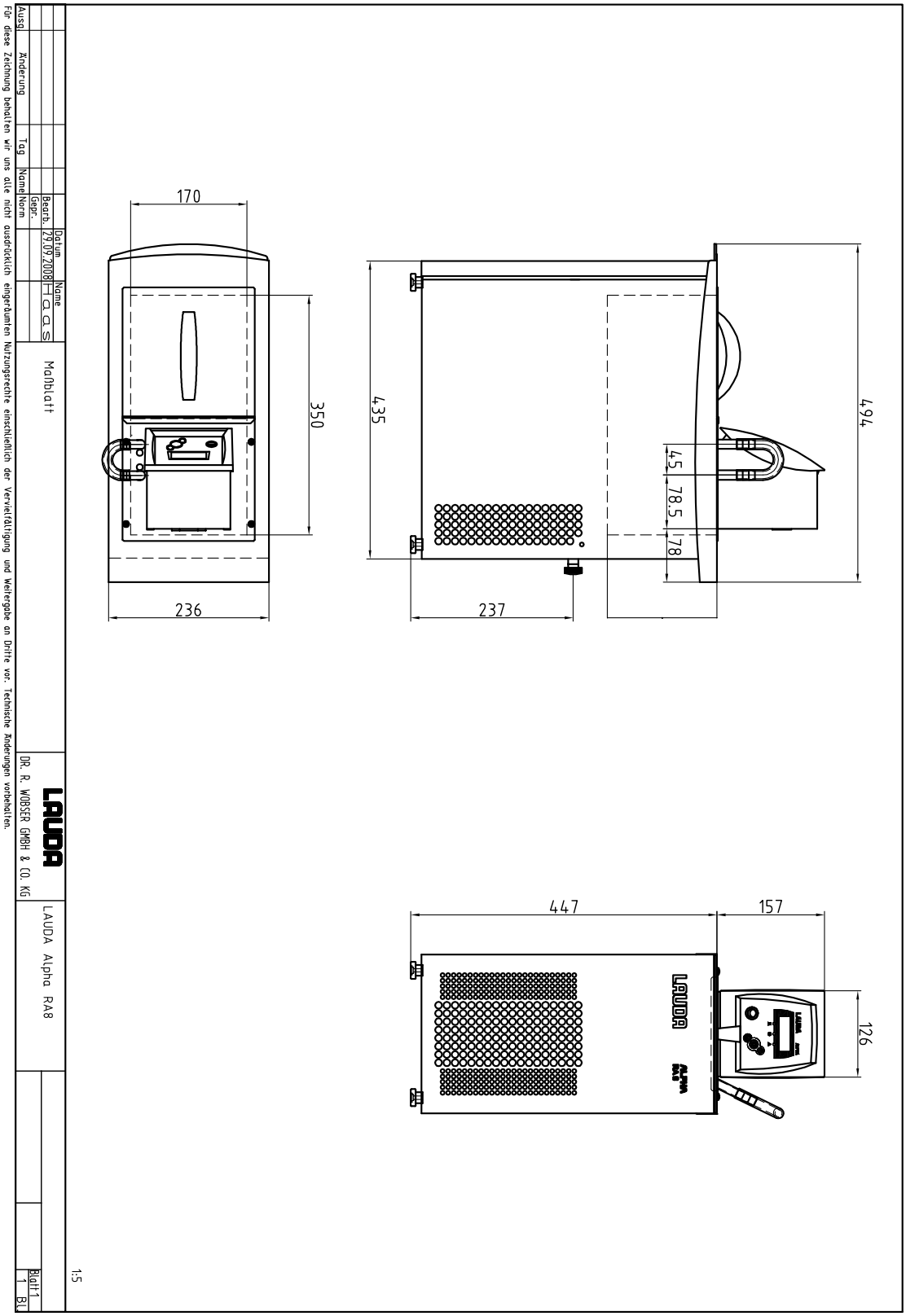


Figure A.22: Dimensioned drawings of water bath.

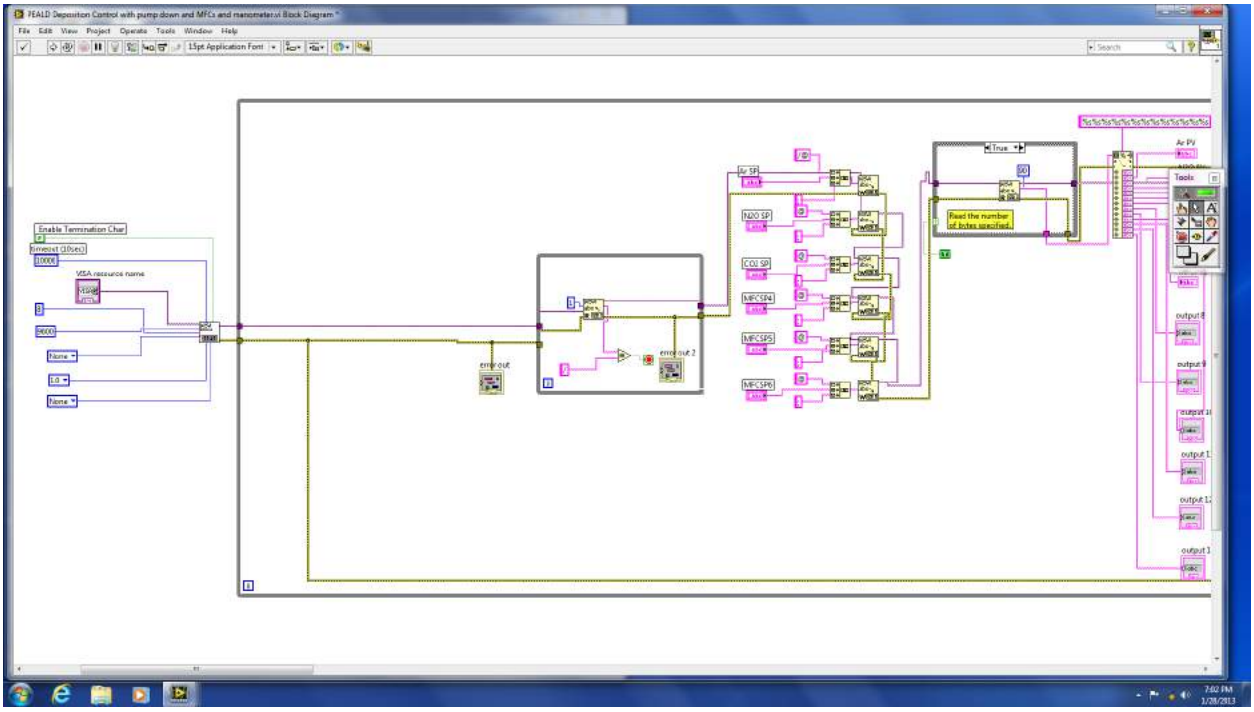


Figure A.23: Labview code screenshot 1 of 6.

A.5 Labview Code

In this section you can find screenshots of the labview code used to program the PEALD system: Figures A.23, A.24, A.25, A.26, A.27, A.28.

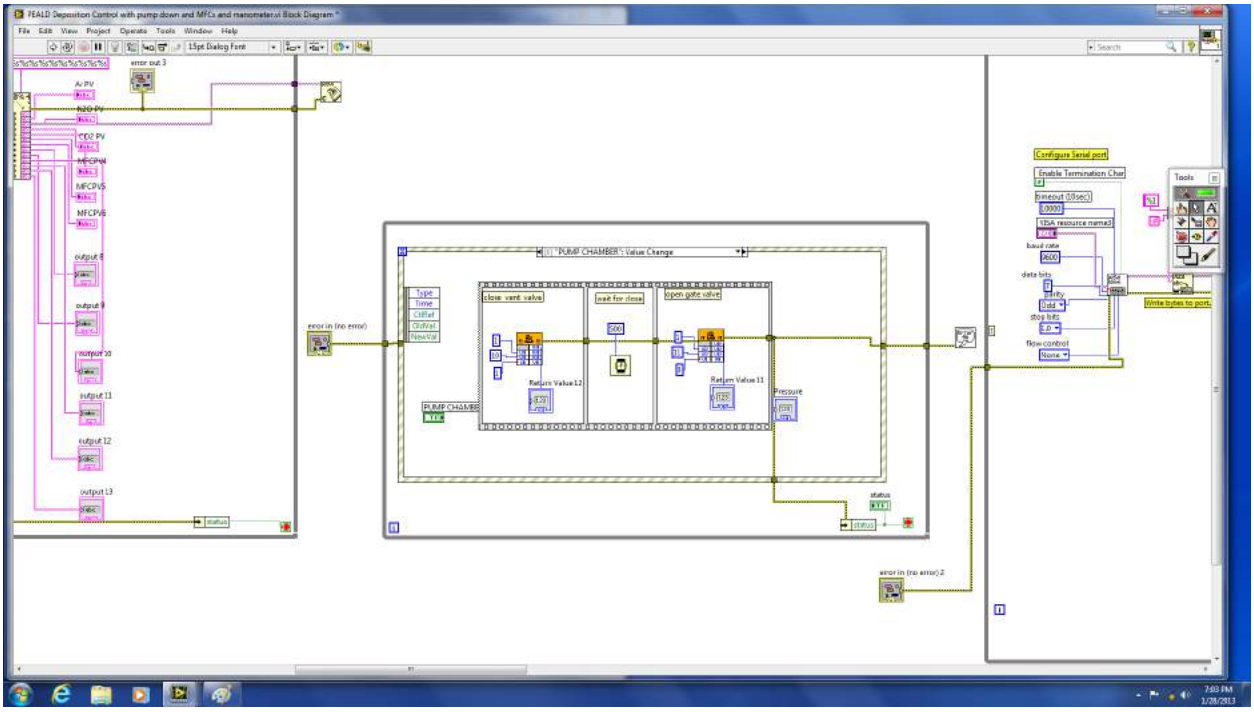


Figure A.24: Labview code screenshot 2 of 6.

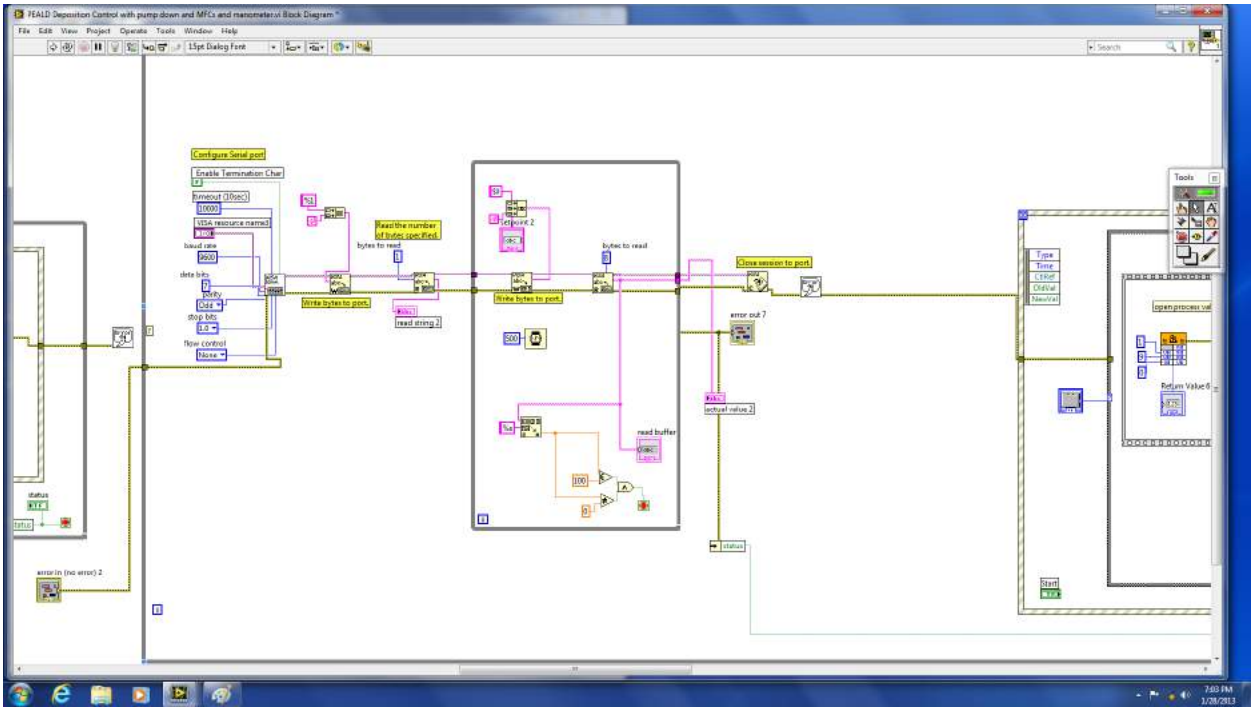


Figure A.25: Labview code screenshot 3 of 6.

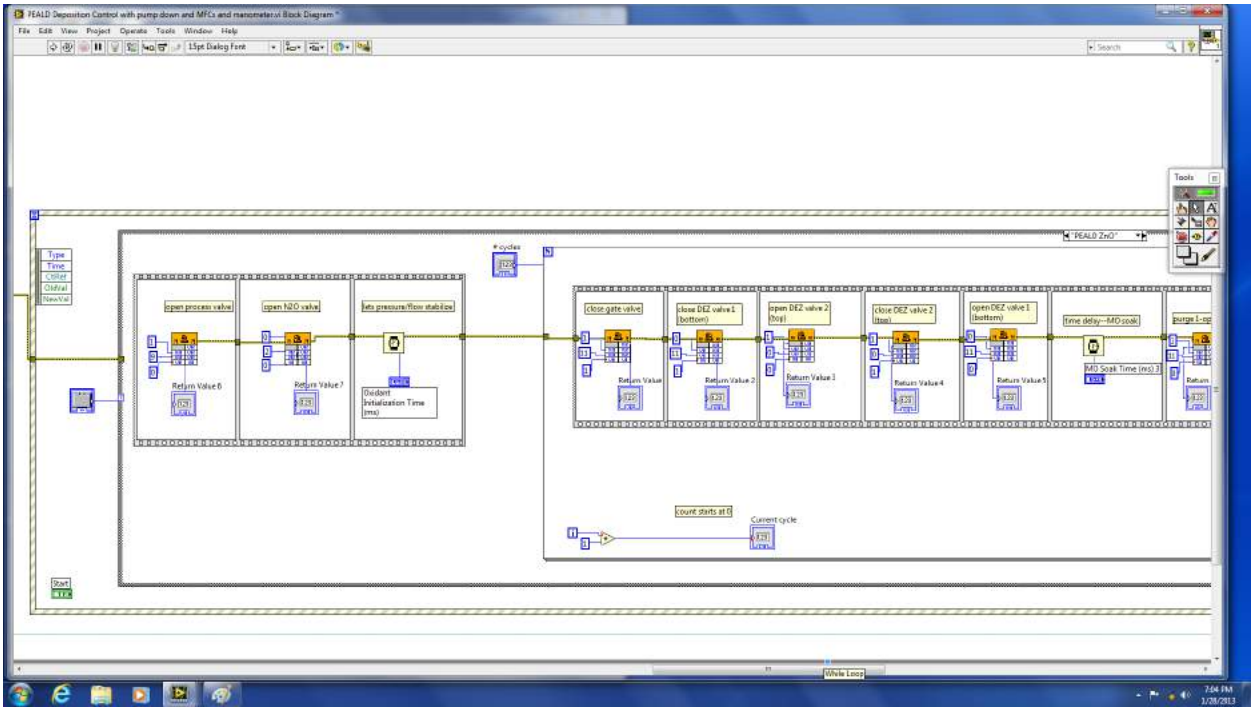


Figure A.26: Labview code screenshot 4 of 6.

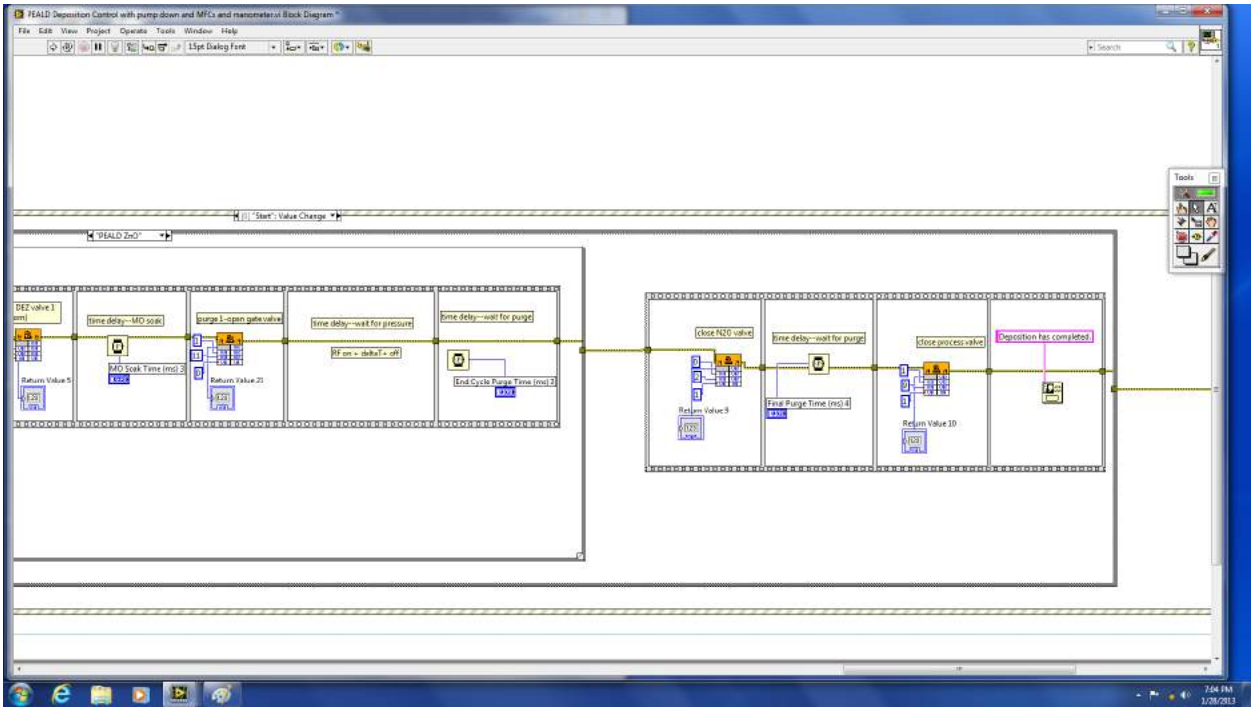


Figure A.27: Labview code screenshot 5 of 6.

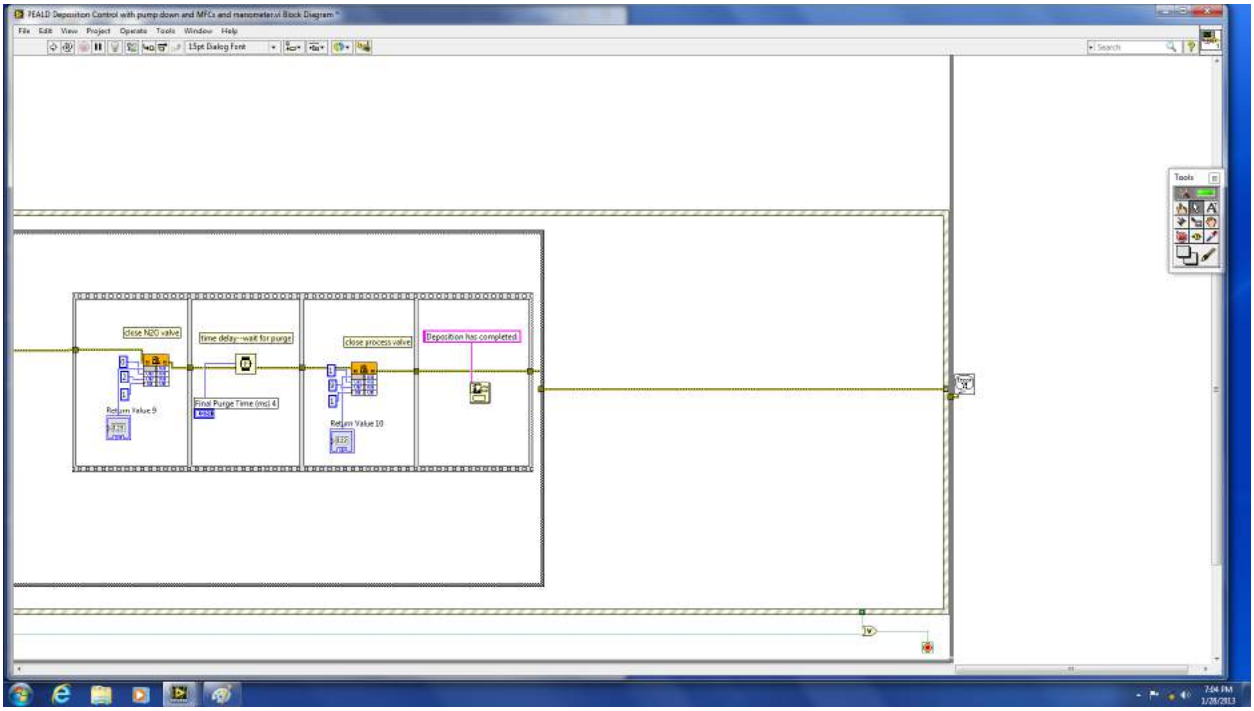


Figure A.28: Labview code screenshot 6 of 6.

Appendix B

TFT-Related Recipes

B.1 Glass Cleaning Procedure

1. Get glass slides out from wire rack under table by the window in J425
2. Blow dry slides individually to remove fiber particles, then place in sample carrier
3. Place sample carrier (with samples) into metal container
4. Put 1 capful of micro 90 in your metal container and fill 5/6 of the way with DI water
5. Put on rightmost hotplate in the fume hood, leaving lid slightly open to prevent bubbling over
6. Set hotplate to "HI", making sure the red light turns on
7. Leave on hotplate for 1 hr–not much longer than that or water will evaporate and expose your samples
8. Turn off heater, lift HOT metal container off and place in sonicator, using a large bunch of texwipes to protect your hands
9. On sonicator, select "SET SONICS", make sure the timer is set to default (60 min), and press "ON"

10. Pour out water and rinse 2X with DI water
11. Repeat steps 4-10
12. Repeat steps 4-10, but WITHOUT Micro 90
13. Leave container filled with fresh DI water with lid on
14. Note: If you use samples infrequently, you may want to check the DI water level to be sure samples are still fully immersed in water

B.2 Unpassivated ZnO TFTs

Gate metal depostion:

1. Use N_2 gun to dry a cleaned glass substrate, and place in 4" plastic sample holder
2. Sputter 100 nm Cr
3. Pattern gate layer:
   (a) 3min 95°C prebake on hotplate
   (b) Spin HMDS, recipe 1 (40sec, 4000rpm)
   (c) Spin AZ 5214 resist, recipe 1 (40sec, 4000rpm)
   (d) 1 min 95°C soft bake on hotplate
   (e) Use MA-6 and gate mask to expose for 40 sec, Al gap 25 μm, hard contact, 5 sec wait time. MAKE SURE YOU LOG IN or the lamp will not turn on!
   (f) Develop in AZ 300MIF for 1 min 20 sec, swirling glass dish
   (g) Rinse thoroughly in DI water
   (h) Dry with N_2 gun
   (i) 3 min 95°C hard bake on hotplate

(j) In acid hood, wet etch Cr with Cr-7 until all the Cr disappears (about 2 min 15 sec)

(k) Rinse thoroughly with DI water

(l) Dry completely with N_2 gun

(m) Strip photoresist with 3 min sonication in acetone, then rinse with acetone and IPA. Do not let the acetone dry before rinsing with IPA!

(n) Dry completely with N_2

(o) Descum in Tepla: ODescum05 (5 min descum recipe)

(p) Sonicate in acetone, rinse in acetone, IPA, DI water and N_2 dry just prior to UV–ozone exposure if time elapses between step m and next step.

Oxide depostion:

1. UV ozone exposure

   (a) First, clean UV ozone oven: set timer to 10 min, and turn on the START button.

   (b) Orange light should turn on

   (c) Within $\sim$ 30 min of oven clean, place sample in center of oven rack, close and lock the chamber, and hit start (timer should still be set for ten minutes, light should turn on). Make sure there are no additional trays or platforms in the UV oven. If there are, remove them.

   (d) After timer has finished, remove sample and exit clean room promptly.

2. Load sample in PEALD chamber. Note: Minimize time between UV ozone exposure and PEALD step

   (a) Vent chamber: hit MANUAL VENT

   (b) Carefully lift lid and place on clean texwipe on lid holder

(c) Place sample in chamber and secure with two metal clips

(d) Replace chamber lid, ensuring that it is centered and RF cable isn't strained

(e) Pump chamber: hit MANUAL PUMP

3. Purge chamber prior to deposition

(a) Set CO_2 MFC to 100 sccm

(b) In process menu, select ALD AL2O3

(c) Set ALD cycles to 0, set CO_2 cycles to 30

(d) Hit "START PROCESS" to purge chamber 30X with CO_2. Repeat as needed to achieve base pressure near 3 mTorr

4. Deposit gate dielectric: 40 nm PEALD Al_2O_3

(a) Make sure CO_2 MFC is set to 100 sccm

(b) Select PEALD Al_2O_3 from the process menu

(c) Enter 325 in no. of cycles

(d) Make sure plasma power is 15 W and plasma time is 3000 ms

(e) Hit START PROCESS.

(f) Make sure pressure immediately prior to deposition phase is between 690 and 697mTorr. If it is not, pause labview and adjust manual throttle valve until correct pressure is achieved.

(g) If plasma does not fire initially, try PAUSING labview while RF power is on, until the matching network adjusts and the plasma turns on with 0 W reflected power. Then deselect PAUSE.

(h) Wait ∼1 hr 45 min, checking on process periodically to make sure plasma fires, etc

(i) When process finished, proceed IMMEDIATELY with ZnO deposition

5. Deposit active layer: 10 nm PEALD ZnO

   (a) Make sure N_2O MFC is set to 100 sccm

   (b) Select PEALD ZnO from the process menu

   (c) Enter 42 in No. of cycles

   (d) Make sure plasma power is 15 W and plasma time is 2500 ms

   (e) Hit START PROCESS. Make sure pressure immediately prior to deposition phase is between 690 and 697 mTorr. If it is not, pause labview and adjust manual throttle valve until correct pressure achieved

   (f) If plasma does not fire initially, try PAUSING labview while RF power is on, until the matching network adjusts and the plasma turns on with 0 reflected power. Then deselect PAUSE.

   (g) When process finished (25 – 30 min), proceed IMMEDIATELY with rest of fabrication

Source and drain deposition:

1. Sonicate in acetone, then acetone and IPA rinse and N_2 dry

2. Now, image reversal...

3. Prebake 10 min 95°C

4. Spin 1X without resist. Then spin AZ 5214 (no HMDS needed), recipe 1

5. Short soft bake, 45 sec 95°C. When done, change hotplate temp to 112°C to allow time to warm up

6. Short expose WITH MASK, 30 sec hard contact (other params the same)

7. Image reversal bake: 1min 15 sec 112°C
8. FLOOD exposure, NO MASK, 60sec. Then WAIT 2 min 30 sec.
9. Develop for 40–50 sec (the shorter you can make it the better, but make absolutely sure development is complete) in AZ300MIF, rinse thoroughly in DI water, N_2 dry
10. Hard bake 120°C 5 min
11. Place in sputterer. 50 nm Ti, 100 nm Au
12. Lift off in acetone in sonicator and do not remove from acetone until all metal appears to have been removed (∼10 min)
13. When removing sample from lift-off beaker, VERY CAREFULLY and IMMEDIATELY drench in fresh acetone, then IPA, then N_2 dry

Isolate devices:

1. 3 min 95C prebake on hotplate
2. 3 min 95C prebake on hotplate
3. Spin HMDS, recipe 1 (40sec, 4000rpm)
4. Spin AZ 5214 resist, recipe 1 (40sec, 4000rpm)
5. 1 min 95C soft bake on hotplate
6. Use MA-6 and VIA mask to expose for 40sec, Al gap 25um, hard contact, 5sec wait time. MAKE SURE YOU LOG IN or the lamp will not turn on!
7. Develop in AZ 300MIF for 1min 20sec, swirling glass dish
8. Rinse thoroughly in DI water
9. Dry with N2 gun

10. 3 min 95C hard bake on hotplate
11. In acid hood, wet etch Al2O3 and ZnO with 80C H3PO4 for 6min–very important we etch all the way through in this step!!
12. Rinse thoroughly with DI water
13. Dry completely with N2 gun
14. Strip photoresist with 3min sonication in acetone, then rinse with acetone, IPA, and DI water. Do not let the acetone dry before rinsing with IPA!
15. Dry completely with N2

B.3 Passivated ZnO TFTs

Total process time: ∼12 hrs total (2 hrs for everything leading up to PEALD, 3.5 hrs for PEALD, 6 hrs for post PEALD processing). If building circuits, additional metallization for interconnects takes about 1 hr extra.

1. OPTION 1, Cr only gate:
   (a) Use N_2 gun to dry a cleaned glass substrate, and place in 4" plastic sample holder
   (b) Sputter 100 nm Cr
   (c) Pattern gate layer:
      i. 3min 95°C prebake on hotplate
      ii. Spin HMDS, recipe 1 (40sec, 4000rpm)
      iii. Spin AZ 5214 resist, recipe 1 (40sec, 4000rpm)
      iv. 1 min 95°C soft bake on hotplate
      v. Use MA-6 and gate mask to expose for 40 sec, Al gap 25 μm, hard contact, 5 sec wait time. MAKE SURE YOU LOG IN or the lamp will not turn on!

vi. Develop in AZ 300MIF for 1 min 20 sec, swirling glass dish

vii. Rinse thoroughly in DI water

viii. Dry with N_2 gun

ix. 3 min 95°C hard bake on hotplate

x. In acid hood, wet etch Cr with Cr-7 until all the Cr disappears (about 2 min 15 sec)

xi. Rinse thoroughly with DI water

xii. Dry completely with N_2 gun

xiii. Strip photoresist with 3 min sonication in acetone, then rinse with acetone and IPA. Do not let the acetone dry before rinsing with IPA!

xiv. Dry completely with N_2

xv. Descum in Tepla: ODescum05 (5 min descum recipe)

xvi. Sonicate in acetone, rinse in acetone, IPA, DI water and N_2 dry just prior to UV–ozone exposure if time elapses between step m and next step.

2. OPTION 2, Cr/Al/Cr gate:

(a) Rinse sample thoroughly in DI water in PECVD room, then N_2 dry. In cleanroom, sonicate glass 3 min in acetone, then rinse with acetone and IPA and N_2 dry

(b) In C405, evaporate min 6 nm Cr / X nm Al/ 22 nm Cr in Edwards. Wait for base pressure of 8E-7 mbar

(c) Pattern gate layer:

i. Sonicate sample 3min in acetone, then rinse with acetone and IPA and N_2 dry

ii. Prebake sample 3 min 95°C on hotplate

iii. Spin HMDS, recipe 1

iv. Spin AZ5214, recipe 1

v. Softbake 1min 95C on hotplate

vi. Center sample under gate mask pattern and expose: 40 sec, hard contact, 25 μm gap, 5 sec wait

vii. Develop $\sim$ 1 min in AZ300MIF, rinse thoroughly with DI water, and N_2 dry check features, then hard bake 3 min 95°C on hotplate

viii. Prepare Cr etchant, Al etchant, and DI water dishes

ix. Etch top Cr, $\sim$ 40 sec in Cr etchant

x. Rinse thoroughly with DI water or immerse in DI and then rinse in DI. Dry sample.

xi. Etch Al, $\sim$5 min for 220 nm in Al etchant (be patient)

xii. Rinse thoroughly with DI water or immerse in DI and then rinse in DI. Dry sample.

xiii. Etch bottom Cr, $\sim$1 min 30 sec in Cr etchant (after Cr appears gone, etch by additional 15 sec)

xiv. Rinse very thoroughly with DI water or immerse in DI and then rinse in DI. Dry sample.

xv. Strip PR: 3–5 min sonication in acetone, rinse in acetone, IPA, and DI water, then N_2 dry.

3. The rest of the recipe is the same, regardless of gate metallization type:

1. UV ozone exposure

(a) First, clean UV ozone oven: set timer to 10 min, and turn on the START button.

(b) Orange light should turn on

(c) Within $\sim$ 30 min of oven clean, place sample in center of oven rack, close and lock the chamber, and hit start (timer should still be set for ten minutes, light

should turn on). Make sure there are no additional trays or platforms in the UV oven. If there are, remove them.

(d) After timer has finished, remove sample and exit clean room promptly.

2. Load sample in PEALD chamber. Note: Minimize time between UV ozone exposure and PEALD step

   (a) Vent chamber: hit MANUAL VENT

   (b) Carefully lift lid and place on clean texwipe on lid holder

   (c) Place sample in chamber and secure with two metal clips

   (d) Replace chamber lid, ensuring that it is centered and RF cable isn't strained

   (e) Pump chamber: hit MANUAL PUMP

3. Purge chamber prior to deposition

   (a) Set CO_2 MFC to 100 sccm

   (b) In process menu, select ALD AL2O3

   (c) Set ALD cycles to 0, set CO_2 cycles to 30

   (d) Hit "START PROCESS" to purge chamber 30X with CO_2. Repeat as needed to achieve base pressure near 3 mTorr

4. Deposit gate dielectric: 40 nm PEALD Al_2O_3

   (a) Make sure CO_2 MFC is set to 100 sccm

   (b) Select PEALD Al_2O_3 from the process menu

   (c) Enter 325 in no. of cycles

   (d) Make sure plasma power is 15 W and plasma time is 3000 ms

   (e) Hit START PROCESS.

(f) Make sure pressure immediately prior to deposition phase is between 690 and 697mTorr. If it is not, pause labview and adjust manual throttle valve until correct pressure is achieved.

(g) If plasma does not fire initially, try PAUSING labview while RF power is on, until the matching network adjusts and the plasma turns on with 0 W reflected power. Then deselect PAUSE.

(h) Wait ∼1 hr 45 min, checking on process periodically to make sure plasma fires, etc

(i) When process finished, proceed IMMEDIATELY with ZnO deposition

5. Deposit active layer: 10 nm PEALD ZnO

(a) Make sure N_2O MFC is set to 100 sccm

(b) Select PEALD ZnO from the process menu

(c) Enter 42 in No. of cycles

(d) Make sure plasma power is 15 W and plasma time is 2500 ms

(e) Hit START PROCESS. Make sure pressure immediately prior to deposition phase is between 690 and 697 mTorr. If it is not, pause labview and adjust manual throttle valve until correct pressure achieved

(f) If plasma does not fire initially, try PAUSING labview while RF power is on, until the matching network adjusts and the plasma turns on with 0 reflected power. Then deselect PAUSE.

(g) When process finished (25 – 30 min), proceed IMMEDIATELY with AL_2O_3 deposition

6. Deposit passivation layer: 35 nm PEALD Al_2O_3

(a) Make sure CO_2 MFC is set to 100 sccm

(b) Select PEALD Al_2O_3 from the process menu

(c) Enter 275 in No. of cycles

(d) Make sure plasma power is 15 W and plasma time is 3000 ms

(e) Hit START PROCESS. Make sure pressure immediately prior to deposition phase is between 690 and 697 mTorr. If it is not, pause labview and adjust manual throttle valve until correct pressure achieved

(f) If plasma does not fire initially, try PAUSING labview while RF power is on, until the matching network adjusts and the plasma turns on with 0 reflected power. Then deselect PAUSE.

(g) Wait ∼1 hr 30 min, checking on process periodically to make sure plasma fires, etc

(h) h. When process finished, promptly remove sample: hit "MANUAL VENT," remove sample, replace lid, and hit "MANUAL PUMP."

7. Source/drain exposure:

(a) Sonicate in acetone, then acetone and IPA rinse and N_2 dry

(b) Prebake 175C 10min on large hotplate/oven in "nanoimprint hood" in litho room

(c) Spin 1X without PMMA. Then Spin PMMA 950k A2 recipe 9: manually enter 60 sec, 4000 rpm, 1000 ramp

(d) Postbake 175°C, 10 min

(e) Now, image reversal...

(f) Prebake 10 min 95°C

(g) Spin 1X without resists. Then spin AZ 5214 (no HMDS needed), recipe 1

(h) Short soft bake, 45 sec 95°C. When done, change hotplate temp to 112°C to allow time to warm up

(i) Short expose WITH MASK, 30 sec hard contact (other params the same)

(j) Image reversal bake: 1min 15 sec 112°C

(k) FLOOD exposure, NO MASK, 60sec. Then WAIT 2 min 30 sec.

(l) Develop for 40–50 sec (the shorter you can make it the better, but make absolutely sure development is complete) in AZ300MIF, rinse thoroughly in DI water, N_2 dry

(m) Hard bake 120°C 5 min

(n) Go pre-clean the plasmatherm: 20 min OClean recipe

(o) Place sample in 790, DESCUM recipe 1 min 15 sec to etch PMMA from S/D. After 35 sec, pause every 10 seconds for 3 seconds. Then, etch with DESCUM again for 20 sec straight.

(p) Etch in $\sim$ 300 mg NaOH / 300 ml H_2O (25 mM solution allowed to warm up for $\sim$30min) at 55°C for 5 min 30 sec, agitate 1X / min. Hold 1 corner down to make sample as flat as possible inside dish Use hotplate from B409!

(q) Rinse thoroughly but gently in DI water and N_2 Dry very very gently

(r) Place in 790, DESCUM 30 sec

(s) Place in sputterer. 50 nm Ti, 100 nm Au

(t) Lift off in acetone in sonicator and do not remove from acetone until all metal appears to have been removed ($\sim$10 min)

(u) When removing sample from lift-off beaker, VERY CAREFULLY and IMMEDIATELY drench in fresh acetone, then IPA, then N_2 dry

8. Isolate devices:

(a) 3 min 95C prebake on hotplate

(b) 3 min 95C prebake on hotplate

(c) Spin HMDS, recipe 1 (40sec, 4000rpm)

(d) Spin AZ 5214 resist, recipe 1 (40sec, 4000rpm)

(e) 1 min 95C soft bake on hotplate

(f) Use MA-6 and VIA mask to expose for 40sec, Al gap 25um, hard contact, 5sec wait time. MAKE SURE YOU LOG IN or the lamp will not turn on!

(g) Develop in AZ 300MIF for 1min 20sec, swirling glass dish

(h) Rinse thoroughly in DI water

(i) Dry with N2 gun

(j) 3 min 95C hard bake on hotplate

(k) In acid hood, wet etch Al2O3 and ZnO with 80C H3PO4 for 6min–very important we etch all the way through in this step!!

(l) Rinse thoroughly with DI water

(m) Dry completely with N2 gun

(n) Strip photoresist with 3min sonication in acetone, then rinse with acetone, IPA, and DI water. Do not let the acetone dry before rinsing with IPA!

(o) Dry completely with N2

9. IF YOU ARE MAKING CIRCUITS, you will need to connect the gate layer to the S/D layer in some places. In this case, add the following steps:

(a) Vias to gate contact:

i. 3 min 95C prebake on hotplate

ii. 3 min 95C prebake on hotplate

iii. Spin HMDS, recipe 1 (40sec, 4000rpm)

iv. Spin AZ 5214 resist, recipe 1 (40sec, 4000rpm)

v. 1 min 95C soft bake on hotplate

vi. Use MA-6 and VIA mask to expose for 40sec, Al gap 25um, hard contact, 5sec wait time. MAKE SURE YOU LOG IN or the lamp will not turn on!

vii. Develop in AZ 300MIF for 1min 20sec, swirling glass dish

viii. Rinse thoroughly in DI water

ix. Dry with N2 gun

x. 3 min 95C hard bake on hotplate

xi. In acid hood, wet etch Al2O3 and ZnO with 80C H3PO4 for 6min–very important we etch all the way through in this step!!

xii. Rinse thoroughly with DI water

xiii. Dry completely with N2 gun

xiv. Strip photoresist with 3min sonication in acetone, then rinse with acetone, IPA, and DI water. Do not let the acetone dry before rinsing with IPA!

xv. Dry completely with N2

B.4 Self-Aligned, Passivated ZnO TFTs

Same as above, except for a few items. The S/D metal must consist of ONLY Ti, as we cannot dry-etch the gold. Aside from this difference, two steps are required to define the S/D metal:

1. Define channel using backside exposure: In step 7i, turn the sample upside down in the MA-6, elevating it on some glass slides to keep it from contacting the rough surface of the substrate holder. Then, expose for slightly longer: 50-55 sec. Then, proceed with the passivated recipe

2. Define outer extent of metal using a dry etch. The design for this mask is essentially a standard S/D mask, but without a channel region. Note that you should not use the island definition mask, since if the same mask is used to isolate devices and to define

the S/D, the S/D will be undercut when the oxide is etched and may short with the gate metal. It is important to always make sure the isolation mask extends BEYOND the S/D area.

(a) 3 min 95C prebake on hotplate

(b) 3 min 95C prebake on hotplate

(c) Spin HMDS, recipe 1 (40sec, 4000rpm)

(d) Spin AZ 5214 resist, recipe 1 (40sec, 4000rpm)

(e) 1 min 95C soft bake on hotplate

(f) Use MA-6 and VIA mask to expose for 40sec, Al gap 25um, hard contact, 5sec wait time. MAKE SURE YOU LOG IN or the lamp will not turn on!

(g) Develop in AZ 300MIF for 1min 20sec, swirling glass dish

(h) Rinse thoroughly in DI water

(i) Dry with N2 gun

(j) 3 min 95C hard bake on hotplate

(k) Use RIE to etch through the Ti with a CF4/O2 plasma

(l) Strip photoresist with 3min sonication in acetone, then rinse with acetone, IPA, and DI water. Do not let the acetone dry before rinsing with IPA!

(m) Dry completely with N2

After this, proceed with normal island isolation using a different mask.

It is important that the gate metal be thick enough that it is opaque, or it will not function properly as a mask.

B.5 PI 2611 Recipe

The following is a recipe for spinning 3.5-μm-thick polyimide substrates from PI2611 (Dupont).

1. Remove PI2611 from storage fridge for 1–2 hours before use, so it can return to room temperature and become less viscous.

2. Solvent clean a 4" silicon wafer to use as a substrate. We typically used "mechanical grade" Si wafers from University Wager because they were cost-effective.

3. Set recipe for spinning. We use a very slow ramp rate to ensure the very viscous PI precursor can distribute evenly across the wafer.

   (a) Stage 1: Ramp from 0 to 500 rpm at a ramp rate of 100rpm/s (e.g., for ten sec)

   (b) Stage 2: Ramp from 500 to 1000 rpm at a ramp rate of 100rpm/s (e.g., for ten sec)

   (c) Stage 3: Ramp from 1000 to 1500 rpm at a ramp rate of 100rpm/s (e.g., for ten sec)

   (d) Stage 4: Ramp from 1500 to 2000 rpm at a ramp rate of 100rpm/s (e.g., for ten sec)

   (e) Stage 5: Ramp from 2000 to 2500 rpm at a ramp rate of 100rpm/s (e.g., for ten sec)

   (f) Stage 6: Ramp from 2500 to 3000 rpm at a ramp rate of 100rpm/s (e.g., for ten sec)

   (g) Stage 7: Ramp from 3000 to 3500 rpm at a ramp rate of 100rpm/s (e.g., for ten sec)

   (h) Stage 8: Ramp from 3500 to 4000 rpm at a ramp rate of 100rpm/s (e.g., for ten sec)

(i) Stage 9: Hold at 4000 rpm for 60 s

4. Test that recipe has been set correctly with dummy wafer.

5. Line spinner with FIBER-FREE fancy texwipes.

6. Place wafer on spinner chuck.

7. Pour a small amount of PI2611 directly from a small bottle (not from the main bottle..). The amount required is VERY small, about the size of a quarter should suffice.

8. Proceed with spinning recipe.

9. Place sample on room temperature hot plate and gradually increase temperature to 90°C for soft-bake. Cover with a clean quartz dish to prevent particles from settling in PI, but make sure there is space for air to escape under the dish.

10. Place sample in quartz wafer carrier and transfer to furnace to cure:

    (a) Turn on N_2 and make sure it is flowing.

    (b) Set furnace ramp rate to 2°C/min.

    (c) Set final setpoint to 350°C.

    (d) Place sample inside and allow to cure for 1 hr after setpoint has been reached. Will take about 3.5 hours to complete.

    (e) Set setpoint to RT and wait for sample to cool before removing.

    (f) Turn off N_2.

Bibliography

[1] J. Robertson and B. Falabretti. Electronic structure of transparent conducting oxides. In *Handbook of Transparent Conductors*, pages 27–50. Springer, 2011.

[2] Fumiyasu Oba, Atsushi Togo, Isao Tanaka, Joachim Paier, and Georg Kresse. Defect energetics in ZnO: A hybrid Hartree-Fock density functional study. *Physical Review B*, 77(24):245202, 2008.

[3] Hong Li, Laura K. Schirra, Jaewon Shim, Hyeunseok Cheun, Bernard Kippelen, Oliver L. A. Monti, and Jean-Luc Bredas. Zinc oxide as a model transparent conducting oxide: A theoretical and experimental study of the impact of hydroxylation, vacancies, interstitials, and extrinsic doping on the electronic properties of the polar ZnO (0002) surface. *Chemistry of Materials*, 24(15):3044–3055, 2012.

[4] K. Jacobi, G. Zwicker, and A. Gutmann. Work function, electron affinity and band bending of zinc oxide surfaces. *Surface Science*, 141(1):109–125, 1984.

[5] Robert K. Swank. Surface properties of II-VI compounds. *Physical Review*, 153(3):844, 1967.

[6] M. Nakano, A Tsukazaki, R. Y. Gunji, K. Ueno, A. Ohtomo, T. Fukumura, and M. Kawasaki. Schottky contact on a ZnO (0001) single crystal with conducting polymer. *Applied Physics Letters*, 91(14):142113, 2007.

[7] S. A. Chevtchenko, J. C. Moore, Ü. Özgür, Xing Gu, A. A. Baski, Hadis Morkoç, B. Nemeth, and J. E. Nause. Comparative study of the (0001) and (000 1^{-}) surfaces of ZnO. *Applied Physics Letters*, 89(18):182111, 2006.

[8] R. A. Powell, W. E. Spicer, and J. C. McMenamin. Photoemission studies of wurtzite zinc oxide. *Physical Review B*, 6(8):3056, 1972.

[9] V. Srikant and D. R. Clarke. On the optical band gap of zinc oxide. *Journal of Applied Physics*, 83(10):5447–5451, 1998.

[10] Ü. Özgür, Ya. I. Alivov, Chunli Liu, A. Teke, M. A. Reshchikov, S. Doğan, V. Avrutin, S.-J. Cho, and H. Morkoc. A comprehensive review of ZnO materials and devices. *Journal of Applied Physics*, 98(4):11, 2005.

[11] S. Cheng and Z. Wu. Microfluidic electronics. *Lab on a Chip*, 12(16):2782–2791, Jun. 2012.

[12] T. Yokota, Y. Inoue, Y. Terakawa, J. Reeder, M. Kaltenbrunner, T. Ware, K. Yang, K. Mabuchi, T. Murakawa, M. Sekino, W. Voit, T. Sekitani, and T. Someya. Ultraflexible, large-area, physiological temperature sensors for multipoint measurements. *Proceedings of the National Academy of Sciences of the United States of America*, 112(47):14533–14538, Sept. 2015.

[13] W. Gao, S. Emaminejad, H. Y. Y. Nyein, S. Challa, K. Chen, A. Peck, H. M. Fahad, H. Shiraki H. Ota, D. Kiriya, D.-H. Lien, G. A. Brooks, R. W. Davis, and A. Javey. Fully integrated wearable sensor arrays for multiplexed in situ perspiration analysis. *Nature*, 529(7587):509–514, Jan. 2016.

[14] Y. Hu, L. Huang, W. Rieutort-Louis, J. Sanz-Robinson, J. C. Sturm, S. Wagner, and N. Verma. A self-powered system for large-scale strain sensing by combining CMOS ICs with large-area electronics. *IEEE Journal of Solid-State Circuits*, 49(4):838–850, Apr. 2014.

[15] Josue Sanz-Robinson, Liechao Huang, Tiffany Moy, Warren Rieutort-Louis, Yingzhe Hu, Sigurd Wagner, James C. Sturm, and Naveen Verma. Large-area microphone array for audio source separation based on a hybrid architecture exploiting thin-film electronics and CMOS. *IEEE Journal of Solid-State Circuits*, 51(4):979–991, 2016.

[16] T. Moy, L. Huang, W. Rieutort-Louis, C. Wu, P. Cuff, S. Wagner, J. C. Sturm, and N. Verma. An EEG acquisition and biomarker-extraction system using low-noise-amplifier and compressive-sensing circuits based on flexible, thin-film electronics. *IEEE Journal of Solid-State Circuits*, 52(1):309–321, Jan. 2017.

[17] T. P. Brody, F. C. Luo, Z. P. Szepesi, and D. H. Davies. A 6 × 6-in 20-LPI electroluminescent display panel. *IEEE Transactions on Electron Devices*, 22(9):739–748, Sep. 1975.

[18] Martin Stutzmann and Christoph E. Nebel. Silicon, amorphous. *Encyclopedia of Applied Physics*, 18:151, 1997.

[19] Yue Kuo. *Thin film transistors. 1. Amorphous silicon thin film transistors*, volume 1. Springer Science & Business Media, 2004.

[20] A. Pecora, L. Maiolo, M. Cuscunà, D. Simeone, A. Minotti, L. Mariucci, and G. Fortunato. Low-temperature polysilicon thin film transistors on polyimide substrates for electronics on plastic. *Solid-State Electronics*, 52(3):348–352, 2008.

[21] A. T. Voutsas. A new era of crystallization: advances in polysilicon crystallization and crystal engineering. *Applied Surface Science*, 208:250–262, 2003.

[22] John Y. W. Seto. The electrical properties of polycrystalline silicon films. *Journal of Applied Physics*, 46(12):5247–5254, 1975.

[23] Ludolf Herbst. Excimer laser advances enable high-performance flat panel displays-excimer lasers are key to the low-temperature annealing of polycrystalline silicon for the volume production of flat panel. *Photonics Spectra*, 40(8):68–75, 2006.

[24] S. D. Brotherton. Polycrystalline silicon thin film transistors. *Semiconductor Science and Technology*, 10(6):721, 1995.

[25] Anderson Janotti and Chris G. Van de Walle. Fundamentals of zinc oxide as a semiconductor. *Reports on Progress in Physics*, 72(12):126501, 2009.

[26] Kenji Nomura, Hiromichi Ohta, Akihiro Takagi, Toshio Kamiya, Masahiro Hirano, and Hideo Hosono. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature*, 432(7016):488, 2004.

[27] Ajay Bhoolokam, Manoj Nag, Soeren Steudel, Jan Genoe, Gerwin Gelinck, Andrey Kadashchuk, Guido Groeseneken, and Paul Heremans. Conduction mechanism in amorphous InGaZnO thin film transistors. *Japanese Journal of Applied Physics*, 55(1):014301, 2015.

[28] Toshio Kamiya, Kenji Nomura, and Hideo Hosono. Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping. *Journal of Display Technology*, 5(7):273–288, 2009.

[29] Veaceslav Coropceanu, Jérôme Cornil, Demetrio A. da Silva Filho, Yoann Olivier, Robert Silbey, and Jean-Luc Brédas. Charge transport in organic semiconductors. *Chemical Reviews*, 107(4):926–952, 2007.

[30] Brijesh Kumar, Brajesh Kumar Kaushik, and Yuvraj Singh Negi. Organic thin film transistors: structures, models, materials, fabrication, and applications: a review. *Polymer Reviews*, 54(1):33–111, 2014.

[31] Björn Lüssem, Moritz Riede, and Karl Leo. Doping of organic semiconductors. *Physica Status Solidi (A)*, 210(1):9–43, 2013.

[32] Steven M. George. Atomic layer deposition: an overview. *Chem. Rev.*, 110(1):111–131, 2010.

[33] Tuomo Suntola. Atomic layer epitaxy. *Thin Solid Films*, 216(1):84–89, 1992.

[34] C. A. Wilson, R. K. Grubbs, and S. M. George. Nucleation and growth during Al_2O_3 atomic layer deposition on polymers. *Chemistry of Materials*, 17(23):5625–5634, 2005.

[35] Mikko Ritala, Markku Leskela, Jan-Pieter Dekker, Cees Mutsaers, Pekka J. Soininen, and Jarmo Skarp. Perfectly conformal TiN and Al_2O_3 films deposited by atomic layer deposition. *Chem. Vap. Deposition*, 5(1):7–9, 1999.

[36] H. B. Profijt, S. E. Potts, M. C. M. Van de Sanden, and W. M. M. Kessels. Plasma-assisted atomic layer deposition: basics, opportunities, and challenges. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, 29(5):050801, 2011.

[37] M. Martinez-Sanchez and P. Lozano. Overview of the physics in the plasma sheath. MIT OpenCourseWare, 2015.

[38] M. Verghese, J. W. Maes, and N. Kobayashi. Atomic layer deposition goes mainstream in 22nm logic technologies. *Solid State Technology*, 53(10):18–22, 2010.

[39] Robertus Johannes Maria Mathilde Snijkers. *The sheath of an RF plasma: measurements and simulations of the ion energy distribution*. PhD thesis, Technische Universiteit Eindhoven, 1993.

[40] H. B. Smith, Christine Charles, and R. W. Boswell. Breakdown behavior in radio-frequency argon discharges. *Physics of Plasmas*, 10(3):875–881, 2003.

[41] Ernst Granneman, Pamela Fischer, Dieter Pierreux, Herbert Terhorst, and Peter Zagwijn. Batch ALD: Characteristics, comparison with single wafer ALD, and examples. *Surface and Coatings Technology*, 201(22):8899–8907, 2007.

[42] Kris Myny, Jan Genoe, and Wim Dehaene. *Robust Design of Digital Circuits on Foil*. Cambridge University Press, 2016.

[43] I-Chun Cheng and Sigurd Wagner. Nanocrystalline silicon thin film transistors. *IEE Proceedings-Circuits, Devices and Systems*, 150(4):339–344, 2003.

[44] Y. Afsar, J. Tang, W. Rieutort-Louis, L. Huang, Y. Hu, J. Sanz-Robinson, N. Verma, S. Wagner, and J.C. Sturm. Impact of bending on flexible metal oxide TFTs and oscillator circuits. *Jnl Soc. Info Display*, 2016.

[45] Xinghui Liu, Hai Ou, Jun Chen, Shaozhi Deng, Ningsheng Xu, and Kai Wang. Highly photosensitive dual-gate a-Si:H TFT and array for low-dose flat-panel X-Ray imaging. *IEEE Photonics Technology Letters*, 28(18):1952–1955, 2016.

[46] Corning 0211 Microsheet Product Information. `https://coresix.com/files/1513/8375/8935/0211.pdf`. Accessed: 2017-07-30.

[47] Properties of 7740 Pyrex Glass. `http://www.valleydesign.com/pyrex.htm`. Accessed: 2017-07-30.

[48] K. Long, A. Z. Kattamis, I.-C. Cheng, H. Gleskova, Sigurd Wagner, J. C. Sturm, M. Stevenson, G. Yu, and M. O'Regan. Active-matrix amorphous-silicon TFT arrays at 180°C on clear plastic and glass substrates for organic light-emitting displays. *IEEE Transactions on Electron Devices*, 53(8):1789–1796, 2006.

[49] Saleem Khan, Leandro Lorenzelli, and Ravinder S. Dahiya. Technologies for printing sensors and electronics over large flexible substrates: a review. *IEEE Sensors Journal*, 15(6):3164–3185, 2015.

[50] C. M. Boutry, A. Nguyen, Q. O. Lawal, A. Chortos, S. Rondeau-Gagne, and Z. Bao. A sensitive and biodegradable pressure sensor array for cardiovascular monitoring. *Advanced Materials*, 27(43):6954–6961, Sept. 2015.

[51] K. Ishida, T.-C. Huang, K. Honda, Y. Shinozuka, H. Fuketa, T. Yokota, U. Zschieschang, H. Klauk, G. Tortissier, T. Sekitani, H. Toshiyoshi, M. Takamiya, T. Someya, and T. Sakurai. Insole pedometer with piezoelectric energy harvester and 2 V organic circuits. *IEEE Journal of Solid-State Circuits*, 48(1):255–264, Jan. 2013.

[52] K. Myny, E. van Veenenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans. An 8-bit, 40-instructions-per-second organic microprocessor on plastic foil. *IEEE Journal of Solid-State Circuits*, 47(1):284–291, Jan. 2012.

[53] K. Myny, S. Smout, M. Rockele, A. Bhoolokam, T. H. Ke, S. Steudel, B. Cobb, A. Gulati, F. G. Rodriguez, K. Obata, M. Marinkovic, D.-V. Pham, A. Hoppe, G. Gelinck, J. Genoe, W. Dehaene, and P. Heremans. A thin-film microprocessor with inkjet print-programmable memory. *Scientific Reports*, 4(7398):1–6, Dec. 2014.

[54] E. Cantatore, T. C. T. Geuns, G. H. Gelinck, E. van Veenendaal, A. F. A. Gruijthuijsen, L. Schrijnemakers, S. Drews, and D. M. De Leeuw. A 13.56-MHz RFID system based on organic transponders. *IEEE Journal of Solid-State Circuits*, 42(1):84–92, Jan. 2007.

[55] P. Harpe, E. Cantatore, and A. van Roermund. A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with data-driven noise reduction. In *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pages 270–271, Feb. 2013.

[56] V. Fiore, E. Ragonese, S. Abdinia, S. Jacob, I. Chartier, R. Coppard, A. van Roermund, E. Cantatore, and G. Palmisano. A 13.56MHz RFID tag with active envelope detection in an organic complementary TFT technology. In *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pages 492–493, Feb. 2014.

[57] W. Rieutort-Louis, L. Huang, Y. Hu, J. Sanz-Robinson, T. Moy, Y. Afsar, J.C. Sturm, N. Verma, and S. Wagner. Current gain of amorphous silicon thin-film transistors above the cutoff frequency. In *Device Research Conference Dig. Tech. Papers*, pages 273–274, Jun. 2014.

[58] N. Verma, Y. Hu, L. Huang, W. Rieutort-Louis, J. Sanz Robinson, T. Moy, B. Glisic, S. Wagner, and J. C. Sturm. Enabling scalable hybrid systems: architectures for exploiting large-area electronics in applications. *Proc. of the IEEE*, 103(4):690–712, Apr. 2015.

[59] Y. Hu, W. Rieutort-Louis, L. Huang, J. Sanz-Robinson, S. Wagner, J. C. Sturm, and N. Verma. Flexible solar-energy harvesting system on plastic with thin-film LC oscillators operating above f_t for inductively-coupled power delivery. In *Proc. IEEE Custom Integrated Circuits Conference*, pages 1–4, Sept. 2012.

[60] P. G. LeComber, W. E. Spear, and A. Ghaith. Amorphous-silicon field-effect device and possible application. *Electronics Letters*, 15(6):179–181, Mar. 1979.

[61] David B. Mitzi, Laura L. Kosbar, Conal E. Murray, Matthew Copel, and Ali Afzali. High-mobility ultrathin semiconducting films prepared by spin coating. *Nature*, 428(6980):299, 2004.

[62] Juan Li, Yuxiang Wu, Jian Xu, and Jianjun Zhang. Ambipolar organic-inorganic hybrid perovskite TFTs. In *Meeting Abstracts*, number 33, pages 2124–2124. The Electrochemical Society, 2016.

[63] Chuan Wang, Kuniharu Takei, Toshitake Takahashi, and Ali Javey. Carbon nanotube electronics–moving forward. *Chemical Society Reviews*, 42(7):2592–2609, 2013.

[64] Max M. Shulaker, Gage Hills, Nishant Patil, Hai Wei, Hong-Yu Chen, H.-S. Philip Wong, and Subhasish Mitra. Carbon nanotube computer. *Nature*, 501(7468):526–530, 2013.

[65] Tae-Jun Ha, Kevin Chen, Steven Chuang, Kin Man Yu, Daisuke Kiriya, and Ali Javey. Highly uniform and stable n-type carbon nanotube transistors by using positively charged silicon nitride thin films. *Nano Letters*, 15(1):392–397, 2014.

[66] Felice Torrisi, Tawfique Hasan, Weiping Wu, Zhipei Sun, Antonio Lombardo, Tero S. Kulmala, Gen-Wen Hsieh, Sungjune Jung, Francesco Bonaccorso, Philip J. Paul, Daping Chu, and Andrea C. Ferrari. Inkjet-printed graphene electronics. *ACS Nano*, 6(4):2992–3006, 2012.

[67] Saungeun Park, Seung Heon Shin, Maruthi N. Yogeesh, Alvin L. Lee, Somayyeh Rahimi, and Deji Akinwande. Extremely high-frequency flexible graphene thin-film transistors. *IEEE Electron Device Letters*, 37(4):512–515, 2016.

[68] Lei Sun, Guoxuan Qin, Jung-Hun Seo, George K Celler, Weidong Zhou, and Zhenqiang Ma. 12-GHz thin-film transistors on transferrable silicon nanomembranes for high-performance flexible electronics. *Small*, 6(22):2553–2557, 2010.

[69] Hoon-Sik Kim, Sang Min Won, Young-Geun Ha, Jong-Hyun Ahn, Antonio Facchetti, Tobin J. Marks, and John A. Rogers. Self-assembled nanodielectrics and silicon nanomembranes for low voltage, flexible transistors, and logic gates on plastic substrates. *Applied Physics Letters*, 95(18):183504, 2009.

[70] Jong-Hyun Ahn, Hoon-Sik Kim, Keon Jae Lee, Zhengtao Zhu, Etienne Menard, Ralph G. Nuzzo, and John A. Rogers. High-speed mechanically flexible single-crystal silicon thin-film transistors on plastic substrates. *IEEE Electron Device Letters*, 27(6):460–462, 2006.

[71] Robert A. Street. *Hydrogenated Amorphous Silicon*. Cambridge University Press, 2005.

[72] R. A. Street, M. Hack, and W. B. Jackson. Mechanisms of thermal equilibration in doped amorphous silicon. *Physical Review B*, 37(8):4209, 1988.

[73] M. H. Brodsky and D. Kaplan. Hydrogenation and the density of defect states in amorphous silicon. *Journal of Non-Crystalline Solids*, 32(1-3):431–435, 1979.

[74] M. Stutzmann. The defect density in amorphous silicon. *Philosophical Magazine B*, 60(4):531–546, 1989.

[75] Z.E. Smith and S. Wagner. Intrinsic dangling-bond density in hydrogenated amorphous silicon. *Physical Review B*, 32(8):5510, 1985.

[76] M. J. Powell, S. C. Deane, I. D. French, J. R. Hughes, and W. I. Milne. A defect-pool model for near-interface states in amorphous silicon thin-film transistors. *Philosophical Magazine B*, 63(1):325–336, 1991.

[77] Ting Liu. *Stability of amorphous silicon thin film transistors and circuits*. PhD thesis, Princeton University, 2013.

[78] J. K. Rath. Low temperature polycrystalline silicon: a review on deposition, physical properties and solar cell applications. *Solar Energy Materials and Solar Cells*, 76(4):431–487, 2003.

[79] Toshiyuki Sameshima, Masaki Hara, and Setsuo Usui. XeCl excimer laser annealing used to fabricate poly-Si TFT's. *Japanese Journal of Applied Physics*, 28(10):1789, 1989.

[80] Tolis Voutsas. Low temperature polysilicon technology for advanced display systems. *Sharp Technical Journal*, pages 51–56, 1997.

[81] K. F. Lee, J. F. Gibbons, K. C. Saraswat, and T. I. Kamins. Thin film MOSFET's fabricated in laser-annealed polycrystalline silicon. *Applied Physics Letters*, 35(2):173–175, 1979.

[82] Seiki Ogura, Paul J. Tsang, William W. Walker, Dale L. Critchlow, and Joseph F. Shepard. Design and characteristics of the lightly doped drain-source (LDD) insulated gate field-effect transistor. *IEEE Transactions on Electron Devices*, 27(8):1359–1367, 1980.

[83] Chennupati Jagadish and Stephen J. Pearton. *Zinc oxide bulk, thin films and nanostructures: processing, properties, and applications*. Elsevier, 2011.

[84] Takuya Matsuo, Shigeyasu Mori, Atsushi Ban, and Akihiko Imaya. 8.3: Invited paper: Advantages of IGZO oxide semiconductor. In *SID Symposium Digest of Technical Papers*, volume 45, pages 83–86. Wiley Online Library, 2014.

[85] Joon Seok Park, Wan-Joo Maeng, Hyun-Suk Kim, and Jin-Seong Park. Review of recent developments in amorphous oxide semiconductor thin-film transistor devices. *Thin Solid Films*, 520(6):1679–1693, 2012.

[86] John L. Lyons, Anderson Janotti, and Chris G. Van de Walle. Theory and modeling of oxide semiconductors. *Semiconductors and Semimetals*, 88:1–37, 2013.

[87] Zhenwei Wang, Pradipta K. Nayak, Jesus A. Caraveo-Frescas, and Husam N. Alshareef. Recent developments in p-type oxide semiconductor materials and devices. *Advanced Materials*, 28(20):3831–3892, 2016.

[88] Suman Nandy, Arghya Banerjee, Elvira Fortunato, and Rodrigo Martins. A review on Cu_2O and CuI-based p-type semiconducting transparent oxide materials: promising candidates for new generation oxide based electronics. *Reviews in Advanced Sciences and Engineering*, 2(4):273–304, 2013.

[89] Jun-Hyun Park, Kichan Jeon, Sangwon Lee, Sangwook Kim, Sunil Kim, Ihun Song, Jaechul Park, Youngsoo Park, Chang Jung Kim, Dong Myong Kim, and Dae Hwan Kim. Self-consistent technique for extracting density of states in amorphous InGaZnO thin film transistors. *Journal of the Electrochemical Society*, 157(3):H272–H277, 2010.

[90] Toshio Kamiya, Kenji Nomura, and Hideo Hosono. Origin of definite Hall voltage and positive slope in mobility-donor density relation in disordered oxide semiconductors. *Applied Physics Letters*, 96(12):122103, 2010.

[91] Toshio Kamiya, Kenji Nomura, and Hideo Hosono. Present status of amorphous In–Ga–Zn–O thin-film transistors. *Science and Technology of Advanced Materials*, 11(4):044305, 2010.

[92] W. Chr Germs, W. H. Adriaans, A. K. Tripathi, W. S. C. Roelofs, B. Cobb, R. A. J. Janssen, G. H. Gelinck, and Martijn Kemerink. Charge transport in amorphous InGaZnO thin-film transistors. *Physical Review B*, 86(15):155319, 2012.

[93] D. Gaspar, L. Pereira, K. Gehrke, B. Galler, E. Fortunato, and R. Martins. High mobility hydrogenated zinc oxide thin films. *Solar Energy Materials and Solar Cells*, 163:255–262, 2017.

[94] Klaus Ellmer and André Bikowski. Intrinsic and extrinsic doping of ZnO and ZnO alloys. *Journal of Physics D: Applied Physics*, 49(41):413002, 2016.

[95] Shanmugam Parthiban and Jang-Yeon Kwon. Role of dopants as a carrier suppressor and strong oxygen binder in amorphous indium-oxide-based field effect transistor. *Journal of Materials Research*, 29(15):1585–1596, 2014.

[96] Hisato Yabuta, Masafumi Sano, Katsumi Abe, Toshiaki Aiba, Tohru Den, Hideya Kumomi, Kenji Nomura, Toshio Kamiya, and Hideo Hosono. High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature RF-magnetron sputtering. *Applied Physics Letters*, 89(11):112123, 2006.

[97] Arun Suresh and J. F. Muth. Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors. *Applied Physics Letters*, 92(3):033502, 2008.

[98] J. B. Franklin, B. Zou, P. Petrov, D. W. McComb, M. P. Ryan, and M. A. McLachlan. Optimised pulsed laser deposition of ZnO thin films on transparent conducting substrates. *Journal of Materials Chemistry*, 21(22):8178–8182, 2011.

[99] Burhan Bayraktaroglu and Kevin Leedy. Pulsed laser deposited ZnO for thin film transistor applications. *ECS Transactions*, 16(12):61–73, 2008.

[100] Dalong Zhao, Devin A. Mourey, and Thomas N. Jackson. Fast flexible plastic substrate ZnO circuits. *IEEE Electron Device Letters*, 31(4):323–325, 2010.

[101] P. F. Carcia, R. S. McLean, and M. H. Reilly. High-performance ZnO thin-film transistors on gate dielectrics grown by atomic layer deposition. *Applied Physics Letters*, 88(12):123509, 2006.

[102] Kunigunde H. Cherenack, Niko S. Munzenrieder, and Gerhard Troster. Impact of mechanical bending on ZnO and IGZO thin-film transistors. *IEEE Electron Device Letters*, 31(11):1254–1256, 2010.

[103] Ying Liu, C. R. Gorla, S. Liang, N. Emanetoglu, Y. Lu, H. Shen, and M. Wraback. Ultraviolet detectors based on epitaxial ZnO films grown by MOCVD. *Journal of Electronic Materials*, 29(1):69–74, 2000.

[104] K. Remashan, Y. S. Choi, S. J. Park, and J. H. Jang. Enhanced performance of MOCVD ZnO TFTs on glass substrates with nitrogen-rich silicon nitride gate dielectric. *Journal of the Electrochemical Society*, 157(1):H60–H64, 2010.

[105] Si Joon Kim, Seokhyun Yoon, and Hyun Jae Kim. Review of solution-processed oxide thin-film transistors. *Japanese Journal of Applied Physics*, 53(2S):02BA02, 2014.

[106] Je-Hun Lee, Do-Hyun Kim, Dong-Ju Yang, Sun-Young Hong, Kap-Soo Yoon, Pil-Soon Hong, Chang-Oh Jeong, Hong-Sik Park, Shi Yul Kim, Soon Kwon Lim, and Sang Soo Kim. 42.2: World's largest (15-inch) XGA AMLCD panel using IGZO oxide TFT. In *SID Symposium Digest of Technical Papers*, volume 39, pages 625–628. Wiley Online Library, 2008.

[107] Jin-Seong Park, Jae Kyeong Jeong, Hyun-Joong Chung, Yeon-Gon Mo, and Hye Dong Kim. Electronic transport properties of amorphous indium-gallium-zinc oxide semiconductor upon exposure to water. *Applied Physics Letters*, 92(7):072104, 2008.

[108] Kwang-Hee Lee, Ji Sim Jung, Kyoung Seok Son, Joon Seok Park, Tae Sang Kim, Rino Choi, Jae Kyeong Jeong, Jang-Yeon Kwon, Bonwon Koo, and Sangyun Lee. The effect of moisture on the photon-enhanced negative bias thermal instability in Ga–In–Zn–O thin film transistors. *Applied Physics Letters*, 95(23):232106, 2009.

[109] K. Wetchakun, T. Samerjai, N. Tamaekong, C. Liewhiran, C. Siriwong, V. Kruefu, A. Wisitsoraat, A. Tuantranont, and S. Phanichphant. Semiconducting metal oxides as sensors for environmentally hazardous gases. *Sensors and Actuators B: Chemical*, 160(1):580–591, 2011.

[110] Jae-Heon Shin, Ji-Su Lee, Chi-Sun Hwang, Sang-Hee Ko Park, Woo-Seok Cheong, Minki Ryu, Chun-Won Byun, Jeong-Ik Lee, and Hye Yong Chu. Light effects on the bias stability of transparent ZnO thin film transistors. *ETRI Journal*, 31(1):62–64, 2009.

[111] Kazushige Takechi, Mitsuru Nakata, Toshimasa Eguchi, Hirotaka Yamaguchi, and Setsuo Kaneko. Comparison of ultraviolet photo-field effects between hydrogenated amorphous silicon and amorphous $InGaZnO_4$ thin-film transistors. *Japanese Journal of Applied Physics*, 48(1R):010203, 2009.

[112] Shinhyuk Yang, Kwang Hwan Ji, Un Ki Kim, Cheol Seong Hwang, Sang-Hee Ko Park, Chi-Sun Hwang, Jin Jang, and Jae Kyeong Jeong. Suppression in the negative bias illumination instability of Zn-Sn-O transistor using oxygen plasma treatment. *Applied Physics Letters*, 99(10):102103, 2011.

[113] Joon Seok Park, Tae Sang Kim, Kyoung Seok Son, Kwang-Hee Lee, Ji Sim Jung, Wan-Joo Maeng, Hyun-Suk Kim, Eok Su Kim, Kyung-Bae Park, Jong-Baek Seon, Jang-Yeon Kwon, Myung Kwan Ryu, and Sangyoon Lee. High-performance and stable transparent Hf–In–Zn–O thin-film transistors with a double-etch-stopper layer. *IEEE Electron Device Letters*, 31(11):1248–1250, 2010.

[114] Christopher R. Newman, C. Daniel Frisbie, Demetrio A. da Silva Filho, Jean-Luc Brédas, Paul C. Ewbank, and Kent R. Mann. Introduction to organic thin film transistors and design of n-channel organic semiconductors. *Chemistry of Materials*, 16(23):4436–4451, 2004.

[115] Frank Ortmann, Friedhelm Bechstedt, and Karsten Hannewald. Theory of charge transport in organic crystals: Beyond Holstein's small-polaron model. *Physical Review B*, 79(23):235206, 2009.

[116] Ajay A. Virkar, Stefan Mannsfeld, Zhenan Bao, and Natalie Stingelin. Organic semiconductor growth and morphology considerations for organic thin-film transistors. *Advanced Materials*, 22(34):3857–3875, 2010.

[117] Henning Sirringhaus. 25th anniversary article: Organic field-effect transistors: the path beyond amorphous silicon. *Advanced Materials*, 26(9):1319–1335, 2014.

[118] Daniel R. Gamota, Paul Brazis, Krishna Kalyanasundaram, and Jie Zhang. *Printed Organic and Molecular Electronics*. Springer Science & Business Media, 2013.

[119] Peter A. Bobbert, Abhinav Sharma, Simon G. J. Mathijssen, Martijn Kemerink, and Dago M. de Leeuw. Operational stability of organic field-effect transistors. *Advanced Materials*, 24(9):1146–1158, 2012.

[120] Jiye Kim, Jaeyoung Jang, Kyunghun Kim, Haekyoung Kim, Se Hyun Kim, and Chan Eon Park. The origin of excellent gate-bias stress stability in organic field-effect transistors employing fluorinated-polymer gate dielectrics. *Advanced Materials*, 26(42):7241–7246, 2014.

[121] B. Lee, A. Wan, D. Mastrogiovanni, J. E. Anthony, E. Garfunkel, and V. Podzorov. Origin of the bias stress instability in single-crystal organic field-effect transistors. *Physical Review B*, 82(8):085302, 2010.

[122] Vinay Gupta and Abhai Mansingh. Influence of postdeposition annealing on the structural and optical properties of sputtered zinc oxide film. *Journal of Applied Physics*, 80(2):1063–1073, 1996.

[123] P. F. Carcia, R. S. McLean, M. H. Reilly, and G. Nunes Jr. Transparent ZnO thin-film transistor fabricated by RF magnetron sputtering. *Applied Physics Letters*, 82(7):1117–1119, 2003.

[124] E. M. Bachari, G. Baud, S. Ben Amor, and M. Jacquet. Structural and optical properties of sputtered ZnO films. *Thin Solid Films*, 348(1):165–172, 1999.

[125] Tommi Tynell and Maarit Karppinen. Atomic layer deposition of ZnO: a review. *Semiconductor Science and Technology*, 29(4):043001, 2014.

[126] Zsfia Baji, Zoltn Lbadi, Zsolt E Horvth, Gyrgy Molnr, Jnos Volk, Istvn Brsony, and Pter Barna. Nucleation and growth modes of ALD ZnO. *Crystal Growth & Design*, 12(11):5615–5620, 2012.

[127] E. Guziewicz, M. Godlewski, L. Wachnicki, T. A. Krajewski, G. Luka, S. Gieraltowska, R. Jakiela, A. Stonert, W. Lisowski, M. Krawczyk, J. W. Sobczak, and A. Jablonski. ALD grown zinc oxide with controllable electrical properties. *Semiconductor Science and Technology*, 27(7):074011, 2012.

[128] M. D. Groner, F. H. Fabreguette, J. W. Elam, and S. M. George. Low-temperature Al_2O_3 atomic layer deposition. *Chemistry of Materials*, 16(4):639–645, 2004.

[129] Ville Miikkulainen, Markku Leskelä, Mikko Ritala, and Riikka L Puurunen. Crystallinity of inorganic films grown by atomic layer deposition: Overview and general trends. *Journal of Applied Physics*, 113(2):2, 2013.

[130] Devin A Mourey. *Plasma-Enhanced Atomic Layer Deposition ZnO For Multifunctional Thin Film Electronics*. The Pennsylvania State University, 2010.

[131] V. A. Lisovskiy and V. D. Yegorenkov. RF breakdown of low-pressure gas and a novel method for determination of electron-drift velocities in gases. *Journal of Physics D: Applied Physics*, 31(23):3349, 1998.

[132] Jose Israel Ramirez. *ZnO Thin Film Electronics for More than Displays*. The Pennsylvania State University, 2015.

[133] John Bacsa, Felix Hanke, Sarah Hindley, Rajesh Odedra, George R. Darling, Anthony C. Jones, and Alexander Steiner. The solid-state structures of dimethylzinc and diethylzinc. *Angewandte Chemie International Edition*, 50(49):11685–11687, 2011.

[134] G. Sean McGrady, John F. C. Turner, Richard M. Ibberson, and Michael Prager. Structure of the trimethylaluminum dimer as determined by powder neutron diffraction at low temperature. *Organometallics*, 19(21):4398–4401, 2000.

[135] Y. Afsar, W. Rieutort-Louis, N. Verma, J. C. Sturm, and S. Wagner. Self-aligned and in-situ passivated ZnO TFTs. In *International Thin Film Transistor Conference*, Delft, Netherlands, Jan. 2014.

[136] Y. Afsar, S. Avasthi, N. Verma, J. C. Sturm, and S. Wagner. Apparent super-linear behavior of cutoff frequency in PEALD ZnO TFTs. In *International Thin Film Transistor Conference*, Rennes, France, Feb. 2015.

[137] Yasmin Afsar, Jenny Tang, Warren Rieutort-Louis, Liechao Huang, Yingzhe Hu, Josue Sanz-Robinson, Sigurd Wagner, Naveen Verma, and James C. Sturm. 18-2: Oxide TFT LC oscillators on glass and plastic for wireless functions in large-area flexible electronic systems. In *SID Symposium Digest of Technical Papers*, volume 47, pages 207–210. Wiley Online Library, 2016.

[138] M. D. Groner, J. W. Elam, F. H. Fabreguette, and Sm. M. George. Electrical characterization of thin Al_2O_3 films grown by atomic layer deposition on silicon and various metal substrates. *Thin Solid Films*, 413(1):186–197, 2002.

[139] N. Y. Yuan, S. Y. Wang, C. B. Tan, X. Q. Wang, G. G. Chen, and J. N. Ding. The influence of deposition temperature on growth mode, optical and mechanical properties of ZnO films prepared by the ALD method. *Journal of Crystal Growth*, 366:43–46, 2013.

[140] A. Illiberi, F. Roozeboom, and P. Poodt. Spatial atomic layer deposition of zinc oxide thin films. *ACS Applied Materials & Interfaces*, 4(1):268–272, 2011.

[141] Naomi Nandakumar, Bas Dielissen, Diana Garcia-Alonso, Zhe Liu, W. M. Kessels, Roger Gortzen, Armin G. Aberle, and Bram Hoex. Spatial atomic layer deposition of intrinsic zinc oxide films for applications in the photovoltaic industry. In *Proc. 6th WCPEC Conf.*, pages 577–578, 2014.

[142] E. Guziewicz, I. A. Kowalik, M. Godlewski, K. Kopalko, V. Osinniy, A. Wójcik, S. Yatsunenko, E. Łusakowska, W. Paszkowicz, and M. Guziewicz. Extremely low temperature growth of ZnO by atomic layer deposition. *Journal of Applied Physics*, 103(3):033515, 2008.

[143] Shelby F. Nelson, David H. Levy, Lee W. Tutt, and Mitchell Burberry. Cycle time effects on growth and transistor characteristics of spatial atomic layer deposition of zinc oxide. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, 30(1):01A154, 2012.

[144] Tommi O. Kääriäinen and David C. Cameron. Plasma-assisted atomic layer deposition of Al_2O_3 at room temperature. *Plasma Processes and Polymers*, 6(S1), 2009.

[145] D. R. G. Mitchell, G. Triani, D. J. Attard, K. S. Finnie, P. J. Evans, C. J. Barbé, and J. R. Bartlett. Atomic layer deposition of TiO_2 and Al_2O_3 thin films and nanolaminates. *Smart Materials and Structures*, 15(1):S57, 2005.

[146] Zs. Baji, Z. Lábadi, Zs. E. Horváth, M. Fried, B. Szentpáli, and I. Bársony. Temperature dependent in situ doping of ALD ZnO. *Journal of Thermal Analysis and Calorimetry*, 105(1):93–99, 2011.

[147] F. K. Shan, G. X. Liu, W. J. Lee, G. H. Lee, I. S. Kim, and B. C. Shin. Structural, electrical, and optical properties of transparent gallium oxide thin films grown by plasma-enhanced atomic layer deposition. *Journal of Applied Physics*, 98(2):023504, 2005.

[148] Chang-Wook Jeong, Jang-Sik Lee, and Seung-Ki Joo. Plasma-assisted atomic layer growth of high-quality aluminum oxide thin films. *Japanese Journal of Applied Physics*, 40(1R):285, 2001.

[149] Burhan Bayraktaroglu, Kevin Leedy, and Robert Neidhard. Microwave ZnO thin-film transistors. *IEEE Electron Device Letters*, 29(9):1024–1026, 2008.

[150] D. L. Raimondi and E. Kay. High resistivity transparent ZnO thin films. *Journal of Vacuum Science and Technology*, 7(1):96–99, 1970.

[151] Triratna Muneshwar, Gem Shoute, Doug Barlage, and Ken Cadien. Plasma enhanced atomic layer deposition of ZnO with diethyl zinc and oxygen plasma: Effect of precursor decomposition. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, 34(5):050605, 2016.

[152] D.-G. Yoo, S.-H. Nam, M. H. Kim, S. H. Jeong, H.-G. Jee, H. J. Lee, N.-E. Lee, B. Y. Hong, Y. J. Kim, D. Jung, and J.-H. Boo. Fabrication of the ZnO thin films using wet-chemical etching processes on application for organic light emitting diode (OLED) devices. *Surface and Coatings Technology*, 202(22):5476–5479, 2008.

[153] Yuchao Wang, Tianzhun Wu, Mingming Chen, Longxing Su, Quanlin Zhang, Lifang Yuan, Yuan Zhu, and Zikang Tang. Well-controlled wet etching of ZnO films using hydrogen peroxide solution. *Applied Surface Science*, 292:34–38, 2014.

[154] Shih-Chia Chang, D. B. Hicks, and R. C. O. Laugal. Patterning of zinc oxide thin films. In *Solid-State Sensor and Actuator Workshop, 1992. 5th Technical Digest., IEEE*, pages 41–45. IEEE, 1992.

[155] Jie Sun, Devin A. Mourey, Dalong Zhao, Sung Kyu Park, Shelby F. Nelson, David H. Levy, Diane Freeman, Peter Cowdery-Corvan, Lee Tutt, and Thomas N. Jackson. ZnO thin-film transistor ring oscillators with 31-ns propagation delay. *IEEE Electron Device Letters*, 29(7):721–723, 2008.

[156] S. de Gendt. *Atomic Layer Deposition Applications 5*. Number 4 in Dielectric and Semiconductor Materials, Devices and Processing. Electrochemical Society, 2009.

[157] Kaige G. Sun, Yuanyuan V. Li, David B. Saint John, and Thomas N. Jackson. pH-controlled selective etching of Al_2O_3 over ZnO. *ACS Applied Materials & Interfaces*, 6(10):7028–7031, 2014.

[158] Peter V. Necliudov, Michael S. Shur, David J. Gundlach, and Thomas N. Jackson. Contact resistance extraction in pentacene thin film transistors. *Solid-State Electronics*, 47(2):259–262, 2003.

[159] Yuanyuan V. Li, Jose Israel Ramirez, Kaige G. Sun, and Thomas N. Jackson. Low-voltage double-gate ZnO thin-film transistor circuits. *IEEE Electron Device Letters*, 34(7):891–893, 2013.

[160] Yasuhiro Shimura, Kenji Nomura, Hiroshi Yanagi, Toshio Kamiya, Masahiro Hirano, and Hideo Hosono. Specific contact resistances between amorphous oxide semiconductor In–Ga–Zn–O and metallic electrodes. *Thin Solid Films*, 516(17):5899–5902, 2008.

[161] Woong-Sun Kim, Yeon-Keon Moon, Kyung-Taek Kim, Je-Hun Lee, Byung-du Ahn, and Jong-Wan Park. An investigation of contact resistance between metal electrodes and amorphous gallium–indium–zinc oxide (a-GIZO) thin-film transistors. *Thin Solid Films*, 518(22):6357–6360, 2010.

[162] Jin-Seong Park, Jae Kyeong Jeong, Yeon-Gon Mo, Hye Dong Kim, and Sun-Il Kim. Improvements in the device characteristics of amorphous indium gallium zinc oxide thin-film transistors by Ar plasma treatment. *Applied Physics Letters*, 90(26):262106, 2007.

[163] Sang-Hee Ko Park, Chi-Sun Hwang, Hu Young Jeong, Hye Yong Chu, and Kyoung Ik Cho. Transparent ZnO-TFT arrays fabricated by atomic layer deposition. *Electrochemical and Solid-State Letters*, 11(1):H10–H14, 2008.

[164] Devin A Mourey, Dalong A Zhao, Ho Him R Fok, Yuanyuan V Li, and Thomas N Jackson. Thermal effects in oxide TFTs. In *Device Research Conference (DRC), 2010*, pages 243–244. IEEE, 2010.

[165] A. R. Hutson. Hall effect studies of doped zinc oxide single crystals. *Physical Review*, 108(2):222, 1957.

[166] David C. Look, Donald C. Reynolds, J. R. Sizelove, R. L. Jones, Cole W. Litton, G. Cantwell, and W. C. Harsch. Electrical properties of bulk ZnO. *Solid State Communications*, 105(6):399–401, 1998.

[167] S. A. Studenikin, Nickolay Golego, and Michael Cocivera. Carrier mobility and density contributions to photoconductivity transients in polycrystalline ZnO films. *Journal of Applied Physics*, 87(5):2413–2421, 2000.

[168] H. Paul Maruska, Amal K. Ghosh, Albert Rose, and Tom Feng. Hall mobility of polycrystalline silicon. *Applied Physics Letters*, 36(5):381–383, 1980.

[169] Kazushige Takechi, Mitsuru Nakata, Toshimasa Eguchi, Hirotaka Yamaguchi, and Setsuo Kaneko. Temperature-dependent transfer characteristics of amorphous $InGaZnO_4$ thin-film transistors. *Japanese Journal of Applied Physics*, 48(1R):011301, 2009.

[170] Shunpei Yamazaki and Tetsuo Tsutsui. *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to Displays*. John Wiley & Sons, 2017.

[171] P. G. Le Comber and W. E. Spear. Electronic transport in amorphous silicon films. *Physical Review Letters*, 25(8):509, 1970.

[172] Arokia Nathan, Sungsik Lee, Sanghun Jeon, Ihun Song, and U-In Chung. 3.1: Invited paper: Amorphous oxide TFTs: Progress and issues. In *SID Symposium Digest of Technical Papers*, volume 43, pages 1–4. Wiley Online Library, 2012.

[173] Yasmin Afsar, John Sarik, Maria Gorlatova, Gil Zussman, and Ioannis Kymissis. Evaluating photovoltaic performance indoors. In *Photovoltaic Specialists Conference (PVSC), 2012 38th IEEE*, pages 001948–001951. IEEE, 2012.

[174] Devin A. Mourey, Mitchell S. Burberry, Dalong A. Zhao, Yuanyuan V. Li, Shelby F. Nelson, Lee Tutt, Thomas D. Pawlik, David H. Levy, and Thomas N. Jackson. Passivation of ZnO TFTs. *Journal of the Society for Information Display*, 18(10):753–761, 2010.

[175] Y. V. Li, K. G. Sun, J. I. Ramirez, and T. N. Jackson. Trilayer ZnO thin-film transistors with *in situ* Al_2O_3 passivation. *IEEE Electron Device Lett.*, 34(11):1400–1402, Nov. 2013.

[176] Devin A. Mourey, Dalong A. Zhao, and Thomas N. Jackson. Self-aligned-gate ZnO TFT circuits. *IEEE Electron Device Letters*, 31(4):326–328, 2010.

[177] I-Chun Cheng, Alex Z. Kattamis, Ke Long, James C. Sturm, and Sigurd Wagner. Self-aligned amorphous-silicon TFTs on clear plastic substrates. *IEEE Electron Device Letters*, 27(3):166–168, 2006.

[178] Christine G. Pappas. Towards a 100 000 TES focal plane array: A robust, high-density, superconducting cable interface. *IEEE Transactions on Applied Superconductivity*, 25(3):1–5, 2015.

[179] Sigurd Wagner, Helena Gleskova, I-Chun Cheng, James C. Sturm, and Z. Suo. Mechanics of TFT technology on flexible substrates. *Flexible Flat Panel Displays*, 14:263–283, 2005.

[180] Haoyu U. Li and Thomas N. Jackson. Oxide semiconductor thin film transistors on thin solution-cast flexible substrates. *IEEE Electron Device Letters*, 36(1):35–37, 2015.

[181] Y. Afsar, W. Rieutort-Louis, L. Huang, Y. Hu, J. Sanz-Robinson, N. Verma, J.C. Sturm, and S. Wagner. f_{MAX} and f_t measurements of PEALD ZnO TFTs for high-frequency oscillators. In *Materials Research Society Meeting*, Boston, MA, Nov. 2014.

[182] Y. Afsar, W. Rieutort-Louis, L. Huang, Y. Hu, J. Sanz-Robinson, N. Verma, J.C. Sturm, and S. Wagner. 10-MHz cross-coupled LC oscillators based on plasma-enhanced ALD ZnO thin-film transistors. In *Materials Research Society Meeting*, San Francisco, CA, April 2015.

[183] Y. Afsar, T. Moy, N. Verma, J. C. Sturm, and S. Wagner. Plasma-enhanced atomic layer deposition of zinc oxide transistors for large-area applications. In *International Workshop on Zinc Oxide and Related Materials*, Niagara Falls, Canada, Sep. 2014.

[184] Y. Afsar, W. Rieutort-Louis, N. Verma, S. Wagner, and J. C. Sturm. ZnO versus a-Si thin-film oscillator circuits for hybrid integration: metrics for design and comparison. In *15th Annual Flexible and Printed Electronics Conference (FLEX2016)*, Monterey, CA, Mar. 2016.

[185] JinFang Huang. Derivation of f_t and f_{MAX} of a MOSFET. University Lecture, 2004.

[186] Level 61 a-Si TFT Model. `http://helpme.scudc.scu.edu/hspice2001/hspice_and_qrg/hspice_2001_2-179.html`. Accessed: 2016-10-15.

[187] Tiffany Moy, Warren Rieutort-Louis, Yingzhe Hu, Liechao Huang, Josue Sanz-Robinson, James C Sturm, Sigurd Wagner, and Naveen Verma. Thin-film circuits for scalable interfacing between large-area electronics and CMOS ICs. In *Device Research Conference (DRC), 2014 72nd Annual*, pages 271–272. IEEE, 2014.

[188] Y. Mehlman, Y. Afsar, T. Moy, S. Wagner, J. C. Sturm, and N. Verma. High-speed scanning circuit based on metal-oxide thin-film-transistors for reduction of large-area to CMOS-IC interconnections. In *International Thin Film Transistor Conference*, Austin, TX, Jan. 2017.

[189] Yingzhe Hu, Warren S. A. Rieutort-Louis, Josue Sanz-Robinson, Liechao Huang, Branko Glišic, James C. Sturm, Sigurd Wagner, and Naveen Verma. Large-scale sensing system combining large-area electronics and CMOS ICs for structural-health monitoring. *IEEE Journal of Solid-State Circuits*, 49(2):513–523, 2014.

[190] Warren Rieutort-Louis, Liechao Huang, Yingzhe Hu, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, and Naveen Verma. A complete fully thin-film PV harvesting and power-management system on plastic with on-sheet battery management and wireless power delivery to off-sheet loads. *IEEE Journal of Photovoltaics*, 4(1):432–439, 2014.

[191] Liechao Huang, Warren Rieutort-Louis, Yingzhe Hu, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, and Naveen Verma. A super-regenerative radio on plastic based on thin-film transistors and antennas on large flexible sheets for distributed communication links. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, pages 458–459. IEEE, 2013.

[192] Anand Subramaniam, Kurtis D. Cantley, and Eric M. Vogel. Logic gates and ring oscillators based on ambipolar nanocrystalline-silicon TFTs. *Active and Passive Electronic Components*, vol. 2013, 2013.

[193] Kris Myny, Soeren Steudel, Steve Smout, Peter Vicca, Francois Furthner, Bas van der Putten, Ashutosh K. Tripathi, Gerwin H. Gelinck, Jan Genoe, Wim Dehaene, and P. Heremans. Organic RFID transponder chip with data rate compatible with electronic product coding. *Organic Electronics*, 11(7):1176–1179, 2010.

[194] Frederik Ante, Daniel Kälblein, Tarek Zaki, Ute Zschieschang, Kazuo Takimiya, Masaaki Ikeda, Tsuyoshi Sekitani, Takao Someya, Joachim N. Burghartz, Klaus Kern, and Hagen Klauk. Contact resistance and megahertz operation of aggressively scaled organic transistors. *Small*, 8(1):73–79, 2012.

[195] P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, and S. D. Theiss. Pentacene-based radio-frequency identification circuitry. *Applied Physics Letters*, 82(22):3964–3966, 2003.

[196] Dong Han Kang, In Kang, Sang Hyun Ryu, and Jin Jang. Self-aligned coplanar a-IGZO TFTs and application to high-speed circuits. *IEEE Electron Device Letters*, 32(10):1385–1387, 2011.

[197] Yuanfeng Chen, Di Geng, Mallory Mativenga, Hyoungsik Nam, and Jin Jang. High-speed pseudo-CMOS circuits using bulk accumulation a-IGZO TFTs. *IEEE Electron Device Letters*, 36(2):153–155, 2015.

[198] Minhun Jung, Jaeyoung Kim, Jinsoo Noh, Namsoo Lim, Chaemin Lim, Gwangyong Lee, Junseok Kim, Hwiwon Kang, Kyunghwan Jung, Ashley D. Leonard, James M. Tour, and Gyoujin Cho. All-printed and roll-to-roll-printable 13.56-MHz-operated 1-bit RF tag on plastic foils. *IEEE Transactions on Electron Devices*, 57(3):571–580, 2010.

[199] Michael G. Kane, Lawrence Goodman, Arthur H. Firester, Paul C. Wilt, Alexander B. Limanov, and James S. Im. 100-MHz CMOS circuits directly fabricated on plastic using sequential laterally solidified silicon. *Journal of the Society for Information Display*, 15(7):471–478, 2007.

[200] Daniel Schall, Martin Otto, Daniel Neumaier, and Heinrich Kurz. Integrated ring oscillators based on high-performance graphene inverters. *Scientific Reports*, 3, 2013.

[201] Matias Troccoli, Themis Afentakis, Ta-Ko Chuang, Abbas Jamshidi, Yu-Lin Chang, Miltiadis K Hatalis, Apostolos T. Voutsas, Masahiro Adachi, and John W. Hartzell. High performance TFT circuits for all-integrated systems on stainless steel foils. In *Thin Film Transistor Technologies (TFTT VII): Proceedings of the International Symposium*, volume 2004, page 166. The Electrochemical Society, 2005.

[202] R. L. Weisfield, M. A. Hartney, R. A. Street, and R. B. Apte. New amorphous-silicon image sensor for X-ray diagnostic medical imaging applications. In *Proc. SPIE 3336*, page 444, Feb. 1998.

[203] Y.Afsar, T. Moy, N. Brady, S. Wagner, J. C. Sturm, and N. Verma. Large-scale acquisition of large-area sensors using an array of frequency-hopping ZnO thin-film-transistor oscillators. In *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pages 256–257, Feb. 2017.

[204] Y.Afsar, T. Moy, N. Brady, S. Wagner, J. C. Sturm, and N. Verma. An architecture for large-area sensor acquisition using frequency-hopping ZnO TFT DCOs. *IEEE Journal of Solid-State Circuits*, 53(1):1–12, Jan. 2018.

[205] Y. Mehlman, Y. Afsar, N. Verma, S. Wagner, and J.C. Sturm. Self-aligned ZnO thin-film transistors with 860 MHz f_T and 2 GHz f_{MAX} for large-area applications. In *Device Research Conference Dig. Tech. Papers*, pages 0–1, Jun. 2017.

[206] B. Razavi. A study of injection locking and pulling in oscillators. *IEEE Journal of Solid-State Circuits*, 39(9):1415–1424, Sept 2004.

[207] Interlink Electronics Force-Sensing Resistor. `http://www.interlinkelectronics.com/`. Accessed: 2016-06-30.

[208] John L Lyons, Anderson Janotti, and Chris G Van de Walle. Why nitrogen cannot lead to p-type conductivity in ZnO. *Applied Physics Letters*, 95(25):252105, 2009.

Appendix C

List of Publications Resulting from this Thesis

C.1 Publications

Y. Afsar, T. Moy, N. Brady, S. Wagner, J. C. Sturm, and N. Verma, "An Architecture for Large-Area Sensor Acquisition Using Frequency-Hopping ZnO TFT DCOs." IEEE Journal of Solid State Circuits, Vol. 53, issue 1, Jan. 2018. (INVITED, Special Issue).

Y. Afsar, J. Tang, W. Rieutort-Louis, L. Huang, Y. Hu, J. Sanz-Robinson, N. Verma, S. Wagner, and J.C. Sturm, "Impact of Bending of Flexible Metal Oxide TFTs and Oscillator Circuits," Journal of the Society for Information Display, Vol. 24, issue 6, pp. 371-380, May 2016. (INVITED, Special Issue: Best of Display Week).

W. Rieutort-Louis, J. Sanz-Robinson, T. Moy, L. Huang, Y. Hu, Y. Afsar, J. C. Sturm, N. Verma, S. Wagner, "Integrating and Interfacing Flexible Electronics in Hybrid Large-Area Systems," IEEE Trans. Components, Packaging and Manufacturing Technology (TCPMT), vol. 5, no. 9, pp. 1219-1229, Sept. 2015. (Invited).

S. Wagner, J. Sanz-Robinson, W. Rieutort-Louis, L. Huang, T. Moy, Y. Hu, Y. Afsar, J. C. Sturm, N. Verma, "Investigating the Architecture of Flexible Large-Area Hybrid Systems," Information Display, Vol. 31, No. 4, July/Aug 2015.

C.2 Conferences

Y. Afsar, T. Moy, N. Brady, S. Wagner, J. C. Sturm, and N. Verma, "Large-Scale Acquisition of Large-Area Sensors Using an Array of Frequency-Hopping ZnO Thin-Film-Transistor Oscillators," IEEE International Solid-State Circuits Conference, February 2017, San Francisco, CA.

Y. Afsar, J. Tang, W. Rieutort-Louis, L. Huang, Y. Hu, J. Sanz-Robinson, N. Verma, S. Wagner, and J.C. Sturm, "Oxide-TFT LC Oscillators on Glass and Plastic for Wireless Functions in Large-Area Flexible Electronic Systems," Society for Information Display 2016 Symposium, May 2016, San Jose, CA. (Outstanding Paper Nomination).

Y. Afsar, W. Rieutort-Louis, N. Verma, S. Wagner, J. C. Sturm, "ZnO versus a-Si thin-film oscillator circuits for hybrid integration: metrics for design and comparison," 15th Annual Flexible and Printed Electronics Conference (FLEX2016), March 2016, Monterey, CA. (First Place Student Poster).

Y. Afsar, W. Rieutort-Louis, L. Huang, Y. Hu, J. Sanz-Robinson, N. Verma, J.C. Sturm, and S. Wagner, "10-MHz cross-coupled LC oscillators based on plasma-enhanced ALD ZnO thin-film transistors," Materials Research Society Meeting, April 2015, San Francisco, CA.

Y. Afsar, W. Rieutort-Louis, N. Verma, J. C. Sturm, and S. Wagner, "Apparent super-linear behavior of cutoff frequency in PEALD ZnO TFTs," International Thin-Film Transistor Conference, February 2015, Rennes, France.

Y. Afsar, W. Rieutort-Louis, N. Verma, J. C. Sturm, and S. Wagner, "f_{MAX} and f_T measurements of PEALD ZnO TFTs for high-frequency oscillators," Materials Research Society Meeting, November 2014, Boston MA.

Y. Afsar, T. Moy, N. Verma, J. C. Sturm, S. Wagner, "Plasma-Enhanced Atomic Layer Deposition Zinc Oxide Thin-Film Transistor-Based Scanning Circuits," International Workshop on Zinc Oxide and Related Materials, September 2014, Niagara Falls, Canada.

Y. Afsar, S. Avasthi, J. C. Sturm, N. Verma, and S. Wagner, "Self-aligned and in-situ passivated ZnO TFTs," International Thin-Film Transistor Conference, January 2014, Delft, Netherlands.

Y. Mehlman, Y. Afsar, N. Verma, J. C. Sturm, "Self-Aligned ZnO Thin-Film Transistors with 860 MHz f_T and 2 GHz f_{MAX} for Large-Area Applications," Device Research Conference, June 2017, Notre Dame, Indiana.

Y. Mehlman, Y. Afsar, T. Moy, S. Wagner, J. C. Sturm, N. Verma, "High-Speed Scanning Circuit Based on Metal-Oxide Thin-Film-Transistors for Reduction of Large-Area to CMOS IC Connections," International Thin-Film Transistor Conference, February 2017, Austin, TX.

N. Verma, Y. Afsar, L. Huang, Y. Hu, T. Moy, W. Rieutort-Louis, J. Sanz-Robinson, S. Wagner, J. C. Sturm, "Creating a Thin-Film Electronics Roadmap for Flexible-Hybrid Systems," 15th Annual Flexible and Printed Electronics Conference (FLEX2016), March 2016, Monterey, CA.

L. Aygun, Y. Afsar, N. Verma, S. Wagner, J. C. Sturm, "High-Frequency ZnO Schottky Diodes for Inductive Non-Contact Interfaces for Hybrid Flexible Electronics/IC Integration," 15th Annual Flexible and Printed Electronics Conference (FLEX2016), March 2016, Monterey, CA.

W. Rieutort-Louis, Y. Afsar, J. C. Sturm, N. Verma, S. Wagner, "Representative Flicker Noise Measurements for Low-Temperature Amorphous Silicon, Organic, and Zinc Oxide Thin-Film Transistors," International Thin-Film Transistor Conference, February 2015, Rennes, France.

S. Wagner, T. Moy, J. Sanz-Robinson, W. Rieutort-Louis, Y. Afsar, Y. Hu, L. Huang, J. C. Sturm, N. Verma, "Thin-Film Technology for Large-Area / CMOS Hybrid Systems," PRIME: Pacific Rim Meeting on Electrochemical and Solid-State Science, October 2016, Honolulu, HI.

L.E. Aygun, N. Verma, Y. Afsar, Y. Hu, L. Huang, T. Moy, J. Sanz-Robinson, W. Rieutort-Louis, S. Wagner, J.C. Sturm, "Hybrid Large-Area Systems and Their Interconnection Backbone," International Symposium on Networks-on-Chip (NOCS), September 2016, Nara, Japan.

J. C. Sturm, J. Sanz-Robinson, H. Jia, W. Rieutort-Louis, Y. Hu, L. Huang, Y. Afsar, T. Moy, "A Natural Human-Machine Interface via a Flexible Hybrid Sheet for Remote Gesture Sensing and Speaker Isolation," 15th Annual Flexible and Printed Electronics Conference (FLEX2016), March 2016, Monterey, CA.

S. Wagner, T. Moy, J. Sanz-Robinson, W. Rieutort-Louis, Y. Afsar, Y. Hu, L. Huang, J. C. Sturm, N. Verma, "Thin-Film Devices for Large-Area / CMOS Hybrid Systems," International Thin Film Transistor Conference, February 2016, Hsinchu, Taiwan.

W. Rieutort-Louis, L. Huang, Y. Hu, J.Sanz Robinson, Y. Afsar, J. C. Sturm, N. Verma, and S. Wagner, "Characterization of Amorphous Silicon Thin-Film Transistor Cutoff Frequency," Device Research Conference, June 2014, Santa Barbara, CA.

S. Avasthi, W. McClain, Y. Afsar, G. Man, J. Jhaveri, K. Nagamatsu, A. Kahn, J. Schwarz, S. Wagner, J. C. Sturm, "Hole-Blocking Metal-Oxide/Crystalline-Silicon Heterojunctions with Recombination Velocity of < 100 cm/s," Materials Research Society Meeting, April 2014, San Francisco, CA.