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Stable Low-Recombination n-Si/TiO_2 Hole-blocking Interface and Its Effect on Silicon Heterojunction Photovoltaics

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***Abstract* — TiO_2 deposited on (100) crystalline silicon at near room temperature results in a hole-blocking, electron-transparent heterojunction. In this paper, we show that this interface can have a minority carrier recombination velocity on the order of 100 cm/s, which is stable for over 5 months in air. Second, we model the effect of such interfaces to replace the diffused n^+/n (back surface field) layer at the cathode of p^+/n and double heterojunction crystalline silicon solar cells. Simulations show that using TiO_2/n-Si with the measured values of interface recombination velocity as a replacement for the n^+/n diffusion at the cathode contact would yield power conversion efficiencies greater than 23%.**

***Index Terms* — titanium oxide, heterojunction, photovoltaic cells, silicon,**

I. Introduction

Recently, titanium dioxide (TiO_2) deposited on crystalline (100) silicon has been shown to form a hole-blocking, electron-transparent interface [1]. This is due to the small conduction band offset (ΔEc), which allows electrons to pass through the TiO_2 and the large valence band offset (ΔE_V), which results in holes being blocked (Fig. 1) [2]. In this paper, we examine the TiO_2/n-Si interface, specifically focusing on the recombination of minority carriers at the interface, with a goal of using the interface to replace the conventional n^+/n backside diffusion in silicon photovoltaics [3]. We first examine the stability of annealed TiO_2/n-Si in terms of s, the interface recombination velocity. Second, we model the effect of s on the power conversion efficiency for both conventional p^+/n-silicon solar cells and double heterojunction crystalline silicon solar cells without a p-n junction.

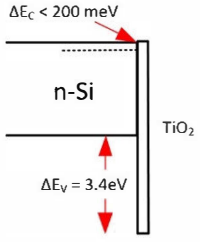

Fig. 1. Conduction and valence band offsets of n-Si/TiO_2 interface

II. Interface Quality

Metal in direct contact with n-type Si serves as a recombination site for minority carriers (holes). Holes in principle could be blocked from this metal contact by an n-Si/TiO_2 interface (Fig. 1). However defects at the n-Si/TiO2 interface can themselves facilitate recombination of minority carriers, which can negate the hole-blocking properties of the n-Si/TiO_2 interface. The recombination rate (R_{int}) is given by:

$$R_{\text{int}} = p_s \cdot s \tag{1}$$

where p_s is the surface minority carrier density assuming no band bending. The interface recombination velocity (cm/s) is represented by s. The recombination velocity is directly proportional to the number of interface defects as shown by (2).

$$s = N_{it} v_{th} \sigma_p \tag{2}$$

N_{it} is the interface defect density, v_{th} is the thermal velocity of holes and σ_p is the capture cross section for holes.

III. Experimental Details

The interface recombination velocity can be calculated by measuring the effective lifetime as given by the following equations.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{s_{front}}{W} + \frac{s_{back}}{W} \tag{3}$$

where τ_{eff} is the actual measured effective lifetime of the minority carriers, τ_{bulk} is the lifetime associated with the bulk, s_{front} and s_{back} are the recombination velocities associated with the front and back interfaces. W is the width of the substrate. (3) is only valid if the minority carrier diffusion length is much longer than the substrate width.

Lifetimes were measured using the Quasi-steady State Photoconductance Decay (QSSPCD) [4] with 300-μm thick $2x10^{15}/cm^3$ n-type Silicon FZ wafers, with bulk lifetimes larger than 1 ms. First, a high-quality thermal oxide was grown on both Si wafer surfaces at 1050 °C to passivate the surface. From the measured effective lifetime, a worst-case value (assuming an infinite τ_{bulk} and no Auger recombination at low excitation densities) of s of 20 cm/s was extracted for

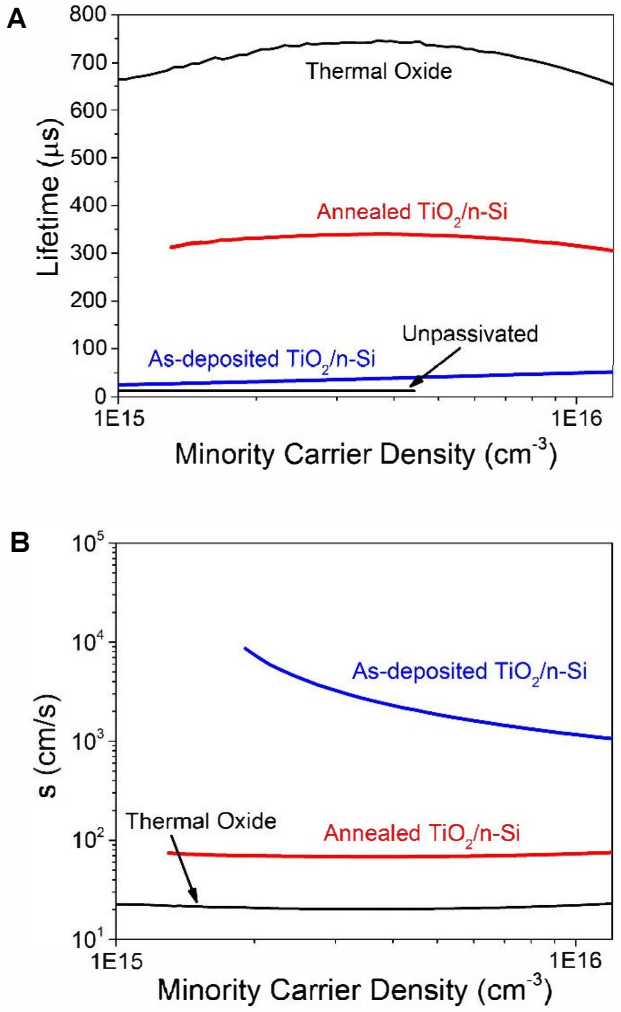

Fig. 2. (A) Lifetime versus minority carrier density (B) recombination velocity versus minority carrier density

both top and bottom Si/SiO_2 interfaces at an excess minority carrier density of $5x10^{15}$ cm^{-3}. Then the oxide on the top was etched off and a native oxide was allowed to grow on the top surface. The effective lifetime was measured again. As expected from the high number of interface defects on the top surface, a low effective lifetime of 10 µs was measured. Next, TiO_2 was deposited at room temperature and the lifetime was measured once more. The effective lifetime improved to 40 µs. Assuming the bulk lifetime and the back side Si/SiO_2 interface did not change, an s of 1900 cm/s was extracted for the as-deposited Si/TiO_2 interface.

It has been demonstrated that annealing at low temperatures (below 400°C) in N_2 ambient can improve the passivation at the n-Si/TiO2 interface [5-6]. After annealing at 250°C for 2 minutes, the effective lifetime increased to 340 µs at a minority carrier density of $5x10^{15}$ cm^{-3} (Fig. 2), which corresponds to an s value of 70 cm/ for n-Si/TiO_2.

For practical applications, stability of the interface is critical. Therefore, we exposed samples to air at room temperature. The interface recombination velocity increased to ~ 200 cm/s after a few days and remained near this value for 150 days (Fig. 3). Assuming $\sigma_p \sim 10^{-16}$ cm^2, an s of 200 cm/s implies a defect density of ~ $2x10^{11}$ cm^{-2}, i.e. only 1 in 10,000 Si atoms is unpassivated. For reference, the best thermal SiO_2 passivated surfaces have a defect density of ~10^{10} cm^{-2}.

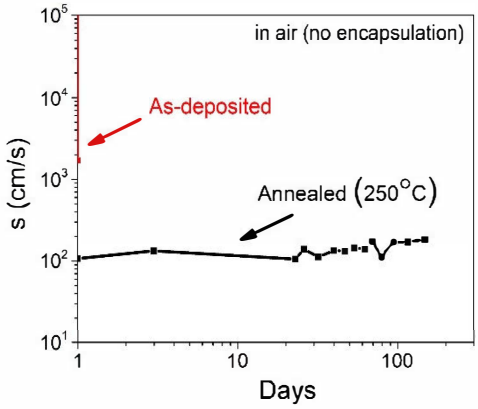

Fig. 3. Recombination velocity versus time at $5x10^{15}$ cm^{-3} minority carrier density

IV. Device Application Modelling

In high-quality p^+/n junctions, dark current and thus V_{OC} are controlled by the hole current from p^+-Si to the back side n-Si/metal contact. The standard practice is to perform a backside n^+ diffusion to create a barrier for holes and reduce dark current (Fig. 4A). Alternatively, to avoid high-temperature diffusion, one could replace the n^+/n diffusion by a thin TiO_2 layer between the n-type Si and the back side metal contact (Fig. 4B). As mentioned earlier, the large valence band offset would block holes from reaching the contact, while the small conduction band offset would allow photocurrent electrons to travel from the silicon, through the TiO_2 to the cathode. However, as also pointed out earlier, in order to successfully replace the backside diffusion, the recombination velocity at the n-Si/TiO_2 interface is important.

We also note that recent work has shown that a p^+/n junction can be replaced for PV purposes by an electron-blocking layer (EBL) heterojunction directly on n-type silicon, such as the organic semiconductor PEDOT on n-Si (Fig. 4C) [6]. In this structure, dark current is again dominated by minority carriers injected into n-type silicon, just as in the p^+/n junction. In both structures, in low-level injection, hole density in the n-type silicon scales as $1/N_D\, e^{qV/kT}$. Thus the effect of s at the n-Si/TiO_2 back interface for both p^+ Si/n-Si/TiO_2/cathode and the EBL/n-Si/TiO_2/cathode structures should be the same.

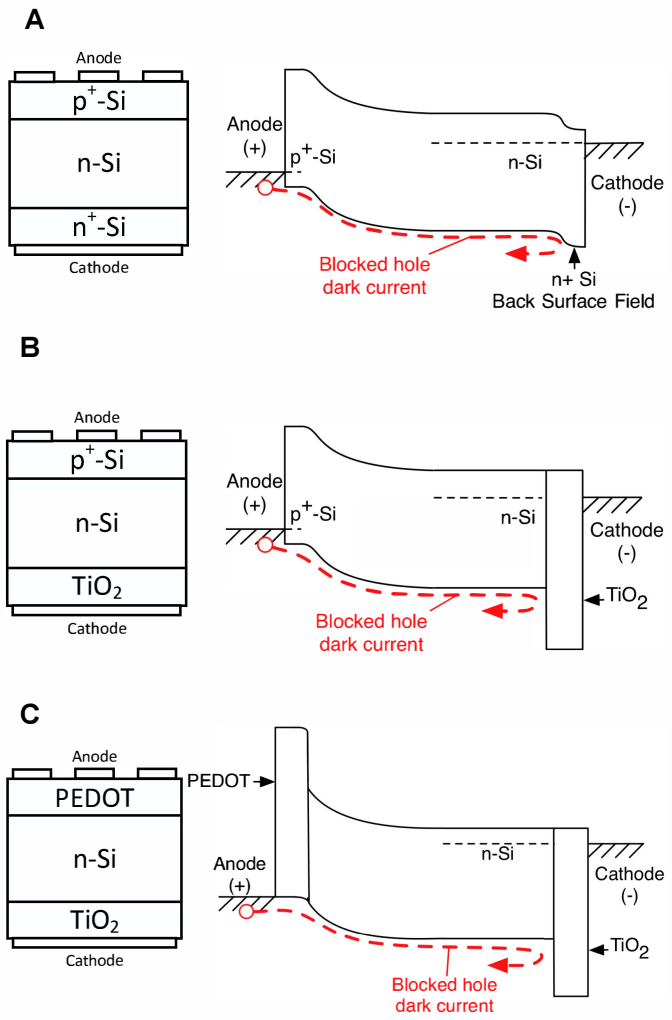

Fig. 4. Structure and band-diagram showing hole-blocking at cathode for (A) conventional p^+-Si/n-Si/n^+-Si (B) p^+-Si/n-Si/TiO_2 (C) PEDOT/n-Si/TiO_2

Simulations were performed to quantify the effect of s on power conversion efficiency for these structures. In Fig. 5A, the simulated IV curves are shown for 100 µm thick substrates with N_D = $5x10^{15}/cm^3$ and lifetimes of 1 ms under AM1.5 illumination assuming a perfect AR coating.

As the recombination velocity is increased from 0 cm/s (perfectly passivated) to 10,000 cm/s, V_{OC} is reduced by 0.15 V. A small decrease in J_{SC} (due to recombination of excited photocarriers at the back interface) is also observable as s increases. Fig. 5B shows the resulting effect on power conversion efficiency. The efficiency drops from over 24% for s = 10 cm/s to less than 19% as s approaches 10,000 cm/s. To achieve a minimum power conversion efficiency of 20%, an s value of 1000 cm/s or less is desirable for the n-Si/TiO_2 interfaces. Our measured s values of 200 cm/s is consistent with a 23% efficiency. Note that lighter substrate doping requires a lower s, whereas higher substrate doping makes the s less critical.

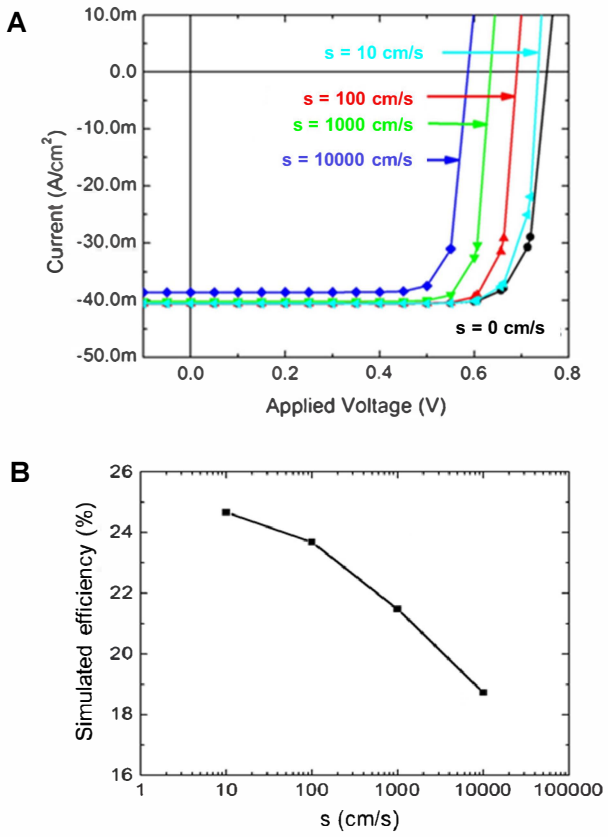

Fig. 5. (A) Simulated IV curves for different values of s at the n-Si/TiO_2 interface. (B) Corresponding power conversion efficiencies

V. Conclusions

We show that TiO_2/n-Si is a stable hole-blocking heterojunction, which could be used to replace the conventional n^+/n back surface field at the n-type contact in silicon photovoltaics. The interface recombination velocity at the TiO_2/n-Si interface can be as low as 70 cm/s and still be as low as 200 cm/s in air for 150 days. This value would be consistent with a power conversion efficiency of 23% in a p^+-Si/n-Si/TiO_2 solar cell or an EBL/n-Si/TiO_2 double heterojunction silicon solar cell with substrate doping of $5x10^{15}$ cm^{-3} and thickness of 100 µm.

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