Proc. IEEE 42nd Photovoltaic Spec. Conf. (PVSC), June 14-19, 2015, New Orleans, LA

DOI: 10.1109/PVSC.2015.7356054

Double-Heterojunction Crystalline Silicon Solar Cell with Electron-Selective TiO_2 Cathode Contact Fabricated at 100ºC with Open-Circuit Voltage of 640 mV

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***Abstract* — A double-heterojunction c-Si solar cell was fabricated at maximum process temperature of 100°C. We demonstrate an electron-selective passivated contact to Si using TiO_2, which increased the open-circuit voltage by 45 mV compared to a device with a direct metal to n-type substrate contact. In the fabricated structure, PEDOT/Si replaced the front-side p-n junction of conventional Si-based solar cells while the Si/TiO_2 interface is formed on the back-side. Compared to previous work [1], the V_{OC} has increased from 620 to 640 mV while maintaining a maximum process temperature of 100°C. Critical to the improved performance is better passivation of the Si/TiO_2 interface. The increase in V_{OC} can be attributed to an interface recombination velocity of ~ 75 cm/s, which is consistent with photoconductance decay measurements.**

***Index Terms* — carrier selective contact, heterojunction, passivation, metal-oxide, silicon, titanium oxide**

I. Introduction

Recently there has been much interest in carrier selective contacts for crystalline silicon solar cells. Carrier selective contacts (CSCs) are a novel approach to realizing high-efficiency silicon solar cells without p-n junctions fabricated at high temperatures (> 800°). TiO_2 on Si(100) has been shown to blocks holes ($\Delta E_V \geq 2.3$ eV) while being transparent to electrons ($\Delta E_C < 0.3$eV) [2]. Furthermore, Si/TiO_2 interfaces have demonstrated effective minority carrier recombination velocities below 10 cm/s [3]. The combination of these properties makes TiO_2 an excellent choice for an electron-selective contact for high efficiency and low-cost Si-based photovoltaics.

Previously, we demonstrated a double-heterojunction crystalline silicon solar [1]. The front-side p+/n junction of a conventional Si solar cell was replaced by a heterojunction formed between n-Si and the organic polymer Poly(3,4-ethylenedioxythiophene) poly (styrenesulfonate) (PEDOT) that blocks electrons but passes holes [4]. The back-side n+/n junction was replaced by the electron-selective Si/TiO_2 heterojunction The band-alignment and structure is shown in Figure 1. We showed that the electron-selective TiO_2 contact increased V_{OC} by 30 mV without degrading short circuit current or fill factor compared to a direct metal contact to the substrate. In this work, we show an increase of the effect of the TiO_2 contact on V_{OC} from 30 mV to 45mV. We accomplished this through reducing interface recombination.

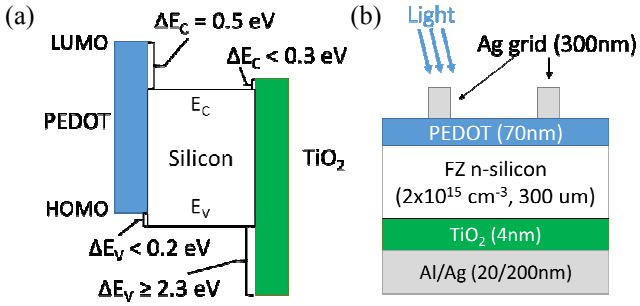

Fig. 1. (a) Band-alignment at PEDOT/Si and Si/TiO2 interface as measured by photoelectron spectroscopy. (b) Device structure [2]

II. Device Principle

The effect of the TiO_2 is shown in Figure 2. A single-sided PEDOT/Si device (with no TiO_2) is displayed in Figure 2(a). The PEDOT/Si interface acts as a hole-selective contact, blocking electrons while being transparent to holes. Furthermore, due to the high work-function of the PEDOT, there is a depletion region in the silicon which collects photogenerated carriers. Because the electron dark current (majority carriers) is blocked by the PEDOT/Si interface, the dark current is now dominated by the hole dark current (minority carriers).

With the electron-selective TiO_2 deposited on the backside (Fig. 2(b)), the hole dark current is blocked. This leads to a further reduction in the dark current and thus an increase in the open-circuit voltage. However, in reality, the Si/TiO_2 interface will have defect states, allowing holes to recombine and thus negating the hole-blocking functionality of the Si/TiO_2 interface (Fig. 2(c)). The interface quality is typically described though an interface recombination velocity S_{eff}. We calculated S_{eff} for different TiO_2 process conditions by measuring the minority carrier lifetime utilizing the Quasi-Steady State Photoconductance Decay (QSSPCD) method [5].

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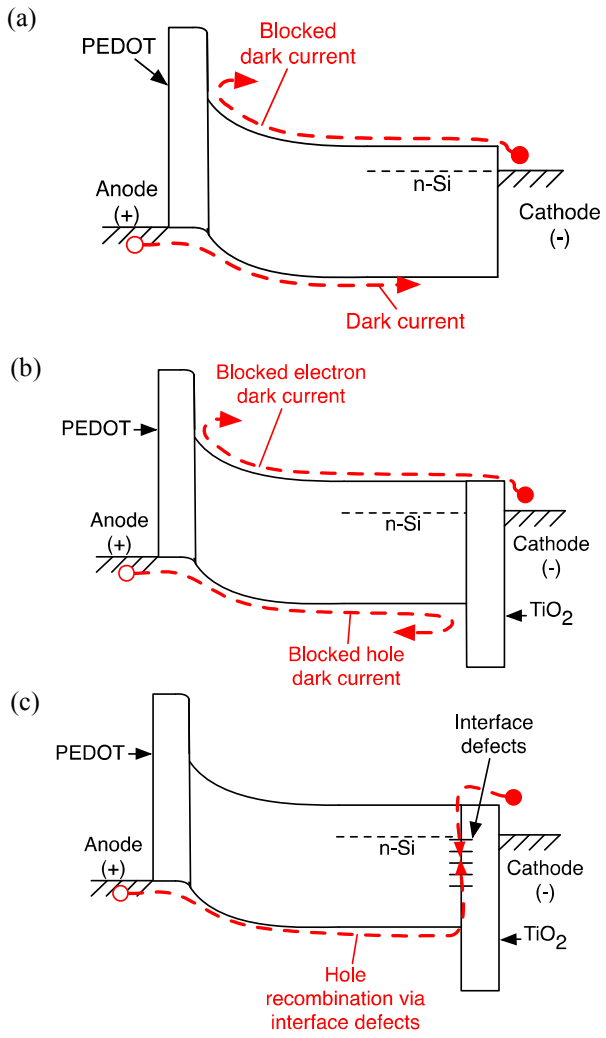

Fig. 2. Band diagrams of (a) Single-sided PEDOT/n-Si device (b) Double-heterojunction with electron-selective TiO_2 contact blocking hole dark current and (c) Double-heterojunction showing interface defects at Si/TiO_2 interface negating hole-blocking.

To elucidate the importance of interface recombination, one notes that the rate of hole transport in the substrate due to diffusion has to match the rate of recombination at the TiO_2 interface, which is proportional to the hole density at that interface. It is straightforward to show that the hole current ($J_{0,h}$) is reduced from its short base value $J_{0,SB}$ (no TiO_2) by a "blocking factor" BF, where

$$J_{0,h} = \frac{qn_i^2 D_p}{N_D W} * \frac{1}{BF} = J_{0,SB} * \frac{1}{BF} \qquad (1)$$

with BF = [(1+D_p/(W*S_{eff})] [1]. The calculated hole density profile is plotted in Figure 3 for an applied bias of 0.60V in dark (short-base scenario) for different S_{eff} values. A lower S_{eff} (smaller gradient) implies a higher BF and a smaller J_0. At S_{eff} = 0 cm/s, the gradient is completely flat. For an $S_{eff} > 10^3$ cm/s there is little effective blocking compared to a direct metal contact. Concomitantly, one can calculate an increase in V_{OC} from the reduced J_0 :

$$\Delta V_{OC} = kT * \ln\left(\frac{J_{0,no\ TiO2}}{J_{0,TiO2}}\right) = kT * \ln(BF) \quad (2)$$

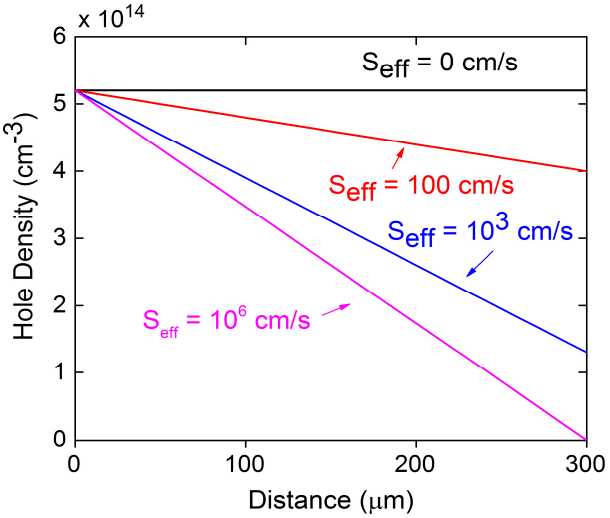

Fig. 3. Simulated hole density profile for a 300 μm thick wafer for different S_{eff} value. The applied bias is 0.60 V. Larger S_{eff} values lead to larger gradients

III. Results And Discussion

To demonstrate the effect of the passivated TiO_2 contact, the two structures from Figure 2(a) and 2(b) - without and with TiO_2 respectively - were fabricated. Experimental details regarding fabrication are given elsewhere [1], with the exception that an additional step was performed: samples were left in N_2 ambient at room temperature for 48 hours. This step improved the passivation of the Si/TiO_2 interface to the same level as a 250°C anneal (measured by QSSPCD, before cathode deposition) [6]. J-V curves under light (solar simulator at ~ 110 mW/cm^2) are shown in Figure 4. The increase in V_{OC} is consistent with the shift in dark current (inset). The relatively low J_{SC} values are due to the lack of an effective AR coating, PEDOT absorption, and the cathode metal coverage. A slight increase in short-circuit current due to the TiO_2 can be attributed to increased collection of long wavelength photons as the Si/TiO2 interface is passivated and thus fewer photogenerated carriers recombine at the cathode.

Figure 5 shows the blocking factor as a function of V_{OC} (from (2)) and S_{eff} from the observed V_{OC} (from (1)). Based on the experimentally observed increase in V_{OC} of 45 mV, we find a BF of 5.4. Using W = 300 μm and assuming D_p = 10

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cm^2s^{-1}, we estimate S_{eff} to be 75 cm/s. This S_{eff} value is consistent with calculated S_{eff} values from QSSPCD measurements of 65 - 85 cm/s at similar light levels.

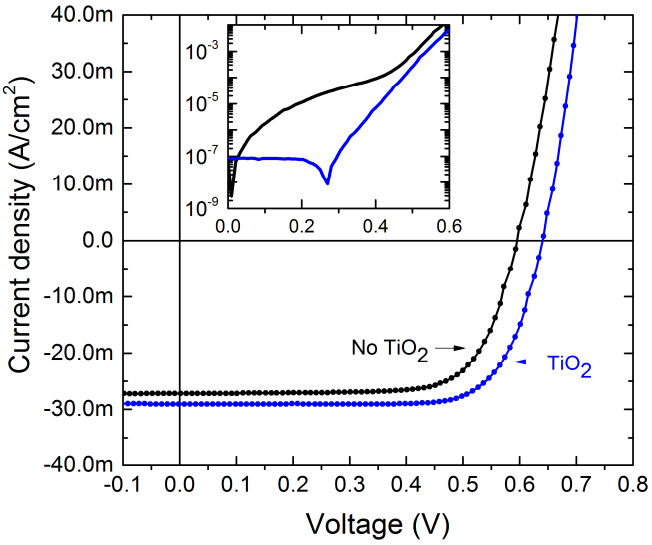

Fig. 4. J-V characteristics of device without TiO_2 (black) and with TiO_2 (blue) respectively under light. (inset shows dark J-V characteristics for 0 to 0.6 V)

TABLE I
SOLAR CELL PARAMETERS OF THE TWO DEVICES IN FIG. 4

	No TiO_2	With TiO_2	Change
V_{OC} (mV)	596	641	45
J_{SC} (mA/cm²)	27.2	29.1	1.9
FF (%)	72.7	74.4	1.7

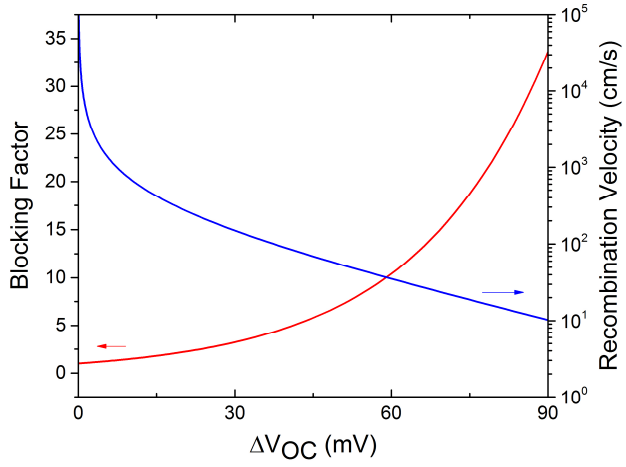

Fig. 5. From ΔV_{OC}, one can calculate the blocking factor (reduction in J_0) and the recombination velocity value required to achieve said ΔV_{OC}.

Figure 6 shows a comparison between $S_{eff}(\Delta V_{OC})$, extracted from ΔV_{OC} using (1) and (2) and S_{eff}(PCD), determined from QSSPCD measurements of the TiO_2/Si interface left in N_2 ambient for 48 hours at room temperature ('stabilized TiO_2'). Additionally, comparison between $S_{eff}(\Delta V_{OC})$ and S_{eff}(PCD) are made for 250°C annealed TiO_2 ('annealed' TiO_2') from previous experiments [6,7]. 250°C-annealed and room T-stabilized (this work) TiO_2 have similar S_{eff}(PCD) values. However 250°C-annealed TiO_2 has a large and high range for $S_{eff}(\Delta V_{OC})$. This indicates that although the 250°C annealing step reduces the recombination velocity measured by QSSPCD compared to as-deposited TiO_2, which typically has a S_{eff}(PCD) ~5000 cm/s, annealing at 250°C may lead to a morphology change (such as pinholes) which could allow the penetration of the cathode metal and thus increase $S_{eff}(\Delta V_{OC})$ and limits the effectiveness of 250°C annealed TiO_2 in a device.

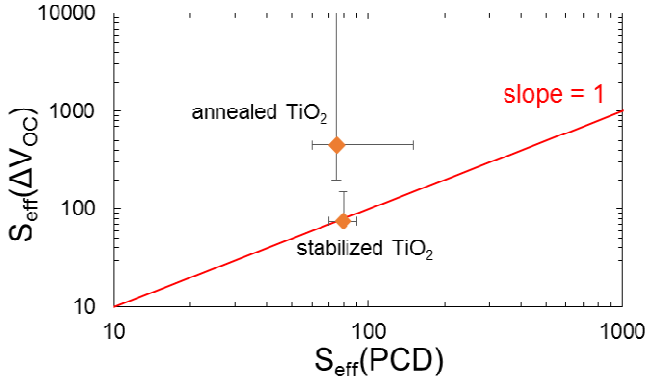

Fig. 6. Comparison of recombination velocities calculated from improvement in V_{OC}, $S_{eff}(\Delta V_{OC})$, and from QSSPCD measurements, S_{eff}(PCD), for 'annealed' TiO_2 (250°C anneal) and 'stabilized TiO2' (N_2 ambient for 48 hours – this work).

IV. CONCLUSIONS

We have shown for the first time the use of an electron-selective TiO_2 contact to improve the open-circuit voltage of crystalline silicon solar cells by 45 mV to reach a V_{OC} of 640 mV with a maximum process temperature of 100°C. The improvement in V_{OC} can be attributed to a well-passivated Si/TiO_2 interface with a recombination velocity of 75 cm/s.

ACKNOWLEDGEMENT

This work was supported by the DOE Sunshot Grant No. DE-EE0005315, the National Science Foundation Princeton MRSEC Grant No. DMR-0819860 and the Princeton Institute for the Science and Technology of Materials. Janam Jhaveri acknowledges support from the Andlinger Center for Energy and the Environment through the Maeder Graduate Fellowship

in Energy and the Environment. Gabriel Man acknowledges support through the Ph.D. fellowship from Natural Sciences and Engineering Research Council of Canada (NSERC).

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