antennas are in progress using different geometries and different excitation methods. It is believed that careful numerical modelling will provide more information on the appropriate choice of materials and their dimensions for achieving full broadband capabilities of multilayered dielectric radiators.

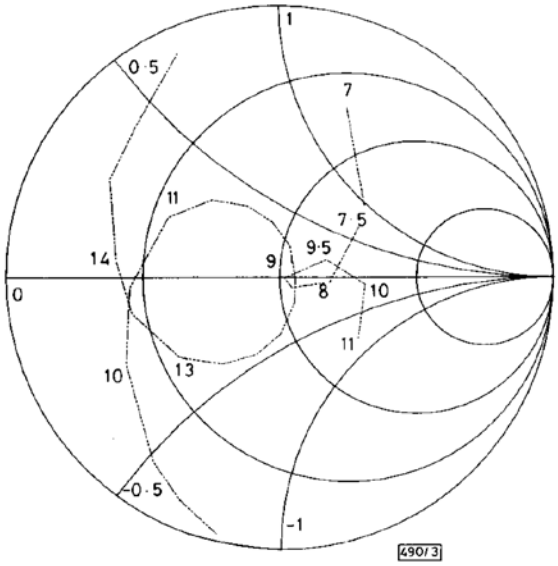

Fig. 3 *Measured input impedances for the antennas in Figs. 1 and 2*
Frequencies are in GHz; left plot is for single resonator and right one is for stacked resonators

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References

1 MUELLER, G. E., and TYRRELL, W. A.: 'Polyrod antennas', *Bell Syst. Tech. J.*, 1947, **26**, pp. 837–851
2 LIER, E., and AAS, J. A.: 'Simple hybrid mode horn feed loaded with a dielectric cone', *Electron. Lett.*, 1985, **21**, pp. 563–564
3 RUTHLEDGE, D.: 'Substrate-lens coupled antennas for millimeter and submillimeter waves', *IEEE Antennas & Propag. Soc. Newsletter*, Aug. 1985, **27**, pp. 5–8
4 LONG, S. A., MCALLISTER, M., and SHEN, L. C.: 'The resonant cylindrical cavity antenna', *IEEE Trans.*, 1983, **AP-31**, pp. 406–412
5 GLISSON, A. W., KAJFEZ, D., and JAMES, J.: 'Evaluation of modes in dielectric resonators using a surface integral equation formulation', *ibid.*, 1983, **MTT-31**, pp. 1023–1029
6 KAJFEZ, D., GLISSON, A. W., and JAMES, J.: 'Computed modal field distributions for isolated dielectric resonators', *ibid.*, 1984, **MTT-32**, pp. 1609–1616
7 SMITH, H. K., and MAYES, P. E.: 'Stacking resonators to increase the bandwidth of low-profile antennas', *ibid.*, 1987, **AP-35**, pp. 1473–1476

DEPENDENCE OF TRANSCONDUCTANCE ON SUBSTRATE BIAS IN ULTRATHIN SILICON-ON-INSULATOR MOS TRANSISTORS

Indexing terms: Semiconductor devices and materials, MOS structures and devices, Transistors, Silicon

A simple model is presented to explain the dependence of the transconductance on the substrate bias in ultrathin silicon-on-insulator MOS transistors. Good agreement with experimental data is found. The model can also be used to predict the dependence of transconductance on the underlying oxide thickness.

Recently it has been shown that the transconductance of fully depleted SOI MOSFETs on thick underlying oxides can exceed that of comparable bulk transistors. In this letter a simple model is presented to explain the dependence of the transconductance of fully depleted SOI MOSFETs on the substrate voltage. Supporting data are also presented. The model can also be used to predict the dependence of the transconductance on the underlying oxide thickness.

In a simple picture, a segment of the channel in an SOI MOS structure may be analysed as shown in Fig. 1. The channel potential is coupled to the top gate via the gate oxide capacitance C_{gate}. In the ideal case, as in a fully depleted SOI film on a very thick substrate, there is no other coupling to the channel. However in most FETs, there is a parasitic capacitance coupling to the channel. With a fully depleted SOI film, any new electric field lines from changing the channel voltage will terminate at the substrate underneath the underlying oxide. We may then define an effective substrate capacitance C_{subs} given by the series combination of the capacitance of the depleted SOI body and of the underlying oxide:

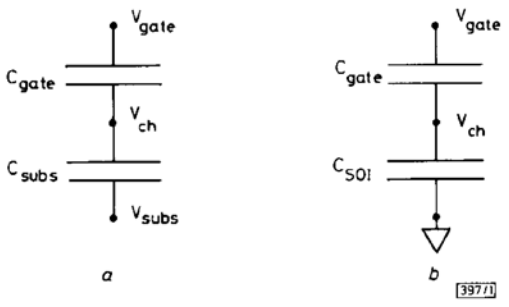

Fig. 1 *Capacitor model for fully depleted SOI FET (a) with depleted SOI film and depleted backside, and (b) with depleted SOI film but accumulated backside*

$$\frac{1}{C_{subs}} \equiv \frac{t_{box}}{\varepsilon_{ox}} + \frac{t_{SOI}}{\varepsilon_{Si}} \tag{1}$$

where ε_{ox} and ε_{Si} are the dielectric constants of silicon and oxide, respectively, and t_{box} and t_{SOI} are the underlying oxide and SOI thicknesses, respectively. This C_{subs} is then a parasitic capacitance which couples the channel to the substrate (Fig. 1). The analogous capacitance in a bulk transistor is the substrate space-charge layer capacitance.

To develop a model for the transistor current one needs an expression for the channel charge Q_{ch} as a function of the gate voltage V_G and the channel voltage V_{ch}. Defining the threshold voltage V_t as the gate voltage required for $Q_{ch} = 0$ when $V_{ch} = 0$, it follows from Fig. 1*a* that

$$Q_{ch}(V_{ch}, V_G) = (V_G - V_t - V_{ch})C_{gate} - V_{ch}\,C_{subs} \tag{2}$$

(We have assumed that the substrate voltage is held fixed.) This expression can then be used in the usual gradual channel approximation formulation to yield an expression for drain current I_D:

$$I_D = \frac{W}{L}\,\mu[(V_G - V_t)V_D\,C_{gate} - \tfrac{1}{2}(C_{gate} + C_{subs})V_D^2] \tag{3}$$

To determine the drain saturation current, one needs to set $Q_{chan} = 0$ to find the drain saturation voltage:

$$V_{DSAT} = V_{ch}|_{Q_{ch}=0} = (V_G - V_t)\frac{C_{gate}}{C_{gate} + C_{subs}} = \gamma(V_G - V_t) \tag{4}$$

$$\gamma \equiv \frac{C_{gate}}{C_{gate} + C_{subs}} \tag{5}$$

Note that we have defined an efficiency factor γ which is always ≤ 1. Substituting eqn. 3 into eqn. 2 and combining terms yields drain saturation current and transconductance:

$$I_{DSAT} = \gamma \frac{W}{2L} C_{gate} \mu (V_G - V_t)^2 \quad (6)$$

$$g_m = \frac{\partial I_{DSAT}}{\partial V_G} = \gamma \frac{W}{2L} C_{gate} \mu (V_G - V_t) \quad (7)$$

The expressions for the saturation current and transconductance are surprisingly simple; they are reduced from their ideal maximum value by the factor γ. For a fully depleted SOI FET with a gate oxide of 250 Å, SOI thickness of 1000 Å and an underlying oxide of 3500 Å, one finds $\gamma = 0{\cdot}94$.

If one applies a very negative substrate bias to a normally fully depleted n-channel SOI FET, the back interface will become accumulated with holes. The potential of this interface will be pinned close to the source voltage, since if it were positively biased holes would be injected into the source.[2] (We assume drain voltages small enough to avoid the 'kink' effect.) Because the potential at the back interface is now pinned, the effective substrate capacitance C_{subs} should now be replaced by simply the capacitance of the SOI film body, $C_{SOI} = \varepsilon_{Si}/t_{SOI}$ (Fig. 1*b*). The above derivation still holds, except that now

$$\gamma \equiv \frac{C_{gate}}{C_{gate} + C_{SOI}} \quad (8)$$

For the parameters described above, this would reduce γ to 0·57, and significantly degrade the transconductance.

As an experiment, n-channel MOSFETs were fabricated in SOI prepared by oxygen implantation. The device parameters corresponded to those just described, and $W/L = 50\,\mu m/8\,\mu m$. Drain saturation current is shown in Fig. 2 for several substrate biases. Because threshold voltages change with the substrate bias, the data are plotted against $V_G - V_t$ for a fair comparison. To analyse these data, it is necessary to have independent information on the charge state of the lower SOI interface. This may be inferred by measurements of threshold voltage against substrate bias.[3] At $V_{subs} = 0$, the threshold voltage in our transistors depends strongly on the substrate bias, indicating full depletion of the SOI film near the source. The SOI film will then also be depleted for higher channel voltages, and thus throughout the entire FET. Eqn. 5 gives

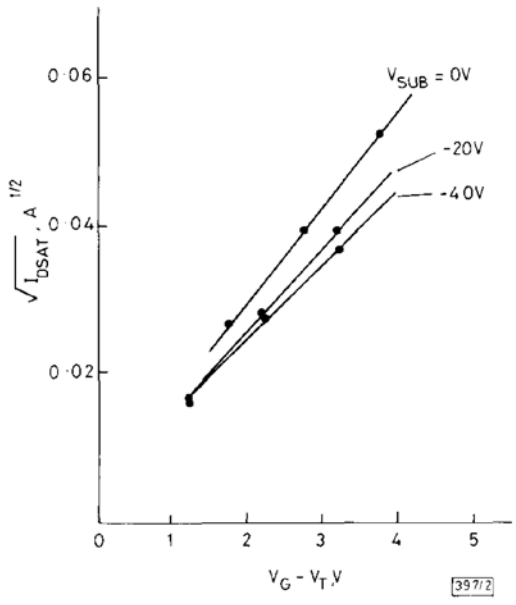

Fig. 2 *Square root of drain current against $V_G - V_t$ for single SOI FET as function of substrate voltage*

Gate oxide thickness is 250 Å, underlying oxide is 3500 Å, SOI thickness is 1000 Å, film doping is $10^{17}\,cm^{-3}$, $W/L = 50\,\mu m/8\,\mu m$

$\gamma = 0{\cdot}94$, and as seen in Fig. 2 this case of full depletion yields the highest transconductance.

For $V_{subs} \leq -10$ V, the threshold voltage in the experimental devices shows little dependence on V_{subs}, indicating accumulation at the lower SOI interface near the source. As one moves to higher channel voltages, keeping the back interface accumulated will of course require more negative substrate bias since the potential at the back interface cannot move by more than a few kT/q. The amount of this extra substrate bias is easily calculated by considering the relative capacitances of the SOI film and the underlying oxide. As the channel voltage is increased by ΔV_{ch} from zero, an increase in the substrate bias of ΔV_{SUBS} from -10 V will be required to maintain an accumulated backside, where $\Delta V_{SUBS} = -\Delta V_{ch}(t_{box}/t_{SOI})(\varepsilon_{Si}/\varepsilon_{SiO_2})$. For the experimental device measured here, this relationship corresponds to $\Delta V_{SUBS} = -10{\cdot}5 V_{ch}$. Thus for a -40 V substrate bias, the backside will be accumulated up to channel voltages of about 3 V (which includes all data points in Fig. 2), and the simple model based on Fig. 1*b* and the reduced γ of eqn. 8 may be used. In Fig. 2, the device with a -40 V substrate bias (fully accumulated backside) has a transconductance that is 0·64 of that of the fully depleted device (zero substrate bias). According to the simple theory outlined earlier, this ratio should be equal to the ratio of the efficiency factors γ of the two transistors. Taking the ratio of $0{\cdot}57/0{\cdot}94 = 0{\cdot}59$, we find good agreement with the experimentally observed ratio. For -20 V on the substrate, the back interface will be accumulated for channel voltages up to ~ 1 V, and the portion of the channel above 1 V will have a depleted backside. Indeed, for a substrate voltage of -20 V, the drain current for $V_G - V_t = 1$ is close to that of -40 V on the substrate (accumulated backside), but as the channel voltage increases ($V_G - V_t$ increases), the drain current rises faster than the accumulated backside case (as in the fully depleted case).

Through the efficiency factor γ, eqn. 4 can also be used to predict the dependence of the device performance in the fully depleted case on the underlying oxide thickness. For example, for the experimental parameters used above $\gamma = 0{\cdot}94$, indicating that the drain current in our experiment is 0·94 of its maximum (which would be achieved with an infinitely thick oxide). However, if the underlying oxide were reduced from 3500 to 1000 Å, γ would be reduced to 0·77. Our analysis has assumed negligible depletion in the SOI substrate, as would be caused by a heavily doped substrate or an accumulated substrate interface. This is the worst-case analysis since any substrate depletion would reduce C_{subs}. However in a real SOI CMOS circuit this worst case will probably be realised for one of the two transistor types.

In summary, a simple model utilising an efficiency parameter γ has been developed to explain the dependence of the transconductance in fully depleted SOI FETs on the substrate voltage and oxide thickness; good agreement with data is found. The results directly imply that consideration of the underlying oxide thickness and the charge condition of the lower SOI interface are very important in the design of high-performance, fully depleted SOI FETs.

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References

1 STURM, J. C., TOKUNAGA, K., and COLINGE, J.-P.: 'Increased drain saturation current in ultra-thin silicon-on-insulator (SOI) MOS transistors', *IEEE Electron Device Lett.*, 1988, **EDL-9**, pp. 460–463
2 COLINGE, J. P.: 'Reduction of kink effect in thin-film SOI MOSFET's', *IEEE Electron Device Lett.*, 1988, **EDL-9**, pp. 97–99
3 LIM, H.-K., and FOSSUM, J. G.: 'Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's', *IEEE Trans. Electron Dev.*, 1983, **ED-30**, pp. 1244–1251