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Increased Drain Saturation Current in Ultra-Thin Silicon-on-Insulator (SOI) MOS Transistors

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Abstract—**Based on considerations of substrate charge, an increased drain saturation current for MOS transistors in ultra-thin silicon-on-insulator (SOI) films is predicted compared to similar transistors in bulk or thick SOI films. For typical parameters of a 200-Å gate oxide with a channel doping of 4×10^{16} cm^{-3}, the drain saturation current in ultra-thin SOI transistors is predicted to be ~40 percent larger than that of bulk structures. An increase of ~30 percent is seen in measurements made on devices in 1000-Å SOI films.**

I. Introduction

THE conventional advantages of silicon-on-insulator (including silicon-on-sapphire) for MOS transistor circuitry have been low nodal capacitances and radiation hardness. Recently, it has been shown that silicon-on-insulator (SOI) MOSFET's fabricated in ultra-thin (< 1000 Å) films offer additional performance advantages for submicrometer ULSI scaling. These advantages include short-channel threshold-voltage stability, improved subthreshold slopes, and hot-electron immunity [1]–[3]. In this letter, an additional advantage of SOI MOSFET's in ultra-thin films will be described. It will be shown that the drain saturation current, and hence saturation transconductance, in ultra-thin SOI MOSFET's can be substantially larger than that of similar FET's in thick SOI films or bulk substrates.

II. Vertical Substrate Electric Fields

The current in a MOS enhancement-mode n-channel transistor depends directly on the number of electrons in the channel. These electrons form a "channel charge," which is supported by the gate electrode. The gate electrode not only supports the channel charge, however; it also supports the charge in the substrate depletion layer required by the band bending between the channel and the substrate. In a conventional MOSFET, as one moves from the source to the drain end of a device, this substrate charge grows as the channel-to-substrate potential grows. If the channel voltage is large enough such that the entire electric field across the gate oxide is required to support the substrate charge, the device is in saturation or "pinched off"—there is no vertical electric field from the gate left to support any charge in the channel.

By integrating the charge in the depletion region from the substrate to the channel, the vertical electric field in the silicon just under the inversion layer (E'_{Si}) can be expressed mathematically as

$$E'_{Si} = \left[\frac{2N_A q}{\epsilon_{Si}} (2\phi_p + V_{CH} - V_{SUBS}) \right]^{1/2} \tag{1}$$

where V_{CH} is the channel voltage and the other terms have their usual meanings. Clearly E'_{Si} (and hence the substrate charge) increases as one goes from source to drain. This change in substrate charge gives rise to the body effect.

To see the scale of this increase in electric field, consider a FET with parameters typical of 1-μm technology: a gate oxide thickness of 200 Å and a channel doping of 4×10^{16} cm^{-3} (assumed constant for simplicity). Fig. 1(a) shows the vertical electric field of a long-channel device as a function of depth plotted for a region of the channel near the source and another near the drain (PISCES-IIB simulation [4]). (To insure long-channel behavior, a device with a 20-μm effective channel length was simulated.) Operating conditions of $V_S = V_{SUBS} = 0$, $V_G - V_T = 3$ V, and $V_D = 2.5$ V were chosen to correspond to the onset of saturation. The rapid change in electric field near the silicon surface ($x = 0$) represents the electrons in the inversion layer, and the electric field just under the inversion layer is a measure of the substrate charge. Note how the substrate charge grows as one moves from the source end of the device to the drain end. This increasing substrate charge comes at the expense of possible electrons in the channel, and hence at the expense of a possibly larger device current.

For comparison, consider a MOSFET in an ultra-thin SOI film. (Consider an 800-Å film with the same gate oxide and channel doping assumed above.) If the film is sufficiently thin so that the film is completely depleted at threshold, the space charge in the SOI body cannot increase as the channel voltage is raised. The vertical electric field in the SOI will vary, however, because of the contribution of the vertical field in the underlying insulator. If we then consider a very thick underlying insulator, with only a finite voltage on the substrate, we then can claim that the field in the insulator is effectively pinned near zero, and that the contribution of this field to the field under the inversion layer is zero.

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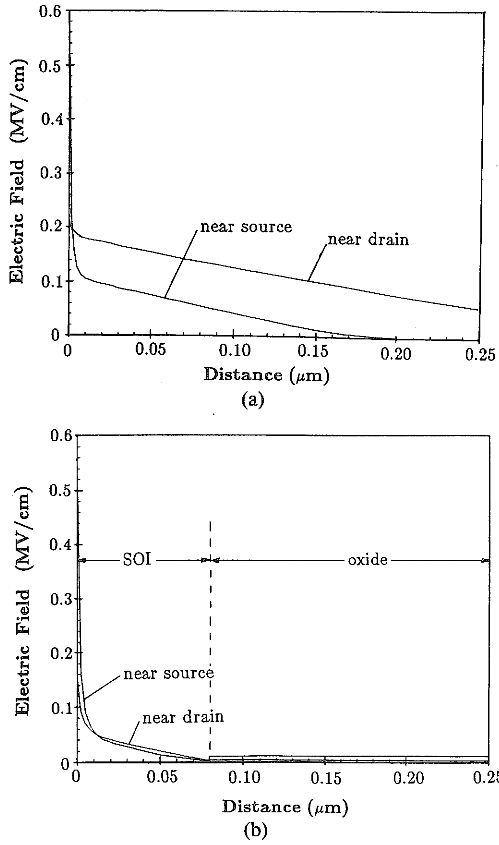

Fig. 1. Vertical electric field in a long-channel MOS transistor near the source and drain ends of the device for (a) a bulk device (b) a device in an 800-Å SOI film ($N_S = 4 \times 10^{16}$ cm^{-3}, $t_{gateox} = 200$ Å, $V_S = V_{SUBS} = 0$, $V_D = 2.5$ V, $V_G - V_T = 3.0$ V). The effective channel length is 20 μm; the "near-source" plot is taken 1.2 μm from the metallurgical source junction, and the "near-drain" plot is taken 0.2 μm from the drain junction. The bulk transistor is on the edge of saturation and the SOI device is not.

Mathematically, using Gauss's law, it is easy to show that

$$E'_{SOI} = \frac{\epsilon_{SiO_2}(V_{CH} + 2|\phi_p| - V_{SUBS}) + \frac{N_A q t_{SOI}^2 \epsilon_{SiO_2}}{2\epsilon_{Si}} + N_A q t_{SOI} t_{ox}}{t_{ox}\epsilon_{Si} + t_{SOI}\epsilon_{SiO_2}} \tag{2}$$

where E'_{SOI} is the vertical field in the SOI FET just under the inversion layer, t_{SOI} is the film thickness, N_A is the SOI film doping, and t_{ox} is the underlying oxide thickness. (We have assumed a zero flat-band voltage between the SOI and the underlying substrate. We have also assumed a substrate voltage such that inversion or accumulation is avoided at the back SOI interface. For small fixed charge densities, $V_{S-SUBS} = 0$ achieves this affect.) If the underlying oxide is thick, then E'_{SOI} reduces to

$$E'_{SOI} = \frac{N_a q t_{SOI}}{\epsilon_{Si}}. \tag{3}$$

As expected, the surface electric field then becomes independent of the channel voltage, and depends only on the space charge in the SOI film.

Fig. 1(b) shows the vertical electric field as a function of depth in a device with a SOI thickness of 800 Å, an underlying oxide thickness of 2 μm, and other parameters the same as those for the bulk device. Again we have chosen $V_S = V_{SUBS} = 0$, $V_G - V_T = 3$ V, and $V_D = 2.5$ V. (Because the threshold voltage of the SOI device was less than that of the bulk device, we hold $V_G - V_T$ fixed for a fair comparison to the bulk device.) Note that in this case the vertical fields due to substrate charge are virtually identical at the source and drain ends of the device. The effective total integrated substrate charge (per unit area) in the SOI device is constant at $\sim 5 \times 10^{-7}$ C/cm^2, while the substrate charge from source to drain in the bulk device has nearly doubled from 1.0×10^{-7} to 1.8×10^{-7} C/cm^2. Both devices had a channel carrier density near the source of 5.0×10^{-7} C/cm^2, but the SOI device still has a significant number of electrons in the inversion layer at the drain end of the device (over 10^{-7} C/cm^2). For comparison, recall that the bulk device had close to zero carriers at the drain corresponding to the onset of saturation. All other things being equal, we would then expect more carriers in the channel of the SOI device (especially near the drain) and hence a higher drain current.

III. Drain Current

Long-channel structures like those just described were modeled using the PISCES-IIB two-dimensional device simulator and fixed channel mobilities, and a homemade one-dimensional simulator using the gradual channel approximation. As expected for long channels, the two methods gave good agreement. Fig. 2 shows a comparison of the results of this fixed mobility simulation. Since the two devices have different threshold voltages, the gate voltages are referenced to the threshold voltage of each device. As expected, the SOI drain current exceeds that of the bulk device. Over the range $V_G - V_T = 0$ to 4 V, the saturation current increase of the SOI device averages ~30 percent. Some practical SOI structures (such as those formed by oxygen implantation) would probably have a thinner oxide (on the order of 3500 Å) than the 2 μm used for the modeling. Using the worst-case boundary condition of a fixed potential under the underlying oxide, this thinner oxide would lead to a slight reduction of the saturation current (5-percent reduction for a 3500-Å oxide).

There is a second effect which should serve to further increase the current in the SOI device. As increasing vertical fields confine carriers closer to the Si–SO_2 interface scattering sites, surface mobilities are known to decrease [5]. Since the vertical fields in ultra-thin SOI devices are in general less than those of bulk devices, especially near the drain end of a device, the carriers in an SOI channel should have a higher mobility than their bulk counterparts. To explore the scale of this effect, data from Sun and Plummer [5] for a typical fixed oxide charge of 10^{11} cm^{-2} were incorporated into our one-dimensional device simulator. Using the same structures described above, the SOI device was found to now have a saturation current ~40 percent larger than the bulk device.

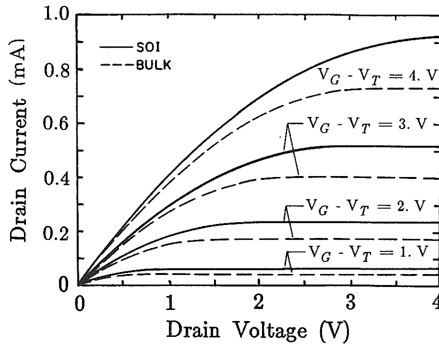

Fig. 2. Simulated curve-tracer characteristics for bulk and ultra-thin film SOI MOSFET's. Fixed and equal electron surface mobilities were used.

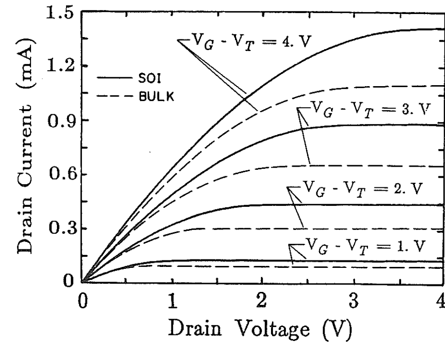

Fig. 3. Curve-tracer characteristics (data) for bulk and 1000-Å SOI MOSFET's. The bulk threshold voltage is 0.7 V and the SOI threshold is 0.2 V. Sources and substrates were grounded in both cases.

(An increase of ~30 percent was found with identical fixed mobilities.)

This effect of increased mobility due to reduced electric fields has already been demonstrated in 1000-Å films with small drain voltages (V_{DS} = 0.1 V) [6]. This concept has not previously been applied to the saturation region (large drain voltages) where transistors in digital circuits generally operate. However, as shown above, our calculations indicate that the new effect of increased carriers in the channel is predicted to have a substantially larger effect on drain current than the increase in mobility.

As an experiment, FET's were fabricated simultaneously in both bulk wafers and in 1000-Å SOI films on 3500-Å oxide created by the oxygen implantation and annealing process. The gate oxide thickness was estimated at 250 Å and the channels in both devices were doped at 10^{17} cm^{-3} p-type. Thus the SOI devices should be fully depleted when ON. Fig. 3 shows the curve-tracer characteristics of otherwise identical 20-μm/8-μm SOI and bulk devices. The gate voltages for each device are referenced to its own threshold voltage. The SOI devices showed a saturation current increase of 25–30 percent over the bulk device. This is somewhat less than our simple modeling would predict. It should be pointed out, however, that the annealing of the SIMOX films to remove the implantation damage was done at 1250°C, lower than is commonly used for optimal SIMOX annealing [7].

IV. Discussion

Using the gradual channel approximation and a constant mobility, the expression for the drain current in a bulk MOS transistor is well known [8]:

$$I_D = \mu_n \frac{W}{L} \left\{ C'_{ox} \left(V_G - V_{FB} - 2|\phi_p| - \frac{1}{2} V_D - \frac{1}{2} V_S \right) \cdot (V_D - V_S) - \frac{2}{3} \sqrt{2\epsilon_{Si} q N_a} [(2|\phi_p| + V_D - V_{sub})^{3/2} - (2|\phi_p| + V_S - V_{SUBS})^{3/2}] \right\}. \quad (4)$$

The symbols in the above expression have their usual meanings, and a constant substrate doping profile is assumed. If one simplifies the derivation of this expression with the assumption of a fixed substrate charge [8], one arrives at the common expression

$$I_D = \mu_n \frac{W}{L} C'_{ox} (V_G - V_T - V_{DS}/2) V_{DS}. \quad (5)$$

Since SOI transistors in ultra-thin films with thick underlying oxides have a fixed vertical substrate electric field, they have a fixed "effective substrate charge," and (5) should be a valid description of drain current. Indeed, using a charge-based model, Lim and Fossum have arrived at an expression similar to (5) for fully depleted SOI MOSFET's [9]. As expected, (4) and (5) agree well with the results of our fixed mobility simulations (Fig. 2).

Our simulations and measurements have been performed for long-channel devices with a fixed substrate doping and gate oxide thickness. With respect to doping and gate oxide thickness, the effect is expected to scale qualitatively as the body effect, i.e., greater with increased substrate doping but less with thinner gate oxides. In the short-channel regime, velocity saturation and other effects make one-dimensional modeling and the gradual channel approximation inappropriate. Thus further work will be necessary to accurately predict scaling of this current enhancement effect into the submicrometer range. The effect described in this paper and other advantages of ultra-thin film SOI depend on the full depletion of the SOI film. With channel dopings in the 10^{17} cm^{-3} range, this will require film thickness of 1000 Å or less.

V. Conclusion

The effective substrate electric field is smaller in MOS devices in ultra-thin SOI films with thick underlying oxides than in similar bulk devices. This leads to more carriers in the channel and thus to an increase of the drain saturation current on the order of 30–40 percent for a 1-μm technology. Further work is needed to explore the importance of this effect in the submicrometer regime.

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