Minority-carrier properties of thin epitaxial silicon films fabricated by limited reaction processing

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Generation lifetimes and diode properties have been measured in epitaxial silicon films grown by limited reaction processing. Generation lifetimes from 1.4 to 94 μs were measured by observing the recovery of MOS capacitors from deep depletion. Planar diodes fabricated in both *n*- and *p*-type epitaxial films show excellent behavior in both forward and reverse bias. *p-n* junctions formed by growing *p*-type epitaxial silicon directly on an *n*-type substrate show no evidence of excessive interface defects or traps.

Limited reaction processing (LRP) is a new technique for fabricating thin semiconductor and insulator layers by controlled high-temperature surface reactions.[1] In an earlier letter, the growth of thin epitaxial silicon layers with extremely abrupt doping profiles was described. The film quality was evaluated in our laboratory by both Rutherford backscattering (RBS)[1] and by majority-carrier mobility measurements. These measurements both showed the material to be indistinguishable from single-crystal silicon substrates. However, these techniques do not provide very exacting tests of crystal quality. Minority-carrier properties and devices provide a much more stringent and ultimately more practical test of the quality of semiconductor layers. In this communication we report the results of generation lifetime measurements and *p-n* junction formation in LRP epitaxial silicon films.

The LRP technique uses the sample temperature to control the start and stop of surface reactions (such as epitaxial growth or oxidation), rather than using the gas flows as is conventionally done. The wafer temperature can be rapidly and reproducibly controlled using radiant heating from lamp banks controlled by microprocessors. (Others have used radiant lamp heating to control the wafer temperature for epitaxial growth, but they have used the gas flows, as opposed to the sample temperature as done here, to control the start and stop of the growth process.[2]) Because the LRP technique minimizes the time a wafer is exposed to high temperature, it has the ability to grow ultrathin epitaxial layers with the detectable transition thickness approaching those of molecular beam epitaxy (MBE).[1,3]

The epitaxial films grown by LRP studied here were typically 2–3 μm thick and had carrier concentrations on the order of 5×10^{16} cm^{-3}. *n*-type films were grown on Sb-doped *n*-type (100) 2-in. silicon substrates with a resistivity of $\sim$0.02 Ω cm, and *p*-type films were grown on boron-doped *p*-type (111) substrates with a resistivity of $\sim$0.05 Ω cm. The source gases for the growth were silane and diborane in a hydrogen carrier for the *p*-type samples, and dichlorosilane for the *n*-type samples. The deposition temperature was in the range of 850–950 °C, the growth pressure was 4.2 Torr, and the growth rate varied from 0.5 to 1.0 μm/min.

The minority-carrier generation lifetimes were measured in the epitaxial films by the technique of deep depletion recovery of MOS capacitors described in principle by Zerbst.[4] The capacitors were formed by oxidizing the epitaxial layers in a steam ambient at 1000 °C to give an oxide thickness of about 650 Å. A high-temperature anneal, metal evaporation, lithography, and patterning, and a 450 °C forming gas anneal completed the fabrication of the test structure. For control purposes, test capacitors were also fabricated directly in both *n*- and *p*-type (100) Czochralski single-crystal substrates, with doping levels comparable or lower than those in the epitaxial films. During the measurements, a computerized feedback system was used to adjust the gate voltage to hold the depletion width (and, hence, the generation volume) constant.[5,6] Guard rings were used to minimize lateral effects. This is especially important for lightly doped layers. Five to ten capacitors were measured on each sample.

The results of the generation lifetime measurements are shown in Table I. In all cases there was some random variation in the measured lifetimes, but the generation lifetimes in the LRP samples were consistently in the range of microseconds for *n*-type epitaxial films and tens of microseconds for *p*-type epitaxial films. Why the *p*-type sample yielded longer lifetimes than the *n*-type sample is not known. While the lifetimes for the LRP films were roughly an order of magnitude lower than those found in the virgin Czochralski wafers, they nevertheless represent excellent material. Generation lifetimes in the 10 μs range are common for epitaxial silicon films used for very large scale integration (VLSI) processing.[7]

The simplest minority-carrier device is a *p-n* junction diode. Planar diodes were fabricated in the LRP epitaxial layers described earlier by ion implantation and annealing. The implants were masked by deposited oxide which was lithographically patterned. A dose of 1×10^{15} cm^{-2} of 50-keV BF_2^+ ions was implanted into an *n*-type epitaxial layer and annealed at 1000 °C for 3 min to create p^+-*n* diodes. As^+ ions (100 keV, 2×10^{15} cm^{-2}) were implanted in a *p*-type epitaxial layer and annealed for 20 s at 1000 °C to create n^+-*p* diodes. The depth of the annealed junctions was on the order of 0.2 μm in both cases, much less than the 2–3 μm thickness of the epitaxial layers. Because the implanted layers were heavily doped, the junction depletion regions were primarily in the lightly doped unimplanted epitaxial material under the heavily doped surface layers. Since the performance of *p-n* junctions is strongly dependent on the material

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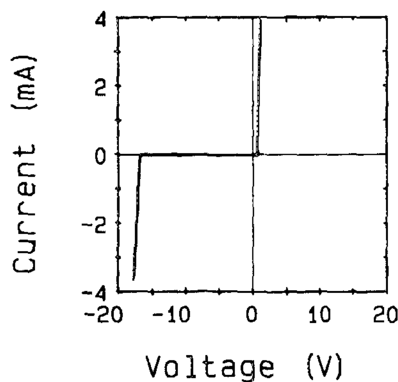

FIG. 1. Typical curve-tracer characteristics for an n^+-p diode.

TABLE I. Generation lifetimes for LRP epitaxial layers and control Czochralski (CZ) wafers.

Sample	Doping type and orientation	Doping level (cm^{-3})	Generation lifetime (μs)
CZ	n-(100)	2×10^{15}	49–87
LRP	n-(100)	2.5×10^{16}	1.4–4.3
CZ	p-(100)	7×10^{16}	144–203
LRP	p-(100)	7×10^{16}	14–94

quality in the depletion region, these diodes should be a good probe of the "as-grown" epitaxial material. Metal contact formation and a forming gas anneal completed the diode fabrication.

Both the n^+-p and p^+-n diodes had well-behaved curve-tracer characteristics (Fig. 1) and had breakdown voltages consistent with the doping of the epitaxial films (24 V for the p^+-n diodes, 16 V for the n^+-p diodes). More interesting is the low current behavior of the diodes in forward bias. A commonly used measure of semiconductor junction quality is the diode quality factor commonly referred to as "n." The quality factor describes how fast the diode current increases in forward bias compared to the ideal maximum slope (59 mV/decade of current at room temperature, $n = 1.00$). In diodes in material with very low lifetimes, the forward current will be dominated by recombination at defects in the depletion region, leading to a slope of 2×59 or 118 mV/decade ($n = 2.00$).[8]

Figure 2 shows the current-voltage relationship of a typical p^+-n diode in forward bias. From the linear portion of the curve on this semilogarithmic plot, a diode quality factor of 1.05 is found. The diode quality factor for the n^+-p diodes was 1.10. Control diodes in Czochralski substrates had a quality factor of 1.00–1.03. The reverse-bias leakage current was measured on p^+-n diodes in the LRP films with an area of 3.4×10^{-4} cm^2. A typical leakage current at a reverse bias of 5 V was 7 pA. Using a simple one-dimensional approximation for the depletion region width, a generation lifetime in the epitaxial film of 4 μs can be calculated to be consistent with the observed currents. This lifetime is within the range of those measured by the deep depletion recovery method (Table I).

Because defects and generation-recombination centers can lower lifetimes by many orders of magnitude, the relatively good lifetimes and diode performance indicate that the LRP epitaxial layers are of rather high quality. Good films suggest accurate alignment of the first epitaxial layers nucleated during the temperature ramp-up in the LRP deposition cycle. This is fortunate because these layers serve as templates for subsequent growth, and a few poor initial layers would likely result in a low-quality film. (Low-temperature deposition for long times results in poor epitaxial alignment or even polycrystalline growth.) Apparently, the rate of increase of the sample temperature (room temperature to $\sim$900 °C in $\sim$3 s) is fast enough to avoid such problems.

To further examine the epitaxial layer–substrate interface, p-n junctions were formed by growing p-type epitaxial silicon films (thickness ~2 μm, doping $\sim5\times10^{17}$ cm^{-3}) directly on the n-type silicon substrates described earlier. The depletion regions associated with the junctions should then include the substrate interface. Individual p-n diodes were formed by aluminum deposition and patterning followed by silicon mesa etching. Note that no ion implantation or high-temperature annealing was required to create the diodes. The forward-bias characteristics of three diodes of different area is shown in Fig. 3. Note that the current scales as the area of the diodes. The diodes exhibit an ideality factor of 1.05, indicating a minimum of defects in the depletion

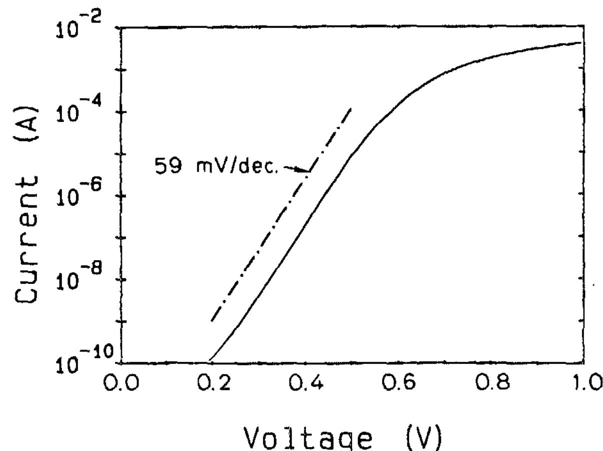

FIG. 2. Typical current-voltage relationship for a p^+-n diode in forward bias. The diode area was 3.4×10^{-4} cm^2.

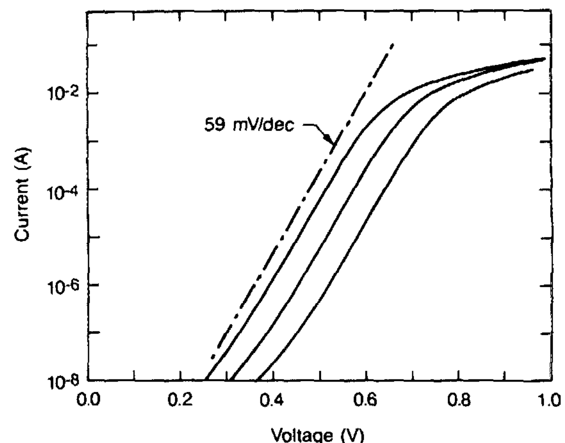

FIG. 3. Forward bias characteristics of substrate–epitaxial layer n-p diodes. The diode areas are 4.9×10^{-2}, 5.1×10^{-3}, and 4.8×10^{-4} cm^2.

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region and, hence, negligible defects at the substrate interface. Thus, the temperature transient during the beginning of the LRP growth cycle appears to have had no adverse affects on the electrical properties of the substrate-epitaxial layer interface. The actual atomic quality of the epitaxial layer-substrate interface is currently under further investigation.

In summary, the minority-carrier properties of silicon epitaxial films grown by limited reaction processing have been investigated. The films exhibit relatively high lifetimes (1–100 μs) and good diode characteristics. Furthermore, the substrate–epitaxial layer interface shows no evidence of excessive traps or recombination centers. High-quality films and interfaces combined with the ability to grow 10-nm layers[3] should make LRP a useful tool for the fabrication of high-performance electronic devices.

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Common occurrence of distortion in semiconductor luminescence spectra

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The distortion of semiconductor luminescence spectra by selective absorption of totally internally reflected rays in the specimen is investigated by varying the effective field of view of the collection optics and by local excitation from a focused electron beam. For example, in undoped InP, the results show that an artifactual enhancement of the acceptor related luminescence by a factor of ~ 50 occurs if the field of view commonly used in luminescence experiments (~ 1 mm) is employed. In addition, a shoulder on a spectral peak close to the absorption edge, which could be interpreted as being due to a separate recombination mechanism, is shown to be merely an artifact arising from this distortion. This communication shows for the first time that the effect can be both detected and eliminated by a novel field-of-view masking technique.

Self-absorption of luminescence is a well-established, but often neglected, phenomenon. Two main effects have to be considered, namely that luminescence is generated over a distribution of depths and that the back surface reflection affects the various paths the collected rays take through the material. The present communication deals with the latter effect which has led to the misinterpretation of spectra, as shown in previous work. For example, Carr and Biard[1] have pointed out that the externally measured room-temperature electroluminescence spectrum of a GaAs *p-n* junction optical source does not match the internal generation spectrum and that this leads to erroneous interpretation of the spectrum.

They showed that this discrepancy was due to the back surface reflection. Dean[2] has noted the importance of this effect in causing artifacts in luminescence spectra. Warwick and Booker[3] have developed the novel field-of-view masking technique, also used in the present work, to investigate such artifacts (referred to as "ghost peaks")[1-3] in cathodoluminescence spectra from InP at 88 K, and have shown that luminescence determination of dopant striation inhomogeneity is erroneous if the effect is not to be eliminated by field-of-view masking. The present work shows for the first time that this effect can be very important in luminescence at liquid-helium temperatures, particularly if the commonly used field of view of ~ 1 mm is employed, and that the artifacts so induced can be both detected and eliminated using the field-of-view masking technique. This technique is shown to be suitable for use at liquid helium temperatures, and so could be used to increase the accuracy of luminescence determinations of, for example, dopant inhomogeneity.

In the present work distortions in the luminescence spectrum of undoped liquid-encapsulated Czochralski-grown InP at 10 K was investigated. The 5-mm-square specimens of 0.3-mm thickness had the top surface, which received the electron beam excitation, polished with 2% v/v Br_2/CH_3OH solution and the bottom surface as cut with the

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