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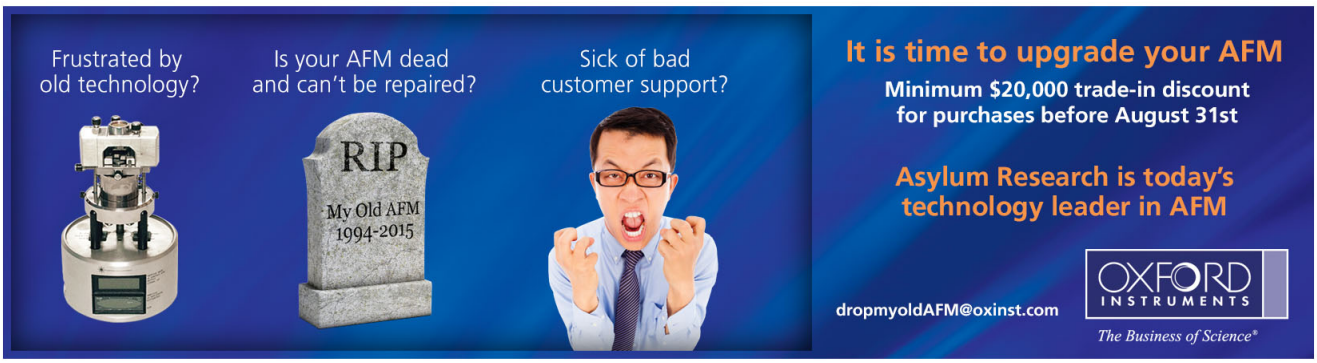

Measurement and reduction of interface states at the recrystallized silicon-underlying insulator interface

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Deep level transient spectroscopy and capacitance-voltage measurements have been performed on an inverted metal-oxide-semiconductor (MOS) capacitor structure to measure the interface state density at the recrystallized silicon-underlying insulator interface. The effects of different recrystallization caps, annealing steps, and different underlying oxides have been investigated. An interface state density in the mid 10^{10} cm^{-2} eV^{-1} range can be consistently obtained, enabling well-behaved MOS transistor channels on the bottom of the recrystallized films.

The interface between a recrystallized silicon film and the underlying insulator can be characterized electrically by both interfacial fixed charge (N_f) and the density of interface states (D_{it}) within the band gap of the semiconductor. These parameters are technologically important as the fixed charge can affect the threshold voltage of metal-oxide-semiconductor field-effect transistors (MOSFET's) on both the bottom and top of the film, and the interface states can degrade the subthreshold slopes of MOSFET's on both the bottom and top of the film. In addition, interface states can serve as generation centers causing leakage current in devices, and act as recombination centers detrimentally affecting minority-carrier devices such as bipolar transistors and solar cells.

Both silicon dioxide and silicon nitride have been used as underlying insulators for recrystallization. However, the interface with an underlying nitride has been found to be of extremely poor quality and exhibit gross charge trapping.[1] Hence we have restricted our work to using silicon dioxide as the underlying insulator. While several studies have been done of the fixed charge associated with the underlying interface,[1–3] only one previous study[2] has been published with data on the interface state densities, with a lowest reported midgap state density of 10^{12} cm^{-2} eV^{-1}. Using an oxide recrystallization cap and appropriate annealing, we have found that an interface state density as low as 4×10^{10} cm^{-2} eV^{-1} is possible.

The test structure used is the inverted MOS capacitor shown in Fig. 1 and was first described by Kamins *et al.*[1] A heavily doped substrate is used as the "gate" electrode to vary the surface potential on the bottom of the recrystallized film. The film doping was chosen so that the maximum depletion width in the film is less than the film width itself. In this way conventional MOS capacitance-voltage (C-V) and deep level transient spectroscopy (DLTS) measurements can be performed on the interface underneath the recrystallized film.

For fabrication of the structure the starting material was n-type silicon wafers which were heavily doped with phosphorus at the surface by conventional diffusion. Silicon dioxide layers of thickness 1500 Å were then either grown thermally or deposited. Polycrystalline silicon (polysilicon) films of 0.5-μm thickness were deposited on the oxide by low pressure chemical vapor deposition (LPCVD). Capping layers of 450-Å LPCVD silicon nitride or 850-Å atmospheric pressure CVD silicon dioxide (silox) were deposited onto the polysilicon to aid the recrystallization step. Boron ion implants of dose 1.5×10^{12} cm^{-2} were done prior to recrystallization. The recrystallization was performed with a cw argon ion laser with the beam shaped to a spot of roughly 200×15 μm^2 and a beam power of approximately 10 W. The samples were held at a substrate temperature of 350–400 °C during the laser processing. The beam was raster scanned at speeds from 10 to 20 cm/s with approximately a 50% overlap between adjacent scan lines to completely cover the sample. A subsequent Secco etch revealed a grain size of about 50×200 μm^2 with a subgrain boundary spacing within each grain of a few microns. The recrystallization uniformly distributed the boron dopant through the silicon film.

After recrystallization, the capping layers were removed and circular islands of diameters from 80 to 2000 μm were defined by plasma etching. This determined the area of the capacitors. After high-temperature annealing in oxygen or nitrogen ambients, a passivating layer of SiO_2 was then deposited, contact holes were opened, and a metal layer of Al:Si (99:1) was deposited by sputtering and lithographically defined. A 15-min 450 °C forming gas anneal completed the processing and insured ohmic contacts to the silicon layer.

In earlier work[1,2] the silicon islands were defined after metallization using the patterned metal as a mask for the plasma etch of the silicon. Although a subsequent forming gas anneal was performed, the island edges were left as bare silicon. This unpassivated surface could cause excessive leakage currents in the structure and adversely affect the measurements.

A previous study has shown that the use of a nitride cap (as compared to an oxide cap) on top of the silicon film during recrystallization results in a large fixed charge at the interface underneath the silicon film.[3] This was attributed to

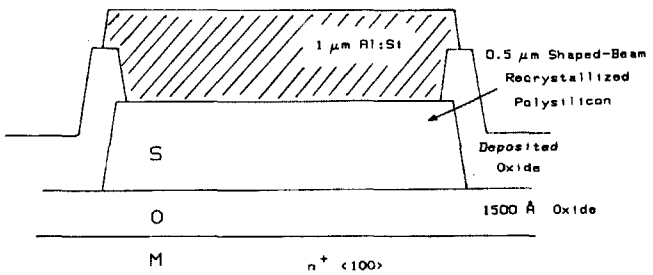

FIG. 1. Inverted MOS capacitor test structure. The recrystallized silicon film was uniformly doped with boron at a concentration of 3×10^{16} cm^{-3}.

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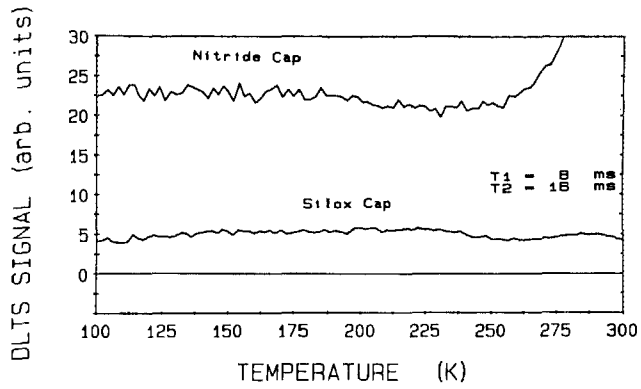

FIG. 2. DLTS spectra for samples recrystallized with a nitride cap and with a silox cap. Samples were annealed for one hour at 900 °C in nitrogen after recrystallization.

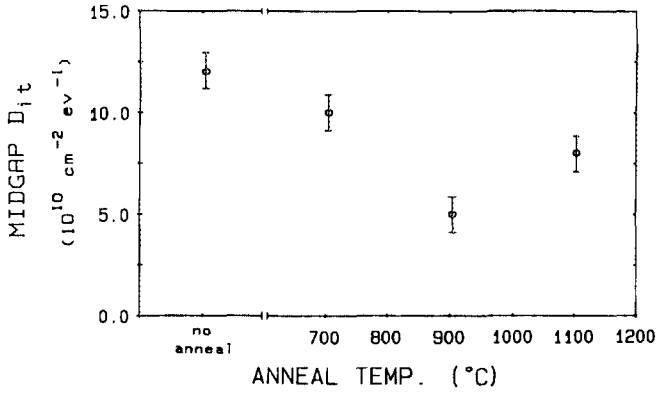

FIG. 3. Annealing behavior of interface state density for samples recrystallized with oxide caps. Anneals were performed in a nitrogen ambient for one hour.

the dissolution of several monolayers of the cap during recrystallization and subsequent segregation of the dissolved nitrogen to the back interface during solidification, leading to formation of an SiN_x layer at the back interface. This interfacial nitride causes the large fixed charge. We observed large interface state densities at the back interface in addition to the large fixed charges previously reported. In Fig. 2 are shown DLTS measurements of the underlying interface for samples processed identically except for the recrystallization cap. The emission signal at low temperatures corresponds to states near the valence-band edge while the signal at higher temperature measures states near midgap. The spectra have been normalized so that the plotted signal is proportional to interface state density. Note a continuum of states with no sharp peaks is observed, characteristic of an interface. (The rise in the signal above 250 K is due to minority-carrier effects and is not significant.) While the absolute determination of interface state densities from DLTS data is difficult,[4] the observed signal level for the nitride cap corresponds roughly to an interface state density of 7×10^{11} cm^{-2} eV^{-1}. *C-V* measurements confirmed a large and variable D_{it} for nitride caps. Before annealing, the midgap D_{it} ranged from 1×10^{11} to over 10×10^{11} cm^{-2} eV^{-1}. High-temperature annealing was found to reduce the interface state density, but a temperature of 1100 °C was necessary for significant improvement.

To avoid effects from an interfacial nitride, experiments were then performed using oxide caps during recrystallization. The midgap interface state density before and after annealing, as extracted from *C-V* measurements, is shown in Fig. 3. Note the observed densities are in the mid 10^{10} cm^{-2} eV^{-1} range, about an order of magnitude below those found with the nitride caps. It was found that the interface state density decreased with 1-h anneals in nitrogen at 700 and 900 °C, but that an 1100 °C anneal increased the state density (as well as the interface fixed charge) over that found from a 900 °C anneal. If interface states are reduced by a relaxation of interfacial stress and annealing of damage in the silicon layer, a further reduction of D_{it} at 1100 °C or at least no increase would be expected. However, it is known that nitrogen can diffuse from an ambient through silicon dioxide and degrade a conventional silicon-silicon dioxide interface.[5] Subsequent SIMS analysis performed on our samples showed a large amount of nitrogen at the back interface for anneals at 1100 °C (Fig. 4). It appears that nitrogen from the ambient diffused through the silicon film and was trapped at the back interface. The resulting interfacial nitride then caused an increase in the interface state density and fixed charge as it does when a nitrogen cap is used for recrystallization. Samples annealed at 1100 °C in oxygen instead of nitrogen did not exhibit an increase in D_{it}, consistent with the interfacial nitride explanation.

The effect of the underlying oxide has also been investigated. Dry thermal oxide with and without HCl in the oxidizing ambient (produced by bubbling oxygen through TCA), wet thermal oxide, and a densified deposited oxide were tried. A wet thermal oxide was found to yield a D_{it} of 9×10^{10} cm^{-2} eV^{-1}, roughly twice that for the other three oxides. The wet oxide was grown at a lower temperature than the dry oxides (1000 °C vs 1100 °C), but both temperatures are above 950 °C, the temperature above which silicon dioxide undergoes viscous flow to relieve stress.[6] Thus, the higher D_{it} for the wet oxide is probably not explained by stress in the oxide. The lowest observed interface state density of 4×10^{10} cm^{-2} eV^{-1} actually occurred with a densified deposited oxide as the underlying insulator. This is especially encouraging since in the only previous reported work with a deposited oxide (plasma CVD), a D_{it} of greater than 10^{12} cm^{-2} eV^{-1} was found.[2] Three-dimensional integration

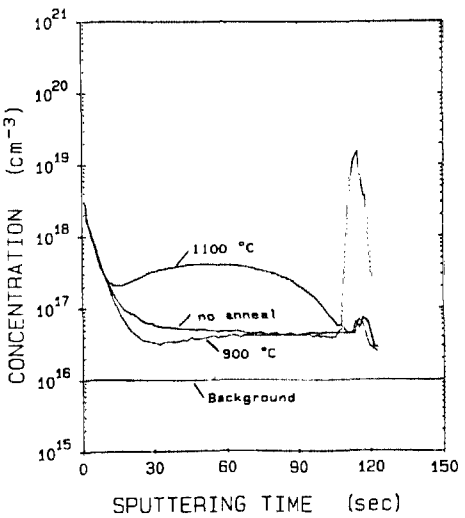

FIG. 4. SIMS data of nitrogen profiles for various anneals.

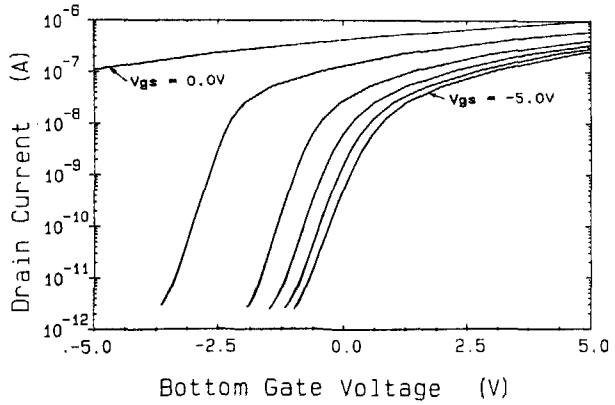

FIG. 5. Subthreshold I-V characteristics of a bottom channel MOS transistor. The source-drain voltage was 100 mV and the top gate voltage was varied from −5.0 to 0.0 V.

of integrated circuits depends on a deposited oxide to shield the underlying structure from the heat generated by laser recrystallization of the top polysilicon layer.

To further electrically examine the bottom interface, n-channel MOSFET's were fabricated in recrystallized films on a deposited oxide. An oxide cap was used during recrystallization. Underneath the deposited oxide was a heavily doped polysilicon layer which served as a bottom gate electrode to modulate the surface potential on the bottom of the recrystallized layer. The subthreshold behavior of the bottom channel MOSFET was investigated by measuring source-drain current while holding the top gate voltage fixed and sweeping the voltage of the bottom gate electrode (Fig. 5). (Note for a top gate voltage of 0 V the source-drain current was mostly in the top channel, and thus changing the bottom gate voltage had little effect.) Interface states cause an effective parasitic capacitance which reduces the coupling of the gate voltage to the silicon surface potential, thus reducing the subthreshold slope. The observed classic subthreshold curves indicate a well-behaved interface, and from the subthreshold slope the interface state density may be extracted.[7] From the data in Fig. 5, an interface state density of 6×10^{10} cm^{-2} eV^{-1} is found, in the same range as the state densities measured by the C-V technique.

In summary, the interface state density of the recrystallized silicon-underlying oxide interface has been investigated. Nitride caps for recrystallization and high-temperature anneals in nitrogen were found to have an adverse effect on the interface due to formation of an interfacial nitride layer. A good interface is possible with a deposited oxide as the underlying insulator, and an interface state density in the mid 10^{10} cm^{-2} eV^{-1} range is repeatably obtainable. This enables high quality MOSFET's to be made on the bottom of recrystallized films.

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Photoluminescence in PbTe-PbEuTeSe multiquantum wells

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Infrared photoluminescence has been studied in a thin (92 Å) PbTe-PbEuTeSe multiquantum well structure. The spectra show good agreement with calculations for the $n = 1$ quantum well transition for a simple two-dimensional electron-hole gas with low-energy broadening consistent with monolayer well width fluctuations. From the measured effective electron temperatures we estimate that the electron-longitudinal optical phonon interaction is significantly reduced in comparison with bulk PbTe.

Recently, the extension of molecular beam epitaxial (MBE) growth techniques to the IV-VI compounds has yielded high quality epitaxial films on PbTe, related ternary compounds, and very low threshold current diode lasers.[1] In particular, diode laser operation has been obtained in single quantum wells based on the $PbTe/Pb_{1-x}Eu_xTe_{1-y}Se_y$ heterojunction, with the PbTe well thicknesses down to 200 Å.[2] In this letter we discuss photoluminescence spectra ob-

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