A Seeded-Channel Silicon-on-Insulator (SOI) MOS Technology

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Abstract—**An improved silicon-on-insulator (SOI) MOSFET transistor structure is presented. The structure retains the density and low-capacitance advantages of SOI, but places the transistor channel region in the single-crystal silicon substrate. This "seeded-channel" configuration avoids floating-body effects and ensures that defects in the SOI will not affect the channel mobility. The technology has been used to successfully fabricate n-channel transistors.**

I. INTRODUCTION

A SILICON-ON-INSULATOR (SOI) MOSFET technology has several important density advantages over bulk silicon, particularly for CMOS circuits. These include: (1) the n^+ to p^+ space may be the lithographic minimum dimension, without the necessity of aligning a well edge inside the space, (2) contact windows may overlap the diffusion edge without substrate leakage problems, and (3) the shorted n^+ and p^+ diffusions of a CMOS inverter may be butted together, without the need for providing a field region in which to terminate the well edge.

The goal of much research in recent years has been to develop a technology for creating high-quality SOI films for these transistors. A common technique shared in these approaches, whether they be liquid-phase beam recrystallization of polysilicon, lateral vapor-phase epitaxial growth, or lateral solid-phase epitaxial growth, has been the use of seed holes to a single-crystal substrate to improve the quality of the SOI films [1]–[4]. In general the film quality is highest nearest the seed hole and degrades with increasing distance from the seed. The arrangement of such seed holes with a suitable spacing would be a complication in the layout of any real circuit. Another practical problem with SOI MOSFET's is the lack of a substrate contact. The resulting floating body causes the "kink" effect [5] and can affect high-speed device performance [6], [7].

We have developed an improved SOI device structure which overcomes these two problems (Fig. 1). The source and drain regions are left in SOI for density advantages and low capacitance, but the channel region is placed directly above a hole in the underlying oxide. Because the channel is in a region directly above a seed hole to the substrate, the silicon quality in the channel region should be high. By achieving only minimal lateral overgrowth from the seed hole (~ 1 μm), the source and drain junctions will still remain on top of the underlying oxide in case of any small misalignment of the gate region from the seed hole. Any defects (such as grain boundaries) in the film on the oxide away from the seed hole will not significantly affect the device performance since these areas serve only as source or drain regions or are removed during the isolation step. Floating body effects are eliminated since the channel now has a direct connection to the substate. The structure could be fabricated by any of the SOI techniques mentioned earlier.

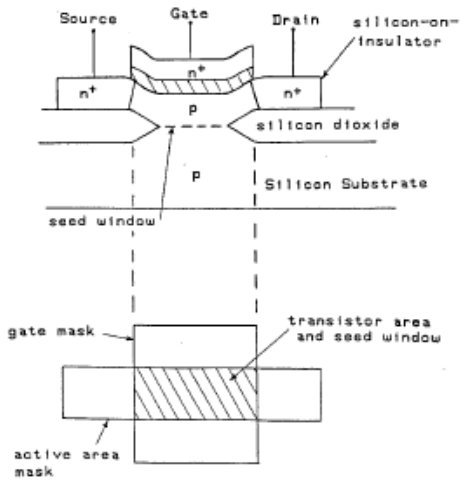

Fig. 1. Cross section and top view of the seeded-channel SOI transistor. The SOI layers in our experiments were formed by laser recrystallization of deposited polysilicon.

The seed hole area can be obtained by the simple intersection of the conventional "active area" and "gate" mask regions (Fig. 1). No special layout considerations are required. By using the existing mask databases to create a new seed hole mask, the structure should be adaptable to all existing MOS mask sets.

It should be noted that a similar buried oxide structure (BOMOS) has previously been reported [8], [9]. However, this structure used conventional epitaxial growth with no lateral growth to create the channel region and yielded polysilicon on top of the buried oxide. Hence the seed window needed to be slightly larger than the source–drain spacing to ensure that the channel region was in single-crystal silicon. This increased window size would place the source–drain junctions in the substrate and reduce the CMOS layout density advantages described earlier.

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II. Experimental Procedure

The starting materials for fabrication of the test devices were ⟨100⟩ 50 Ω·cm p-type silicon wafers. A field oxide 400-nm thick was grown by local oxidation to create seed holes. A combination of the "gate" and "active area" masks of a standard NMOS circuit were used to define the hole areas. LPCVD polysilion (0.4 μm) and an oxide anti-reflection cap were then deposited and densified to arrive at the structure shown in Fig. 2.

The polysilicon was then recrystallized using a scanning argon ion laser with the beam shaped to an elliptical spot of about 200 × 15 μm^2. The substrate was preheated to 450°C. The scan speed was 10 cm/s and adjacent scan lines were overlapped by ~50 percent. The laser power of 12 W was sufficient to melt down to the original silicon substrate in the seed windows. Melting completely through the polysilicon is necessary for the single-crystal substrate to act as a seed during the resolidificaton. The occasional grain-boundary defects in the recrystallzied film, as revealed by a defect etch, were confined to the areas over the oxide. The seed window areas (future channel regions) were free of such defects. Mass transport during the recrystallization was initially observed but was eliminated by proper annealing of the deposited oxide cap.

After the recrystallization, the anti-reflection cap was removed by wet chemical etching. A conventional NMOS process (gate oxide thickness ~40 nm) with a modified isolation step was then used to fabricate the transistors. Care was taken to align the transistors directly over the seed holes. Both enhancement and depletion transistors as well as devices without any enhancement or depletion implant were fabricated. Control devices were fabricated simultaneously in conventional substrates.

III. Results

Capacitance–voltage measurements were performed on a *C–V* structure in a large seed window. In regions both with and without the enhancement implant, the measurements indicated an excessively large p-type dopant concentration in the substrate. For example, in regions with the enhancement implant, the experimental wafers showed a doping level of about 1 × 10^{17} cm^{-3}, compared to 3 × 10^{16} cm^{-3} in a control wafer. Further experiments and spreading resistance measurements revealed that the "undoped" oxide cap contained a large boron concentration. (The deposition reactor was peviously used for boron-doped oxides). It it believed that this boron was the source of the doping in the recrystallized films.

The transistors exhibited well-behaved curve-tracer characteistics. The performance of a device with a 2-μm channel length is shown in Fig. 3. No "kink" effect was observed, as expected because of the substrate contact. The threshold voltages of all of the experimental transistors (enhancement, depletion, and W-devices) ranged from 0.4 to 1.5 V, more positive than found in the control devices. The magnitude and direction of the shift is consistent with the excess p-type channel doping in the experimental devices.

The surface mobilities extracted from long-channel (50-μm) enhancement devices were about 25 percent lower than those found in the control transistors. This difference is also

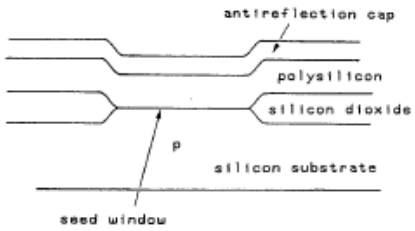

Fig. 2. Seeded SOI structure before laser recrystallization and transistor fabrication.

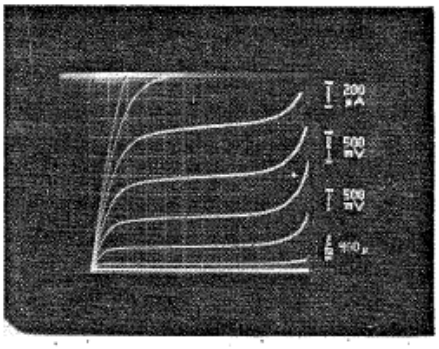

Fig. 3. Curve-tracer characteristics for an enhancement device with W = 50 μm and L = 2 μm.

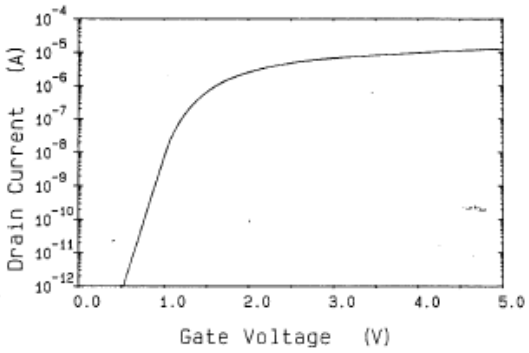

Fig. 4. Low current behavior of an enhancement device with a channel length of 50 μm. The drain voltage was 0.1 V and the source and substrate were grounded.

believed to be caused by the excess channel doping. (The increased vertical field accompanying higher channel doping causes extra scattering to degrade the surface mobility [10].) According to [10], an increase in channel concentration from 3 × 10^{16} cm^{-3} to 1 × 10^{17} cm^{-3} will degrade electron surface mobility by 15 percent, accounting for a majority of the mobility degradation seen. A more direct comparison may be made by comparing the unimplanted experimental transistors with the control enhancement transistors. These devices had similar threshold voltages (0.9 V ± 0.1 V and 1.1 V, respectively), indicating similar channel doping and similar required vertical fields. The average surface mobility of the unimplanted experimental devices was some 10 percent lower than that of the enhancement control devices (564 versus 630 $cm^2/V \cdot s$). The reason for this 10 percent mobility reduction is not known.

The low current characteristics of the devices were also well-behaved (Fig. 4) with a subthreshold slope of 120 mV/

decade seen on the enhancement devices. Although no yield analysis or detailed measurements were performed, leakage currents on large geometry devices with a source–drain voltage of 100 mV were found to be in the range of 1 pA.

Many source–drain shorts were observed in devices with channel lengths under two microns. This is believed due to the channel regions not being perfectly aligned with the seed holes. Grain boundaries do exist in the recrystallized polysilicon on oxide, and excessive diffusion of the source–drain dopant would occur if a grain boundary were present in the channel region of a transistor [11].

IV. Summary

A new SOI transistor structure with a seeded channel region has been presented. The configuration retains the density and speed advantages of SOI but eliminates floating substrate effects and layout problems caused by conventional SOI seeding techniques. The structure should be easily adaptable to all existing MOS circuits. Because of the reduced source-substrate junction area compared to conventional substrate transistors, a CMOS process made with such a structure should be very latch-up resistant.

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