An EEG Acquisition and Biomarker-Extraction System Using Low-Noise-Amplifier and Compressive-Sensing Circuits Based on Flexible, Thin-Film Electronics

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***Abstract*— This paper presents an electroencephalogram (EEG) acquisition and biomarker-extraction system based on flexible, thin-film electronics. There exist commercial, single-use, flexible, pre-gelled electrode arrays; however, these are fully passive, requiring cabling to transfer sensitive, low-amplitude signals to external electronics for readout and processing. This work presents an active EEG acquisition system on flex, based on amorphous silicon (a-Si) thin-film transistors (TFTs). The system incorporates embedded chopper-stabilized a-Si TFT low-noise amplifiers, to enhance signal integrity, and a-Si TFT compressive-sensing scanning circuits, to enable reduction of EEG data from many channels onto a single interface, for subsequent processing by a CMOS IC. Further, the system uses an algorithm, by which spectral-energy features, a key EEG biomarker, are extracted directly from the compressed signals. We demonstrate a prototype, performing EEG acquisition from a human subject, and compressed EEG reconstruction and seizure detection via analog replay of patient data. The TFT amplifier achieves a noise PSD of 230 nV/$\sqrt{}$Hz. Seizure detection, at up to 64× compression, achieves error rates <8%. Reconstruction is demonstrated at up to 8× compression.**

***Index Terms*— Amorphous silicon (a-Si), chopper stabilization, compressive sensing, flexible electronics, seizure detection, thin-film transistor (TFT).**

I. Introduction

ELECTROENCEPHALOGRAMS (EEGs) are electrical signals that originate in the brain, but which can be measured on the surface of the scalp. The non-invasive nature of EEG acquisition makes it a useful sensing modality for many medical applications. However, EEG acquisition systems today are limited by a number of critical factors. A typical EEG array consists of 20 or more electrodes, in many cases over a hundred. The first challenge is that a trained technician is needed to ensure proper electrode placement. The second challenge is that the large amount of cabling involved can cause patient discomfort, especially during long-term recording (e.g., required to diagnose sleep disorders, to perform preoperative planning to map seizure foci in epilepsy patients, etc.). The third challenge is that this cabling, distributed over the scalp, impacts mechanical stability, causing motion artifacts during EEG recording.

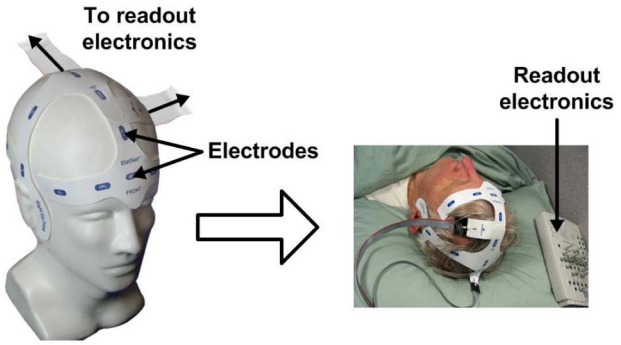

Fig. 1. StatNet system: a flexible, single-use, pre-gelled EEG electrode array [1].

There have been many efforts, and in fact significant progress, in addressing these challenges. For example, Fig. 1 shows a flexible EEG electrode array from HydroDot called StatNet [1]. By integrating all the electrodes into a single unit, the electrode positions are fixed, substantially easing their placement. The electrodes are also pre-gelled, significantly facilitating electrode/skin preparation. As well, these arrays are single-use, which reduces the risk of infection, a major concern with traditional multi-use arrays. Thus, this system addresses many of the previously described challenges. However, such systems are fully passive, requiring substantial cabling to convey sensitive signals to external readout electronics, which degrades robustness and patient comfort.

To address this limitation, this work introduces active circuitry into the flexible electrode array for instrumentation and ultimately processing of the EEG signals. Such a system requires a technology that can implement flexible, active electronics. A first option is to transfer crystalline silicon islands,

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from a wafer, onto flexible substrates. This has been demonstrated in an implanted electrocorticogram (ECoG) array [2]. A challenge that arises is that transfer printing involves several fairly complex fabrication steps, based on wafers that are generally small. While this is viable for an implanted ECoG system where the focus is high-resolution sensing, but over a small area, it is limiting for an EEG array where a large area (i.e., over the entire scalp) is needed. A second option is to use large-area electronics (LAE), which involves low-temperature processing of thin-film devices directly onto large ($\sim$ m^2), flexible substrates. Thus, it possible to directly pattern active circuitry onto multiple flexible electrode arrays at once, enabling scalable fabrication and a high level of flexibility (e.g., transistor parameters are characterized in [3] with respect to bending radius).

In this paper, we present an EEG acquisition system to support hybrid LAE-CMOS integration, where flexible LAE sheets integrate amplifiers and compressive-sensing circuits, such that the resulting compressed signals may be transmitted for processing to a CMOS IC via a single interface [4] (typically achieved by electrical wire bonding to the flexible substrate at a location of reduced bending [5]). Of particular interest for processing is the extraction of spectral-energy features, a key biomarker in the EEG, directly on the compressed signals, since sparse reconstruction following compressive sensing is computationally intensive for an embedded IC. Section II describes the system-level design considerations, including motivation for adopting a hybrid architecture. Section III describes, in detail, the implementation and design of the various sub-blocks which comprise the system. Section IV presents the system prototype and demonstrates performance through EEG acquisition from a human subject as well as EEG amplification, reconstruction, and seizure detection from analog replay of data from an epileptic patient. Finally, Section V provides conclusions.

II. System Architecture

To achieve flexible form-factor sensing along with active functionality for signal acquisition and ultimately processing, we focus on a hybrid system architecture, combining LAE with silicon CMOS [6]. This is because, while LAE offers specific advantages, the low-temperature processing involved also leads to low-performance active devices, such as thin-film transistors (TFTs). For example, the workhorse LAE technology used commercially today in the flat-panel display industry is amorphous-silicon (a-Si). Low-temperature processing results in low electron mobility ($\sim$1 cm^2/Vs), and even lower hole mobility ($\sim$0.05 cm^2/Vs). In fact, while NMOS TFTs have low performance, PMOS TFTs are practically inviable. Low-temperature processing also results in reduced gate-dielectric quality, and thus limited gate-stack scalability. Finally, to margin against expansion/contraction of thin-films during processing, increased TFT overlap regions are required (e.g., gate-drain/-source overlaps), leading to large device capacitances. The net effect is a large required supply voltage for adequate drive currents (elevating energy) and a maximum unity-current-gain frequency, f_T, that is limited

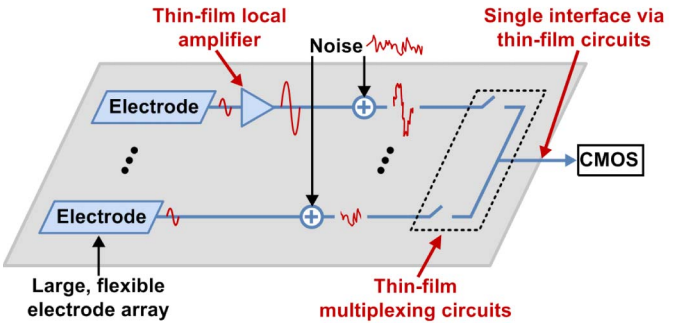

Fig. 2. Amplifiers and multiplexing circuitry must be implemented in LAE for improved SNR and reduced interfacing complexity.

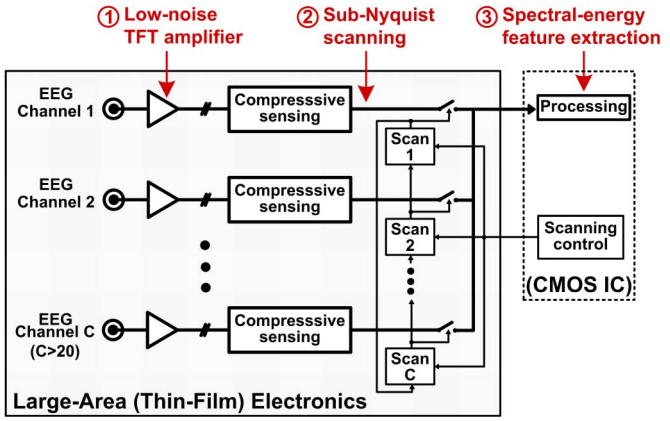

Fig. 3. System architecture for the EEG acquisition and biomarker-extraction system, where LAE circuits interface with an eventual CMOS IC.

to about 1 MHz. By comparison, crystalline silicon CMOS transistors have approximately an order of magnitude lower supply voltage and five orders of magnitude higher f_T.

Because of this disparity in performance, hybrid systems aim to move as much of the complex functionality into the CMOS domain as possible. However, there remain a few critical functionalities that must be implemented in the LAE domain (Fig. 2). First, EEG acquisition requires the electrodes to be distributed over a large area (i.e., over the scalp), whereas the CMOS IC is centralized. As such, the interconnections between the electrodes and the CMOS IC are susceptible to noise. This motivates the placement of amplifiers as close as possible to the electrodes, to maximize the SNR of the EEG signals. Thus, the amplifiers are implemented using LAE TFTs. Second, EEG acquisition often requires many distributed electrodes. However, integration of a CMOS IC is limited by the number of interconnections required (size, cost, robustness). This motivates multiplexing circuitry to reduce all the connections to a single interface. Thus, the multiplexing circuitry is implemented using LAE TFTs. Due to the lower performance and energy efficiency of TFTs, the formation of these components comes with energy and speed limitations, which must be analyzed and addressed. This is the focus of Section III-A.1 and Section III-B, respectively.

Based on the desire for these specific components in the LAE domain, Fig. 3 shows the architecture of the presented EEG acquisition and feature-extraction system. The hybrid

TABLE I

EXTRACTED 1/f-NOISE K PARAMETERS FOR THIN-FILM TECHNOLOGIES [9] AND 130 nm SILICON-CMOS [6]

	a-Si	DNTT (organic)	ZnO	130 nm Si-CMOS
K [V^2F]	3×10^{-21}	1×10^{-20}	5×10^{-21}	1×10^{-24}

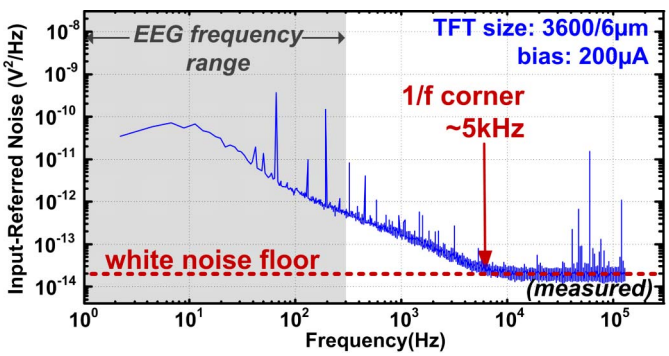

Fig. 4. Measured noise PSD of an a-Si TFT amplifier.

system consists of three key components:

1) TFT-based chopper-stabilized low-noise amplifiers located near the electrodes to enhance the SNR of the EEG signals.
2) TFT-based multiplexing circuitry to reduce all of the EEG signals onto a single interface to ease connection to an embedded IC. This is done via compressive-sensing acquisition, which allows for sub-Nyquist sampling of the electrode channels.
3) An algorithm to extract features of the EEG directly from the compressed signal, in the CMOS domain.

III. SYSTEM IMPLEMENTATION

This section describes the details of the three components of the system.

A. TFT Low-Noise Amplifiers

The main challenge in building TFT low-noise amplifiers is that TFTs exhibit high 1/f noise. In particular, this noise falls directly in the band of interest for EEG signals, which generally have very low amplitudes (i.e., 10–100 μV). While 1/f noise poses a key limitation for EEG acquisition even with silicon-CMOS amplifiers [7], [8], the situation is worse with TFTs, as low-temperature processing leads to high carrier-trap densities in the semiconductor and semiconductor-dielectric interface [9]. Indeed, the value of process-dependent parameter K (with drain-current power-spectral density (PSD): $I^2_{1/f} = K/(C_iWLf)\times g^2_m$) for a-Si is about 3 orders of magnitude higher than that of silicon CMOS (Table I) [6], [9]. Fig. 4 shows the measured input-referred noise PSD from a resistively loaded differential-pair TFT amplifier with tail biasing of 200 μA.

A standard method used to decrease 1/f noise in transistors is to increase the gate area (i.e., width and length). Indeed, TFTs exhibit the expected decreased 1/f noise with increased area [Fig. 5(a)]. However, as mentioned in Section II, low-temperature deposition results in reduced gate-dielectric quality, leaving it susceptible to pinholes. Therefore, as we increase the area, the likelihood of TFT failure also increases [Fig. 5(b)]. Thus, the extent to which area upsizing can address 1/f noise is limited in TFTs.

An alternative is to use a chopper-stabilized amplifier topology [10]. Chopper stabilization is a technique whereby we first up-modulate the signal to a band not limited by the 1/f noise. Amplification is performed in this frequency band, with reduced susceptibility to 1/f noise. Following amplification, down-modulation of the amplified signal brings it back to its original frequency. The difficulty with using this topology is that it requires the amplifier to operate at higher frequencies. Thus, the first step is to analyze the feasibility of performing chopper stabilization despite the reduced performance of low-temperature-processed TFTs.

1) Feasibility of Chopper-Stabilized TFT Amplifiers: Using Fig. 4 as an example of the noise PSD for a-Si TFT amplifiers, for the given biasing, the 1/f noise corner is $\approx$ 5 kHz. To viably perform the up-modulation needed in chopper stabilization, the TFTs need to operate with an f_T at least an order of magnitude higher (i.e., $f_T \geq 50$ kHz). It has been previously experimentally shown that with gate-overdrive biasing, our a-Si TFTs can achieve f_T's of $\approx$ 1 MHz [11]. Thus, chopper-stabilized TFT amplifiers can be implemented. However, operating transistors at a higher f_T, and thus a higher gate-overdrive biasing, impacts power efficiency.

To analyze power efficiency, we use the metric of transconductance efficiency (g_m/I_D) versus f_T (Fig. 6). Achieving higher f_T requires increased gate-overdrive biasing on the transistor. For f_T's required, a silicon-CMOS transistor could remain in sub-threshold where the g_m/I_D is at a maximum. We do point out that unlike silicon-CMOS transistors, a-Si TFTs do not have constant g_m/I_D in sub-threshold due to a non-constant sub-threshold slope. This is because in most amorphous semiconductors, below the edge of the conduction band, there exist trap states whose density increases exponentially as their energy approaches the conduction band edge [12]. Thus, as the gate voltage increases in sub-threshold, an increasingly higher fraction of the added electrons go into the trap states and do not contribute to current, thus degrading the sub-threshold slope. However, for the f_T's required, the a-Si TFTs require biasing far above threshold, incurring a more significant degradation in g_m/I_D. Thus, an important consideration is how much degradation in g_m/I_D is incurred as a result of employing localized, flexible TFT-based amplifiers instead of silicon-CMOS amplifiers. As shown in Fig. 6, for an f_T of 50 kHz (i.e., for signal up-modulation beyond the 5 kHz 1/f noise corner), the g_m/I_D for an a-Si TFT is found to be within a factor of 20 of that for a silicon-CMOS transistor. We expect this value to improve as we move towards higher-performance materials.

Analysis of higher-performance materials.

In this work, we focus on a-Si TFTs due to their relative prominence in other commercial applications and greater maturity in terms of systems demonstrations. However, with the introduction of higher-performance materials, such as

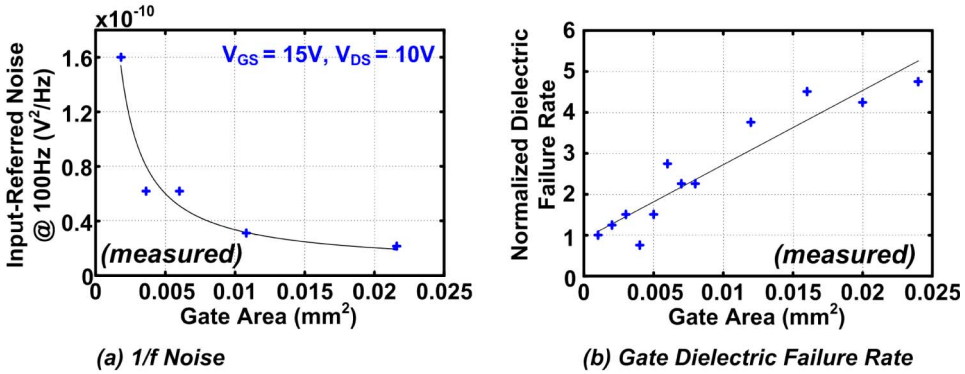

Fig. 5. Effect of TFT sizing (i.e., gate width and length) on (a) 1/f noise, and (b) rate of gate-dielectric failure.

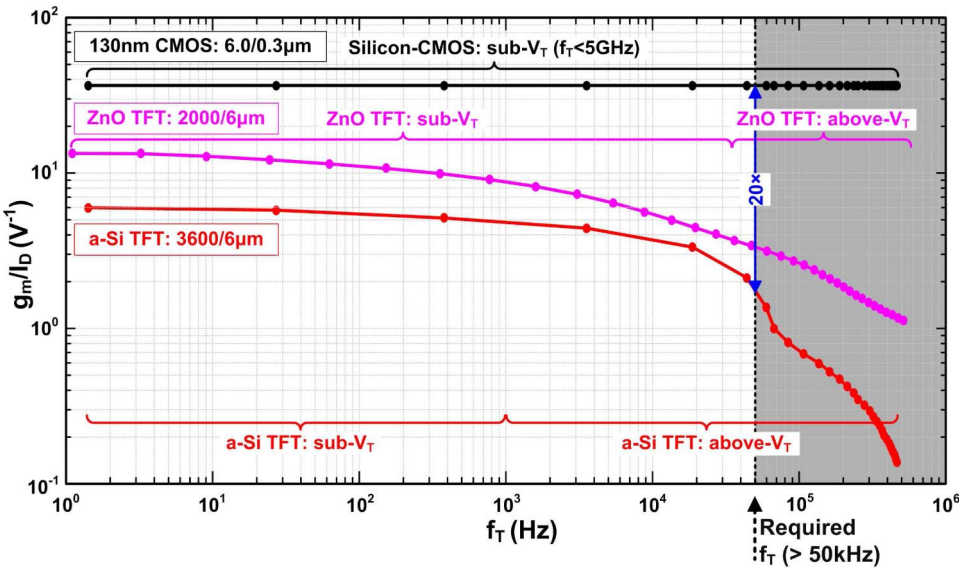

Fig. 6. g_m/I_D versus f_T for an amorphous-silicon TFT, a zinc oxide TFT, and a silicon-CMOS transistor.

metal oxides, we also provide analysis of how such technologies would impact low-noise-amplifier design. Specifically, we focus on zinc-oxide (ZnO) TFTs fabricated in our lab using plasma-enhanced atomic layer deposition (PEALD), as described in [13] (achieving performance similar to that typically reported, e.g., [14]). To compare a-Si versus ZnO, we focus on three areas, which pertain to our system, and specifically to low-noise chopper-stabilized amplifiers:

1) **Noise:** From Table I, we see that the K-values are similar across both technologies [9]. Thus, both technologies are similarly limited by the 1/f noise characteristics mentioned above.
2) $\mathbf{g_m/I_D}$: Fig. 6 shows the g_m/I_D versus f_T. As expected, the ZnO TFTs exhibit superior g_m/I_D compared to the a-Si TFTs, both in the sub-threshold and above-threshold regions. This is due to steeper sub-threshold slope and higher electron mobility, respectively. However, as observed in Fig. 6, the effect of non-constant sub-threshold slope due to trap states (which causes non-constant g_m/I_D) is more prominent in the ZnO TFTs than in the a-Si TFTs (as described in [15]). As a result, for the particular f_T focused on in this work, the improvement in g_m/I_D is more modest than for other f_T's; nonetheless, the ZnO TFTs show significant promise for improving g_m/I_D.
3) **Supply voltage:** An advantage of moving to a technology such as ZnO, is that the high electron mobility (~10–20 cm^2/Vs) allows us to achieve a higher f_T at a lower gate-overdrive voltage. This enables an overall reduction in the required supply voltage, having a further benefit on power efficiency.

While these comparisons between ZnO and a-Si TFTs are based on devices fabricated in-house with specific processes, we believe that the overall trends suggest that future work integrating higher-performance technologies, such as ZnO, represents a promising step forward.

2) Chopper-Stabilized TFT Amplifier Implementation: Fig. 7 shows the circuit schematic, including sizing, of the chopper-stabilized TFT amplifier employed in the system. The input EEG signal is AC-coupled before the input chopper. The amplifier stage itself is a standard differential pair. For testability the tail biasing of the two branches is separated by coupling the sources of the input pair through a large 20 nF capacitor. At AC frequencies of interest the capacitor

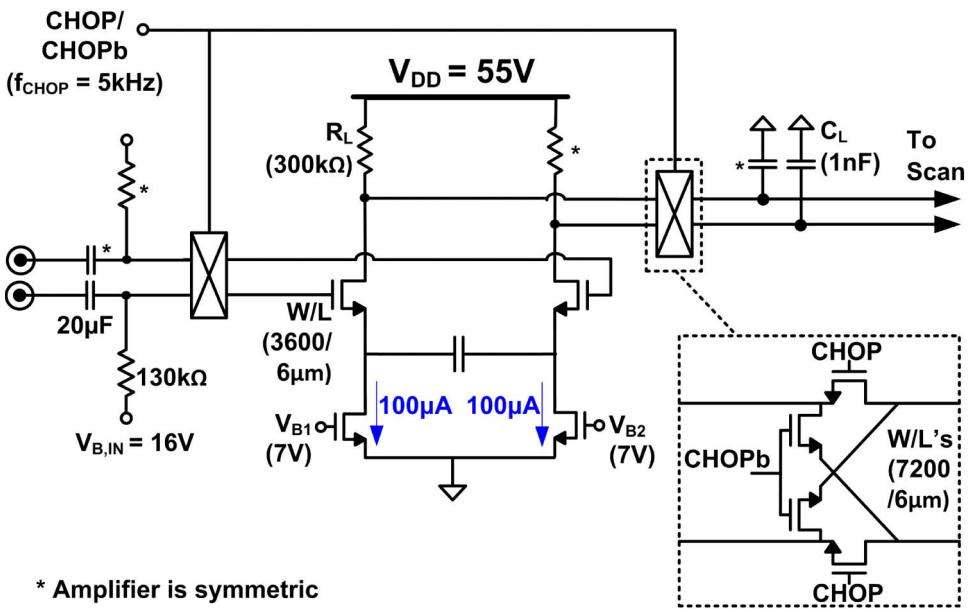

Fig. 7. Chopper-stabilized TFT low-noise amplifier circuit.

behaves as a short; at DC this enables different biasing of each branch to explore the effects of input-pair mismatch. We point out, that all measurements and analysis presented use the same gate-biasing on the tail devices of the two branches, eliminating the need for the coupling capacitor, effectively reducing the topology to a standard differential pair. Following output chopping, the signal is fed through a single-pole filter formed by the load capacitors. These give a –3 dB frequency of 500 Hz to filter chopping artifacts. The inset in Fig. 7 shows the chopper circuit, which consists of NMOS TFT switches that are fed with a 5 kHz chopping frequency chopping signal, having a voltage swing of 36 V. This is a typical swing voltage used to generate the required TFT drive current (i.e., 8.4 kΩ on-resistance), and is provided from the CMOS domain through a TFT level shifter [16].

A large input capacitor for AC coupling is used, since the input chopper combines with the input capacitance of the differential pair, to form switched-capacitor resistors, whose total value (to small-signal ground) is given by:

$$R_{SC} = \frac{1}{2\pi f_{CHOP} \times C_G}, \tag{1}$$

where f_{CHOP} is the chopping frequency, and C_G is the gate capacitance of each input device in the differential pair. For the low high-pass cut-off frequencies needed for AC coupling EEG signals ($\approx$0.06 Hz), R_{SC} determines the minimum input capacitance required ($\approx$2 μF for f_{CHOP} = 5 kHz). Thus, to maximize R_{SC} for a given chopping frequency (determined by the 1/f corner), a small C_G is desired. This can be achieved by reducing the transistor width; however, this requires higher gate-overdrive biasing for a given g_m, resulting in lower g_m/I_D. Thus, required input capacitance size raises an additional trade-off with g_m/I_D, which is again related to f_T (i.e., large device capacitance for a given g_m), and poses a challenge for TFT implementations. However, previous work has shown that there is significant scope for reducing the TFT capacitance through device-level enhancements. For instance, the implemented TFTs use a standard 10 μm gate-source/-drain overlap, with a capacitance of 1.67 fF/μm; alternatively, self-aligned processing yields significantly lower overlap ($\approx$1 μm), with a capacitance of 0.44 fF/μm [17]. With regards to interfacing with surface-EEG electrodes, the resulting R_{SC} is orders of magnitude higher than the typical electrode series resistance, and the chosen input capacitance is on the order of the typical electrode series capacitance [18], ensuring adequate electrode drive capability.

B. TFT Scanning for Compressive-Sensing Acquisition

The EEG channels are multiplexed, using the TFT-based scanning circuit shown in Fig. 8 [16]. Three input signals from a CMOS IC are fed into TFT level converters to generate higher voltage swings for a two-phase clock (CLK/CLKb) and a global reset signal (GRST), required for TFT scan block operation. The scan blocks then generate sequential enable signals allowing us to access the electrode signals one at a time via a single output interface.

1) TFT Scan Blocks: Each block receives an input signal CIN, from the previous block, and a RST signal from the subsequent block. Running through a scanning sequence once ensures a condition where CIN is low and RST is high. This causes node X to be high and EN[N] to be low, remaining in this state with no static power consumption via charge stored on C_{int}. During a subsequent scan, when the previous block is enabled and its clock signal is high, CIN of the current block rises, causing C_{int} to be discharged. Next, when the previous block's clock signal transitions low, CIN is deasserted, causing node X and EN[N] to rise (via coupling through C_{int}). This causes the current block to be enabled, at the same time asserting RST of the previous block.

The speed of the scanning block is limited by a critical time constant set by the load resistor R_L and output capacitor C_{int}. We first note that with the absence of PMOS transistors, the

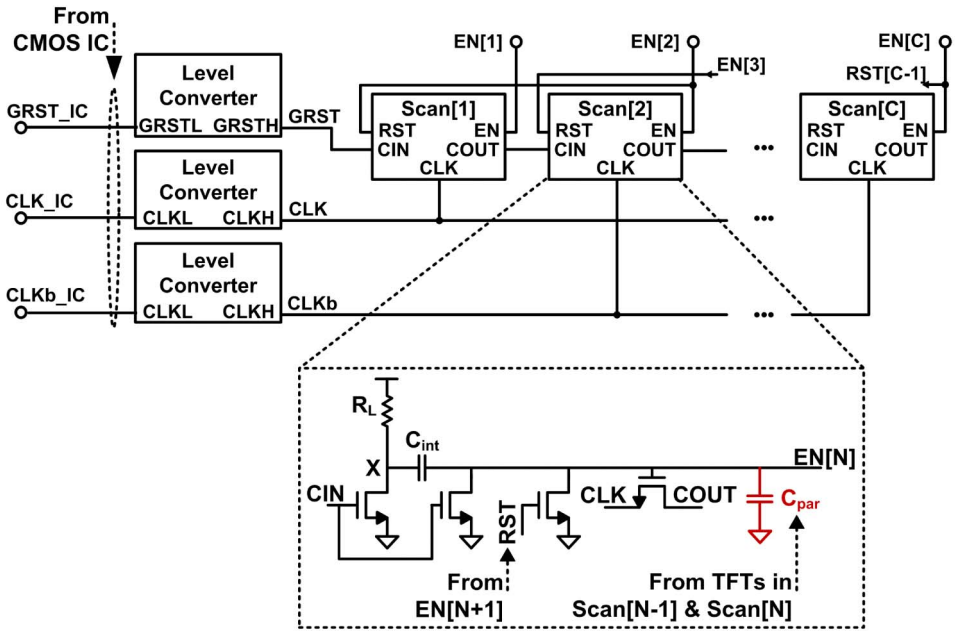

Fig. 8. TFT scanning circuit [16].

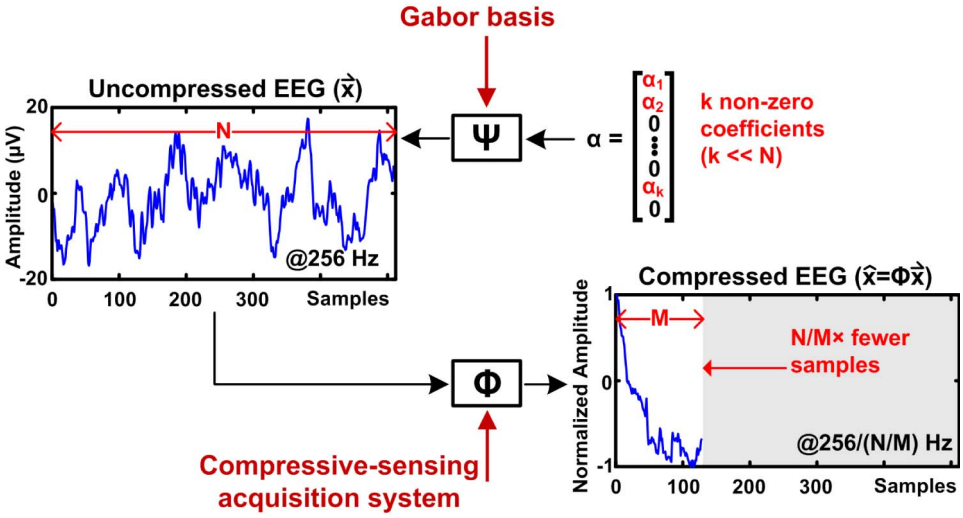

Fig. 9. Application of compressive sensing for EEG acquisition at a sub-Nyquist rate.

scan block relies on pseudo-NMOS inverter stage for charging and discharging node X. Thus, for adequate swing, R_L must large with respect to the on resistance of the stage's TFT. On the other hand, when node X rises, the enable signal EN[N] is raised through a capacitor divider formed by C_{int} and the parasitic load capacitances of subsequent TFTs. As such, C_{int} must be sized to be significantly larger than the TFT parasitic capacitances. Therefore, both R_L and C_{int} are set by the TFT. For a-Si TFTs, this time constant limits the scanning speed to about 10 kHz, which has implications for EEG acquisition. While the EEG signals themselves have a bandwidth of about 300 Hz, after passive single-pole filtering of each channel, a bandwidth of 2 kHz is required for robust Nyquist sampling. This would limit the number of channels in the system to less than 5.

2) Compressive-Sensing Acquisition: To overcome the TFT scanning-circuit speed limitation, an algorithmic approach is employed. Compressive sensing is an approach that allows us to acquire a signal using samples taken at a rate potentially much lower than the Nyquist rate. This is possible if the signal can be represented in some transform domain, where it exhibits sparsity [19]. For example, EEG is known to be sparse in the Gabor basis (labeled Ψ), which is a time-frequency basis [20]. This means that taking the Gabor transform of an EEG signal, the majority of the transform coefficients α_i would be zero (Fig. 9). According to compressive sensing theory, we can sample at a rate related to the number of non-zero coefficients k in this sparse basis, rather than the Nyquist rate [19]. Moreover, there is no need to explicitly transform a signal into its sparse basis. Rather, we can instead

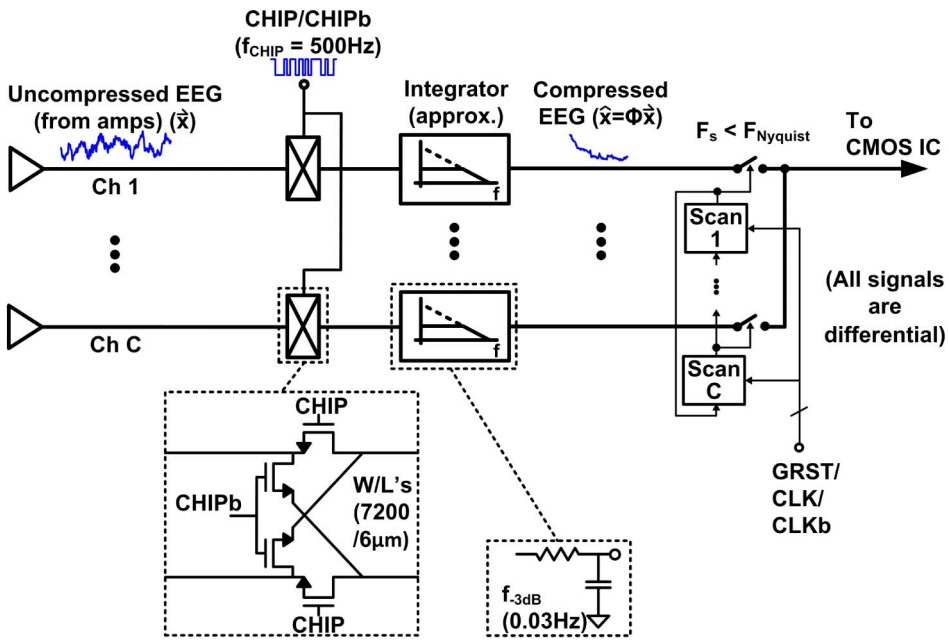

Fig. 10. Compressive-sensing acquisition circuits based on TFTs for sub-Nyquist scanning.

take a small number of random measurements (represented as multiplication of a vector of N EEG samples by an M × N matrix Φ, where M ≪ N) as long as these are incoherent with the sparse basis (more precisely, ΦΨ must satisfy the Restricted Isometry Property, RIP) [19], [21].

Fig. 10 shows the sub-Nyquist scanning circuit used in the system, which uses a compressive-sensing based architecture [22]. The theory of compressive sensing is developed for discrete time signals; however, for continuous time EEG signals, this architecture exploits the fact that filtering corresponds to a convolution operation. Thus, modulation by a random chipping sequence, followed by low-pass filtering and sampling below the Nyquist rate, corresponds to multiplication of Nyquist input samples, represented as a vector $\vec{x}$, by a random matrix Φ, yielding a lower-dimensional vector $\hat{x}$ [22]. With high probability, such a matrix Φ satisfies RIP with any time-frequency basis (i.e., Gabor basis) [23]. Thus, the architecture performs compressive sensing. The inset of Fig. 10 illustrates the implementation of the modulator circuit, which is similar to how modulation is performed in the chopper-stabilized amplifier (Fig. 7), but instead it is fed a pseudorandom ±1, 500 Hz chipping sequence, which would come from a CMOS IC. This is followed by a low-pass single-pole filter with a low cutoff frequency (≈0.03 Hz) to approximate integration.

Compressive sensing states it is possible to reconstruct the original signal $\vec{x}$ from $\hat{x}$ [19]. Namely, expressing the EEG as its Gabor transform ($\vec{x} = \Psi\vec{\alpha}$), we can represent $\hat{x}$ as follows:

$$\hat{x} = \Phi\Psi\vec{\alpha} = V\vec{\alpha} \tag{2}$$

where $V \equiv \Phi\Psi$. Reconstruction then involves finding a sparse solution for $\vec{\alpha}$, which is usually done through l1-norm minimization. However, l1-norm minimization is computationally intensive for an embedded CMOS IC [24]. Thus, we employ a method from which features of the EEG, namely the spectral-energy distribution, can be extracted directly from the compressed signals, without the need for complete reconstruction.

C. Spectral-Energy Feature Extraction

Spectral-energy extraction is performed by first feeding the EEG signal $\vec{x}$ through a transformation H corresponding to band-pass filtering:

$$\vec{y} = H\vec{x} = H\Psi\vec{\alpha}. \tag{3}$$

After this, the output $\vec{y}$ can be used to derive the energy, by taking the vector's inner product with itself:

$$\text{Energy} = ||\vec{y}||_2^2 = \vec{x}^{\mathsf{T}} H^{\mathsf{T}} H\vec{x}. \tag{4}$$

However, we only have access to the compressed signal $\hat{x}$, rather than the original signal $\vec{x}$ or its sparse representation $\vec{\alpha}$. Further, for the feature extraction above, we do not require a sparse solution (as needed for reconstruction), and thus we do not require l1-norm minimization. As an alternative, we explore the use of l2-norm minimization, noting that this is much simpler, leading to a linear estimator E of $\vec{x}$ (i.e., $\vec{x} \approx E\hat{x}$), with the following analytical expression:

$$E = \Phi^{\mathsf{T}}(\Phi\Phi^{\mathsf{T}})^{-1}. \tag{5}$$

Now, the targeted spectral-energy feature is calculated as follows:

$$\text{Energy} = ||\vec{y}||_2^2 \approx ||HE\hat{x}||_2^2 = \vec{x}^{\mathsf{T}}\Phi^{\mathsf{T}}E^{\mathsf{T}}H^{\mathsf{T}}HE\Phi\vec{x}. \tag{6}$$

We note from (5), that with Φ being a random matrix, E will also exhibit properties of a random matrix. Namely, when a matrix has entries that are uncorrelated and zero mean, its inner product with itself approaches the identity matrix [25], [26]. The importance of this property for our

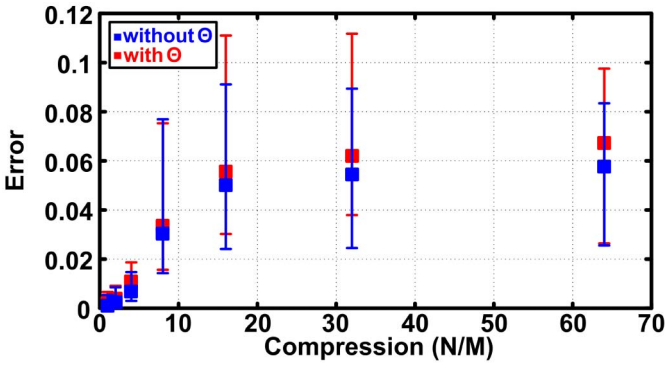

Fig. 11. Error between energy derived from the ideal $\vec{y}$ and energy derived from the estimated $\vec{y}$ across 10k $\vec{\alpha}$ with elements derived from a uniform random variable, versus compression rate. The error bars show min/max values across 8 different band-pass filter transformations H, which will be used later for seizure detection.

formulation is first shown considering energy estimation of an unfiltered signal:

$$\text{Energy} = ||\vec{x}||_2^2 \approx ||E\hat{x}||_2^2 \approx \vec{x}^{\mathsf{T}}\Phi^{\mathsf{T}}E^{\mathsf{T}}E\Phi\vec{x}. \tag{7}$$

With $E^{\mathsf{T}}E$ and $\Phi^{\mathsf{T}}\Phi$ in turn approaching an identity matrix, we see that the energy of $\vec{x}$ can be estimated directly from the signal acquired through compressive sensing $\hat{x}$ (i.e., $\hat{x} = \Phi\vec{x}$). Next, considering energy estimation in a particular band, limited by filter H, we point out that the need for reconstruction via the estimator E arises because H is only known for application to the time-domain signal.

Because the ability for $E^{\mathsf{T}}E$ (and $\Phi^{\mathsf{T}}\Phi$) to approach an identity matrix is limited by the rank deficiency of a compressive matrix [26], we expect that this approach, based on linear estimation, incurs error. To characterize this, we can measure the error between energy derived from the ideal $\vec{y} = \mathrm{H}\Psi\vec{\alpha}$ and energy derived from the estimated $\vec{y} = \mathrm{H}\Psi E_\alpha V\vec{\alpha}$. Note that the input vectors correspond to $\vec{\alpha}$ (rather than $\vec{x}$) and E_α is used to reconstruct $\vec{\alpha}$ (rather than $\vec{x}$); this allows us to employ Ψ and $V = \Phi\Psi$, which is preferred because these are known by definition or can be directly measured from the system (unlike Φ in isolation) [22]:

$$\text{Error} = \frac{\sum_i (||H\Psi\vec{\alpha}_i||_2^2 - k \times ||H\Psi E_\alpha V\vec{\alpha}_i||_2^2)^2}{\sum_i (||H\Psi\vec{\alpha}_i||_2^2)^2}, \tag{8}$$

where k is a scaling factor, and i refers to the samples of input vectors $\vec{\alpha}_i$. In Fig. 11, we show this error, averaging across 10k samples of $\vec{\alpha}_i$, with elements drawn from a uniform random variable. We see that the error is small even at high levels of compression.

In fact, given that our interest is in the spectral energies, we notice another opportunity to reduce the computational complexity. Namely, we introduce a $\mathrm{K} \times \mathrm{N}$ random matrix Θ (where $\mathrm{K} \leq \mathrm{N}$), whose elements are drawn from a Gaussian distribution. By introducing Θ, the energy from the band-pass filtered signal $\vec{y}$ can be estimated from that of $\Theta\vec{y}$. When the energy is extracted in this way, the randomness of Θ causes the intermediate matrix $\Theta^{\mathsf{T}}\Theta$ to approach the identity matrix [25], [26]. Thus, it is possible to extract the energy of the original signal $\vec{y}$ from that of $\Theta\vec{y}$. This incurs only little additional error (Fig. 11), while reducing computational complexity, as shown by the resulting matrix dimensions in Fig. 12. That is, rather than solving for $\vec{y}$, we solve for $\Theta\vec{y}$. As such, the $\mathrm{N}\times\mathrm{N}$ band-pass filter transformation is multiplied by a $\mathrm{K} \times \mathrm{N}$ matrix. Since we can make K less than N, this leads to an overall smaller matrix ($\mathrm{K} \times \mathrm{N}$), resulting in fewer multiply operations.

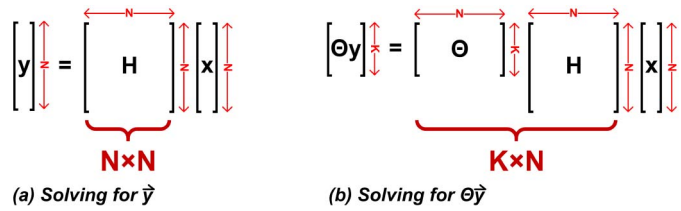

Fig. 12. System for deriving (a) $\vec{y}$, and (b) $\Theta\vec{y}$, showing fewer operations required for deriving $\Theta\vec{y}$.

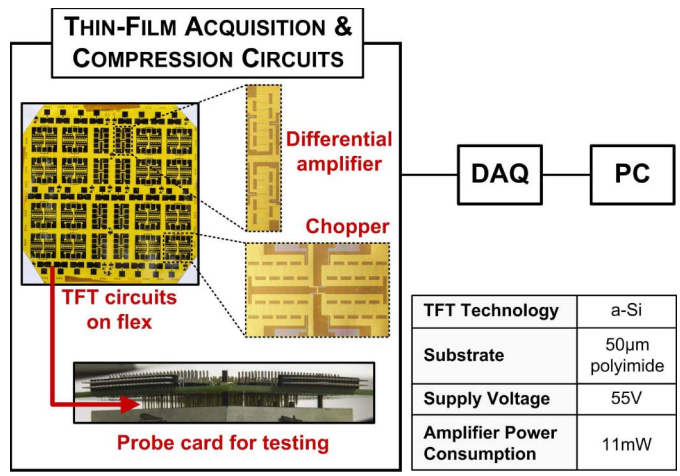

Fig. 13. Thin-film system prototype testing setup and measurement summary.

IV. System Demonstration

Fig. 13 shows the system prototype setup and measurement summary. The TFT chopper and differential amplifier circuits are fabricated in-house on 50 μm-thick polyimide foil, at temperatures $< 180\,^{\circ}\mathrm{C}$. To ease testability, a probe card and DAQ are used to access the TFT circuits and their outputs. This is followed by a PC, used for processing and analysis.

A. Thin-Film Transistors, Resistors, and Capacitors

The TFTs used in the flexible circuits are fabricated using standard a-Si TFT technology with a silicon-nitride gate dielectric [27]. A typical TFT transfer curve is shown in Fig. 14 and detailed transistor characterization under bending is provided in [3].

The resistors and capacitors used in the amplifier and chopper circuits for the system prototype are external, surface-mount components to ease testability and experimentation. However, we routinely fabricate and integrate thin-film resistors and capacitors into flexible circuits (namely, to create

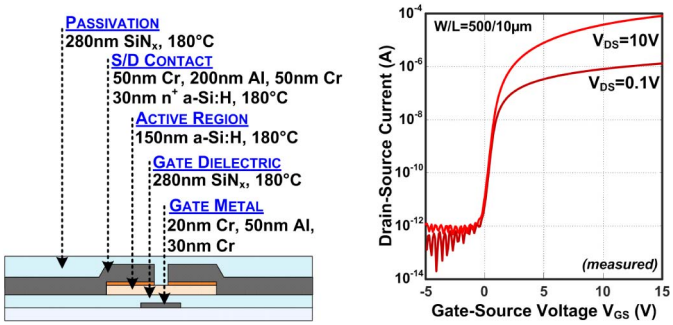

Fig. 14. Amorphous-silicon thin-film transistor structure and transfer curve.

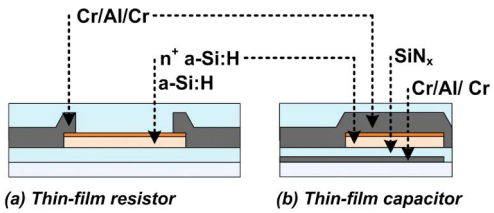

Fig. 15. Structure of an amorphous-silicon (a) thin-film resistor, and (b) thin-film capacitor.

passive loads, as well as voltage-divider and current-mirror biasing structures, as needed in the front-end LNA); these are integrated monolithically within the TFT fabrication process [28].

In particular, thin-film resistors are fabricated using n^+ doped a-Si [Fig. 15(a)]. An interdigitated finger structure is typically employed to achieve the large areas required to generate the resistances needed [9]. With this structure, a 300 kΩ resistance (needed in the chopper-stabilized amplifier) can be achieved by using a 2200 μm × 20 μm structure with a 30 nm layer of n^+ doped a-Si.

Thin-film capacitors are fabricated using the TFT gate dielectric [Fig. 15(b)]. A metal-dielectric-semiconductor-metal structure, rather than metal-dielectric-metal, is used as the semiconductor layer improves the quality of the dielectric, making it less susceptible to shorting [9]. A 280 nm-thick silicon-nitride dielectric achieves a capacitance $\approx$200 pF/mm^2 [9]. Such a capacitance density can result in large areas for the AC-coupling input capacitor (Section III). A possible future step is to explore ZnO technology which, via atomic layer deposition (ALD) can achieve a 40 nm-thick aluminum-oxide layer with capacitance $\approx$1800 pF/mm^2 [13], which is almost 10× more dense.

B. TFT-Based Chopper-Stabilized Amplifier

Fig. 16 shows the gain, common-mode rejection ratio (CMRR) and noise PSD of the TFT amplifier with and without chopping. The noise PSD with chopper stabilization is shown after single-pole low-pass filtering, causing the additional 20 dB/decade roll-off observed. We see that with 5 kHz chopping, the noise decreases in the band of interest to 2.3 μV_{RMS} over a 100 Hz bandwidth. Additionally, the CMRR in that same band is increased from 20 dB to above 40 dB. We note that for EEG acquisition often a higher CMRR is desired (e.g., > 80 dB). In the prototype system, the measured CMRR is due to mismatch of the fabricated TFTs, largely limited due to processing in an academic cleanroom (not limited by the amplifier topology itself).

C. EEG Acquisition

To demonstrate the system prototype, EEG acquisition is performed, recording α-waves from a human subject using standard Ag/AgCl electrodes. Fig. 17 shows the setup used. Two electrodes feed into the TFT low-noise amplifier, one connected to the occipital location and one connected on the apex (reference). During acquisition, the subject cycles through 10 second periods of closing/opening the eyes. From the short-time Fourier transform shown in Fig. 17, the expected 10 Hz rhythm of the α-wave is observed when the subject's eyes are closed. Fig. 17 also shows results from EEG acquisition without chopper-stabilization. In this case, the 1/f noise dominates in both the eyes-open and -closed states.

We also demonstrate compressed EEG acquisition, which includes use of the TFT sub-Nyquist scanning circuits, with the setup shown in Fig. 18. Instead of using scalp-interfaced electrodes, a function generator is used for analog replay of EEG data from an epileptic patient. The EEG data for this test is obtained from the CHB-MIT database [29], [30], and the function-generator output is appropriately scaled to the corresponding EEG amplitudes.

As discussed in Section III, it is possible to reconstruct the original EEG signal from the compressed measurements taken by the system, by solving (2). To perform the optimization required for reconstruction, CVX, a package for specifying and solving convex programs, was used [31], [32]. Fig. 19 shows representative examples of reconstructed EEG waveforms acquired compressively at up to 8x below the Nyquist rate. However, as previously mentioned, our primary interest is in performing feature extraction directly on the compressively sensed EEG. This, and its use to demonstrate seizure detection, is described below.

D. Compressed Seizure Detection

Fig. 20 illustrates the algorithm used for seizure detection, based on [33]. Spectral-energy features of the EEG are used as biomarkers for classifying the onset of a seizure. Specifically, 8 spectral-energy features are derived from each channel of EEG data over two-second epochs. For this, each EEG channel is fed into 8 band-pass filters, centered from 0–21 Hz, and the energy of the resulting output signal is accumulated over each epoch to derive one feature. Thus, over 7 EEG channels, the total dimensionality of the feature vector is 56. This feature vector is fed to a support-vector machine (SVM) classifier with radial-basis function kernel (implemented in MATLAB) to derive the detector output. In our system, the signal over which energy accumulation is performed is derived from linear estimation directly using the compressively acquired samples (Section III-C).

To evaluate the effects of both compression and linear estimation on the derived features, we compare the spectral-energy estimates for EEG acquired through Nyquist sampling

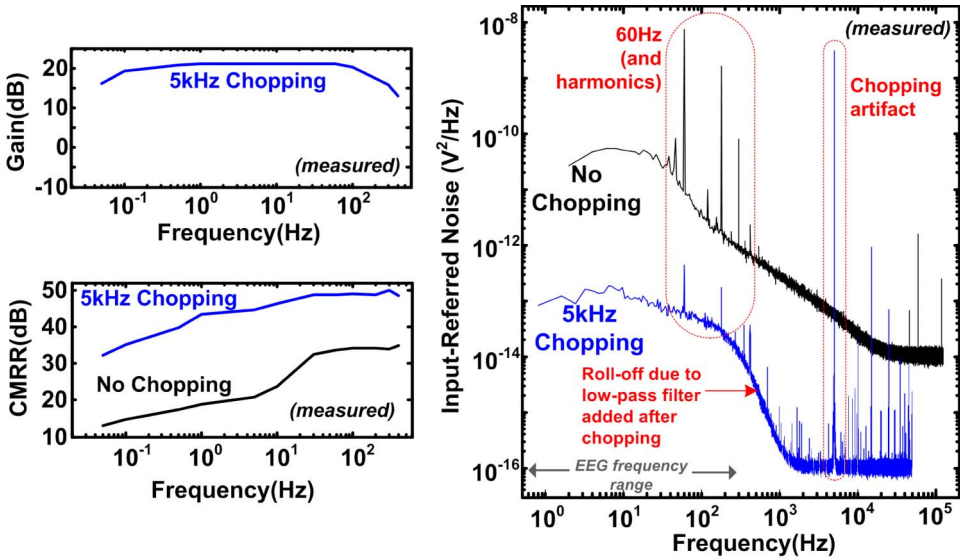

Fig. 16. Measurements of the amorphous-silicon TFT chopper-stabilized amplifier.

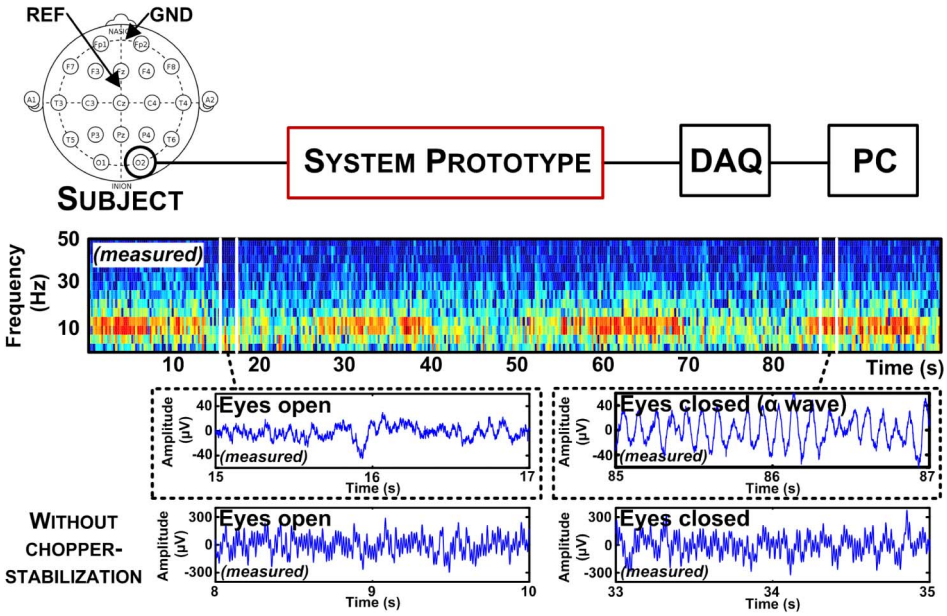

Fig. 17. Setup and measured results of EEG acquisition from a human subject.

Fig. 18. Setup for compressively sensed EEG acquisition.

and compressed sampling, where Θ is selected to be $M \times N$ (i.e., $K = M$). Fig. 21 shows representative spectral-energy features from one of the filters (centered around 0 Hz), for one EEG channel of a patient from the CHB-MIT dataset, across various seizure and non-seizure epochs. At all the compression ratios, the spectral energy is well estimated compared to that derived from Nyquist-sampled signals.

Fig. 22 shows the seizure-detection results versus various compression factors. The dataset consists of 4950 non-seizure and 100 seizure epochs of EEG randomly sampled from one epileptic patient in the CHB-MIT database. The results are shown as true positive (tp), true negative (tn), and error rates. We observe that performance is maintained even out to high compression factors. Because EEG segments are randomly sampled from the available CHB-MIT data, raw classification results are provided, rather than the usual metrics of sensitivity, false-alarm rate, and latency [33].

V. Conclusion

This paper presented an EEG acquisition and biomarker-extraction system based on flexible, thin-film electronics. The system utilizes LAE to form an EEG acquisition system on

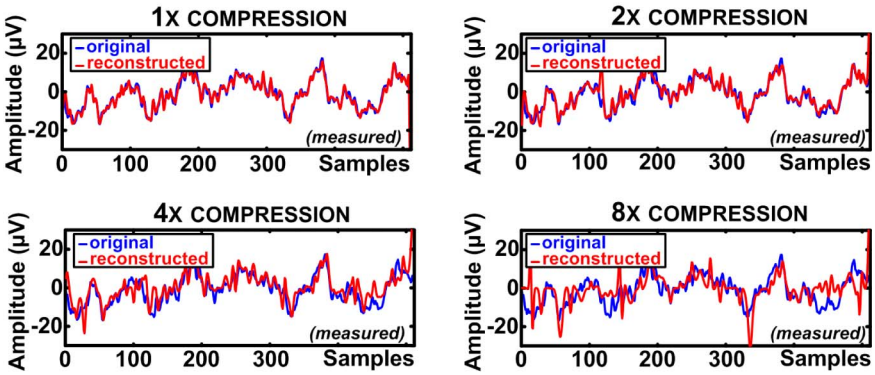

Fig. 19. Reconstructed EEG signals for various compression factors from measured samples (from the CHB-MIT dataset).

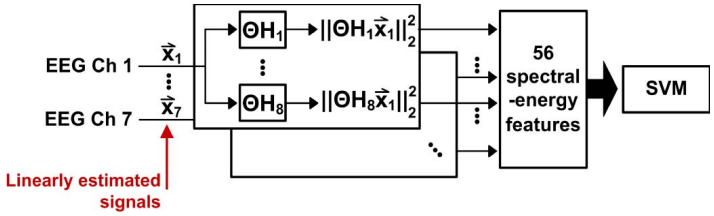

Fig. 20. Seizure-detection algorithm employed.

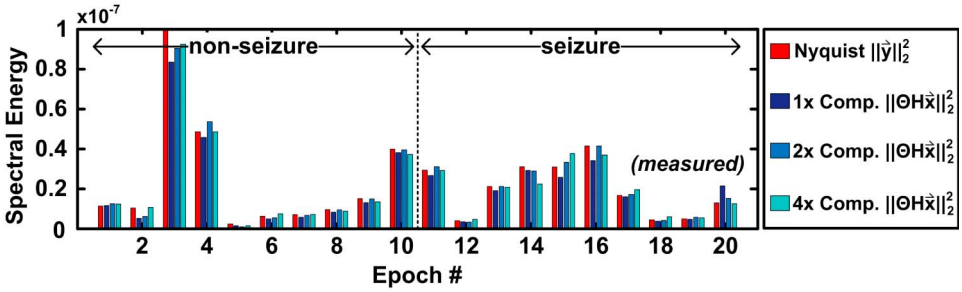

Fig. 21. Comparison of spectral-energy feature estimates (in band centered at 0 Hz) for several epochs of EEG data from one channel (from the CHB-MIT dataset).

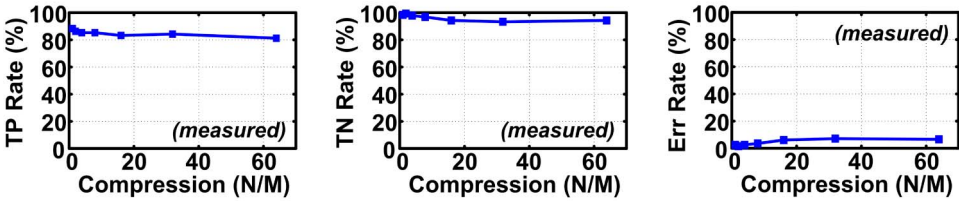

Fig. 22. Measured classification results for seizure detection.

flex with active electronics. More specifically, the system includes TFT-based chopper-stabilized amplifiers as well as compressive-sensing acquisition TFT circuits. Furthermore, the system incorporates an algorithm which can extract EEG biomarkers (i.e., spectral-energy features), directly from the compressively acquired EEG signals.

To demonstrate the system prototype, EEG acquisition, namely α-wave recording, from a human subject is performed. Compressed EEG acquisition using data from an epileptic patient in the CHB-MIT database is also demonstrated. Reconstruction of compressively sensed EEG waveforms at up to $8\times$ compression is successfully shown. As well, spectral-feature-extraction for seizure detection using 7 channels of compressively sampled EEGs is also succesfully shown, with high performance out to large compression factors (e.g., an error rate $< 8\%$ is achieved at $64\times$ compression).

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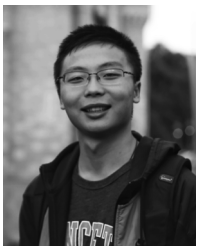

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Dr. Sturm has won more than ten awards for teaching excellence and was a National Science Foundation Presidential Young Investigator. In 1996 and 1997, he was the technical program chair and general chair of the IEEE Device Research Conference, respectively. He served on the organizing committee of IEDM (1988 to 1992 and 1998 to 1999), having chaired both the solid-state device and detectors/sensors/displays committees. He has served on the boards of directors of the Materials Research Society and the Device Research Conference, and co-founded Aegis Lightwave and SpaceTouch.

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