The inset in Figure 5.4 shows the physical assembly of the various components of the HMSD sheet. The use of lamination as described in earlier chapters provides a path for low-cost integration of batteries and multiple free-standing substrates onto which on-sheet a-Si thin-film components (e.g. photovoltaics, Thin-Film Transistors, Thin-Film Diodes) are patterned. Conductive adhesive (e.g. anisotropic conductive film, ACF) provides the low-resistance, mechanically-robust contact between the illustrated planes.

In the following sections, we describe all the components of the HMSD sheet, with particular focus on circuits and devices to meet two key requirements of the sheet. First is the need for **reliable and safe charging of the thin-film batteries from DC-output solar modules** as well as the protection of these batteries from excessive discharge during on-sheet load powering. Second is the need for **off-sheet power delivery from solar cells**; for this, the DC power output is converted to AC via a thin-film power inverter whose power-transfer efficiency is enhanced by operating beyond the TFT f_t frequency limit as described in previous sections.

5.3 System architecture

Fig. 5.5 shows a block diagram of the HMSD sheet. The solar module consists of a-Si solar cells in series, operating at an output voltage, V_{solar}. DC power from the module is distributed on the large-area sheet to

1. an on-sheet power-storage, management and delivery block that comprises batteries, a battery-discharge-regulator subsystem, and on-sheet loads,

2. a wireless power-delivery block, that comprises an inverter for wireless power delivery to off-sheet loads (with their own local energy-storage/regulation circuits).

Under solar illumination, DC current is supplied to both the on-sheet and off-sheet power blocks. In the former, the supplied current is split between charging the batteries ($I_{Battery}$) and delivering power to the on-sheet load (I_{Load}), whilst in the latter, current is delivered to the oscillator (I_{Osc}). Without illumination, current is supplied from the batteries to the on-sheet load and the off-sheet block is not operational.

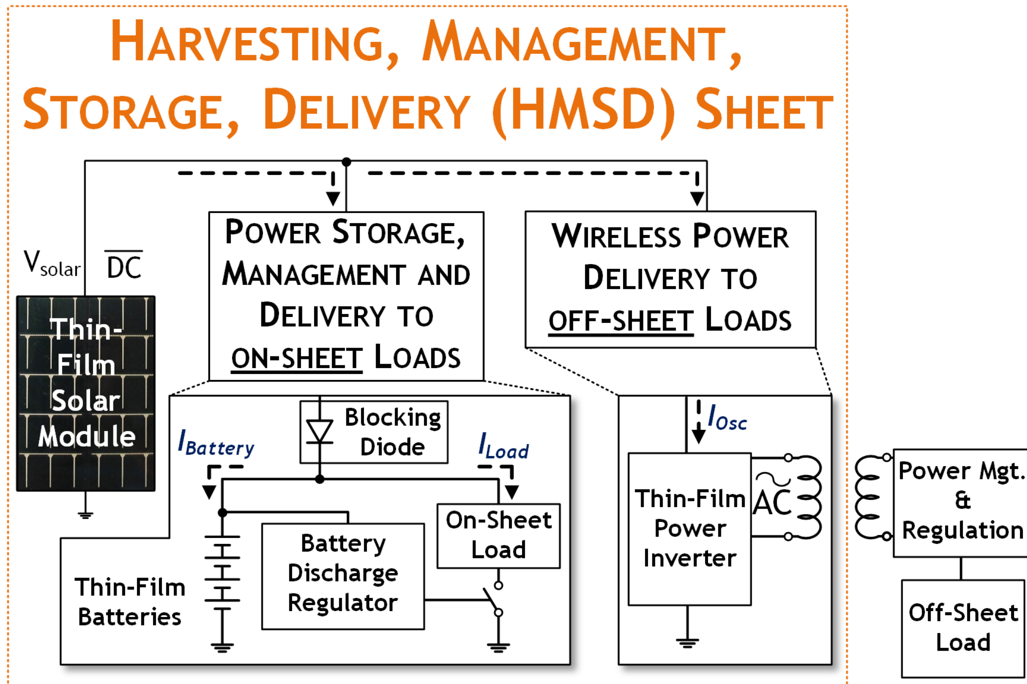


Figure 5.5: Schematic representation of the harvesting, management, storage and delivery (HMSD) sheet system architecture

For the HMSD sheet, Thin-Film Transistors (TFTs), Thin-Film Diodes (TFDs using amorphous or nano-crystalline Si), Thin-Film Diode-Connected Transistors and Thin-Film Resistors (TFRs) are fabricated. Circuits constructed from these components were shielded from light to minimize off-state leakage. Typical device structures and characteristics are described in Chapter 1.

Section 5.4 describes the operation of the on-sheet power-management block and section 5.5 describes the detailed operation of the off-sheet power-delivery block. Section 5.6 presents the measurement results.

5.4 Power regulation and delivery to on-sheet loads

In this section the subsystems of the HMSD sheet for power storage, power-management and power delivery to on-sheet-loads are discussed.

5.4.1 Interfacing with the solar module: blocking diode design

The blocking diode (D_b) prevents leakage from the batteries under low-illumination conditions (i.e. when V_{solar} drops). It could be implemented using either diode-connected TFTs (attractive from an integration perspective), or either a-Si or nc-Si Schottky thin-film diodes (TFD), as shown in a generalization of the power-management block circuit in Figure 5.6. A first evaluation of the performance of the blocking diode can be made by studying the circuit behavior under a range of different loads, R_L. For small resistive loads, $V_{battery}$ droops due to the voltage drop across the blocking diode required to sustain I_{Pmgt}.

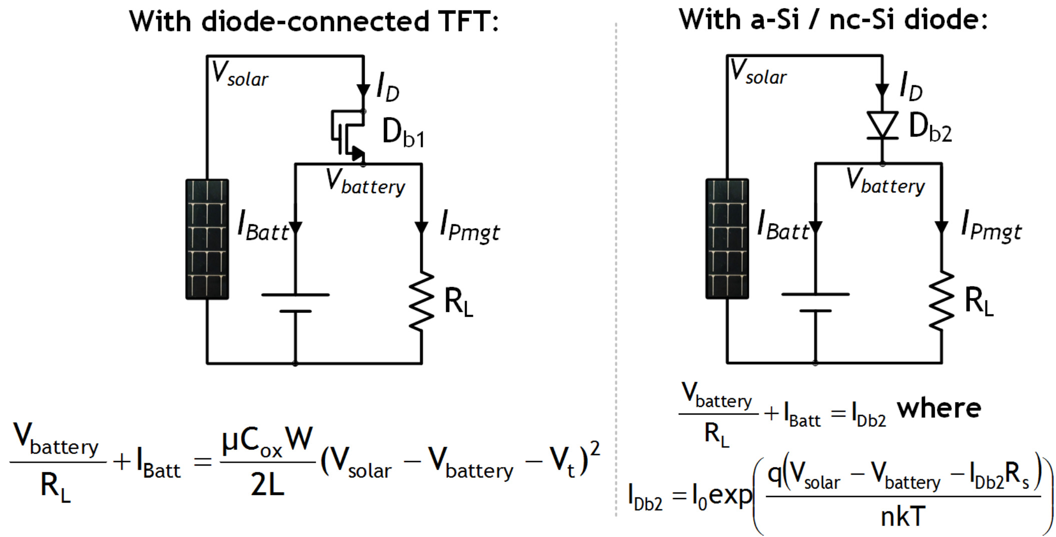


Figure 5.6: Options for the blocking diode interfacing the battery management circuitry with the solar module using either diode connected Thin-Film Transistors or Thin-Film Diodes

A critical condition can be identified where, for a given solar module voltage (V_{solar}), $V_{battery}$ has drooped to the point that the charging current (I_{Batt}) drops to zero (at which point $V_{battery}$ is simply the nominal output voltage of the stack of batteries). This point sets the minimum resistive load that can be powered by the on-sheet block, and thus serves as a performance metric for the system. When using a diode connected TFT (which is connected to always be in saturation when above V_T) this occurs when:

$$R_L < \frac{V_{battery(nominal)}}{\frac{\mu C_i W}{2L}(V_{solar} - V_{battery(nominal)} - V_T)^2}$$

whereas for the case of an a-Si or nc-Si diode, this occurs when

$$R_L < \frac{V_{battery(nominal)}}{I_{Db2}}$$

where I_{Db2} is defined in Figure 5.6, including the diode series resistance component R_S. A second evaluation of the performance is necessary however, considering the reverse leakage current of the blocking diode under the low-illumination condition. Here, nearly the full nominal voltage of the batteries appears across D_{b1}/D_{b2}; an excessive reverse leakage can result in permanent damage of the batteries due to draining as described previously. An analysis of the three diode options is provided in Section 5.6.

5.4.2 Thin-film battery discharge regulator

Figure 5.7 shows the details of the battery-discharge regulator block. This block is connected to the solar module through the charge-blocking diode, D_{b1}, and it gates the current provided to an on-sheet load through the use of M_1 to ensure safe discharge levels for the batteries. For analysis, a purely resistive load is used to represent on-sheet loads; in practice, these could be embedded functionality circuits (e.g sensing, power metering).

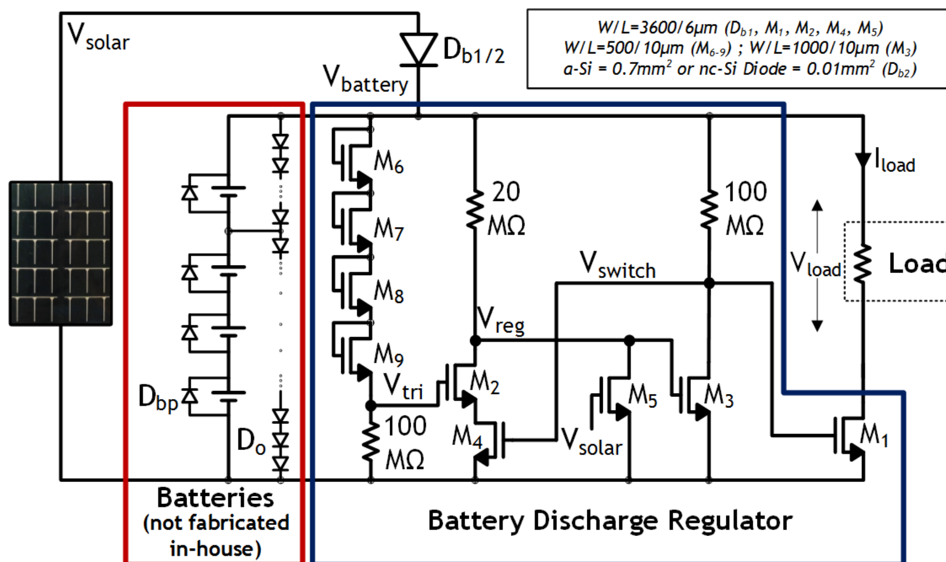


Figure 5.7: HMSD sheet sub-blocks for power storage, management and delivery to on-sheet loads

Four series-connected 300 µA h thin-film Li-ion batteries as previously described are used for energy storage, providing a nominal output voltage, $V_{battery}$, of 15.6V. This value is chosen to satisfy the voltage-level requirements in typical thin-film circuits. The diode stack D_o could potentially be used to ensure proper charging conditions for the batteries (though this was not implemented), while the TFT circuit ($M_1 - M_9$) is used to ensure proper discharging conditions during load powering. During charging, the batteries may not be exposed to a charging voltage greater than ≈16.5V (4x4.125V); to ensure this, the chain of current-shunting diodes, D_o, could provide regulation if this voltage is exceeded. Bypass diodes, D_{bp}, are typically included in parallel with each battery to ensure current continuity if one battery fails.

Under low illumination, the batteries take over powering of the load. Close to the fully-discharged state, as described earlier, the output voltage begins to drop rapidly; however, following from previous discussion, a drop below ≈10V (4 x 2.5V) must be prevented to avoid permanent battery damage.

A low-voltage cut-off circuit is thus implemented, as shown in Figure 5.7, to provide rapid turn-off of the load current via a regenerative circuit. V_{tri} follows the battery voltage, through the voltage drop across a chain of diode-connected TFTs, M_{6-9}. During battery powering, M_2 and M_4 are initially 'on', pulling V_{reg} low; however, the M_{6-9} chain is designed such that when the battery voltage drops below 10V, V_{reg} rises, thereby pulling V_{switch} low through M_3. This causes M_4 to begin to turn off, triggering regeneration on V_{reg} and V_{switch}. This causes the load current to turn off through rapid control of the power TFT M_1.

With full-swing regeneration on V_{switch}, a large on-to-off ratio of 10^5 for the battery current can thus be achieved through M_1 control. Activation of M_1 is subsequently achieved by resetting the circuit through M_5. With M_5 controlled by V_{solar}, battery discharge is prevented until after the battery has been partly/fully recharged, following the return of illumination.

In the 'off' state, current results primarily from static current through the branches of the regenerative stages and through M_1. M_1's current can be handled as described in the following subsection, while the current through the regenerative stages can be minimized through sizing of the associated thin-film resistors. After low-voltage cut-off occurs, the normal battery operating voltage is re-developed on $V_{battery}$ and maintained due to the lower current being drawn, with an effective small increase in battery capacity. The width of M_1 is designed so that the level of leakage

current is such that low-voltage battery failure would not occur until after at least 100h. For an application, this can be set as desired to be much longer than the expected interval expected between daily illumination periods.

5.4.3 Power delivery to on-sheet load

To design the power-TFT M_1, two optimal conditions can be considered. First, the optimal power point for the load is achieved when M_1 imposes a voltage drop equivalent to the load voltage, i.e. $V_{M1} = V_{load} = V_{battery}/2$. Second, the optimal power delivery efficiency is achieved when M_1 exhibits minimal voltage drop. However, this requires either reduction of the load current (and, therefore, load power) or reduction of the effective TFT resistance through increased M_1 width or through an array of parallel-connected TFTs. Though viable, this could increase the off-state leakage and can thus only be pursued to levels permitted by battery discharge limits and expected illumination-cycle periods.

5.5 Wireless power delivery to off-sheet loads

The block to deliver power wirelessly to off-sheet loads consists of an LC oscillator-based on-sheet inverter as described in Chapter 4, which enables the inductive coupling for wireless power delivery to an off-sheet load. Methods for increasing the output power (described in Section 4) include increasing solar-module voltage or optimizing TFT-width for the specific loads expected on the large-area sheet that is receiving the power.

5.6 Measurement results

The entire photovoltaic-based HMSD sheet is fabricated on 50 µm-thick polyimide, at a maximum temperature of 180 °C. The system prototype is shown in Figure 5.8, while the thin-film-circuit micrograph is in Fig. 5.9 and a system performance summary is in Table 5.1.

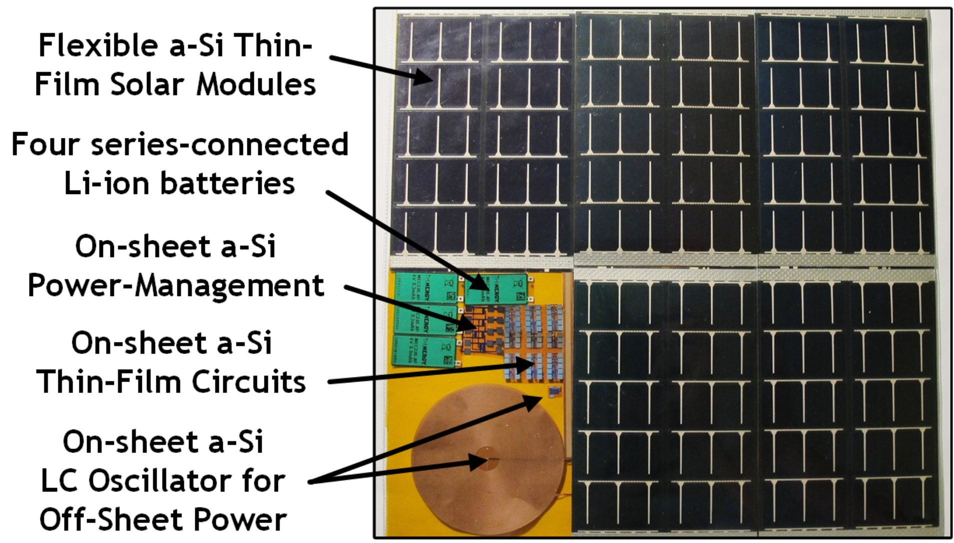


Figure 5.8: System prototype on a flexible polyimide sheet (20 x 15cm) showing the assembled thin-film components: solar modules, batteries, thin-film circuits and wireless power transfer inductors

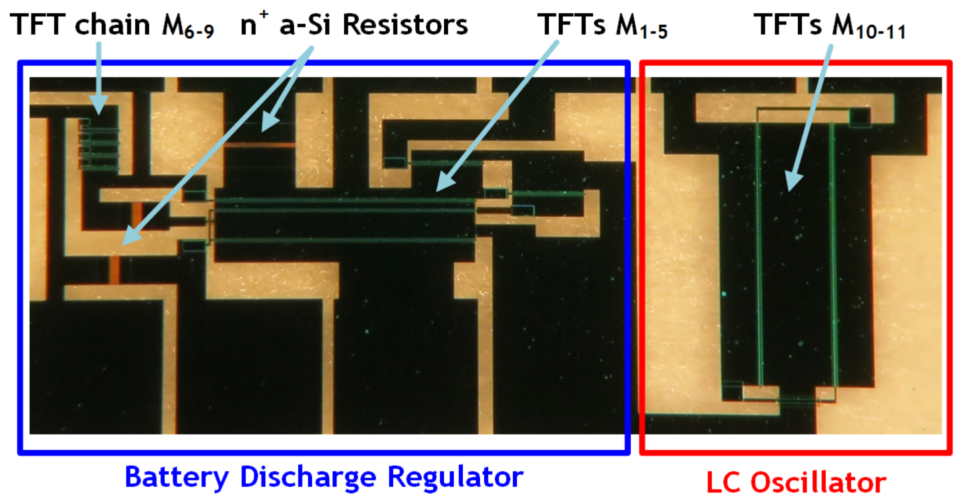


Figure 5.9: Micrographs of HMSD thin-film circuits (10 x 5 mm)

5.6.1 Power regulation and delivery to on-sheet loads

5.6.1.1 Thin-Film blocking diode optimization

A comparison of the three blocking diode options is performed in Table 5.2 using the performance metrics described earlier, with $V_{battery}$=15.6V and V_{solar}=19V for the TFT-based and a-Si Schottky diodes (leading to a 3.4V allowable diode-voltage drop). For the nc-Si diodes, a V_{solar}=17.5V is

Table 5.1: HMSD sheet system performance summary

a-Si solar module	V_{oc}=19V, Area=240 cm^2 Under indoor illumination=0.4 mW/cm^2
Batteries	4 x Li/$LiCoO_2$/LiPON, 300 µA h, 3.9V, 2.5V<Operating voltage per battery <4.12V
On-sheet load,power	1.2 mW to 150 kΩ
Largest on-sheet load	150 kΩ with a 0.7 mm^2 a-Si blocking diode
On-sheet standby current	240nA (circuit) + 120nA (blocking diode)
Off-Sheet max. load power	10mW to 10kΩ at 21% transfer,efficiency
Off-Sheet transmission	Frequency 2MHz, 2cm-radius inductors

used for comparison as voltage drops larger than 3V are unreliably sustained due to the large current densities achieved.

Table 5.2: Performance metrics for blocking diode options

Blocking Diode	**Metric 1: On-Current Delivery to Load**	**Metric 2: Reverse leakage at -15.6V**
Diode connected TFT (W/L = 3600/6 µm)	For Vgs=Vds=3.4V, Id=10 µA → Minimum R_L=1.5 MΩ	<500pA
a-Si Schottky Diode (Area = 1 mm^2)	For Vd=3.4V, Id=200 µA → Minimum R_L=80 kΩ	≈100nA
nc-Si Schottky Diode (Area = 0.01 mm^2)	For Vd=2V, Id=5mA → Minimum R_L=3 kΩ	≈3 µA

Whilst the diode-connected TFT provides an attractive on-current to reverse-leakage ratio, for practical TFT dimensions, the on-current is lower than the manufactured a-Si diodes. The a-Si Schottky diode used in this system provides good forward current (≈ 200 µA) when the solar module is charging the battery and powering the load, while giving a reverse leakage (≈ 100 nA at -15.6V) which is reasonable, in that it is on the same order as the static leakage through the power-management block, as will be described later. The diode size could be increased further to support higher load currents at the cost of proportionally higher reverse leakage. The nc-Si diode has a better on-off ratio, potentially allowing for slightly better forward current; however, depending on the required reverse leakage conditions, very small diodes (<0.0005 mm^2) might be required, which are challenging to manufacture.

Figure 5.10 shows the drop on the battery-voltage rail that arises due to voltage drops across the blocking diode D_{b1} (a-Si, 1mm^2 diode) as the load current increases (i.e. due to reduced on-sheet loads).

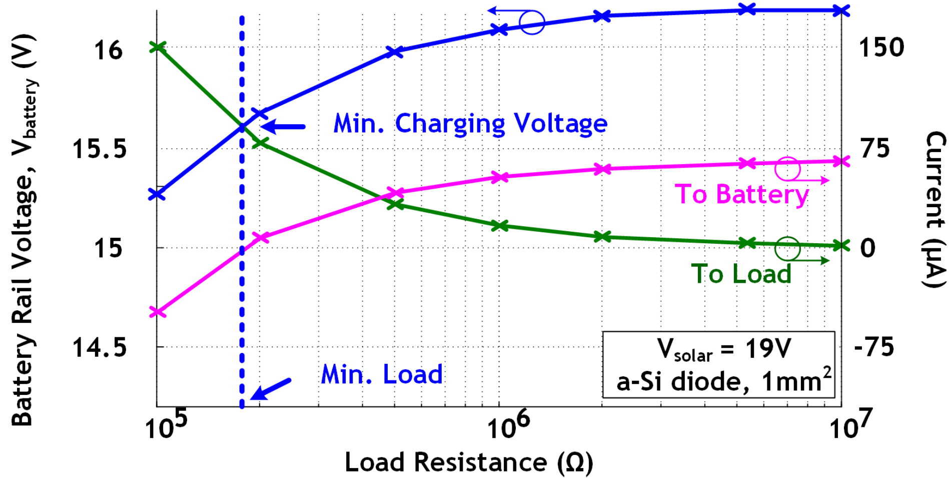


Figure 5.10: Measured effect of blocking diode voltage drop on battery-charging current

With a 0.7mm^2 a-Si TFD, loads less than 150 kΩ are still powered, but the voltage on $V_{battery}$ falls below 15.6V and is no longer sufficient to provide charging current to the batteries.

5.6.1.2 Thin-film battery discharge regulator

Figure 5.11 shows measured waveforms for the on-sheet battery discharge regulator subsystem. For testing, power at a level of ≈5mW is delivered for 45 minutes from the batteries to a 10 kΩ load.

As the battery is discharged, the nominal output voltage is initially maintained, but beyond 40 minutes begins to decrease. Once $V_{battery}$ reaches the critical-discharge level (≈10V), the low-voltage cutoff circuit triggers, and the load current is disabled by the power TFT M_1. Subsequently, the current drawn from the batteries drops to below 360nA, protecting the battery from further discharge.

At this point, the voltage of the batteries returns to a level close to the nominal output voltage due to the greatly reduced current being drawn. A reset through M_5 arising from renewed solar-module illumination is also shown.

The variability of the M_{6-9} voltage drop (i.e. due to TFT threshold-voltage variation) could potentially shift the trigger point; however, measurements across many diode chains found that the

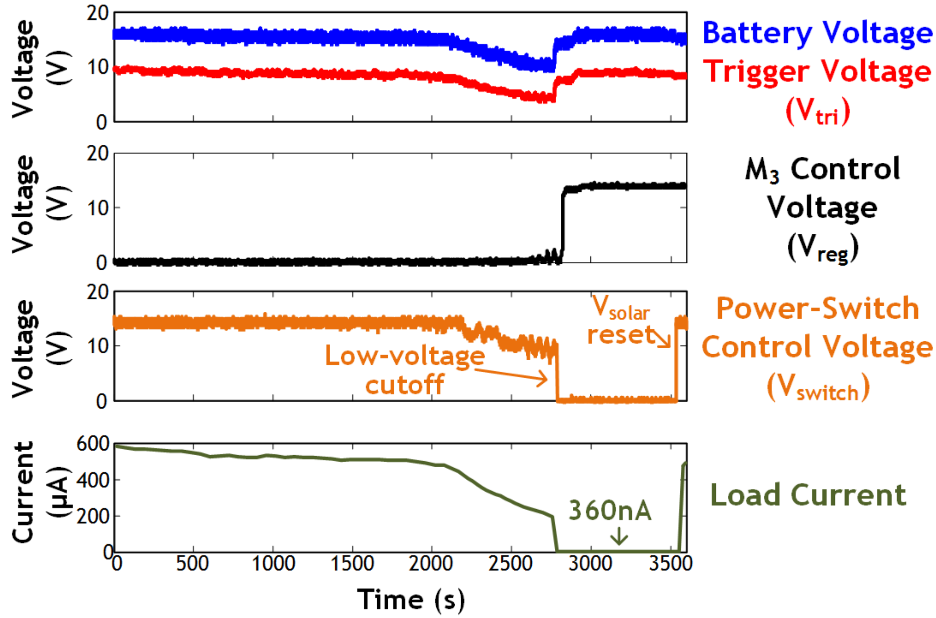
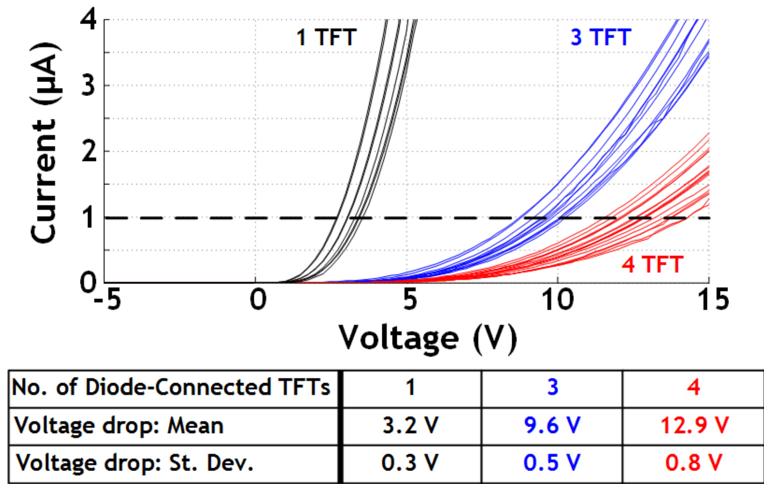


Figure 5.11: Measured waveforms for on-sheet power delivery



No. of Diode-Connected TFTs	1	3	4
Voltage drop: Mean	3.2 V	9.6 V	12.9 V
Voltage drop: St. Dev.	0.3 V	0.5 V	0.8 V

Figure 5.12: TFT diode chain variability statistics at $I_{diode-chain} = 1\,\mu A$

range required to ensure correct regeneration can reliably be achieved with modest margining, as set by the standard deviations shown in Figure 5.12.

5.6.1.3 Thin-film on-sheet power delivery

Figure 5.13 shows how the voltage drop across the power TFT switch scales with the width of the switch (implemented as parallel TFTs, for testing performed without charge-blocking diode D_{b1}).

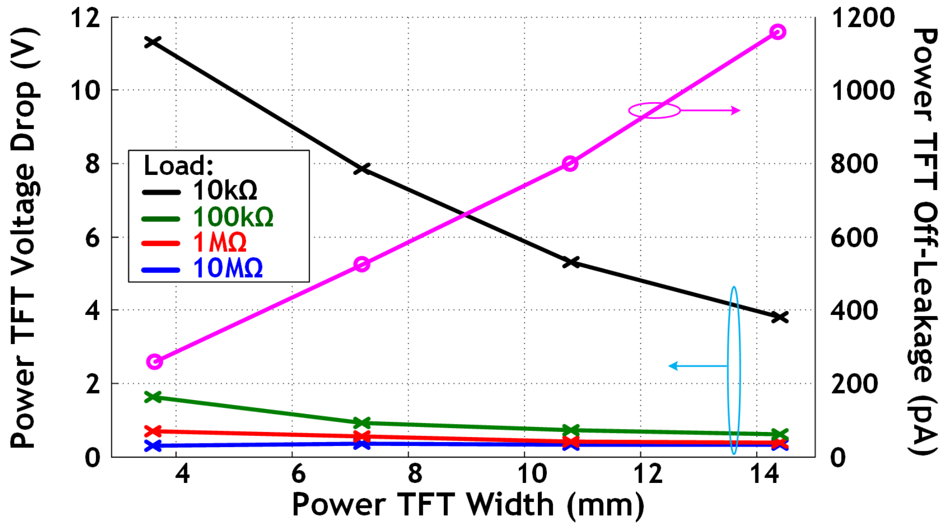


Figure 5.13: Tradeoffs of power-TFT M_1 voltage drop and off-leakage incurred through scaling of the M_1 TFT width

Wider switches result in reduced drops and large V_{load}; however, as shown, this comes at the cost of larger off-state leakage current (shown for V_{drop}=15.6V). In the prototyped design, however, this leakage is very small compared to the leakage due to the regenerative branches of the cutoff circuit.

As discussed earlier, two optimization approaches may be considered for power delivered to the on-sheet load: optimal power delivery or power delivery efficiency.

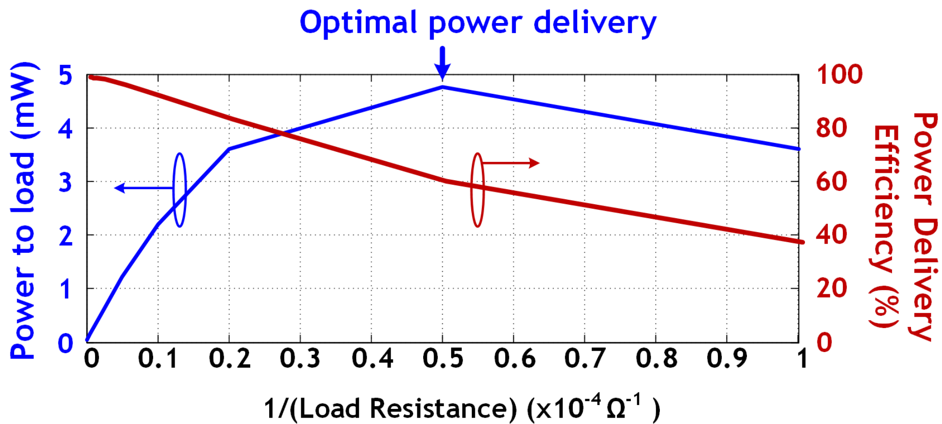


Figure 5.14: Tradeoff of power delivered versus power delivery efficiency to on-sheet loads

Figure 5.14 illustrates this tradeoff whereby with larger resistive loads higher delivery efficiency is achieved at the expense of power delivered to the load.

5.6.2 Wireless power delivery to off-sheet loads

The LC oscillator, based on those described in Section 4, delivers power wirelessly (at 2MHz) to an off-sheet resistive load via 2cm-radius patterned 25 µm-thick copper inductors. As before, the inductors could be monolithically fabricated onto the HMSD sheet through an additive process, but for this system demonstration, are fabricated separately and mounted for testing. At a V_{solar} of 19V, with 1mm separation separation between the source and load inductors, the LC oscillator delivers 8mW (under indoor lighting conditions) with 21% power-transfer efficiency, drawing power directly from the solar module.

5.7 Conclusions

A fully thin-film power harvesting, management, storage and delivery (HMSD) sheet is demonstrated based on PV harvesters. It delivers power both locally to an on-sheet battery, battery-management system and load, as well as wirelessly to off-sheet loads through a LC-oscillator-based power inverter. The use of thin-film batteries enables the continuous operation of embedded systems under temporary conditions of reduced illumination. For reliable battery operation, integrated circuitry for controlling the charging and discharging conditions on the batteries is demonstrated enabling mW-level output power with low off-state leakage.

The typical level of power consumption of a CMOS IC we develop is on the order of a few hundred micro-watts. While the results presented show that such a system could be *continuously* powered from a thin-film battery for at least 30-45 minutes, in practice it is very likely that readout from sensors would be duty cycled at a low rate of perhaps a few short measurements per hour. Assuming a dark period of 12h (the extreme of a diurnal cycle), this system would allow for measurements for at least 5-6 minutes per hour, which is likely suitable for sensing of slowly-changing ambient conditions.

Chapter 6

Conclusions

Large-area electronics makes a wide-range of highly compelling energy-harvesting devices possible. The ability to integrate TFTs raises the possibility of creating complete powering systems. However, the distinctive characteristics and limitations faced with TFTs makes the consideration of alternate topologies necessary for the power circuits. This work demonstrates alternate topologies for power-transfer, power-amplification, and control stages. TFT optimizations and thin-film devices were considered, specifically in the context of achieving manufacturable power systems on flexible substrates.

The benefits of non-contact interfacing in hybrid systems was introduced and then two power systems for wireless load charging from solar-energy harvesting were described. The oscillator-based system achieves high efficiency at high output power levels for a given size of passive thanks to its ability to operate at high frequencies, enabling high quality inductive coupling. In addition, no efficiency-reducing overheads are introduced that arise from the necessary use of control stages in the capacitive-based system. Work is described on the potential use of thick-film conductors for LC-oscillator topologies. Finally, a fully thin-film power harvesting, management, storage and delivery (HMSD) sheet was demonstrated.

Circuit design, analysis and measurements in the systems presented was done by this author in collaboration with Liechao Huang and Yingzhe Hu. All thin-film design and fabrication was performed by this author. The thick-film inductor designed was performed by this author at the

University of Tokyo in collaboration with Naoji Matsuhisa. The thin-film battery management system was designed, manufactured and tested exclusively by this author.

Part III

Communication Systems

Chapter 1

Introduction

In the previous part of this thesis, we introduced a number of architectures for non-contact interfacing of power over short distances using planar patterned capacitors and inductors. Of course, these interfaces could also be used to transfer signals between multiple functional planes of a system (and is the approach in fact used in e.g. RFID systems). For large-scale systems on plastic, however, a need exists for efficient *medium to long-range* communication of information.

Let us begin by acknowledging that very high-performance, low-energy transceivers are already available and widespread in conventional (CMOS and more) IC technology. The energy efficiency of these is such that it is very unlikely that large-area approaches will ever replace these for long-distance transmission of information to base-stations. Nevertheless, in a distributed hybrid architecture some form of on-sheet short to medium-distance communication to sensors, harvesters or other computational units may make sense from an energy, integration-of-subsystems or cost perspective, or in cases where the installation environment of sheets preclude high-performance wireless transmission (e.g. on metal surfaces).

Two approaches can be taken in the large-area domain: communication either through *wireline* or *wireless* techniques.

For wired communication, there exists the ability to pattern long-range (0.01-10m) interconnects on plastic. Analysis from our group [61] has shown that this can be an attractive alternative to CMOS wireless transceivers in terms of energy/bit. One of the challenges with this is the ability to achieve optimal communication efficiency in the presence of the unpredictable large-area

interconnect impedances, hence the transceivers must be capable of self-adjusting the modulation frequency to match the resonant point of the wireline impedance [61].

For wireless communication, a key challenge is the ability to design a good antenna. Through large-area patterning, an opportunity is raised to use the same materials used for long-range interconnects (e.g. copper on plastic) to create physically-large antennas, with increased radiation efficiency. In this section we will demonstrate a fully-thin-film radio that uses such large-antennas and the ability we described in earlier sections to operate TFTs at frequencies near or beyond their f_T.

Chapter 2

A thin-film radio on plastic

In this chapter we will demonstrate a super-regenerative (SR) transceiver with integrated antenna on plastic that leverages the attribute of large area to create high-quality passives; this enables resonant TFT circuits at high frequencies (near f_T) and allows for large antennas, maximizing the communication distance.

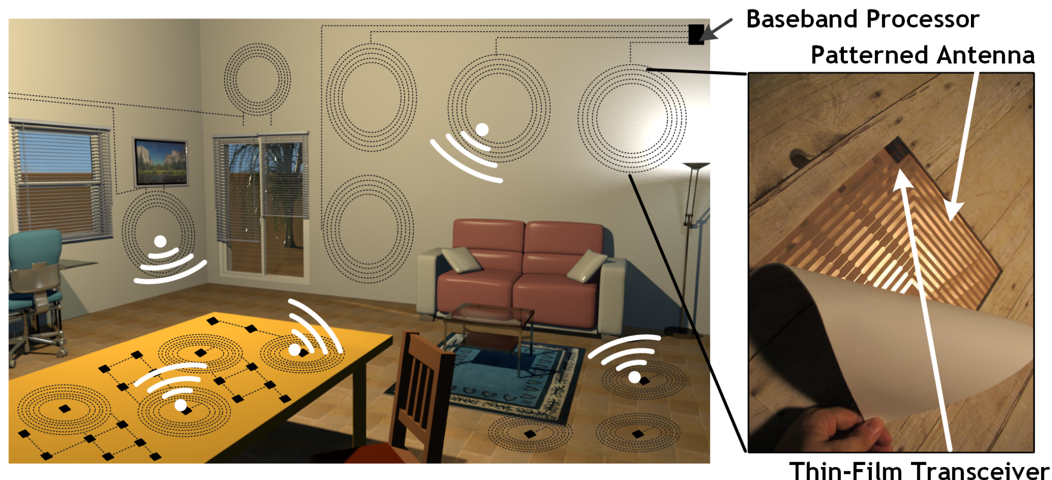


Figure 2.1: Large-area distributed antennas for communication

The resulting carrier frequency is 900kHz, and the range is over 12m (at 2kb/s). As shown in Figure 2.1, this could enable sheets integrating arrays of radio front-ends for distributing a large number of communication links over large areas.

2.1 System architecture

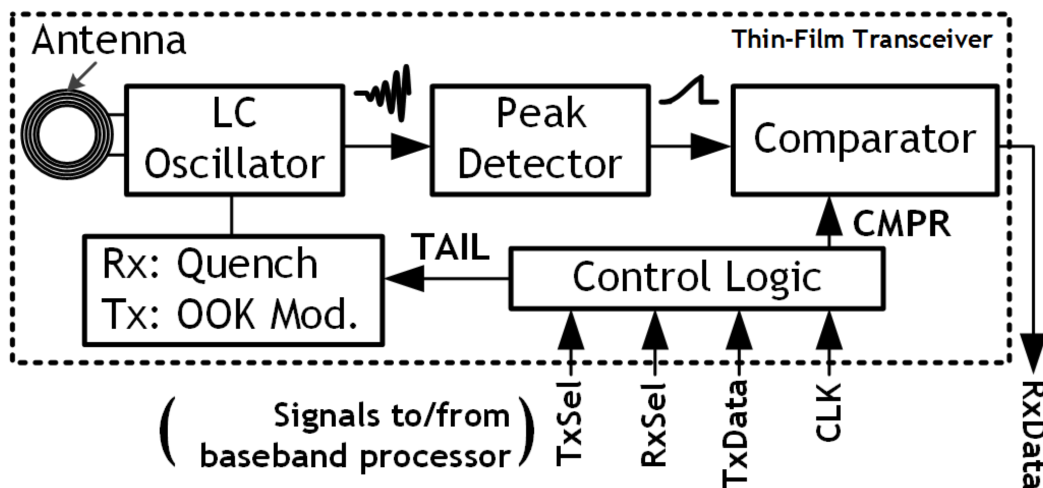


Figure 2.2: Transceiver system architecture

Figure 2.2 shows the system architecture for the transceiver in transmit and receive modes. The circuits are based on the amorphous-silicon (a-Si) TFTs processed at 180 °C that we introduced earlier in Part I. The critical block is the LC oscillator, as demonstrated in Part II, with the tank inductors act as the antenna.

In Transmit (Tx) mode, data is transmitted by gating the oscillator for on-off-keying (OOK) modulation; in Receive (Rx) mode OOK data is received by sensing the oscillator startup time with respect to a quench signal. The design is based on three key insights:

1. LC oscillators offer the benefit that performance limitations due to TFTs can be overcome by the ability to form high-quality passives (as we showed in Part II)

2. the ability to pattern large inductor antennas, with dimensions on the order of a meter, substantially improves coupling between transmit and receive antennas

3. active transceivers result in superior scalability in communication distance as compared to a passive transponder

Figure 2.3 illustrates how these factors enhance communication distance. At the achieved frequency, the carrier wavelength is ≈300m, implying that the antennas are electrically small and, for the distances of interest, operate dominantly in near-field mode.

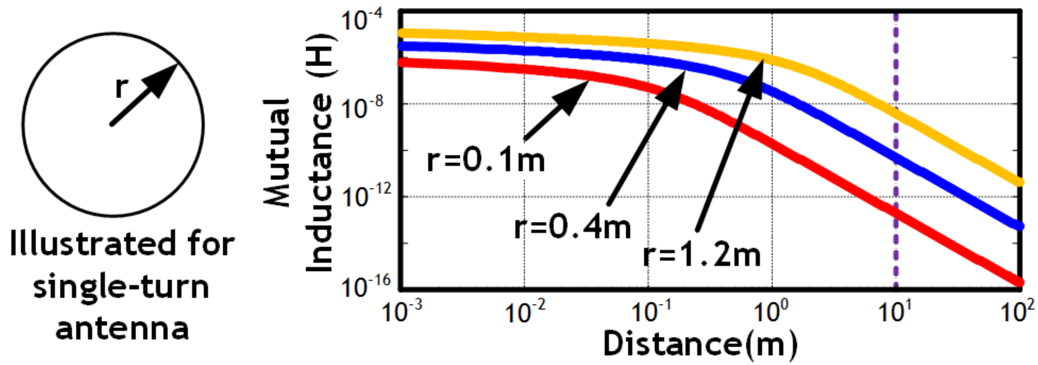


Figure 2.3: Mutual inductance versus antenna size

In this case, antenna coupling is determined by mutual inductance, which greatly improves with large antennas, as shown. In the near field, inductor coupling also makes communication based on impedance modulation possible, enabling a passive transponder. However, Figure 2.4 shows that the received signal due to a reflected impedance degrades quadratically with mutual inductance (M), thus falling rapidly with distance; whereas the received signal due to an active transmitter degrades only linearly with M, enabling the distance we achieve.

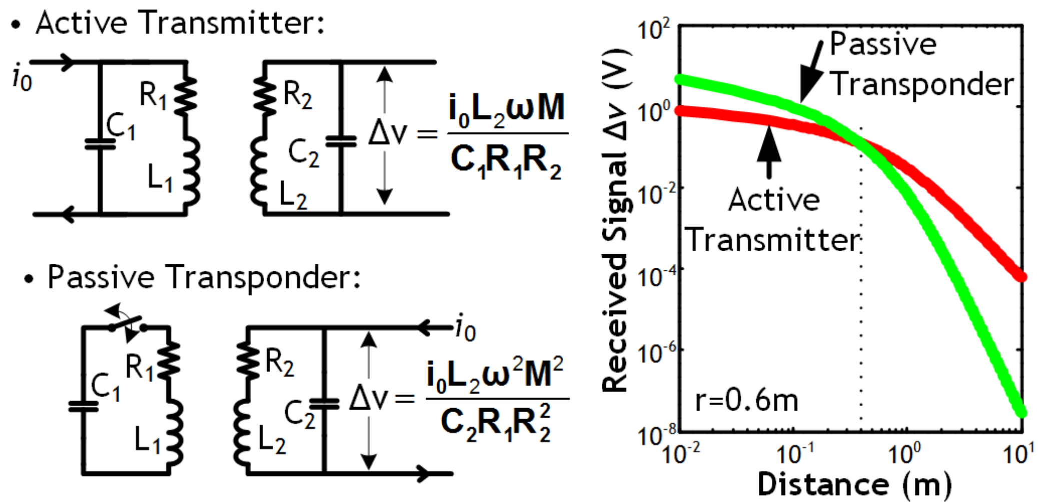


Figure 2.4: Active vs passive communication range scaling

2.2 An application of the LC oscillator

Figure 2.5 shows the details of the LC oscillator, including the gate resistance, R_g ($\approx 50\,\Omega$ for a bottom-gate TFT structure) and capacitance of the subsequent block, C_L (i.e. the peak-detector). As described in Part II, the positive-feedback oscillation condition requires that $g_m R_{tank} > 1$ for the cross-coupled stages. Note here that the LC oscillator is outfitted with a tail device which gates the current to the oscillator.

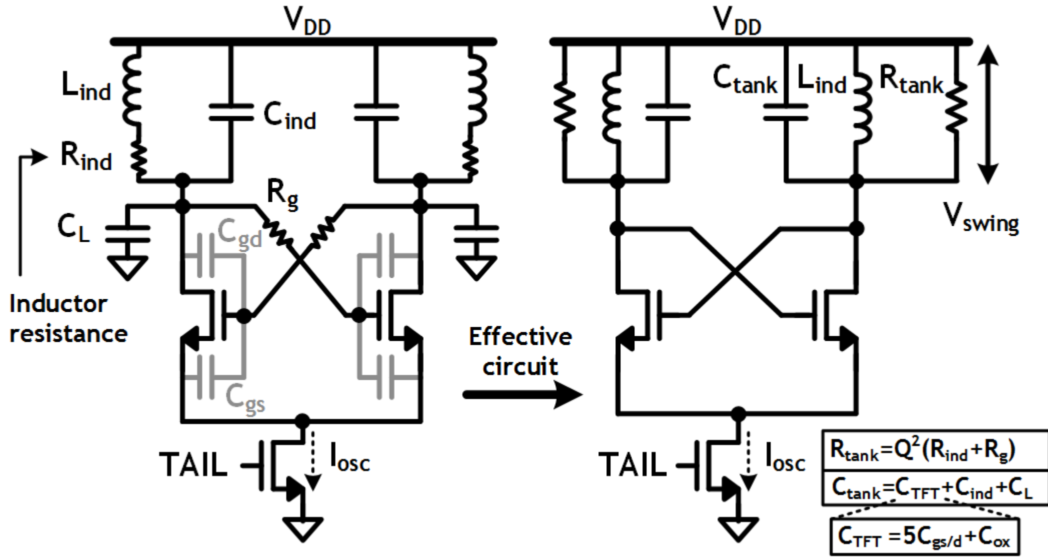


Figure 2.5: The LC oscillator

The voltage induced in a receive antenna due to the current in a transmit antenna i_{ind} is given by:

$$V_{received} = M\frac{di_{ind}}{dt}$$

with M depending on physical parameters of the antennas and distance. For the transmit antenna, we can conversely state that the voltage swing in the transmit tank, V_{swing}, is equal to:

$$V_{swing} = L_{ind}\frac{di_{ind}}{dt}$$

With the voltage swing also equal to $V_{swing} = I_{osc} \times R_{tank}$, we can state that:

$$\frac{di_{ind}}{dt} = \frac{I_{osc} \times R_{tank}}{L_{ind}} = \frac{I_{osc} \times Q^2(R_{ind} + R_g)}{L_{ind}}$$

The *power efficiency* of the transmit oscillator can thus be represented by normalizing $\frac{di_{ind}}{dt}$ with the current consumed by the oscillator I_{osc}:

$$\frac{1}{I_{osc}}\frac{di_{ind}}{dt} = \frac{Q^2(R_{ind}+R_g)}{L_{ind}} = \frac{1}{C_{tank}(R_{ind}+R_g)}$$

where we have used the fact that:

$$Q = \frac{1}{(R_{ind}+R_g)}\sqrt{\frac{L_{ind}}{C_{tank}}}$$

This quantity is maximized by minimizing C_{tank} (i.e. $C_{TFT}+C_L+C_{ind}$) and $R_{ind}+R_g$. Inductor area scaling helps with both of these. First, patterning thick planar traces, leads to low R_{ind}. Second, C_{ind} benefits from patterning inductor traces with adequate separation, leaving C_{tank} limited by the TFT and load capacitances. The TFT parasitics are $C_{gs/d} \approx 7pF$, $C_{gs/d} \approx 5pF$, $R_g \approx 50\,\Omega$, and for the coupled 0.6×1.2m inductors used, $L_{ind} \approx 180\,\mu H$, $R_{ind} \approx 4\,\Omega$, $C_{ind} \approx 10pF$; to drive the load capacitance (20pF) at an oscillator voltage (V_{swing}) of 10V, this allows I_{osc} of 500 µA from a 20V supply.

2.3 Thin-film envelope detector and comparator

Figure 2.6 shows the envelope detector and comparator. The oscillator signal is AC coupled to the envelope detector. The primary concern is ensuring that high-frequency components do not conduct to the output via the TFT gate-source capacitances. In the topology, rectification is achieved by the non-linear TFT currents on the source node, and the capacitive transmission effect is cancelled by the differential structure, where $C_{gs1,2}$ pull the source node in opposite directions. Waveforms are shown in Figure 2.7.

The availability of only NMOS TFTs in a-Si technology poses challenges for achieving strong regeneration in the comparator. In the topology used, the NMOS regenerative devices are in the pull-down path, in series with the input devices. Although a parallel regenerative path would lead to faster regeneration, the input devices in series improve sensitivity and robustness by making the regeneration path explicitly dependent on the input signal. To further enhance robustness, the TFT lengths are upsized to 10 µm, rather than 6 µm, which is used for all other devices in the radio.

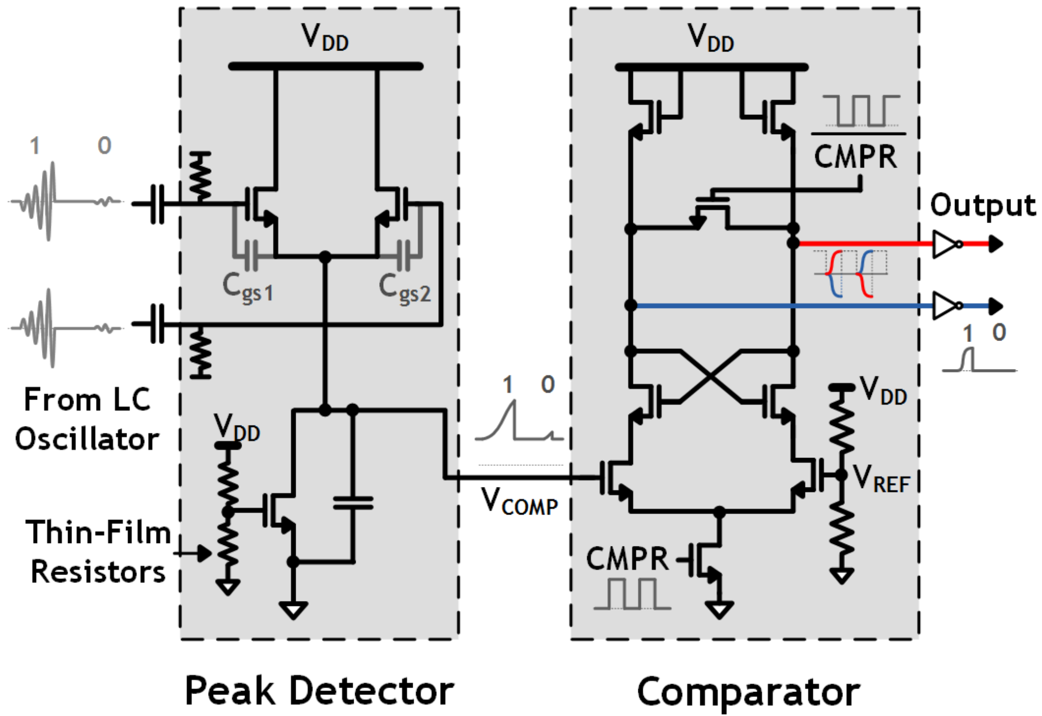


Figure 2.6: Envelope detector and comparator

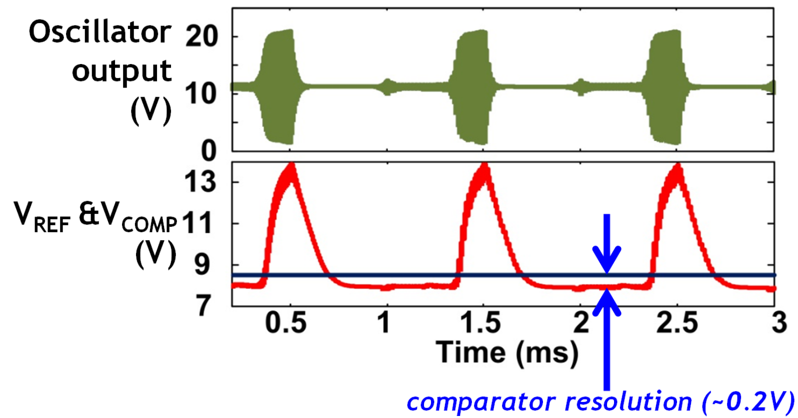


Figure 2.7: Envelope detector waveforms

To ensure sufficient strength of the regenerative path, the biasing point of the input devices, which is set by the envelope detector output, is maximized. For this, the envelope detector inputs and tail current are biased, so that the output is at the highest level at which the Rx-mode oscillator swing (5V) can be tracked without being saturated by V_{DD}. Biasing is achieved using thin-film doped a-Si resistive dividers. Waveforms for the comparator are shown in Figure 2.8. It was decided to

use a ‘high’ reset state for the comparator since, even though this results in weaker control of the CLK TFT with high voltages on its drain and source, the two following benefits are noted:

1. It is easier to use the NMOS TFT devices to pull down the output nodes during regeneration and,
2. In the high state, both sides of the cross-coupled latch are forced to the same voltage (‘off’) as the tail TFT is off. Hence, once CMPR is set high, regeneration is easier.

In practice though, topologies of both types were implemented and little difference was seen in their performance.

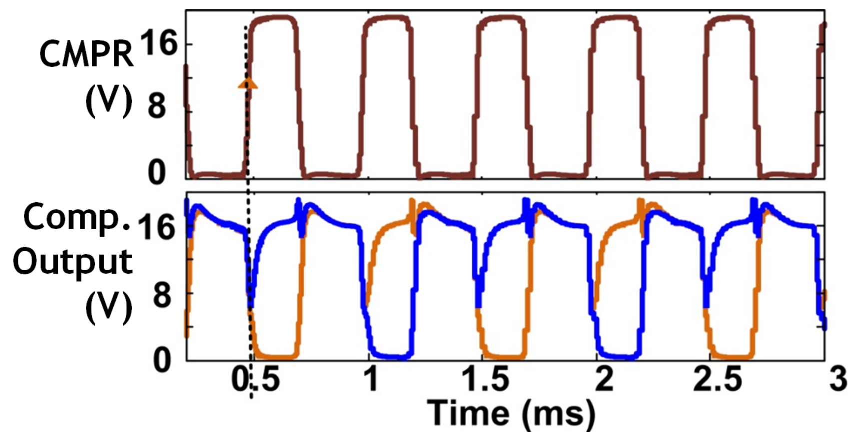


Figure 2.8: Comparator waveforms

2.4 Control logic

Figure 2.9 shows the control block. A baseband processor, which can be placed at a distant location on the sheet, provides clock, data, and Tx/Rx-selection signals via patterned large-area interconnect. To enable synchronization of the radio, clock (CLK) is used to derive the oscillator tail-control (TAIL) and comparator-enable (CMPR) signals, as shown. In Rx mode, TAIL is a quench signal (QUENCH); when CLK is high, QUENCH is set by the voltage divider to a low value that suppresses oscillations. Then, to maximize receiver sensitivity, a gradual turn on is desired [62]; this is achieved by using a weak NMOS device (M1) to charge QUENCH. CMPR is then derived from a delay chain, to position the comparator decision instance at a point just before that where the oscillator would start up in the absence of receive data. In Tx mode, TAIL is a

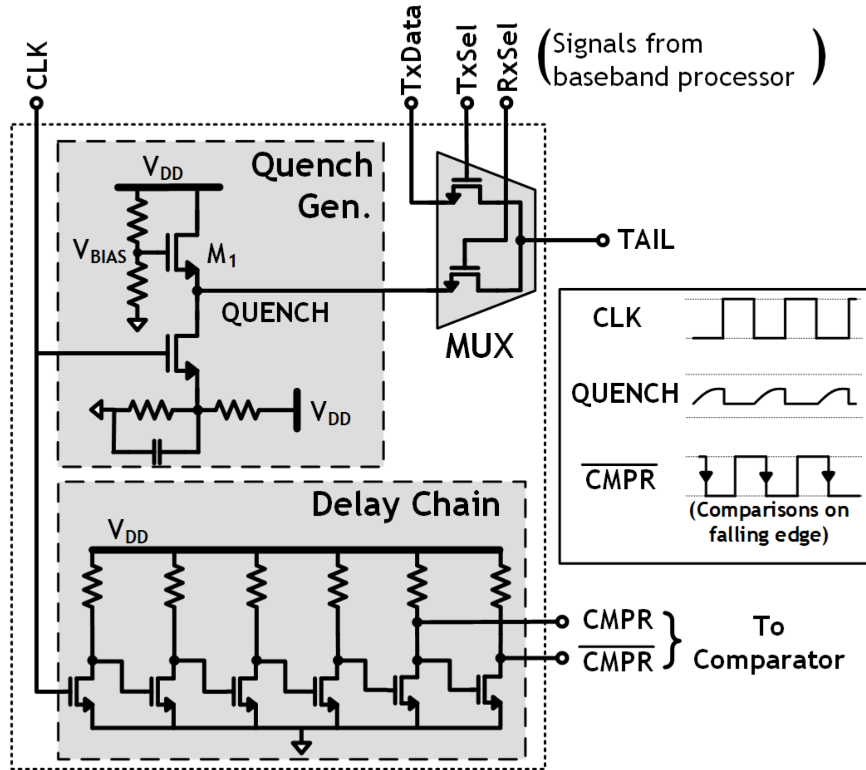


Figure 2.9: Thin-film control block for oscillator quench and comparator-enable signals in RX mode and OOK in TX mode

full-swing signal derived from the transmit data, and it is used to switch the oscillator for OOK modulation.

2.5 System measurements

Figure 2.10 shows measured waveforms from the prototype fabricated on 50 µm polyimide and Figure 2.11 shows the prototype micrographs.

For data rates of 2kb/s and 4kb/s the communication distance is 12m and 7m (BER less than 0.1%), achieved using the 0.6×1.2m antennas, and with measured receiver sensitivity of -80dBm (sensitivity is defined as the minimum power received that leads to a discernible result at a particular data rate, in our case a 1V eye in the envelope detector). The sensitivity was measured by feeding in power using a signal generator to the receiving antenna tank through a large discrete resistance and coupling capacitor connected to the drain of one of the cross-coupled TFTs. With an estimated

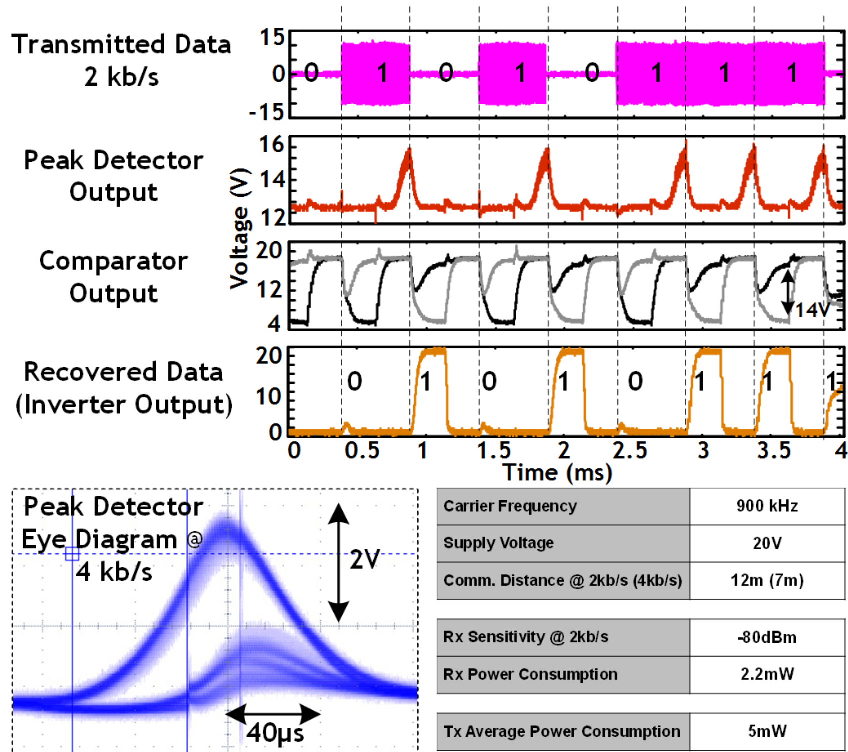


Figure 2.10: Measured waveforms and performance summary of the thin-film radio on plastic

R_{tank} of about 22 kΩ and an input coupling resistor of 1.5 MΩ, a minimum of 50mV$_{pp}$ is required for a 1V eye. This corresponds to a sensitivity of -80dBm.

The bit-error rate measurement is shown in Figure 2.12 along with the testing setup. With a 20V supply, the total Rx/Tx power consumption is 2.2mW/5mW.

As described earlier, the ability to pattern large devices in the large-area-electronics technology also enables the integrated radio sheets to be fully self-powered, by patterning physically-large energy-harvesting devices that are capable of providing more than enough power for the system. As an example, we have tested the radio by powering it using a flexible thin-film 550 cm^2 a-Si solar module (Figure 2.13). With all components based on the same a-Si technology, it is possible to apply the radio-integrated sheets envisioned onto surfaces without the need for providing/distributing any additional power source.

Circuit design, analysis and measurements for the thin-film radio was done by this author in collaboration with Liechao Huang (and Yingzhe Hu). All thin-film fabrication was performed by this author.

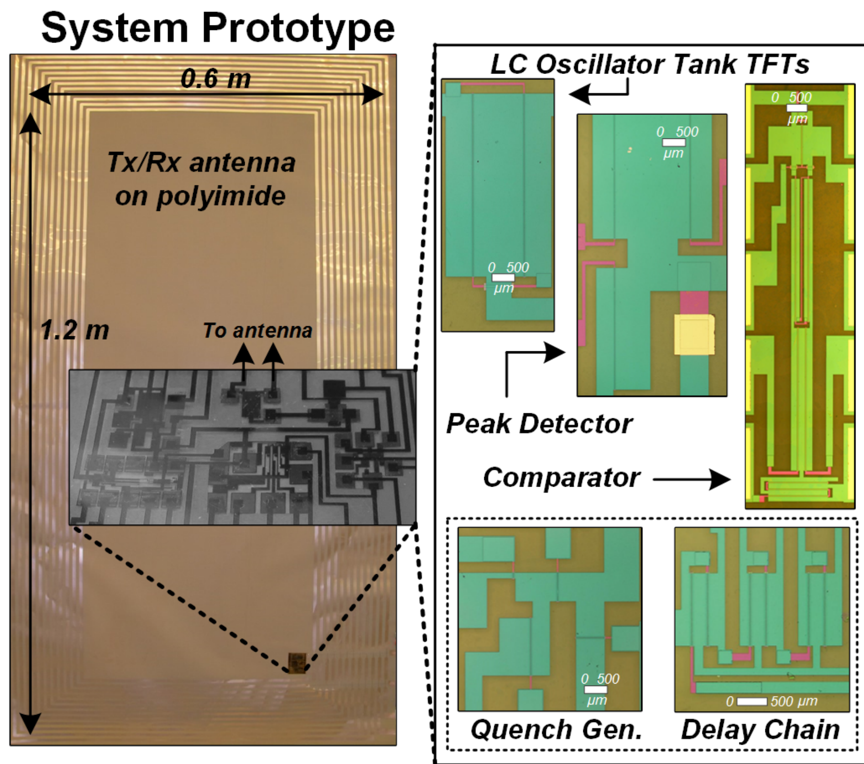


Figure 2.11: System micrographs

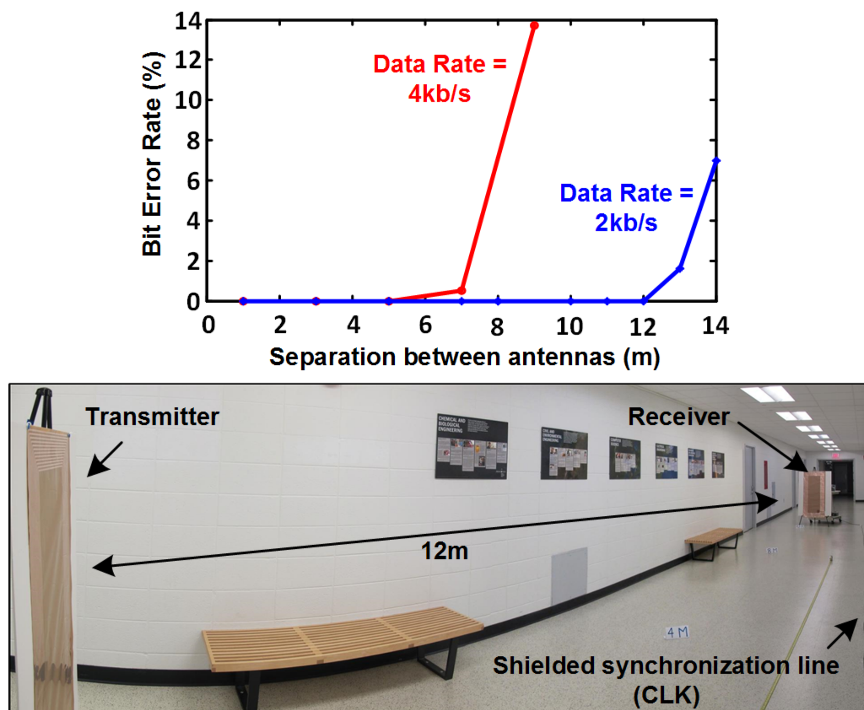


Figure 2.12: Bit error rate as a function of distance

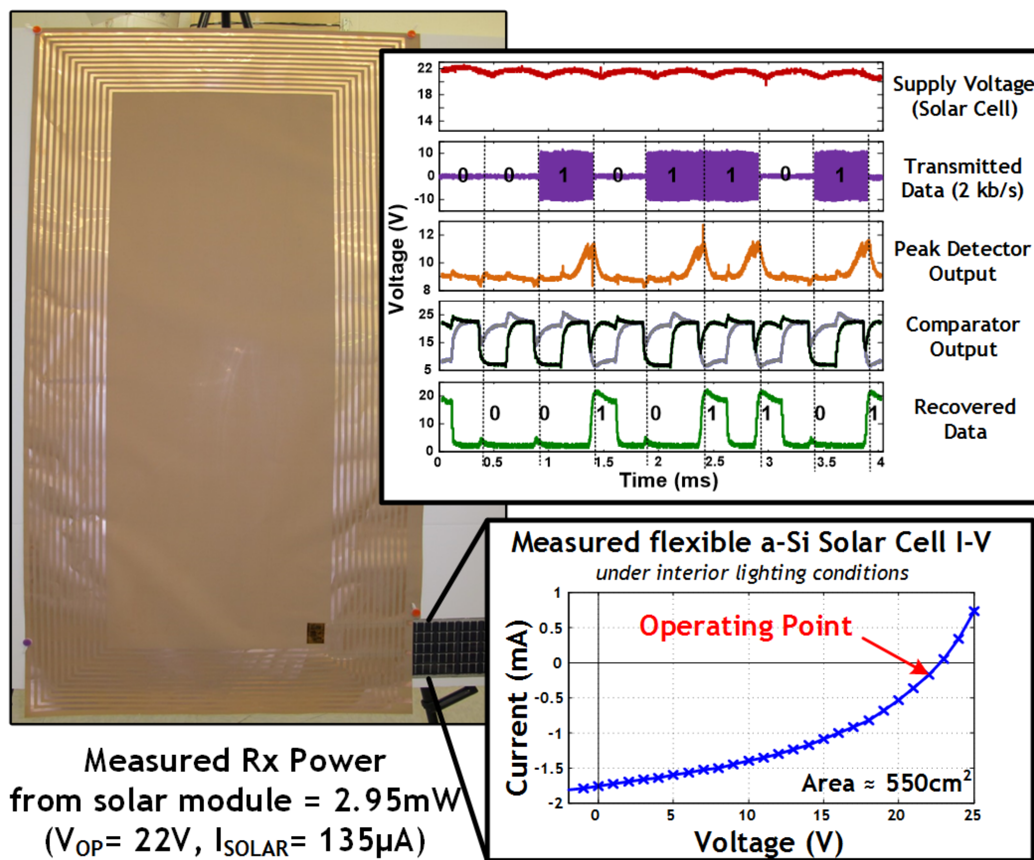


Figure 2.13: Self-powering of the thin-film radio on plastic

Part IV

Sensing Systems

Chapter 1

Introduction

The ability to create powering and communication blocks which we have seen in Parts II and III allows us to augment the core functionality of the key thin-film functionality of hybrid systems: sensing.

As described at the start of this thesis, large-area electronics has enabled the creation of a wide range of diverse thin-film transducers on large (potentially flexible) substrates, making possible physically distributed sensor arrays. As an example, as of 2015, Gen 10 thin-film manufacturing facilities have glass panel processing capabilities on the order of $9\,\mathrm{m}^2$ [47]. These are likely to keep increasing in size, and carrier substrates will continue to diversify. As such, architectures for scalable access and readout of large numbers of thin-film sensors will gain in importance. In the next few chapters, we present approaches to achieve this in the context of a system for Structural Health Monitoring (SHM). In particular, thin-film circuits are used that are realizable using similar thin-film fabrication technologies.

Chapter 2 introduces the SHM system followed by Chapter 3 which describes two low-speed scan-chains for reading out from thin-film sensors. In Chapter 4 we describe two sensor access readout interface circuits (one for a resistive strain gauge and the other for TFT-based strain sensors).

Chapter 2

Structural health monitoring

A number of severe infrastructure failures in the US have brought increased attention to the plight of aging structures across the country and beyond. A specific example is that of bridges of which there are over 600,000 in the US[24]; out of those, recent estimates suggest that **over 11% of highway bridges are structurally deficient**.

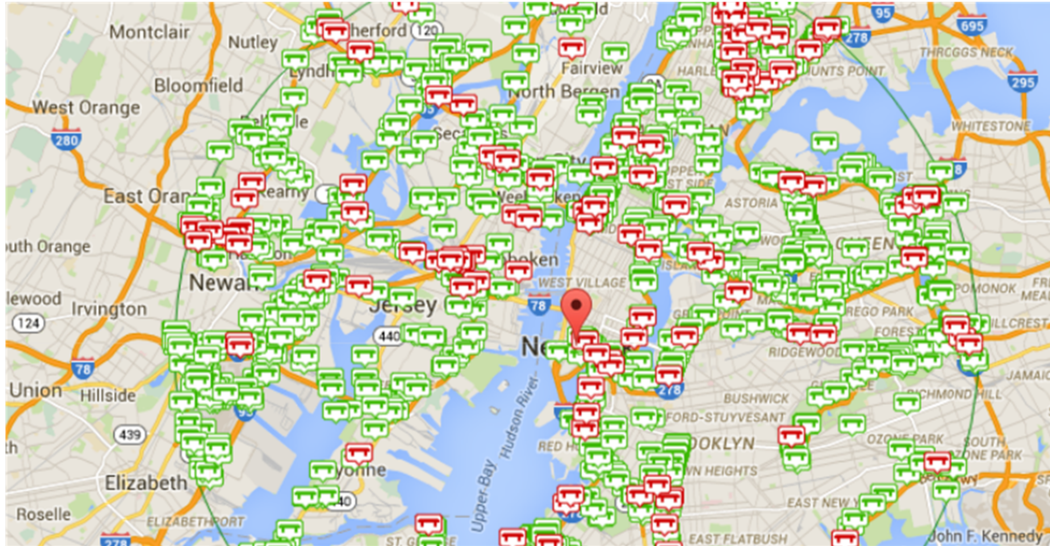


Figure 2.1: Structurally deficient bridges as of April 2015 in the NY area, shown in red (Transport for America)[24]

This is illustrated in Figure 2.1 which in red highlights deficient bridges in the NY area alone. Whilst much progress was made in the early 90s to address this issue, the progress of repaired bridges has stalled in the last two decades [24]. Furthermore, a large number of bridges are not

deemed structurally deficient, yet are operated under larger loads than ever designed for and as such a much larger number of bridges may require attention (an example of this is the I-5 bridge that collapsed in the Skagit river in 2013). A strong need therefore exits to develop tools to aid in early-stage diagnoses of structural degradations, preventing collapses and providing continuous real time monitoring of structures; this is termed *Structural Health Monitoring*.

Several approaches exist for structural health monitoring, ranging from theoretical modeling to the embedding of optical sensors [63]. In most cases, these focus on measuring or identifying structural points (decks, cables, pylons, etc.) experiencing excessive stress; this is typically done through the proxy of the measurable quantity, *strain* which quantifies physical deformation. Two key challenges exist here:

1. Many SHM monitoring systems cannot be embedded into already-built structures,
2. The sensing resolution required to make the SHM effective is on the cm-scale, whilst many current techniques have sensors distributed at much further intervals [63], thus likely to miss the formation of cracks or defects.

In this chapter we look at how Large-Area Electronics could help address both of these challenges, through the formation of physically-large strain sensing sheets that can be conformally applied on arbitrary surfaces and contain dense sensing arrays.

2.1 System architecture

The structural health-monitoring *hybrid* system, which we have developed in a sheet-like format integrates a large number of functionalities as shown in Figure 2.2[64]. These include:

- Thin-film power harvesting and distribution,
- Thin- or thick-film sensors,
- Thin-film sensor access and readout interface circuits,
- A CMOS IC that performs voltage conversion and regulation, sensor readout and control,
- Non-contact transfer of power and signals between the large-area sheet and the CMOS IC.

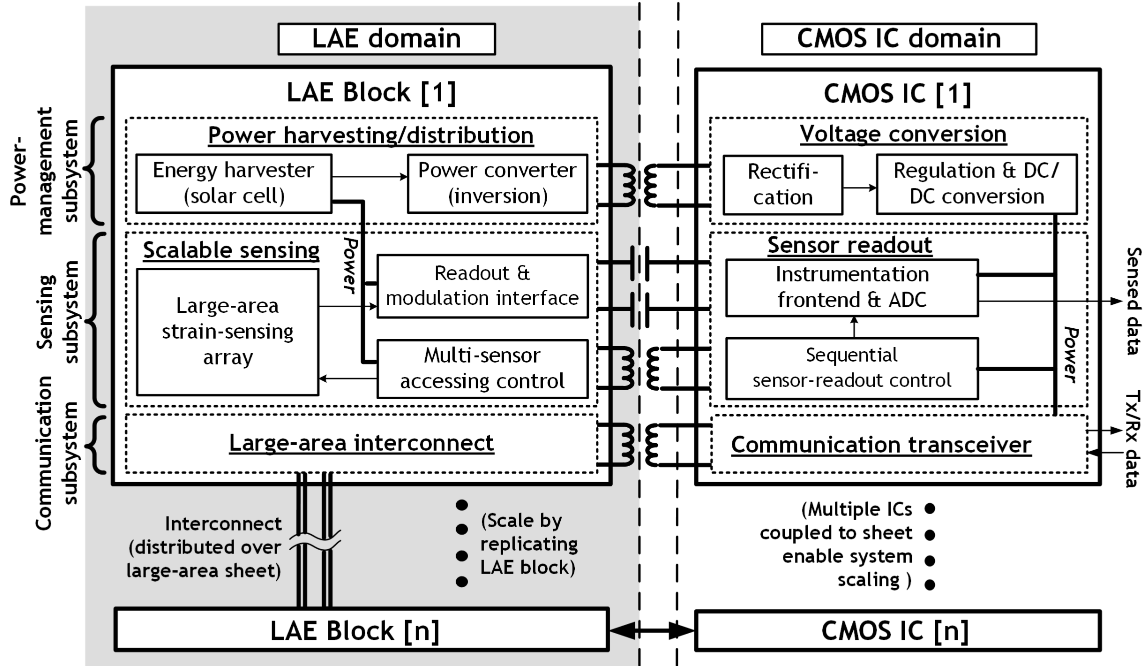


Figure 2.2: Self-powered hybrid system for large-scale strain sensing

The distribution of features between the large-area (thin-film) domain and the CMOS domain is chosen to leverage the complementary strengths and weaknesses offered by LAE and CMOS as described in the introduction of this thesis. The power-harvesting and distribution blocks are implemented using an LC oscillator as described in Part II Chapter 4, with CMOS components as described in [64]. In the following sections we explore in detail the thin-film implementation and design of the other sensing subsystems, highlighting techniques to reduce the number of interfaces between the thin-film large-area sheet and the CMOS IC.

Figure 2.3 shows a block diagram of the sensor-array interfacing circuits. These circuits provide (1) access and (2) readout from the sensor-array. On the left is the small CMOS IC sheet, and on the right a large-area sheet with a large number of TFT sensors.

The first block of the system is a TFT circuit that allows for the sequential access of these many sensors, controlled by the CMOS IC. The key idea is that for ease of assembly, it is highly desirable to minimize the number of interfaces between the two sheets. The multi-sensor access control block thus takes a small number of signals from the IC over inductive links and generates a large number of sensor control signals.

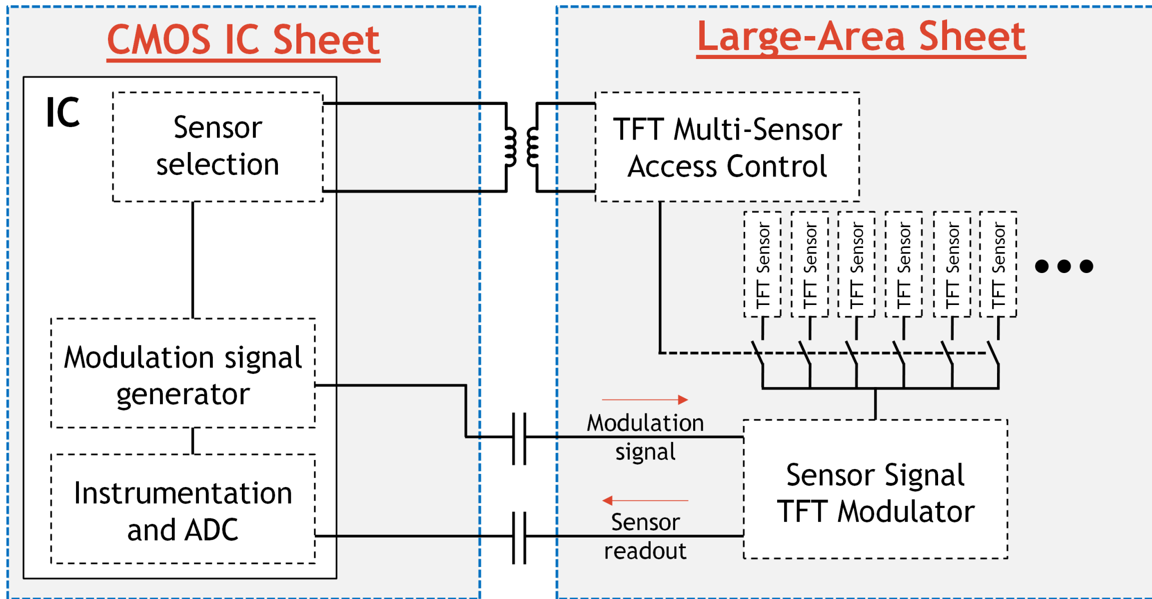


Figure 2.3: Sensor sub-system architecture with non-contact interfaces

As shown these sensors are thus multiplexed onto a single output channel which is fed into a TFT-based modulator. For this block, the modulation signal comes across a capacitive interface from a signal generator on the IC. The output modulated signal is then returned to the IC through another capacitive interface, and processed using custom instrumentation.

Chapter 3

Circuits for sensor access control

In this chapter, we first focus on the sensor access-control circuits. While the IC operates at 1.2V, the a-Si TFT circuits need over 5 V for reasonable performance as a result of threshold voltages on the order of 1-2V. Inductive non-contact interfaces can provide voltage step-up according to the turns ratio of the primary and secondary coils. Figure 3.1 shows the schematic of the inductive interface, which includes a thin-film demodulator constructed using thin-film Schottky nanocrystalline diodes as described earlier to minimize the voltage drop across the demodulator.

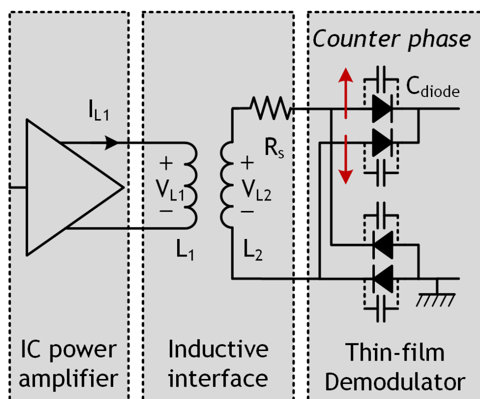


Figure 3.1: Inductive interface offering voltage step up of control signals

A key challenge, however, is the thin-film diodes, which, due to AC conduction, would limit the demodulation of high input frequencies. To overcome this a full-wave rectifier topology is adopted, wherein the high-frequency signal appears at the demodulator inputs in counter phase.

We demonstrate this interface rectifying successfully at 1.5MHz (though it has also been measured to provide good rectification well beyond 20 MHz).

The rectified control circuits are then passed to a low-speed scanning circuit developed to generate sequential enable signals to access individual sensors.

3.1 Low-speed scan chain for multiplexing

Figure 3.2 shows the low-speed scanning circuit architecture which generates the sensor enable signals EN<N>.

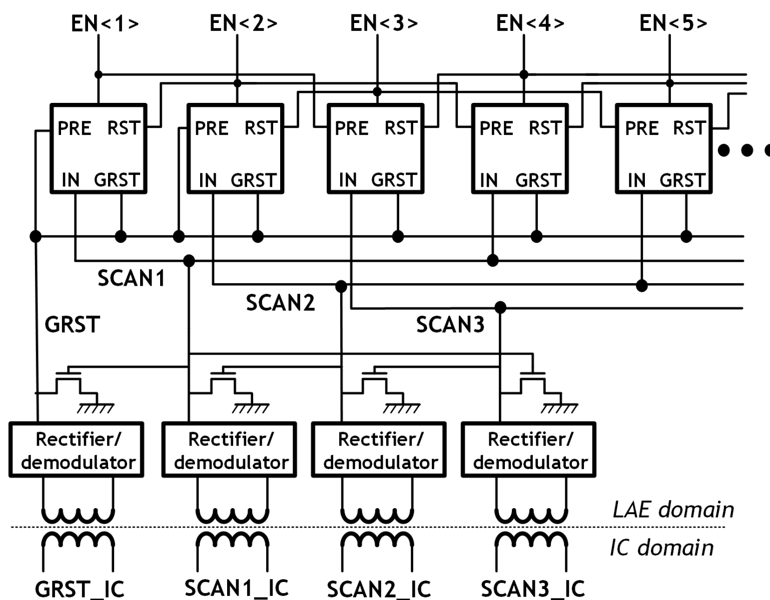


Figure 3.2: Thin-film large-area circuits for access control of multiple sensors

An important attribute is that this circuit requires just four control signals from the IC interface to enable multi-sensor accessing. GRST serves as a global reset and SCAN1–3, which are asserted in a round-robin manner, form three-phase control signals for stepping through the chain.

As described in earlier sections, a key challenge with LAE TFTs is that they typically present only unipolar devices; for instance a-Si:H TFTs are predominantly NMOS devices. In order to preserve full-swing voltage levels (>6V) through the scan chain, we develop a circuit that operates using *three-phase control*. Specifically, the use of three-phase control allows us to create a dynamic pass-transistor topology, enhanced by bootstrapping. Figure 3.3 shows the core of the circuit and Figure 3.4 shows measured waveforms.

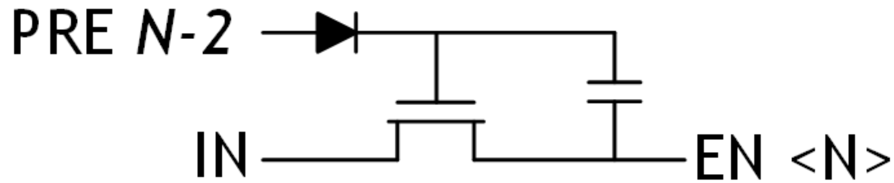


Figure 3.3: Bootstrapped, dynamic pass-transistor logic circuit

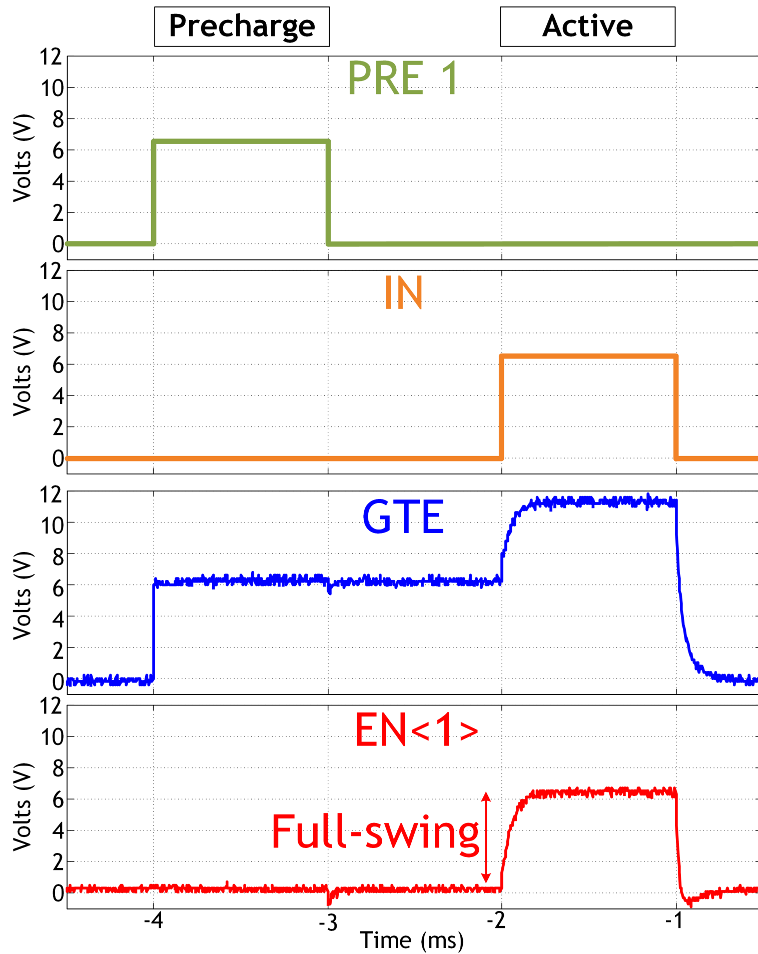


Figure 3.4: Waveforms for the bootstrapped scan chain element. The GTE waveform is the signal at the gate of the bootstrapped pass-transistor

The Nth scanning element receives a precharge signal (PRE) from the N-2 element to precharge its bootstrap capacitor through a Schottky-barrier TFD. Then, two phases later, its input (IN) is asserted, generating a full-swing output enable (EN<N>) through the pass transistor. Figure 3.5 shows the full circuit of the scanning element which adds 4 TFTs which help to perform resetting of the scanning element. This is achieved through a reset signal (RST) that is received from the

N+1 element, discharging both the output and bootstrap capacitor. All TFTs used in the scanning circuit have a W/L of 500/10μm to ensure a large drive current)

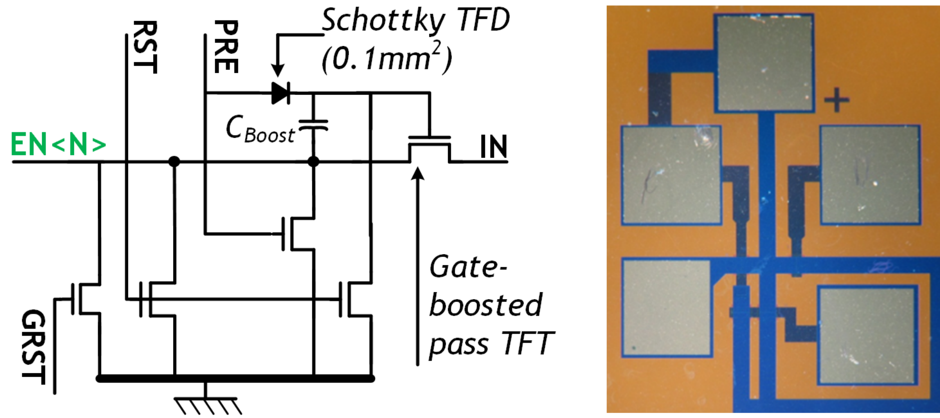


Figure 3.5: Complete thin-film scanning circuit (and micrograph)

Figure 3.6 shows the measured waveforms of the thin-film access control circuits (for multiple scan elements). The 1.2V, AC-modulated control signals from the prototype IC (SCAN1—3_IC) are stepped up to 6V and rectified. Round-robin assertion of the stepped up SCAN1—3 signals generates the sequential enable signals (EN<N>).

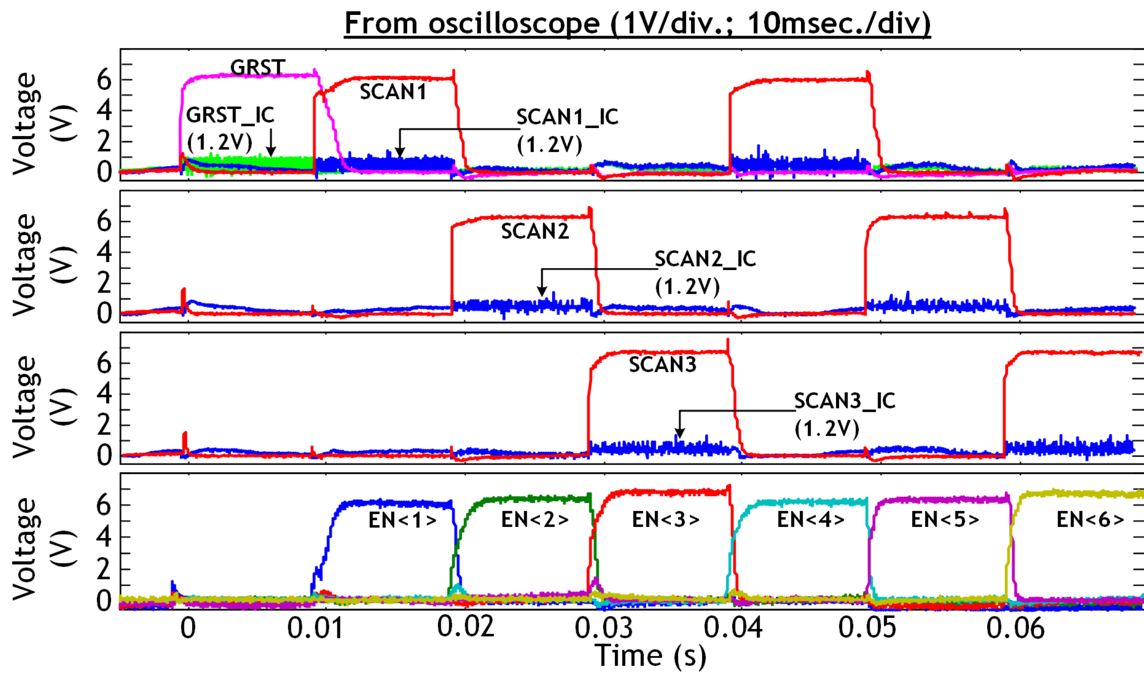


Figure 3.6: Waveforms for enable signals EN<1-6>

Up to 10 cascaded elements were demonstrated, all fabricated on plastic an assembled on a copper backplane as shown in the Figure. Intermediate testing of each scanning element is performed as shown in Figure 3.7 using micro-alligator clips.

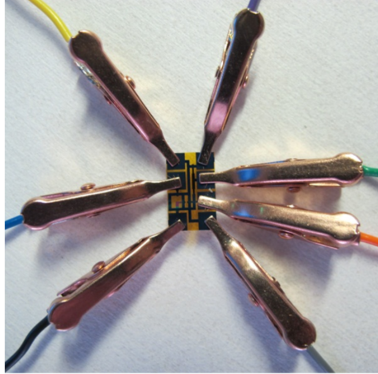


Figure 3.7: Individual testing of scan elements prior to assembly on a flexible copper backplane

The maximum access speed is 500 Hz, limited by the charging of the output node (measurements performed with a 100pF capacitive load).

In order to realize the circuit shown in the micrograph in Figure 3.5, well-performing capacitors, crossovers and vias are required. Integrated capacitors are fabricated as shown in Figure 3.8(a); a metal-insulator-semiconductor-metal structure is adopted rather than a simple metal-insulator-metal since the latter was shown to be susceptible to shorting, probably as a result of pinholes through the insulator. A typical capacitance of 200pF/mm^2 is achieved. A similar structure is used for metal-layer cross-overs with the TFT active layer retained, except that the metal intersection area is minimized to minimize the coupling capacitance at the crossover.

Purely metallic vias are realized as shown in Figure 3.8(b); typically these are at least 0.2x0.3mm and demonstrate a low resistance on the order of $2\,\Omega\,\mathrm{mm}^2$. This is in contrast to metal-n$^+$ a-Si-metal vias which present several 2-3 order of magnitude larger via resistance.

3.2 Three-phase coupled scan chain

The scan circuit described in the previous sections requires control signals from a CMOS IC. Even though only a small number (4) are required, an alternative possibility is to generate the low-frequency control signals directly in the thin-film domain using TFT circuits. We demonstrate this using the three-phase non- overlapping clock generator shown in Figure 3.9.

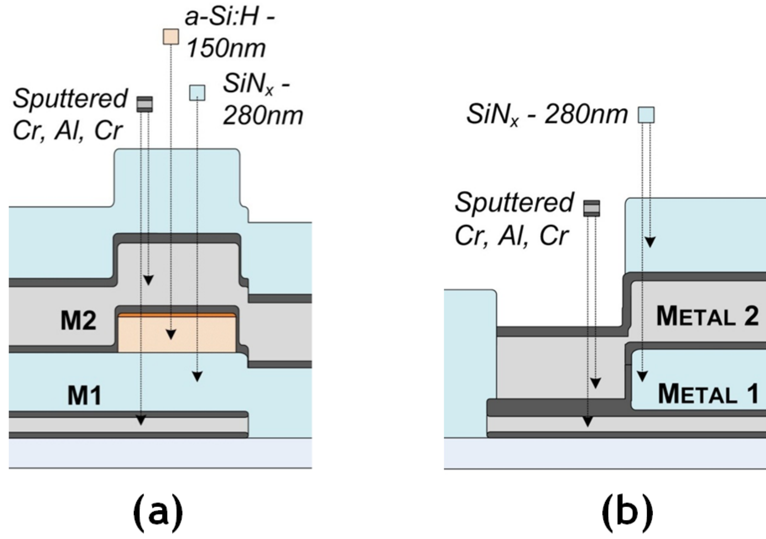


Figure 3.8: Thin-film designs required for circuit realization (a) caps/cross-overs (b) vias

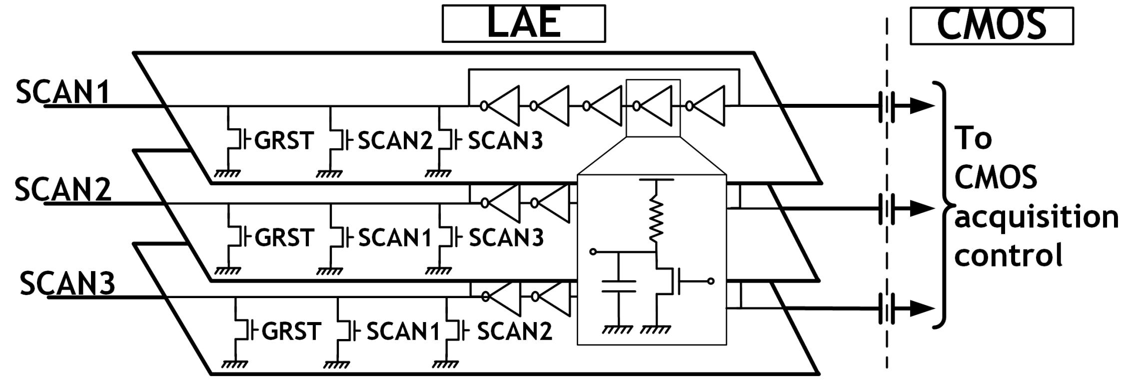


Figure 3.9: LAE-based three-phase control is achieved using NOR-gate coupled TFT oscillators and interfacing with IC is achieved capacitively to enable edge detection for synchronization

The circuit consists of three ring oscillators (as described in Part II) implemented by resistively-loaded inverter stages. The ring-oscillator outputs are coupled using an effective three-input NOR gate to achieve non-overlapping SCAN1—3 signals (note, GRST is provided by the IC through an inductive interface as previously). Due to the use of free-running oscillators, the duration of each signal is imprecisely controlled. However, the benefit is that coupling to the CMOS IC does not require voltage step up or AC-modulation, thereby reducing power consumption in the IC. Rather, the SCAN1—3 signals can be provided directly to the CMOS IC via capacitive coupling; as described below, the IC then performs sequential sensor acquisition by detecting the SCAN1—3 edges, which can be done robustly thanks to the high-speed CMOS transistors. Figure 3.10 shows

waveforms illustrating this three-phase control. As can be seen, the oscillators are not completely balanced, however symmetry can be achieved through optimization of the oscillator loads.

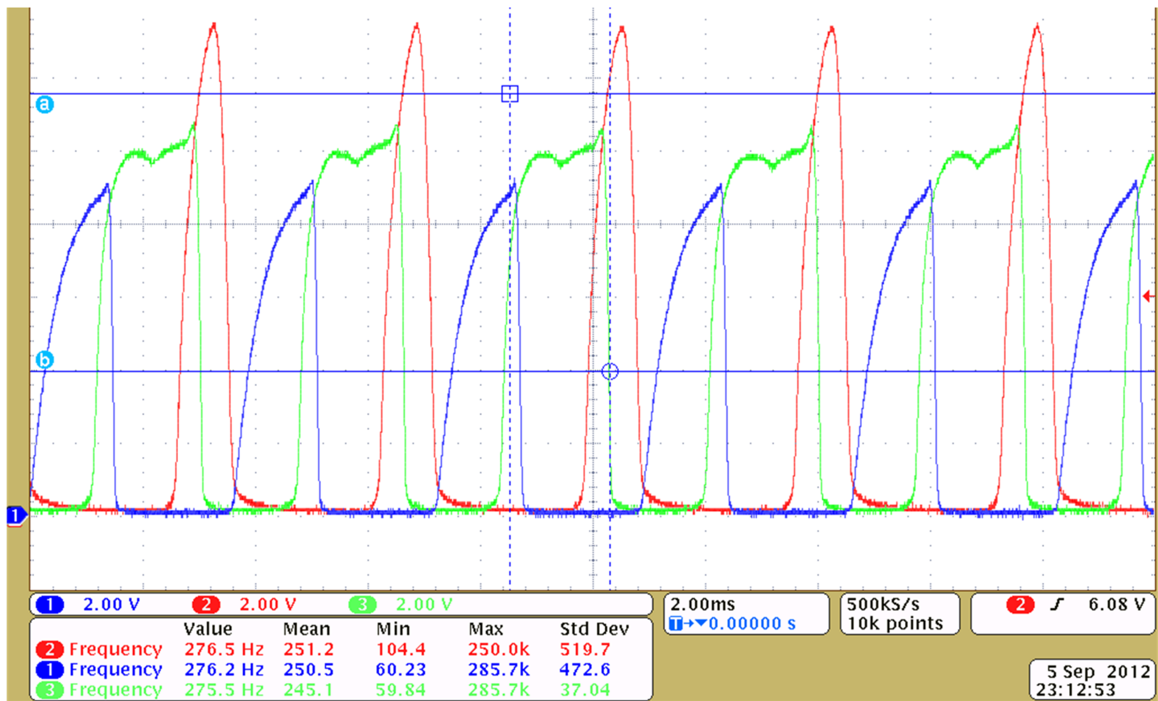


Figure 3.10: Waveforms for the LAE-based three-phase control is achieved using NOR-gate coupled TFT oscillators and interfacing with IC is achieved capacitively to enable edge detection for synchronization

Chapter 4

Circuits for sensor readout

Having discussed the sensor access control circuits, in this section we look at two topologies that can be used to take a sensor output and modulate it for transfer over a minimal number of non-contact interfaces. We consider readout from two types of sensors:

- Thick-film resistive strain gauges
- Strain-sensitive thin-film transistors

4.1 Strain sensing with thick-film resistive strain gauges

In this first implementation, the sensor units consist of thick-film constantan resistive strain gauges (Omega SGT-4/1000-FB13) in a bridge configuration, as well as TFT access switches as shown in Figure 4.1.

The bridge configuration is standard for strain monitoring applications, with reference strain gauges in each branch oriented orthogonally to enable measurement of the relative strain between two axes. The individual strain gauges have a resistance that is altered under relative strain due to geometric changes caused by mechanical deformation such that:

$$\text{strain} = \frac{\Delta L}{L} = \frac{1}{G}\frac{\Delta R}{R}$$

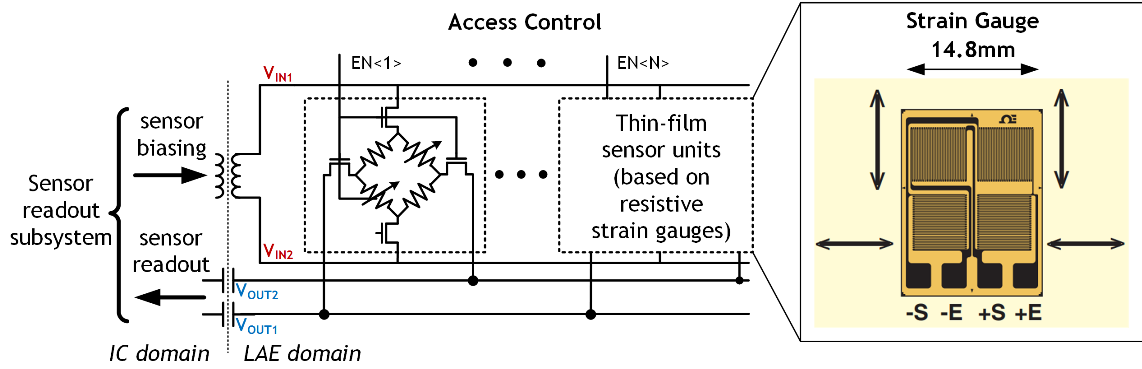


Figure 4.1: Sensor array circuit and strain gauges

where G is a parameter known as the gauge factor. The strain gauges are calibrated for aluminium beams and have a standard resistance of $\approx 1\,\mathrm{k}\Omega$. The bridge is excited using a differential AC sensor bias $V_{IN1} - V_{IN2}$ (200kHz, thus below f_t) across the top and bottom of the bridge (such that minimal common mode signals are generated at the sensor bridge outputs), and the output of the bridge is returned to the IC over a capacitive interface. Figure 4.2 illustrates this, with in (a) the switches activated by an enable (EN) signal, and in (b) with the switches deactivated.

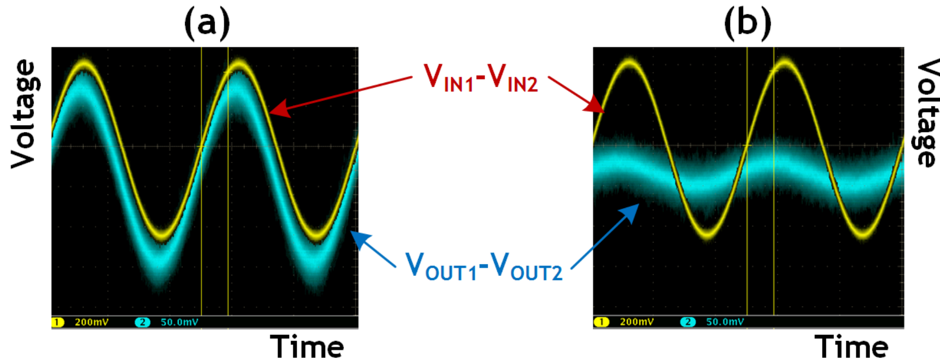


Figure 4.2: Sensor readout waveforms

CMOS Readout circuits consist of a synchronous Gm-C integrator followed by a ADC (described in [61])

4.1.1 Wide interdigitated TFTs for sensor access

Large TFTs with W/L of 60000/6μm are used for the access switches, to provide sufficiently-low on-resistance ($\approx 1.5\,\mathrm{k}\Omega$ at V_{gs}=6V), comparable to the nominal strain-gauge resistance. The material

stack is identical to that of the our standard amorphous silicon TFT, but the source-drain contacts are interdigitated for compactness as shown in Figure 4.3.

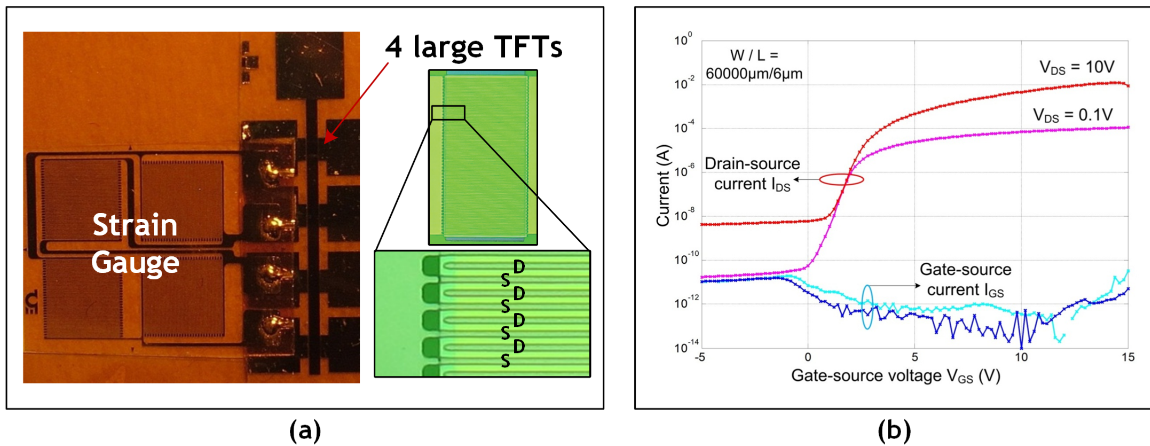


Figure 4.3: Interdigitated thin-film transistors (a) micrograph (with the 4 TFTs and an enlarged view), (b) I-V curve

A common gate is used across all the interdigitations; as such the capacitive load on the scanning circuits is quite large with a total loading of $\approx 700\,\text{pF}$ ($180\,\text{pF}$ each) on the access-scanning circuits; they thus limit the maximum speed of readout.

The source-drain leakage is also unexpectedly high. This was most likely a result of a slightly inappropriate layout of the device, with the gate not underlying the full active region as shown in the mask layout overview as shown in Figure 4.4. This means that some regions of the active region are slightly free from the influence of the gate, which may result in the leakage observed.

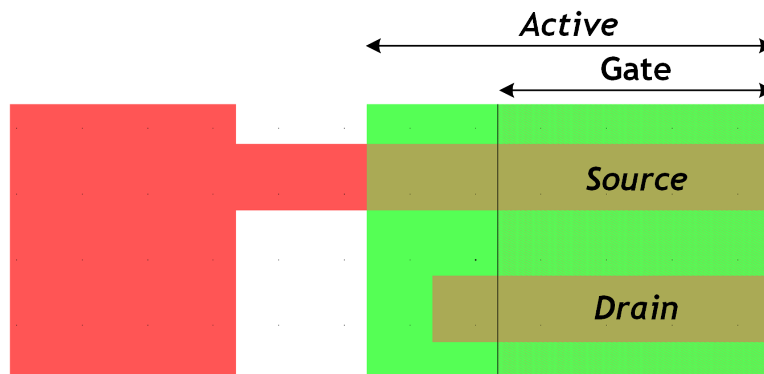


Figure 4.4: The gate of the interdigitated TFT does not fully underly the active region

4.1.2 System for strain readout measurements

The complete system components are shown in Figure 4.5.

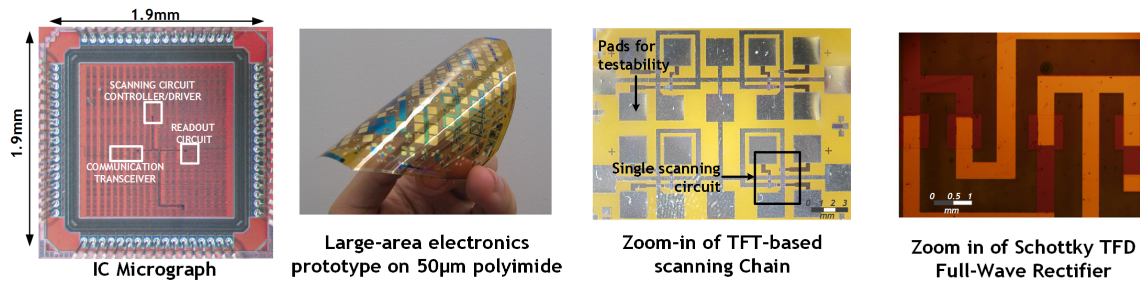


Figure 4.5: Micrograph of the 130 nm CMOS IC and large-area electronics components fabricated on polyimide foil

To characterize the readout subsystem, tests were performed using the resistive strain sensors. Figure 4.6(a) shows the strain-measurement setup in the lab, where the LAE sensors were bonded to a 180 cm cantilever beam which was loaded with known weights.

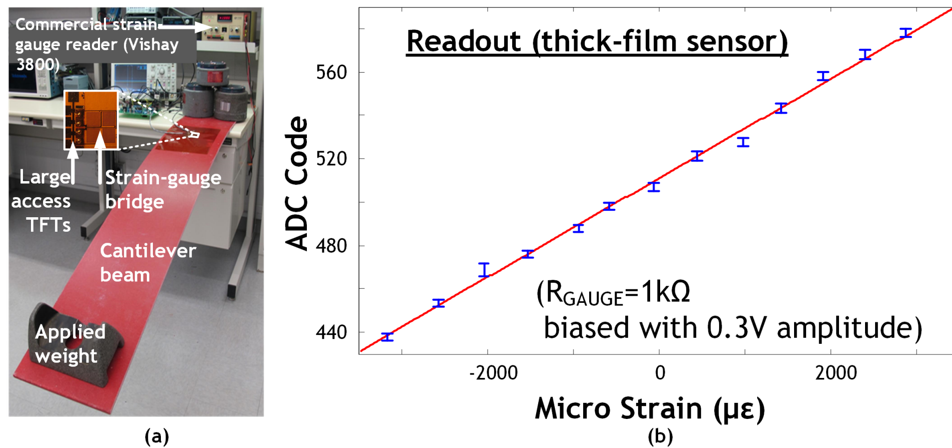


Figure 4.6: Readout circuit (a) test setup on cantilever beam, (b) test result with constantan strain sensors under tension and compression

Reference strain sensors, read by a commercial system (Vishay 3800), were also bonded for comparison. Figure 4.6(b) shows the measured readout curves from the prototype for the constantan strain sensors. The x-axis shows the strain (ratio of length deformation to nominal length), measured using reference sensors read out via the Vishay 3800. The maximum non-linearity is 20.7 μStrain (1μStrain= 1×10^{-6}) and the readout noise is 17.9 μStrain_{RMS}. The total readout energy is 270 nJ/measurement.

4.2 Strain sensing with thin-film transistors

In this second implementation, the sensor units consist of thin-film transistors. The topology described below enables non-contact current-readout from TFTs, which have previously been demonstrated as having rich physical responses to a variety of different processes [65][66][67][68].

4.2.1 Strain response of TFTs

Strain sensing is realized through the mobility response of a-Si TFTs. To characterize the TFT strain sensor, the TFT current was read using a transimpedance amplifier. TFTs ideally exhibit a linear mobility relationship with strain as shown by the measurements from fabricated TFTs plotted in Figure 4.7. Under tensile strain, the mobility increases whilst under compressive strain, it decreases.

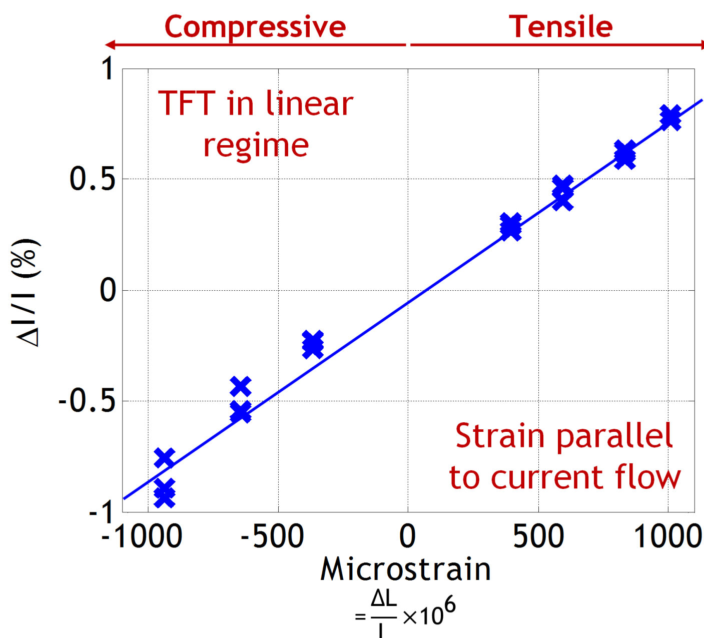


Figure 4.7: Mobility response of TFT-based strain sensors

Consequently, the TFT current can be used to derive a gauge factor:

$$G = \frac{\frac{\Delta I_{DS}}{I_{DS}}}{\frac{\Delta L}{L}}$$

where I_{DS} is the TFT drain-source current and L is the length of the TFT channel along the direction of strain. This is measured to be approximately 7.5 with a 3600/6μm TFT biased in the linear regime (V_{GS}=10V, V_{DS}=2V). This compares well to previous reported measurements of the gauge factor of amorphous silicon TFTs [3]. Compared with resistive strain sensors, which have a gauge factor of ≈2 and are widely used, TFTs give greater response.

4.2.2 Differential Gilbert modulator

A challenge with TFT-based sensors is that the output signal, which is typically their current, is DC. Readout over a non-contact interface therefore requires AC modulation. This is achieved using the TFT-based Gilbert-type modulator shown in Figure 4.8.

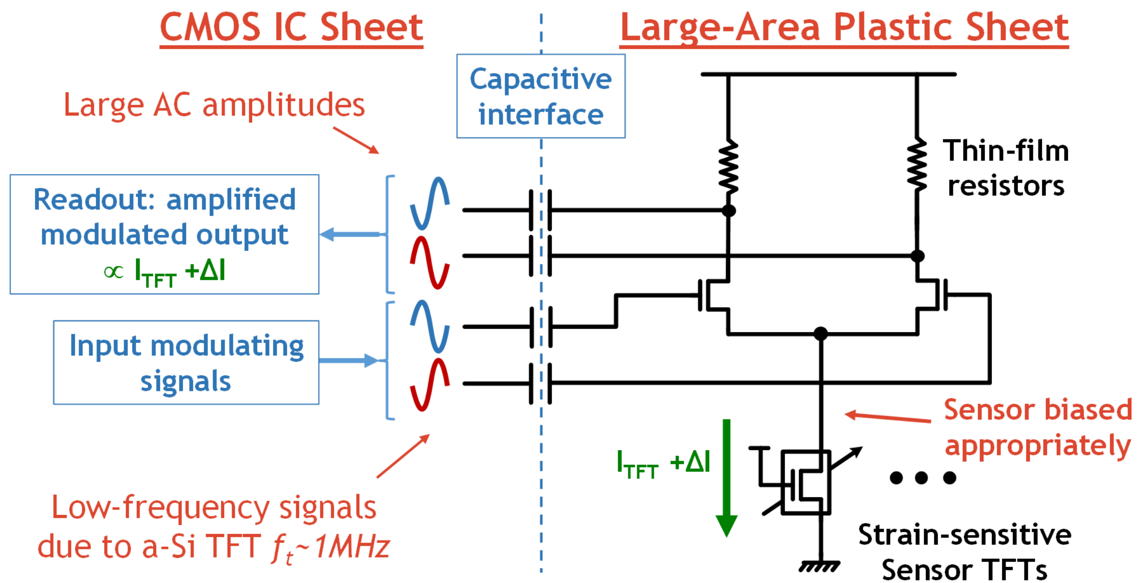


Figure 4.8: Gilbert-type modulator for DC-AC modulation of the TFT sensor current

The Gilbert-type modulator consists firstly of a primary-TFT differential pair structure (M1/2), with thin-film n+ a-Si resistive loads (30 MΩ/sq); a TFT sensor serves as the tail current source (T3), biased in an appropriate regime for sensing mobility changes as a result of applied mechanical strain. The two inputs to the differential pair TFTs (T1/2) are counter-phase sinusoidal signals, which generate an amplified and AC-modulated output whose amplitude is proportional to the sensor-TFT (T3) current. This differential AC output can then be capacitively (wirelessly) coupled to an IC for readout; for efficient transfer, capacitive readout is used due to the limitation in

operating frequency imposed by the low a-Si TFT ft of ≈1MHz (as described earlier). A modulation frequency of 100 kHz is thus used provided by the CMOS IC.

Such a structure, however, results in large AC amplitudes at the modulator output nodes, of which only a small fraction is representative of the actual strain-induced T3 current change. In addition, the intrinsic drain current drop due to TFT threshold voltage shift is also mirrored directly in this AC amplitude.

In order to overcome the additional drift source of correlated effects such as temperature, an additional TFT differential pair (T4/5) is used (also driven by sinusoidal inputs), whose outputs are connected to the outputs of the primary differential-pair structure, to cancel the sensor-independent signal. This is shown in Figures 4.9 and 4.10.

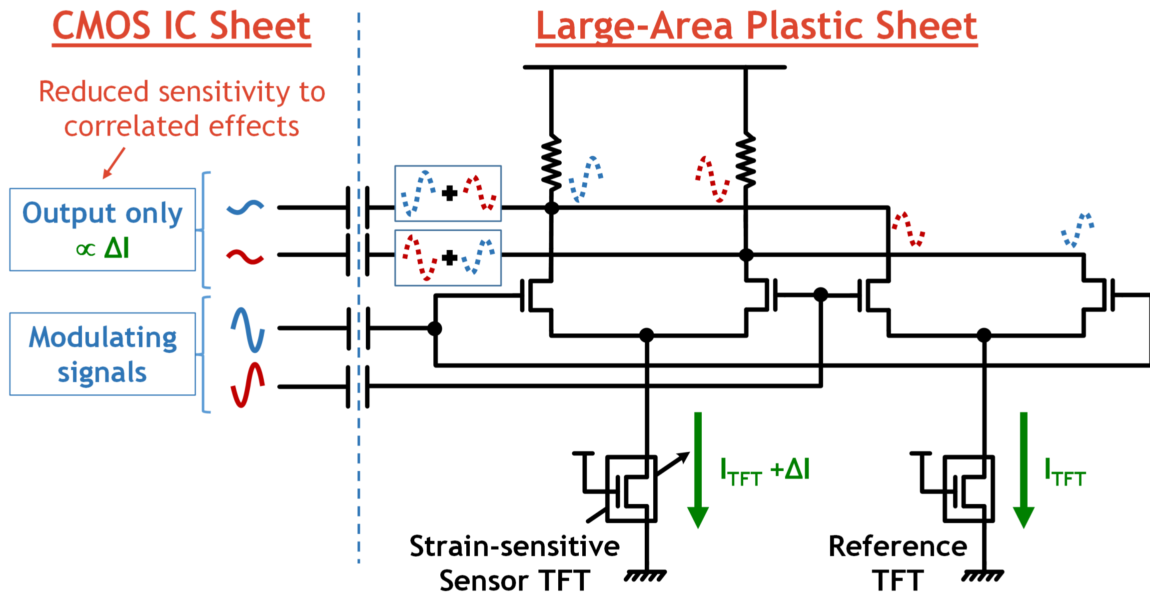


Figure 4.9: Thin-film differential Gilbert cell

This additional differential pair uses an orthogonally laid-out strain-invariant reference TFT as its tail current source (T6). Assuming TFTs T6 and T3 are fairly well current-matched and experience similar V_T drift, the effect of this drift on the output AC signal of the TFTs is mitigated. Using the described architecture, readout can be achieved from multiple TFT sensors by selectively gating each TFT sensor into the Gilbert-cell tail using a series of TFT interdigitated access switches as described in the previous section. A micrograph of the complete differential Gilbert modulator is shown in Figure 4.11.

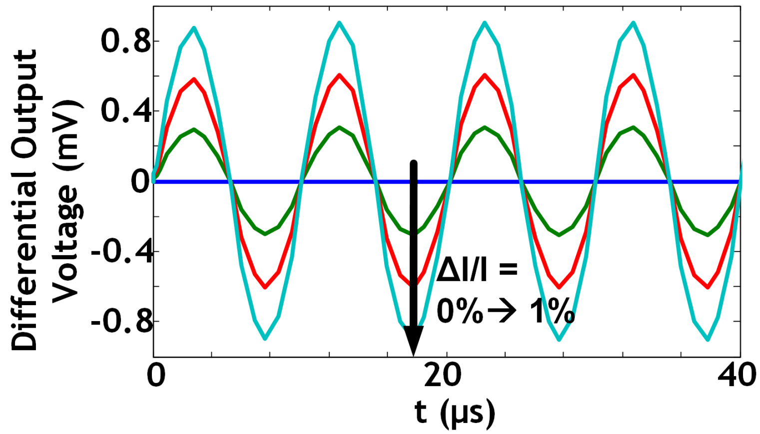


Figure 4.10: Simulations showing the output voltage generated due to different $\frac{\Delta I_{DS}}{I_{DS}}$ from the TFT sensors

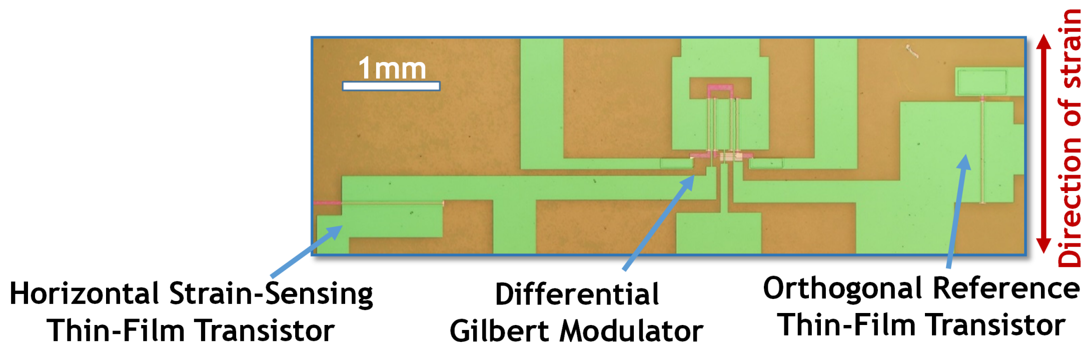


Figure 4.11: Micrograph of the complete Gilbert modulator on plastic

Typical waveforms for the single/differential modulators are shown in Figure 4.12.

4.2.3 System strain readout measurements

The complete system components are shown in Figure 4.13.

Once again, to characterize the readout subsystem, tests were performed using both a calibrated resistor and the LAE strain sensors. Figure 4.14 shows the strain-measurement setup in the lab, as before.

To characterize the integrated LAE-CMOS readout circuits, a variable TFT current source was used at the Gilbert-cell tail node; Figure 4.15(a) shows the response, with maximum nonlinearity of 45 μStrain and noise level of 106 μStrain$_{RMS}$. Figure 4.15(b)shows the strain-readout performance of the complete system using TFT strain sensors and LAE-CMOS readout circuits; the maximum

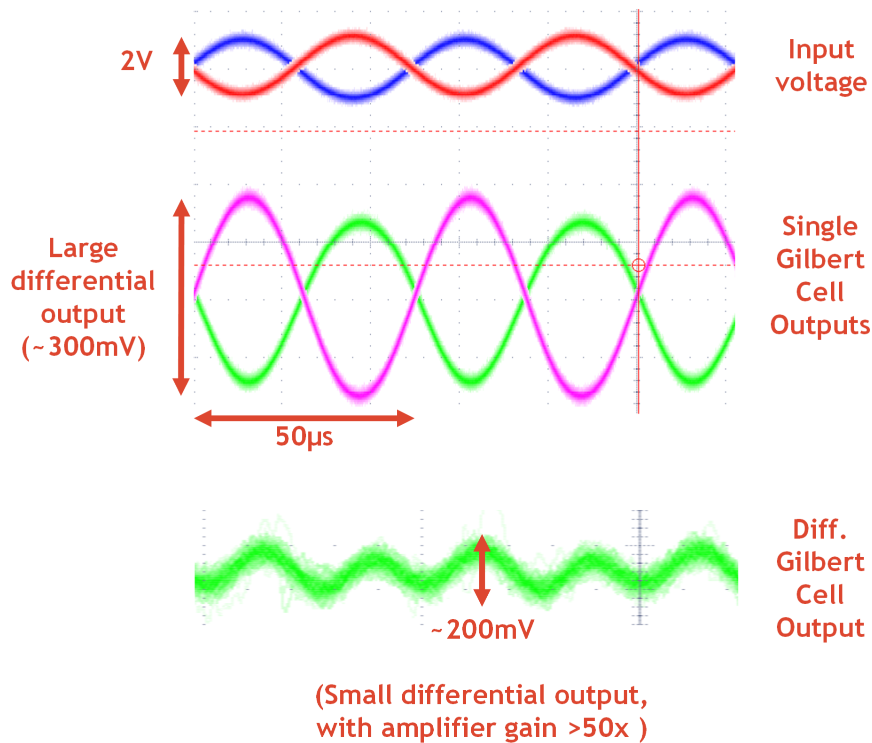


Figure 4.12: Differential setup substantially decreases the large output signals of the single Gilbert cell

nonlinearity and noise level are 180 μStrain and 141 μStrain_{RMS} respectively, which meet the requirements for damage detection in SHM applications [69]. The increased nonlinearity and noise are due to low-frequency threshold-voltage noise in the a-Si TFTs.

The maximum access speed is 500 Hz, limited once again by the operation of the LAE scan chain. The resulting IC energy/measurement is 148 nJ for acquisition and 286 nJ for IC-based sensor-access control.

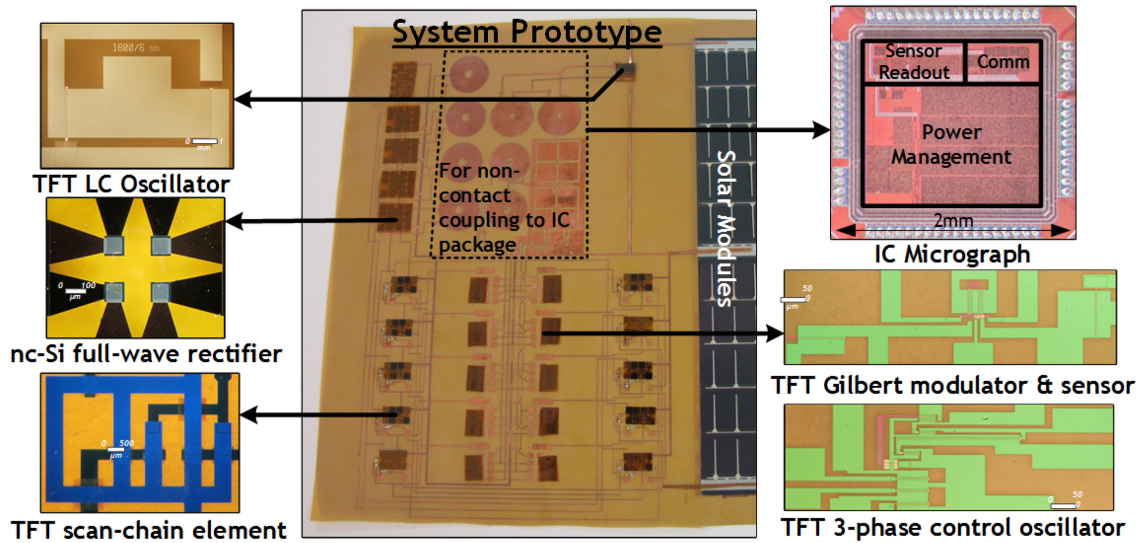


Figure 4.13: Micrograph of the 130 nm CMOS IC and large-area electronics components are fabricated on polyimide foil

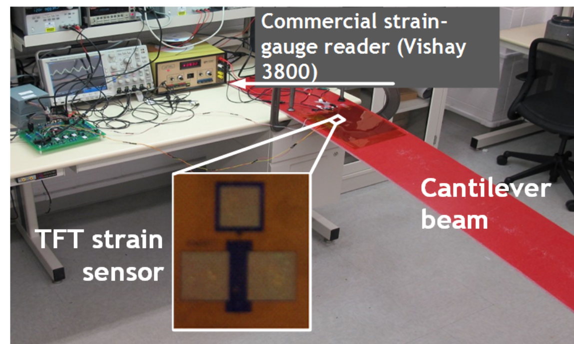


Figure 4.14: Test setup on a cantilever beam

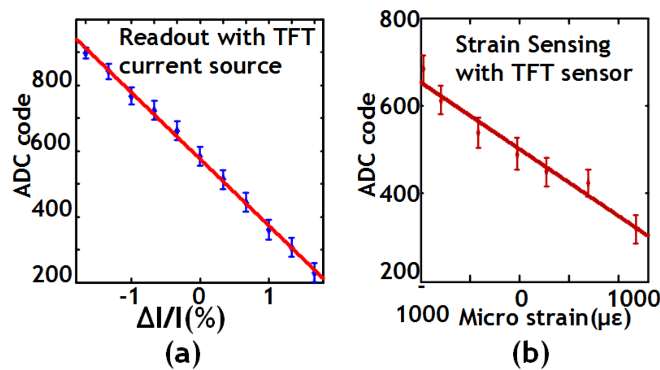


Figure 4.15: Sensor subsystem response showing (a) isolated readout performance of acquisition circuits obtained by using a calibrated TFT current source at the tail node of the LAE Gilbert cell, and (b) overall strain response of the system using TFT sensors

Chapter 5

Conclusion

In this part we presented the architecture and design of a scalable strain-sensing system for structural-health monitoring applications. The system combines LAE and CMOS technologies to leverage their respective strengths within power-management, sensing, and communication subsystems. To allow the functionality of each subsystem to be optimally distributed between the two technologies, non-contact interfaces based on inductive and capacitive coupling are employed. These substantially improve system scalability by avoiding metallurgical bonds at the inter- faces of the two technologies.

Two scan-chain circuits are presented that illustrate methods for generating many sensor access signals from a small number of interfaces from the CMOS ICs. Subsequently, two approaches for strain sensing and readout are described. The first technique uses reading out from copper strain sensors through large access TFTs. The second leverages the TFTs themselves as strain sensors (through a change in mobility) and enables readout through the use of Gilbert-type multiplier.

Circuit design, analysis and measurements in the systems presented was done by this author in collaboration with Liechao Huang, Yingzhe Hu and Josue Sanz-Robinson. Thin-film full-wave rectifier design was done by Josue Sanz-Robinson. Analysis of the effect of mobility on TFTs was done in collaboration with Josue Sanz-Robinson. All other thin-film designs and circuits described were fabricated and tested by this author. CMOS ICs were developed by Liechao Huang and Yingzhe Hu.

Part V

Augmenting Thin-Film Systems with Machine Learning

Chapter 1

Introduction

In this thesis, we have repeatedly noted the benefits of Large-Area Electronics (LAE) as a technology for sensing over physically large areas. One commercial example of this is X-ray imagers, which today integrate approximately ten million amorphous silicon pixels over planes that span 0.5x0.5m as shown in Figure 1.1.

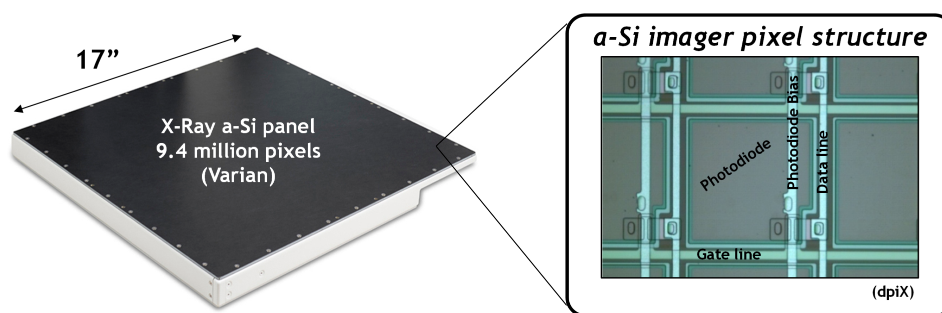


Figure 1.1: Physically large X-ray panels approach square meter dimensions

A key challenge in such systems though, as described in previous sections, is the interfaces from the large sensing-arrays: there now exists a large amount of distributed sensor data that requires processing and analysis. In particular, this is seen as a critical challenge to the continued scaling of such systems.

Two possible options for processing the sensor data exist. First, in addition to sensors, large-area electronics also enables the formation of Thin-Film Transistors (TFTs); these could be used to implement processing functions. Second, all of the sensor data can be sent to CMOS ICs for

processing; this results in hybrid systems based on, for example, amorphous silicon large-area electronics and CMOS [64].

In practice, the first option is challenging because low-temperature processing, from which LAE derives benefits in terms of sensing, also results in low electrical performance of TFTs as seen throughout this thesis. Typical mobilities (μ), unity-current-gain frequencies (f_T), and required supply voltages are orders of magnitude worse than those of silicon CMOS transistors. For example, as we have shown, n-channel a-Si TFTs achieve electron mobilities in the area of 1cm^2/Vs, unity-current-gain frequencies in the area of 1MHz, and threshold voltages over 1V (compared to approximately 500cm^2/Vs, 300GHz, 0.3V, for typical CMOS transistors). In addition, the TFTs exhibit high variability in important parameters such as threshold voltage and mobility. This can be seen in Figure 1.2, where these quantities are measured over an array of 100 devices that we have fabricated on a single glass substrate.

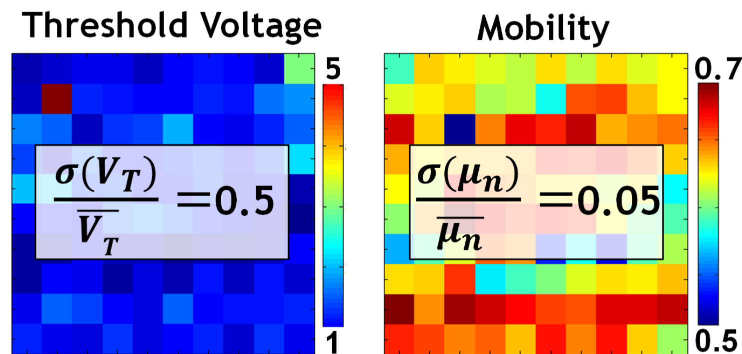


Figure 1.2: Variation in mobility (in cm^2/Vs) and threshold voltage (in V) across 100 thin-film transistors on a single glass sample

Given the disparity in electrical performance and reliability between TFTs and CMOS transistors, the hybrid system option is appealing. However, this now requires a potentially large number of physical interfaces between the two different technologies. For instance, afore-mentioned X-ray panels, commonly available today as shown in Figure 1.3, require thousands of such interfaces. The assembly associated with these poses a primary limitation to cost, reliability, and ultimately the scalability of these systems.

In this section, we propose an approach that addresses this interface challenge by taking data from many image-sensor pixels and processing them using simple, low-performance, variation-prone

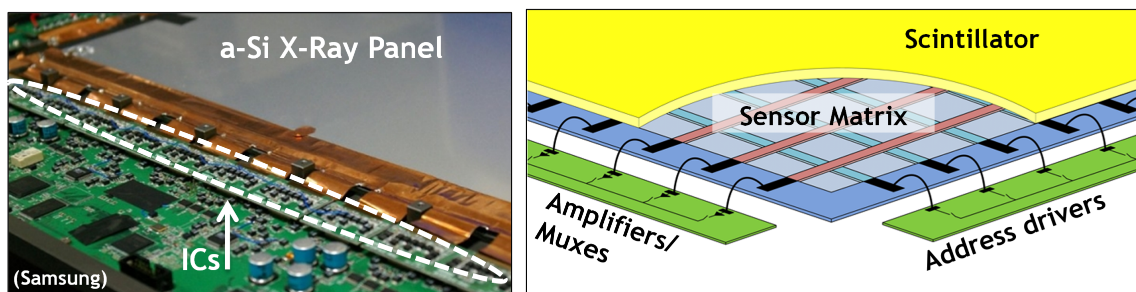


Figure 1.3: Current X-Ray imagers have thousands of interfaces to the sensing panel

thin-film circuits. This results in a reduced number of signals, which can then be transmitted from the large-area panel for the purpose of image detection and classification.

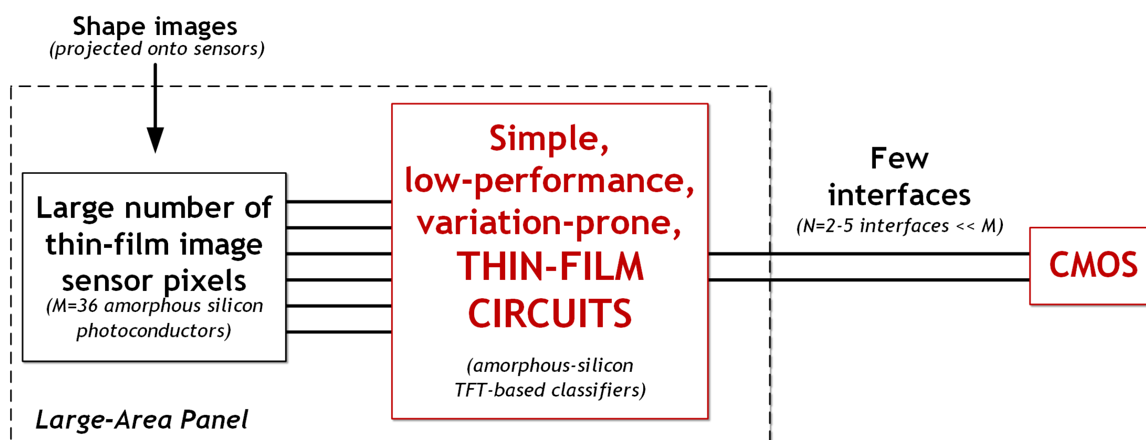


Figure 1.4: Reduction in interfaces from the large-area panel is achieved using simple thin-film circuits

This approach is illustrated in Figure 1.4. The driving insight is that a reduction in interfaces is achieved by transmitting only higher-level information, more closely tied to the application of interest, as opposed to the raw pixel data. In Chapter 2 we identify such information, which corresponds to elemental classification decisions can be derived using low-performance devices. These decisions are leveraged in a machine-learning algorithm to derive a high-accuracy classification decision. In Chapter 3 we describe the TFT circuits that implement the simple classifiers blocks required. Finally in Chapter 4 we demonstrate the complete image-detection system, classifying five shape classes with a performance close to that of a Support Vector Machine (SVM), a widely used strong classifier whose complexity precludes implementation using TFT circuits.

Chapter 2

Machine learning with low-performance devices

2.1 Machine-learning

A number of algorithms have emerged from the domain of machine learning that enable data-driven methods for modeling and analyzing application signals. This enables the creation of models for inference (i.e. making decisions) from data that may be too complex to otherwise model analytically. The particular inference we focus on in this work is the classification of shapes from image-sensor signals. Using machine-learning algorithms for classification, we can employ previously observed instances of data to create a model by which classification can be performed on future instances of data.

The basic operation of such a classifier is shown in Figure 2.1, consisting of two key components. The first component is a trainer, which is used to learn the classification model from previous data; this is typically performed off line. The second is the classifier itself, which uses the model to classify incoming data continuously and in real time.

Figure 2.1 illustrates the example of shape classification, detecting rings from all other shapes. A training set provides feature vectors along with labels of the shapes to the trainer. The trainer uses data mapped in a feature space, along with associated labels, to form a decision boundary. The representation of this boundary, referred to as a model, is then fed to a classifier, which distinguishes

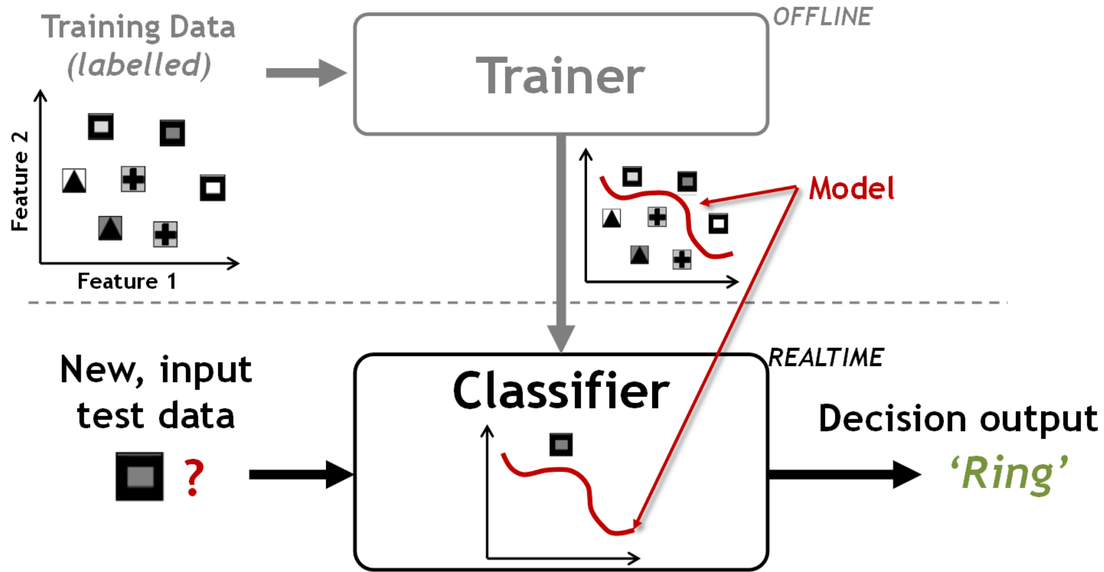


Figure 2.1: Architecture of a machine-learning classification system

rings from all other shapes from the incoming sensor data. Depending on how the data from the two classes (in this case rings versus other shape) is distributed in the feature space, a flexible and potentially complex decision boundary may be required. This is discussed in greater detail next, using actual data from the proposed system.

2.1.1 Strong and weak classifiers

In machine learning, there exist the concepts of a *strong classifier* and a *weak classifier*. A strong classifier is one that can be trained to fit arbitrary data distributions, while a weak classifier is one that cannot be. For this reason, weak classifiers typically result in a high rate of errors, typically dependent on the precise distribution of data in the application. For this reason, weak classifiers are often inadequate, and our ultimate objective is to create a strong classifier.

To motivate this more concretely, we present first a linear classifier, which is a weak classifier. A linear classifier is implemented by applying a weight, derived from training, to each input feature and then taking a linear combination over the weighted features; mathematically this amounts to a dot-product operation between the feature vector $\vec{x}$ and a model vector $\vec{c}$, derived from training. The result of the dot product is then compared to a threshold b, in order to make classification

decisions:

$$y = \begin{cases} \text{rings}, & \vec{c} \cdot \vec{x} > b \\ \text{other shapes}, & \vec{c} \cdot \vec{x} \leq b \end{cases} \tag{2.1}$$

Figure 2.2 shows data, corresponding to the actual shapes from the image-detection system demonstrated (specifically, rings versus all other shapes). The feature vector is the 36 raw outputs from image-sensing pixels (photoconductors), onto which shape images have been projected.

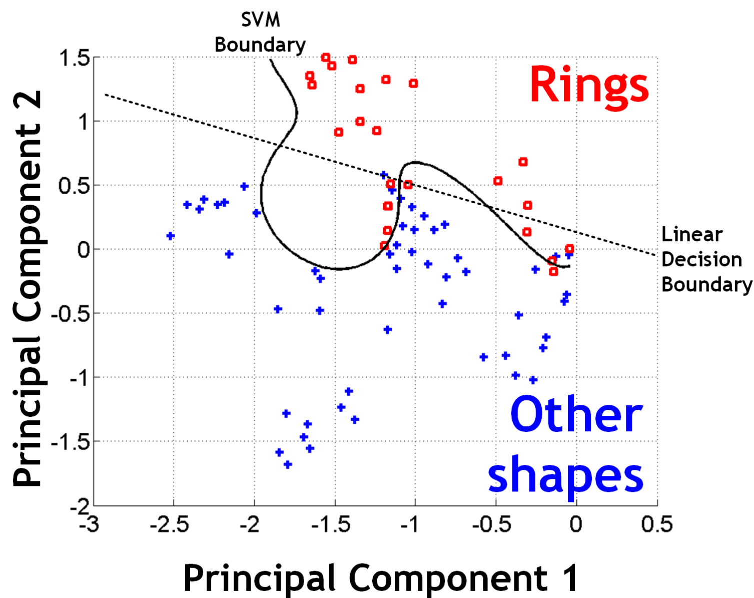


Figure 2.2: Measured image data illustrates the inadequacy of linear decision boundaries

While the actual feature vector dimensionality is 36, to help visualize the data, principal component analysis is performed, projecting the data vectors onto two principal components. A linear-classifier decision boundary, obtained from training, is also shown. As seen, such a boundary is inadequate, resulting in many of data points being misclassified. A more flexible decision boundary from a strong classifier is required, as obtained from training an SVM classifier with radial-basis function (RBF) kernel, also shown in Figure 2.2. Unfortunately, such a classifier requires the ability to reliably perform complex computations, and thus its direct implementation is not feasible using TFT circuits.

In the following subsections, the proposed approach is presented for enabling TFT implementations of the computations required for strong classification. Two ideas are exploited. The first idea is *boosting*. This addresses the problem of inadequate fitting of weak classifiers to the data distribu-

tions, by employing an ensemble of weak-classifier decisions to form a strong classifier. Specifically, we employ the boosting algorithm known as Adaptive Boosting (AdaBoost) [70]. The second idea, is *Error-Adaptive Classifier Boosting (EACB)* [72]. This addresses the problem of high variability and non-ideality in the weak-classifier implementations, by training the weak classifiers in a manner that is aware and responsive to the decision errors that these cause.

2.1.2 Adaptive boosting (AdaBoost)

AdaBoost uses a fundamentally weak classifier building block, such as a simple linear classifier, which cannot fit to arbitrary training data.

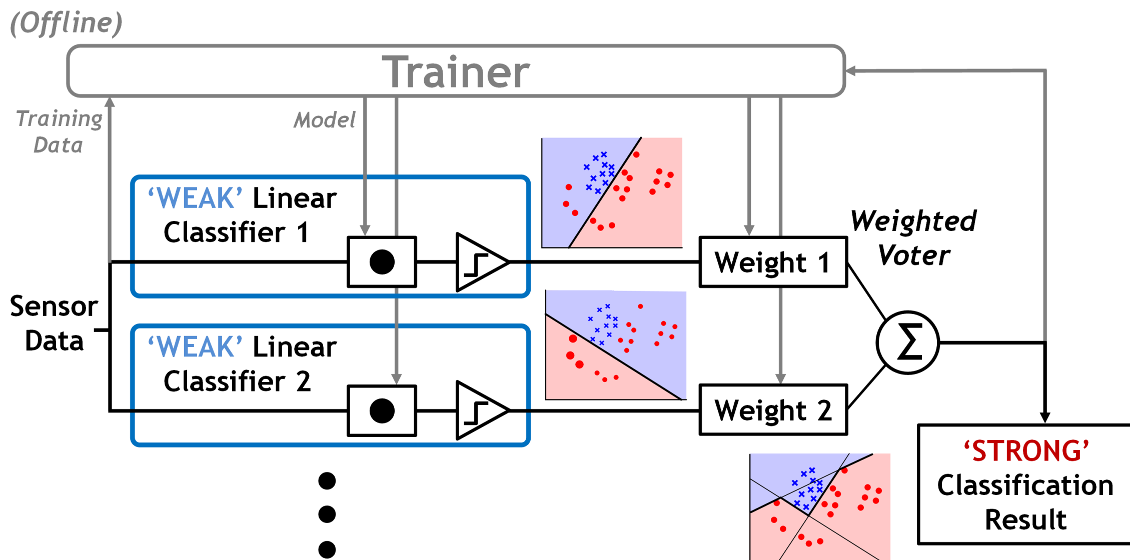


Figure 2.3: Architecture of the AdaBoost algorithm

The architecture of the algorithm is shown in Figure 2.3. AdaBoost trains the weak classifiers iteratively, by emphasizing the training data instances that are incorrectly fit by previous weak classifiers. As a result, subsequent weak classifiers adaptively improve overall fitting to the training set. The final classification decision is then made by performing weighted voting over the individual classifier outputs (weighted voting is simply implemented using a signed adder). The overall result is a strong classifier, yet constructed from a set of weak classifiers, which may be substantially simpler to implement.

An important attribute of AdaBoost noted by theoretical work is that fitting to arbitrary distributions can be achieved even with extremely weak classifiers, namely, which perform only

marginally better then 50/50 guessing [70]. This opens up the option to consider weak classifiers that have a topology that can viably be implemented using simple TFTs circuits.

However, TFT implementation of even simple weak-classifier circuits faces practical challenges. In addition to the fitting errors incurred with weak classifiers, implementation using TFTs will suffer from large static variations and high circuit fault rates, giving rise to another prominent source of errors. To overcome this, we employ EACB.

2.1.3 Error-Adaptive Classifier Boosting

Previous work has resulted in an algorithm know as error-adaptive classifier boosting (EACB), whereby weak-classifier implementations that substantially deviate from their nominal behavior can be employed within the framework of AdaBoost [71][72]. EACB exploits the fact that, in AdaBoost, weak classifiers are trained iteratively. This means that knowledge of the errors due to circuit non-idealities in a particular instance of weak-classifier hardware can be used to adaptively train subsequent iterations of weak classifiers. By exploiting data-driven training, complex and severe errors manifesting from the non-ideal implementation of previous weak-classifier iterations can thus be effectively overcome.

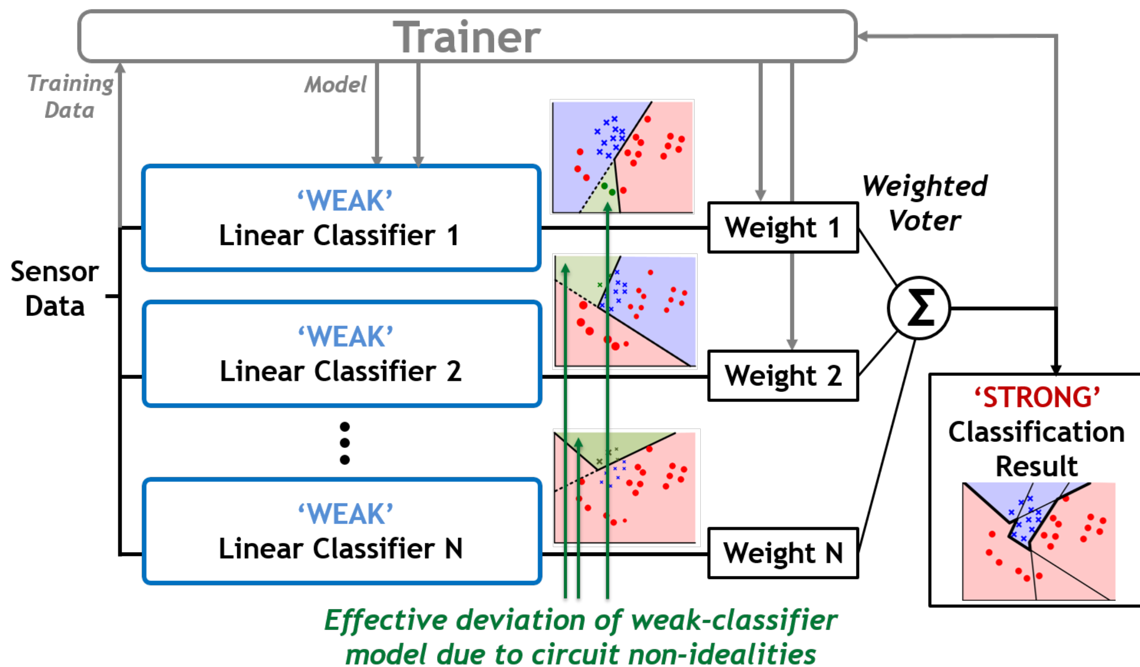


Figure 2.4: Error-Adaptive Classifier Boosting

This is shown schematically in Figure 2.4, where the nominal linear decision boundaries of the weak classifiers are perturbed due to circuit non-idealities. Subsequent weak-classifier models are adapted to address the resulting misclassified points.

Previous work on EACB has resulted in two key outcomes [71]. First, it has shown that the performance achieved through this approach corresponds to the fundamental level of information that is preserved in the presence of the non-idealities; namely, the performance achieved corresponds to the mutual information between the error-affected data and the true class membership, regardless of the magnitude or rate of the errors. Second, it has shown that EACB training can be achieved efficiently using low-complexity embedded hardware (i.e. microcontroller with low MIPS and modest embedded memory [71]). Further, utilizing the error-affected data from the system itself in order to perform training, various methods can also be employed for generating training labels within the system itself.

We show in this work that EACB applied to AdaBoost enables the implementation of a high-performance classifier (achieving performance near the level of an ideal SVM) using simple, variation-prone TFT circuits for the weak classifiers. This leaves only the weighted voter requiring error-free computation, as previous work has shown that final classification performance is sensitive to voter errors [71]. The next section describes the implementation and analysis (based on simulations) for an image-detection system, which thus employs TFT-based weak classifiers to substantially reduce the number of interfaces from the LAE domain, with the weighted voter (signed adder) presumed to be implemented in the CMOS domain.

Chapter 3

Thin-film classifier implementation

Having outlined the algorithmic approach used to create a strong classifier from simple, variation-prone TFT circuits, this section describes the implementation. Figure 3.1 illustrates the following components required in a complete system:

(1) a sensor array (image-sensing pixels);

(2) a serial interface for acquiring training data;

(3) a trainer for constructing the classification model from training data;

(4) a serial interface for loading the models from training into the weak classifiers;

(5) the weak classifiers themselves for applying the models in order to derive image-detection decisions on the sensor data in real time;

(6) a weighted voter for deriving the final image-detection decision.

Among the components, the sensor array [labelled (1)] and the classifier [labelled (5)] operate continuously, and are thus particularly critical. The trainer [labelled (3)] operates infrequently (one time in our demonstration) and is presumed to be implemented on a CMOS IC, using an algorithm similar to that previously demonstrated [72]. Both the training-set acquisition interface and the model-loading interface [labelled (2) and (4)] require thin-film scanning circuits to control switches for multiplexing data onto a serial interface. The scanning circuits can be simple digital

circuits and can operate at low speed, since training occurs infrequently. Such circuits are routinely incorporated for row-scanning in active-matrix systems. As an example, scanning circuits previously described can be used for this purpose. For the current system demonstration, these circuits are not included. Finally, having reduced the interfaces from the sensor-array signals to a small number of weak-classifier decisions, the weighted voter [labelled (6)] is presumed to be implemented on a CMOS IC, using a signed adder (since its errors impact overall performance [72]). Thus, the focus of the system demonstration is the sensor array and ensemble of weak classifiers, which operate continuously.

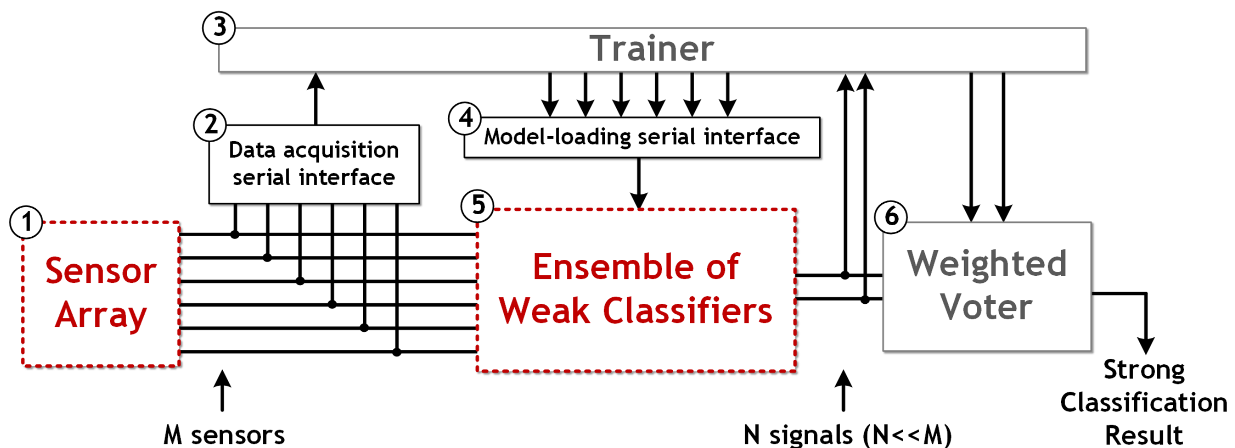


Figure 3.1: Components required for the trainer and classifier

3.1 Classifier implementation

The weak classifiers are implemented using TFT circuits. In particular, each weak classifier implements an approximation to a linear classifier, represented by the function previously shown in Equation 2.1. The dot-product operation required is implemented using a TFT circuit, which also is capable of storing the weights $\vec{c}$ obtained from model training.

The weak classifiers thus reduce M sensor signals to N dot-product outputs. The reduced signals are then presumed to feed a CMOS IC, which implements thresholding and weighted voting. Next, we will look closer at the implementation of the model-programmable weak classifiers.

3.1.1 Weak 'linear' classifier sub-unit

The dot product within the linear classifiers is implemented as shown in Figure 3.2. Approximation to multiplication between each sensor and each weight from model training is achieved through a series combination of TFTs.

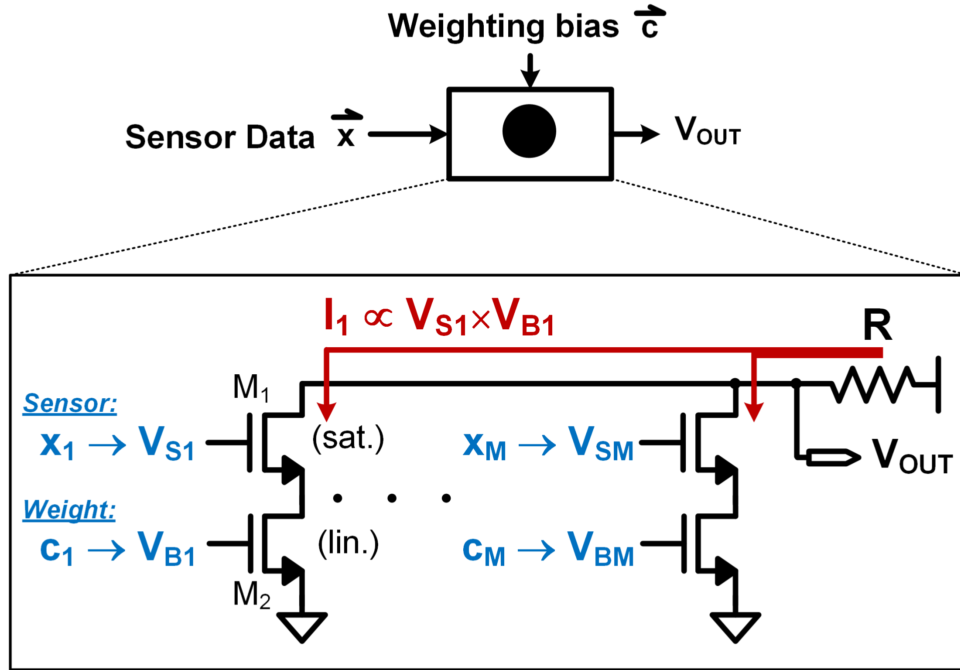


Figure 3.2: Thin-film implementation of the linear classifier dot-product approximation

The thin-film transistors are biased with M1 in saturation (having transconductance g_{m1}) and M2 in the linear region (giving effective resistance R_{B2}). For M2 we thus have:

$$\frac{1}{R_{B2}} \approx \frac{dI_1}{dV_{ds,M2}} = k\frac{W}{L}\left[(V_{B1} - V_T) - V_{ds,M2}\right] \tag{3.1}$$

and for M1 we have:

$$I_1 = k\frac{W}{2L}(V_{S1} - I_1R_{B2} - V_T)^2 = \frac{g_{m1}}{2}(V_{S1} - I_1R_{B2} - V_T) \tag{3.2}$$

Rearranging this results in:

$$I_1 = \frac{g_{m1}(V_{S1} - V_T)}{2 + g_{m1}R_{B2}} \tag{3.3}$$

If $g_{m1}R_{B2} \gg 2$ is sufficiently satisfied, and M2 is in deep triode such that $(V_{B1} - V_T) \gg V_{ds,M2}$ is sufficiently satisfied, the output current of the series connected TFTs implements an approximation to multiplication:

$$I_1 \approx \frac{(V_{S1} - V_T)}{R_{B2}} \approx k\frac{W}{L}(V_{B1} - V_T)(V_{S1} - V_T) \tag{3.4}$$

Following this, the summation required within the dot-product operation is then realized by combining the output currents from these branches through the resistor R.

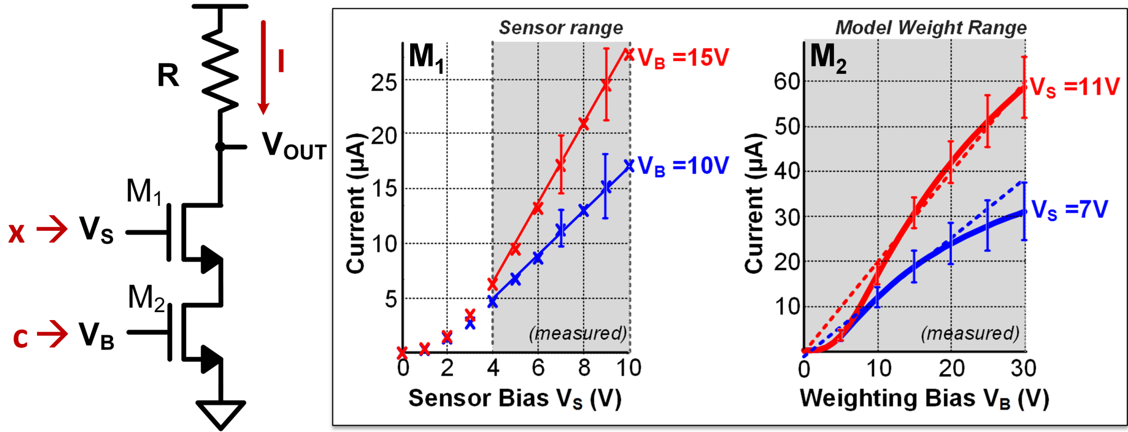


Figure 3.3: Non-ideal deviation and variation in the dot-product approximation circuit

In practice, though, this circuit only approximates multiplication. This is because of nonlinearity (arising due to the use of the g_{m1} term), approximations (arising as described above), and variations (arising in all the TFTs). From measurements taken at representative bias voltages, the actual transfer functions achieved for each input (gate of M1 and gate of M2) to the output current are illustrated in Figure 3.3. We see that the transfer function from M1, over the designated voltage range (output of the sensor), is fairly linear, and thus implements a good approximation to multiplication. On the other hand, the transfer function from M2 is substantially nonlinear, and thus implements a somewhat worse approximation to multiplication (the ideal multiplication transfer function is overlayed in dotted curves). This motivates the decision to feed the sensor signal to M1 and apply the model weight to M2. The reason for this is that the model weight does not change continuously; rather, once derived from training, the proper biasing level (V_B) can be determined by computationally applying the inverse of the nominal transfer function from M2, thus mitigating the impact of its nonlinearity. On the other hand, the sensor signal changes

continuously, and is thus preferable to apply directly to the circuit without any explicit mechanism (e.g. additional circuitry) to mitigate the impact of nonlinearity.

In addition to non-ideal deviations in the nominal transfer functions, the TFT circuits also suffer from substantial variation. Shown as error bars in Figure 3.3, the resulting variations in the transfer functions (measured from 10 circuits) are severe. Specifically, the device-level variations are measured as reported in Figure 3.4. To overcome this, the EACB algorithm is leveraged, and analysis from simulation is presented below.

Measured levels of variation					
Output Resistance	$\overline{r_0}$ = 10MΩ σ = 0.1MΩ	Threshold Voltage	$\overline{V_T}$ = 2V σ = 0.3V	Mobility	$\overline{\mu}$ = 0.7 cm²/Vs σ = 0.02 cm²/Vs

Figure 3.4: Measured sources of thin-film variation

3.1.2 Classifier model programmability

As mentioned, in the multiplication circuit, the gate of M2 is used to apply the trainer-derived model weight. This implies that the circuit must support storage of a programmable analog voltage at the gate of M2. To achieve this, non-volatile charge trapping in the gate dielectric of a TFT is used. Application of a large electric field on the TFT gate effectively results in a large, controllable threshold voltage shift.

This is shown in Figure 3.5 which plots the measured drain current vs. gate voltage for a standard TFT, and for a TFT programmed to have a threshold voltage shift of 30V (with error bars showing results over 6 devices). For large model weights, a small positive threshold-voltage shift is applied, while for small model weights, a large positive threshold voltage shift is applied. Though training typically only occurs once in the system, this form of programming is reversible through the application of a large negative voltage on the TFT gate.

One complication that arises in practice is that the model weights derived from training can be negative. To address this, pseudo-differential multiplication branches are used to create the complete multiplication circuit, as shown in Figure 3.6. For example, to apply a negative weight, the left branch is programmed with a large threshold voltage, essentially turning it off, whilst the right branch is programmed with a low threshold voltage, appropriately set.

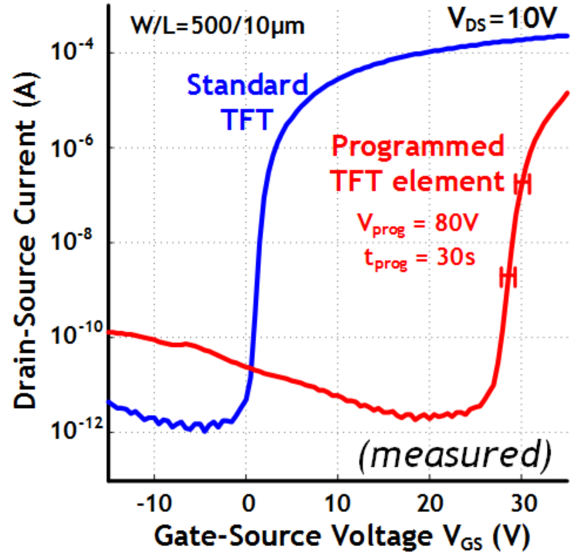


Figure 3.5: TFT I-V curves showing threshold voltage shift for model-programming of TFT classifier

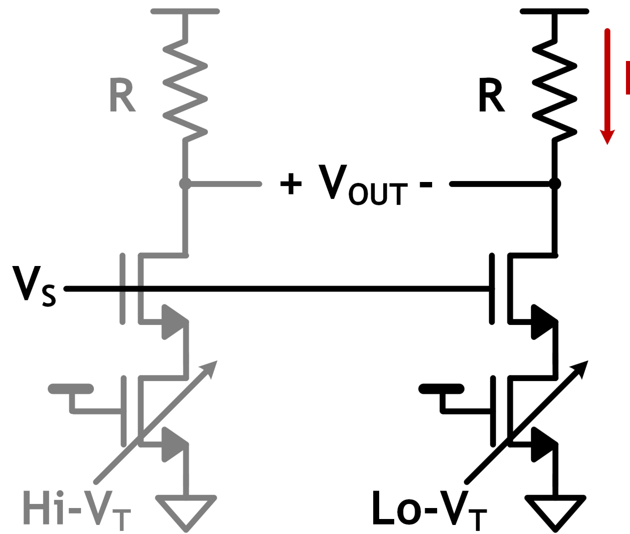


Figure 3.6: Complete pseudo-differential multiplication circuit for the application of a negative model weight

3.1.3 Overall implementation

Figure 3.7 shows the overall implementation with the weak classifiers comprising the summed outputs from the pseudo-differential multiplication units.

Thirty-six sensor signals, corresponding to the outputs from photoconductor pixels for image sensing, feed the ensemble of weak classifiers, all appropriately V_T-shifted based on the model weights derived from training. The outputs, thus corresponding to the dot-product results, are

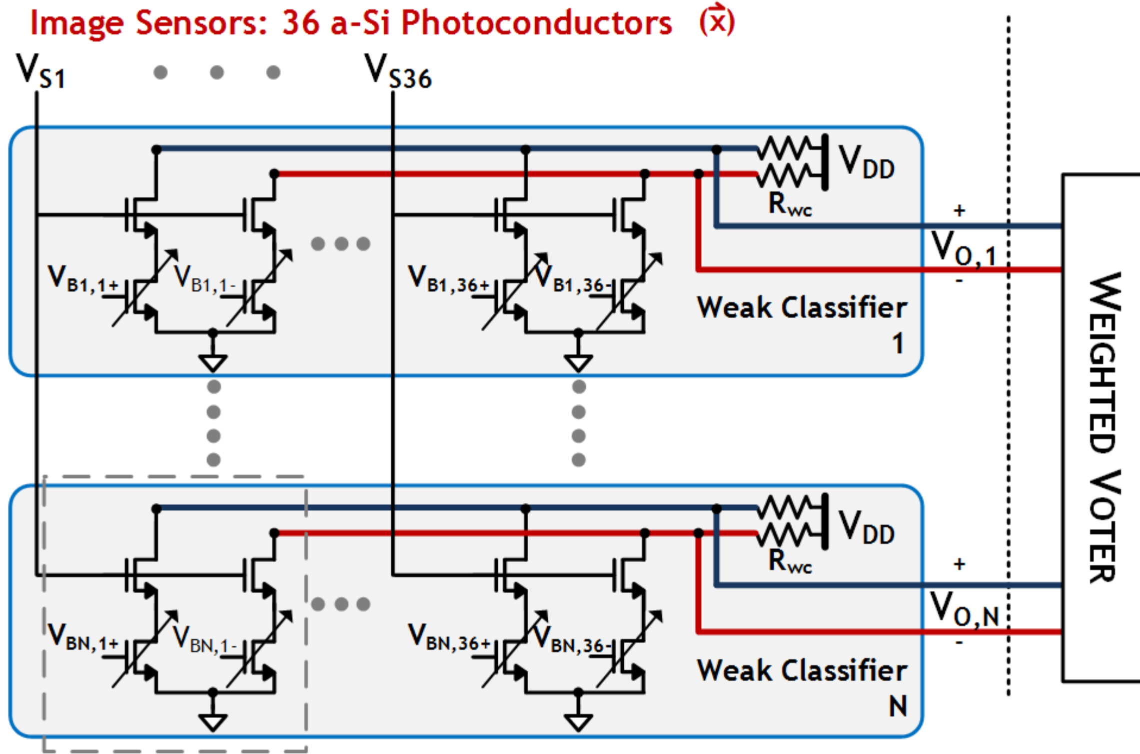


Figure 3.7: Complete thin-film sensing and classification system

subsequently thresholded to derive the weak-classifier decisions. The ultimate goal of this implementation is to reduce the large number of sensor signals to just a small number interfaces for the weak classifier decisions.

To analyze the system, simulations are performed by creating statistical models of the TFT-based weak classifiers. First, we extract a Level 61 SPICE model of the TFTs from device measurements (as earlier in this thesis). Transistor-level simulations are then performed in Spectre to characterize the transfer functions of the multiplication unit, which is used in the weak classifiers. The transfer functions are represented numerically and augmented with measured device-level variation data to create a statistical model of the units usable in MATLAB. Monte Carlo simulations are then performed in MATLAB of the entire system, consisting of multiple weak classifiers composed of variation-affected multiplier units. Using the shape dataset, the weak classifiers are trained, employing both the AdaBoost and EACB algorithms. Figure 3.8 shows the simulation results for classifiers trained to four shapes. The metrics used for characterizing classification performance are true-positive (tp) rate and true-negative (tn) rate. As an example, considering the classification of rings vs all the other shapes in the dataset,

$$\text{True positive rate} = \frac{\text{number of correctly classified } \textit{ring instances} \text{ in the dataset datapoints}}{\text{total number of } \textit{ring instances} \text{ in the dataset}} \tag{3.5}$$

$$\text{True negative rate} = \frac{\text{number of correctly classified } \textit{other shapes}}{\text{total number of instances of } \textit{other shapes} \text{ in the dataset}}. \tag{3.6}$$

As can be seen in Figure 3.8, while AdaBoost alone is inadequate, EACB enables high classification to be achieved.

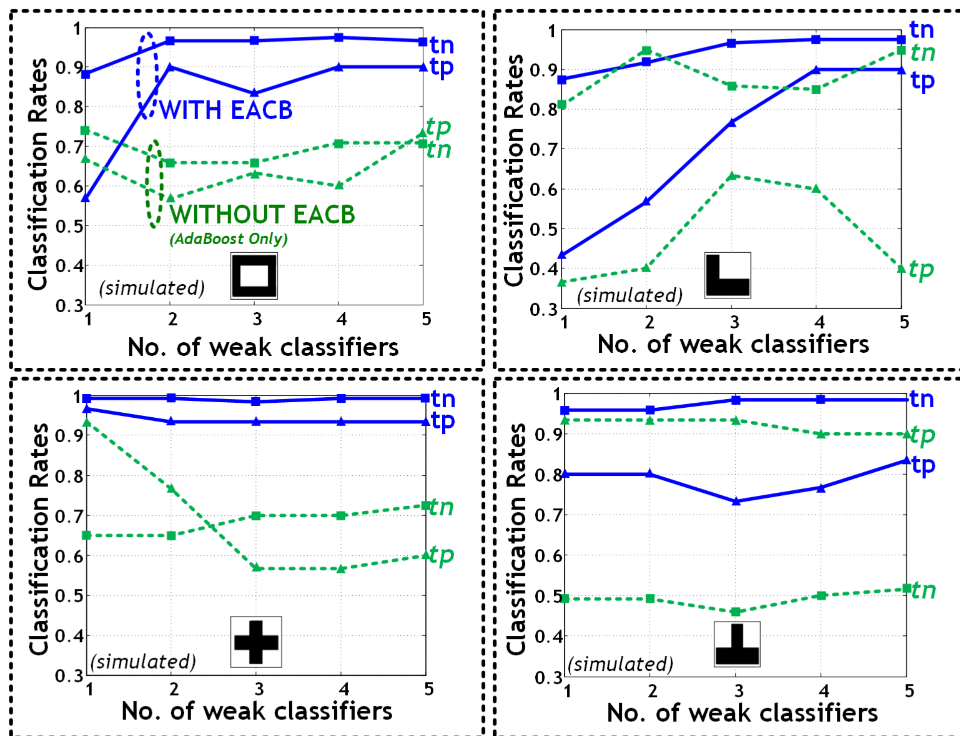


Figure 3.8: Simulated classification rates with and without the implementation of Error-Adaptive Classifier Boosting (EACB) (shown for one vs. all classification of 4 shapes).

Chapter 4

System demonstration

In this section the thin-film system prototype is presented. As shown in Figure 4.1 it consists of two glass samples onto which both thin-film amorphous-silicon sensors and transistors are fabricated in-house using a maximum processing temperature of 180 °C.

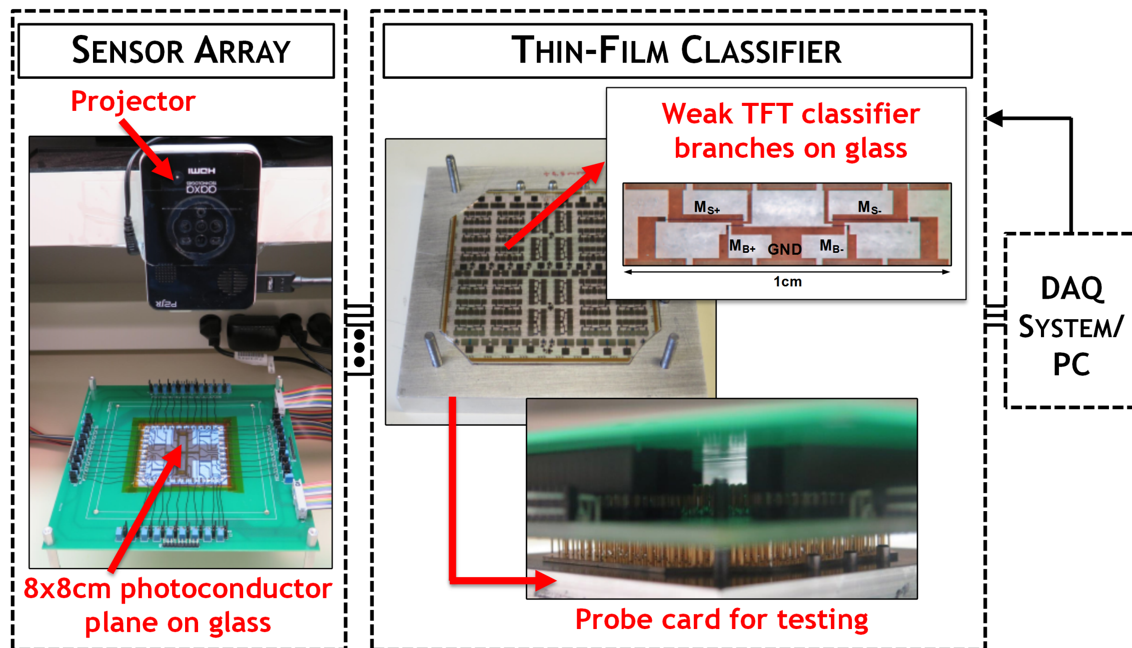


Figure 4.1: Thin-film prototype

The first sample is an 8x8cm array of 36 image sensors onto which images are projected using a micro-projector. The outputs from the sensors are passed to the second sample, consisting of the TFT-based weak classifiers. To aid testability, interfacing between the two samples is achieved

using a probe card, which permits the acquisition of both weak classifier and sensor outputs, for processing and analysis by a PC.

4.1 Image sensors

The image-sensing array is constructed using sensor pixels based on thin-film photoconductors. The photoconductors are pictured in Figure 4.2.

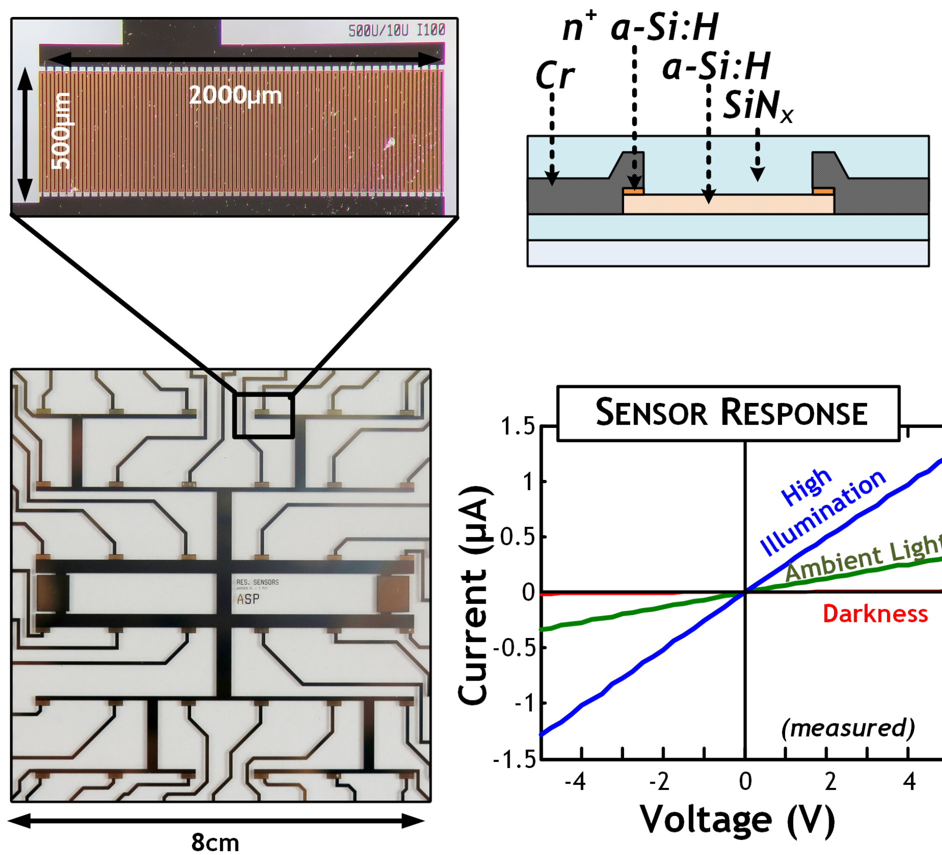


Figure 4.2: Thin-film photoconductors

These are formed by interdigitated undoped amorphous silicon with a thickness of 150nm. As shown, these exhibit strong change in I-V response under different illumination conditions. To implement the complete sensor pixel, this photoconductor is configured as one leg of a voltage divider, where the other leg is a fixed thin-film resistor (750kΩ).

The output voltage from 36 sensors over time is shown in Figure 4.3 under two illumination conditions. Though a strong photoresponse can be observed, a substantial amount of variation

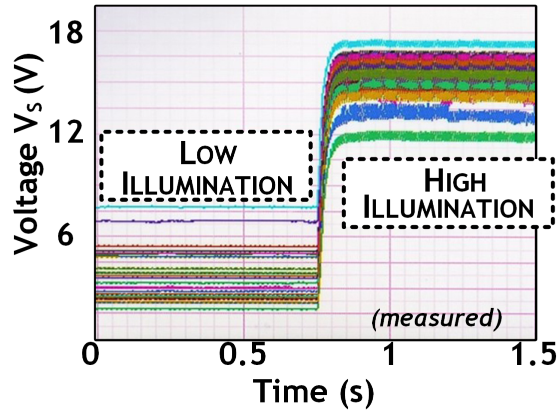


Figure 4.3: Variability in thin-film photoconductors

across the sensors can also be seen. The use of a data-driven machine-learning algorithm allows for modeling of the acquired data even in the presence of such large variations across the sensors.

4.2 Thin-Film Transistors

The TFTs used in the weak classifiers are fabricated using our standard amorphous silicon process technology, as presented earlier in this thesis.

As described previously, programmability of the weak classifier is achieved via gate-dielectric charge trapping in TFTs with the same structure, simply by applying a large programming voltage on the gate. Typical programming (erase) voltages are +80V (-80V), with a drain and source voltage of 0V in both cases. A typical threshold-voltage shift vs. programming-time characteristic is shown in Figure 4.4 as described earlier, this threshold voltage shift can be mapped appropriately to a model weight obtained from training by applying the inverse transfer function of the multiplication circuit). It is also worth noting that the variation in programmed and erase states is small ($\sigma(V_T) \leq 1V$), so the desired shifts can be achieved repeatably. This level of variation in V_T is easily tolerated as a result of using the EACB algorithm.

A potential future focus for the implementation is the programming voltages and programming times required, both of which are somewhat large. Substantial room exists to optimize these. For instance, previous work has demonstrated these can be reduced by using a slightly modified TFT structure, consisting of the addition of an explicit amorphous silicon floating gate [17]. Meanwhile, Figure 4.5 shows the retention time characteristic of the programmable element; some optimization

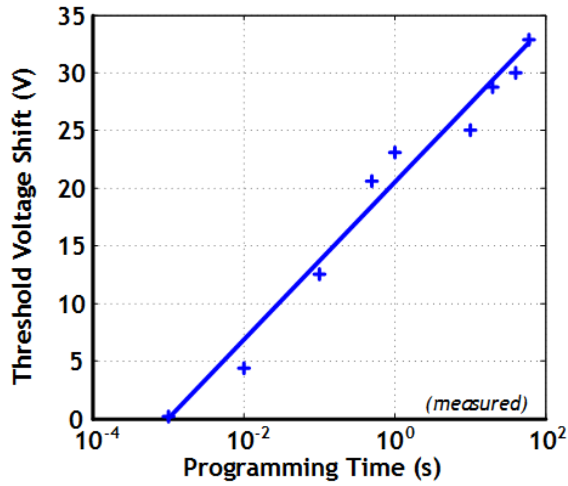


Figure 4.4: Effect of programming time on threshold-voltage shift of amorphous silicon thin-film transistor at a gate voltage of +80V vs. source and drain

is clearly required to avoid the need for repeated programming, with a trade-off likely existing between programming voltage, programming time and retention time.

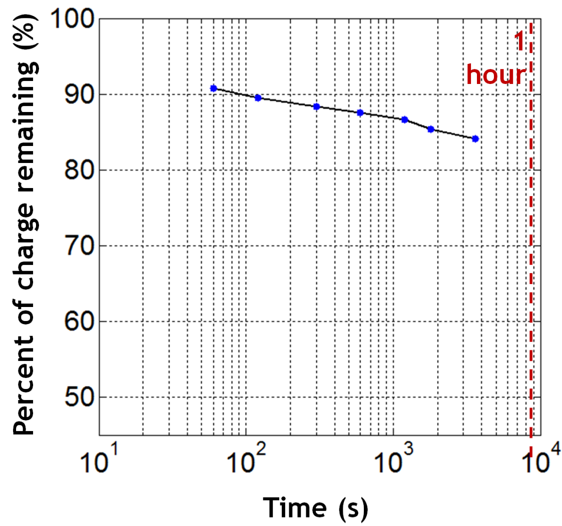


Figure 4.5: Retention time characteristic of the programmable TFT

4.3 Image classification system

Some of the images from the dataset used for testing the thin-film shape classifier are shown in Figure 4.6. In total, 150 data instances are used, comprising 5 shapes with 10 background intensities, under three illumination conditions.

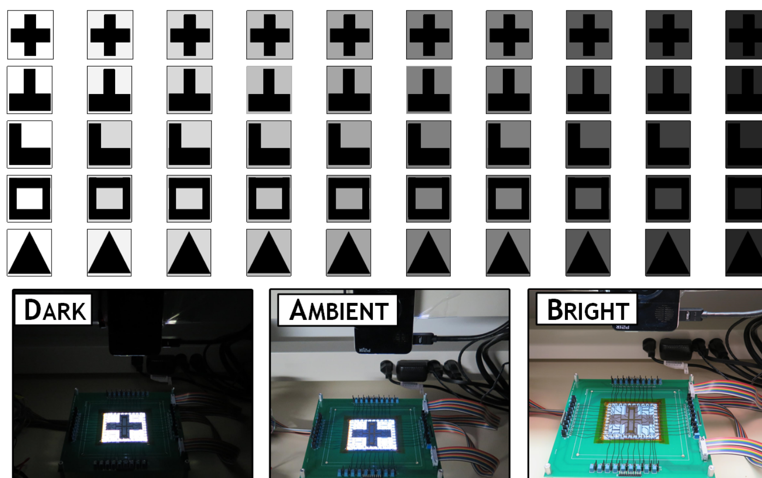


Figure 4.6: Subset of dataset used for classification

Figure 4.7 shows plots of true positive and true negative rates for one-vs.-all classification of each shape with respect to the number of weak classifiers used. As can be seen for all shapes, boosted performance is observed, as TFT weak classifier iterations are added. Indeed, high overall classification performance is achieved with very few weak classifiers in all cases.

For reference, horizontal lines show the performance achieved when performing classification using an ideal MATLAB-implemented SVM classifier, a widely used strong classifier. Only between 2 and 5 weak classifiers are required to achieve performance at the level near that of the SVM, implying a substantial reduction in the number of interfaces, compared to the 36 raw sensor inputs.

Figure 4.8 highlights the importance of using the EACB algorithm as opposed to simply using the AdaBoost algorithm, illustrated for the case of classification of ring vs. other shapes. Without EACB, even with 7 weak-classifier iterations, convergence is not achieved and low classification performance is observed, whereas EACB leads to substantially boosted performance. In addition, Figure 4.9 also illustrates the robustness to variation thanks to EACB, as a result of programming variability to the level of that observed with the programmable TFTs used.

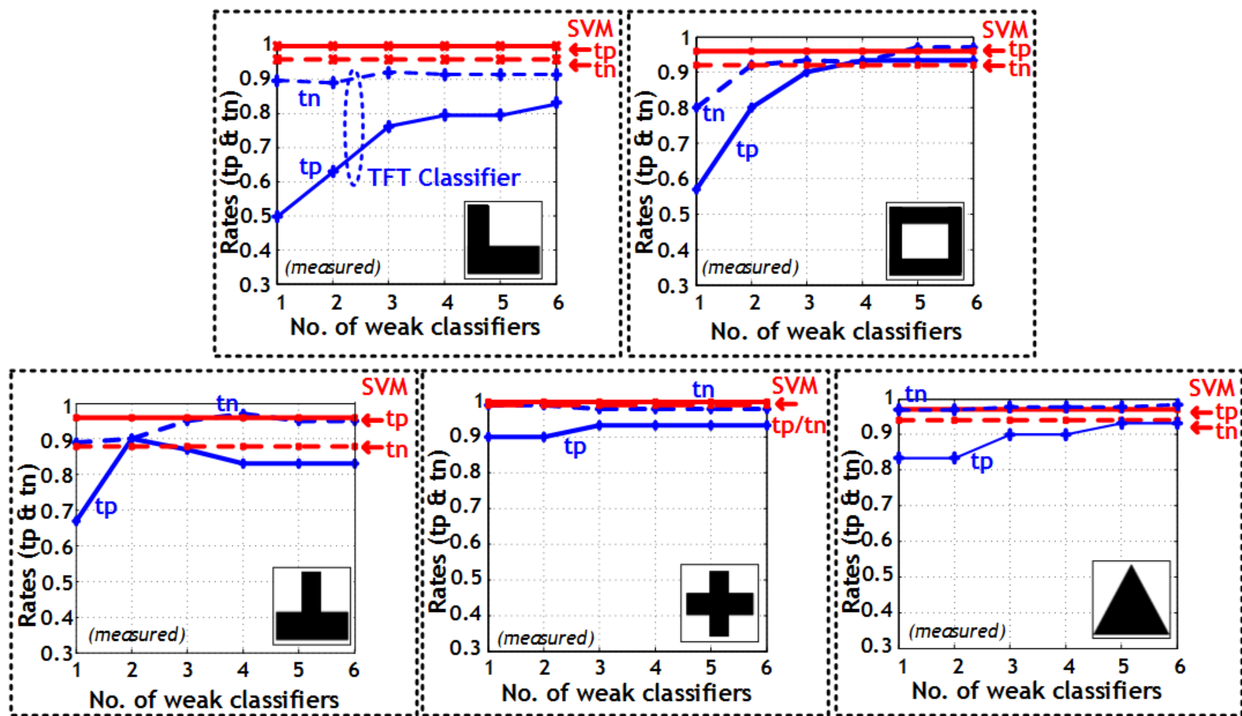


Figure 4.7: Classification results

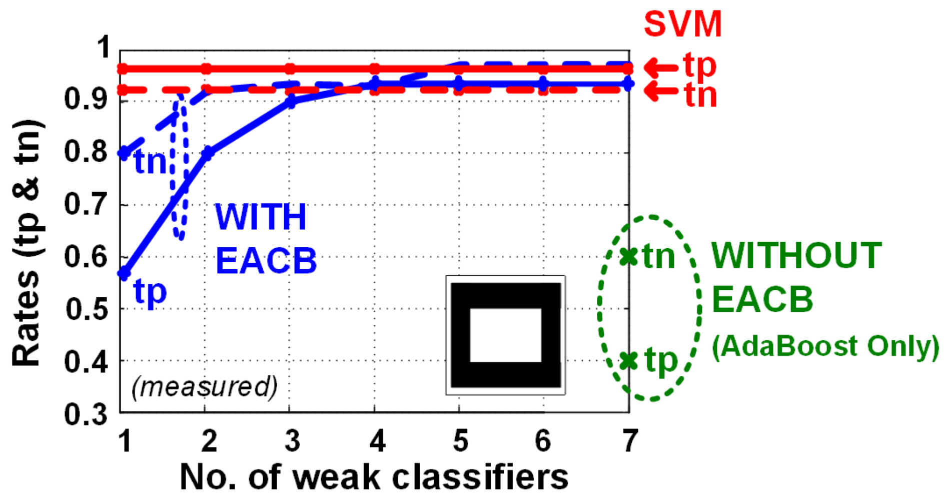


Figure 4.8: Effect of error-adaptive classifier boosting

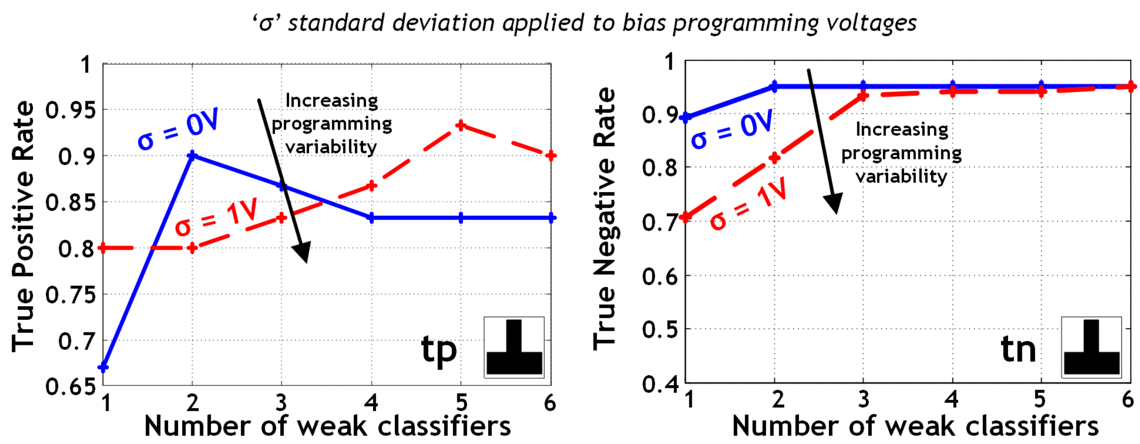


Figure 4.9: System robustness to programming deviations

Chapter 5

Conclusions

In this section, we have discussed the implementation of a thin-film sensing and classification system based on large-area electronics (LAE). While LAE enables the formation of diverse and expansive arrays of sensors, the resulting thin-film transistors (TFTs) have low performance and high variability, precluding the implementation of complex functions for processing sensor signals. The presented system uses a machine-learning algorithm, known as Error-Adaptive Classifier Boosting (EACB), which enables the creation of a strong classifier using an ensemble of simple classifier circuits having low electrical performance and high variability. Implemented using TFTs, the weak-classifier circuits reduce the sensor outputs to a small number of signals, which can be provided to a CMOS IC to make the final classification decisions.

High classification performance is demonstrated for a shape classification system, at the level of a strong complex classifier (SVM), even in the presence of substantial sensor and TFT variability. Trained to detect five different shapes, a reduction in signals of 3.5-9$\times$ is achieved with respect the raw 36 sensor outputs.

Circuit design, analysis and measurements in the systems presented were done by this author in close collaboration with Tiffany Moy. Light sensors were developed by this author. Circuit fabrication was done by this author and Tiffany Moy. Boosting code and simulations were developed by Zhuo Wang and software for interfacing to and acquiring from the thin-film electronics developed by this author.

Part VI

Thesis conclusions

In this thesis, we have provided a foundation for the development and design of hybrid systems that leverage the strengths of large-area electronics and crystalline-silicon CMOS ICs. We find that large-area electronics excels in sensing and energy-harvesting capabilities, though a key challenge is the realization of systems that combine this richness with the computational strength of CMOS ICs. The interface between these two technologies is closely explored through the use of novel thin-film circuit topologies for non-contact transfer of power and signals over a minimal number of interfaces. In most of these, substantial thin-film device optimization is required in order to enable operation or increase performance. For this we explore and apply well known device approaches such as self-alignment and channel length reduction to in-circuit devices. We investigate a number of systems as platform demonstrators (powering systems, communication systems, sensing systems). We finish the thesis by introducing the idea that even though thin-film technologies are low performance and generally variable, algorithmic techniques allow us, for the first time, to create thin-film systems that perform higher-level functions on large-sensing arrays. Much of this work will likely also be applicable to a range of post-CMOS technologies. There is a lot of potential for these systems, and it is the belief of this author that very interesting intuition will be garnered through upscaling, enabling a range of new applications.

Appendix A

Thin-Film Fabrication Processes

This chapter summarizes the key thin-film fabrication processes used in construction of our hybrid systems.

A.1 Standard blanket-passivated, back-channel cut TFT Recipe

Prepare substrate

- Clean glass substrate as per procedure listed later in this chapter
- Use a glass scribe (or the dicing saw) to remove approximately 1cm corners of the glass substrate. This is to allow the glass to fit on top of a 4in wafer (this can be done before or after cleaning).
- Deposit 150nm SiN_x passivation layer (SiH4/NH3/H2=6/60/200sccm, 35mins, 500mT, 5W, 200/200/200C)

Gate metal deposition and patterning

- Sputter using Angstrom Sputterer either Cr (50nm, recipe SturmDC2Cr500) or Cr/Al/Cr (30/50/20nm, recipes WagnerDC2Cr300/SturmRFAl500/WagnerDC2Cr200)
- Pre-bake on hot plate at 95C, 3mins

- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Soft-bake on hot plate at 95C, 1min
- LEVEL 1 mask (Gate Metal): UV Intensity = 2.0 mW/cm^2, 40s
- Develop: AZ300MIF, 60s
- Hard-bake on hot plate at 95C, 3min
- Wet etch Cr with Cr-7 etchant, 45s (if have Al, etch using Al-11 or Al 80:3:15 NP for 4mins)
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min

---

Deposit TFT stack

- Heat in Load Lock for 10 mins at 100C
- Ar Plasma on sample in N-chamber (Ar=50sccm, 4mins, 500mT, 12W, 200/200/200C)
- Deposit 275(-300)nm SiN_x gate dielectric (SiH4/NH3/H2=6/60/200sccm, 60(-70)mins, 500mT, 5W, 200/200/200C)
- Deposit 150nm a-Si (SiH4/H2=16/200sccm, 60mins, 500mT, 4W, 200/200/200C)
- Deposit 30nm n^+ a-Si (SiH4/PH3=44/10sccm, 4mins, 500mT, 4W, 200/200/200C). Note-PH3 is diluted 1% in H2.

Etch a-Si and SiN_x

- Pre-bake on hot plate at 95C, 3mins
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Soft-bake on hot plate at 95C, 1min

- LEVEL 2 mask (Active Region): UV Intensity = 2.0 mW/cm^2, 40s
- Develop: AZ300MIF, 60s
- Hard-bake on hot plate at 95C, 3min
- Tape glass sample onto 4in wafer
- Etch a-Si using Samco 800, recipe 66, 42 cycles
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min
- Pre-bake on hot plate at 95C, 3mins
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Soft-bake on hot plate at 95C, 1min
- LEVEL 3 mask (Via): UV Intensity = 2.0 mW/cm^2, 40s
- Develop: AZ300MIF, 60s
- Hard-bake on hot plate at 95C, 3min
- Tape glass sample onto 6in wafer
- Etch SiN_x using PT720, CF_4/O_2=70/10sccm, 100mT, 100W, 3:40mins
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min

---

Source/drain metal deposition and patterning

- 10s dip in 100:1 BOE
- Sputter using Angstrom Sputterer either Cr (100nm, recipe SturmDC2Cr1kA) or Cr/Al/Cr (50/200/50nm)
- Pre-bake on hot plate at 95C, 3mins

- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Soft-bake on hot plate at 95C, 1min
- LEVEL 4 mask (S/D): UV Intensity = 2.0 mW/cm^2, 40s
- Develop: AZ300MIF, 60s
- Hard-bake on hot plate at 95C, 3min
- Wet etch Cr with Cr-7 etchant, 45s (if have Al, etch using Al-11 or Al 80:3:15 NP for 10mins)
- Tape glass sample onto 4in wafer
- Etch a-Si using Samco 800, recipe 66, 12 cycles
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min

---

Deposit and pattern passivation layer

- Ar Plasma on sample in N-chamber (Ar=50sccm, 4mins, 500mT, 12W, 200/200/200C)
- Deposit 250nm SiN$_x$ gate dielectric (SiH4/NH3/H2=6/60/200sccm, 50mins, 500mT, 5W, 200/200/200C)
- Pre-bake on hot plate at 95C, 3mins
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Soft-bake on hot plate at 95C, 1min
- LEVEL 5 mask (Passivation): UV Intensity = 2.0 mW/cm^2, 40s
- Develop: AZ300MIF, 60s
- Hard-bake on hot plate at 95C, 3min

- Tape glass sample onto 6in wafer
- Etch SiN_x using PT720, CF_4/O_2=70/10sccm, 100mT, 100W, 3:40mins
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min

---

Deposit contact layer for soldering (optional)

- Sputter using Angstrom Sputterer Cr/Au (50/300nm, recipe SturmDC2Cr500, SturmDC1Au3kA)
- *Image Reversal:*
- Pre-bake on hot plate at 95C, 3mins
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Soft-bake on hot plate at 95C, **45s**
- LEVEL 5 mask (Via): UV Intensity = 2.0 mW/cm^2, 30s
- Bake on hot plate at 110, **75s**
- Flood UV Exposure, UV Intensity = 2.0 mW/cm^2, 60s
- Develop: AZ300MIF, 60s
- Hard-bake on hot plate at 95C, 3min
- Wet etch Au with GE-6 etchant, 60s then Cr-7 etchant, 45s
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min
- Note: this mask layer can also be done by liftoff without image reversal if necessary

---

Anneal sample

- Anneal sample in PECVD for 1h at 180C (or at the maximum temperature possible in the vacuum oven for 1h)

For processing on plastic, all steps are identical except that during lithography, the plastic sample is mounted on a glass slide using a drop of water (place slide on spin chuck, place small drop of water in center, place plastic sample on slide, blow dry excess water out through edges, spin using recipe 1). When sample is in PECVD, place a glass slide between the graphite plate and the plastic sample.

A.2 Self-Aligned TFT recipes

Prepare substrate

- See Standard TFT Recipe

Gate metal deposition and patterning

- Sputter using Angstrom Sputterer Cr (50nm, recipe SturmDC2Cr500)
- Pre-bake on hot plate at 95C, 3mins
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Soft-bake on hot plate at 95C, 1min
- Gate Metal Mask: UV Intensity = 2.0 mW/cm^2, 40s
- Develop: AZ300MIF, 60s
- Hard-bake on hot plate at 95C, 3min
- Wet etch Cr with Cr-7 etchant, 45s
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min

---

Deposit TFT stack

- Heat in LL for 10 mins at 100C
- Ar Plasma on sample in N-chamber (Ar=50sccm, 4mins, 500mT, 12W, 200/200/200C)
- Deposit 275(-300)nm SiN_x gate dielectric (SiH4/NH3/H2=6/60/200sccm, 60(-70)mins, 500mT, 5W, 200/200/200C)
- Deposit 30nm a-Si (SiH4=50sccm, 2:40mins, 500mT, 4W, 200/200/200C)
- Deposit 100(-150)nm SiN_x gate dielectric (SiH4/NH3=6/150sccm, 30mins, 500mT, 5W, 200/200/200C)

Pattern a-Si on top of gate and self-align top-passivation

- Pre-bake on hot plate at 95C, 3mins
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Soft-bake on hot plate at 95C, 1min
- Active Region Mask: UV Intensity = 2.0 mW/cm^2, 40s
- Flip sample over and backside UV Angled Exposure Intensity = 3.5 mW/cm^2 (CI2), 600s (with TFT widths parallel to edge that has been lifted up to be angled), then rotate sample by 180 degrees and repeat for 600s.
- Develop: AZ300MIF, 30s
- Hard-bake on hot plate at 95C, 3min

Etch top-passivation

- Dip for 6s in 10:1 BOE. Rinse thoroughly.

- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min

---

Deposit n+ doped layer

- Deposit 30nm n^+ a-Si (SiH4/PH3=44/10sccm, 4mins, 500mT, 4W, 200/200/200C). Note-PH3 is diluted 1% in H2.

Create Source/Drain Overlap and deposit source/drain

- Use method described above for creating top passivation self-alignment (in preparation for a lift-off process).
- Sputter using Angstrom Sputterer Cr (100nm, recipe SturmDC2Cr1kA)
- Lift off using sonication in acetone. If needed use a cue-tip to encourage the liftoff process. Rinse with isopropanol

---

Source/drain metal deposition and patterning

- Pre-bake on hot plate at 95C, 3mins
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Soft-bake on hot plate at 95C, 1min
- S/D mask : UV Intensity = 2.0 mW/cm^2, 40s
- Develop: AZ300MIF, 60s
- Hard-bake on hot plate at 95C, 3min
- Wet etch Cr with Cr-7 etchant, 45s
- Tape glass sample onto 4in wafer

Dry etch n+ amorphous silicon

- Tape glass sample onto 4in wafer
- Etch n+ a-Si using Samco 800, recipe 66, 6 cycles
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min

---

Pattern a-Si island

- Pre-bake on hot plate at 95C, 3mins
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Soft-bake on hot plate at 95C, 1min
- Active Region Mask: UV Intensity = 2.0 mW/cm^2, 40s
- Develop: AZ300MIF, 60s
- Hard-bake on hot plate at 95C, 3min
- Tape glass sample onto 4in wafer
- Etch a-Si using Samco 800, recipe 66, 3 cycles
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min

---

Etch gate via holes in SiN$_x$

- Pre-bake on hot plate at 95C, 3mins
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s

- Soft-bake on hot plate at 95C, 1min
- Gate Via Mask: UV Intensity = 2.0 mW/cm^2, 40s
- Tape glass sample onto 6in wafer
- Etch SiN_x using PT720, CF_4/O_2=70/10sccm, 100mT, 100W, 3:40mins
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min

---

Anneal sample

- Anneal sample in PECVD for 1h at 180C (or at the maximum temperature possible in the vacuum oven for 1h)

For processing on plastic, all steps are identical except that during lithography, the plastic sample is mounted on a glass slide using a drop of water (place slide on spin chuck, place small drop of water in center, place plastic sample on slide, blow dry excess water out through edges, spin using recipe 1). When sample is in PECVD, place a glass slide between the graphite plate and the plastic sample.

A.3 Stepper TFT recipes

Processing for Stepper TFTs is almost the same as for standard TFTs except on 4 inch wafers. The difference is in the preparation of the photoresist and the development of the sample after exposure in the stepper.

Application of photoresist

- Set the temperature of the YES Prime oven to 148C and wait for the temperature to stabilize at that setpoint. Make sure the valve is correctly set to HMDS as opposed to ammonia.
- Place wafer into YES Prime oven and run recipe 1 to deposit a uniform layer of HMDS. After process is complete, return the YES oven temperature to 90C.
- Place wafer on a large circular flat spin-chuck (with no rubber o-ring).

- Apply AZ701 Photoresist and spin using Recipe 1 (the obtained thickness is between 0.3-1.1μm)
- Use recipe CLEANFRONTBACK on the Brewer Science Spinprocessor to remove edge-bead on the wafer and clean the back side.
- Soft bake the wafer at 90C for 60s.

Exposure parameters

- Exposure dose: 1700J/m^2
- If the wafer has resist, set the 'Focus Mark Wafer Surface Condition' to 3, else set it to 0.
- For auto-alignment of Level 2 and above, in the Auto-Alignment menu, the following are set: (1) AGA sub-menu: 1 HeNe normal, mode 4/4, mark B=-1, Y=-0.8 (2) TVPA sub-menu: Mark Type PEN (pattern entry), Illumination 13 (the max intensity of the halogen lamp is 17), Max to 90%.

Development of exposed photoresist

- Wipe cold hot plate with EBRPG to remove photoresist residue.
- Post-exposure bake of wafer at 110C for 60s.
- Place 1 wafer on the hotplate at a time.
- Develop using AZ300MIF for 60s (no shaking).
- Rinse the front and back of the wafer carefully.
- NO additional bake.

Loading wafers into the stepper

- Blow dry the wafer carrier including the bottom and hold it from the top.
- Blow dry the wafer and put it in slot 1, with the resist facing up towards the inside of the wafer carrier.

- Put the large wafer flat facing towards the outside of the wafer carrier (the side with no wall).
- Blow dry the bottom of the holder again.
- Load the wafer carrier on position C1 - carrier is loaded properly when the green light goes on.
- Set the desired illumination intensity and press 'Link' (this changes the parameters only in a temporary way, whereas 'Job Save' saves the settings permanently).
- Press 'Start'
- When the 'Lot End' light flashes and the buzzer sounds, the process is done!

Manual pattern recognition If alignment mark recognition fails during auto-alignment, the pattern can be learned using the following procedure:

- Once an error is shown, close the error and use 'Joystick PA' to align the left mark on the display into the correct position.
- Click on 'Pattern'.
- Go to Page 3 and select 'Left'.
- Click on 'Ready' then 'Go'. If no buzzer sounds, the recognition is successful. If this fails, attempt to adjust the illumination in the AGA/TVPA settings in the defined process.
- Click on 'Align' to resume the auto-alignment.

Reticles (masks) available in stepper

- warren1.rf : Gate Metal
- warren2.rf : a-Si island
- warren3.rf : Via
- warren4.rf : S/D

Jobs (processes) available in stepper

- /Liu/w1.job : Level 1, Gate Metal
- /Liu/w2overlay.job : Level 2, a-Si island, with auto-alignment through the a-Si island layer (this is successfully achieved even though the a-Si is not transparent)
- /Liu/w3overlay.job : Level 3, Via, with auto-alignment
- /Liu/w4overlay.job : Level 4, S/D, with auto-alignment

Calibration tests run after a stepper re-start

- IUC intensity uniformity check
- Reticle robotic arm check
- FRA fine reticle alignment check (using 'ideal' wafer)
- Rinse the front and back of the wafer carefully.
- SRC stage rotation correction

Intensity Uniformity Check

- Select COMMAND >ALPHABET >i >(wait) >iuc
- Select NEW ACQUISITION >Switch FILE 'OFF' to 'ON' >ACTIVATE. Click NEW >EXIT >MEASURE.
- In the best case, the difference in high and low (distribution) should be <2%. If >4%, then something is wrong.
- when END is displayed, click on FILE >Switch FILE 'ON' to 'OFF' >EXIT >GRAPHIC to show a visual representation of the intensity uniformity.

Stage Rotation Check This check calibrates the optic and stage rotation by measuring the difference in angle between marks on the optics and the stage.

- Load the Standard Reticle N03665-4 (in slot 14).
- COMMAND >ALPHABET >S >SRC.

- Note down the previous data ‘Rotation’ e.g. 6.308ppm >Click MEASURE
- When done press ‘Entry m’ (should be between -10 and 10 ppm. If greater than 20ppm there is a problem.
- Unload the Standard Reticle.

Other Stepper checks

- In Status, check the pressure (should be 1000hPa) and the life of the mercury lamp (maximum 200h lifetime).
- The coolant oil C-OIL should be plus/minus 0.05C around 19C.
- The STAGE and BERTH1/BERTH2 and LENS temperature measurements should be at 23C.

A.4 Thin-film resistor recipe

Prepare substrate

- Clean glass substrate as per procedure listed later in this chapter.
- Use a glass scribe (or the dicing saw) to remove approximately 1cm corners of the glass substrate. This is to allow the glass to fit on top of a 4in wafer (this can be done before or after cleaning).
- Deposit 150nm SiN_x passivation layer (SiH4/NH3/H2=6/60/200sccm, 35mins, 500mT, 5W, 200/200/200C).

Deposit resistor stack

- Deposit up to 150nm a-Si (SiH4/H2=16/200sccm, 60mins, 500mT, 4W, 200/200/200C).
- Deposit 30nm n^+ a-Si (SiH4/PH3=44/10sccm, 4mins, 500mT, 4W, 200/200/200C). Note- PH3 is diluted 1% in H2.

Etch a-Si

- Pre-bake on hot plate at 95C, 3mins.
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s.
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s.
- Soft-bake on hot plate at 95C, 1min.
- ISLAND MASK: UV Intensity = 3.5 mW/cm^2, 40s.
- Develop: AZ300MIF, 60s.
- Hard-bake on hot plate at 95C, 3min.
- Tape glass sample onto 4in wafer.
- Etch a-Si using Samco 800, recipe 66, 42 cycles.
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min.

Liftoff-patterning and deposition

- Pre-bake on hot plate at 95C, 3mins.
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s.
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s.
- Soft-bake on hot plate at 95C, 1min.
- RESISTOR METAL MASK: UV Intensity = 3.5 mW/cm^2, 40s.
- Develop: AZ300MIF, 60s.
- No hard bake.
- Sputter using Angstrom Sputterer Cr (100nm, recipe SturmDC2Cr1kA).

- Strip PR: sonicate in acetone until liftoff complete (Q-tip may be necessary), then sonicate in isopropanol for 1 min.

Deposit and pattern passivation layer

- Ar Plasma on sample in N-chamber (Ar=50sccm, 4mins, 500mT, 12W, 200/200/200C).
- Deposit 250nm SiN_x gate dielectric (SiH4/NH3/H2=6/60/200sccm, 50mins, 500mT, 5W, 200/200/200C)
- Pre-bake on hot plate at 95C, 3mins.
- Spin on HMDS: Speed=4000rpm, Ramp=1000rpm/s, Time=40s.
- Spin on AZ5214: Speed=4000rpm, Ramp=1000rpm/s, Time=40s.
- Soft-bake on hot plate at 95C, 1min.
- PASSIVATION MASK: UV Intensity = 3.5 mW/cm^2, 40s.
- Develop: AZ300MIF, 60s.
- Hard-bake on hot plate at 95C, 3min.
- Tape glass sample onto 6in wafer.
- Etch SiN_x using PT720, CF_4/O_2=70/10sccm, 100mT, 100W, 3:40mins.
- Strip PR: sonicate in acetone for 1 min, then sonicate in isopropanol for 1 min.

Anneal sample

- Anneal sample in PECVD for 1h at 180C (or at the maximum temperature possible in the vacuum oven for 1h).

A.5 PECVD uniformity

Measurement of PECVD uniformity of doped amorphous silicon performed in November 2012 in the P-chamber shown in Figure A.1.

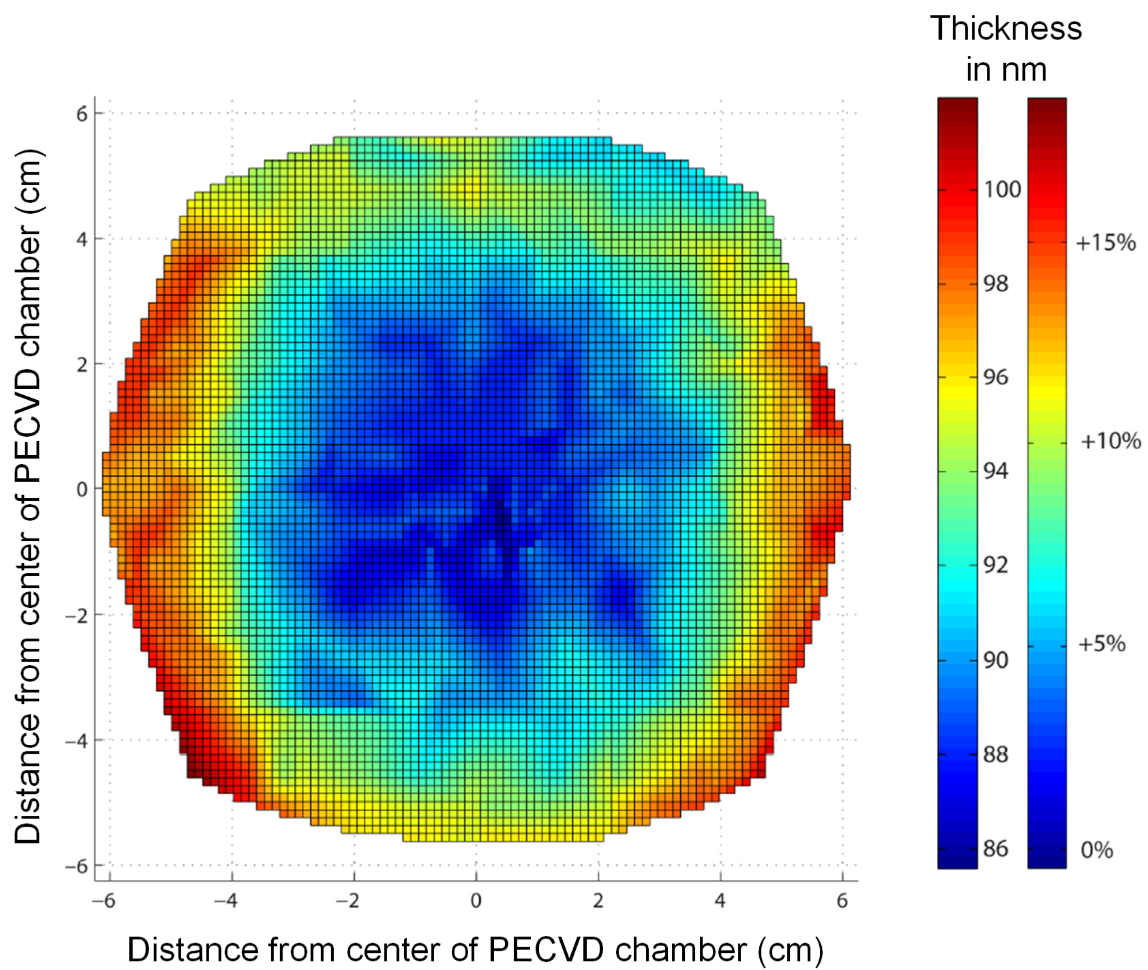


Figure A.1: P-chamber uniformity

A.6 Glass chamfer cutting procedure

The following describes a procedure for removing the corners of glass substrates and scoring marks for alignment of the gate layer mask as shown in Figure A.2. These settings are to be used with the ADT dicer in bowen hall.

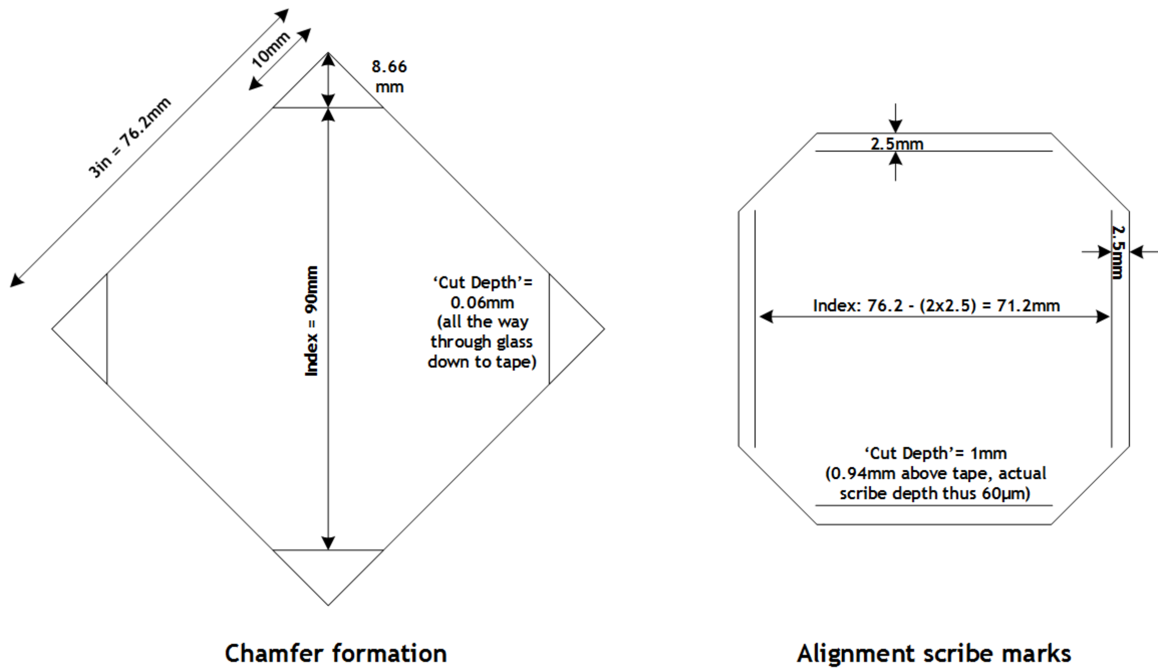


Figure A.2: Dicing of corners and scoring of alignment guides

- Prepare bare glass slides by spinning photoresist (e.g. AZ5214) on one surface.
- Affix glass slide to the dicing tape, as shown in Figure A.3

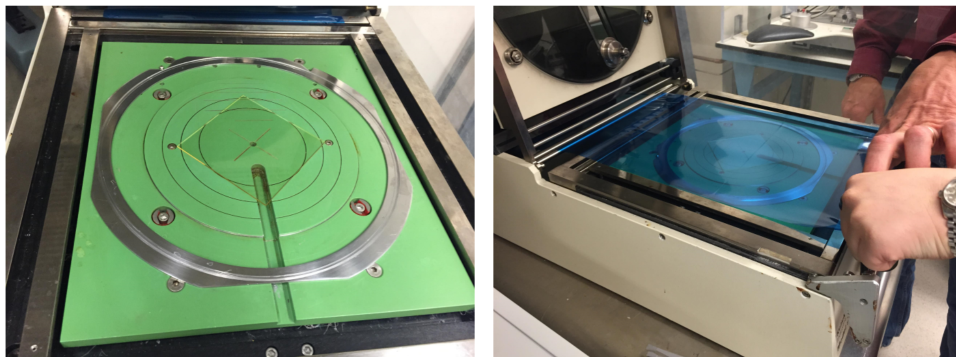


Figure A.3: Mounting on dicing tape, in diamond configuration

- Click Auto, Define Job. Select the recipe Glass_1500_chmfr_3x3_1mm. Click apply.
- Load the mounted glass slide in the dicer, with the slide facing up.
- Enter Camera Mode.
- Check which blade is loaded by right-clicking on the blade bottom left, then going to 'Blade Type'. To change it, click on 'Blade Change'.
- Open the right chamber, push the lever down to open the blade window, use the torque wrench to remove the existing blade. Make sure the spacer is on, load a 'Resinoid Hubbed CA-010-325-125' blade using the blade removal tool, then use the torque wrench to lock it in place.
- In the software select 'Choose Blade' and pick the resinoid blade. For successful cutting, the blade bottom left should show F greater than 1mm. Press finish and the dicer will measure the blade exposure.
- Click 'Load wafer' and Finish.
- Click Wafer Auto Alignment, go to region of the right corner (should be done automatically) and click on the right corner. Click Next, go to the region of the left corner (again, should be automatic) and click on the left corner. Click next to complete the horizontal rotation alignment and click Finish.
- Go to the top corner and then using the 'Yr' option of S mode, go down 8.88mm (or the amount that the diagonal is measured to be minus 90, divided by two). Click Finish.
- At this point the sample rotates 90 degrees. There is no need to realign, so click Next, then Next.
- Define the cut position again by going to the top corner and going down 8.88mm. Click Finish, followed by 'Full Cut'.
- Say 'Yes' to 'Perform Y offset check', position the blade outside the region of the glass sample and perform a single cut in the tape. Focus on cut and increase the size of the blue window to fill the cut width. Click Finish.

- The cuts are performed.

In order to repeat this for the alignment scribe marks, switch to recipe Glassalign-scribes_3x3_1mm_GPC. In this recipe, cut depth is changed to give a 60 micron scribe, the index is changed to 71.2mm and the cut speed is increased to 5mm/s.

Figure A.4: Parameters for the chamfer cut recipe

A.7 Glass cleaning procedure

- Blow dry the new glass slides to remove white particles, and place in metal container.
- Add one cap of Micro-90 and fill the container with water.
- Heat the container on the hot plate (on high) for 1 hour.
- Sonicate for 1 hour.

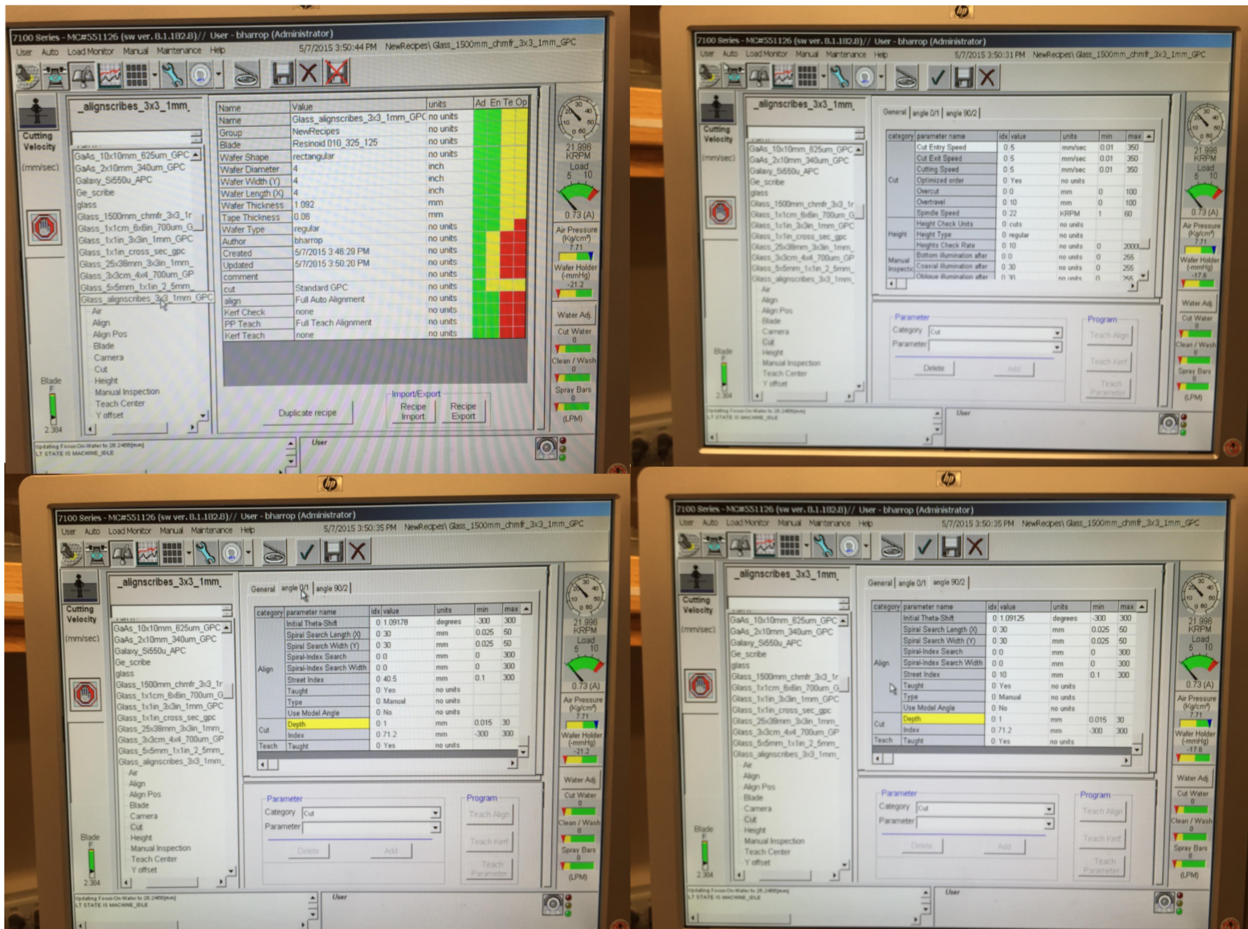


Figure A.5: Parameters for the alignment guide scribe recipe

- Drain the metal container, repeat this process once with Micro-90 again, and then once more with just water.
- Drain the container and re-fill with water.

A.8 2015 Training Mask

In 2015, the TFT training mask was redeveloped to accommodate the new ZnO process and increase the number of test structures. The top half of the sample can be used for a-Si training whilst the bottom half for ZnO training (not simultaneously). The mask layout is shown in Figure A.6 consisting of:

1. TFTs with different widths and channel lengths (can be used for contact resistance extraction)

2. A large island of semiconductor for 4-point probe measurement

3. Source/Drain and Gate metal traces for metal resistivity measurement

4. Capacitors

A.9 ITO Processing technique

Etching of Indium Tin Oxide on PET can be done using 10:1 diluted HCl. For Sigma Aldrich ITO 1ft x 1ft x 5mil, with 60 Ohms per square, 2.5 mins are required for a complete etch.

A.10 Removal of polyimide on ICs

The top passivation of IBM 130nm fabricated ICs consists of a stack of 1.35 microns of oxide, 0.45 microns of nitride and 2.5 microns of polyimide. In order to remove the polyimide, a oxygen plasma can be performed in the Tepla for 6 x 10 minutes (using the standard resist strip recipe).

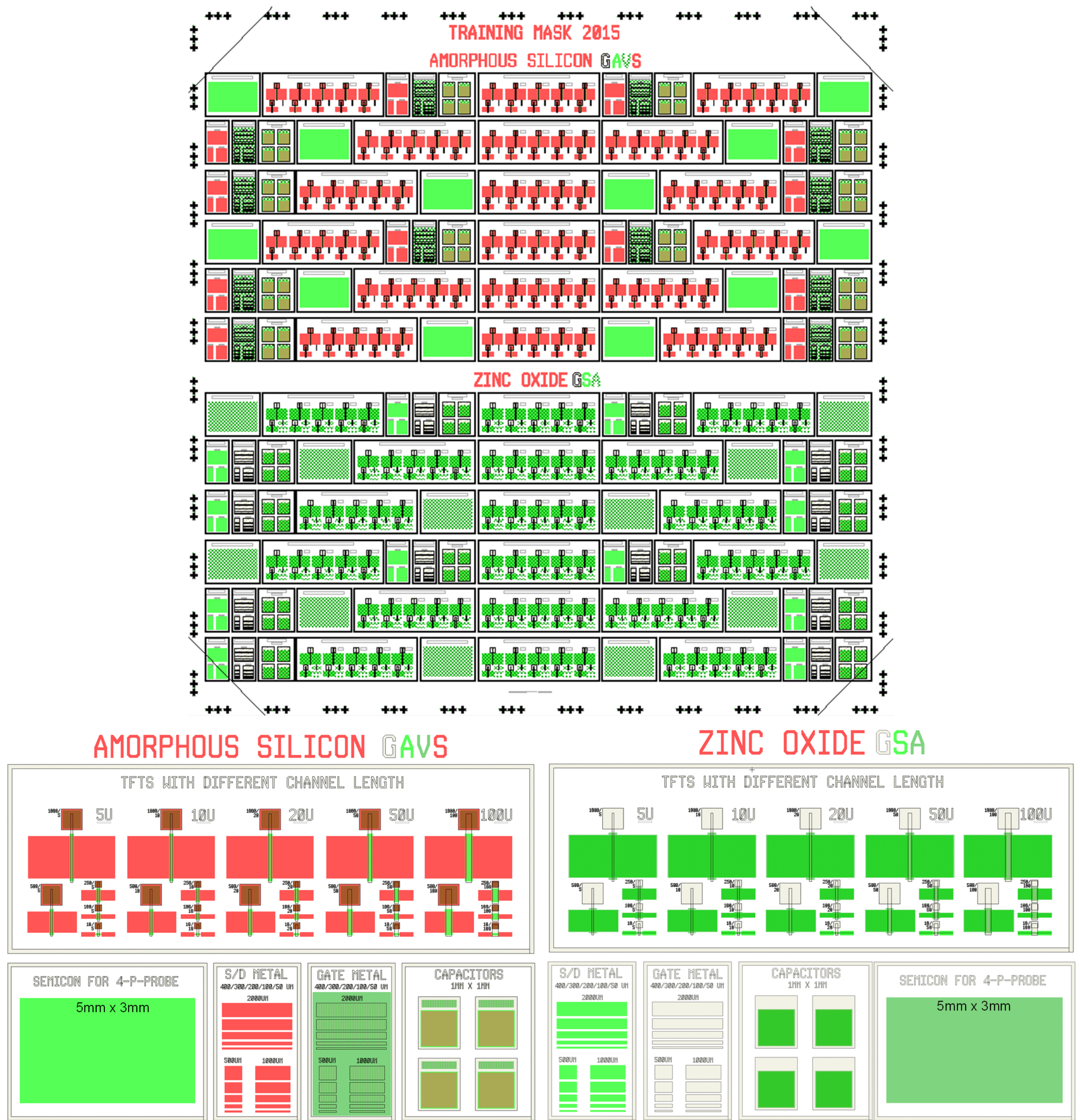


Figure A.6: 2015 New Training Mask

Appendix B

Catalogue of mask sets

This chapter presents an index of all the masks sets manufactured for the work presented in this thesis, stored in three black mask boxes in J425.

Mask Box 1:

Slot	Mask Set	Date	Layer
1	Scanning Circuit and X-Coupled Oscillators (Katherine Song)	5/2011	Gate
2			Active
3			Active (with extra a-Si regions for crossovers, WRL 7/2011)
4			Via
5			S/D
6			Passivation (WRL 6/2011)
7	Large TFTs and Scanning Elements	7/2011	Gate
8			Active
9			Via
10			S/D
11			Passivation

12	Scanning Elements and Input Circuits	8/2011	Gate
13			Active
14			Via
15			S/D
16			Passivation
17	Scanning Elements and Input Circuits V2	11/2011	Gate
18			Active
19			Via
20			S/D
21			Passivation
22	Large TFTs and Ring Oscillators	12/2011	Gate
23			Active
24			Via
25			S/D
26			Passivation
27	Ring Oscillators v2	1/2012	Gate
28			Active
29			Via
30			S/D

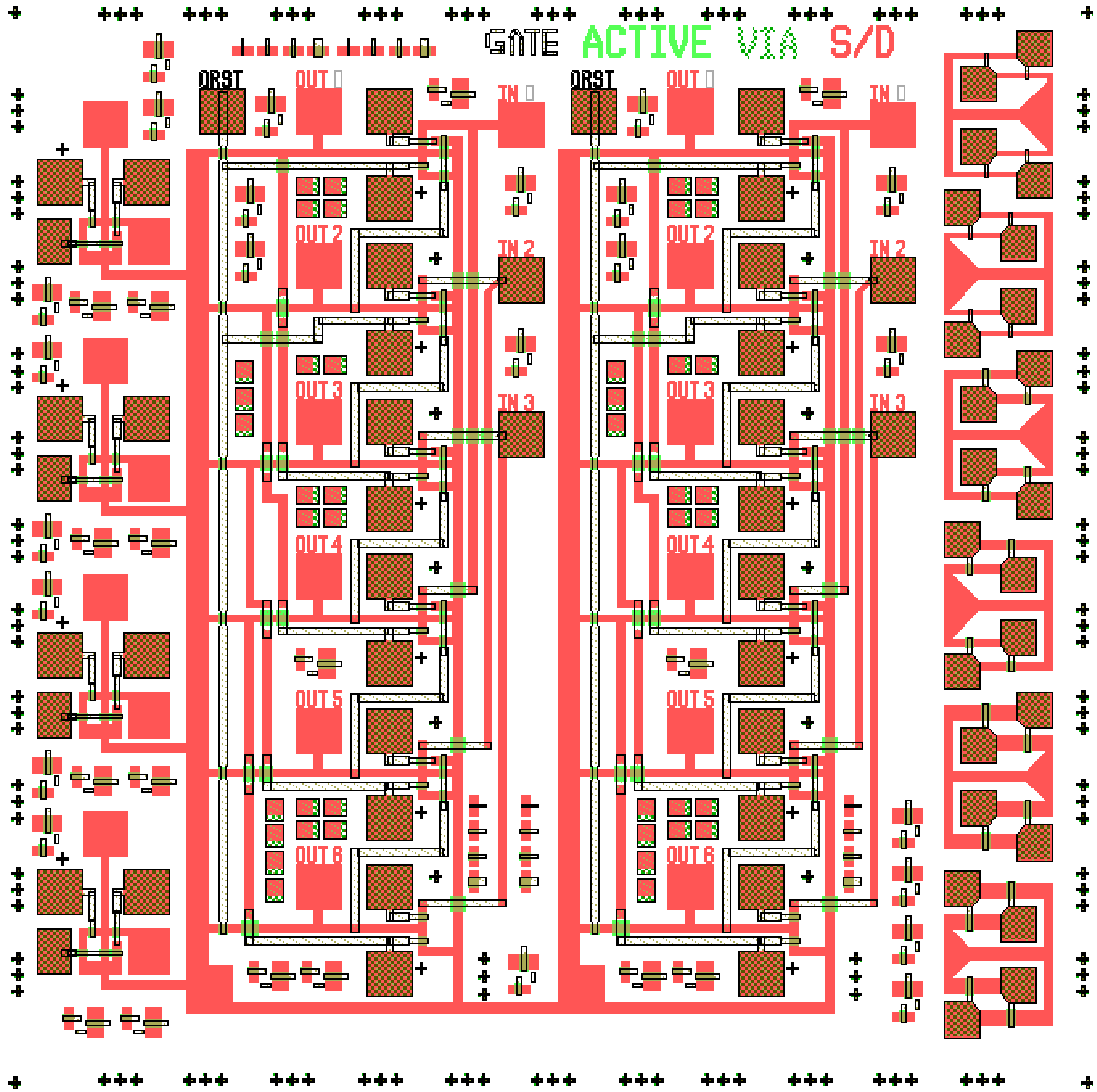


Figure B.1: Individual scan elements, two scan chains, cross-coupled TFTs for LC oscillators (WRL_Jul2011_scanelements.tdb)

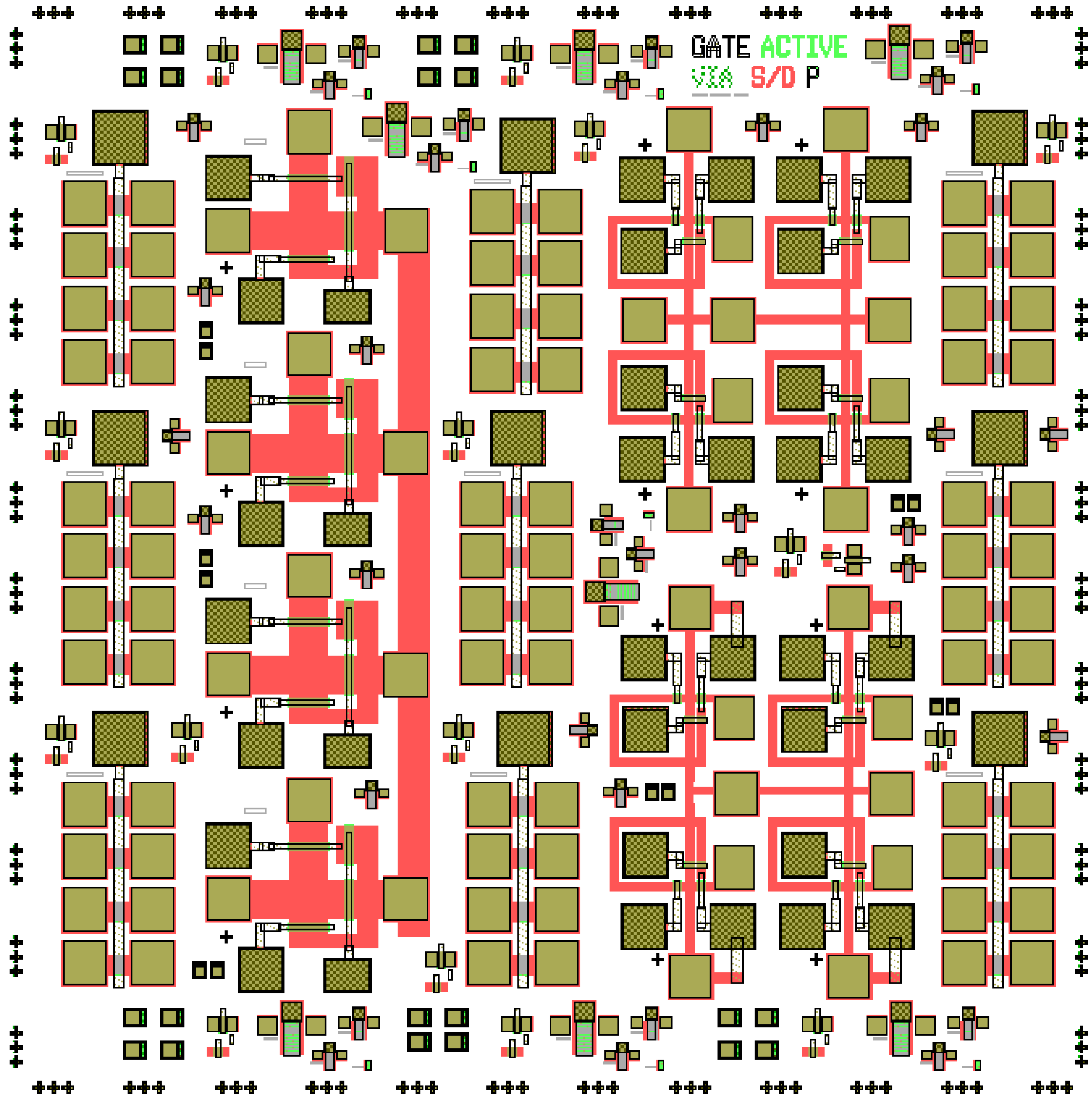


Figure B.2: Individual scan elements with wider TFTs, individual scan elements with integrated capacitors, nine groups of four wide TFTs (WRL-LargeTFTMaskv2.tdb)

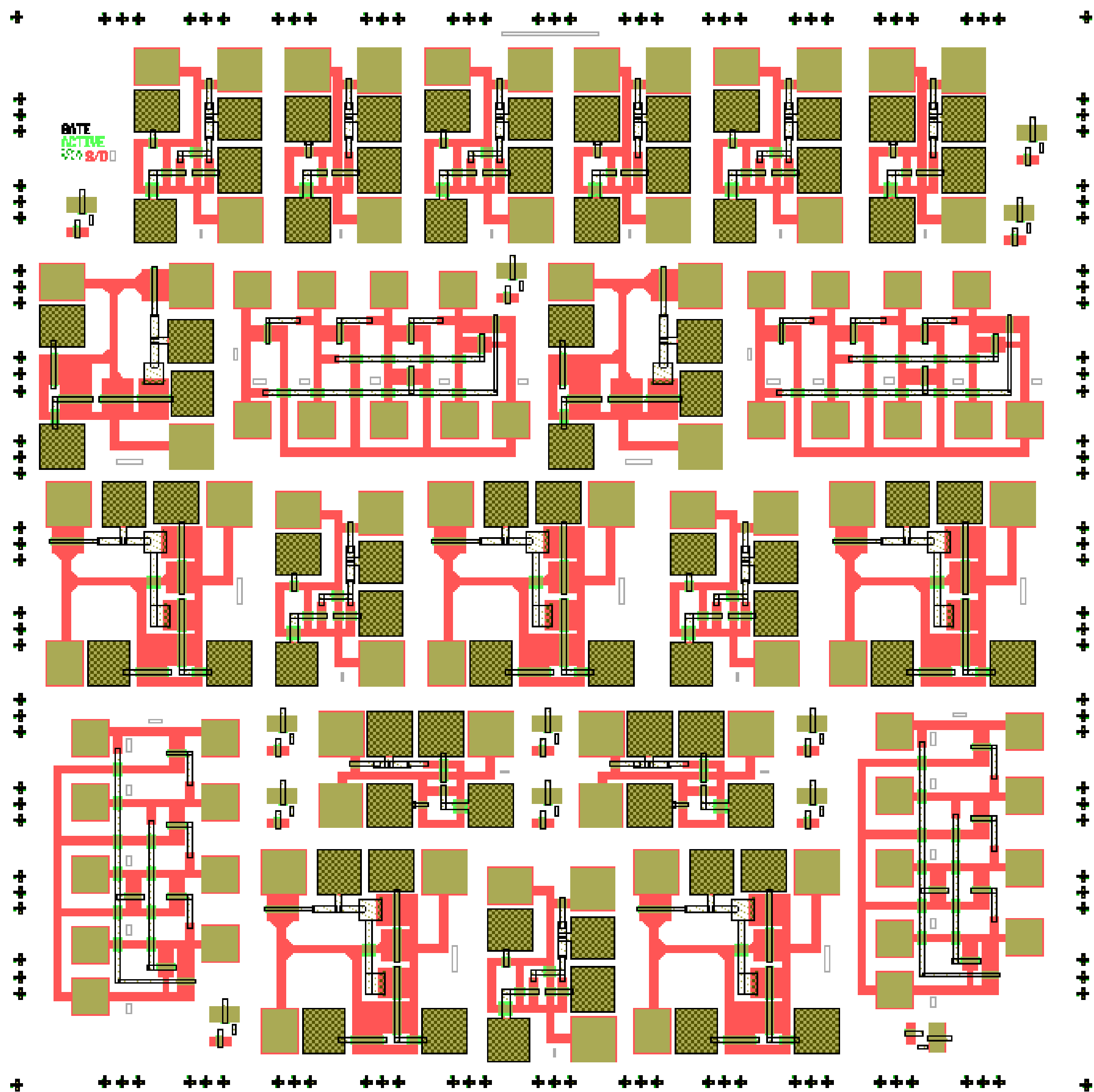


Figure B.3: Individual scan elements, input circuits with reset capability (WRL_Aug2011_scanning.tdb)

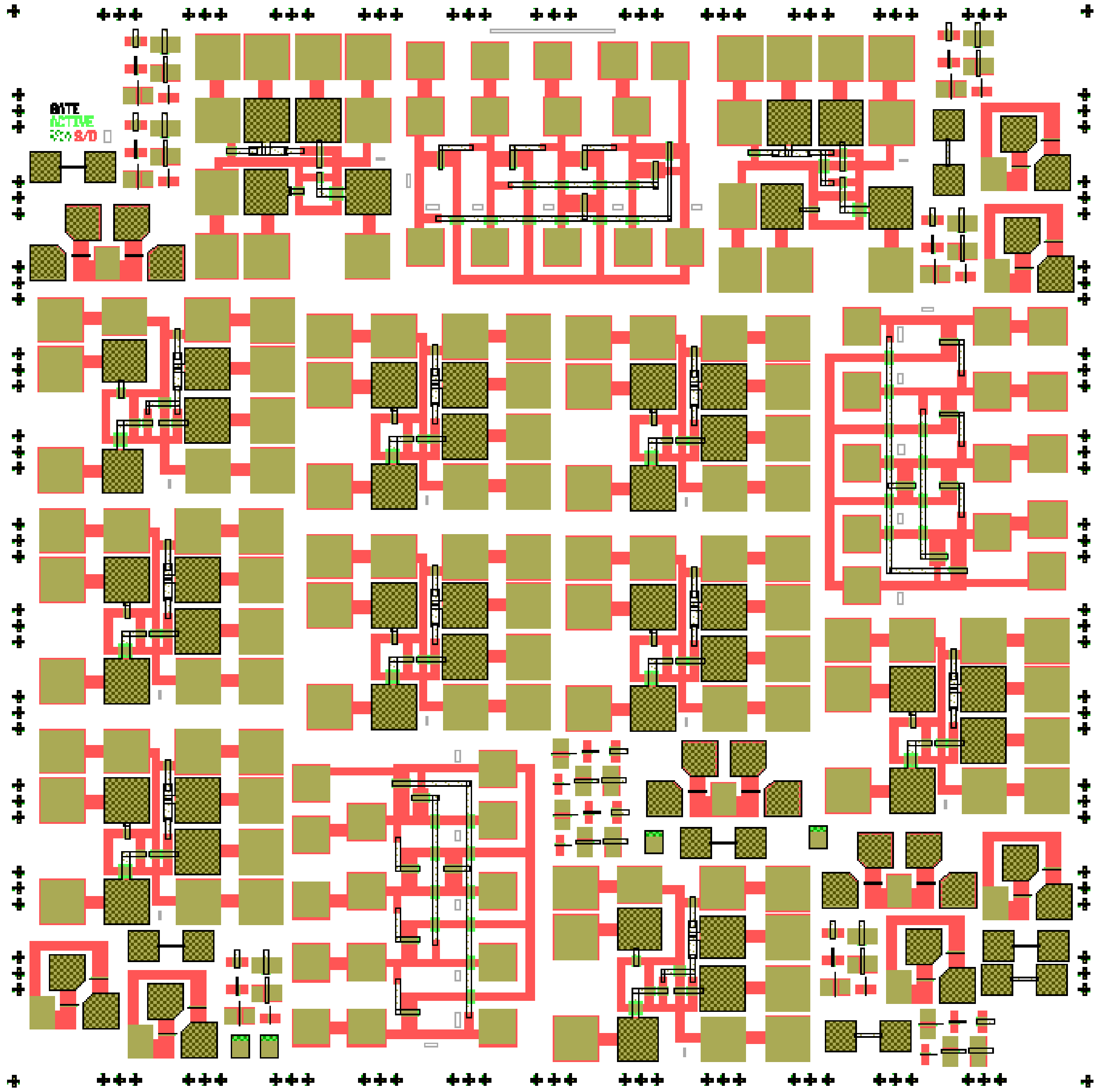


Figure B.4: Individual scan elements and input circuits with testing capability for on-flex assembly. Double pads are used- alligator clips can be connected to one and once the circuit has been ascertained functional, those can be cut off using a blade or scissors- this mitigates damage to the pad that will be connected to the copper backplane using conductive tape (WRL_Oct2011_scanning.tdb)

Figure B.5: Ring oscillators, test array of large TFTs and differential pairs of TFTs (with tail current source) (WRL-LargeTFTMask-Nov11.tdb)

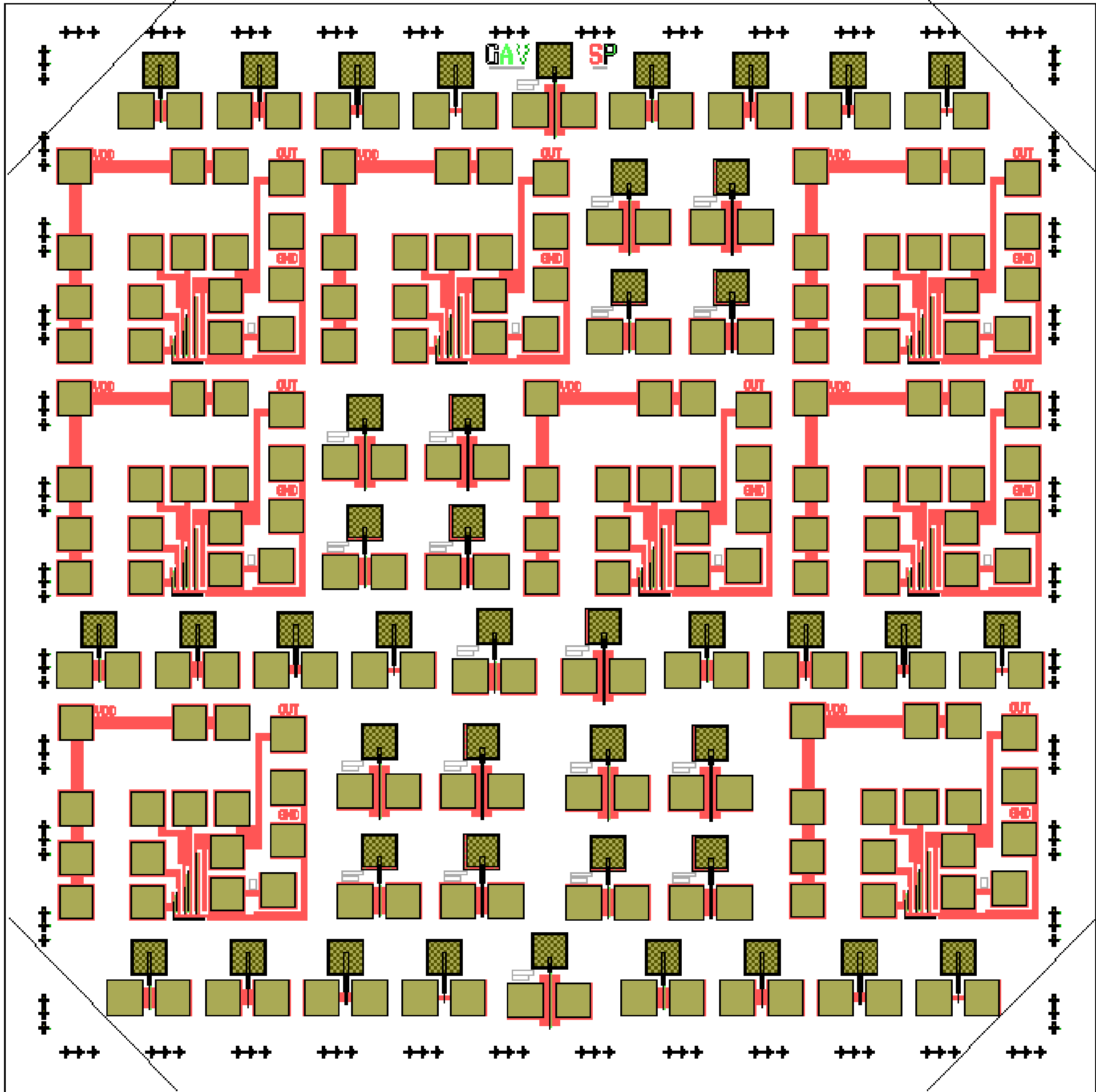


Figure B.6: Ring oscillators (WRL-RingOscillatorJan2012Original.tdb)

Mask Box 2:

Slot	Mask Set	Date	Layer
1	Ring Oscillators v2	1/2012	Passivation
2	Resistors v1	1/2012	Active
3			S/D
4			Passivation
5	Resistors v2	2/2012	Active
6			S/D
7			Passivation
8	Ring Oscillators with integrated resistors	2/2012	Active
9	(Use same gate/via/passivation as v2)		Resistor Liftoff
10			S/D
11	LC Oscillators and Electrode Array Matrix	3/2012	Gate
12			Active
13			Via
14			S/D
15			Passivation
16	Radio Circuits v1 (All circuits)	7/2012	Gate
17			Active
18			Via
19			S/D
20			Passivation
21			Connectors Type 1
22			Connectors Type 2
23	Radio Circuits v2 (Comparators)	8/2012	Gate
24			Active
25			Via
26			S/D
27			Passivation

28			Connectors
29	Gilbert Cells and 3 Phase Circuits	8/2012	Gate
30			Active

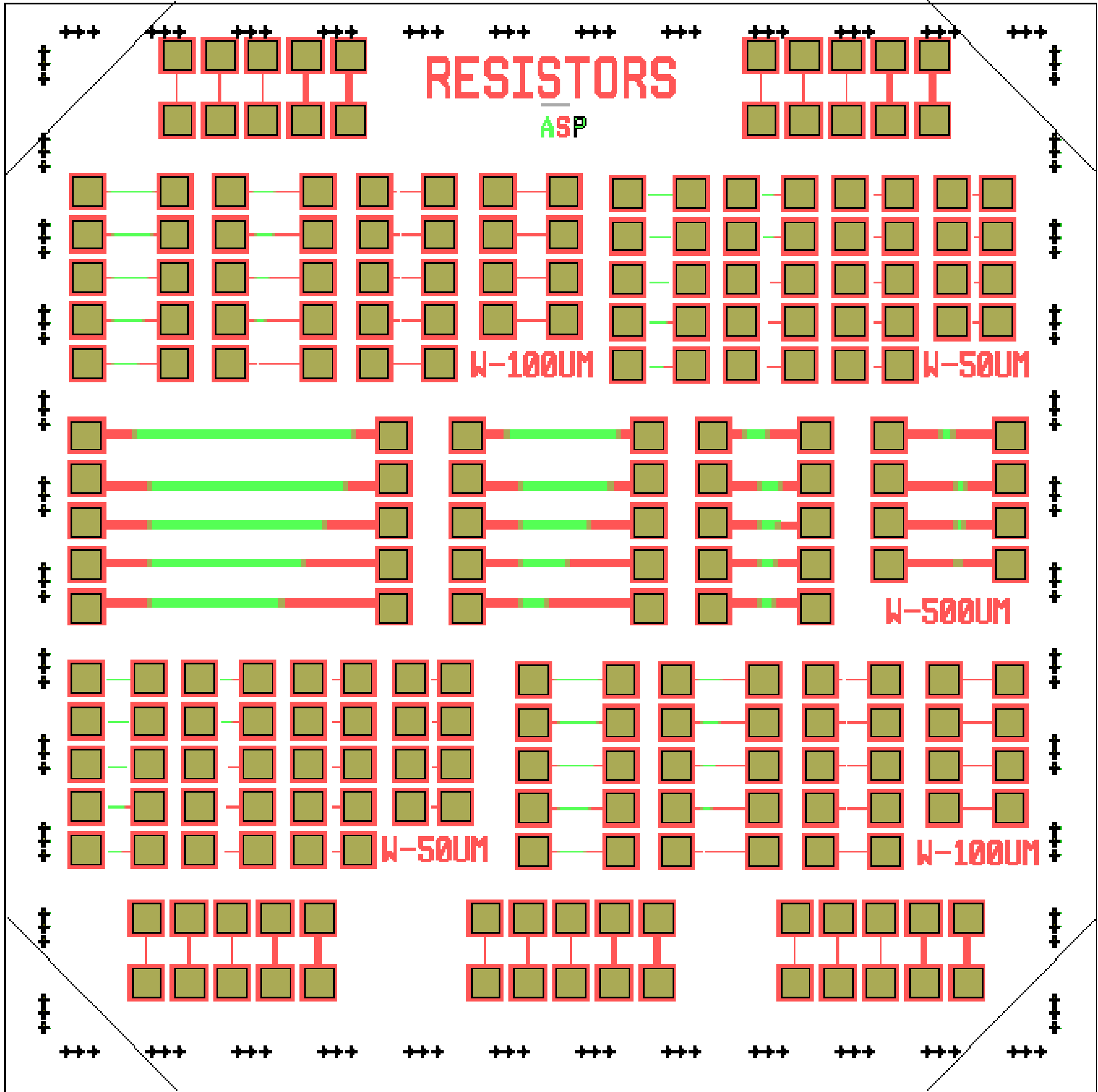


Figure B.7: Thin-film resistors (WRL-Resistors.tdb)

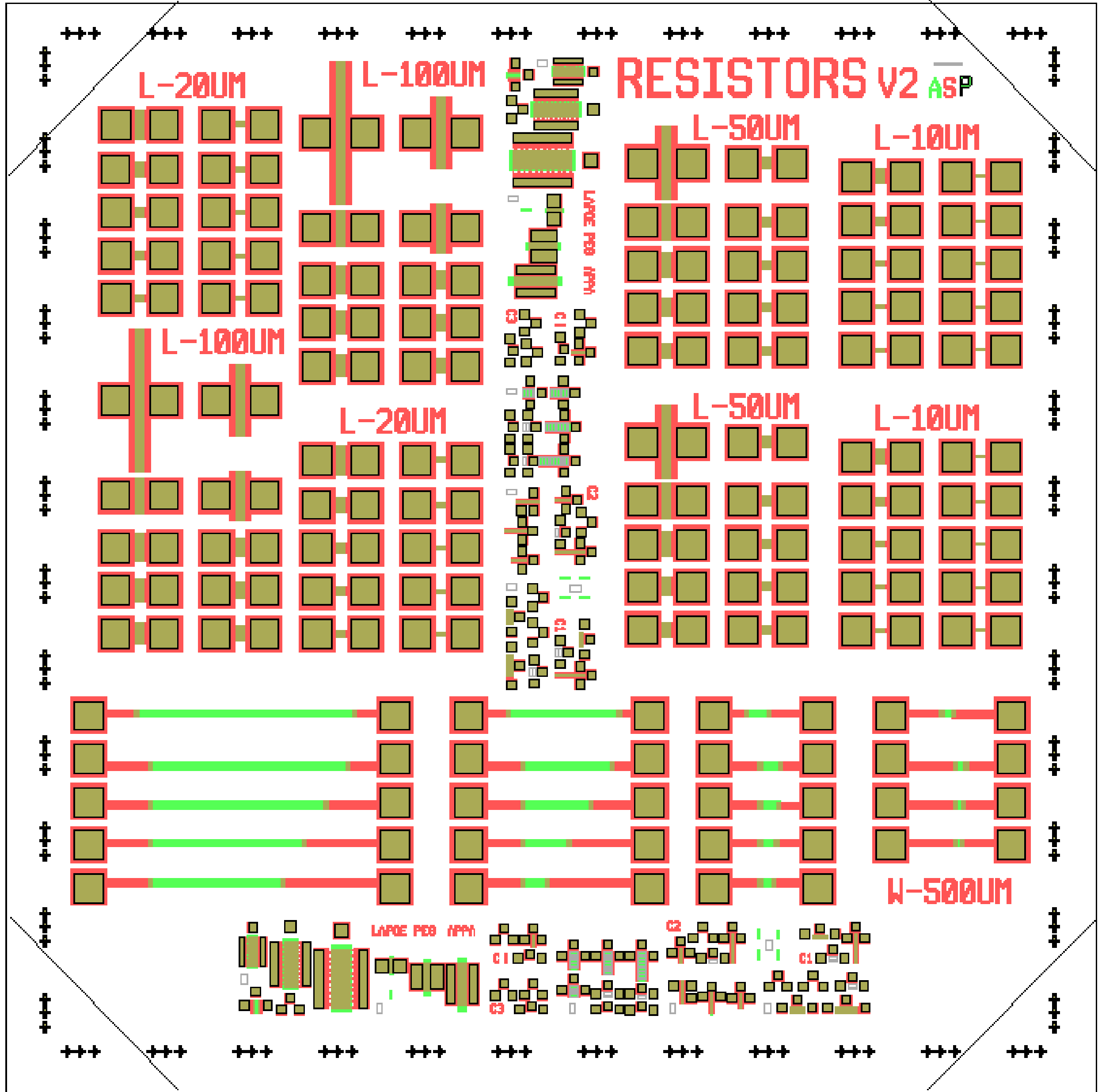


Figure B.8: Thin-film resistors of more appropriate dimensions for resistances on the order of 100kOhm (WRL-Resistorsv2.tdb)

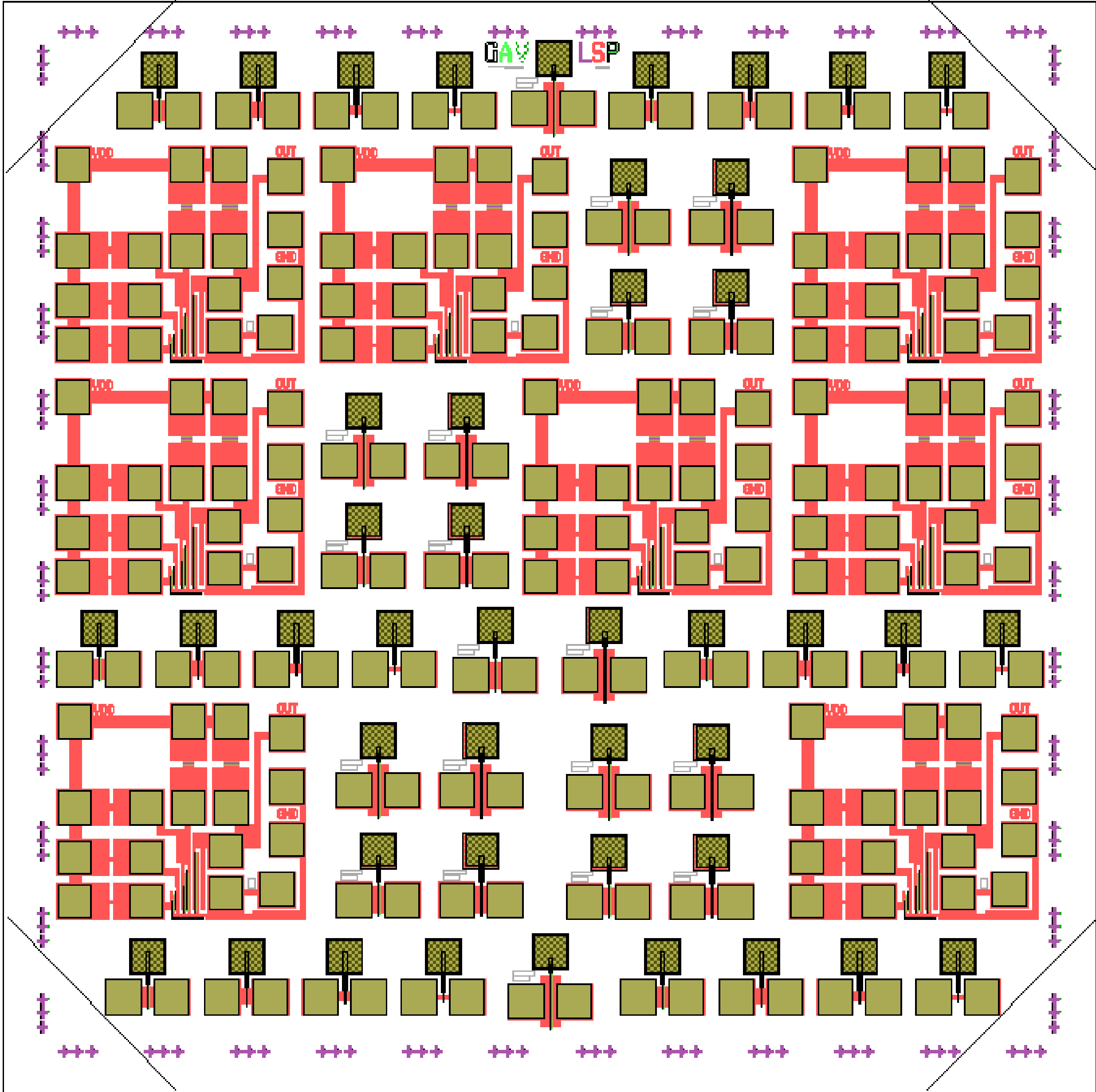


Figure B.9: Ring oscillators with integrated thin-film resistors (WRL-RingOscillatorJun2012.tdb)

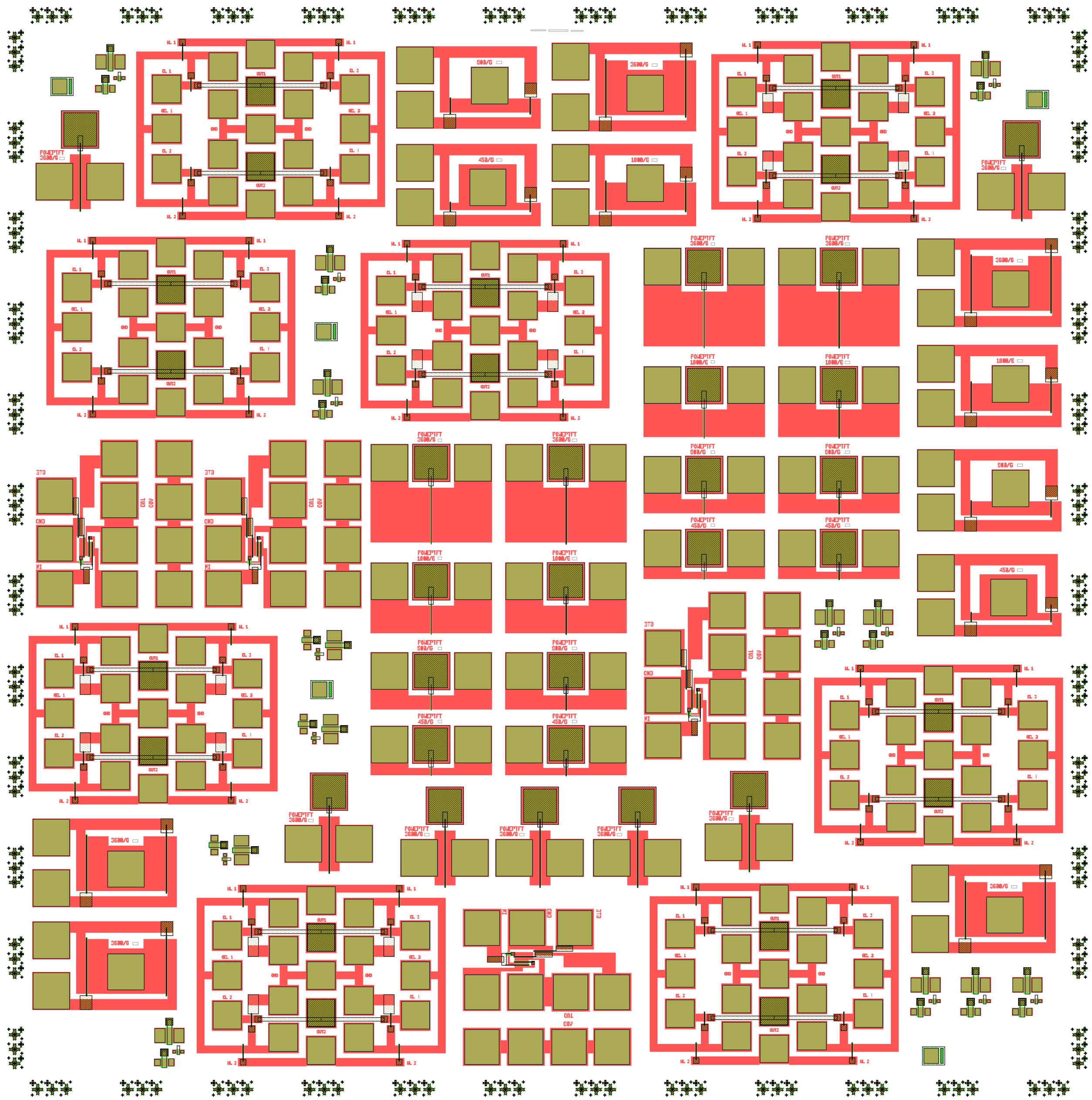


Figure B.10: LC Oscillators, Power (wide) TFTs and Electrode Array Matrix for T. Moy's Undergraduate thesis. Also has more compact scan elements, but never tested. (TMWR-TFTMask.tdb)

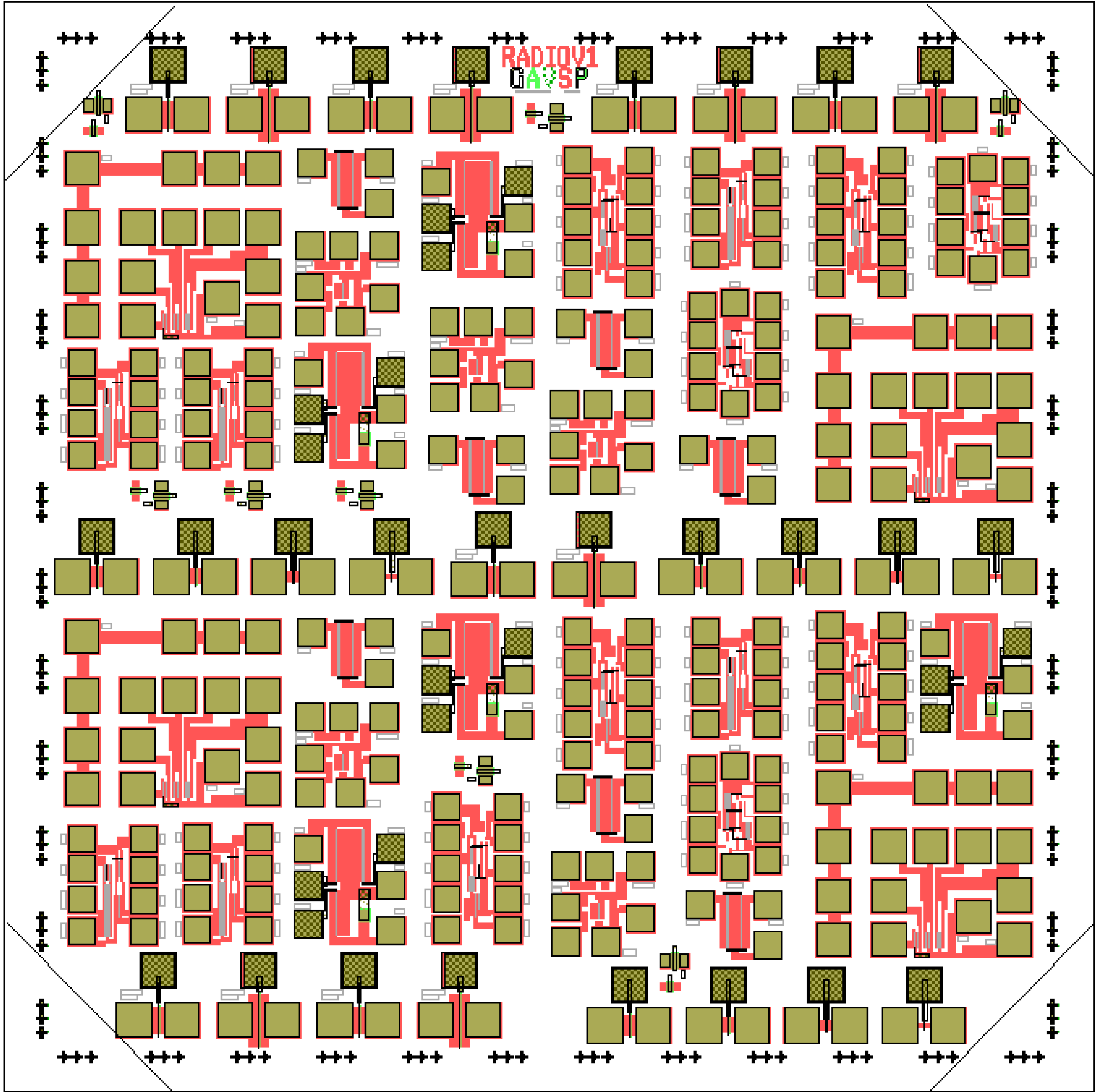


Figure B.11: Thin-film radio circuits: comparators, digital logic, LC oscillator, peak detector, quench generator (WRL-Comparator72012.tdb)

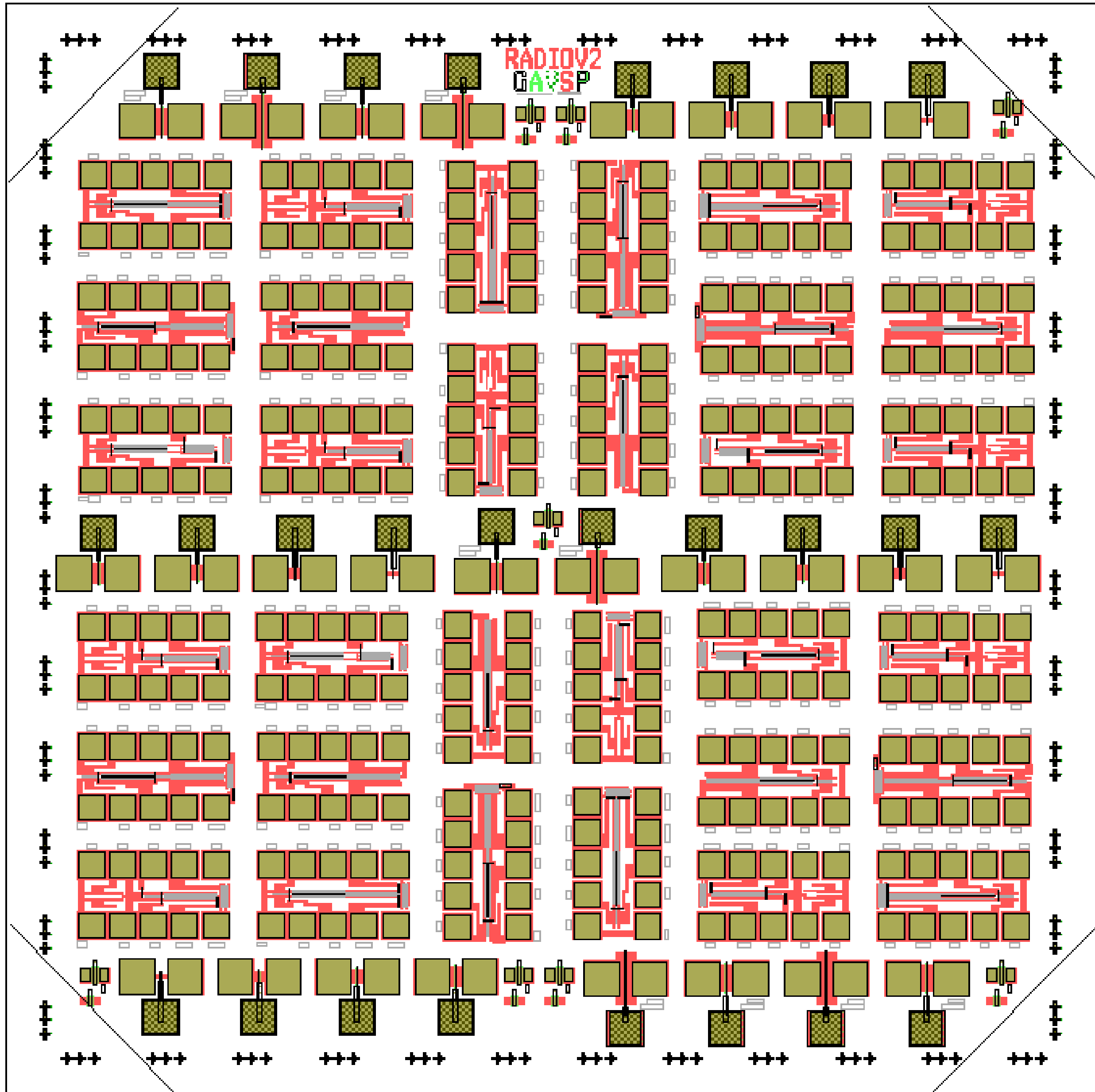


Figure B.12: Thin-film radio circuits: comparators (WRL-Comparator82012.tdb)

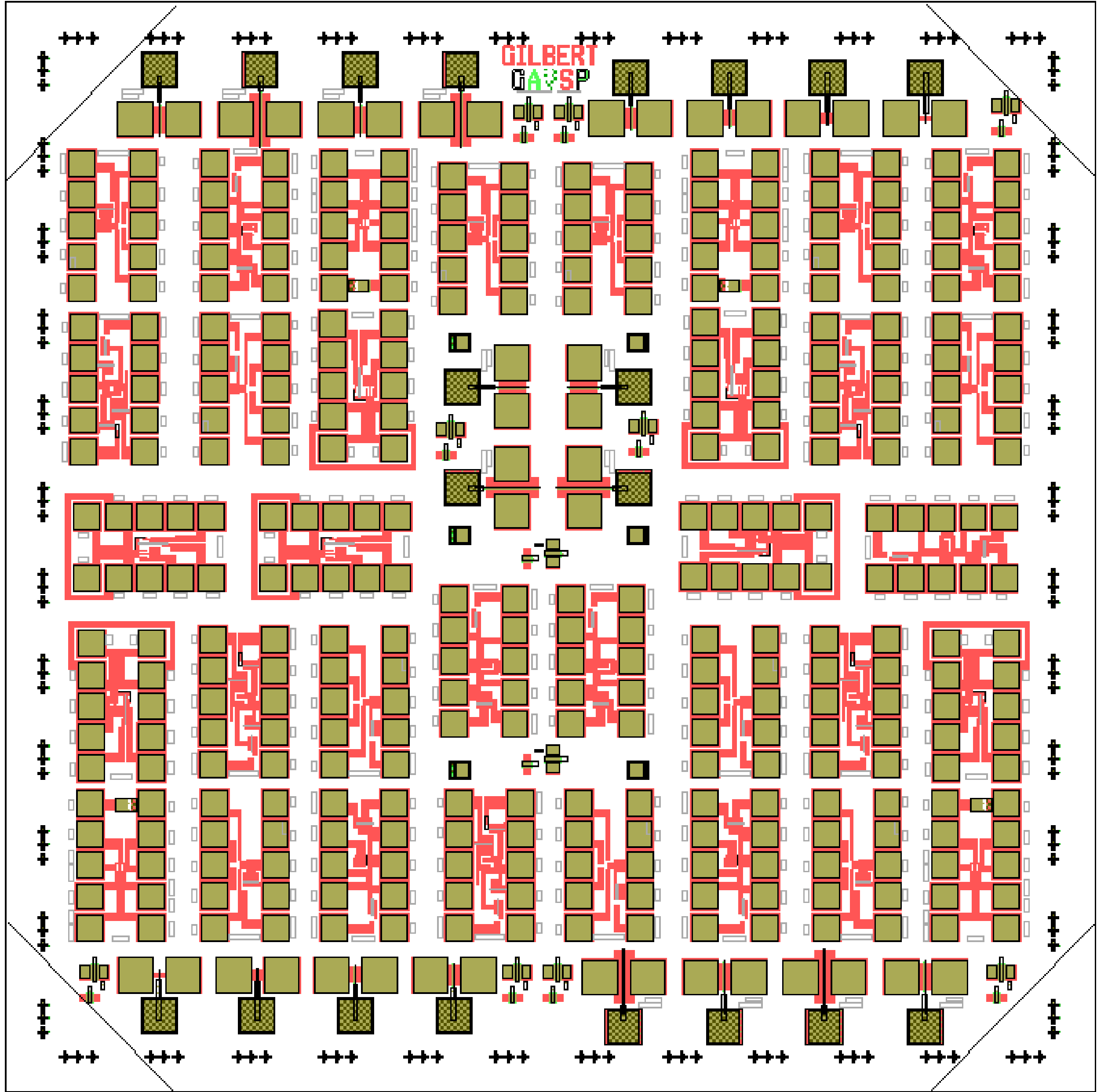


Figure B.13: Gilbert cells and 3-phase circuit elements (WRL-Gilbert82012.tdb)

Mask Box 3:

Slot	Mask Set	Date	Layer
1			Via
2			S/D
3			Passivation
4	Colpitts circuits	12/2012	Gate
5			Active
6			Via
7			S/D
8			Passivation
9	Battery Management Circuits	2/2013	Gate
10			Active
11			Via
12			S/D
13			Passivation
14	Battery Management with integrated resistors and self aligned TFTs	2/2013	Gate
15			Active
16			Via
17			S/D
18			Resistor
19			Passivation
20			Connectors
21	Self-Aligned TFTs (never used)	6/2013	Gate
22			Active
23			Via
24			S/D
25	IC Patterning	8/2013	
26	IC Silicon Breakout Carrier v1	1/2014	

27	IC Silicon Breakout Carrier v2 (Closer carriers)	1/2014	
28	Silicon Breakout Carrier for Glass MEMS Samples	1/2014	
29	TFT Classifiers	4/2014	Gate
30			Active

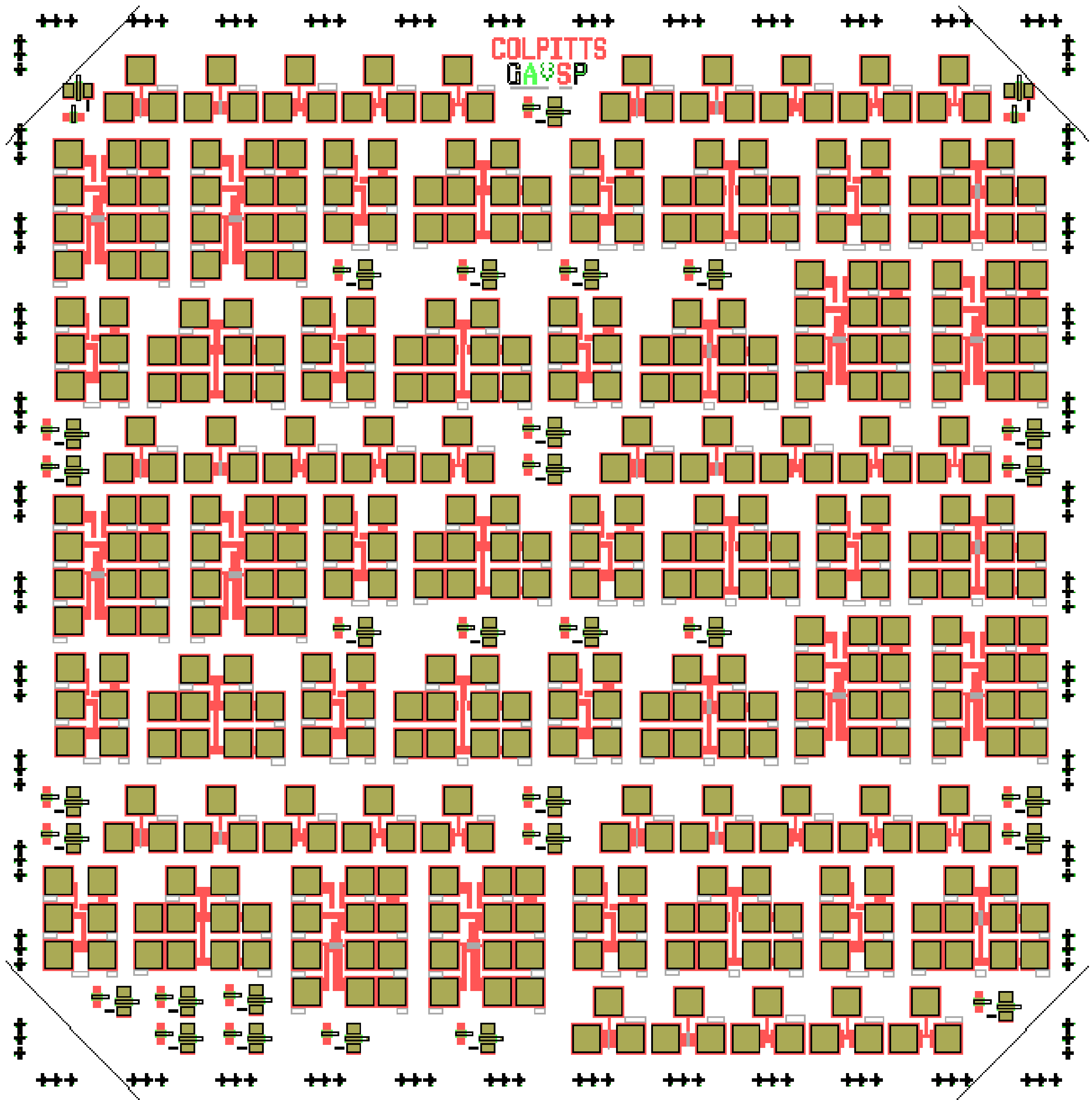


Figure B.14: Colpitts circuits (WRLMEMScirc.tdb)

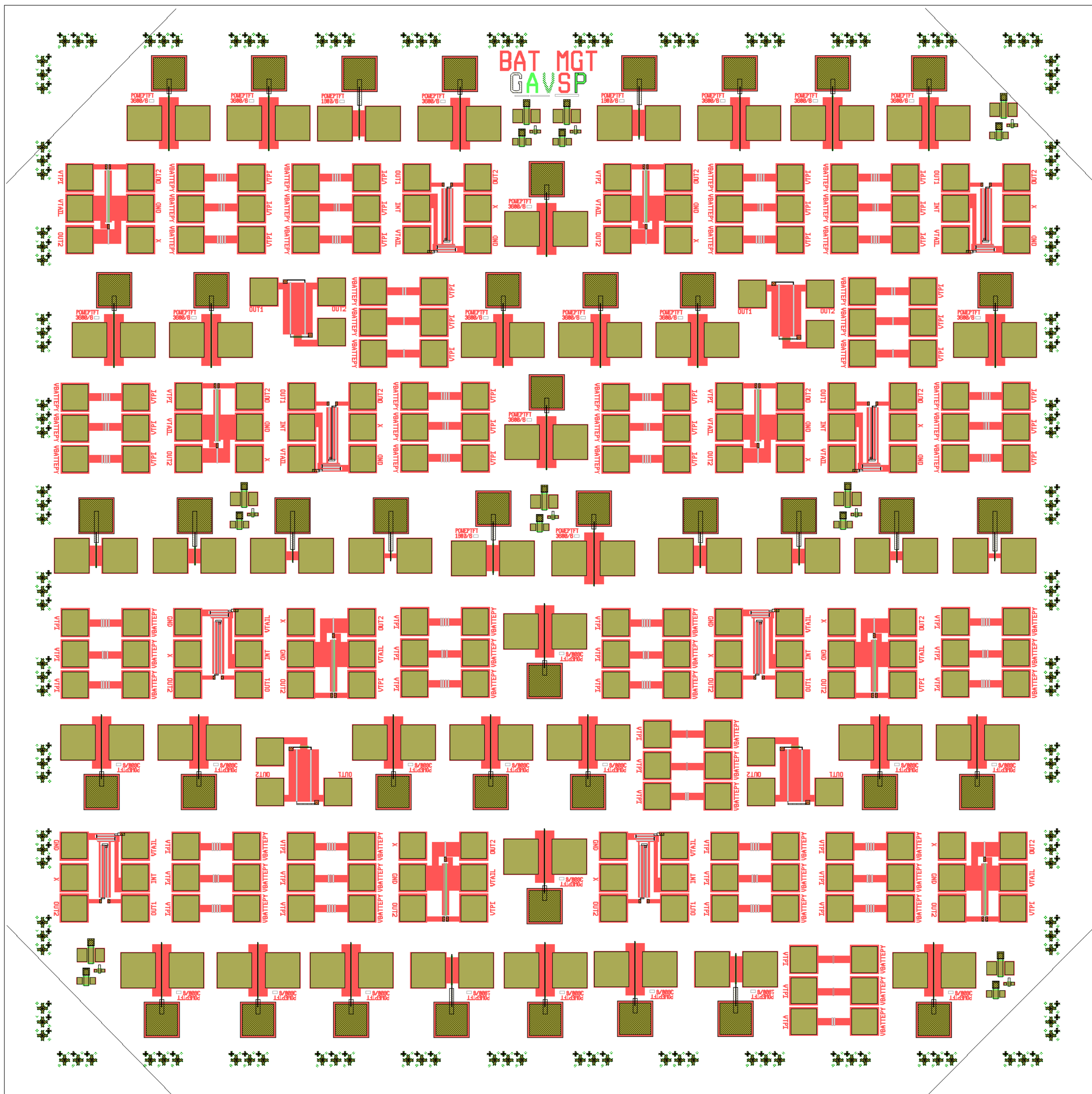


Figure B.15: Battery management circuits (WRLBatteryCharger12013.tdb)

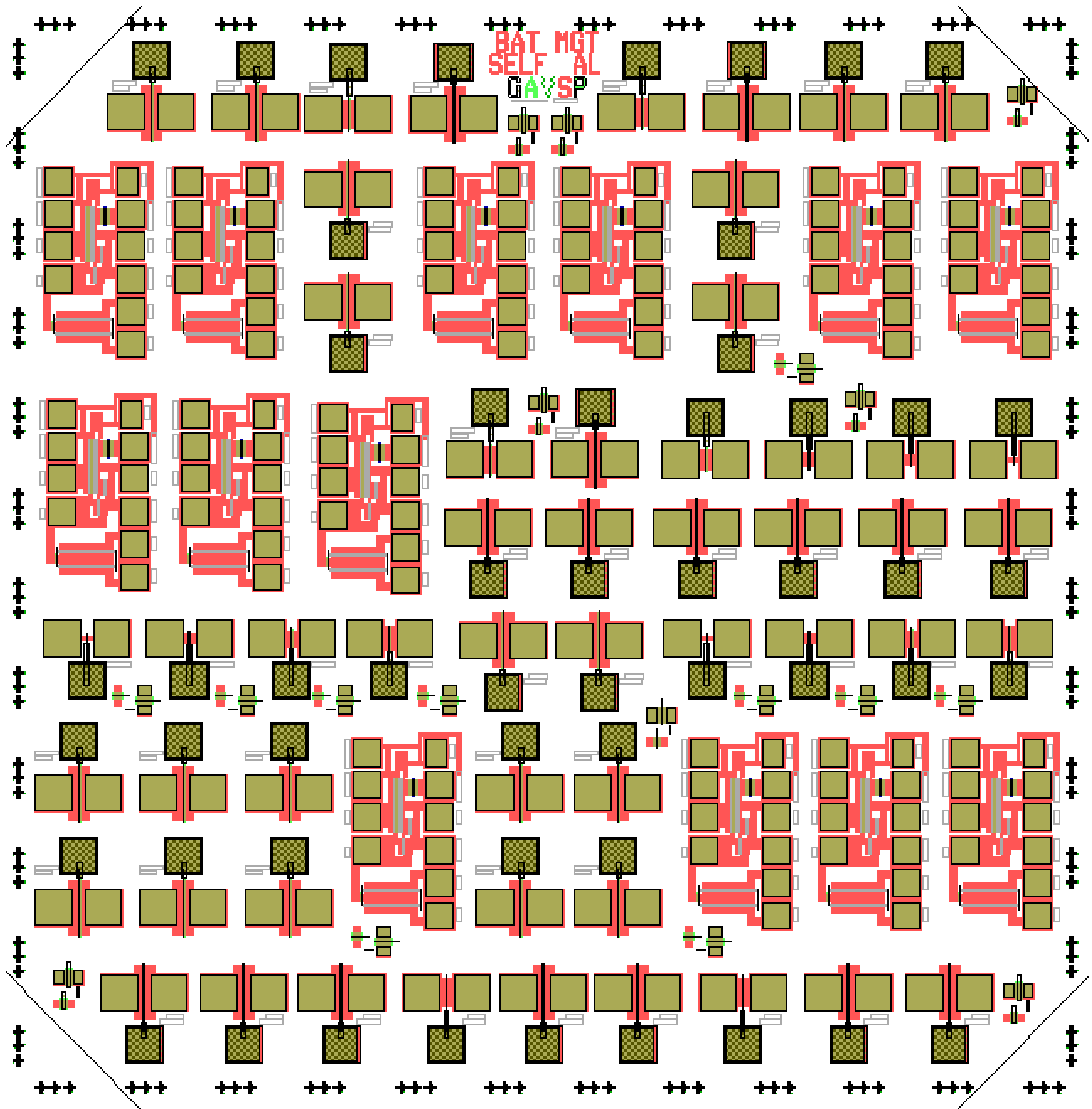


Figure B.16: Battery management circuits with integrated resistors and self aligned TFTs (WRL-BatteryCharger22013.tdb)

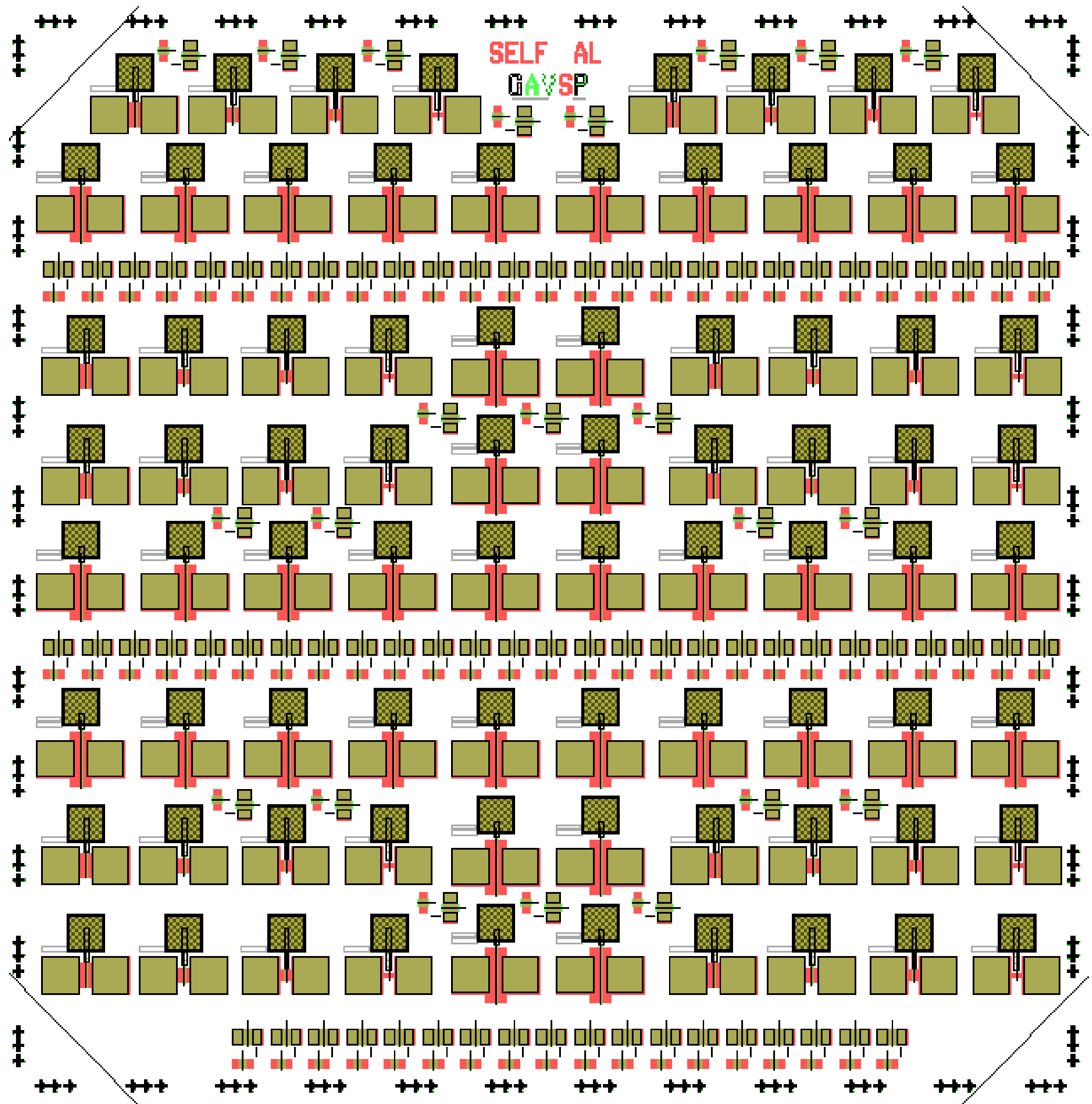


Figure B.17: Self aligned TFTs (WRLSelfAl62013.tdb)

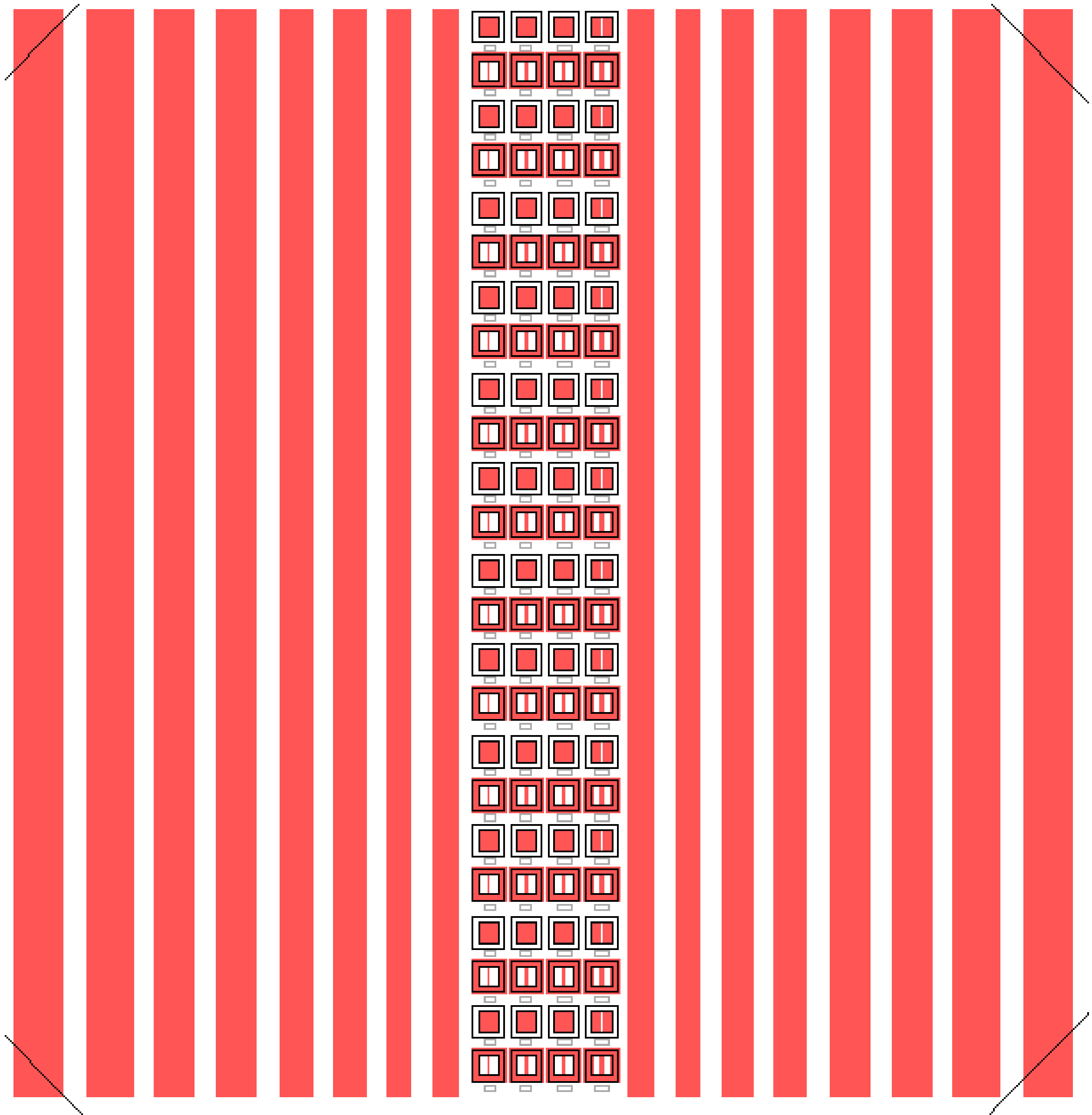


Figure B.18: IC Patterning and rectangles for ITO conductivity and patterning testing (WRLIC-TracesICPlates.tdb)

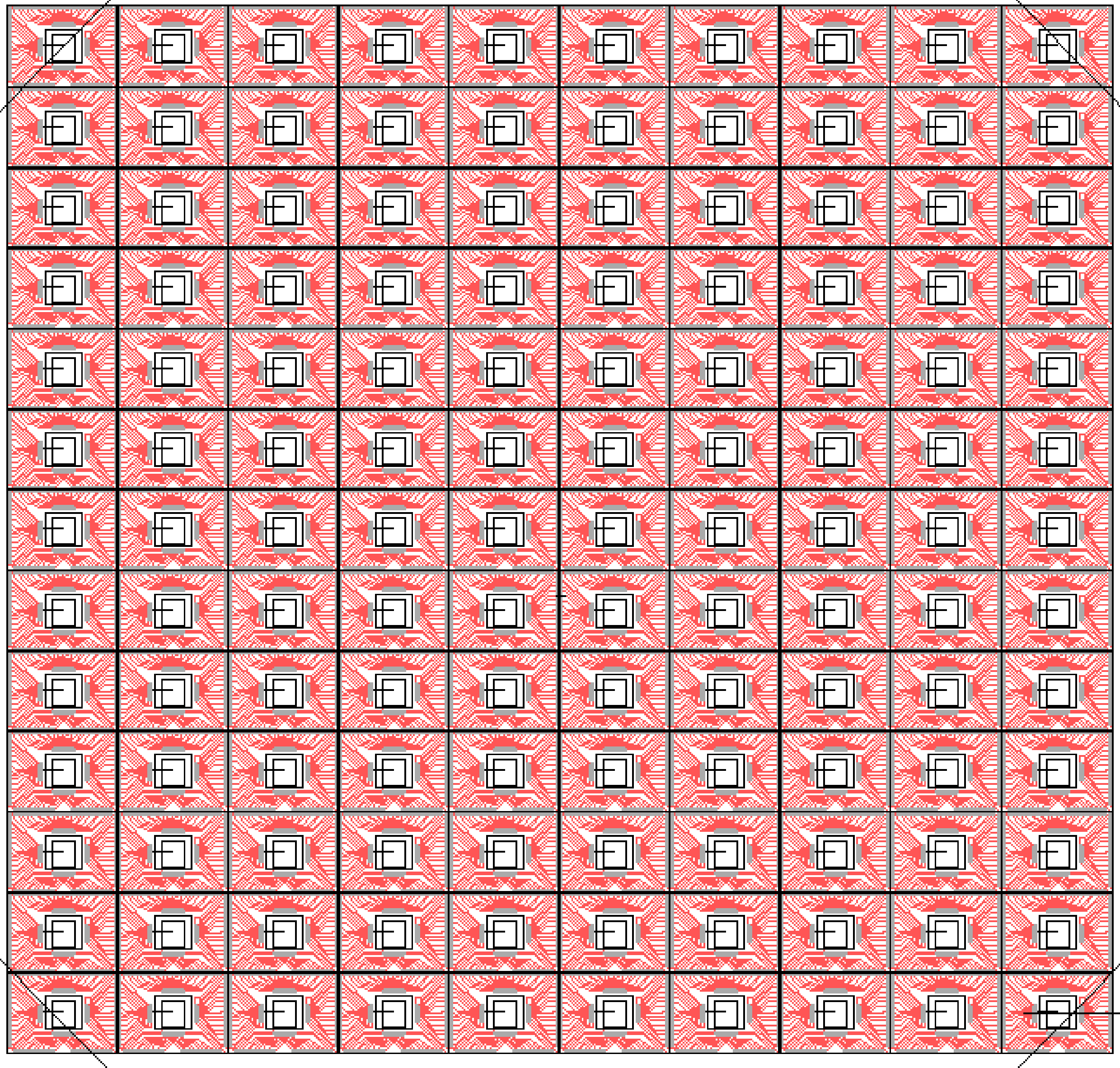


Figure B.19: IC Silicon Breakout Carrier v2 (Closer carriers). V1 is identical except with more separated carriers making them harder to dice (WRLICTracesICPlates.tdb)

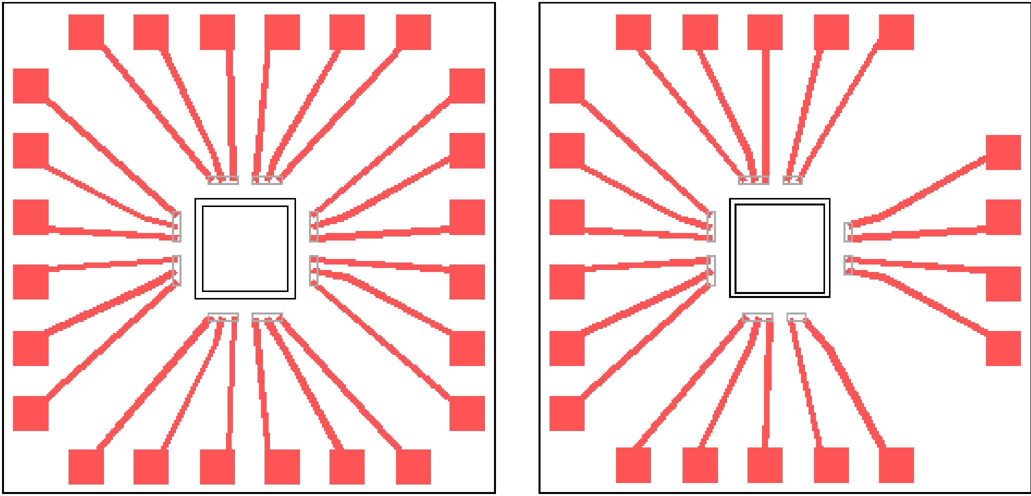


Figure B.20: Silicon Breakout Carrier for Glass MEMS Samples (WRLICTracesICPlates.tdb)

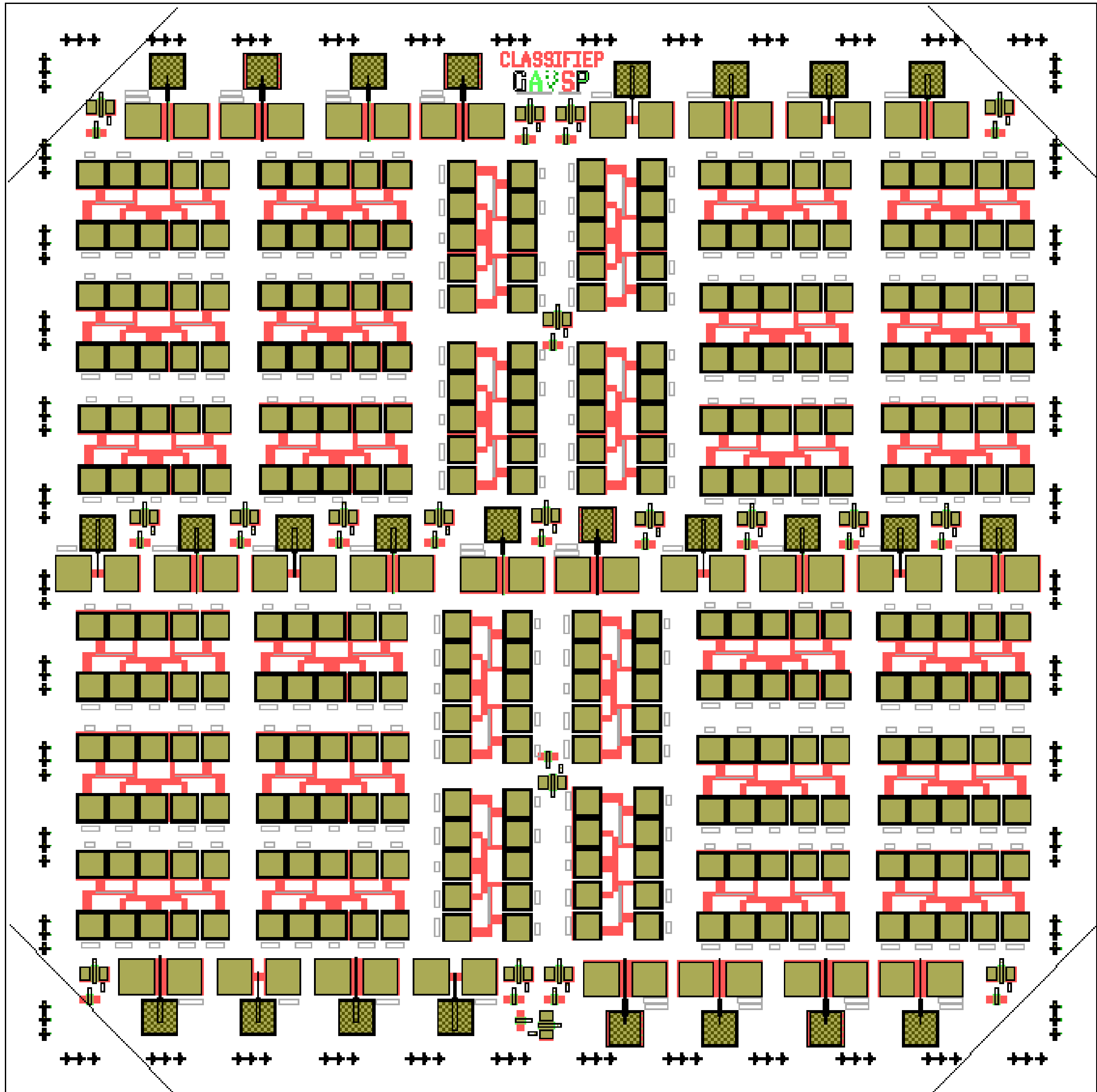


Figure B.21: TFT Classifiers (WRLTMClassifiers.tdb)

Mask Box 4:

Slot	Mask Set	Date	Layer
1			Via
2			S/D
3			Passivation
4	a-Si Photoconductor Array	4/2014	Active
5			S/D
6			Passivation
7			Connectors
8	Inductor mask 1		
9	Inductor mask 2		
10	Inductor mask 3		

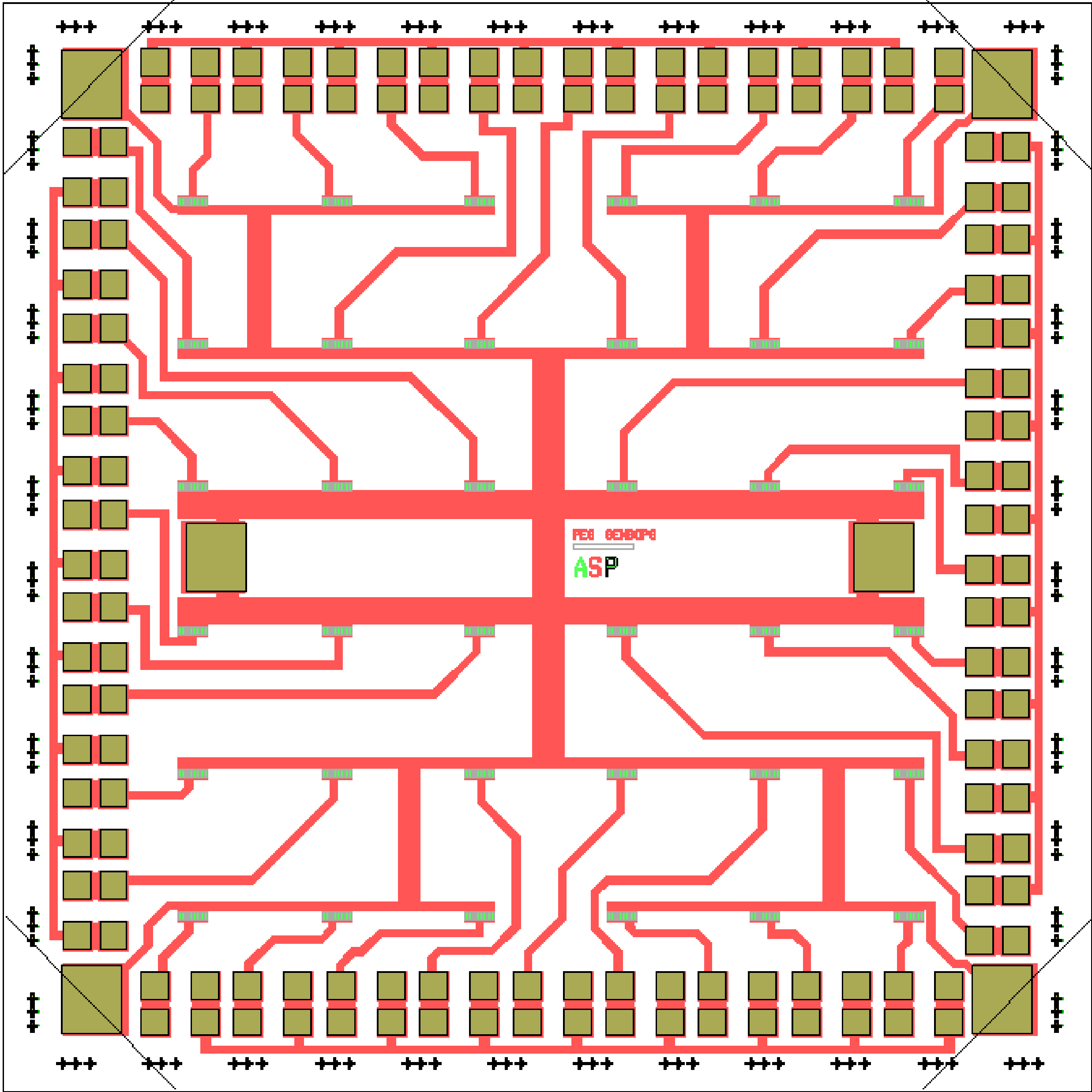


Figure B.22: a-Si 6x6 photoconductor array (WRLResistiveSensorArray.tdb)

5 Inch Masks:

In addition to the five stepper masks, the following are fabricated 5 inch masks

No.	Mask set	Date	Layer
1	Radio Circuits v2 connectors	8/2012	
2	Radio Plastic Carrier	8/2012	

Appendix C

Techniques for interfacing to Thin-Film Circuits

In this section, practical techniques for testing intermediate steps in the building of complete systems are described. A visual summary of these is shown in Figure C.1.

C.1 Soldering techniques

All circuits, on both glass and flexible substrates, are provided with many 2x2mm contact pads for external testing. We use a number of contact metal combinations for probing or for soldering pads. In amorphous silicon TFTs, the top metal for interconnect and pads is typically chrome, onto which additional layers of chrome and gold or chrome and platinum (usually 30nm and 250nm respectively) may be sputtered or evaporated. Both of these combinations allow for excellent electrical and mechanical connections using conventional lead solder, even at temperatures below 250 °C. Aluminium as a top metal cannot be soldered to.

Circuits with fewer than 10 connections usually can be tested in individual blocks, by directly connecting supplies and pattern generators. To test circuits and sensor arrays of medium complexity, it is often easiest to break out all connections to an external printed circuit board (PCB), using soldering as shown in Figures C.1 (b), followed by control and readout using data acquisition cards.

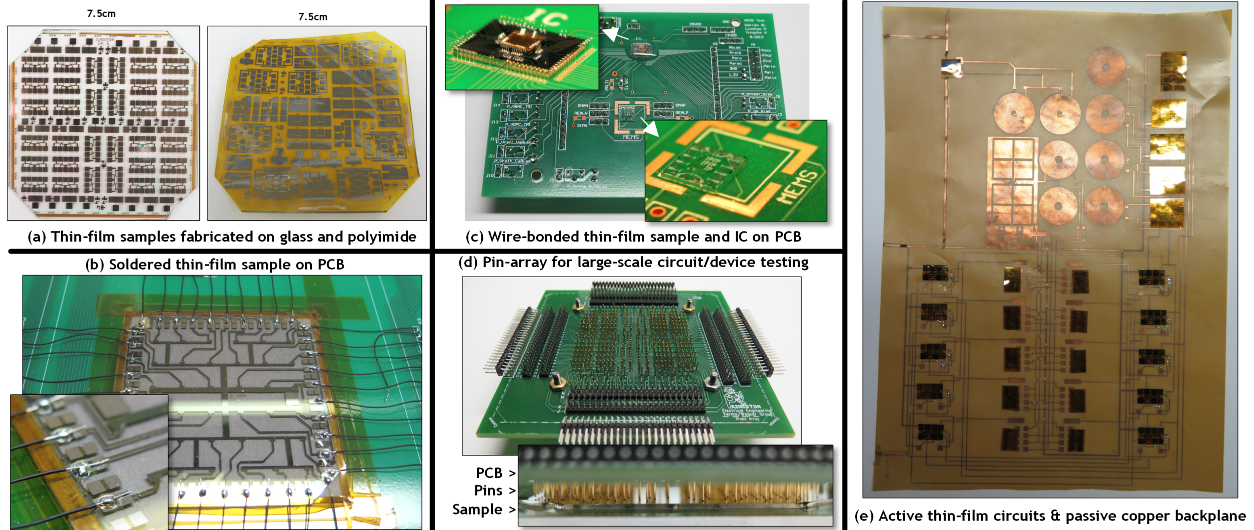


Figure C.1: Illustrative examples of provisions for practical system testing, leading up to integrated systems on flexible substrates; (a) a-Si or ZnO thin-film amplifier samples are fabricated on 7.5x7.5cm glass and polyimide substrates, using the same fabrication process for both substrates, at temperatures lower than 180C; (b) Gold or platinum-gold metallization allows the direct soldering of wires to the thin-film samples, in this case a light-sensing array; (c) For smaller-pitch contacts wire-bonding to a chrome or gold metallization layer is used to interface to a larger test board with exposed copper traces, pictured here is an a-Si MEMS sample on glass; (d) For circuits with a large number of connections a spring-loaded pin-array is used to break out headers on the edge of a printed circuit board; (e) represents a path to the integration described in this thesis with active circuits on polyimide bonded to a copper backplane using unidirectional conductive adhesive Pictured is a strain sensing sheet that integrates sensors, access control circuits, modulators and demodulators, all in thin-film technology.

C.2 Wire-bonding

Figure C.1 (c) shows how wire-bonding can also be used to break out, from both glass samples and from integrated circuits, onto a PCB; the integrated circuit is supported on an **oxidized** silicon wafer carrier, to fan out the tight pitches of the IC to a more appropriate PCB spacing. Ideally the PCB is manufactured with exposed copper lines, which must be gently scratched prior to bonding to remove surface oxides. Pads smaller than 100 microns become challenging to wirebond, and appropriate metals for the top bonding surface are aluminium or platinum.

For bonding the following parameters on the wirebonder in Jadwin are useful starting points:

- Chrome pad to a copper PCB off a 1mm thick glass substrate: Loop Height (LH)=220 to 300, RVL=170, RVH=170

- CMOS IC pad to silicon carrier: Loop Height (LH)=190, RVL=70, RVH=200

C.3 Pin-Array

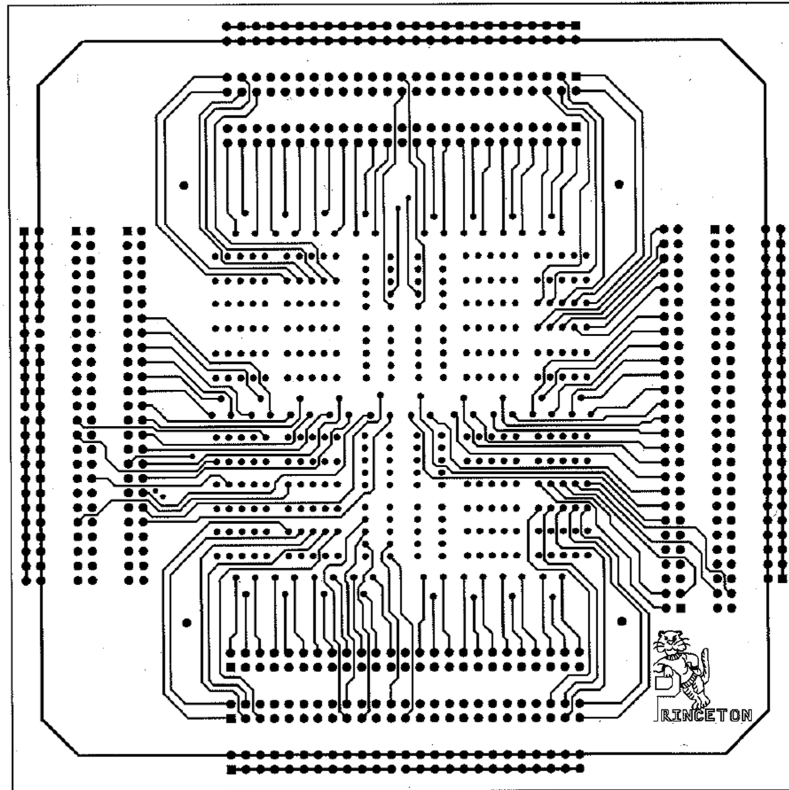
Figure C.1 (d) highlights the next level of integration experiments. We have developed a pin array that enables testing of all devices and circuits of a sample. This array consists of 400 spring loaded pins [74] soldered through-hole on a printed circuit board. These are distributed over a 7.5x7.5cm area in a predetermined pattern, which matches the pattern on the substrate with thin-film circuits, and routed to external headers. The pins are manually compressed onto the substrate through the use of the four pictured screws/nuts. When interfaced with external data acquisition boards, the pin array subsequently allows us to programmatically test and interconnect a large number of working circuits and devices, to then integrate several functions. With this setup, we have demonstrated circuits with simultaneous operation of over 250 TFTs on glass.

The pin-array PCB consists of a 4-layer PCB of dimensions 5.4inx5.4in. PCB layer maps are shown in Figures C.2 and C.3. The pin array base dimensions are shown in Figure C.5.

The pin mappings are arising from these PCB layers are shown in Figure C.4.

Thanks to Bert Harrop for assistance in developing this interface technique.

TOP LAYER



INNER LAYER 1

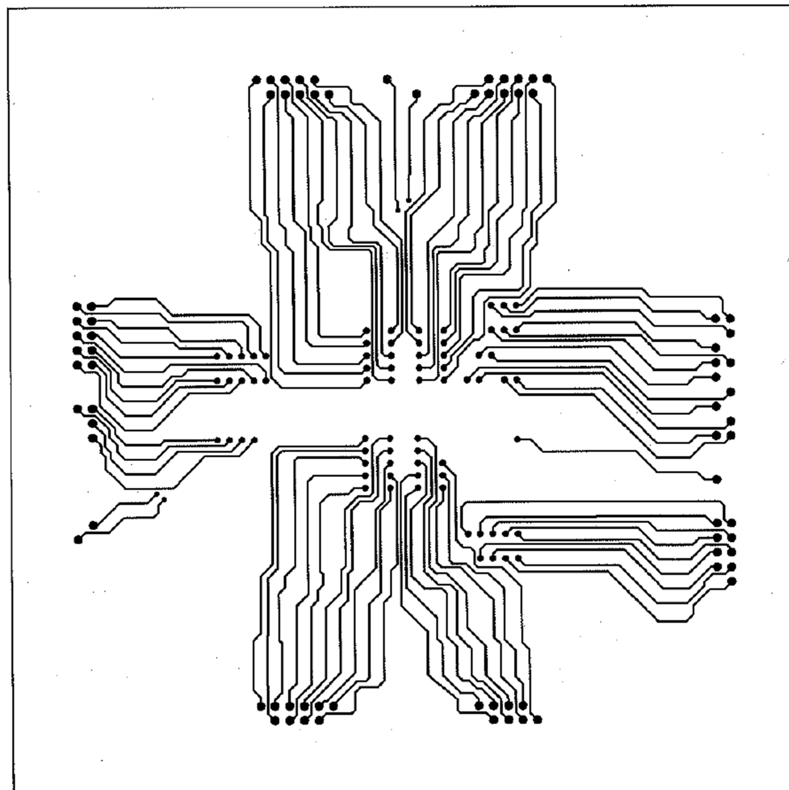
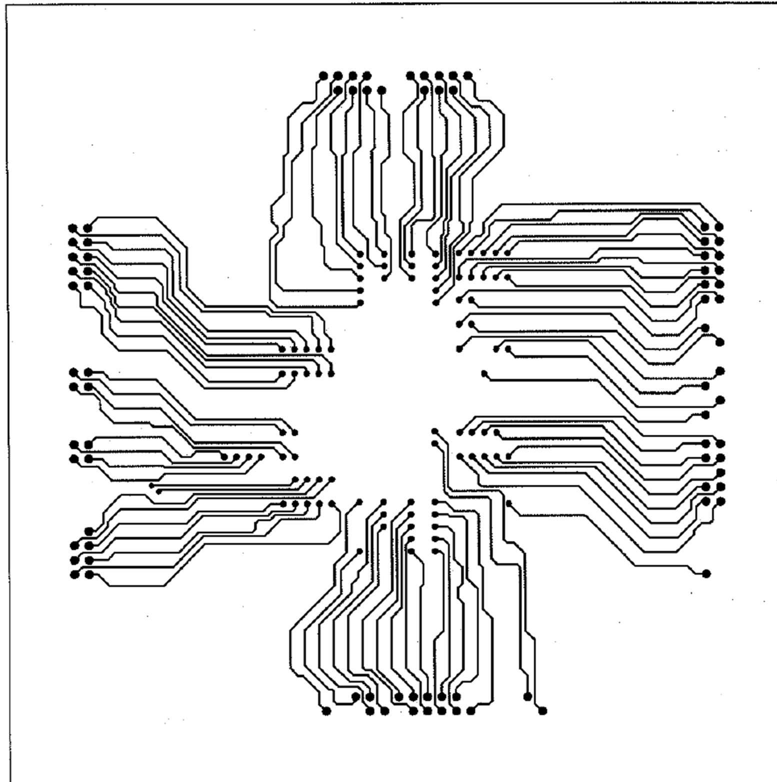


Figure C.2: Pin array PCB Top and Inner Layer 1



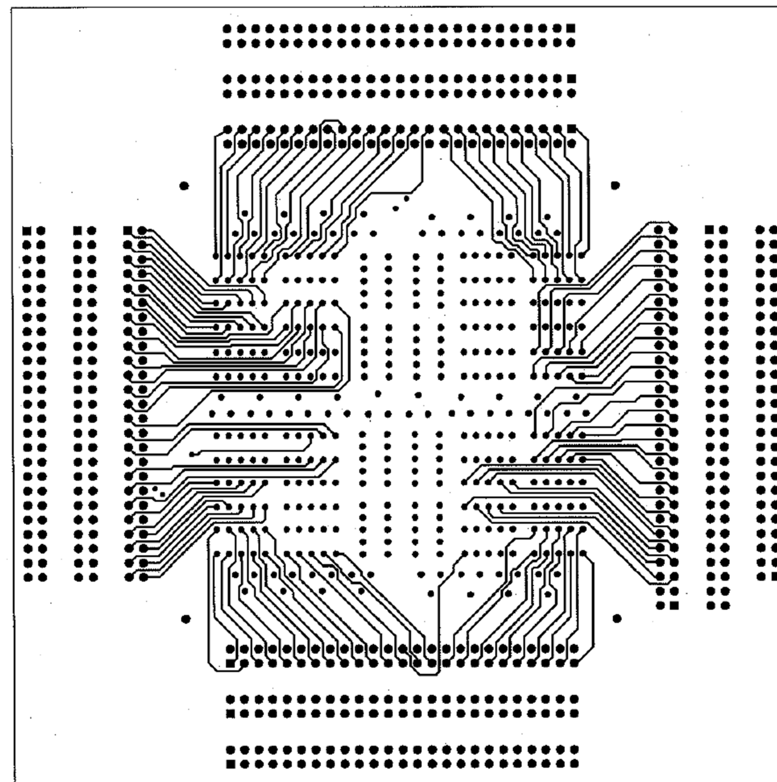


Figure C.3: Pin array PCB Inner Layer 2 and Bottom Layer

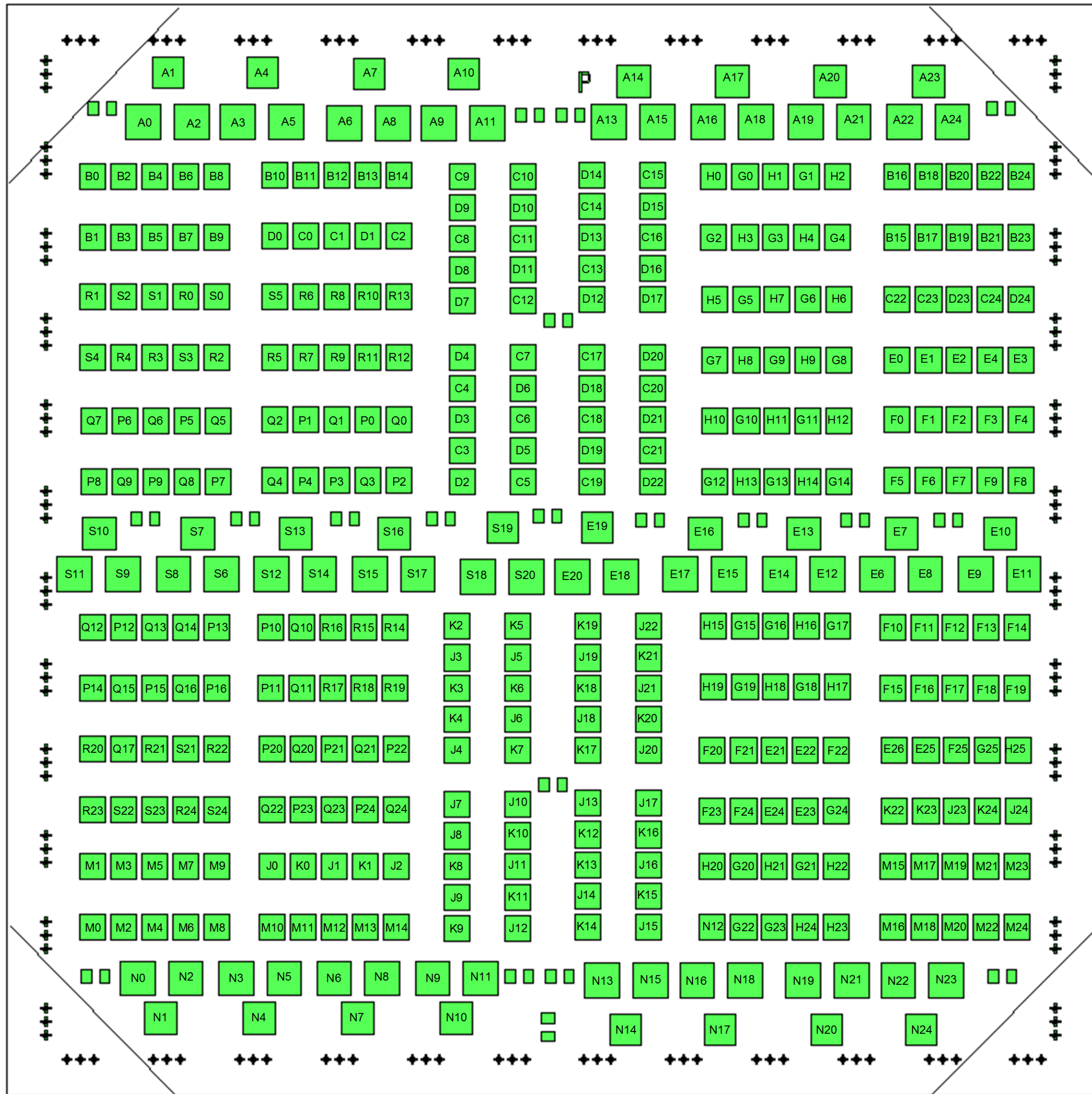


Figure C.4: Pin array mapping to outer connectors

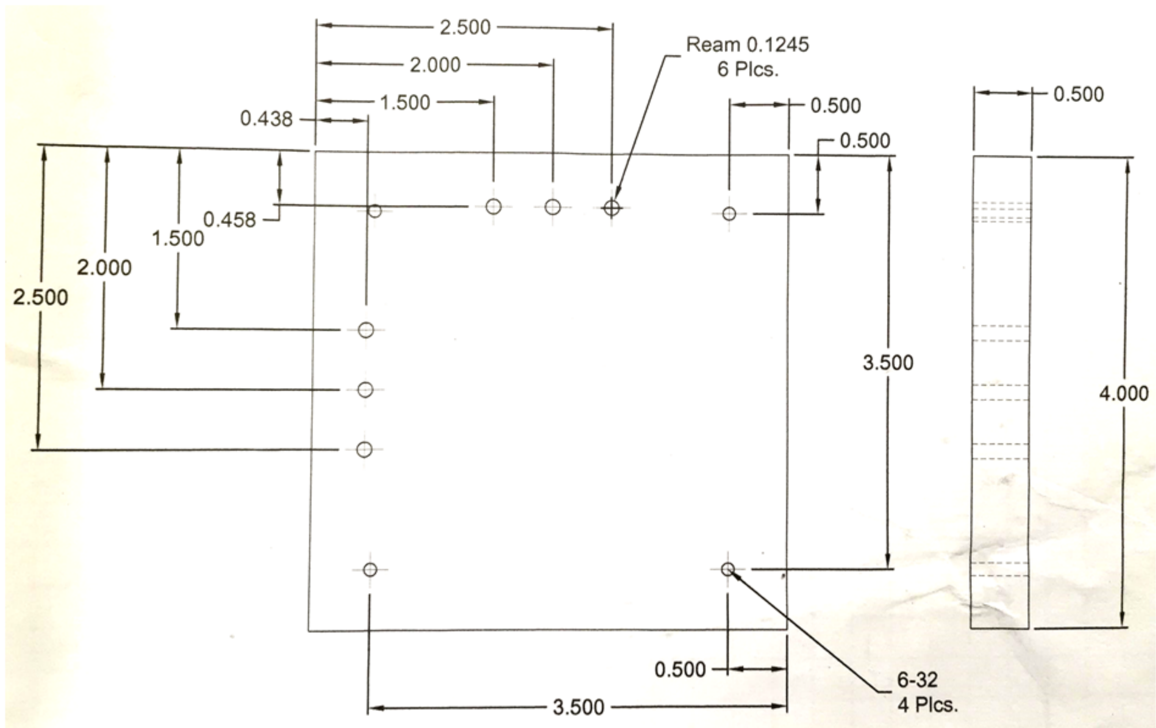


Figure C.5: Pin array mapping to outer connectors

C.4 Integration on flex

Figure C.1 (e) illustrates integration with a passive backplane. Working circuits on plastic are identified and laminated onto a passive copper backplane, which is patterned with conductors and inductors/capacitors, to form a working system. Connection to the active circuits is typically achieved using the unidirectional conductive adhesive tape, 3M 9703 Z-axis conductive adhesive, which provides a contact resistance of less than $0.03\,\Omega\,\mathrm{cm}^2$. For the testing of the individual circuit blocks, connectors can be manufactured on polyimide through the patterning of deposited low resistance Chrome/Gold (50nm/300nm). The resistivity of the connector lines is on the order of $25\,\mathrm{n}\Omega\,\mathrm{m}$; for a typical line of dimension 4.5cm by $600\,\mu\mathrm{m}$, this translates into a resistance of approximately 6 ohms. The connector patterns are designed to match the pad layouts on the thin-film sample and can be mated on one end to the flex circuits using the conductive tape and on the other to flat alligator clips; these have proven a very useful method for testing. A typical mask layout and test setup is shown in Figure C.6.

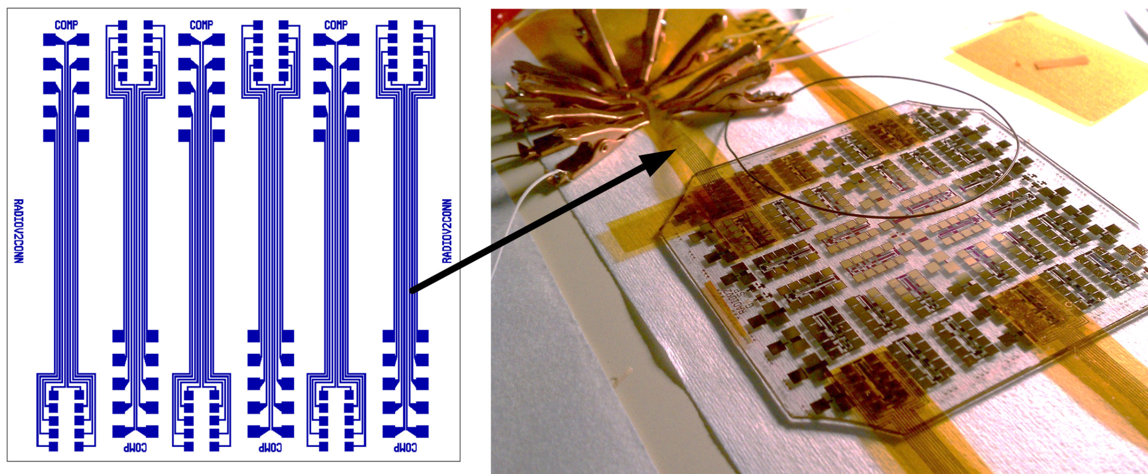


Figure C.6: Patterned connectors on polyimide

C.5 MATLAB code for interfacing using DAQ systems

The code sample below illustrates how to interface to a thin-film sample using a MCC DAQ card system in MATLAB, showing both output and input of data (1608G and 3105). This uses the

legacy interface which only works using 32 bit Matlab. The legacy interface tends to crash for large acquired datasets:

```
function [ yy ,samppersamp] = SensorOutput(sensorout,numtrainsample)
% function to output from two DAQ cards (one with 16 channels, one with 13 channels
%and read data in from two channels
%Sample data inputted is in sensorout and consists of 30 columns of data
%with numtrainsample instances for each column i.e. a numtrainsample x 30
%matrix

numsensors=size(sensorout,2);

%get analog output object with settings (number is board number from Instacal)
ao=analogoutput('mcc',5);
%add 16 channels to output, x:y is channel number
chan=addchannel(ao,0:15);
%set sample rate in samples per second per channel
aosamp=6;
set(ao,'SampleRate',aosamp);
%repeat buffer x number of times in a row (repeats waveform)
set(ao,'RepeatOutput',0);
%Put this line here so that sensor outputs only start when Trigger function
%used later
set(ao,'TriggerType','Manual');

%get analog output object with settings (number is board number from Instacal)
ao2=analogoutput('mcc',6);
%add 6 channels to output, x:y is channel number
chan=addchannel(ao2,0:12);
%set sample rate in samples per second per channel
```

```
aosamp=6;
set(ao2,'SampleRate',aosamp);
%repeat buffer x number of times in a row (repeats waveform)
set(ao2,'RepeatOutput',0);
%Put this line here so that sensor outputs only start when Trigger function
%used later
set(ao2,'TriggerType','Manual');

%add analog input in channel object. Samples for 1 second at 1000Hz
ai=analoginput('mcc',1);
ch=addchannel(ai,0:1);
%set sample rate (so we get 50 samples per output)
samples=aosamp*50;
%set the number of samples to read
set(ai,'SampleRate',samples);
count =(numtrainsample*samples/aosamp)+samples;
ai.SamplesPerTrigger = count;
%And the trigger method
set(ai,'TriggerType','Manual');

%compute samples per sampple
samppersamp=samples/aosamp;

%put data to transmit on the output buffers (one column per channel, with
%Numtrainsample instances per column)
putdata(ao,sensorout(:,1:16));
putdata(ao2,sensorout(:,17:29));
%start the output DAQs and the input DAQ
start([ao,ao2]);
start(ai);
```

```
%Trigger the start of the output sequences
trigger([ao,ao2,ai]);
% Read in the acquired data once it is collected
yy=getdata(ai);

% Clear the buffers in the input/output devices, stop the DAQs and delete
% the DAQ objects
flushdata(ai);
stop([ai,ao,ao2]);
delete([ai,ao,ao2]);
clear ai ao ao2;

end
```

The code sample below illustrates how to interface to a thin-film sample using a PCI-6229 DAQ card system in MATLAB, showing both output and input of data. NI DAQ Mx must be installed, and the DAQ may need to be registered once by running MATLAB in Administrator mode and running daqregister('nidaq'). This uses the session-based interface:

```
s = daq.createSession('ni');
%
% s.DurationInSeconds = 17; % session duration
samplerate=10000;
s.Rate =samplerate; %# samples per second;

%Add ANALOG OUTPUT CHANNEL 1-4
addAnalogOutputChannel(s,'Dev1',0:3,'Voltage'); %output channels are default single ended

% %'Dev1' is the name of the NI DAQ (daq.getDevices can be used to find the name of the DAQ)
% % Add ANALOG INPUT CHANNEL 1
ch = addAnalogInputChannel(s,'Dev1',0,'Voltage');
```

```
ch.InputType = 'SingleEnded'; %want to have single ended inputs
ch.Range = [-5,5]; % can set voltage range from -1 to +1; -5 to +5, -10 to +10

% % Add ANALOG INPUT CHANNEL 2
% ch = addAnalogInputChannel(s,'Dev1',1,'Voltage');
% ch.InputType = 'SingleEnded'; %want to have single ended inputs
% ch.Range = [-5,5]; % can set voltage range from -1 to +1; -5 to +5, -10 to +10
%
% % Add ANALOG INPUT CHANNEL 3
% ch = addAnalogInputChannel(s,'Dev1',2,'Voltage');
% ch.InputType = 'SingleEnded'; %want to have single ended inputs
% ch.Range = [-5,5]; % can set voltage range from -1 to +1; -5 to +5, -10 to +10
%
% % Add ANALOG INPUT CHANNEL 4
% ch = addAnalogInputChannel(s,'Dev1',3,'Voltage');
% ch.InputType = 'SingleEnded'; %want to have single ended inputs
% ch.Range = [-5,5]; % can set voltage range from -1 to +1; -5 to +5, -10 to +10

%Create data for a sine wave
output_data = 5*sin(linspace(0,2*pi,2000)');

%output_data is a matrix with one column per channel
output_data= [output_data,output_data,output_data,output_data];

%Queue the data, output it and record it in the variable captured.
%Time information is kept in the time variable
queueOutputData(s,output_data);
[captured,time]=startForeground(s);
```

The following code snippet shows how to control the Agilent power supplies directly from MATLAB to further automate system testing. The Instrument Control Toolbox is used and the driver ‘AgilentE3647ivi.mdd’ can be downloaded from the MATLAB website. The power supply is connected using a USB to COM cable (e.g. USB Serial Converter manufactured by plugable).

```
% Create a device object.
deviceObj = icdevice('AgilentE3647ivi.mdd', 'COM3');
% Connect device object to hardware.
connect(deviceObj);

% Query property value(s).
get1 = get(deviceObj, 'InstrumentModel')

%Set output voltage
set(deviceObj.Output(2), 'VoltageLevel', 20);

% Resets device (outputs off).
groupObj = get(deviceObj, 'Utility');
groupObj = groupObj(1);
invoke(groupObj, 'Reset');

% Disconnect device
disconnect(deviceObj);
```

Appendix D

Creating TFT simulation models

This section contains an intuitive manual for the fitting of SPICE models using the Level 15/61 SPICE model.

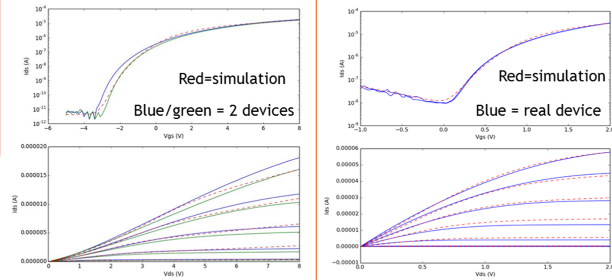
An intuitive guide to manual fitting with the Level 15/61 SPICE TFT model

Warren Rieutort-Louis, May 2014

Aim

Create models for simulation of *ft* and circuits

Level 15 (AIM Spice) and the corresponding, identical, Level 61 model (Cadence) can be used to fit to a wide variety of devices



The Level 15/61 model

This (originally a-Si) TFT model has a number of parameters shown below to define a model:

Model name · **MOSFET type (pmos *or* nmos)** · **Level number (15 for AIM-SPICE, 61 for Cadence/Spectre)**

Model parameters:

```
.model ModTFTDNTT pmos (level=15
+ ALPHASAT=0.4, CGSO=8.9E-10, CGDO=8.9E-10
+ DEFO=0.5, DELTA=0.5, EL=0.7, EMU=0.06
+ EPS=10, EPSI=3.5, GAMMA=0.1, GMIN=2E+023
+ IOL=1E-012, KASAT=0.006, KVT=-0.036, LAMBDA=0.26
+ M=6, MUBAND=0.00001, RD=100000, RS=100000
+ SIGMAO=5E-013, TNOM=27, TOX=90e-9, V0=0.11
+ VAA=75000, VDSL=7, VFB=-4.5, VGSL=-2, VMIN=0.3
+ VTO=-3)
```

Brackets optional in Cadence/Spectre

Including the model

AIM-Spice (Student Version) - [C:\Users\Warren\Deskt
File Edit Search View Format Options Analysis Postp

```
TFT simulation

vd d 0 dc -2.1
vg g 0 dc
m1 d g 0 0 ModTFTDNTT w=1000u l=40u


.model ModTFTDNTT pmos (level=15
+ ALPHASAT=0.4
+ CGSO=5.16E-09
+ CGDO=5.16E-09
+ DEFO=0.8
+ DELTA=0.05
+ EL=0.7
+ EMU=0.03
+ EPS=11
+ EPSI=3.5
+ GAMMA=0.1
+ GMIN=1E+023
+ IOL=1E-08
+ KASAT=0.006
+ KVT=-0.036
+ LAMBDA=0.01
+ M=3.1
+ MUBAND=0.000138
+ RD=500
+ RS=500
+ SIGMAO=2E-013
+ TNOM=27
+ TOX=3.9e-9
+ V0=0.099
+ VAA=7500
+ VDSL=3
+ VFB=-0.5
+ VGSL=0.6
+ VMIN=0.3
+ VTO=-0.6)
```

In AIM-SPICE, simply include the model at the bottom of the simulation file, declaring transistor width and lengths as shown

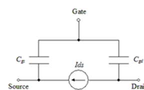
In Cadence/Spectre, place the model in a *.m file, then include that file in the ADE model libraries menu

Formal parameter descriptions

From AIM Spice reference

Amorphous-Si TFT Model ASIA2 (Level 15) Previous Top Next

Name	Parameter	Units	Default
ALPHASAT	Saturation modulation parameter	-	0.6
CGDO	Gate-drain overlap capacitance per meter channel width	F/m	0.0
CGSO	Gate-source overlap capacitance per meter channel width	F/m	0.0
DEF0	Dark Fermi level position	eV	0.6
DELTA	Transition width parameter	-	5
EL	Activation energy of the hole leakage current	eV	0.35
EMU	Field effect mobility activation energy	eV	0.06
EPS	Relative dielectric constant of substrate	-	11
EPSI	Relative dielectric constant of gate insulator	-	7.4
GAMMA	Power law mobility parameter	-	0.4
GMIN	Minimum density of deep states	$m^{-3}eV^{-1}$	1E23
IOL	Zero bias leakage current	A	3E-14
KASAT	Temperature coefficient of ALPHASAT	1/°C	0.006
KVT	Threshold voltage temperature coefficient	V/°C	-0.036
LAMBDA	Output conductance parameter	1/V	0.0008
M	Knee shape parameter	-	2.5
MUBAND	Conduction band mobility	m^2 / Vs	0.001
RD	Drain resistance	Ω	0.0
RS	Source resistance	Ω	0.0
SIGMA0	Minimum leakage current parameter	A	1E-14
TNOM	Parameter measurement temperature	°C	27
TOX	Thin-oxide thickness	m	1.0e-7
V0	Characteristic voltage for deep states	V	0.12
VAA	Characteristic voltage for field effect mobility (determined by tail states)	V	7.5E3
VDSL	Hole leakage current drain voltage parameter	V	7
VFB	Flat band voltage	V	-3
VGSL	Hole leakage current gate voltage parameter	V	7
VMIN	Convergence parameter	V	0.3
VTO	Zero-bias threshold voltage	V	0.0



First steps to fitting model

As first steps:

1. Firstly declare a basic Level 15/61 model and a basic MOSFET circuit with two DC voltage sources, one at the drain, one at the gate.
2. Set the Width and Length of the TFT you are trying to model to in the appropriate location
3. In the model, set the appropriate semiconductor relative permittivity (*EPS*) and gate dielectric relative permittivity (*EPSI*)
4. Set the gate dielectric thickness in *TOX*
5. Set the nominal temperature *TNOM* to 27
6. Set the band mobility parameter *MUBAND* to a value close to the expected conduction band mobility in your material (e.g. 0.001 in a-Si)- note band mobility and field effect mobility are not the same for all material systems!
7. Start with low /RD/RS of 0-a few hundred ohms.
8. *Set all the other parameters to their default value in the previous slide*

General procedure

The following procedure is often the easiest for fitting:

1. Fit the log(Ids)-Vgs *at one Vds value* first
2. Observe the fitting to the Ids-Vds curve for different Vgs
3. Make corrections to fit to the Ids-Vds curve
4. Verify that corrections did not affect the log(Ids)-Vgs fit

It is much easier to focus on one curve at a time when fitting rather than trying to fit everything at once.

The remainder of this document is meant as a intuition-driven guide to fitting a model, rather than focusing on the (complex) equation system of the Level 15/61 model system. The numerical examples and plots shown are for PMOS devices (x-axis flipped), but the principles are identical for NMOS devices.

Ignore these parameters

For a basic Id/Vgs fit, ignore the following parameters which basically impart temperature dependence to the model:

Name	Parameter	Units	Default
ALPHASAT	Saturation modulation parameter	-	0.6
CGDO	Gate-drain overlap capacitance per meter channel width	F/m	0.0
CGSO	Gate-source overlap capacitance per meter channel width	F/m	0.0
DEF0	Dark Fermi level position	eV	0.6
DELTA	Transition width parameter	-	5
EL	Activation energy of the hole leakage current	eV	0.35
EMU	Field effect mobility activation energy	eV	0.06
EPS	Relative dielectric constant of substrate	-	11
EPSI	Relative dielectric constant of gate insulator	-	7.4
GAMMA	Power law mobility parameter	-	0.4
GMIN	Minimum density of deep states	$m^{-3}eV^{-1}$	1E23
IOL	Zero bias leakage current	A	3E-14
KASAT	Temperature coefficient of ALPHASAT	1/°C	0.006
KVT	Threshold voltage temperature coefficient	V/°C	-0.036
LAMBDA	Output conductance parameter	1/V	0.0008
M	Knee shape parameter	-	2.5
MUBAND	Conduction band mobility	m^2 / Vs	0.001
RD	Drain resistance	Ω	0.0
RS	Source resistance	Ω	0.0
SIGMA0	Minimum leakage current parameter	A	1E-14
TNOM	Parameter measurement temperature	°C	27
TOX	Thin-oxide thickness	m	1.0e-7
V0	Characteristic voltage for deep states	V	0.12
VAA	Characteristic voltage for field effect mobility (determined by tail states)	V	7.5E3
VDSL	Hole leakage current drain voltage parameter	V	7
VFB	Flat band voltage	V	-3
VGSL	Hole leakage current gate voltage parameter	V	7
VMIN	Convergence parameter	V	0.3
VTO	Zero-bias threshold voltage	V	0.0

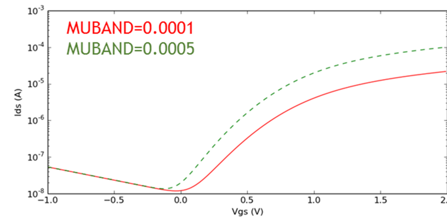
Not a temp. dependent parameter but in general it is also possible to fit ignoring VMIN

Not a very useful parameter in fitting, generally leave at 7.5E3

Fitting Id-Vgs → Subthreshold and On-state

Effect of MUBAND

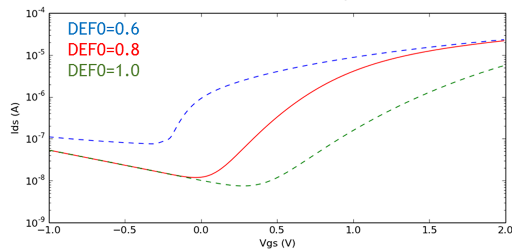
MUBAND is the *band* mobility- closely related to the FET mobility although it may not be equal to it e.g. in a-Si, band mobility is typ. ~10x FET mobility



When to change	Change MUBAND when Ids is overall too low or too high in sub-Vt and 'on state'. This is almost a direct vertical translation but does not affect leakage in off-state.
Change by	Once in the right ballpark, by small steps of e.g. 0.00005

Effect of DEF0

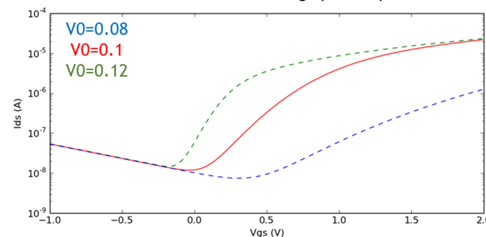
DEF0 is the *dark Fermi level* position.



When to change	DEF0 has dramatic impact on the overall shape of Id-Vgs. Decreasing DEF0 principally increases the subthreshold slope (and hence also affects apparent Vt). See also V0.
Change by	Very small amounts, try 0.05 steps at a time, starting around 0.6-0.7

Effect of V0

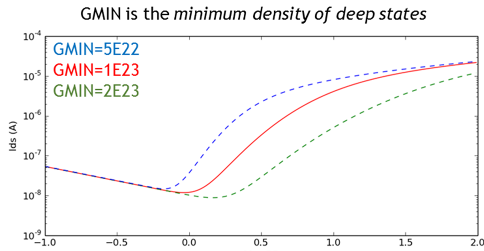
V0 is the *characteristic voltage for deep states*



When to change	Much like DEF0, V0 also has dramatic impact on the subthreshold slope. It is not obvious which one it is best to change.
Change by	Very small amounts, try 0.01 steps at a time, starting around 0.1

Effect of GMIN

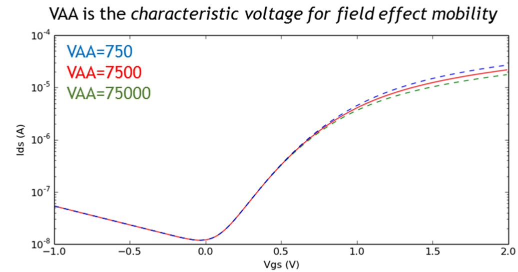
GMIN is the *minimum density of deep states*



When to change	GMIN has an impact similar to V0 (unsurprising since one determines distribution the other determines the *number* of deep states). Whilst GMIN will affect the minimum leakage, it is easier to control this with IOL/SIGMA0, decoupling the leakage from the on-state.
Change by	Change by factors of x2 around 1E23. In general though, I have found that keeping GMIN at 1E23 and changing V0 is usually more effective.

Effect of VAA

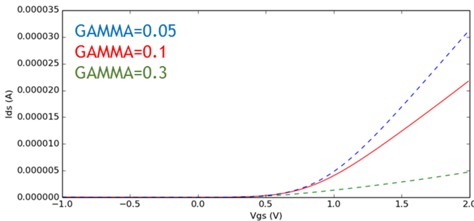
VAA is the *characteristic voltage for field effect mobility*



When to change	When a minor correction to the slope at high gate voltages is required.
Change by	Very significantly (see graph) to observe any difference

Effect of GAMMA

GAMMA is the *power law mobility parameter* which determines how number of carriers (i.e. current) changes as a function of Vgs above threshold



When to change	When the above-VT Ids-Vgs relationship does not follow the correct power relationship
Change by	Very slightly (0.05-0.1)

Fitting Id-Vgs (continued) → Threshold Voltage

Threshold Voltage

Setting the turn on and threshold voltage is not a simple affair since it depends on a lot of parameters.

The minimum Ids point can in practice be set by the intersection of the sub-threshold slope (controlled by V0/DEF0/GMIN) and the leakage characteristics (IOL, SIGMA0 etc. (see later)), but its position can also be shifted by V0 and VFB.

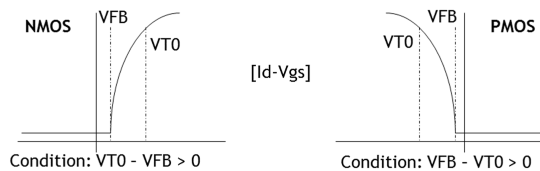
Two parameters, VT0 and VFB define the effective 'threshold voltage'.

VT0 characterizes the charge contribution by gate voltage to the channel when above threshold

VFB characterizes the charge contribution when below threshold, and close relates to an effective 'turn-on' voltage

Threshold Voltage

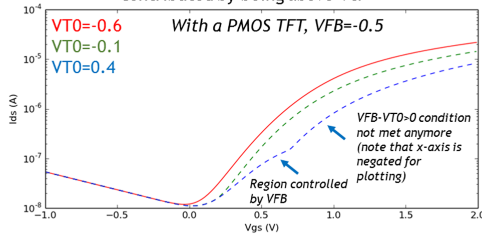
When considering the actual values of VT and VFB (not magnitude), the following must be met



Practically speaking, I keep VFB/VT0 close together (with a few 100mVs), satisfying the above conditions

Effect of VT0

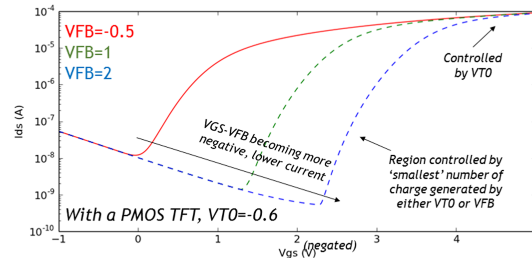
VT0 is defined as the *zero-bias threshold voltage* and dictates charge contributed by being above Vt.



When to change	Shifting VT0 shifts the 'on-state characteristic'. Note that it does this independently from the sub-vt characteristic set by VFB whose contribution rolls-off, so at some point a discontinuity starts to appear.
Change by	Proportionally to desired voltage shift, typ. 100s of mV

Effect of VFB

VFB is defined as the *flat band voltage* and is used to calculate charge contributed by voltage *above* the flatband voltage



When to change	VFB controls horizontal shift in the exponential region
Change by	Proportionally to desired voltage shift, typ. 100s of mV

Fitting Id-Vgs (continued) → Leakage Current

Modelling Leakage

The parameters determining the leakage current are the following:

Name	Parameter	Units	Default
ALPHASAT	Saturation modulation parameter	-	0.6
CGDO	Gate-drain overlap capacitance per meter channel width	F/m	0.0
CGSO	Gate-source overlap capacitance per meter channel width	F/m	0.0
DEF0	Dark Fermi level position	eV	0.6
DELTA	Transition width parameter	-	5
EL	Activation energy of the hole leakage current	eV	0.35
EMU	Field effect mobility activation energy	eV	0.06
EPS	Relative dielectric constant of substrate	-	11
EPSI	Relative dielectric constant of gate insulator	-	7.4
GAMMA	Power law mobility parameter	-	0.4
GMIN	Minimum density of deep states	$m^{-3}eV^{-1}$	1E23
IOL	Zero bias leakage current	A	3E-14
KASAT	Temperature coefficient of ALPHASAT	1/°C	0.006
KVT	Threshold voltage temperature coefficient	V/°C	-0.036
LAMBDA	Output conductance parameter	1/V	0.0008
M	Knee shape parameter	-	2.5
MUBAND	Conduction band mobility	m^2 / Vs	0.001
RD	Drain resistance	Ω	0.0
RS	Source resistance	Ω	0.0
SIGMA0	Minimum leakage current parameter	A	1E-14
TNOM	Parameter measurement temperature	°C	27
TOX	Thin-oxide thickness	m	1.0e-7
V0	Characteristic voltage for deep states	V	0.12
VAA	Characteristic voltage for field effect mobility (determined by tail states)	V	7.5E3
VDSL	Hole leakage current drain voltage parameter	V	7
VFB	Flat band voltage	V	-3
VGSL	Hole leakage current gate voltage parameter	V	7
VMIN	Convergence parameter	V	0.3
VTO	Zero-bias threshold voltage	V	0.0

Modelling Leakage

The leakage equations for the Level 15 model are some of the few that are actually 'easy' to understand.

$$I_{leakage} = I_{hl} + I_{\min}$$

$$I_{hl} = \mathrm{IOL}\left[\exp\left(\frac{V_{ds}}{\mathrm{VDSL}}\right) - 1\right]\exp\left(-\frac{V_{gs}}{\mathrm{VGSL}}\right)\exp\left[\frac{\mathrm{EL}}{q}\left(\frac{1}{V_{tho}} - \frac{1}{V_{th}}\right)\right]$$

Constant (IOL) — Vds dependence (exponential) — Vgs dependence — Temperature dependence

Note: I never change EL

$$I_{\min} = \mathrm{SIGMA0} \cdot V_{ds}$$

Vds dependence *(linear)*

You can fit to either a linear or exponential Vds dependence.

Modelling Leakage

Some common cases:

Vgs dependence:

Case (1):
Leakage current is independent of Vgs → Make VGSL very large in magnitude (PMOS = +ve, NMOS=-ve)

Case (2):
Leakage current is dependent on Vgs → Make VGSL comparable to turn on voltage, and make IOL close to the minimum leakage value

Vds dependence:

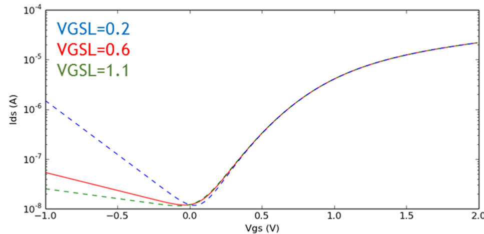
Case (1):
Leakage current is exponentially related to Vds → Make VDSL comparable to turn on voltage, IOL close to min. leakage value, SIGMA0 very small

Case (2):
Leakage current is linearly dependent to Vds → Make VDSL very large, SIGMA0 comparable to IOL.

Practically speaking, I rarely model to Vds, and make SIGMA0 small and VDSL large.

Effect of VGSL

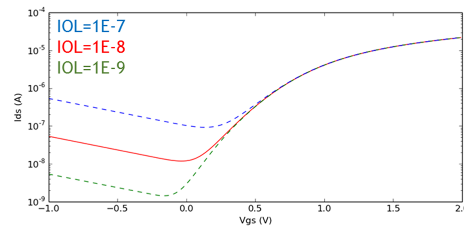
In an example where Ids is exponentially dependent on Vgs



When to change	VGSL controls the slope of the leakage current
Change by	Small amounts- this is an exponential relationship- smaller VGSL = steeper slope. Control the minimum by IOL.

Effect of IOL

In an example where Ids is exponentially dependent on Vgs

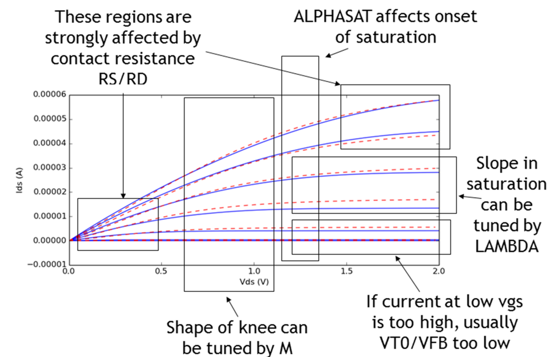


When to change	IOL controls the minimum leakage current. Note that due to the piecewise assembly of the model, the leakage current does not shift the minimum vertically, but instead an apparent turn on voltage shift is also seen. Correct for this with V0/DEF0 and VFB/VT0 as required.
Change by	Usually orders of magnitude to get in the right range, then smaller.

Fitting Id-Vds

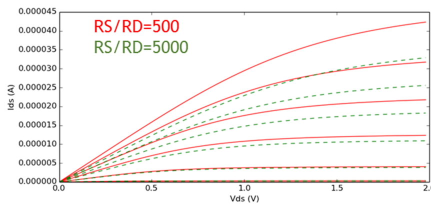
With a relatively close fit for Id-Vgs (need not be perfect), we switch to modelling Id-Vds. In general, the fit we have done for Id-Vgs will work well for one of the output curves, but not quite for the others.

Modelling Id-Vds: some hints



Effect of RS/RD

RS and RD are source/drain contact resistances

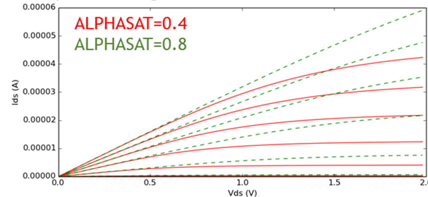


Be *very* wary of fitting current using RS/RD (prefer e.g. MUBAND) unless you have good reason to believe this is necessary. It is very easy to overfit with RS/RD to explain low currents only to find later that current does not scale appropriately with e.g. channel length

When to change	- When the spread at low VDS is too large - When the current at high VGS AND VDS is too high but not at low VGS
Change by	Usually orders of magnitude to get in the right range, then smaller.

Effect of ALPHASAT

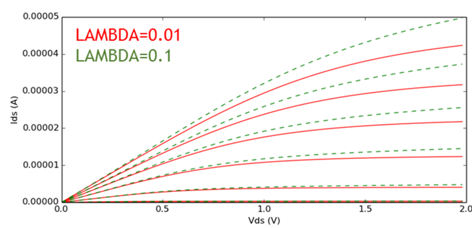
Physically, ALPHASAT attempts to model the effect of the non-uniform depletion charge in the TFT channel due to Vds



When to change	Small changes in ALPHASAT primarily affects the point where saturation begins (effectively a Vdssat parameter). Smaller ALPHASAT results in earlier saturation. Note that this is NOT channel length modulation (see LAMBDA), *use if the linear region current fits well but saturation is occurring too late in your model*
Change by	Change by small amounts e.g. 0.05-0.1

Effect of LAMBDA

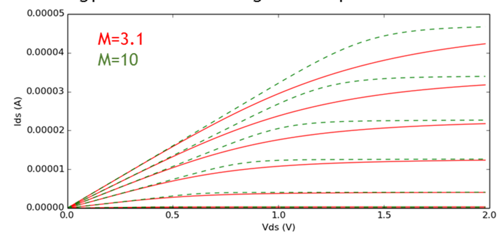
LAMBDA models channel length modulation



When to change	Use LAMBDA to control the slope at high VDS in saturation. Make sure though that the TFT being modelled does in fact reach saturation and is not limited by ALPHASAT.
Change by	Change by moderate amounts, but for very good devices, do not hesitate to make LAMBDA small.

Effect of M

M is a fitting parameter that changes the shape of the Id-Vds 'knee'



When to change	When the transition between linear and saturation regions is not sufficiently sharp. Larger M = sharper knee.
Change by	Change by integer values

Appendix E

Calibration procedure for TFT f_t measurements

One port calibration is performed using SMA-N adapters on the end of the SMA cables that connects to the VNA. The calibration kit fixtures are used on Port 1 to measure OPEN/SHORT/50OHM standards under the ECal mode on the VNA. For the THRU measurement, two BNC micro-alligator clips are connected to each SMA cable with a SMA-BNC adapter, and the red connections of the micro-alligator clips on ports 1 and 2 are clipped together.

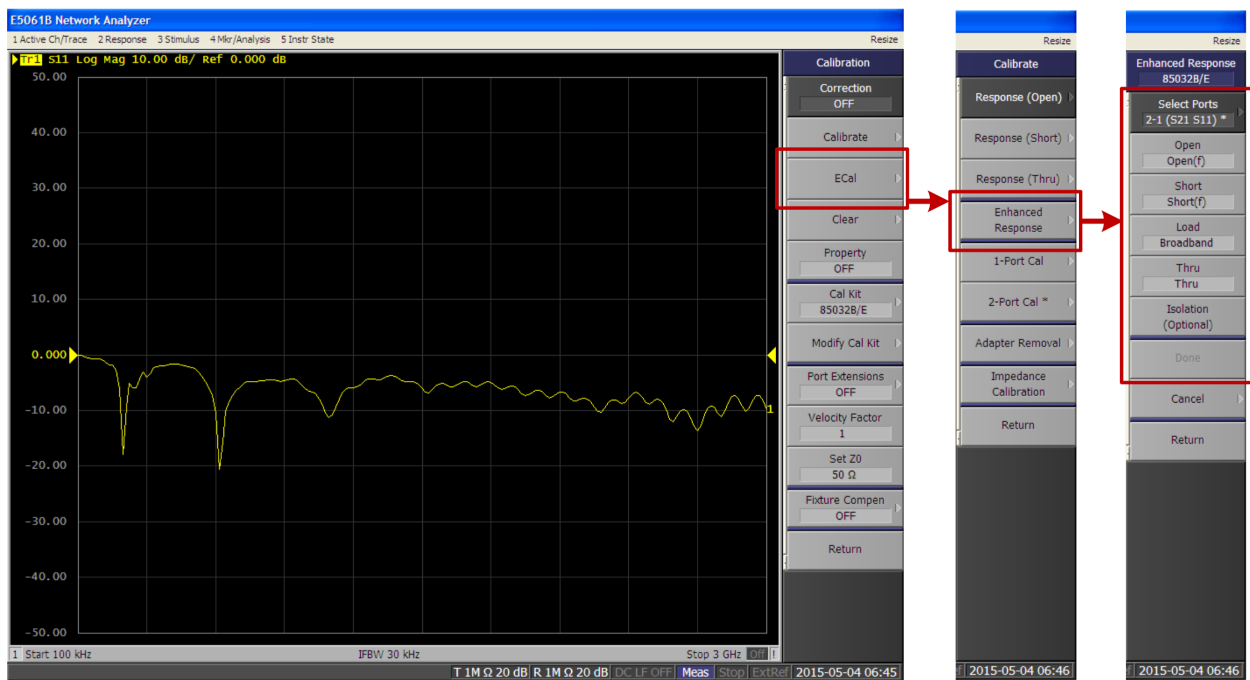


Figure E.1: Calibration on the VNA

Appendix F

List of publications and patent disclosures

F.1 Patents

- “System and method for interfacing large-area electronics with integrated circuit devices”, US Patent Application 13/367,856, 2012
- “System for 3-D Position and Gesture Sensing of Human Hand”, US Patent Application, 2013
- “A Large-Area Image Sensing and Detection System Based on Embedded Thin-Film Classifiers”, US Patent Application, 2014
- “Selective Self-Aligned Plating Of Heterojunction Solar Cells” US Patent Application 14/031732, 2013 (from IBM internship)

F.2 Journal publications

1. “A Complete Fully Thin-film PV Harvesting and Power-management System on Plastic with On-sheet Battery Management and Wireless Power Delivery to Off-sheet Loads”, Warren Rieutort-Louis, Liechao Huang, Yingzhe Hu, Josue Sanz Robinson, Sigurd Wagner, James

C. Sturm, and Naveen Verma, *IEEE Journal of Photovoltaics*, Vol. 4, Iss. 1, Pages 432-439 (2014)

2. "Large-scale Sensing System Combining Large-area Electronics and CMOS ICs for Structural Health Monitoring", Yingzhe Hu, Warren Rieutort-Louis, Josue Sanz Robinson, Liechao Huang, Branko Glisic, James C. Sturm, Sigurd Wagner, N. Verma, *IEEE Journal of Solid State Circuits*, Vol. 49, Iss. 2, Pages 513-523 (2014)

3. "A Self-powered System for Large-scale Strain Sensing by Combining CMOS ICs with Large-area Electronics", Yingzhe Hu, Liechao Huang, Warren Rieutort-Louis, Josue Sanz Robinson, James C. Sturm, Sigurd Wagner, N. Verma, *IEEE Journal of Solid State Circuits*, Vol. 49, Iss. 4, Pages 838-850 (2014) invited

4. "Hybrid Amorphous / Nanocrystalline Silicon Schottky Diodes for High Frequency Rectification", Josue Sanz-Robinson, Warren Rieutort-Louis, Yingzhe Hu, Liechao Huang, Naveen Verma, Sigurd Wagner, James C. Sturm, *IEEE Electron Device Letters*, Vol. 35, Iss. 4, Pages 425-427 (2014)

5. "A System Based on Capacitive Interfacing of CMOS with Post-processed Thin-film MEMS Resonators Employing Synchronous Readout for Parasitic Nulling", Liechao Huang, Warren Rieutort-Louis, Alexandra Gualdino, Laura Taegno, Yingzhe Hu, Joao Mouro, Josue Sanz-Robinson, James C. Sturm, Sigurd Wagner, Virginia Chu, Joao P. Conde, Naveen Verma, *IEEE Journal of Solid State Circuits*, Vol. 50, Iss. 4, Pages 1002-1015 (2015)

6. "Enabling Scalable Hybrid Systems: architectures for exploiting large-area electronics in applications", Naveen Verma, Yingzhe Hu, Liechao Huang, Warren Rieutort-Louis, Josue Sanz Robinson, Tiffany Moy, Branko Glisic, Sigurd Wagner, James C. Sturm, *Proceedings of IEEE* (2015)

7. "A Large-Area Image Sensing and Detection System Based on Embedded Thin-Film Classifiers", Warren Rieutort-Louis, Tiffany Moy, Zhuo Wang, Sigurd Wagner, James C. Sturm, Naveen Verma, *IEEE Journal of Solid State Circuits* (2015) Invited

8. “Integrating and Interfacing Flexible Electronics in Hybrid, Large-area Systems”, Warren Rieutort-Louis, Josue Sanz-Robinson, Tiffany Moy, Yasmin Afsar, Yingzhe Hu, Liechao Huang, James C. Sturm, Naveen Verma, Sigurd Wagner, *IEEE Journal of Components, Packaging and Manufacturing Technology* (2015) Invited

9. “Architecture of flexible large-area hybrid systems”, Sigurd Wagner, Warren Rieutort-Louis, Liechao Huang, Josue Sanz-Robinson, Tiffany Moy, Yingzhe Hu, Yasmin Afsar, James C. Sturm, Naveen Verma, *Information Display* (2015) Invited

F.3 Conference talks and posters

1. “Thin-film transistors and circuit-design styles for scalable control and access functionality over sensor arrays on plastic”, Warren Rieutort-Louis, Josue Sanz Robinson, James C. Sturm, Sigurd Wagner, Naveen Verma, *Materials Research Society Spring Meeting* (2012)

2. “A Full-Wave Bridge Rectifier Based on Amorphous Silicon Schottky Diodes for Integration with Inductively Coupled Links on Plastic”, Josue Sanz-Robinson, Warren Rieutort-Louis, Naveen Verma, Sigurd Wagner, James C. Sturm, *Materials Research Society Spring Meeting* (2012)

3. “High-resolution Sensing Sheet for Structural-health Monitoring via Scalable Interfacing of Flexible Electronics with High-performance ICs”, Yingzhe Hu, Warren Rieutort-Louis, Josue Sanz-Robinson, Katherine Song, James C. Sturm, Sigurd Wagner, Naveen Verma, *VLSI Symposium on Circuits*, Pages 120-121 (2012)

4. “Integrated All-silicon Thin-film Power Electronics on Flexible Sheets For Ubiquitous Wireless Charging Stations based on Solar-energy Harvesting”, Liechao Huang, Warren Rieutort-Louis, Yingzhe Hu, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, Naveen Verma, *VLSI Symposium on Circuits*, Pages 198-199 (2012)

5. “A Figure of Merit for Oscillator-Based Thin-Film Circuits on Plastic for High-Performance Signaling, Energy Harvesting and Driving of Actuation Circuits” Warren Rieutort-Louis,

Liechao Huang, Yingzhe Hu, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, Naveen Verma, *Device Research Conference* (2012), Pages 117-118 Poster

6. "Frequency Dependence of Amorphous Silicon Schottky Diodes for Large-Area Rectification Applications", Josue Sanz-Robinson, Warren Rieutort-Louis, Naveen Verma, Sigurd Wagner, James C. Sturm, *Device Research Conference* (2012), Pages 135-136 Poster

7. "Rapid Prototyping of Copper Inductor Coils by Mechanical Milling on Rigid and Flexible Substrates for Large-Area-Electronics", Therin Young, Warren Rieutort-Louis, James C. Sturm, *MIRTHE Summer Workshop* (2012) Summer Student

8. "Flexible Solar-Energy Harvesting System on Plastic with Thin-film LC Oscillators Operating Above ft for Inductively-coupled Power Delivery", Yingzhe Hu, Warren Rieutort-Louis, Liechao Huang, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, Naveen Verma, *Custom Integrated Circuits Conference*, Pages 1-4 (2012)

9. "Device Optimization for Integration of Thin-Film Power Electronics with Thin-Film Energy-harvesting Devices to Create Power-delivery Systems on Plastic Sheets" Warren Rieutort-Louis, Josue Sanz Robinson, Yingzhe Hu, Liechao Huang, James C. Sturm, Naveen Verma, Sigurd Wagner, *International Electron Devices Meeting*, Pages 12.3.1-12.3.4 (2012)

10. "A Super-Regenerative Radio on Plastic based on Thin-film Transistors and Antennas on Large, Flexible Sheets for Distributed Communication Links" Liechao Huang, Warren Rieutort-Louis, Yingzhe Hu, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, Naveen Verma, *International Solid State Circuits Conference*, Pages 458-459 (2013)

11. "Effect of Low-Temperature TFT Processing on Power Delivery from Thin-Film Power Electronics on Flexible Substrates", Warren Rieutort-Louis, Yingzhe Hu, Liechao Huang, Josue Sanz Robinson, Sigurd Wagner, Naveen Verma, James C. Sturm, *Materials Research Society Spring Meeting*, Paper E2.02 (2013) available on MRS OnDemand

12. "Hybrid Nanocrystalline / Amorphous Silicon Schottky Diodes for Large Area Electronic Systems" Josue Sanz Robinson, Yingzhe Hu, Warren Rieutort-Louis, Liechao Huang, Naveen

Verma, Sigurd Wagner, and James C. Sturm *Materials Research Society Spring Meeting* (2013)

13. "A Complete Fully Thin-Film PV Harvesting and Power-management System on Plastic with On-sheet Battery Management and Wireless Power Delivery to Off-sheet Loads", Warren Rieutort-Louis, Liechao Huang, Yingzhe Hu, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, Naveen Verma, *Photovoltaics Specialist Conference* (2013) Finalist for Best Student Paper Award

14. "A Fully Self-powered Hybrid System Based on CMOS ICs and Large-area Electronics for Large-scale Strain Monitoring", Yingzhe Hu, Liechao Huang, Josue Sanz Robinson, Warren Rieutort-Louis, Sigurd Wagner, James C. Sturm, Naveen Verma, *VLSI Symposium on Circuits*, Pages C212-C213 (2013) Best Student Paper Award

15. "Readout from Amorphous Silicon Thin-film Transistor-based Strain Sensing Sheets Over Non-Contact Interfaces using a TFT Gilbert-Type Modulator", Warren Rieutort-Louis, Josue Sanz Robinson, Yingzhe Hu, Liechao Huang, James C. Sturm, Naveen Verma, Sigurd Wagner, *International Conference on Amorphous and Nanocrystalline Semiconductors* (2013)

16. "High Current Density, Hybrid Nanocrystalline / Amorphous Silicon Schottky Diodes", Josue Sanz Robinson, Warren Rieutort-Louis, Yingzhe Hu, Liechao Huang, Naveen Verma, Sigurd Wagner, James C. Sturm, *International Conference on Amorphous and Nanocrystalline Semiconductors* (2013)

17. "Energy Harvesting and Power Management for Sensing Skins in SHM Applications", Yingzhe Hu, Liechao Huang, Josue Sanz Robinson, Warren Rieutort-Louis, Sigurd Wagner, James C. Sturm, Naveen Verma, *International Workshop on Structural Health Monitoring (IWSHM)* (2013)

18. "Hybrid Electronic Systems for Intelligent Surfaces", Warren Rieutort-Louis, Yingzhe Hu, Liechao Huang, Josue Sanz-Robinson, James C. Sturm, Naveen Verma, Sigurd Wagner, *Brazilian Materials Research Society Meeting, SPBMat* (2013)

19. “Modulation Doped Hydrogenated Amorphous Silicon Germanium Superlattice Contacts and Application to Optoelectronic Devices”, Bahman Hekmatshoar, Warren Rieutort-Louis, Davood Shahrjerdi, Richard Haight *ECS Meeting*, Paper E1-1853 (2013)

20. “Amorphous Silicon: a reliable model and platform for large-area circuits and systems”, Warren Rieutort-Louis, Josue Sanz-Robinson, Liechao Huang, Yingzhe Hu, James C. Sturm, Naveen Verma, Sigurd Wagner, *International Thin-Film Transistor Conference* (2014) Poster

21. “3D Gesture Sensing System for Interactive Displays based on Extended-range Capacitive Sensing”, Yingzhe Hu, Liechao Huang, Warren Rieutort-Louis, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, Naveen Verma, *International Solid State Circuits Conference*, Pages 212-213 (2014)

22. “Self-Aligned Thin-Film Transistor-based Oscillators”, Warren Rieutort-Louis, Liechao Huang, Yingzhe Hu, Josue Sanz-Robinson, Naveen Verma, James C. Sturm, Sigurd Wagner, *Materials Research Society Spring Meeting* (2014) Poster, nominated for Best Poster Award

23. “An ASIC for Readout of Post-Processed Thin-film MEMS Resonators by Employing Capacitive Interfacing and Active Parasitic Cancellation”, Liechao Huang, Warren Rieutort-Louis, Alexandra Gualdino, Laura Taegno, Yingzhe Hu, Joao Mouro, Josue Sanz-Robinson, James C. Sturm, Sigurd Wagner, Virginia Chu, Joao P. Conde, Naveen Verma, *VLSI Symposium on Circuits* (2014)

24. “Current Gain of Amorphous Silicon Thin-Film Transistors Above the Cutoff Frequency”, Warren Rieutort-Louis, Liechao Huang, Yingzhe Hu, Josue Sanz-Robinson, Tiffany Moy, Yasmin Afsar, James C. Sturm, Naveen Verma, Sigurd Wagner *Device Research Conference*, Pages 273-274 (2014)

25. “Thin-Film Circuits for Scalable Interfacing Between Large-Area Electronics and CMOS ICs”, Tiffany Moy, Warren Rieutort-Louis, Yingzhe Hu, Liechao Huang, Josue Sanz-Robinson, James C. Sturm, Sigurd Wagner, Naveen Verma, *Device Research Conference*, Pages 271-272 (2014)

26. "3D Multi-Gesture Sensing System for Large Areas based on Pixel Self-Capacitance Readout using TFT Scanning and Frequency-Conversion Circuits", Yingzhe Hu, Tiffany Moy, Liechao Huang, Warren Rieutort-Louis, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, Naveen Verma *Custom Integrated Circuits Conference* (2014) Poster

27. "A Large-Area Image Sensing and Detection System Based on Embedded Thin-Film Classifiers", Warren Rieutort-Louis, Tiffany Moy, Zhuo Wang, Sigurd Wagner, James C. Sturm, Naveen Verma, *International Solid State Circuits Conference*, Paper 16.2 (2015)

28. "Representative Flicker Noise Measurements For Low-Temperature Amorphous Silicon, Organic and Zinc Oxide Thin-Film Transistors", Warren Rieutort-Louis, Ren Shidachi, Yasmin Afsar, James C. Sturm, Naveen Verma, Takao Someya, Sigurd Wagner, *International Thin-Film Transistor Conference* (2015)

29. "Voltage Threshold Shift-Based Programmable Amorphous Silicon TFTs for use in Large-Area Systems", Tiffany Moy, Warren Rieutort-Louis, James C. Sturm, Sigurd Wagner and Naveen Verma, *International Thin-Film Transistor Conference* (2015)

30. "Apparent super-linear behavior of cutoff frequency in PEALD ZnO TFTs", Yasmin Afsar, Warren Rieutort-Louis, Naveen Verma, James C. Sturm, Sigurd Wagner, *International Thin-Film Transistor Conference* (2015) Poster

31. "A Thin-Film, Large-Area Image Compression System for Sensing and Detection", Tiffany Moy, Warren Rieutort-Louis, Zhuo Wang, Sigurd Wagner, James C. Sturm, Naveen Verma, *Custom Integrated Circuits Conference* (2015) Submitted

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