Molecular-scale Organic Electronic Devices for Integrated Nonvolatile Memory Application

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Abstract

Self-assembly techniques that allow the controlled growth of nanometer-scale organic molecular films present new opportunities to develop electronic devices with dimensions much smaller than those of current technologies. In this thesis we address several of the challenges to realizing this goal, and demonstrate a molecular-scale programmable-resistance memory device.

Although technologically attractive, field-effect transistors (FETs) with a self-assembled organic channel are difficult to realize due to the poor gate-channel coupling. We have used electrostatic modeling to determine guidelines that allow the maximum gate modulation of the channel potential in these devices.

Molecular-scale devices with integrated metal wiring are desirable for practical application. However, this typically requires the vacuum deposition of metal electrodes, which can damage the thin organic layer. We developed several approaches to fabricate two-terminal molecular-scale devices with vacuum-deposited metal electrodes and minimal defects in the organic layer. To demonstrate these device structures, we used films consisting of 1 to 12 self-assembled layers of 11-mercaptoundecanoic acid (MUA). The device structures that we developed included two large-area planar structures as well as a minimal-area structure that utilizes an insulating film to limit the device area to the edge of a metal layer. These structures allowed the first study of the mechanism of conduction in MUA films, which was characterized as Richardson-Schottky emission.

Finally, we found that these devices could be operated as a programmable memory by applying voltage pulses to increase or decrease the conductivity over a range of 10^3. The conductivity of the stored state could be read non-destructively with low-voltage pulses. Devices had remarkably large conductance (in the low-resistance state) of up to 10^6 S/cm^2 at 1 V, programmed states remained stable for many months, and devices were functional for more than 10^4 programming cycles. The likely mechanism for the programmable resistance was the formation and destruction of conducting paths due to metal injected into the MUA film. We discuss their practical application and show that because of their high conductance these devices are uniquely promising among organic memories for use in dense, high-speed memory arrays, where large conductance is required to minimize resistance-capacitance delays.

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Chapter 1

Introduction

1.1 Inorganic Crystalline Semiconductors

Inorganic crystalline semiconductors (predominantly silicon) have dominated the active-electronics industry since the 1950's [2]. Integrated circuits based on silicon are a cornerstone of modern society, and have enabled some of the most important recent technological trends, including the growth of the personal computer in the 1980's and early 90's, the internet in the late 90's, and wireless networks and mobile electronic devices in this century. Many of these new applications are in part a result of the tremendous progress in fabricating integrated circuits that constantly increase in complexity and performance at constant or decreasing cost. This trend, often characterized by the doubling of the number of transistors on a silicon chip every 18 to 24 months, has now achieved wide recognition as Moore's law [3].

One of the reasons for this technological success is that the electronic properties of silicon and other crystalline semiconductors are governed by band-like transport of charge-carriers in a semi-infinite lattice comprised of strongly bonding atoms [4]. This results in very high charge carrier mobilities, which allows crystalline semiconductors to operate at very high speeds and low voltages. Furthermore, by the addition of electrical dopants, the number of charge carriers (and hence the resistivity of the Si) can be altered in a controllable manner.

Despite their remarkable performance, inorganic crystalline semiconductors have several drawbacks. First, they require relatively high fabrication costs to minimize crystalline defects that degrade their electrical properties. Second, the brittle nature of most crystalline substrates makes them difficult to use in applications that require mechanical flexibility, although the thinning of silicon substrates to thicknesses of 10 to 30 μm to increase their tolerance of mechanical stress has increased their versatility [5]. Third, even though doping can be used to change a semiconducting crystal's resistivity, it is difficult to alter other properties (such as its bandgap), limiting its versatility. Finally, as devices scale to several nanometers, the crystal no longer acts as a semi-infinite lattice, and surface and quantum effects begin to dominate electrical

characteristics [6, 7]. Highly scaled devices therefore no longer have electrical properties that are similar to larger devices. Furthermore, the statistical nature of the doping process used to control electrical properties makes it very difficult to ensure uniform doping concentrations at the nanometer scale, leading to large, uncontrollable variations in device properties. It is thus very difficult to ensure that highly scaled devices in a crystalline semiconductor will behave uniformly, a prerequisite for any integrated circuit.

1.2 Opportunities for Organic Semiconductors in Highly-Scaled Applications

Unlike inorganic semiconductors, organic (i.e. carbon-based) semiconductors have historically played a negligible role as the active elements of electronic circuits (although they have found significant application in other areas of electronics, such as in electrical insulation and as photoconductors in photocopiers and laser printers [8-10]). One reason for this minimal role is that organic materials typically form amorphous or polycrystalline materials in which the weak bonding between molecules limits the mobility of charge carriers. However, organic semiconductors have a number of strengths that complement the weaknesses of crystalline semiconductors. These strengths include low deposition costs and mechanical flexibility (both due in part to their amorphous or polycrystalline nature), and an enormous variety of readily synthesizable structures, resulting in a great degree of control over functionality [2]. These strengths have resulted in considerable recent interest in organic semiconductors.

Most of this attention has focused on organic light-emitting devices (OLEDs). OLEDs have much potential for use in applications such as full-color displays because of their low deposition costs, reasonable electroluminescence efficiencies, and tunable emission [8, 11, 12]. In contrast, crystalline semiconductors based on III-V semiconductors such as AlGaAs have better electroluminescent efficiencies but at much higher fabrication costs, and because their bandgap (and therefore emission) is more difficult to tune they are not as compatible with multi-color emission [13]. OLEDs may therefore represent a better route to the goal of a high-performance, low-cost, flexible, low-power, and light-weight (highly portable) display. The OLED research that

has occurred within the last two decades has already resulted in the commercial production of initial generations of OLED displays [12].

The success enjoyed by OLEDs has encouraged researchers to explore other potential applications of organic semiconductors. Most of these lie in optoelectronics, and include solar cells, photodetectors, and thin-film transistors (the transistors would likely be used as support electronics for optoelectronic devices, e.g. to drive OLEDs in a display) [11]. A common feature of these applications is the requirement that devices be fabricated over a large area. In large-area devices, the ability to deposit organic materials at low cost provides an important advantage over most inorganic semiconductors (although amorphous and polycrystalline Si technologies represent promising alternative approaches [14-16]). However, the varied functionality of organic materials makes them of interest for other electronics besides these large-area optoelectronic applications. One such application that within the past several years has generated considerable interest is electronic memory [17]. This interest is driven by the enormous demand for low-cost and high-performance memory for use in portable electronic devices.

In fact, there is growing interest in utilizing organic materials in applications that lie completely outside the field of large-area electronics. In particular, the discipline of molecular electronics seeks to use individual organic molecules as the active elements of highly-scaled (i.e. very small) electronic circuits [3, 18]. Organic molecules, with a typical dimensions of ~1-3 nm, could be several orders of magnitude smaller than the current size of typical silicon FETs (~100 nm) [2]. Moreover, charge transport in single molecules would not depend on doping concentrations and should be less susceptible to surface effects, so that the each molecular device would in principle behave identically [6]. Chemical techniques (such as self-assembly) may enable massively parallel fabrication (and integration) of molecular devices, similar to very large scale integration (VLSI) techniques in silicon.

1.3 Electrical Properties of Metal-Molecule Junctions

A key step in achieving the goal of using individual molecules as active circuit elements is the theoretical and experimental understanding of charge transport through metal-molecule-metal junctions [19]. These molecular junctions can contain one molecule or a single molecular layer. It is expected that a molecular layer will act, to

first order, as group of molecules conducting in parallel (although recent results suggest that this may be too simplistic [20]). A theoretical understanding of how the structure and properties of different molecules and metals affect charge transport in these junctions should allow the design of molecules with properties that could be tailored for circuit application.

In this section, we discuss molecular energy levels and their relationship to the electrical properties of molecular junctions. Molecular energy levels can be calculated by combining the atomic orbitals of the constituent atoms. The simplest example is the molecular σ bond that is formed between two carbon atoms in an alkane chain such as polyethylene $(CH_2)_n$ (Fig. 1.1). The two hybrid (sp^3) atomic orbitals of the carbons form two new molecular orbitals, called σ and σ^*. The interaction between the atomic orbitals leads to an energy splitting, so that the σ orbital has lower energy than the atomic orbitals, while the σ^* orbital has higher energy. Occupation of the σ orbital is energetically favorable, so it is filled by electrons (with opposite spins) from the initial atomic orbitals, resulting in bonding. Occupation of the σ^* orbital would result in higher energy, so the σ^* orbital is called the anti-bonding state. The significant overlap of the original atomic orbitals leads to a relatively large energy difference $E_{\sigma^*-\sigma}$ between the molecular orbitals [21].

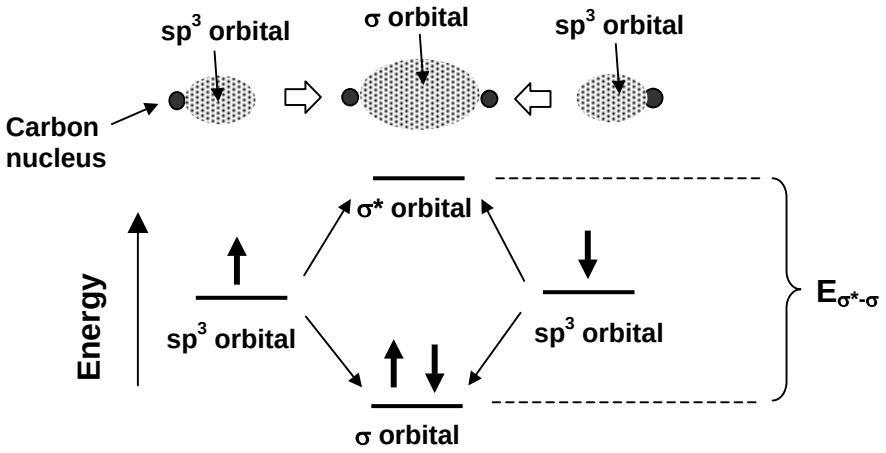


Figure 1.1. Schematic representation of σ bonding between 2 carbon atoms. On top is the most probable location of electrons in the sp^3 orbitals of the isolated carbon atoms and in the molecular σ bond. On the bottom are the relative energy levels of the atomic and molecular orbitals.

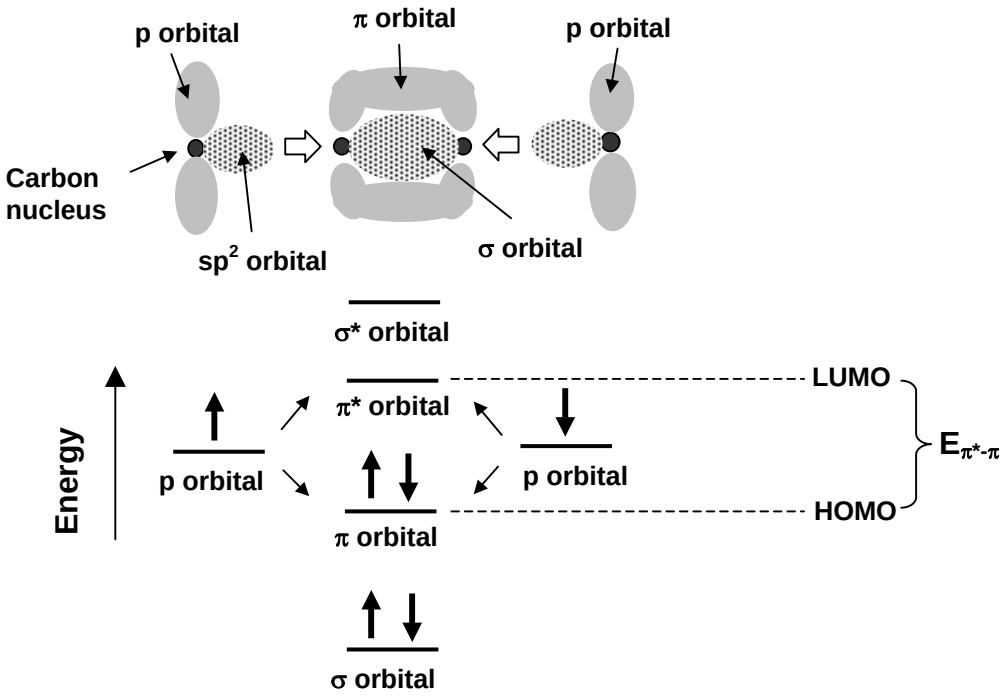


Figure 1.2. Schematic representation of double bonding between 2 carbon atoms. On top is the most probable location of electrons in the p orbitals of the isolated carbon atoms and in the molecular π bond. On the bottom are the relative energy levels of the atomic and molecular orbitals. In this example, electrons fill the σ and π orbitals, so that the π orbital is the highest occupied molecular orbital (HOMO) and the π* orbital is the lowest unoccupied molecular orbital (LUMO).

A double bond between carbon atoms is formed from atomic p orbitals that mix to form molecular π and π* orbitals (Fig. 1.2). The smaller spatial overlap between the p orbitals (which are perpendicular to the bond axis) results in a smaller splitting energy ($E_{\pi^*-\pi}$) between the π and π* orbitals. Unlike σ orbitals, which are localized between atomic nuclei, π orbitals are often delocalized over many atoms. In these instances, the molecular orbital consists of multiple atomic orbitals. This most commonly occurs in carbon chains with alternating single and double bonds (called conjugated bonds). A representation of a delocalized π orbital, consisting of multiple atomic p orbitals, is shown for the benzene molecule in Figure 1.3.

A typical organic molecule contains many orbitals, with each constituent atom contributing an orbital for each of its valence electrons. These electrons then occupy (with two electrons per orbital) those molecular orbitals with the lowest energy. Of

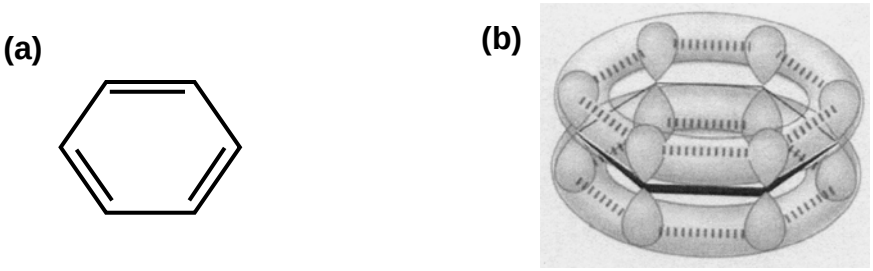


Figure 1.3. (a) Benzene ring with alternating double and single carbon bonds, resulting in conjugation. (b) Representation of spatial location and extent of π orbitals formed from atomic p orbitals in benzene ring (from Ref. [1]).

special importance in determining the electrical properties of the molecule is its highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO). In the example of Figure 1.2, the HOMO is the π orbital, while the LUMO is the π^* orbital. We will see that to some extent the HOMO and LUMO levels (and the energy gap between them) play roles analogous to the valence and conduction levels (and bandgap) in a crystalline semiconductor.

To model current flow through a molecule or molecular layer between two electrodes, it is common to use approaches that were originally developed in the 1980's to describe mesoscopic systems (e.g. two-dimensional electron gases) [22]. In the Landauer-Buttiker formalism that can be used to describe coherent electron transport, the current for a voltage *V* is obtained with the formula [23]:

$$I = \frac{2e}{h} \int_{-\infty}^{\infty} dE\, T(E,V)\,[\, f(E-\mu_1) - f(E-\mu_2)\,]. \qquad (1)$$

Here, *e* is the charge of an electron, *h* is Planck's constant, *T(E,V)* is the probability that an electron with energy *E* is transmitted through the junction, μ_1 and μ_2 are the chemical potentials of the electrodes, and *f(E)* is the Fermi-Dirac distribution. For small bias voltages, the applied voltage *V* is equal to $(\mu_1 - \mu_2)/e$. This equation intuitively implies that the number of electrons that pass through the junction is given by the transmission probability at a given energy, multiplied by the probability that there is an electron with this energy in one electrode as well as an empty state in the second electrode for the electron to enter, then integrated over all possible energies. This equation is applicable at very low temperatures; at higher temperatures, modes of

transport that involve inelastic scattering (primarily with the vibrations of atomic nuclei) become important, requiring more complex approaches [24].

For room temperature measurements at small voltages, equation (1) can be simplified to [22]:

$$I = \frac{2e^2}{h} T(E_F) V \,, \tag{2}$$

where E_F is the Fermi level (determined by the electrodes). The quantity $2e^2/h$ is equal to $(12.9\ \text{k}\Omega)^{-1}$ and is referred to as the conductance quantum. E_F must lie in the gap between the HOMO and LUMO of the molecule (otherwise charge would be transferred between molecules and electrodes until this condition is fulfilled) [24]. Because the transmission coefficient is evaluated at E_F, the level closest to E_F (i.e. the HOMO or LUMO) dominates charge transport. This situation is very similar to that of an inorganic semiconductor between metal electrodes, where the proximity of the semiconductor's valence or conduction level to E_F determines the amount and type of conduction (i.e. conducting vs insulating, and electron vs hole conduction). For molecules such as alkane chains that have only σ bonds, the large difference in energy between σ and σ^* orbitals (Fig. 1.1) leads to a large energy gap between HOMO and LUMO (typically >7 eV [25, 26]). This makes it unlikely that either level will reside near the Fermi energy, so alkanes tend to be relatively good insulators. Conjugated molecules (such as benzene) have lower energy gaps between the HOMO and LUMO (due to the smaller splitting of π and π^* orbitals (Fig. 1.2)); these lower energy gaps (typically ~3 eV [21]) help make them better conductors than alkane chains.

More quantitative determination of the transmission coefficient (and its equivalent in more complicated, inelastic theories) from first principles remains a challenge. Calculations are very sensitive to the exact nature of the binding between metal and molecule and the degree of charge transfer during this binding [24, 27-29]. For example, when a molecule is attached to an electrode for measurement, its orbitals are significantly perturbed by the metallic states, so that the apparent properties of the molecule can depend intimately on the metal used to measure it [30]. For this reason, workers are generally careful to refer to conduction as through a metal-molecule-metal junction, and not through the molecule itself [22]. However, it is often difficult to calculate how molecular and metallic states interact, especially since this interaction can depend on the exact geometry of the binding between the molecule and metal

surface [31]. Nevertheless, several instances of promising agreement between experimental measurements and theoretical calculations of transport in molecular junctions have already been reported [32, 33].

1.4 Conduction in Organic Solids

Although we focus on molecular-scale organic films in this thesis, our devices are not strictly metal-monolayer-metal junctions and instead consist of multiple self-assembled organic layers. In addition to charge transport within molecules and between molecules and electrodes, charge transfer between molecules is therefore relevant for our films. For large numbers of self-assembled layers, the behavior of our devices should approach those of bulk organic solids. Fortunately, much of the discussion of Section 1.3 is relevant to electrical conduction in organic solids. Unlike the atoms in inorganic crystalline semiconductors that form covalent or ionic bonds, the constituents of an organic solid (which can range from small molecules to lengthy polymers that comprise enormous numbers of atoms) interact weakly, through van der Waals forces. This usually results in an amorphous or polycrystalline film. Furthermore, molecular energy levels in the solid phase are left relatively undisturbed, so that many of the features of single molecules are retained. For example, solids composed of alkane chains remain much less conductive than those based on conjugated molecules. The molecular HOMO, LUMO, and how these levels align with metal energy levels also remain key considerations.

However, the enormous variety in the composition of organic solids (i.e. polymers vs small molecules, conjugated vs alkane chains, etc) has led to a wide range of device characteristics. This has made it difficult to develop a unified, quantitative model for charge transport in organic solids akin to the band model in crystalline semiconductors. As a result, researchers have employed a variety of semi-empirical models to describe individual results. These include bulk-limited mechanisms such as trap-limited and hopping models, as well as field-emission and tunneling models that suggest injection-limited conduction [34-36]. In many cases unambiguous determination of an appropriate model has remained difficult. Still, it is widely agreed that the limited intermolecular interaction leads to a localization of electronic states, so that in amorphous organic semiconductors the charge transfer between molecules occurs due to thermally-activated hops [34]. Encouraging progress

is being made in the development of more fundamental and broadly relevant models based on this understanding (such as the model of Bassler and coworkers, which describes charge transport in organics as hopping within a Gaussian density of states) [37-40].

1.5 Molecular Films by Self-Assembly

Self-assembly processes, where smaller elements spontaneously organize to create larger ordered structures, have attracted much recent interest [41]. In our work, we focus on the solution-based deposition of thin organic films by self-assembly, which is proving to be a very powerful technique in the fabrication of molecular junctions [6, 18]. Typically, a substrate is immersed into a solution containing the self-assembling molecule (Fig 1.4(a)). Chemically active functional groups on the end of this molecule then attach to the substrate (Fig. 1.4(b)). After an immersion of several hours, the strong reaction between the functional groups and substrate as well as the Van der Waals forces between adjacent molecules can lead to a close-packed, uniformly-oriented crystalline self-assembled monolayer (SAM) of the molecules (Fig. 1.4(c)). An important feature of this process is that after molecules have attached to all of the available sites on the substrate, the growth process cannot continue. The process is therefore self-limiting, and allows features having vertical dimensions on the scale of a single molecular length (1-2 nm) to be deposited without the need for extremely precise

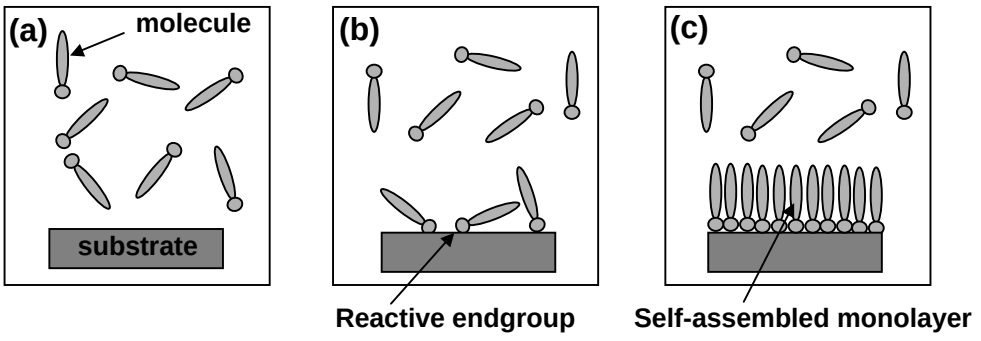


Figure 1.4. Growth of a self-assembled monolayer. (a) Substrate is immersed in dilute solution containing assembling molecule. (b) Reactive endgroup causes molecules to attach to substrate. (c) After several hours, a densely packed monolayer is formed.

(and expensive) equipment.

If the substrate on which the SAM is deposited is metallic and the top of the layer is placed in contact with a second metal layer so that the SAM is contacted by two electrodes, an electrical device (i.e. molecular junction) with the SAM as the active layer is formed. Because of the relative ease of self-assembling a monolayer in comparison with the difficulty of manipulating a single molecule, self-assembly has become a common approach for making molecular junctions. In addition to finding current use in fabricating molecular junctions for research, self-assembly may also be promising for manufacturing because enormous numbers of molecules (or, in principle, molecular devices) can be deposited in parallel at locations precisely specified with appropriate chemistries (although interconnection for circuit operation remains a critical challenge) [42].

1.6 Summary and Thesis Organization

Electronic devices based on crystalline silicon have enjoyed enormous technological success, but face growing challenges in continued scaling to reduced device dimensions. Molecular-scale electronics offer exciting possibilities for making devices that can achieve (i) the ultimate in scaling (1-2 nm) with high reproducibility (since molecules would not be sensitive to doping variations or surface effects), (ii) a wide variety of functionality, and (iii) low-cost, parallel fabrication by self-assembly methods. Similar to organic solids, the electronic properties of molecular-scale devices will depend on the HOMO and LUMO orbitals, which play roles analogous to the valence and conduction levels in crystalline semiconductors. A key approach for preparing molecular-scale devices will likely be solution-based self assembly, which has already found widespread use in fabricating electronic devices based on self-assembled monolayers.

In this thesis, we study organic molecular films for use in highly scaled circuits, with a focus on electronic memory. The use of organic semiconductors in highly scaled (rather than large-area) applications results in a number of challenges. In the first portion of this thesis, we address several challenges in preparing devices based on self-assembled nanometer-scale organic films. We then consider the opportunities for new memory technologies, and the requirements for integrating an organic memory device into high-speed and high-density circuits for practical application. Finally, we

demonstrate a molecular-scale organic memory device that meets many of these requirements.

Chapter 2 explores the scaling of the field-effect transistor (the key component of most active circuits) to molecular dimensions based on electrostatics. Optimal geometries for making three-terminal measurements at the molecular-scale are determined. Because of the geometric constraints of three-terminal devices, two-terminal organic devices may ultimately be of more technological interest.

For maximum flexibility, and because of the difficulty in making electrical contacts to single-organic-layer devices, a molecule that can form multiple self-assembled layers was chosen for detailed study in this thesis. Chapter 3 describes the growth and characterization of self-assembled multilayers of this molecule, 11-mercaptoundecanoic acid (MUA).

One of the most critical challenges in the development of molecular-scale devices is due to the very thin (~1 to 2 nm) nature of most self-assembled films. This makes it very difficult to fabricate them with integrated metal wiring, as required for practical application. For example, if a conventional technique such as vacuum evaporation is used to deposit a top metal electrode, the energetic metal atoms are likely to penetrate the thin organic layer, leading to electrical shorting that obscures the electrical characteristics of the organic layer. Chapter 4 discusses the fabrication of two-terminal molecular-scale device structures that are compatible with integrated metal wiring for practical application. These test structures are used to make the first reported electrical measurements on MUA multilayer films. The dependence of the electrical characteristics on fabrication conditions is explored, and the optimal conditions for preparing MUA devices with a very high yield of devices with minimal electrical defects are determined. Finally, a model for the electrical transport through the MUA layers, based on Richardson-Schottky emission, is proposed.

Chapter 5 describes the development of an alternative device structure having minimal device area, and discusses the electrical properties of devices fabricated with this structure.

In Chapter 6, the opportunities for new memory technologies are explored, and some emerging organic memory technologies are reviewed. The requirements for the integration of organic memory devices into high-speed and high-density circuits are considered.

Chapters 7 and 8 present the key results of this thesis. In Chapter 7, the characteristics of a novel, highly conductive two-terminal molecular-scale memory based on MUA films and the device structures described in Chapters 4 and 5 is reported. In Chapter 8, a possible mechanism based on the formation and destruction of conducting paths is studied to explain the observed programmable conductance of the devices. These devices have promising attributes that meet many of the requirements for use in high-speed and high-density memory circuits.

Chapter 9 reviews the major conclusions of this thesis and suggests possible directions for future work.

Appendix A reports additional work that was done to investigate the physics of a solvent-enhanced dye diffusion process that can be used to pattern polymer light-emitting diodes (PLEDs) for full-color emission.

Additional experimental details are included in Appendix B.

References

[1] M. Jones, *Organic Chemistry*. 1st ed. 1997, New York: W. W. Norton and Company.

[2] R. L. McCreery, "Molecular Electronics" *The Electrochemical Society Interface* **13** (1), 25,30 (2004).

[3] J. M. Tour, "Molecular Electronics. Synthesis and Testing of Components" *Accounts of Chemical Research* **33** (11), 791-804 (2000).

[4] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*. 2nd ed. 1986, New York: John Wiley and Sons.

[5] G. Klink, M. Feil, F. Ansorge, R. Aschenbrenner and H. Reichl, "Innovative Packaging Concepts for Ultra Thin Integrated Circuits" in *Electronic Components and Technology Conference Proceedings, 51st*, Orlando, FL, 1034-1039 (2001).

[6] D. L. Allara, T. D. Dunbar, P. S. Weiss, L. A. Bumm, M. T. Cygan, J. M. Tour, W. A. Reinerth, Y. Yao, M. Kozaki and L. Jones, *Evolution of Strategies for Self-Assembly and Hookup of Molecule-Based Devices*, in *Molecular Electronics: Science and Technology*. 1998. p. 349-370.

[7] B. A. Mantooth and P. S. Weiss, "Fabrication, Assembly, and Characterization of Molecular Electronic Components" *Proceedings of the IEEE* **91** (11), 1785-1802 (2003).

[8] K. Kaneto, K. Kudo, Y. Ohmori, M. Onoda and M. Iwamoto, "Recent Progress in Organic Film Devices for Optics and Electronics" *IEICE Transactions on Electronics* **E81-C** (7), 1009-1019 (1998).

[9] J. M. Shaw and P. F. Seidler, "Organic Electronics: Introduction" *IBM Journal of Research and Development* **45** (1), 2-9 (2001).

[10] P. Gregory, *High-Technology Applications of Organic Colorants*. 1991, New York: Plenum Press.

[11] S. R. Forrest, "Active Optoelectronics Using Thin-Film Organic Semiconductors" *IEEE Journal on Selected Topics in Quantum Electronics* **6** (6), 1072-1083 (2000).

[12] G. Parthasarathy, J. Liu and A. R. Duggal, "Organic Light Emitting Devices: From Displays to Lighting" *The Electrochemical Society Interface* **12** (2), 42-47 (2003).

[13] U. Mitschke and P. Bauerle, "The Electroluminescence of Organic Materials" *Journal of Materials Chemistry* **10**, 1471-1507 (2000).

[14] F. Lemmi, W. Chung, S. Lin, P. M. Smith, T. Sasagawa, B. C. Drews, A. Hua, J. R. Stern and J. Y. Chen, "High-Performance Tfts Fabricated on Plastic Substrates" *IEEE Electron Device Letters* **25** (7), 486-488 (2004).

[15] D. Pribat, *The Use of Thin Silicon Films in Flat Panel Displays*, in *Advanced Materials Forum Ii*. 2004. p. 56-63.

[16] M. G. Clark, "Current Status and Future-Prospects of Poly-Si Devices" *IEEE Proceedings-Circuits Devices and Systems* **141** (1), 3-8 (1994).

[17] Y. Yang, L. P. Ma and J. H. Wu, "Organic Thin-Film Memory" *MRS Bulletin* **29** (11), 833-837 (2004).

[18] M. A. Reed, "Molecular-Scale Electronics" *Proceedings of the IEEE* **87** (4), 652-658 (1999).

[19] C. R. Kagan and M. A. Ratner, "Molecular Transport Junctions: An Introduction" *MRS Bulletin* **29** (6), 376-384 (2004).

[20] Y. Selzer, L. T. Cai, M. A. Cabassi, Y. X. Yao, J. M. Tour, T. S. Mayer and D. L. Allara, "Effect of Local Environment on Molecular Conduction: Isolated Molecule Versus Self-Assembled Monolayer" *Nano Letters* **5** (1), 61-65 (2005).

[21] A. Moliton and R. C. Hiorns, "Review of Electronic and Optical Properties of Semiconducting Pi-Conjugated Polymers: Applications in Optoelectronics" *Polymer International* **53**, 1397-1412 (2004).

[22] M. C. Hersam and R. G. Reifenberger, "Charge Transport through Molecular Junctions" *MRS Bulletin* **29** (6), 385-390 (2004).

[23] S. Datta, *Electronic Transport in Mesoscopic Systems*, in *Cambridge Studies in Semiconductor Physics and Microelectronic Engineering*, H. Ahmed, M. Pepper and A. Broers, Editors. 1995, Cambridge University Press: Cambridge.

[24] A. Nitzan and M. A. Ratner, "Electron Transport in Molecular Wire Junctions" *Science* **300** (5624), 1384-1389 (2003).

[25] A. Salomon, D. Cahen, S. Lindsay, J. Tomfohr, V. B. Engelkes and C. D. Frisbie, "Comparison of Electronic Transport Measurements on Organic Molecules" *Advanced Materials* **15** (22), 1881-1890 (2003).

[26] G. Teyssedre and C. Laurent, "Charge Transport Modeling in Insulating Polymers: From Molecular to Macroscopic Scale" *IEEE Transactions on Dielectrics and Electrical Insulation* **12** (5), 857-875 (2005).

[27] Y. Xue, S. Datta and M. A. Ratner, "Charge Transfer And "Band Lineup" In Molecular Electronic Devices: A Chemical and Numerical Interpretation" *Journal of Chemical Physics* **115** (9), 4292-4299 (2001).

[28] V. Mujica, A. E. Roitberg and M. A. Ratner, "Molecular Wire Conductance: Electrostatic Potential Spatial Profile" *Journal of Chemical Physics* **112** (15), 6834-6839 (2000).

[29] A. W. Ghosh, P. Damle, S. Datta and A. Nitzan, "Molecular Electronics: Theory and Device Prospects" *MRS Bulletin* **29** (6), 391-395 (2004).

[30] H. Basch and M. A. Ratner, "Binding at Molecule/Gold Transport Interfaces. Ii. Orbitals and Density of States" *Journal of Chemical Physics* **119** (22), 11943-11950 (2003).

[31] E. G. Emberly and G. Kirczenow, "Theoretical Study of Electrical Conduction through a Molecule Connected to Metallic Nanocontacts" *Physical Review B* **58** (16), 10911-10920 (1998).

[32] C. Kuergueris, J.-P. Bourgoin and S. Palacin, "Electron Transport through a Metal-Molecule-Metal Junction" *Physical Review B* **59** (19), 12505-12513 (1999).

[33] J. G. Kushmerick, D. B. Holt, J. C. Yang, J. Naciri, M. H. Moore and R. Shashidhar, "Metal-Molecule Contacts and Charge Transport across Monomolecular Layers: Measurement and Theory" *Physical Review Letters* **89** (5), 086802 (2002).

[34] M. A. Baldo and S. R. Forrest, "Interface-Limited Injection in Amorphous Organic Semiconductors" *Physical Review B* **64** (8), 085201 (2001).

[35] D. Braun, "Electronic Injection and Conduction Processes for Polymer Devices" *Journal of Polymer Science Part B-Polymer Physics* **41** (21), 2622-2629 (2003).

[36] N. Tessler and Y. Roichman, "Amorphous Organic Molecule/Polymer Diodes and Transistors-Comparison between Predictions Based on Gaussian or Exponential Density of States" *Organic Electronics* (In press)(2005).

[37] S. Barth, U. Wolf, H. Bassler, P. Muller, H. Riel, H. Vestweber, P. F. Seidler and W. Riess, "Current Injection from a Metal to a Disordered Hopping System. Iii. Comparison between Experiment and Monte Carlo Simulation" *Physical Review B* **60** (12), 8791-8797 (1999).

[38] U. Wolf, S. Barth and H. Bassler, "Electrode Versus Space-Charge-Limited Conduction in Organic Light-Emitting Diodes" *Applied Physics Letters* **75** (14), 2035-2037 (1999).

[39] U. Wolf, V. I. Arkhipov and H. Bassler, "Current Injection from a Metal to a Disordered Hopping System. I. Monte Carlo Simulation" *Physical Review B* **59** (11), 7507-7513 (1999).

[40] V. I. Arkhipov, U. Wolf and H. Bassler, "Current Injection from a Metal to a Disordered Hopping System. Ii. Comparison between Analytic Theory and Simulation" *Physical Review B* **59** (11), 7514-7520 (1999).

[41] M. V. Tirrell and A. Katz, "Self-Assembly in Materials Synthesis" *MRS Bulletin* **30** (10), 700-701 (2005).

[42] J. R. Heath and M. A. Ratner, "Molecular Electronics" *Physics Today* **56** (5), 43-49 (2003).

Chapter 2

Electrostatic Modeling of Molecular-Scale FETs

2.1 Introduction

This chapter examines the subthreshold operation of molecular-scale field-effect transistors (FETs) using electrostatic considerations. Transistors are the essential components of most electronic circuits. Because of the difficulties in the continued scaling of Si FETs, transistors based on organic self-assembled monolayers and single-molecules are very appealing and experimental efforts to fabricate these devices have received considerable attention [1-6]. In this chapter we will focus on monolayer FETs, although many of our results are also valid for single-molecule FETs. A schematic of the typical geometry of a monolayer FET is shown in Fig. 2.1(a). The molecular layer is sandwiched between metal source and drain electrodes, while the gate electrode is separated from the monolayer by a thin insulating layer (typically SiO_2 or Al_2O_3). Experimentally, monolayer FETs are very challenging to prepare, due to the difficulty of making electrical contact to the monolayer without electrical shorting (as discussed previously in Chapter 1, and in further detail in Chapter 4) as well as the additional requirement that the monolayer be adjacent to a third terminal for gating. We suggest an experimental approach for fabricating molecular-scale FETs in Chapter 5.

At the heart of all FETs, the gate must be able to modulate the electric potential (and hence the carrier concentration) at or near the surface of the semiconductor/organic layer. In the case of molecule-based FETs, the gate must modulate the surface potential of the organic layer by a substantial fraction of the gap between the HOMO and LUMO levels, which is typically several volts for a conjugated molecule. For example, experimental measurements of the model Au-benzenedithiol-Au system suggest that it will be necessary to modulate the surface potential by ~1 V to align molecular levels with source-drain Fermi levels [7].

In VLSI devices, it is well known that the influence of the source and drain at short channel lengths reduces the ability of the gate to control the channel potential [8]. In modern VLSI technology, the ratio of gate insulator thickness (t_{ins}) to channel length

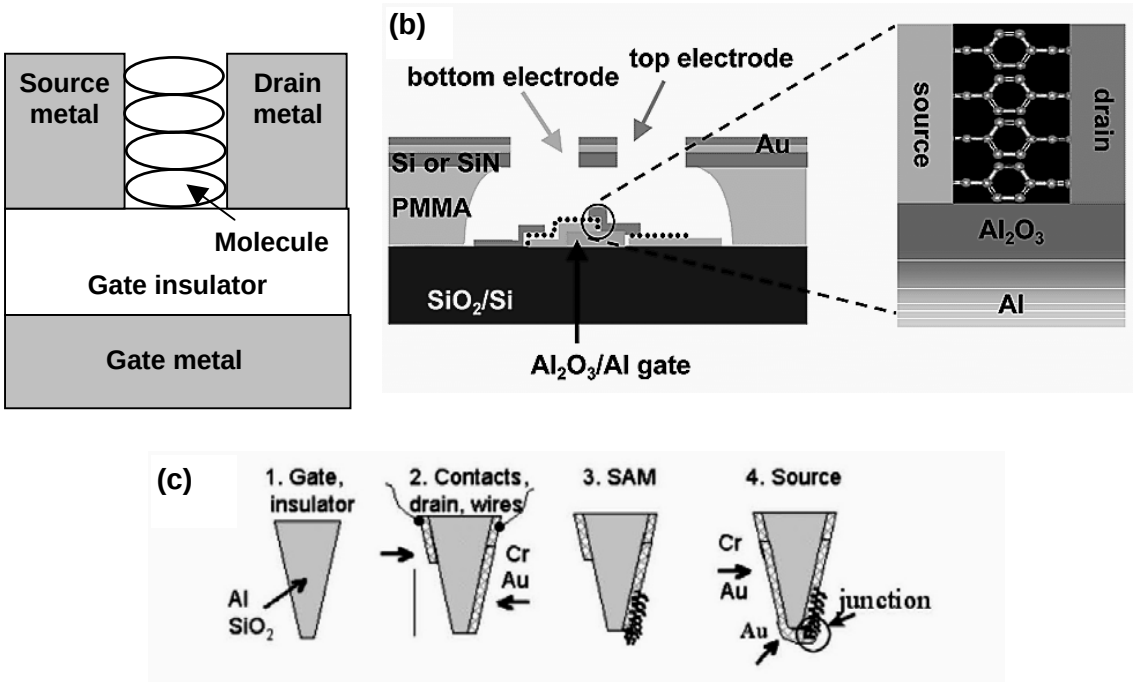


Figure 2.1. (a) Typical geometry of a monolayer FET. Molecule (channel) lengths are generally 1-3 nm, while gate insulator thicknesses range from 2 to 20 nm. (b) Schematic of geometry used by J.-O Lee et al to fabricate monolayer FETs (from Ref [1]). A gold bottom (source) electrode was evaporated onto an aluminum gate electrode (covered by a thin Al_2O_3 layer that served as a gate insulator). After growing an organic monolayer on this electrode, a top gold film (drain electrode) was deposited. The source and drain electrodes were patterned by directional evaporations through a pre-fabricated bridge structure. The inset depicts one of the benzenedithiol monolayers used in the study. (c) Schematic of fabrication process used by N. B. Zhitenev et al to prepare monolayer FETs (from Ref [2]). After depositing an Al gate and SiO_2 gate insulator on a quartz tip (step 1) (these layers are not explicitly shown in the diagram), metal contact electrodes then layers of Cr and Au were deposited (step 2). A monolayer was grown on the gold (step 3), and finally a second gold (drain) electrode was deposited to contact the monolayer (step 4).

(L) is maintained at ~ 1/45 to ensure optimum gate control over source-drain current [9]. This ratio is impossible to obtain in monolayer FETs, where molecular lengths (which determine the channel length) are typically 2-3 nm (implying t_{ins} of less than 0.04 nm to maintain a ratio of 1/45). Because of the difficulty in making gate insulators less than 1 to 2 nm thick, most monolayer FETs will have much larger ratios t_{ins}/L of at least 1, making gate-channel coupling difficult.

Despite the challenges imposed by the geometry of a monolayer FET, in 2001 J. H. Schön et al described self-assembled monolayer FETs (SAMFETs) with

remarkable characteristics that included large charge-carrier mobilities (>100 cm^2/s) and large ON-OFF ratios (>10^5) [10-15]. SAMFETs utilized a variety of conjugated molecules (such as benzendithiol) with typical lengths of several nanometers to form the FET channel and employed a 30 nm SiO_2 layer as a gate insulator, resulting in t_{ins}/L ~ 30. This is much larger than the desired 1/45 value. Nevertheless, from the published data we estimated a very low subthreshold slope of 50 mV/decade, which is even lower than the theoretical limit for Si FETs (~60 mV/decade) [16]. This implies that only very small changes in the gate voltage were required to increase or decrease the source-drain current in the subthreshold regime, suggesting a very strong gate-channel coupling in contrast to what is expected based on known VLSI scaling considerations.

This discrepancy between reported results and the predictions of known VLSI scaling considerations provided the original motivation for the electrostatic modeling of the subthreshold operation of monolayer FETs described in this chapter. After we began this study, it was found that the results reported by J. H. Schön et al were based on data falsified by J. H. Schön so were fraudulent (coauthors of the papers that included falsified data were found innocent of any scientific misconduct) [17]. More recently, other experimenters have been able to fabricate and measure self-assembled monolayers in three-terminal FET structures, with mixed results. For example, J.-O Lee et al have prepared monolayer FET structures by the evaporation of a gold source electrode (on which the monolayer was then grown) followed by a gold drain electrode onto an aluminum electrode (covered with 2-3 nm Al_2O_3 layer that served as a gate insulator) (Fig 2.1(b)) [1]. A pre-fabricated bridge structure was used to mask the source and drain layers to minimize their overlap and define the device area. Of the 5 molecular layers studied, only those consisting of benzenedithiol displayed a weak gating effect, at high gate voltages. In another example, N. B. Zhitenev et al have fabricated FETs on the tip of a quartz rod by exploiting the tip geometry and angled metal evaporations to pattern source and drain electrodes deposited on the tip (the tip was first coated with Al to act as a gate and then a 30 nm SiO_2 film for a gate insulator) (Fig. 2.1(c)) [2]. At low temperatures, sharp steps in the current through conjugated molecules were observed when scanning the gate voltage. However, relatively large gate voltages (2 V) were required to obtain small modulations in the source-drain current, suggesting that the gate was only weakly coupled to the organic monolayer channel.

Because of the nontraditional geometry of monolayer FETs resulting in poor gate-channel coupling, new guidelines are needed to determine optimal transistor designs. In this chapter, we use 2-D electrostatic modeling to determine monolayer-FET structures with the maximum capability to modulate the channel potential via the gate terminal for transistor action.

2.2 Setup of Electrostatic Simulations

The FET geometry used in the electrostatic simulations is shown in Figure 2.2. The adjustable parameters included the channel length L, gate insulator thickness t_{ins}, and channel and insulator dielectric constants κ_{org} and κ_{ins}. The channel dielectric constant was set to κ_{org}=2.5, while κ_{ins} was varied to represent different gate insulator materials [18, 19]. The electric potential inside the channel was calculated for a voltage V_g applied to the gate with the source and drain grounded. The modeling was done assuming an insulating (undoped) organic channel and neglecting any surface charges. This assumption of negligible charge in the organic channel is valid below threshold. In this region (which is the focus of our study), one is trying to modulate the surface potential to reach the point where charges significantly accumulate.

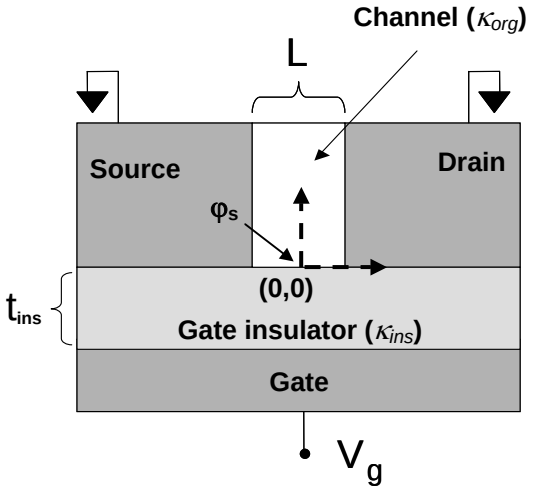


Figure 2.2. FET geometry used in simulations. Variable parameters are channel length L, insulator thickness t_{ins}, and insulator and channel dielectric constants κ_{ins} and κ_{org}. The surface potential φ_s is defined at the origin of the x-y coordinate system. The inverted structure with gate on bottom is typical in monolayer FETs but is not critical to the results.

Of particular interest is the surface potential φ_s at a position located on the semiconductor/gate-insulator interface and centered between the source and drain electrodes in the channel. The location of φ_s was also used to define the origin of an *x*-*y* coordinate system in the channel region (the *x*-axis is parallel to the channel length and the *y*-axis is perpendicular). Potentials and electric fields in the device were calculated with the Macsyma PDE-Solver program. When evaluating the potential near the corners of the source and drain electrodes, these corners were given a finite radius of curvature (typically 0.2 to 0.5 nm) to minimize physically unrealistic effects that result from the assumption of perfectly sharp corners. For most calculations (especially when the potential near the corners was not of interest) the choice of sharp or rounded corners had little effect.

2.3 Simulation Results

For a given gate voltage, the maximum potential in the channel is φ_s. The decay of the potential at the surface of the channel away from the center along the *x*-axis is relatively slow for small t_{ins}/L (which corresponds to a typical VLSI FET), but occurs very quickly for large t_{ins}/L (due to the relative proximity of the source and drain electrodes) (Fig. 2.3(a)). Inside the channel, the decay of the potential away from the channel surface (along the y-axis) is almost independent of t_{ins} and is primarily

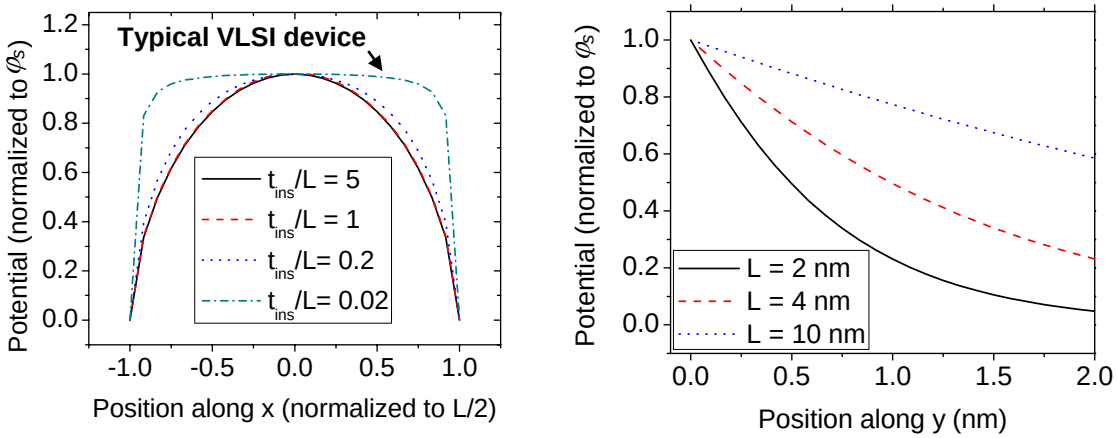


Figure 2.3. (a) Potential (normalized to φ_s) along the *x*-axis at $y = 0$ for various t_{ins}/L ($t_{ins}/L = 0.02$ corresponds to a typical VLSI device). The *x*-coordinates are normalized to L/2. (b) Potential (normalized to φ_s) along the y-axis (into the channel) at $x = 0$ for constant $t_{ins} = 4$ nm and different *L*.

determined by L (Fig. 2.3(b).). For example, for a channel length of 2 nm, which is the length of a typical self-assembled monolayer, the potential decays to less than 10% of its maximum value after a distance of 2 nm. For a typical lateral spacing between molecules of 0.5 nm [20], the gate will only be able to modulate the first several layers of molecules in the channel.

Because φ_s is the maximum possible potential in the channel for a given V_g, we will now focus on its dependence on different geometries. A main interest is the channel coupling efficiency $\xi = \varphi_s / V_g$. This quantity decreases rapidly as the ratio t_{ins}/L is increased (Fig. 2.4). For a typical VLSI transistor ($t_{ins}/L = 0.02$), ξ is near unity. However, a monolayer FET with an insulator thickness of 2 to 20 nm and monolayer thickness of 1 to 2 nm will have a much higher $t_{ins}/L > 2$ and a $\xi < 0.1$ [1-6]. It is also clear from Fig. 2.4 that a gate insulator with a high dielectric constant does not significantly improve the coupling. The best way to improve the coupling is to decrease t_{ins}/L to values of less than 1. For monolayers having a thickness of 1 to 2 nm this represents an enormous challenge because it would require the gate insulator to have a thickness below 1 to 2 nm.

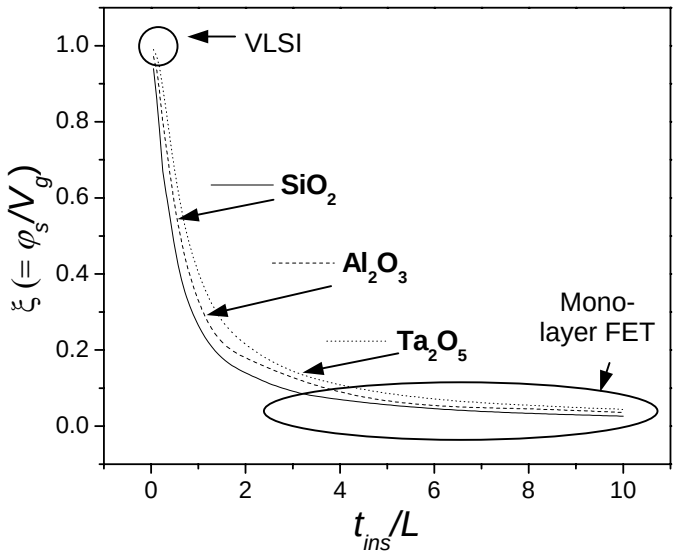


Figure 2.4. Coupling efficiency ξ vs. t_{ins}/L for an organic channel with $\kappa_{org} = 2.5$ and gate insulators SiO_2 ($\kappa_{ins} = 3.9$), Al_2O_3 ($\kappa_{ins} = 9$), and Ta_2O_5 ($\kappa_{ins} = 25$). Also shown is coupling for typical VLSI transistor ($t_{ins}/L \sim 0.03$) and typical monolayer FET ($t_{ins}/L \sim 2$ - 20).

The relationship shown in Fig. 2.4 is supported by reported results on gated monolayer and single-molecular layer structures. For example, in the device structure of Zhitenev et al ([2], Fig. 2.1(c)), the ratio of t_{ins}/L is ~25, and the authors find that the gate voltage is 50 to 100 times less effective in controlling device conductance than the source-drain bias (loosely implying ξ ~ 0.01 to 0.02). For t_{ins}/L = 25, our calculations indicate that ξ = 0.02, in close agreement. Similarly, in experiments on single-molecule FETs, where we estimate t_{ins}/L ranges between 3 to 10, the published plots of conductance vs both source-drain voltage and gate voltage (at temperatures below 5 K) suggest that ξ ranges between 0.02 to 0.1 [4, 5]. We base this estimate on the size of the region with a negligible differential conductance (i.e. conductance gap) as a function of source-drain voltage (typically a few mV) (for fixed gate voltage) in comparison with the size of the conductance gap as a function of gate voltage (typically ~100 mV) (with fixed source-drain voltage). Although a three-dimensional model would be necessary to accurately model the geometry in these single-molecule FETs, our two-dimensional model suggests that for t_{ins}/L between 3 to 10, we would expect ξ ~ 0.03 to 0.09, in agreement with the reported results.

Intuitively, the decreased gate-channel coupling is a result of increased capacitance to the source and drain. If we model φ_S as being connected to the gate, drain, and source electrodes by the capacitances C_G, C_D, and C_S (Fig. 2.5), we find that the channel potential is given by

$$\varphi_S = \frac{C_G V_G + C_D V_D + C_S V_S}{C_G + C_D + C_S}, \tag{1}$$

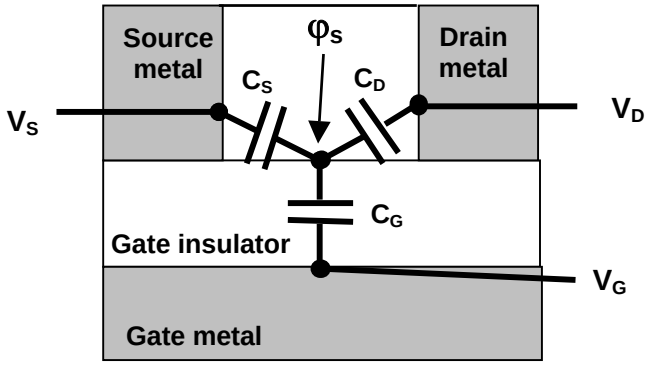


Figure 2.5. Capacitor model to estimate φ_S.

where V_G, V_D, and V_S are the potentials on the gate, drain, and source. For classical long-channel FETs, the long channel length (with respect to the gate insulator thickness) ensures that $C_G >> C_S, C_D$, so that $\varphi_s \approx V_G$ and $\xi \approx 1$. In molecular-scale FETs, this condition is no longer true, and for $V_D = V_S = 0$ (as in our simulations)

$$\varphi_S = \frac{C_G V_G}{C_G + C_D + C_S}, \tag{2}$$

so that $\xi = C_G / (C_G + C_D + C_S)$. This quantity goes to 0 for large t_{ins}/L ($C_S, C_D >> C_G$), as was seen in Figure 2.4.

The above analysis suggests (falsely) that structures with thin gate insulators and high κ_{ins} should be used for a maximum surface modulation. However, the possibility of dielectric breakdown of the gate insulator must also be considered. Figure 2.6 shows the electric fields inside an SiO_2 gate insulator as a function of t_{ins} under the condition that a sufficient voltage is applied to the gate to obtain φ_s = 1 V. Both the vertical gate field in the middle of the channel (line A, inset) and the gate-drain field (line B, inset) are similar at thick t_{ins} for given L. Although the gate-channel field drops with thin t_{ins}, the gate-drain field grows rapidly.

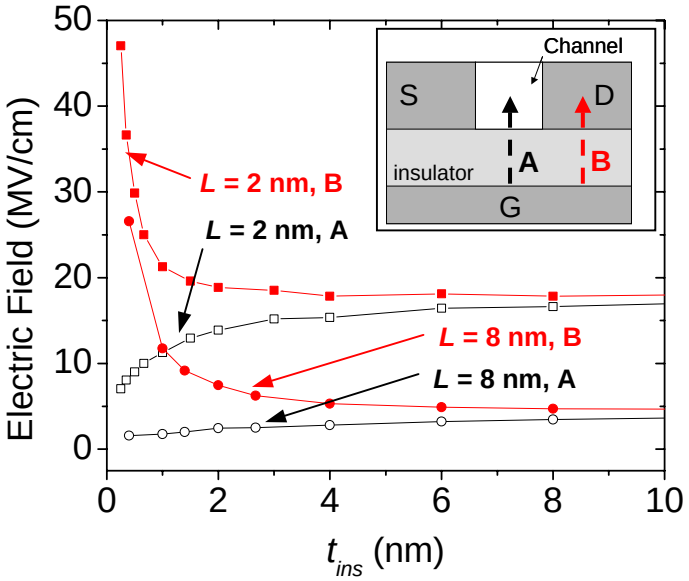


Figure 2.6. Electric fields along axes A and B (inset) in an SiO_2 gate insulator necessary to obtain $\Delta\varphi_s$ = 1 V as a function of t_{ins} for L = 2 nm and L = 8 nm. The highest field, which is along axis B, limits the gate modulation.

This effect is illustrated in more detail in Figure 2.7. Here, the potential along lines A and B is plotted for t_{ins} = 5 nm and L = 1 nm. In both cases, a gate voltage sufficient to obtain φ_s = 0.5 V is applied. For the case of t_{ins} = 5 nm, a larger voltage is necessary, but the slope of the potential (or electric field) is below the breakdown field (~ 0.5 V/nm) along both A (gate to channel) and B (gate to drain). Along A, the insulator must sustain a voltage drop of (2.3 V – 0.5 V) over 5 nm to yield an electric field of 0.36 V/nm. Similarly, the insulator sustains a field of (2.3 V– 0 V) / 5 nm = 0.46 V/nm along B. When t_{ins} is reduced to 1 nm, the electric field along A decreases slightly (0.7 V- 0.5 V) V/ 1 nm = 0.2 V/nm. However, the electric field along B increases (0.7 V- 0 V)/ 1 nm = 0.7 V/nm, exceeding the breakdown field in SiO_2 of 0.5 V/nm (= 5 MV/cm). Because the insulator in the source-drain region must sustain the entire voltage drop (instead of just the difference between the gate and channel potential) it is the limiting factor in the voltage that can be applied to the gate to modulate the channel potential. We note that this limit is not observed in VLSI in

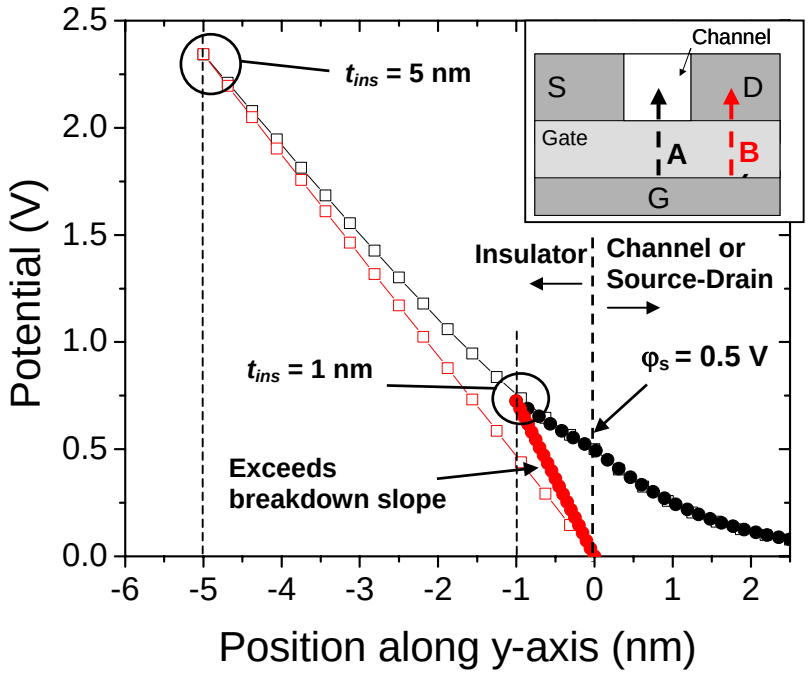


Figure 2.7. Potential along lines A (black) and B (red) (inset) for SiO_2 gate insulators with t_{ins} = 5 nm (hollow) and 1 nm (solid). The channel length is 4 nm. In both cases the applied gate voltage is sufficient to obtain φ_s = 0.5 V. For t_{ins} = 1 nm, the slope of the potential along line B exceeds the breakdown field of 0.5V/nm.

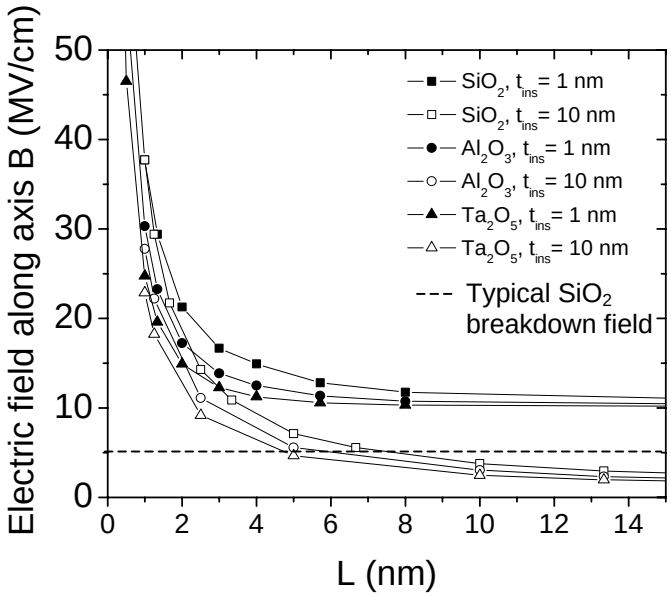


Figure 2.8. Average electric fields along axis B (inset, Figure 2.7) necessary to obtain $\Delta\varphi_s$ = 1 vs *L* for different gate dielectrics of thickness 1 and 10 nm. A typical breakdown field (5 MV/cm) for SiO_2 is also shown. SiO_2 structures with t_{ins} = 10 nm and *L* > 4 nm will be able to modulate φ_s by 1 V without insulator breakdown.

silicon because of longer channels and lower required $\Delta\varphi_s$ [21].

These results indicate that increasing t_{ins} is (counter intuitively) the optimal approach to obtain a gating effect, although this decreases the transistor transconductance. We can use this constraint of dielectric breakdown in the gate-drain region to determine if, for a given channel length, it is possible (with appropriate choice of gate insulator thickness) to modulate the channel potential by 1 V. For example, with *L* = 2 nm, $\Delta\varphi_s$ of 1 V would require an SiO_2 field of 18-22 MV/cm regardless of the gate insulator thickness, well beyond breakdown (~5 MV/cm in SiO_2) (Fig. 2.8). If *L* is increased to 5 nm, a field of 15 MV/cm is required if t_{ins} = 1 nm, but with a thicker t_{ins} = 10 nm the field decreases to ~5 MV/cm, near breakdown. Insulators with high dielectric constants do not provide a significant advantage. Although the required electric fields in Al_2O_3 and Ta_2O_5 are lower than in SiO_2, this advantage is offset by lower breakdown fields (~ 3 MV/cm for Ta_2O_5) [22]. It will thus be very difficult to modulate the channel potential of device with *L* < 5 nm by 1 V, regardless of the gate insulator material or thickness.

We finally discuss the importance of two assumptions made in this discussion. The first is that we could calculate the electrostatic potential in the nanometer scale device using a classical treatment. For example, the gate insulator and molecular channel were treated as uniform insulators characterized only by a dielectric constant, which is a macroscopic property that is only well defined for bulk materials [23]. In particular, this implies that for an applied voltage between source and drain electrodes (with no gate field) the potential in the channel decreases linearly. However, theoretical modeling suggests that the electrostatic potential inside of a biased molecular junction is highly nonuniform, and most of the potential drop is likely to occur near where the molecular layer contacts the source and drain electrodes [24-27]. A more realistic calculation of the channel potential would therefore require use of a charge-screening model [25] or preferably simultaneous solution of Poisson's equation and the Schrödinger equation [28].

A second assumption that we made was that variations of the surface potential of the organic layer on the order of 1 V will be required to obtain transistor action. Molecules with smaller bandgaps (or closer alignment of molecular levels to source and drain Fermi levels) will clearly relax the design requirements. Still, a substantial offset in the molecular levels with respect to source and drain Fermi levels is necessary to avoid undesired thermal excitation of carriers into molecular transport levels leading to large transistor OFF currents. Tuning of energy level alignment may therefore improve transistor performance but is not expected to fundamentally change the results discussed in this chapter.

2.4 Summary and Conclusions

Molecular-scale FETs may allow shrinking of device dimensions to several nm, enabling highly scaled electronic circuits. However, the unusual geometry of monolayer FETs, which is a result of their ultrashort channel lengths, can inhibit the ability of the gate to modulate the channel potential for transistor action due to electrostatic coupling between the channel and source and drain. This chapter has analyzed molecular-scale FET operation from an electrostatics perspective to determine scaling guidelines for FETs with these unique geometries. The main results are:

(i) Contrary to expectations, the gate insulator thickness should not be scaled to very short dimensions to obtain a maximum modulation of the surface potential. For a fixed gate field, thicker gate insulators allow maximum modulation of the channel potential.

(ii) Although high-κ gate dielectrics may allow increased gate-channel coupling, this advantage is offset in practice by lower breakdown fields.

(iii) Regardless of the choice of gate insulator, it will be very difficult to modulate the channel potential by 1 V for channels less than 5 nm in length.

These results indicate that an optimal approach to realizing monolayer and single-molecule FETs is to use relatively long molecules (> 5 nm) and avoid ultrathin gate insulators. This will allow maximum gate modulation of the surface potential of the organic layer, although the gate-channel coupling efficiency may be relatively low, limiting the transconductance.

Although molecular-scale FETs will allow three-terminal probing of the fundamental electrical properties of single molecules and molecular layers, the low transconductance of monolayer FETs may limit their technological impact. Two-terminal molecular-scale devices may therefore ultimately be of more technological interest.

References

[1] J. O. Lee, G. Lientschnig, F. Wiertz, M. Struijk, R. A. J. Janssen, R. Egberink, D. N. Reinhoudt, P. Hadley and C. Dekker, "Absence of Strong Gate Effects in Electrical Measurements on Phenylene-Based Conjugated Molecules" *Nano Letters* **3** (2), 113-117 (2003).

[2] N. B. Zhitenev, H. Meng and Z. Bao, "Conductance of Small Molecular Junctions" *Physical Review Letters* **88** (22), 226801 (2002).

[3] D. GoldhaberGordon, M. S. Montemerlo, J. C. Love, G. J. Opiteck and J. C. Ellenbogen, "Overview of Nanoelectronic Devices" *Proceedings of the IEEE* **85** (4), 521-540 (1997).

[4] W. J. Liang, M. P. Shores, M. Bockrath, J. R. Long and H. Park, "Kondo Resonance in a Single-Molecule Transistor" *Nature* **417** (6890), 725-729 (2002).

[5] J. Park, A. N. Pasupathy, J. I. Goldsmith, C. Chang, Y. Yaish, J. R. Petta, M. Rinkoski, J. P. Sethna, H. D. Abruna, P. L. McEuen and D. C. Ralph, "Coulomb

Blockade and the Kondo Effect in Single-Atom Transistors" *Nature* **417** (6890), 722-725 (2002).

[6] N. B. Zhitenev, A. Erbe, H. Meng and Z. Bao, "Gated Molecular Devices Using Self-Assembled Monolayers" *Nanotechnology* **14** (2), 254-7 (2003).

[7] S. Hong, R. Reifenberger, W. Tian, S. Datta, J. I. Henderson and C. P. Kubiak, "Molecular Conductance Spectroscopy of Conjugated, Phenyl-Based Molecules on Au(111): The Effect of End Groups on Molecular Conduction" *Superlattices and Microstructures* **28** (4), 289-303 (2000).

[8] Y. Taur, *Fundamentals of Modern VLSI Devices*. 1998, New York: Cambridge University Press. 469.

[9] S. Thompson, P. Packan and M. Bohr, "MOS Scaling: Transistor Challenges for the 21st Century" *Intel Technology Journal* **2** (3)(1998).

[10] J. H. Schon, H. Meng and Z. N. Bao, "Self-Assembled Monolayer Organic Field-Effect Transistors (Vol 413, Pg 713, 2001)" *Nature* **422** (6927), 92-92 (2003).

[11] J. H. Schon, H. Meng and Z. Bao, "Field-Effect Modulation of the Conductance of Single Molecules (Vol 294, Pg 2138, 2001)" *Science* **298** (5595), 961-961 (2002).

[12] J. H. Schon and Z. Bao, "Nanoscale Organic Transistors Based on Self-Assembled Monolayers (Retracted Article. See Vol 82, Pg 1313, 2003)" *Applied Physics Letters* **80** (5), 847-849 (2002).

[13] J. H. Schon and Z. Bao, "Organic Insulator/Semiconductor Heterostructure Monolayer Transistors" *Applied Physics Letters* **80** (2), 332-333 (2002).

[14] J. H. Schon, H. Meng and Z. N. Bao, "Field-Effect Modulation of the Conductance of Single Molecules" *Science* **294** (5549), 2138-2140 (2001).

[15] J. H. Schon, H. Meng and Z. N. Bao, "Self-Assembled Monolayer Organic Field-Effect Transistors (Vol 413, Vol 713, 2001)" *Nature* **414** (6862), 470-470 (2001).

[16] S. Sze, *Physics of Semiconductor Devices*. 2nd ed. 1981, New York: John Wiley and Sons.

[17] G. Brumfiel, "Misconduct Finding at Bell Labs Shakes Physics Community" *Nature* **419**, 419-421 (2002).

[18] R. Haag, M. A. Rampi, R. E. Holmlin and G. M. Whitesides, "Electrical Breakdown of Aliphatic and Aromatic Self-Assembled Monolayers Used as Nanometer-Thick Organic Dielectrics" *Journal of the American Chemical Society* **121** (34), 7895-7906 (1999).

[19] G. D. Wilk, R. M. Wallace and J. M. Anthony, "High-Kappa Gate Dielectrics: Current Status and Materials Properties Considerations" *Journal of Applied Physics* **89** (10), 5243-5275 (2001).

[20] A. Ulman, "Formation and Structure of Self-Assembled Monolayers" *Chemical Reviews* **96** (4), 1533-1554 (1996).

[21] B. G. Streetman and S. Banerjee, *Solid State Electronic Devices*. 5 ed. 2000, Upper Saddle River, NJ: Prentice Hall.

[22] J. W. McPherson, J. Kim, A. Shanware, H. Mogul and J. Rodriguez, "Trends in the Ultimate Breakdown Strength of High Dielectric-Constant Materials" *IEEE Transactions on Electron Devices* **50** (8), 1771-1778 (2003).

[23] D. J. Griffiths, *Introduction to Electrodynamics*. 3rd ed. 1999, Upper Saddle River: Prentice Hall.

[24] Y. Xue, S. Datta and M. A. Ratner, "Charge Transfer And "Band Lineup" In Molecular Electronic Devices: A Chemical and Numerical Interpretation" *Journal of Chemical Physics* **115** (9), 4292-4299 (2001).

[25] A. Nitzan, M. Galperin, G.-L. Ingold and H. Grabert, "On the Electrostatic Potential Profile in Biased Molecular Wires" *Journal of Chemical Physics* **117** (23), 10837-10841 (2002).

[26] S. Datta, W. Tian, S. Hong, R. Reifenberger, J. I. Henderson and C. P. Kubiak, "Current-Voltage Characteristics of Self-Assembled Monolayers by Scanning Tunneling Microscopy" *Physical Review Letters* **79** (13), 2530-2533 (1997).

[27] W. Tian, S. Datta, S. Hong, R. Reifenberger, J. I. Henderson and C. P. Kubiak, "Conductance Spectra of Molecular Wires" *Journal of Chemical Physics* **109** (7), 2874-2882 (1998).

[28] V. Mujica, A. E. Roitberg and M. A. Ratner, "Molecular Wire Conductance: Electrostatic Potential Spatial Profile" *Journal of Chemical Physics* **112** (15), 6834-6839 (2000).

Chapter 3

Growth and Characterization of MUA Self-Assembled Multilayer Films

3.1 Introduction

This chapter describes the growth and characterization of thin, self-assembled multilayer films of the molecule 11-mercaptoundecanoic acid (MUA) on gold substrates. These films comprise the active layer in most of the electronic devices fabricated and tested in this thesis. Self-assembled films of MUA on gold were chosen for detailed study for several reasons. First, MUA can be grown layer by layer (as described in Section 3.3) to allow a wide range of device characteristics to be explored. This range includes highly scaled devices containing a single layer to thicker, bulk-like films with many MUA layers. The ability to fabricate devices with thick films is useful because of the difficulty of forming a top metal contact to monolayer devices without causing electrical shorts, as discussed in Chapter 4. Experimentally, thick and robust films enable quick testing and development of device structures; as fabrication techniques are refined the number of MUA layers can then be decreased with minimal process modification to fabricate monolayer devices.

The second reason that MUA was chosen for detailed study is that its self-assembly process uses relatively common and straightforward chemistry. Self-assembly of the MUA on the gold substrate is driven by the attachment of a thiol group on the molecule to the gold surface. Thiolate-gold chemistry is the most widely used basis for growing self-assembled layers [2, 3]. Gold is often preferred over other substrate materials because its resistance to oxidation ensures a relatively stable platform for self-assembly [4]. The strength of the thiolate-gold bond (1.9 eV) also contributes to the stability of self-assembled layers on gold [5]. Finally, the chemical processes required to grow the layers are relatively simple, requiring only a wet-bench, ethanol, and de-ionized water. These factors simplify device processing and also allow many of the results of this thesis to be more readily applicable to the wide range of systems that also employ thiolate-gold chemistry.

The third advantage of MUA multilayer films is that they will in principle enable better gate-channel coupling in molecular-scale FETs. As discussed in Chapter 2, the ultrashort channel lengths make it difficult for the gate of monolayer FETs to modulate the surface potential of the channel (monolayer) by an amount sufficient for transistor action. Monolayers thicker than 5 nm should have the best possibility of demonstrating transistor action; however, it is difficult to synthesize and self-assemble molecules of this length [6]. Self-assembled multilayers offer an alternative approach to fabricating molecular-scale transistors with channel lengths greater than 5 nm.

Finally, although we will show later that MUA can be used as the active layer in programmable-resistance memory devices, we note that MUA was not studied because of any intrinsic properties that were expected to allow it to be used as the active layer in future devices. Indeed, as will be discussed in Chapter 8, we think the programmable resistance of our devices is due to the injection of metal from the electrodes into the MUA film, and not the MUA film itself (although we will show that several of the characteristics of MUA are desirable for optimal device operation). Consisting of an alkane chain, MUA was predicted to form a simple insulating film for testing of different device structures. We anticipated eventually replacing MUA with multiple self-assembled layers of alternative molecules (such as conjugated 4,4'-dimercaptobiphenyl) that use similar growth chemistries [7]. This would allow us to retain the developed device structures as well as the advantages of a self-assembled multilayer film when fabricating devices for more practical application.

Study of MUA multilayer films grown on gold was therefore motivated by the range of electrical characteristics that can be explored, the common and straightforward chemistry of the MUA growth process, and the possibility of eventually making molecular-scale FETs with multilayer channels. This chapter describes the growth and characterization of MUA films on gold. In Section 3.2, two techniques for depositing the gold substrate are described. Growth of MUA multilayer films on these gold substrates is described in Section 3.3. In Section 3.4, these films are characterized by ellipsometry, Rutherford backscattering (RBS), atomic force microscopy (AFM), and ultraviolet photoelectron spectroscopy (UPS). The chapter is summarized in Section 3.5.

3.2 Deposition of Gold Substrates*

Because of the very thin (1-2 nm) nature of most self-assembled monolayers, the surface features of the substrate on which the film grows can play a critical role in the quality of the monolayer [8]. Vacuum deposition of gold results in a polycrystalline thin film. To grow monolayers with very few defects, these films should have relatively large, atomically flat regions. However, the most common methods of evaporating gold films, by room-temperature electron-beam or thermal evaporation, result in relatively rough films with grain sizes of only 15 – 25 nm, independent of the substrate onto which the film is deposited [9]. One well-known approach to improve the crystallinity of vacuum-deposited gold films is to heat the substrate (typically to 200 to 300° C) during and/or after gold deposition [10-13]. This approach was not pursued for two reasons. First, from a practical perspective our vacuum evaporation chamber was not equipped with a substrate heater. More importantly, because the increased crystallinity is due to larger grain sizes, the surface roughness of the film can increase significantly. Alternative, template-stripping approaches have thus become the preferred method of forming ultraflat gold surfaces for the growth of self-assembled organic layers [14].

In the template-stripping approach, a thin layer of gold is vacuum deposited onto an atomically flat substrate that serves as a template (Fig. 3.1(a)). This substrate is often freshly-cleaved mica (heated to 300 °C during deposition of the gold) [15], although Si substrates covered with a thin layer of SiO_2 can also be used (without heating) [13, 16, 17]. After evaporation, the gold film is then attached to a target substrate with epoxy to provide a mechanical support for the fragile film (Fig. 3.1(b)).

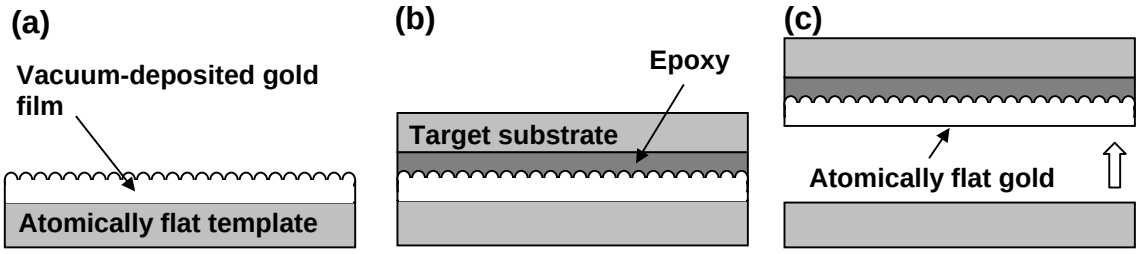


Figure 3.1. Preparation of template-stripped gold film. (a) Thin gold film is vacuum deposited on atomically flat template (mica or SiO_2). (b) Gold film is glued to target substrate. (c) Target substrate is peeled away from template to reveal atomically flat gold.

* Please refer to Appendix B for additional experimental details.

Finally, the film is peeled from the template to reveal the atomically-flat gold surface that had been in contact with the template (Fig. 3.1(c)). Because the mica (or SiO_2 film) and gold are inert, the gold does not adhere to the template and can be stripped without requiring a chemical etch or ultrasonic agitation.

Both direct thermal evaporation and template-stripping were used to prepare gold films in this thesis. To prepare directly deposited gold films, a Si substrate (with native oxide) was cleaned by acetone in an ultrasonic bath then rinsed with isopropanol and promptly loaded into a thermal evaporator. At a base pressure of 10^{-6} torr, 5 nm layers of Ti (for adhesion) and then gold (80-100 nm) were evaporated onto the Si at rates of 0.1 to 0.5 nm/s. In these evaporations the temperature of the Si substrate was not controlled (so was roughly equal to room temperature).

Si wafers with a thin oxide layer were used as a template for preparation of flat gold because of their wide availability, and the need to heat mica substrates to 300 °C during gold deposition would have required the addition of a substrate heater to our vacuum deposition chamber. Preparation began with cleaning of a 4" Si wafer with acetone and isopropanol rinses, followed by a piranha clean (1:1 sulfuric acid and hydrogen peroxide (30% in water) for 15 min) to grow a thin layer of SiO_2 on the Si wafer. The thin silicon oxide layer is necessary to prevent gold-silicon bonding during the thermal evaporation [16]. Immediately after cleaning, the wafer was placed in an e-beam evaporator. A ~100 nm film of gold was deposited at a base pressure of 10^{-6} torr at an evaporation rate of 0.1 to 0.5 nm/s (without heating the silicon wafer). After removing the sample from the evaporator, a two-part epoxy, EPO-TEK 377 (obtained from Epoxy Technology, Inc.) was used to glue either Si or glass target substrates to the top of the gold film. EPO-TEK 377 was chosen because of its resistance to the organic solvents used in the growth of the self-assembled layers [16]). The epoxy was cured by heating the wafer on a hotplate at 130 °C for > 2 hours. To strip the target substrate from the template, it was only necessary to apply slight initial pressure to the edge of the substrates with a razor blade (without chemical processing). All preparation was done in the Princeton Institute for the Science and Technology of Materials (PRISM) cleanroom to minimize particle contamination of the template/flat-gold surface.

For brevity, we will refer to directly deposited films as "regular", and template-stripped films as "flat". For both regular or flat gold films, monolayer growth or surface

analysis (by ellipsometry or AFM) was performed immediately after removing the films from vacuum (for regular films) or stripping from the template (for flat films) to minimize contamination of the gold surface. The results of the surface analysis of the bare gold are presented in Section 3.4.

3.3 Growth of MUA Multilayer

Self-assembled multilayers of MUA were grown on gold substrates following a procedure that was demonstrated to us by Dr. Zhenan Bao (Bell Laboratories, Lucent Technology, Murray Hill, NJ; presently an Associate Professor of Chemical Engineering at Stanford University, Stanford, CA). This approach to self-assembled multilayer growth was originally described by Evans et al [18]. An RCA-1 clean (5:1:1 deionized water, hydrogen peroxide (30% in water), and ammonium hydroxide, heated to ~70 °C for 20 minutes) was used to clean all glassware prior to use. 1 mM solutions of MUA ($C_{11}H_{22}O_2S$, 95%, purchased from Aldrich) in ethanol (anhydrous, 99.5+%, purchased from Aldrich) were prepared by dissolving 0.013 g of MUA in 60 mL of ethanol. 1 mM solutions of copper(II) perchlorate hexahydrate ($Cu(ClO_4)_2*6H_2O$, 98%, purchased from Aldrich) in ethanol were prepared by dissolving 0.022 g of $Cu(ClO_4)_2$ in 60 mL of ethanol.

Growth of multiple layers of MUA consisted of the following steps:

1. Freshly deposited (or template-stripped) gold substrates were immersed in MUA solution for 2 to 24 hours to grow the first monolayer of MUA (Fig. 3.2(a)).

2. The samples were rinsed in a sequence of ethanol, deionized water, and then ethanol, without drying. We found that a thorough second ethanol rinse was critical for removing deionized water from the substrate prior to immersion in the $Cu(ClO_4)_2$ solution. As discussed in further detail in Section 3.4.1, inadvertent introduction of water to the $Cu(ClO_4)_2$ solution led to undesired multilayer deposition.

3. The substrates were placed in the $Cu(ClO_4)_2$ solution for 5 min to deposit a layer of Cu^{2+} ions on the MUA layer (Fig. 3.2(b)).

4. The samples were rinsed thoroughly in ethanol, without drying.

5. The samples were returned to the MUA solution for 2 to 24 hours to grow a second layer of MUA on top of the Cu^{2+} (Fig. 3.2(c)).

Steps 2 through 5 could be repeated to grow an arbitrary number of MUA layers. After growing several MUA layers, the MUA and $Cu(ClO_4)_2$ solutions were replaced with fresh solutions to minimize the possibility of inadvertent cross-contamination. The length of the immersion in MUA solution did not have an observable effect over the 2 to 24 hour range that we studied. A standard growth time for each MUA layer was ~ 3 hours; however, when growing films with many MUA layers it was common to grow one of the MUA layers overnight (or over a portion of the weekend), resulting in much longer immersion times of up to 24 hours. When film growth was complete, the samples were removed from solution, rinsed in ethanol and water, and then dried in a stream of nitrogen gas. If dried samples required storage for more than several minutes before starting another process step, they were placed in a Vacuum Atmospheres glovebox having an inert nitrogen atmosphere (< 1 ppm water and oxygen) to avoid oxidation of the thiolate groups [19].

Following several experimental studies, the chemistry of this process is mostly understood, although some questions remain [18, 20-23]. Relatively long immersion times in the MUA solution allow the formation of a higher-quality monolayer.

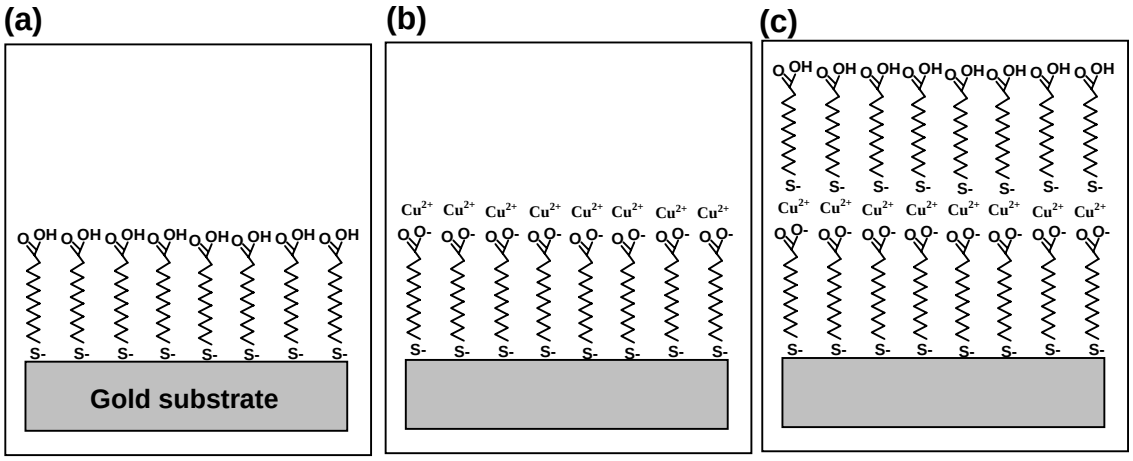


Figure 3.2. Schematic of MUA multilayer growth. (a) Upon immersion of a gold substrate in MUA solution, a monolayer of MUA grows on the gold. (b) The sample is placed in $Cu(ClO_4)_2$ solution to deposit Cu^{2+} ions on the MUA monolayer. (c) When the sample is returned to the MUA solutions, thiol endgroups bind to the copper leading to the growth of a second MUA layer (with the same orientation as the first). The actual stoichiometry of the Cu-MUA bonds may be more complicated than the indicated 1:1 ratio.

Experiments indicate that monolayers typically reach 90% of their final thickness within the first minute of growth, but it can take several hours for the remaining defects to be annealed and the layer to reach its full thickness [24]. Although the COO^- group on MUA can bond to gold, the thiolate-gold bond is energetically favored so the vast majority of molecules will attach to the gold via the sulfur, as depicted in Fig. 3.2(a); this conclusion is supported by XPS measurements [18]. Most XPS measurements also indicate that Cu is deposited on the MUA as Cu^{2+}, and upon re-immersion in MUA the thiol endgroup binds to the Cu layer so that all of the MUA layers have the same orientation [20, 22]. However, there is some disagreement regarding the exact bonding between the COO^-, Cu, and S groups that form the linkages between MUA layers, so that the 1:1:1 binding depicted in Fig. 3.2(c) may be inaccurate. Some groups have reported that the Cu remains in the 2+ oxidation state [22], while others suggest that it is reduced to a 1+ state when it binds to the second MUA layer [20]. One XPS study indicated that the ratio of copper ions to molecules is approximately 1 to 2.5, although other measurements suggested an even higher ratio of 1 to 4 [22]. In contrast, our measurements using RBS (Section 3.4.2) suggest a 1:1 ratio of Cu to molecules as indicated in Fig. 3.2(c).

3.4 Characterization of MUA Multilayers and Gold Substrates

3.4.1 Ellipsometry

Ellipsometry was used extensively, both as a means to determine the thickness of the layers and most frequently as a way to monitor the deposition of MUA layers on batches of samples during the growth process. All ellipsometric measurements were performed with a Gaertner Scientific L3W16 ellipsometer at a wavelength of 632.8 nm, with an angle of incidence of 70° and polarizer angle of 45°. The ellipsometer was powered on at least 15 minutes prior to measurements to allow the laser to stabilize. The ellipsometric constants Ψ and Δ were collected at 5 to 7 different locations on each sample. In the case of the bare gold substrate, these measurements were used to directly fit (using the Gaertner software program) an average value for n_s and k_s, the real and imaginary components of the substrate's complex index of refraction. For the MUA film, the extraction of average values of the film thickness t and the optical constants of the film, n_f and k_f, from the measured values of Ψ and Δ was slightly more complicated. For an optically transparent film on a reflecting substrate, the measured

values of Ψ and Δ depend on 5 parameters: t, n_f, k_f, n_s, and k_s. To calculate t (the parameter of interest), n_s, and k_s were fixed at values previously measured on a bare gold substrate, n_f was fixed to the expected value of 1.45, and t and k_f were varied (by the software program) to obtain the best fit to the parameters Ψ and Δ [25]. The best-fit value for k_f was generally near 0, as expected for an alkane chain [26].

Because of the thin nature of the MUA films that we studied, the accurate extraction of their properties was very sensitive to an accurate measurement of the properties of the gold substrate. All measurements on bare gold substrates were made within 5 to 10 min of exposing the gold to atmosphere to avoid surface contamination (measurements on samples with MUA layers were also made within 5 to 10 minutes of removal from solution for the same reason). Average values of n_s and k_s for bare gold were 0.16 and 3.53. However, the optical constants of bare gold varied slightly (between n_s = 0.14 to 0.22, and k_s = 3.47 to 3.60) for gold prepared at different times. A gold sample prepared at the same time as the gold substrates used in the MUA growth was therefore always measured to determine the values of n_s and k_s that were used to calculate the MUA film thickness.

Ellipsometry measurements revealed a linear increase in the film thickness with number of layers for up to at least 12 MUA layers (Fig. 3.3). Film thicknesses measured on flat and regular gold substrates were similar. The slope in Figure 3.3 indicates an average thickness of 1.6 nm/layer, which is in reasonable agreement with previous measurements (1.4 nm/layer [18]) and estimates of the thickness of the MUA layer based on the bond lengths of the molecule (1.58 nm, neglecting the Cu interlayers and assuming that the MUA stands perpendicular to the gold surface). The similarity between the measured thickness and molecular length suggests that the MUA is forming dense, close-packed layers that are oriented nearly vertically. If there were a large number of vacancies or if the molecules were highly tilted, a lower average thickness would be obtained. However, more accurate techniques such as Fourier transform infrared (FTIR) spectroscopy would be needed to measure the tilt angle of the MUA films.

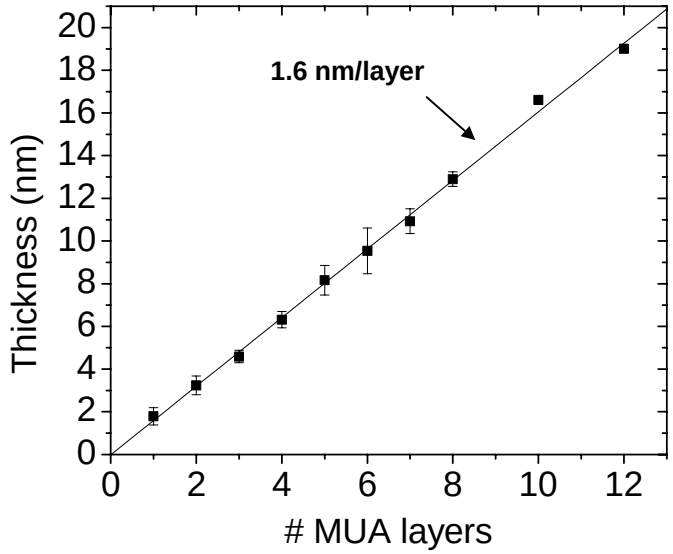


Figure 3.3. Thickness (determined by ellipsometry) vs # of MUA layers for MUA deposited on regular gold substrates. The slope corresponds to 1.6 nm/layer. Measured thicknesses and error bars (below 8 MUA layers) are the average and standard deviation of measurements on at least 5 separate samples (and on each sample 5 to 7 locations were measured to determine an average sample thickness); for 10 and 12 MUA layers only 5 to 7 locations on one sample were measured.

The general consistency of the relationship between thickness and number of MUA layers shown in Figure 3.3 allowed occasional problems with the MUA growth to be detected by checking the thickness of the film during the growth. A common problem is revealed in Figure 3.4. In this instance, during the growth of a 13-layer film, after 8 MUA layers the thickness of subsequent layers increased dramatically to 3 nm/layer. Similar transitions to faster growth regimes were often observed, typically after the growth of 6 to 8 MUA layers. It is likely that the reason for the fast growth was accidental introduction of water into the $Cu(ClO_4)_2$ solution. If a small amount of deionized water (~1% by volume) was intentionally added to the $Cu(ClO_4)_2$ solution during MUA growth, similar growth rates of ~ 3 nm/layer were observed (Figure 3.4). A possible reason for the enhanced growth is that the water may hydrolyze the $Cu(ClO_4)_2$ to make a compound such as $Cu(OH)_x$, which could form a multilayer itself [27]. To avoid this undesired multilayer growth, in later MUA growths samples were rinsed in ethanol very thoroughly prior to immersion in $Cu(ClO_4)_2$ solution to remove any water,

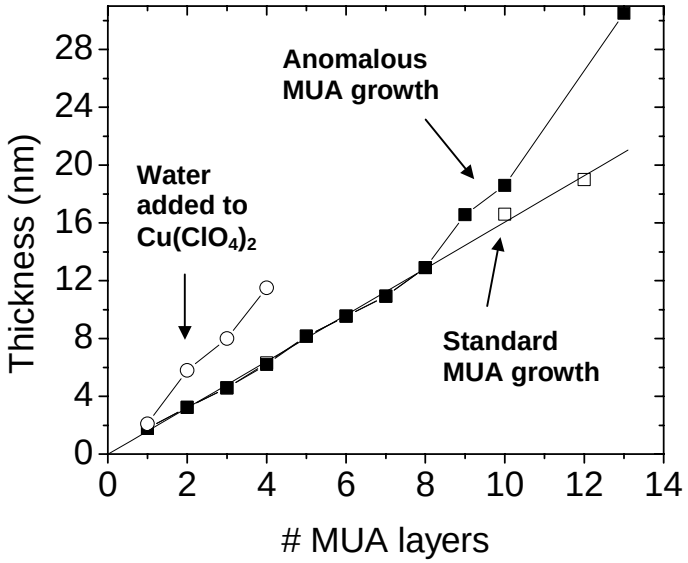


Figure 3.4. Example of anomalous MUA growth in which the apparent layer thickness increases from 1.6 nm/layer to 3 nm/layer after 8 MUA layers (solid squares). For comparison, a MUA growth in which water was added to the $Cu(ClO_4)_2$ solution (hollow circles) and the standard MUA growth plot (from Figure 3.3) (hollow squares) are also shown.

and both MUA and $Cu(ClO_4)_2$ solutions were changed frequently (after every 2 to 3 layers of MUA). This practice led to more consistent MUA growth rates.

3.4.2 Rutherford Backscattering

RBS was used to estimate the density of molecules and copper atoms in each layer and to determine the amount of Cu per molecule in each of the MUA-Cu bilayers. RBS measurement and analysis was performed by Dr. Michael Strathman at Thin Film Analysis, Inc. (San Jose, CA), using a 2.3 MeV He++ beam with the ion detector located at 170°. MUA films of several different thicknesses were prepared for the analysis in the standard manner on regular gold (25 to 50 nm thick) films. The density of copper atoms in each layer was determined directly from analysis of the RBS spectra, while the density of MUA molecules was determined by measuring the amount of sulfur (there is one S atom in each MUA molecule). As expected, both S and Cu densities increased linearly with the number of MUA layers (Fig. 3.5). The slope of the

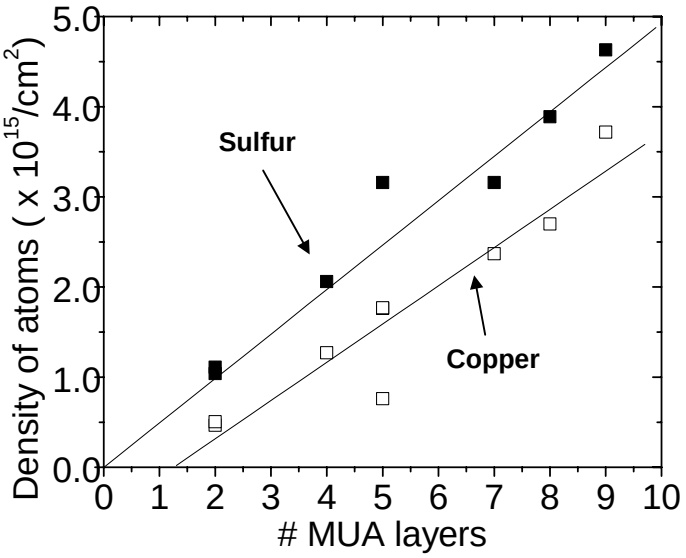


Figure 3.5. Area density of sulfur and copper atoms vs number of MUA layers as determined by RBS. The density of MUA is equivalent to the sulfur density.

S data, 5 x 10^{14} atoms/cm^2/layer, is similar to the density expected for a close-packed layer of MUA (4.6 x 10^{14} atoms/cm^2 in the case of the similar molecule $CO_2H(CH_2)_{15}SH$) [28]. Like the ellipsometry measurement, this confirms that the MUA layer does not have a large number of vacancy defects and is instead densely packed.

The slope of the Cu data (4 x 10^{14} atoms/cm^2/layer) indicates a density of Cu that is similar to that of MUA. This contradicts previous XPS measurements, which suggested that there is only 1 Cu/2.5 molecules as discussed in Section 3.3 [22]. The nearly 1:1 ratio that we measure (4 x 10^{14}/5 x 10^{14} = 0.8 Cu/molecule) suggests that the schematic in Fig. 3.2(c) may accurately represent the bonding in the MUA layer. In this relatively simple understanding, one Cu^{2+} bonds directly to a COO^- and S^- group. One problem with this picture is that this would require the presence of a monolayer of positive charge during deposition of the Cu^{2+}, which would initially bind only to a COO-. The extent to which this charge might be screened by the solution is unclear. Furthermore, a 1:1 ratio of Cu to MUA is consistent with alternative oxidation and bonding schemes [23]. Further work would therefore be necessary for an explicit understanding of the nature of the bonding between Cu and MUA layers.

3.4.3 Atomic Force Microscopy

AFM was used to characterize the roughness of films having different numbers of MUA layers. For molecular-scale films, surface roughness can play a critical role in determining electrical characteristics. For example, if the roughness of the film is comparable to the thickness of the film, this may indicate the presence of defects such as pinholes that would lead to electrical shorting. All AFM images were recorded with a Digital Instruments Dimension 3100 AFM in tapping or noncontact mode. NSC14 or NSC15 silicon cantilevers, ordered from Mikromasch, with resonant frequencies between 110-220 or 265-400 kHz, respectively, were used in all scans. Similar results were obtained for both operating modes and tips, so the specific conditions under which the images and data in this section were taken will not be specified. To confirm that the noncontact and tapping mode images were due to the MUA layer and not artifacts, a single-layer MUA sample on flat gold was examined with contact-mode AFM by Ying Hu in the lab of Professor Giacinto Scoles in the Chemistry Department at Princeton University. Surface roughness and peak-to-valley distances measured in this mode were very similar to ones measured on the same sample in noncontact and tapping modes, indicating that any measurement artifacts in these modes are very limited.

AFM images of bare gold samples reveal significant differences between gold deposited by thermal evaporation (regular) and template-stripped (flat) gold. The surface of thermally evaporated, regular gold was relatively rough, with grain sizes of 25-50 nm, and surface variations of ~ 1 nm RMS and peak-to-valley (PV) ranges of ~11 nm (for a 3 micron scan) (Fig. 3.6(a)). These characteristics are typical of gold evaporated at room temperature [9]. Template-stripped, flat gold had much larger flat regions up to 400 nm in size, and much lower surface variations of <0.3 nm RMS and 5 nm peak-to-valley (PV) (Fig. 3.6(b)). Most of the surface variation on flat gold samples was due to the large crevices between the flat regions. If the surface variation was measured only in the flat regions, values of <0.1 nm RMS and 1-3 nm PV were often obtained.

AFM topographical images of regular and flat gold samples with 0, 1, and 4 layers of MUA are shown in Figure 3.7. Due to the roughness of the regular gold and its small grain size, the effect of the MUA layer on the topography is difficult to discern. The effect of the MUA layer is more apparent in the images on flat gold, where the texture of the first MUA layer is clearly visible. The underlying features of the gold

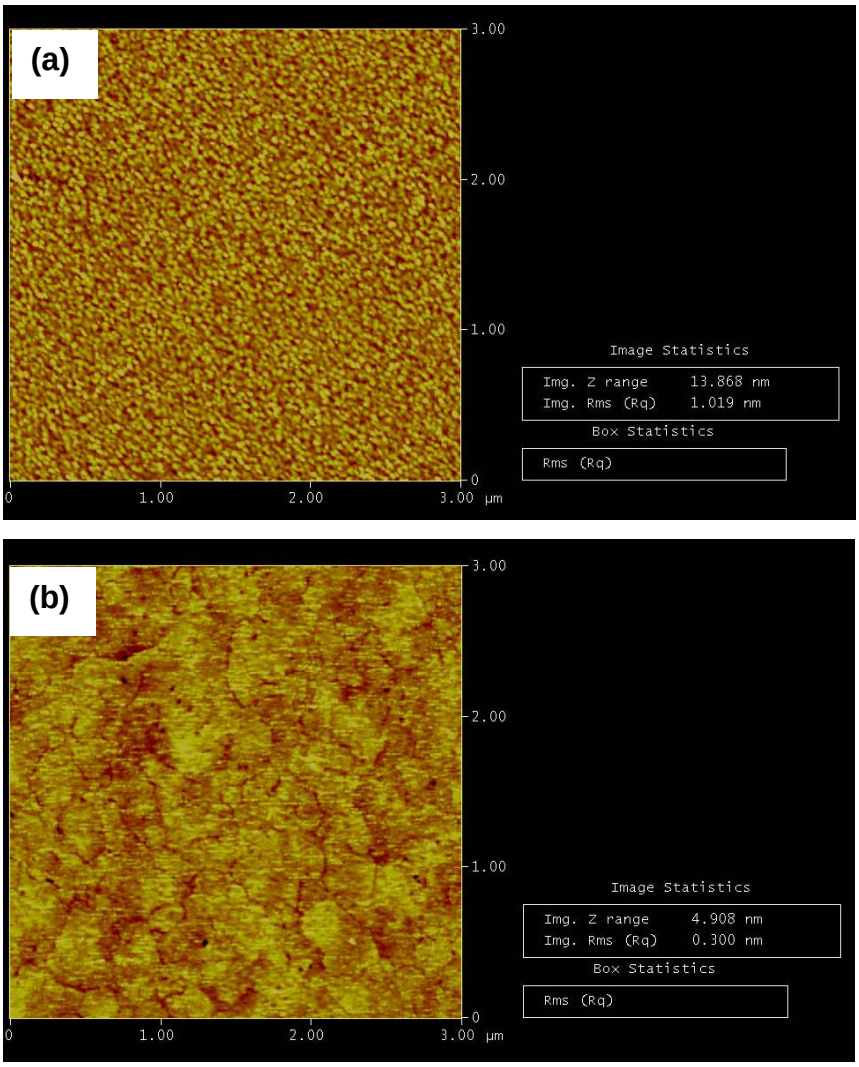


Figure 3.6. 3 µm AFM scans of (a) regular and (b) flat gold.

substrate remain visible until after 4 layers of MUA, at which point the features of the MUA dominate.

The roughness of the regular gold substrate makes it difficult to determine the actual roughness of the MUA layer on these substrates. Therefore, RMS and PV roughness as a function of number of MUA layers was measured primarily in the large flat regions (shown in Fig. 3.7) of template-stripped gold samples. The relatively smooth bare gold in these regions (<0.1 nm RMS and 1-3 nm PV) allowed a more direct measurement of the roughness that is intrinsic to the MUA film. Average

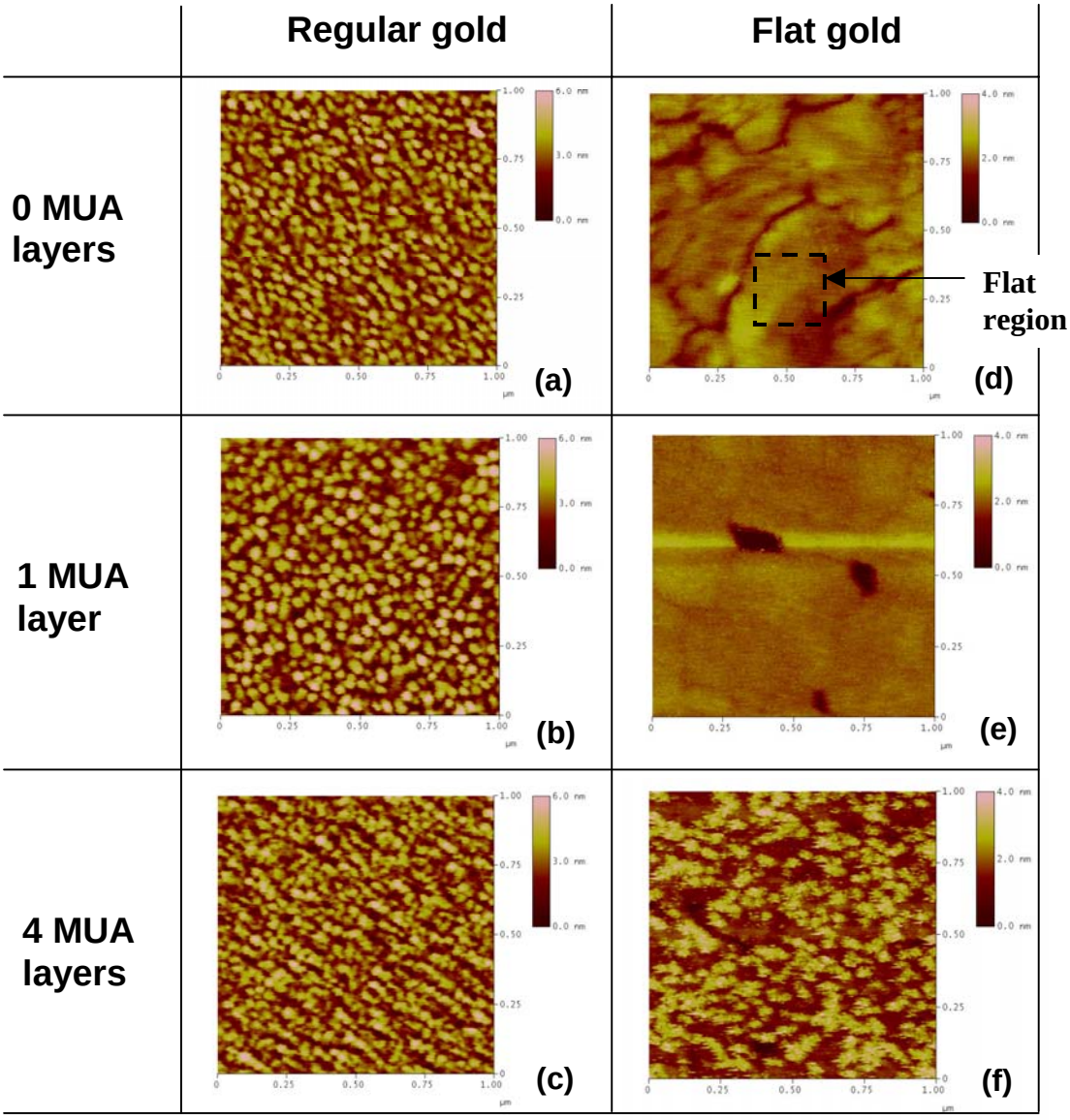


Figure 3.7. 1 x 1 μm^2 AFM topographical images of MUA on regular and flat gold. (a) Bare regular gold. (b) 1 MUA layer on regular gold. (c) 4 MUA layers on regular gold. (d) Bare flat gold. (e) 1 MUA layer on flat gold. (f) 4 MUA layers on flat gold. All scans on regular gold are shown on a 6 nm scale, while scans on flat gold are shown on a 4 nm scale. In (d), we show an example of a flat region where roughness (for Figure 3.8) was measured.

roughness values for different numbers of MUA layers were determined by measuring the roughness in 4 to 5 different flat regions on 2 to 3 different samples for each thickness (so that each average value represents 8 to 12 different measurements). For comparison, roughness measurements for single, 1-μm scans on MUA grown on regular gold were also recorded. For both regular and flat gold, the RMS and PV surface roughness generally increased with the number of MUA layers (Fig. 3.8, (a) and (b)). RMS values for MUA on regular gold were relatively high, starting at 1 nm for bare gold and increasing linearly with a slope of 0.1 nm/layer. RMS values for MUA on flat gold were much smaller, starting at 0.1 nm for bare gold, then increasing linearly with a slope of 0.08 nm/layer, which is similar to the slope measured on regular gold. PV values displayed similar behavior, increasing with slopes of 1.6 nm/layer and 0.8 nm/layer for MUA on regular and flat gold, respectively. One interesting feature in the regular gold data is that the PV roughness actually decreases with the addition of the first MUA layer, from 11 nm to 8 nm. This suggests that the MUA may actually cause some smoothing of the surface.

Two quantities that are better indicators of the possibility of pinholes in the film are the RMS and PV roughness of the MUA films divided by the total thickness of the MUA film. These quantities, plotted vs number of MUA layers, are shown in Fig. 3.9.

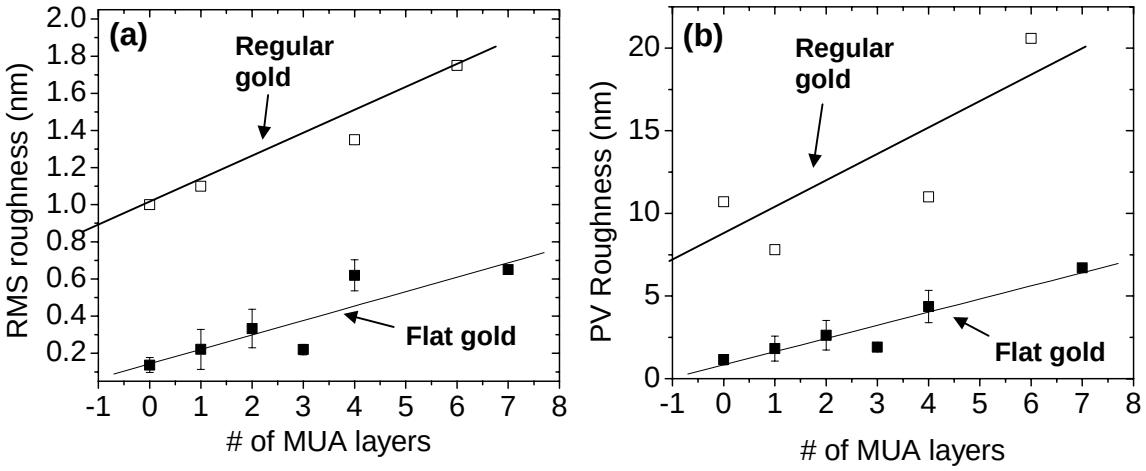


Figure 3.8. Roughness of MUA film on regular and template-stripped gold substrates vs # of MUA layers. (a) RMS roughness. (b) PV roughness. To determine roughness on template-stripped gold, multiple measurements in only flat regions were averaged; the error bars represent the standard deviation of those measurements.

On regular gold, the RMS roughness represents a substantial fraction (0.7) of the 1-layer MUA film, but this fraction decreases rapidly as the number of layers is increased. On flat gold, the RMS roughness represents a much smaller fraction of the MUA film and is less dependent on film thickness, ranging from 0.14 at 1 layer to 0.06 at 7 layers with a slope of –0.01/layer. Similar trends are observed for the PV roughness, with a slope of –0.07/layer for MUA on flat gold. For both the PV and RMS roughness of measurements on regular gold, the large initial fractional roughness that rapidly decreases as the number of MUA layers increases reflects the large component of roughness that is due to the gold itself.

Consideration of Figure 3.9 suggests two important results. First, we note that the fractional RMS and PV variations in the MUA films measured on flat gold, which are characteristic of the MUA film itself and not the underlying substrate, are roughly independent (and even decrease slightly) with the number of MUA layers. This indicates that the quality of the MUA multilayer structure does not decrease as the number of layers increases, and instead the layers remain densely packed (~0.1 RMS fractional roughness) regardless of the number of MUA layers. However, there are significant PV variations in these layers, comparable to their total thickness, even for multiple MUA layers.

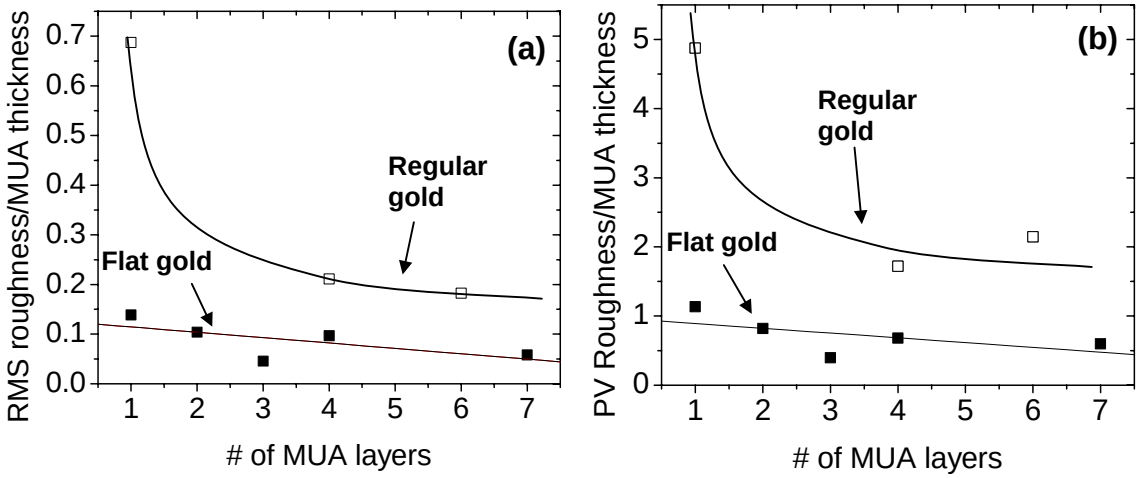


Figure 3.9. Roughness of MUA films (from Figure 3.8) divided by MUA thickness vs number of MUA layers. (a) RMS roughness/MUA thickness. (b) PV roughness/MUA thickness. The MUA thickness was estimated as 1.6 nm/layer, as measured by ellipsometry. The lines are drawn to guide the eye and do not represent fitting to the data.

Second, we note that the fractional roughness of the MUA film deposited on the regular gold substrate decreases rapidly as the number of MUA layers is increased, indicating that the MUA layers have a flattening effect on the rough gold substrate. In practice, the relatively large roughness intrinsic in the gold substrate may lead to electrical shorting when the film is contacted by a top electrode. To minimize this possibility, more MUA layers are desirable. This conclusion is applicable to devices made on both regular and flat gold films: if the roughness of MUA on flat gold is measured over the entire surface (instead of only the flat areas as in Figure 3.8 and 3.9), results comparable to those on regular gold are obtained. Both of these results therefore encourage the use of thicker MUA films for electrical testing because these films remain high-quality and help to minimize the effect of roughness in the gold. However, even MUA films with multiple layers have significant PV variations, which may increase the likelihood of parasitic currents in devices.

3.4.4 Ultraviolet Photoelectron Spectroscopy

UPS measurements were used to characterize the electronic levels in the MUA layer (and their alignment with electronic levels in the gold substrate). Because only emitted electrons are studied in this approach, we obtain information about electronic levels that are filled (i.e. those below the Fermi level). A complementary technique such as inverse photoemission spectroscopy (IPES) could be used to study empty electronic levels and is a potential direction for future work.

All UPS measurement and analysis was carried out with the help of Alan Wan, a graduate student in the laboratory of Professor Antoine Kahn in the Department of Electrical Engineering at Princeton University. Experiments were performed in a high-vacuum system (base pressure ~10^{-10} torr) in this lab. After growing MUA layers on regular gold in the standard manner (Section 3.3), samples were removed from solution in a nitrogen glovebox, rinsed with ethanol, then transferred to the load-lock in a nitrogen-filled carrier vessel. For comparison measurements on a hexadecanethiol (HDT) monolayer, the monolayer was grown by immersing a freshly-evaporated gold substrate into a dilute (~ 1 mM) solution of HDT in ethanol for several hours, then removing, rinsing with ethanol, and loading into the vacuum chamber.

The He-I (21.2 eV) and He-II (40.8 eV) lines from a He lamp were used for sample excitation. Photoelectrons were measured with a double-pass cylindrical mirror analyzer with an energy resolution of 0.15 eV [29]. A 3 V bias was applied to enhance

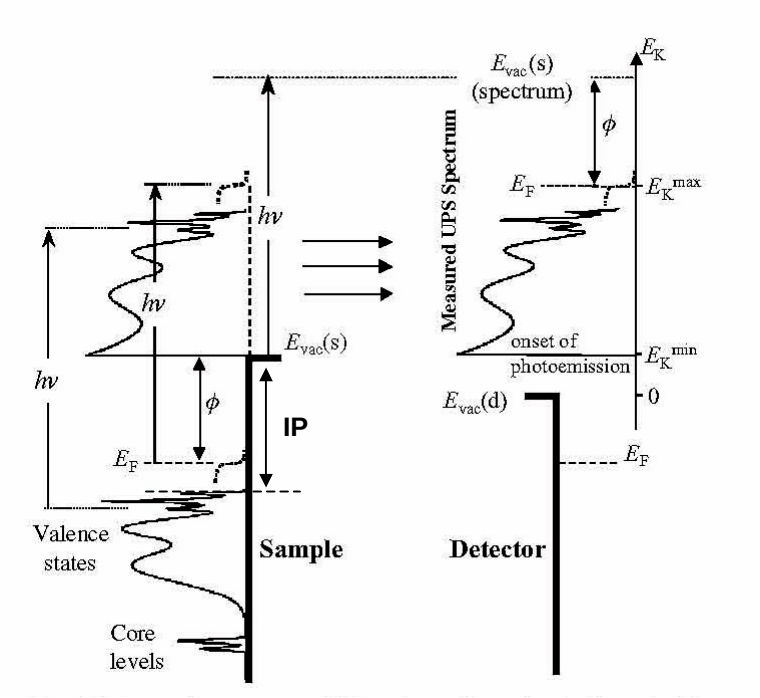


Figure 3.10. Schematic of energy levels in UPS spectra (from Ref [1]).

the collection of low kinetic-energy (KE) electrons. A gold sample (prepared at the same time as the gold used for MUA growth) that was cleaned *in situ* by sputtering of Ar+ ions at 1 kV for 5 min was used to measure gold electronic levels.

A schematic that defines the energy levels of interest in a UPS measurement is shown for a generalized semiconductor sample and detector in Figure 3.10 (from Ref [1]). An incoming photon with energy $h\nu$ excites an electron from the semiconductor core or valence levels. If the excited electron has sufficient energy to reach the vacuum level of the semiconductor $E_{vac}(s)$ (and is close to the surface of the semiconductor) it can be emitted into the vacuum, and collected by the detector, where its KE (E_K) upon arrival is recorded. Note that the vacuum levels of the semiconductor and detector ($E_{vac}(s)$ and $E_{vac}(d)$) are not necessarily at the same energy as these levels depend on the relative work functions of the materials [1]. In the diagram $E_{vac}(d)$ lies below $E_{vac}(s)$ (so that the lowest kinetic-energy electrons measured by the detector are those that have nearly zero kinetic energy when emitted from the sample); we ensure that this condition exists (regardless of the alignment of vacuum levels) by applying a 3 V bias. The semiconductor is usually electrically connected to a metal

sample (in our case, the gold substrate on which we grow the MUA layers); its work function ϕ and Fermi level E_F are also shown in the diagram. In this diagram, the metal and semiconductor share the vacuum level $E_{vac}(s)$. More generally, the metal can have a different vacuum level $E_{vac}(m)$. We are primarily interested in three quantities: (i) the metal work function ϕ, (ii) the difference between $E_{vac}(s)$ and $E_{vac}(m)$ (which is the relative surface dipole Δ between the materials), and (iii) the ionization potential (*IP*) of the semiconductor, which is the difference in energy between $E_{vac}(s)$ and the top of the valence band (or HOMO, for an organic semiconductor).

The spectrum of the reference gold sample is shown in Figure 3.11 (for the 21.2 eV line). The onset of photoemission (at $E_{K,Au}^{min}$ = 2.9 eV) is due partially to electrons from deep levels that have received just enough energy to reach $E_{vac}(m)$, as well as electrons from higher energy levels that have lost energy due to scattering prior to emission. These secondary electrons form the bulk of the low KE electrons. The highest KE ($E_{K,Au}^{max}$ =18.8 eV) electrons map out the Fermi function near the gold E_F. Two intensity peaks can also be seen at high KE (between 12 and 16 eV); these are

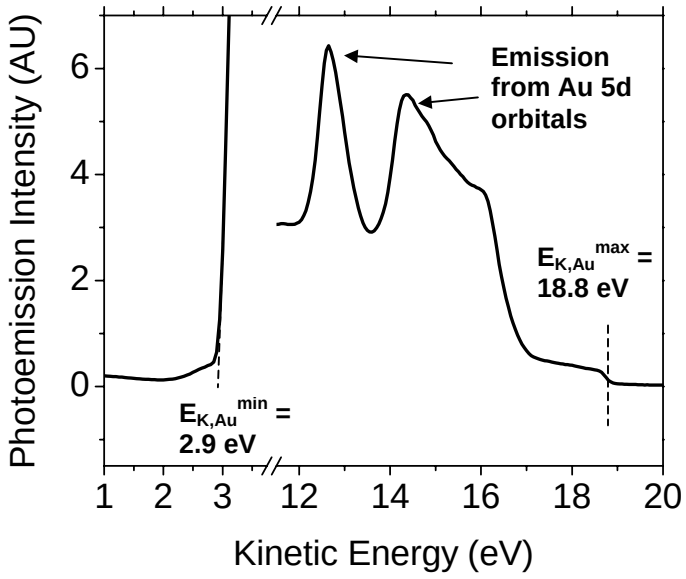


Figure 3.11. UPS spectra showing photoemission intensity vs the (relative) kinetic energy of the emitted electrons of a reference gold sample. The onset of photoemission (at $E_{K,Au}^{min}$ = 2.9 eV) is determined by a tangent to the slope of the plot at onset. The highest-KE electrons map out the gold Fermi level; the value of $E_{K,Au}^{max}$ = 18.8 eV is determined by the center of the gold Fermi step, as shown. Also visible are emission peaks from Au 5d levels.

due to electrons emitted from the Au(5d) states [30]. Because of secondary electrons, it is difficult to correlate the UPS spectrum to solid-state energy levels at lower KE, so we do not show the spectrum between 3 and 12 eV. By examining Fig. 3.10, we find that ϕ is equal to $h\nu$ minus the quantity ($E_{K,Au}^{max}$- $E_{K,Au}^{min}$). We therefore determine ϕ for the cleaned, reference gold sample to be 21.2 eV – (18.8 - 2.9) eV = 5.3 eV. This is comparable to the value (5.4 $\pm$ 0.1 eV) obtained for clean gold in other work using the same vacuum system [29].

Next, we consider the UPS spectra of samples with 1 MUA layer and 6 MUA layers on a gold substrate (for the 21.2 eV photons) (Fig. 3.12). The escape depth for electrons with KE of ~15 eV in hydrocarbon films is less than 1 nm [30, 31], so that emission from the gold substrate is already minimal for the 1 MUA layer film (with a thickness of ~ 1.5 nm) and negligible for the 6 MUA layer film. It is immediately clear that the onset of emission from the MUA occurs at a lower energy ($E_{K,,MUA}^{min}$) than from the reference gold. This energy difference is equal to the relative surface dipole

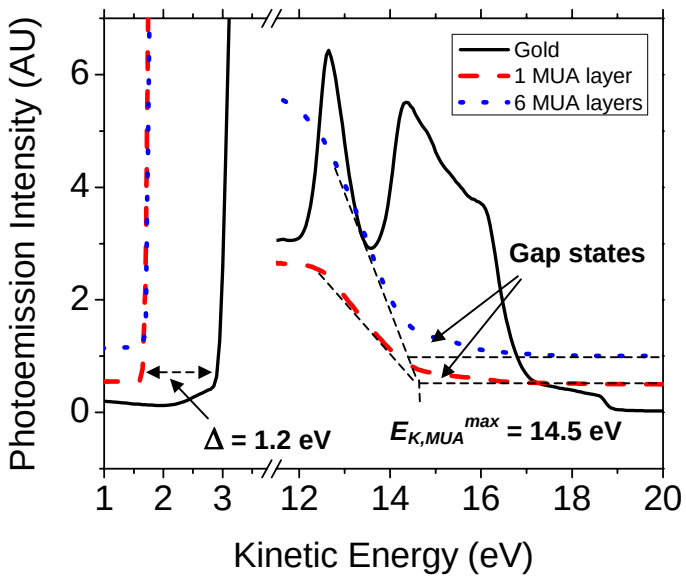


Figure 3.12. UPS spectra showing photoemission intensity vs the (relative) kinetic energy of the emitted electrons for 1 MUA layer and 6 MUA layers samples, along with reference gold spectrum. The curves are offset for visibility. The difference between $E_{K,Au}^{min}$ and $E_{K,MUA}^{min}$ determines Δ (= 1.2 eV) for both 1 and 6 MUA layers. $E_{K,MUA}^{max}$ = 14.5 eV for both samples is determined by the tangent to spectra near 14 eV. However, the signal intensity remains higher than background even at higher KE than $E_{K,MUA}^{max}$, suggesting the existence of higher-energy gap (or shallow trap) states within the HOMO-LUMO gap.

between the surfaces, so we find $\Delta = E_{K,Au}^{min} - E_{K,MUA}^{min}$ = 2.9 eV – 1.7 eV = 1.2 eV for both the 1 MUA and 6 MUA layer samples. This dipole energy is very similar to that obtained in previous measurements of alkanethiols on gold (~1.3 eV for octadecanethiol), and is thus primarily due to charge transfer in the thiol-Au bond [30]. To confirm that the dipole was due to the thiol-Au bonding (and not the polar COOH group on the top of the MUA), we also performed measurements on a monolayer of hexadecanethiol (HDT) (which consists of a thiol endgroup and a 16-carbon alkane chain, with no COOH group) and obtained a dipole of 1.4 eV, comparable to the value obtained with the MUA.

We now examine the high KE electrons. As in other UPS measurements on alkanethiol monolayes, no strong spectral features emerge below the HOMO level, so we focus on energies higher than 12 eV. To extract the *IP*, we use a tangent line as shown in Fig. 3.12 to extrapolate to the background electron intensity to determine $E_{K,MUA}^{max} \cong$ 14.5 eV for both samples. We then use a similar procedure as was used to calculate ϕ, and find that IP = $h\nu$ - ($E_{K,MUA}^{max} - E_{K,MUA}^{min}$) = 21.2 eV – (14.5 – 1.7) eV = 8.4 eV.

We also note that there appear to be electrons with energy higher than $E_{K,MUA}^{max}$ as we have defined it. Very similar states were observed when we repeated the measurement with the higher-energy (40.8 eV) He line. Therefore, we believe that these electrons are not measurement artifacts and instead reveal the existence of additional filled levels with energies higher than our estimate of the HOMO. We will refer to these as trap states existing within the HOMO-LUMO gap. It is important to note that in reality there is some ambiguity as to the nature of these trap levels, as the definition of the HOMO that we use is somewhat arbitrary (so that it could be argued that these levels should be defined as the HOMO). Nevertheless, for the purpose of our discussion we will treat these levels as being distinct from molecular HOMO levels and existing in the energy gap of the MUA. The observation of gap levels is not uncommon in studies of organic films on metals and such levels are often attributed to surface-induced disorder. For example, other solids consisting of singly-bonded carbon chains (such as polyethylene) are known to contain a relatively high density of shallow, localized states within the HOMO-LUMO gap due to conformation disorders [32].

Overall, very few differences between the spectra of the 1 MUA layer and 6 MUA layer samples are apparent, suggesting that the multilayer structure retains an electronic structure similar to the single layer sample, despite the additional Cu layers. Alternatively, it is possible that any levels due to Cu are difficult to observe (a result of the depth of the Cu ions, which are covered by a MUA layer and therefore 1.5 nm below the surface, below the escape depth of electrons), or contributed levels from Cu may exist as empty states (and so would not be detected in this approach).

We can construct a partial energy-level diagram for the Au-MUA system based on the UPS measurements (Fig. 3.13(a)). Because of the similarity between 1 MUA layer and 6 MUA layer spectra, this diagram represents either a monolayer or multilayer system. In the diagram, the Au E_F lies 5.3 eV below $E_{vac}(Au)$. The surface dipole causes $E_{vac}(MUA)$ to lie 1.2 eV below $E_{vac}(Au)$, and the MUA HOMO level lies 8.4 eV below this level This suggests a very large barrier Φ_{HOMO} = 4.4 eV for charge injection into the HOMO. However, as discussed earlier, the presence of trap states (which are known to contribute to conduction processes in polyethylene [32]) extending ~ 2 eV higher than the HOMO would result in a much lower charge injection barrier of Φ_{FTS} = 2.4 eV.

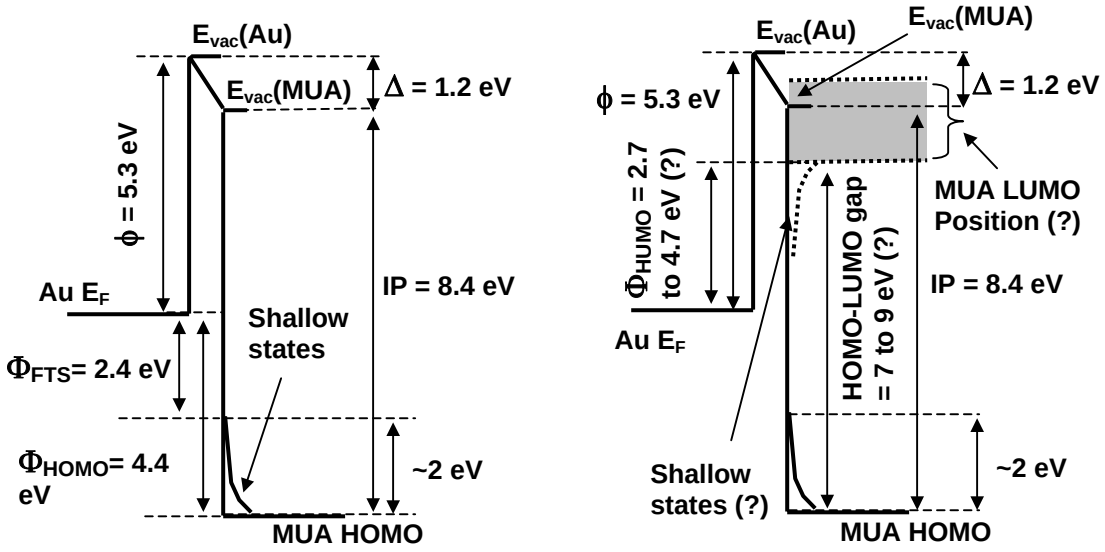


Figure 3.13. (a) Partial energy-level diagram for the Au-MUA (single or multilayer) system suggested by UPS. (b) Speculative position of MUA LUMO (shaded), as well as possible trap states near LUMO, based on literature values of the HOMO-LUMO gap in similar systems.

We can also speculate on a more complete energy-level diagram for the Au-MUA system by assuming a HOMO-LUMO gap of 7 to 9 eV (Fig 3.13(b)) (this estimate is based on theoretical calculations of the HOMO-LUMO gap in alkane chains and experimental measurements of bulk polyethylene) [32-34]. A HOMO-LUMO gap larger than the IP (8.4 eV) would result in a material with negative electron affinity (NEA) (i.e. electrons in the LUMO would have an even higher energy than in vacuum). Although generally unusual, NEA has been observed in polyethylene (which also has a singly-bonded carbon backbone) [32], so may be possible in the MUA. A HOMO-LUMO gap of 7 to 9 eV would result in a charge injection barrier (into the LUMO) of Φ_{LUMO} = 2.7 to 4.7 eV, potentially much lower than the barrier into the HOMO (Φ_{HOMO} = 4.4 eV). Moreover, if (empty) shallow levels exist below the LUMO similar to those above the HOMO (as is likely [32]), this barrier could be lowered even further. We will return to this consideration of energy levels in the Au-MUA system when we discuss the charge transport mechanism of Au-MUA-Au devices in Section 4.4.4.

3.5 Summary

Multilayer MUA films were chosen for detailed study in this thesis because they allow a range of device characteristics to be explored, they can be grown by utilizing straightforward and widely used chemistry, and because multilayer films may be one option to increase gate-channel coupling if used in molecular-scale FETs. Gold substrates were prepared by either direct thermal evaporation, or template-stripping to obtain large atomically flat regions. Repeated bilayers of MUA and Cu were grown on the gold substrates by alternating immersions of the substrate in dilute solutions of MUA and $Cu(ClO_4)_2$ in ethanol. Characterization of these films by ellipsometry revealed a linear increase of 1.6 nm/layer as the number of MUA layers was increased. RBS measurements suggested that the MUA forms close-packed layers with a density of 5 x 10^{14} molecules/cm^2 (= 5 molecules/nm^2). AFM confirmed that the MUA forms dense layers with an RMS fractional roughness of <0.1, although PV variations remained comparable to the thickness of the film even for multiple layers. Nevertheless, the smoothing effect that thicker films have on the roughness due to the gold substrate itself suggests that multiple-layer devices may be most useful for fabricating devices that have minimal electrical defects. Finally, UPS measurements suggested a partial band diagram for the Au-MUA system in which the MUA HOMO

lies 4.4 eV below the Au Fermi level, but a number of gap states exist in the MUA at higher energies.

References

[1] D. Cahen and A. Kahn, "Electron Energetics at Surfaces and Interfaces: Concepts and Experiments" *Advanced Materials* **15** (4), 271-277 (2003).

[2] A. Kumar, H. A. Biebuyck and G. M. Whitesides, "Patterning Self-Assembled Monolayers - Applications in Materials Science" *Langmuir* **10** (5), 1498-1511 (1994).

[3] A. Ulman, "Formation and Structure of Self-Assembled Monolayers" *Chemical Reviews* **96** (4), 1533-1554 (1996).

[4] P. E. Laibinis, G. M. Whitesides, D. L. Allara, Y. T. Tao, A. N. Parikh and R. G. Nuzzo, "Comparison of the Structures and Wetting Properties of Self-Assembled Monolayers of Normal-Alkanethiols on the Coinage Metal-Surfaces, Cu, Ag, Au" *Journal of the American Chemical Society* **113** (19), 7152-7167 (1991).

[5] B. A. Mantooth and P. S. Weiss, "Fabrication, Assembly, and Characterization of Molecular Electronic Components" *Proceedings of the IEEE* **91** (11), 1785-1802 (2003).

[6] J. M. Tour, L. Jones, D. L. Pearson, J. J. S. Lamba, T. P. Burgin, G. M. Whitesides, D. L. Allara, A. N. Parikh and S. V. Atre, "Self-Assembled Monolayers and Multilayers of Conjugated Thiols, Alpha,Omega-Dithiols, and Thioacetyl-Containing Adsorbates - Understanding Attachments between Potential Molecular Wires and Gold Surfaces" *Journal of the American Chemical Society* **117** (37), 9529-9534 (1995).

[7] T. L. Brower, J. C. Garno, A. Ulman, G. Y. Liu, C. Yan, A. Golzhauser and M. Grunze, "Self-Assembled Multilayers of 4,4 '-Dimercaptobiphenyl Formed by Cu(Ii)-Catalyzed Oxidation" *Langmuir* **18** (16), 6207-6216 (2002).

[8] J. J. Gooding, F. Mearns, W. R. Yang and J. Q. Liu, "Self-Assembled Monolayers into the 21(St) Century: Recent Advances and Applications" *Electroanalysis* **15** (2), 81-96 (2003).

[9] N. G. Semaltianos and E. G. Wilson, "Investigation of the Surface Morphology of Thermally Evaporated Thin Gold Films on Mica, Glass, Silicon and Calcium Fluoride Substrates by Scanning Tunneling Microscopy" *Thin Solid Films* **366** (1-2), 111-116 (2000).

[10] Y. Golan, L. Margulis, S. Matlis and I. Rubinstein, "Vacuum-Deposited Gold-Films .2. Role of the Crystallographic Orientation of Oxide-Covered Silicon Substrates" *Journal of the Electrochemical Society* **142** (5), 1629-1633 (1995).

[11] Y. Golan, L. Margulis and I. Rubinstein, "Vacuum-Deposited Gold-Films .1. Factors Affecting the Film Morphology" *Surface Science* **264** (3), 312-326 (1992).

[12] A. Hammiche, R. P. Webb and I. H. Wilson, "A Scanning-Tunneling-Microscopy Study of Thin Gold-Films Evaporated on Silicon" *Vacuum* **45** (5), 569-573 (1994).

[13] C. Masens, J. Schulte, M. Phillips and S. Dligatch, "Ultra Flat Gold Surfaces for Use in Chemical Force Microscopy: Scanning Probe Microscopy Studies of the Effect of Preparation Regime on Surface Morphology" *Microscopy and Microanalysis* **6** (2), 113-120 (2000).

[14] P. Wagner, M. Hegner, H. J. Guntherodt and G. Semenza, "Formation and in-Situ Modification of Monolayers Chemisorbed on Ultraflat Template-Stripped Gold Surfaces" *Langmuir* **11** (10), 3867-3875 (1995).

[15] I. Touzov and C. B. Gorman, "Tip-Induced Structural Rearrangements of Alkanethiolate Self-Assembled Monolayers on Gold" *Journal of Physical Chemistry B* **101** (27), 5263-5276 (1997).

[16] J. J. Blackstock, Z. Y. Li, M. R. Freeman and D. R. Stewart, "Ultra-Flat Platinum Surfaces from Template-Stripping of Sputter Deposited Films" *Surface Science* **546** (2-3), 87-96 (2003).

[17] D. Stamou, D. Gourdon, M. Liley, N. A. Burnham, A. Kulik, H. Vogel and C. Duschl, "Uniformly Flat Gold Surfaces: Imaging the Domain Structure of Organic Monolayers Using Scanning Force Microscopy" *Langmuir* **13** (9), 2425-2428 (1997).

[18] S. D. Evans, A. Ulman, K. E. Goppert-Berarducci and L. J. Gerenser, "Self-Assembled Multilayers of Omega-Mercaptoalkanoic Acids - Selective Ionic Interactions" *Journal of the American Chemical Society* **113** (15), 5866-5868 (1991).

[19] M. T. Lee, C. C. Hsueh, M. S. Freund and G. S. Ferguson, "Air Oxidation of Self-Assembled Monolayers on Polycrystalline Gold: The Role of the Gold Substrate" *Langmuir* **14** (22), 6419-6423 (1998).

[20] M. Brust, P. M. Blass and A. J. Bard, "Self-Assembly of Photoluminescent Copper(I)-Dithiol Multilayer Thin Films and Bulk Materials" *Langmuir* **13** (21), 5602-5607 (1997).

[21] S. D. Evans, T. M. Flynn and A. Ulman, "Self-Assembled Multilayer Formation on Predefined Templates" *Langmuir* **11** (10), 3811-3814 (1995).

[22] T. L. Freeman, S. D. Evans and A. Ulman, "XPS Studies of Self-Assembled Multilayer Films" *Langmuir* **11** (11), 4411-4417 (1995).

[23] T. Yamaguchi, R. Sakai, K. Takahashi and T. Komura, "Electron Transfer Rate of Redox Ion Controlled by Electrostatic Interaction with Bilayer Films Assembled Using Thiolate-Copper Ion-Carboxylate Bridges" *Electrochimica Acta* **48** (5), 589-597 (2003).

[24] D. K. Schwartz, "Mechanisms and Kinetics of Self-Assembled Monolayer Formation" *Annual Review of Physical Chemistry* **52**, 107-137 (2001).

[25] M. M. Walczak, C. K. Chung, S. M. Stole, C. A. Widrig and M. D. Porter, "Structure and Interfacial Properties of Spontaneously Adsorbed Normal-Alkanethiolate Monolayers on Evaporated Silver Surfaces" *Journal of the American Chemical Society* **113** (7), 2370-2378 (1991).

[26] J. C. Love, D. B. Wolfe, R. Haasch, M. L. Chabinyc, K. E. Paul, G. M. Whitesides and R. G. Nuzzo, "Formation and Structure of Self-Assembled Monolayers of Alkanethiolates on Palladium" *Journal of the American Chemical Society* **125** (9), 2597-2609 (2003).

[27] Z. Bao, Personal Communication (2005).

[28] G. L. Fisher, A. E. Hooper, R. L. Opila, D. L. Allara and N. Winograd, "The Interaction of Vapor-Deposited Al Atoms with CO_2H Groups at the Surface of a Self-Assembled Alkanethiolate Monolayer on Gold" *Journal of Physical Chemistry B* **104** (14), 3267-3273 (2000).

[29] A. Wan, J. Hwang, F. Amy and A. Kahn, "Impact of Electrode Contamination on the Alpha-NPD/Au Hole Injection Barrier" *Organic Electronics* **6**, 47-54 (2005).

[30] D. M. Alloway, M. Hofmann, D. L. Smith, N. E. Gruhn, A. L. Graham, R. Colorado, Jr., V. H. Wysocki, T. R. Lee, P. A. Lee and N. R. Armstrong, "Interface Dipoles Arising from Self-Assembled Monolayers on Gold: UV-Photoemission Studies of Alkanethiols and Partially Fluorinated Alkanethiols" *Journal of Physical Chemistry B* **107** (42), 11690-9 (2003).

[31] A. S. Duwez, G. Pfister-Guillouzo, J. Delhalle and J. Riga, "Probing Organization and Structural Characteristics of Alkanethiols Adsorbed on Gold and of Model Alkane Compounds through Their Valence Electronic Structure: An Ultraviolet Photoelectron Spectroscopy Study" *Journal of Physical Chemistry B* **104** (38), 9029-9037 (2000).

[32] G. Teyssedre and C. Laurent, "Charge Transport Modeling in Insulating Polymers: From Molecular to Macroscopic Scale" *IEEE Transactions on Dielectrics and Electrical Insulation* **12** (5), 857-875 (2005).

[33] A. Salomon, D. Cahen, S. Lindsay, J. Tomfohr, V. B. Engelkes and C. D. Frisbie, "Comparison of Electronic Transport Measurements on Organic Molecules" *Advanced Materials* **15** (22), 1881-1890 (2003).

[34] K. J. Less and E. G. Wilson, "Intrinsic Photoconduction and Photoemission in Polyethylene" *Journal of Physics C-Solid State Physics* **6** (21), 3110-3121 (1973).

Chapter 4

Electrical Characteristics of MUA Films in a Two-Terminal Planar Device Structure

4.1 Introduction

The simplest form a molecular-scale device can take is a two-terminal structure with the molecular layer sandwiched between top and bottom electrodes. The ability to fabricate this simple structure is also a prerequisite for the preparation of more complicated three-terminal (FET) structures. In this chapter, we describe the development of a two-terminal device structure, then use it to make the first reported measurements of the electrical properties of multiple layers of MUA. This same structure will also be used to fabricate molecular-scale memory devices based on MUA films in Chapter 7.

The critical requirement that we impose on any device in our work is that it be capable of integration with metal interconnects for fabrication of large-scale device arrays. This creates two challenges. First, organic films have limited compatibility with conventional photolithography because the deposition and development of the polymer photoresist can degrade the quality of the organic layer. Any photolithography must therefore be done prior to the deposition of the organic layer. Second, because of the ultrathin nature of molecular-scale films, if a conventional technique such as thermal evaporation is used to deposit a metal electrode on top of the film it is very likely that some of the evaporated metal will penetrate through the film. Metal penetration leads to electrical shorting that obscures the characteristics of the organic layer.

To avoid this problem, workers who study the electrical characteristics of monolayers and single molecules have developed novel techniques to form electrical contacts to the organic layer or molecule without evaporating a top electrode [5]. These techniques include using a Hg drop as a top electrode (Fig. 4.1(a) [3, 7-9], mechanically controlled break junctions (Fig. 4.1(b) [10, 11], nanopores in a silicon nitride membrance (Fig. 4.1(c)) [12-14], nanowires (and nanowires with a nanoparticle bridge) (Fig. 4.1(d) and (e) [4, 15], crossed wires attracted my magnetic deflection (Fig.

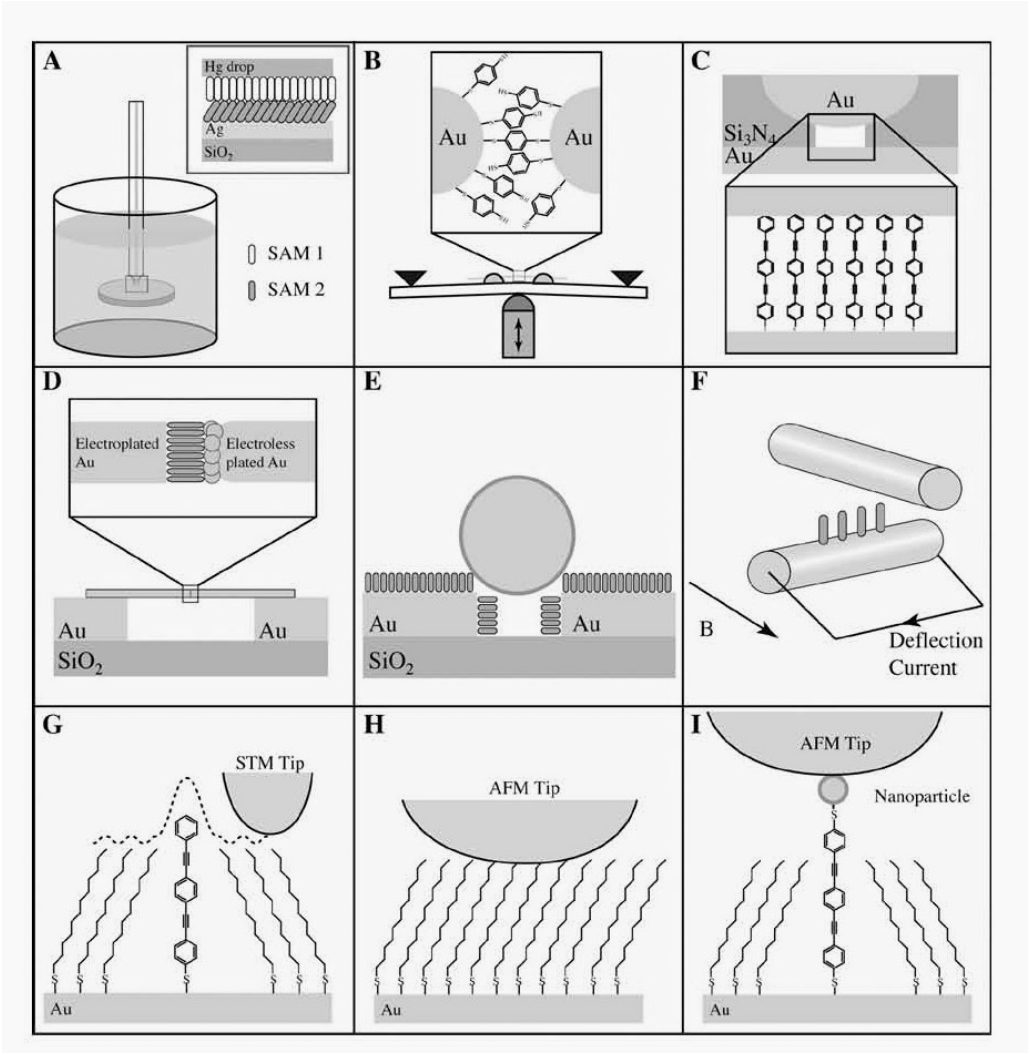


Figure 4.1. Various experimental techniques to measure the conductance of single molecules and molecular layers (from Ref [5]). (a) Hg drop junction. (b) Mechanically controlled break junctions. (c) Nanopore. (d) Nanowire (e) Nanoparticle bridge. (f) Crossed wires. (g) STM. (h) Conducting-probe AFM. (i) Nanoparticle-coupled conducting-probe AFM.

4.1(f))[16], and a variety techniques that utilize the tip of scanning tunning microscope (STM) or AFM (Fig. 4.1(g),(h), and (i)) [2, 6, 17]. Most of these approaches are clearly not compatible with large-scale device integration.

Although some initial results on the electroless deposition of electrodes on monolayers [4] and microcontact printing from a soft stamp [18] are promising, most integration approaches will probably employ vacuum-deposited metal electrodes on top of the molecular-scale film [19]. In our work we therefore use thermal evaporation to

deposit the top metal on all devices. To minimize the problem of metal penetration during thermal evaporation, we study multilayer MUA films that are expected to be more resistant to penetration, and optimize the evaporation procedure. To avoid the problem of photolithography incompatibility, we use metal shadow masks for patterning during device fabrication. The resulting devices are relatively large area because it is difficult to obtain shadow masks with dimensions below ~25 μm; an alternative approach to minimize device area is described in Chapter 5.

This chapter is organized as follows. Section 4.2 discusses the fabrication of the two device structures and summarizes the fabrication parameters that we explored. Section 4.3 describes electrical measurements on multiple layers of MUA using these structures, and describes how different fabrication parameters affected device performance. Finally, the physical basis for the observed device characteristics is discussed in Section 4.4, and Richardson-Schottky emission is used to describe the injection-limited charge transport in some of the devices.

4.2 Device Fabrication*

The initial device structure that we investigated utilized the overlap between a gold layer (patterned prior to multilayer growth) and a second, patterned top gold layer to define the device area. This structure is referred to as the pre-patterned metal (PrPM) structure. Si substrates with a thin (30 nm) thermal oxide layer were cleaned with acetone and isopropanol then loaded into a thermal evaporator. 5 nm Ti (for adhesion) and 30 to 50 nm Au layers were evaporated through a shadow mask unto the Si substrate at a base pressure of 10^{-6} torr and a rate of 0.1 to 0.5 nm/s (Fig. 4.2(a)). Substrates were then immersed in MUA solution to grow a multilayer film following the procedure outlined in Section 3.3 (Fig. 4.2(b)). After MUA growth, a 30 to 50 nm top metal electrode was deposited onto the samples through a shadow mask (the parameters of this evaporation were varied, as described later) (Fig. 4.2(c)). The second metal layer was not aligned to the first, so that the active device area (defined by the overlap of the two gold electrodes) varied between 10 to >1000 μm^2, depending on the size of the features used in the shadow-mask pattern (Fig. 4.2(d)). The PrPM device was contacted by electrical probes in the relatively large (>30 x 30 μm^2) regions adjacent to the overlap area (direct probing of the contact area was avoided to prevent

* For additional fabrication and experimental details, please refer to Appendix B.

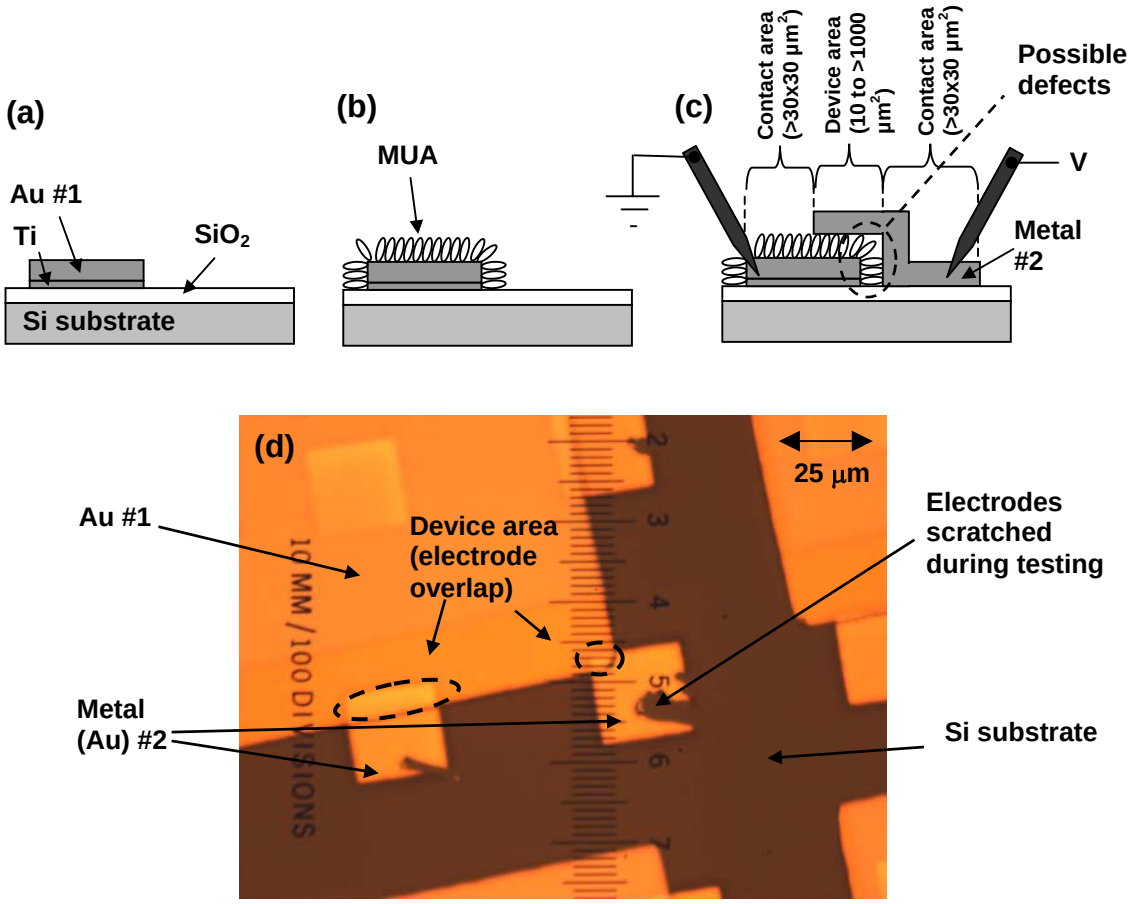


Figure 4.2. Schematic of PrPM device fabrication and structure, and top view of devices. (a) A 5 nm layer of Ti and a 30 to 50 nm layer of Au are deposited through a shadow mask onto an oxidized Si wafer. (b) A MUA multilayer is grown on the prepatterned metal layer. (c) The second metal layer is deposited through a shadow mask to form the top electrode. (d) Microscope image of devices (top view). The dark background is the Si substrate, while the large squares are the first gold electrodes and the smaller squares are the second gold electrodes (some of which are scratched after testing). As shown in (c) and (d), the device area (10 to >1000 μm^2) is defined by the overlap of the two metal layers while the contact areas (>30 x 30 μm^2) are regions without overlap. For electrical measurements, the bottom gold electrode is grounded and a voltage is applied to the top. Also shown in (c) is the region where defects are most likely, as discussed in Section 4.4.

the needle probe from puncturing the thin metal and MUA layers). One drawback of this approach is that it cannot be used to test flat gold films because of the difficulty of bonding a patterned film to a target substrate and then stripping it from the template without a significantly modified procedure. For example, if we attempted to bond a target substrate to a patterned gold film on a template using the procedure described earlier (Fig. 3.1), in the regions where there was no gold film the applied glue would bond the target substrate directly to the template, making the film unusable.

The incompatibility of the PrPM device structure with flat-gold films led to the development of a second structure that used a post-patterned-insulator (PoPI) to limit device areas. In this structure, a uniform gold film was prepared on a Si substrate, either by direct thermal evaporation (with a 5 nm Ti layer) or by template-stripping (as described in Chapter 3). A MUA multilayer film was then grown on the gold layer (Fig. 4.3(a)). Next, a patterned layer of silicon oxide (SiO_x, 50 to 70 nm, 0.1 to 0.7 nm/s, base pressure 10^{-5} torr) was deposited by e-beam evaporation through a shadow mask (Fig. 4.3(b)). Finally, a 30 to 50 nm metal electrode was deposited by thermal evaporation through a shadow mask (without alignment) (the parameters of this evaporation were varied, as described later). In this structure, the thin SiO_x allows probes to contact the top electrode without penetrating the thin device, and more importantly minimizes the device area to 10 to >1000 μm^2 (Fig. 4.3(c)). A wide variety of device areas were achieved by evaporating the second metal electrode at an angle (with respect to the SiO_x squares), so that in addition to different top electrode sizes (determined by the shadow mask pattern) some electrodes would randomly overlap over large areas and others over small areas, as shown in Fig. 4.3(d). (This was also done with the PrPM devices, although for the devices shown in Fig. 4.2(d) this approach was not used).

The shadow masks used to pattern the SiOx and 2^{nd} gold layers (as well as both gold layers in the PrPM structure) were clipped directly onto the substrate, so that in principle there was intimate contact between the substrate and mask (which also means there is a possibility that the organic layer can be scratched by the metal mask). In practice, slight bending in the very thin shadow mask made it unlikely that there was intimate contact between mask and sample in most locations. Nevertheless, care was taken when loading and unloading the samples to minimize possible scratching of the organic layer by the shadow mask.

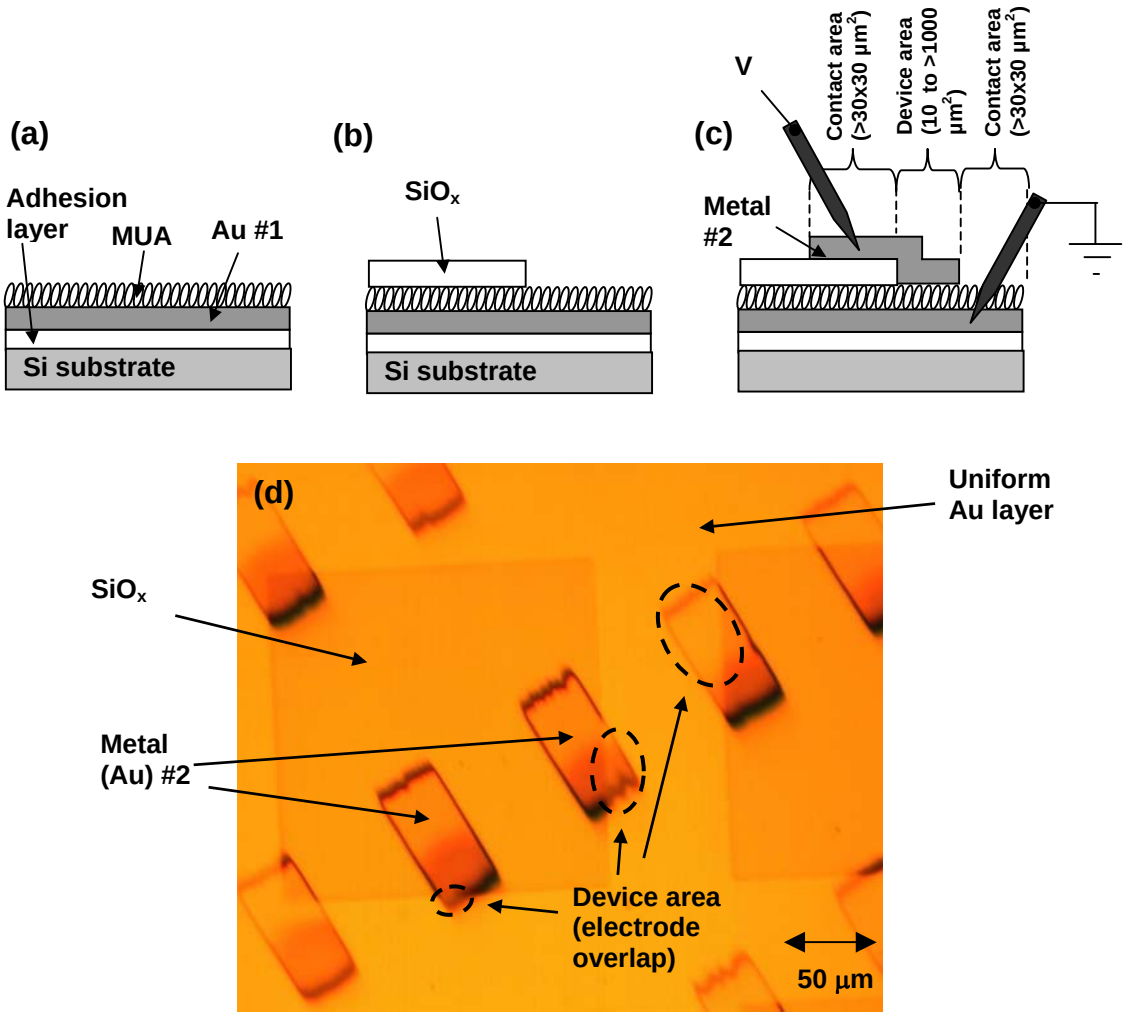


Figure 4.3. Schematic of PoPI device fabrication and structure, and top view of devices. (a) A uniform gold film (80 to 100 nm) is attached to a Si substrate with a 5 nm Ti layer (regular gold films) or epoxy (flat gold films). A MUA multilayer film is grown on the gold. (b) A 70 nm SiO_x layer (patterned with a shadow mask) is deposited by e-beam evaporation. (c) A second metal layer (patterned with a shadow mask) is deposited. (d) Microscope image of devices (top view). The background is the first gold layer, the large off-color squares are the SiO_x, and the small rectangles are the second gold electrodes. These are deposited at an angle (with respect to the SiO_x squares) to obtain a variety of device areas. As shown in (c) and (d), this active device area (10 to >1000 μm^2) is defined by regions where the gold electrodes overlap without the presence of SiO_x. For electrical measurements, the bottom gold electrode is grounded and a voltage is applied to the top electrode. Contact areas (>30x30 μm^2) are located on top of and adjacent to the SiO_x.

A number of fabrication conditions were varied to study their effects on the electrical characteristics of the devices. Because of the importance of evaporating the top contact without shorting the thin organic film, most of these variables are related to the evaporation of the second metal. They include the choice of the evaporated metal, the angle of deposition, whether or not the substrate was cooled during evaporation, and the evaporation rate. Table 4.1 summarizes these different conditions. Also specified are the most common deposition parameters; these default parameters were used to fabricate all devices described in this work unless otherwise specified.

A custom-designed sample stage with thermal shielding was constructed to allow the low-temperature, shallow-angle depositions that were explored in this work (Fig. 4.4). Stainless steel, variable-angle sample holders could be attached to a hollow stainless-steel stage that was filled with liquid nitrogen during the evaporations. The temperature was monitored with a thermocouple gauge inserted into a hole on the side of the shallow-angle sample holder near the sample. Prior to attaching the thermocouple to the stage, the thermocouple was covered with a high-vacuum-compatible heat-transfer compound (Dow Corning 340 silicone heat sink compound) to ensure good thermal contact (and help adhere the thermocouple to the stage). We also found that it was necessary to apply this heat-transfer compound between the shallow-angle holder and stage that was filled with liquid nitrogen to ensure good evaporation of the top electrode. To decrease the thermal flux incident on the sample

Fabrication parameter	Conditions explored	Typical Conditon
Device structure	PrPM or PoPI	PoPI
Bottom gold topology	regular or flat	regular
# of MUA layers	1 to 11	-
Top electrode metal	gold or aluminum	gold
Angle of deposition (degrees)	20, 30, 50	20
Deposition rate	0.01 to 1 nm/s	0.05 nm/s
Substrate temperature	100 or 300 K	100 K

Table 4.1. Fabrication parameters varied during device preparation. The angle of deposition refers to the deposition angle (with respect to the substrate) for the second metal layer. Similarly, deposition rate refers to the deposition rate of the second metal layer, and substrate temperature is the temperature at which the sample was held during this deposition. Unless otherwise specified, devices were fabricated with the default conditions of the third column.

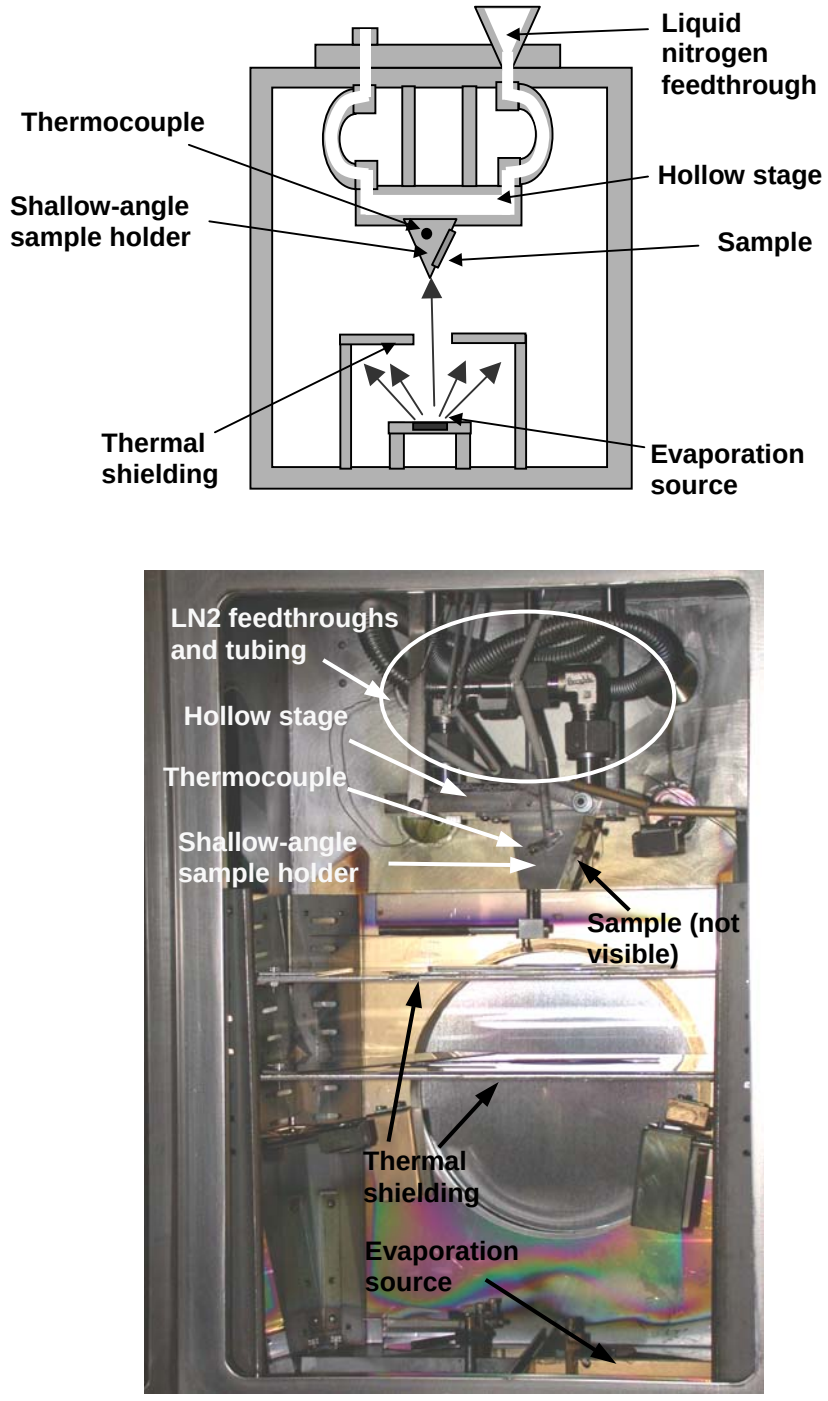


Figure 4.4. Schematic and photograph of custom-designed sample stage for liquid-nitrogen-cooled, shallow-angle evaporations. The temperature is monitored with a thermocouple attached to the shallow-angle sample holder near the sample. Thermal shielding minimizes the thermal flux incident on the sample from the evaporator.

during the evaporation, two layers of 1.5 mm thick stainless-steel thermal shielding (visible in the photograph of Figure 4.4) (with holes of 6 and 7.5 cm diameter to allow the passage of evaporated metal) were installed between the evaporation source and substrate.

4.3 Electrical Measurements

All room-temperature electrical measurements in this thesis were performed with a Micromanipulator 6000 probestation installed in a nitrogren glove box (<1 ppm water and oxygen) (made by Vacuum Atmospheres, Inc.) to avoid oxidation of the thiolate groups in the MUA [20]. An Agilent 4155C semiconductor parameter analyzer was used to apply voltage to the device and measure current. To calculate current density, each device's area was estimated from a microscope image. Temperature-dependent electrical measurements were performed in a Low-Temperature MicroProbe (LTMP) system purchased from MMR Technologies. In all measurements, the bottom gold layer was grounded and the voltage was applied to the top metal layer (as shown in Fig. 4.2 and 4.3).

Because of its alkane-chain backbone, MUA will likely have a relatively large gap of ~ 7 to 9 eV between its highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) [21, 22]. Based on UPS measurements (Section 3.4.4) that suggested a large barrier to charge injection into the film, the films should be insulating, as expected for an alkane molecule (the interspersed Cu layers may complicate this analysis, although they did not appear to have an effect on electronic levels in the UPS measurements).

All of the devices could be classified as either insulating or shorted. Shorted devices were characterized by current densities of $10^7 A/cm^2$ at 1 V (Currents were greater than 10 mA at 1 V for device areas of 10 to > 1000 μm^2). These very large current densities were similar to those measured on control devices fabricated without a MUA layer, which suggests that the charge transport in these shorted devices was due to metal from the electrodes penetrating the organic layer. Insulating devices had much lower current densities of less than 10^2 A/cm^2. However, the current densities in insulating devices often varied dramatically, over a range of up to 10^5, even for devices fabricated in the same batch. Based on this variation, insulating devices could be further classified into high-, medium-, or low-current groups. In addition to high

currents, devices in the first group shared relatively linear and symmetric current density vs voltage (*J-V*) traces (Fig. 4.5(a)). Unlike the high-current devices, low-current devices typically had rectifying characteristics with an exponential dependence of current on voltage (Fig. 4.5(c)), and medium-current-density devices had characteristics that lay between those of the high- and low-current devices (Fig. 4.5(b)). By varying the fabrication conditions, samples in which all (or nearly all) of the devices were in one group could be fabricated; however, for most fabrication conditions a mixture of devices was observed.

For all of the devices, the electrical measurements were insensitive to the voltage scan direction or measurement speed. All electrical characteristics were stable if the voltage was kept within a certain range. For PrPM devices, this range was typically ±1 V. A higher range of ±2V or ±3V could often be applied to PoPI devices without loss of stability. We will delay discussing the breakdown voltage (i.e. the voltage at which devices entered an irreversible, higher-conductance state) until Chapter 7.

As we will show later, the current densities in PoPI devices were generally much lower than in PrPM devices (for devices with the same number of MUA layers). Indeed, for many PoPI devices at voltages below 1 V the current was below the noise level in our experimental apparatus and could not be measured. Thus, in later sections when we compare PrPM and PoPI device conductances, we typically calculate conductances for PrPM devices at 0.5 V (because these devices were not stable above 1 V), but must use higher voltages to accurately calculate the conductance of PoPI devices. Because the electrical characteristics of MUA devices are nonlinear, this results in an underestimate of the PrPM conductance in comparison to PoPI devices, but this underestimation does not affect any of the conclusions that we will make.

To check the quality of the insulating SiO_x films used in the PoPI structure, we tested 70-nm thick SiOx films (contacted by gold electrodes). The currents in these large-area (>100 x 100 μm^2) devices remained below the noise level of the parameter analyzer until large (> 8 V) voltages were applied to the films. This confirms that the current that we measure in the PoPI devices is due to transport through the thin MUA layer, and not through the larger-area (but thicker) SiO_x film.

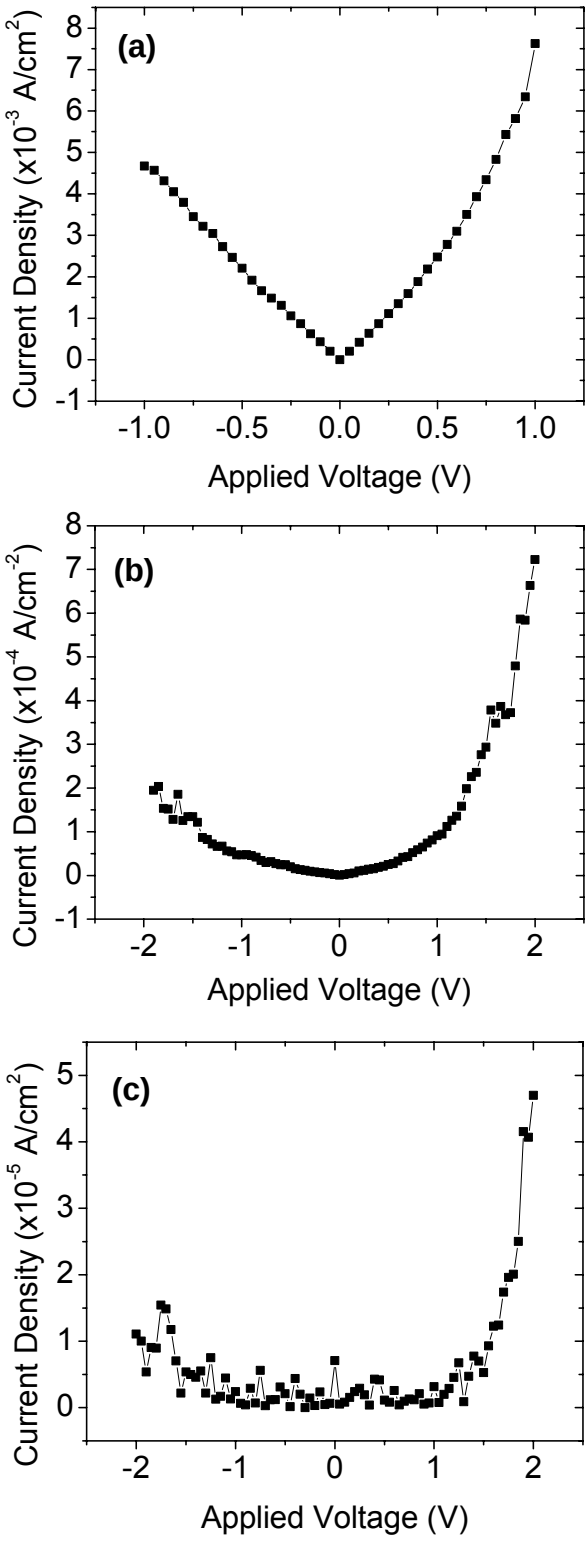


Figure 4.5. Current density vs applied voltage for several insulating 7-layer MUA devices on a regular gold substrate with the top gold electrode deposited at 50˚. Note that the y-axis is scaled differently for each device. (a) High-current device. (b) Medium-current device. (c) Low-current device.

We will now explore how the fabrication parameters and several other factors affected the yield of insulating (unshorted) devices and the electrical characteristics of these insulating devices. After reporting the effects of different fabrication conditions on device performance, in Section 4.4 we will discuss the physical basis for the observed device behavior.

4.3.1 Device Area and Fabrication Dates

Before reporting the effect of different fabrication parameters on device behavior, we first describe the effect of two other factors: device area and fabrication dates. Although there is considerable scatter in the conductance/area of different devices, two trends are still apparent when this quantity is plotted vs device area for the PoPI and PrPM structures (Figure 4.6). For the 7-layer PoPI devices, the conductance/area (measured at 1 V) tended to increase (from 10^{-5} S/cm^2 at 50 μm^2 to 10 S/cm^2 at >1000 μm^2) as the device area was increased. If the data is fitted with a power law, we find that conductance/area increased with area with an exponent of 3.1. Similar trends, with exponents between 2 to 3, were measured on PoPI devices with different numbers of MUA layers. For the 9-layer PrPM devices, an opposite trend was observed, with conductance/area (measured at 0.5 V) decreasing (with a power-law exponent of –1.1) from 10^{-1} S/cm^2 at 2 μm^2 to 10^{-3} S/cm^2 at >500 μm^2.

We also estimated the variation in device performance when identical processing conditions were used to prepare devices on different dates. To compare groups of devices fabricated at different times, we use a cumulative probability plot of the conductance/area of the devices. To create this plot, the devices are first numbered in order of their conductance/area (so that the device with the lowest conductance is assigned 1, and the device with the highest conductance is assigned *n*, for a batch with *n* devices) [23]. In the cumulative probability plot, a device's *x*-coordinate is its conductance/area, and its y-coordinate is the device number (divided by *n* + 1). The premise of this plot is that measurements on different samples prepared under identical conditions (i.e. within the same batch) provide an estimate of the how the measured quantity (in this case, conductance/area) is statistically distributed. The cumulative probability plot thus estimates the probability that a

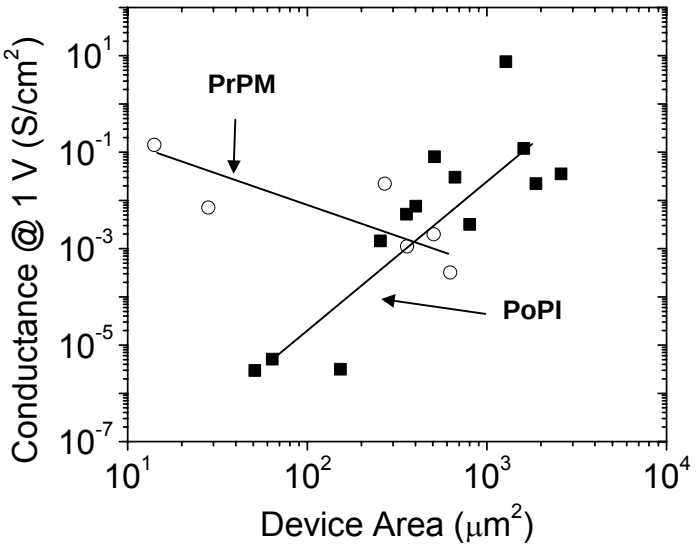


Figure 4.6. Conductance/area vs device area for PoPI and PrPM devices. The PoPI devices had 7 MUA layers and the PrPM devices had 9 MUA layers. Device conductance was calculated at 1 V for the PoPI devices and 0.5 V for the PrPM devices. Fitting with a power law indicated a that the conductance depended on area with an exponent of 3.1 in PoPI devices, and –1.1 in PrPM devices.

measurement on a device within a given batch will return a value at or below the x-coordinate.

Batches of devices prepared under identical conditions (8 MUA layers on flat gold) one month apart are compared on a cumulative probability plot in Figure 4.7(a). The geometric mean conductance (which is calculated by taking the exponential of the average of the logarithms of each data point) for each batch is similar ($4x10^{-5}$ S/cm^2 vs $7x10^{-5}$ S/cm^2), and the probability plots of the batches lie almost on top of each other. This suggests that there is no significant difference between the batches. This is confirmed by a t-test [24], which indicates that the null hypothesis (that there is no significant difference between the batches) is true with 0.47 probability. In general, for a difference to be statistically significant, the null hypothesis should be true with less than 0.05 probability (so that there is a more than 95% probability that the difference is significant). However, there are clear differences between devices fabricated under nominally identical conditions one year apart (Fig. 4.7(b)). Devices prepared in 2005 had a (geometric) mean conductance/area of $4x10^{-4}$ S/cm^2, while those fabricated in

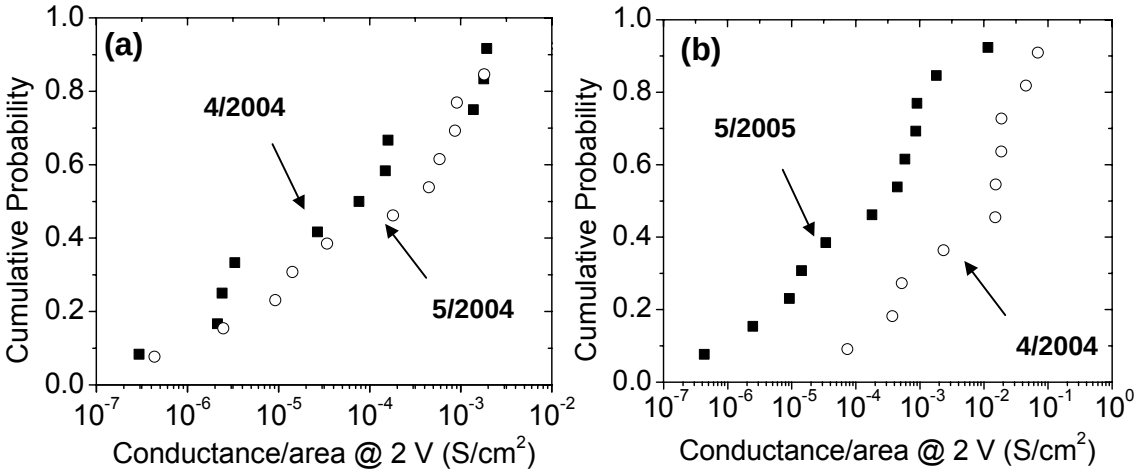


Figure 4.7. Cumulative probability plots for devices fabricated under identical conditions on different dates. (a) 8-layer devices on flat gold fabricated during 4/2004 and 5/2004. (b) 8-layer devices on regular gold fabricated in 4/2004 and 5/2005.

2004 had a mean of 5×10^{-3} S/cm^2. The null hypothesis for this case is true with a probability of 0.025, which indicates a statistically significant difference. Based on these two results, it is reasonable to compare devices fabricated within a month of each other; however, the change in processing between 2004 and 2005 (which will be discussed further in Section 4.4.1) makes comparison of devices prepared in different years unreliable.

To avoid drawing false conclusions when measuring the effect of different processing conditions on device performance, we take several precautions. First, for each batch of devices a variety of different device areas are sampled, so that the device areas in one batch are not significantly larger (or smaller) than in the batch to which it is being compared. Second, when comparing devices fabricated under different conditions, we only consider those prepared within the same month, and in most cases the same day or week.

4.3.2 Device Structure, Gold Topology, and Number of MUA layers

Devices fabricated in the PoPI structure had (on average) much lower conductances (by ~10^2) than those made with the PrPM structure, regardless of MUA thickness (Fig. 4.8). Because of the significant scatter in the conductance, the geometric mean is also plotted for each thickness and structure. Corresponding to the higher conductances shown in Figure 4.8, all devices fabricated with the PrPM structure had current-voltage characteristics similar to the high-current device shown in Fig. 4.5(a). In contrast, in the PoPI structure all three of the device types of Figure 4.5 (high, medium, and low current) were observed. PoPI devices also had significantly higher yields than PrPM structures (Fig. 4.9). We calculate yield as the fraction of unshorted devices (which include all three device types of Fig. 4.5, as even the high-current devices (Fig. 4.5(a)) had much lower current than shorted devices). The difference in structures was especially important for devices with fewer than 7 MUA layers, where no unshorted devices were measured for the PrPM structure, but yields of ~0.1 could be obtained with the PoPI structure down to 3 MUA layers.

No consistent differences were observed for devices fabricated on flat or

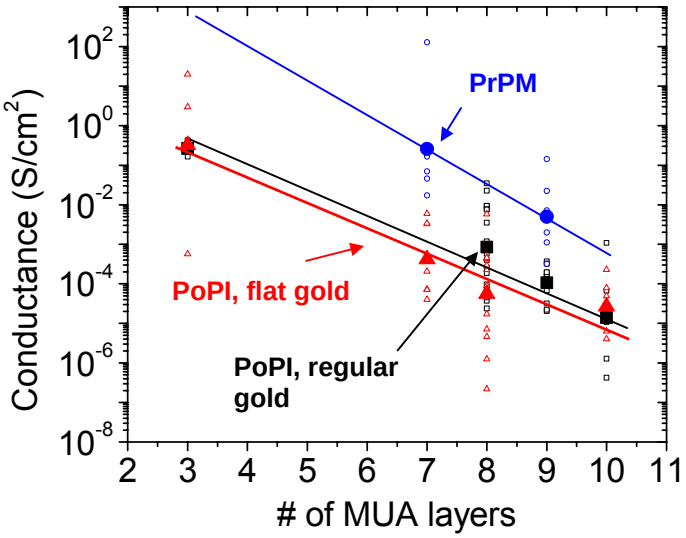


Figure 4.8. Conductance/area vs number of MUA layers for devices fabricated with PrPM structure, the PoPI structure with on regular gold, and the PoPI structure on flat gold. Hollow points represent individual data points and solid points represent their geometric mean. The conductance was measured at 0.5 V on PrPM devices and 2 V for PoPI devices.

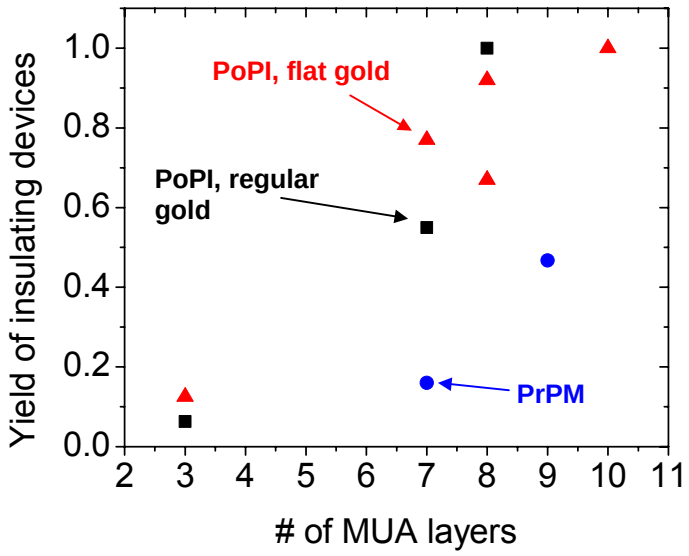


Figure 4.9. Yield of devices fabricated in PrPM structure and PoPI structures (on flat and regular gold) vs number of MUA layers. Each point represents 15 to 30 tested devices.

regular gold in the PoPI structure. Conductances on both flat and regular gold were comparable for each MUA thickness (Fig. 4.8). For devices with 7 or 8 MUA layers, the conductances of regular-gold devices were higher than for flat gold, but for devices with 3 and 10 MUA layers, regular-gold devices had slightly lower conductances than flat-gold devices. Yields were also similar (Fig. 4.9).

The number of MUA layers played a critical role, both in conductance and yield. Device conductance decreased exponentially as the number of MUA layers was increased (Fig. 4.8) for PoPI and PrPM devices. Fitting to the geometric means of the conductance at each thickness results in slopes of one decade/1.2 layers, one decade/1.7 layers, and one decade/1.6 layers for PrPM structures, regular-gold PoPI structures, and flat-gold PoPI structures, respectively. Yield increased with the number of MUA layers, and for PoPI devices with 7 to 8 layers yields near unity were regularly achieved (Fig. 4.9).

4.3.3 Deposition of the Top Metal Electrode

The angle of deposition of the top electrode played an important role in determining device characteristics. Devices with the top electrode deposited at a shallow angle (with respect to the substrate) had lower current densities than those deposited at an angle more normal to the substrate (Fig. 4.10(a)). Current density decreased from 3.6×10^{-3} S/cm^2 at 50º to 5.6×10^{-5} S/cm^2 at 20º. The yield of 0.9 for devices fabricated at a shallow angle (20º) was also higher than those fabricated at 50º, which had a yield of only 0.6 (Fig. 4.10(b)).

Replacing the top gold electrode with aluminum resulted in an enormous decrease in current density, from a (geometric) mean conductance of 0.3 S/cm^2 at 3 V for devices with a Au top electrode, to 3.6×10^{-5} S/cm^2 for devices with an Al top electrode (Fig. 4.11(a)). The temperature of the substrate during deposition of the top electrode, and the rate at which it was deposited, had much smaller effects. Decreasing the temperature of the substrate resulted in a slight decrease in conductance, from 3.4×10^{-2} S/cm^2 at 1 V (at 300 K) to 8.7×10^{-3} S/cm^2 (at 100 K) (Fig. 4.11(b)). However, this decrease corresponds to a null-hypothesis probability of 0.15, so would generally not be considered statistically significant. To confirm that the decrease was not due to the adsorption of contaminates onto the sample from the vacuum chamber while at low temperature [25], a control sample that was attached to

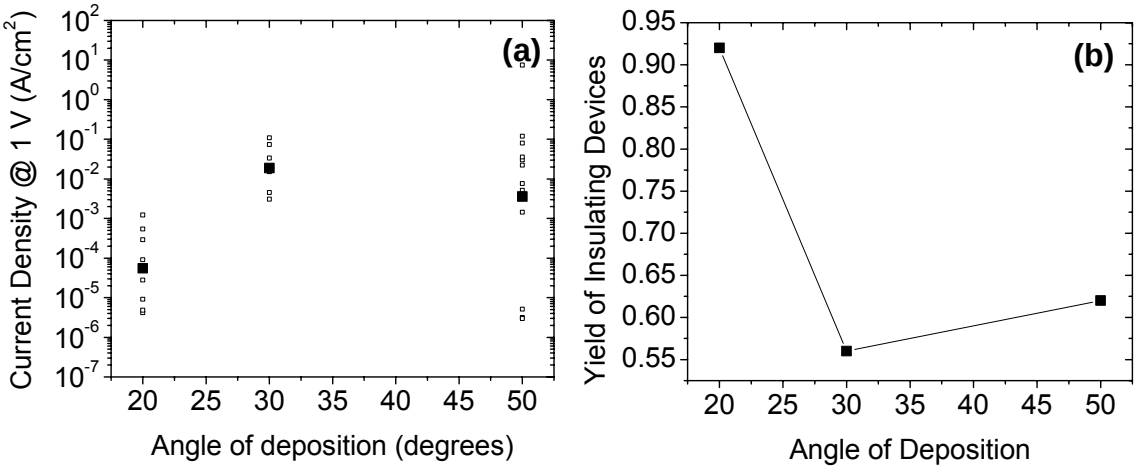


Figure 4.10. Dependence of device performance on the angle of deposition for gold electrodes deposited on a 7 MUA layer device on flat gold. (a) Current density (at 1 V). (b) Yield of insulating devices. Each point corresponds to 15 to 25 measured devices.

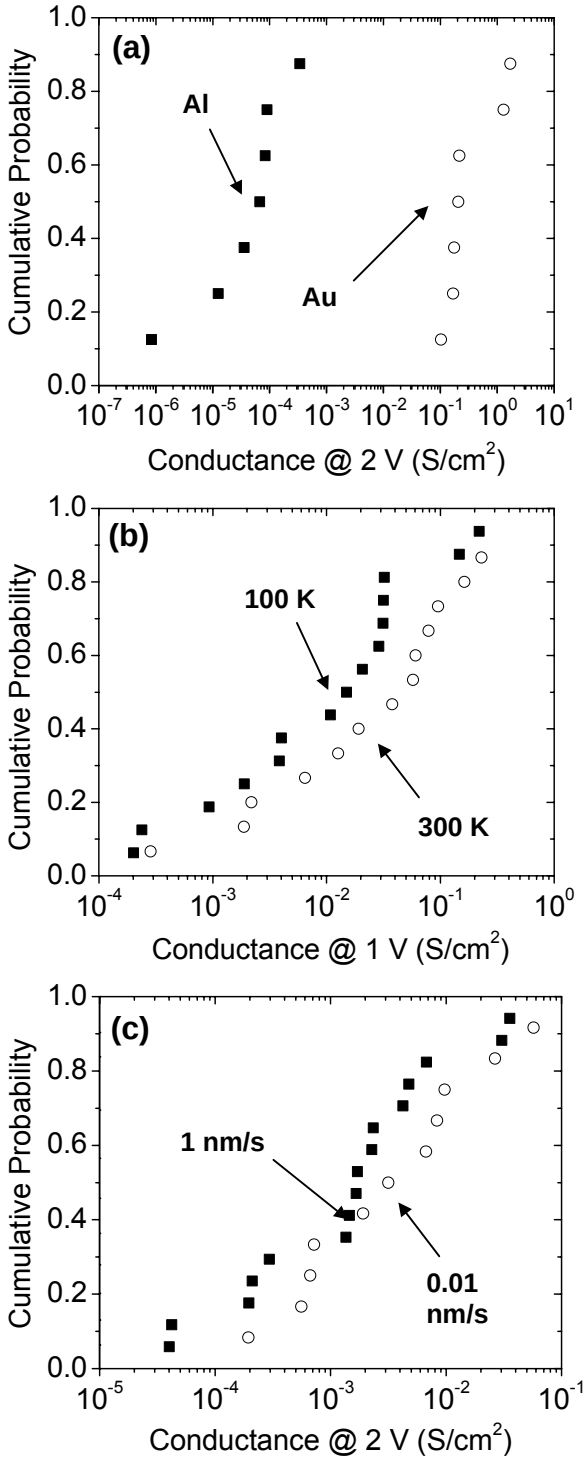


Figure 4.11. Effect of top metal deposition conditions on device conductance. (a) Cumulative probability plot of the conductance/area at 3 V of 11-layer devices fabricated with Au or Al electrodes. (b) Cumulative probability plot of the conductance/area at 1 V of 8-layer devices with top gold electrode deposited at 30º with the substrate at 100 or 300 K. (c) Cumulative probability plot of the conductance/area at 2 V of 8-layer samples with the top gold electrode deposited at 50º at rates of 1 nm/s or 0.1 nm/s.

the cooled stage during metal evaporation (but masked from the metal source) was measured by ellipsometry. No thickness increase was measured, suggesting that contamination does not play a significant role in the decreased conductance. Increasing the deposition rate from 0.01 nm/s to 1 nm/s, also resulted in a slight decrease in conductance, from $3x10^{-3}$ S/cm^2 at 2 V to $1x10^{-3}$ S/cm^2 (Fig. 4.11(c)). This decrease was even less significant, with a null hypothesis probability of 0.27. The choice of metal, substrate temperature, and deposition rate had no significant effects on device yield.

4.4 Discussion of Electrical Characteristics

We now discuss the electrical characteristics reported in Section 4.3. A prominent feature of these characteristics was the considerable scatter in the currents of the insulating devices, even in those fabricated under identical conditions. This raises a critical question: which of the device characteristics (if any) represent fundamental electron transport through MUA, and which represent imperfections in the fabrication process? For example, one could argue that in devices with the lowest conductance (Fig. 4.5(c)) we are measuring transport through the MUA layers; while in those with higher conductance (Fig. 4.5(a) and (b)) the current is dominated by electrical defects such as gold that penetrates the MUA layer, but in insufficient quantities for shorting. Alternatively, these high-conductance devices may represent transport through the MUA layer, while devices with low conductance may be a result of poor electrical contact between the gold electrodes and MUA layer. Rather than answering this question immediately, we will make the assumption that the first argument is correct, and that high currents in devices are due to electrical defects. We will show that this assumption is justified because it will allow us to provide a consistent explanation for all of the observed characteristics. Further evidence for the correctness of this assumption will also come later, when we discuss the physical mechanism for the programmable conductance observed in these films in Chapter 8. In this section, we will first discuss how the fabrication conditions affected device performance (Section 4.4.1) and summarize optimum processing conditions (Section 4.4.2). We will later relate electrical characteristics to previous results (Section 4.4.3) then focus on a group of devices having the fewest defects and discuss the physical mechanism for conductance in these devices (Section 4.4.4).

4.4.1 Role of the Fabrication Conditions in Device Performance

We first address the decrease in conductance for devices fabricated under nominally identical conditions from 2004 to 2005 (Fig. 4.7(b)). The main change in the fabrication process that occurred between 2004 and 2005 was the introduction of more careful procedures to eliminate accidental contamination by water in the $Cu(ClO_4)_2$ solution during MUA growth. As discussed in Chapter 3, water contamination led to increased MUA deposition rates. It is likely that water contamination also led to the increased conductances of the 2004 devices. An observation that supports this possibility is that in two batches of 10-layer samples prepared in 2004, higher conductances were obtained than in samples with 7 or 8 layers, in contrast to the usual trend of decreasing conductance with number of MUA layers (as in Fig. 4.8). In the cases when this occurred, ellipsometry measurements on the 10-layer samples revealed unusually large thicknesses, suggesting water contamination. A likely mechanism for the increased current densities of contaminated devices is that the uncontrolled growth decreases the quality of the deposited layer, increasing the likelihood of metal penetration. This may occur even for small amounts of contamination, leading to increased current densities for the 2004 devices even when the change in thickness was not noticeable with the ellipsometer.

The most important factor (other than number of MUA layers) in determining device conductance (and yield) was the device structure. PoPI devices had significantly lower current densities and higher yields than PrPM devices (Fig. 4.8 and 4.9), suggesting that the MUA films fabricated with PrPM structures were more likely to have defects than those on PoPI structures. Indeed, all PrPM devices had roughly linear current-voltage characteristics (resembling those of the high-current device in Fig. 4.5(a)), which we attribute to current through defects. The most likely region where defects may occur is on the edge of the pre-patterned gold layer (Fig. 4.2(c)). Previous work has shown that self-assembled monolayers grown on the edge of metal films have an increased defect density, presumably because of the increased metal roughness in these areas [26]. The presence of the thin Ti layer may also lead to defects as thiol-based monolayers do not assemble on Ti [27]. Unlike the PrPM structure, in the PoPI structure the MUA is grown on a planar gold film (Fig. 4.3(c)). This results in higher-quality, lower-conductance devices, as well as increased device yield. Growth on a planar gold film is therefore a critical advantage of the PoPI

structure because it eliminates the possibility of defects along the edge of the first gold layer that lead to poorer electrical characteristics.

The increase in conductance/area with device area for PoPI structures (Fig. 4.6) is probably due to the increased likelihood of unusually large defects in larger area devices. If defects of different sizes are distributed normally in the MUA film, as the device area increases more possible defects are sampled and there is an increased likelihood that the device will include an unusually large defect. If we make the reasonable assumption that the current is carried predominantly in the largest defect (or defects), then if an unusually large defect is included in a large-area device, its conductance/area will increase, as we observe. We also observed that the yield of large-area devices was lower than small-area devices, although no attempts to quantify this relationship were made.

A different trend is observed for PrPM structures, where the conductance/area decreases slightly as the area is increased (Fig. 4.6). In PrPM structures, the defects are likely concentrated near the edge of the first gold layer, and the conductance is therefore not as sensitive to the overlap area. Increased leakage current along the edges of a device is a general phenomenon that has been observed in a range of different devices structures and materials, including crystalline-silicon/metal Schottky diodes and amorphous silicon n-i-p diodes [28-30]. By measuring devices with differing ratios of device area to peripheral (edge) length, it is possible to distinguish between the currents due to the device area and edges (and even corners, which can have an additional contribution to the total current) [31]. Such a study is a promising avenue for future work, and may allow more detailed comparison to the devices fabricated in Chapter 5, which (as we will discuss) share some common features with these PrPM structures.

The role of gold topology in determining device characteristics was minimal (Fig. 4.8 and 4.9). Although the large flat regions in template-stripped gold presumably enable the formation of higher quality MUA layers, the surfaces of these substrates still contain trenches at the interfaces between flat gold regions (Fig. 3.7(d)). It is likely that these regions are prone to defects, offsetting any advantage that the flat regions may have in determining device conductance and yield. However, if devices with dimensions much smaller than the typical flat region (~300 nm) were fabricated so that most device areas would not overlay an interface region, this may result in higher

quality devices. Some groups have used this approach in making monolayer devices with promising results [14, 32].

Increasing the number of MUA layers decreased the device conductance and increased the yield (Fig. 4.8 and 4.9). This is due to two effects. First, as the thickness of the MUA layer is increased, its RMS roughness (as a fraction of layer thickness) decreases to <0.1 (Fig. 3.9), leading to devices with fewer defects. Second, increased MUA thickness decreased the conductance/area in low-current devices without defects. As discussed further in Section 4.4.4, in these devices the transport mechanism is Richardson-Schottky emission. Increasing the device thickness decreased the electric field (at a given voltage), leading to decreased conductance.

We now examine the role of the top electrode (and its deposition) in determining electrical conduction. The interface between metal layers evaporated onto self-assembled monolayers and other organic films has received a considerable amount of attention [33-39]. A fundamental challenge is that the lowest energy state of a metal/organic system is one in which the metal (which has a high surface energy) is covered by the organic (which has a low surface energy) [33, 34]. This lowest-energy state is the opposite of what is sought when a metal layer is evaporated onto an organic film. There is thus a tendency for an evaporated metal atom to diffuse through the organic film to reach a lower energy state, a process that can occur readily because of the thermal and/or kinetic energy of the evaporated metal atom. To minimize this possibility, we explored a number of different evaporation conditions.

The first deposition condition that we consider is the angle of deposition. We found that evaporation at a shallow angle causes a decrease in current density (by a factor of 300 from 50º to 20º) as well as an increase in yield (Fig. 4.10). These results are similar to previous work by C.-C. Kuo et al, in which shallow-angle evaporation of metal onto monolayers of mercaptohexadecanoic acid resulted in a decrease in current density by a factor of 200 with respect to deposition normal to the substrate [40]. Kuo et al argued that the decreased current was a result of the metal atom's momentum not assisting movement into the monolayer. We alter this argument slightly, and note that evaporation at a shallow angle allows pinhole defects present in our organic layer to be physically masked by adjacent molecules (Figure 4.12).

The second variable in top-metal evaporation was the choice of material. In our work, the conductance/area of devices with a top Al electrode was dramatically lower, by a factor of 10^4 at 2 V, than those with gold electrodes (Fig. 4.11(a)). One possible

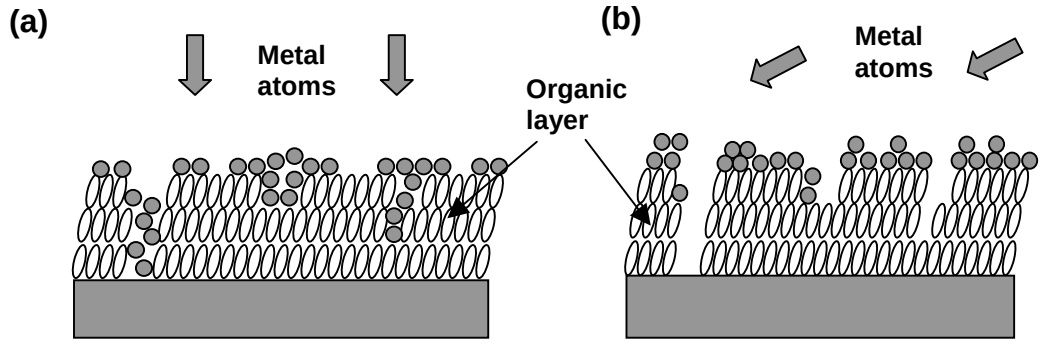


Figure 4.12. Conceptual diagrams of the interaction between evaporated metal atoms and organic layer during (a) normal and (b) shallow angle evaporations. In the normal evaporation, the metal penetrates through pinhole defects in the organic layer. In the shallow angle evaporation, these pinholes are masked by adjacent regions.

reason for the change is the different metal work functions (5.1 eV for Au and 4.1 eV for Al) resulting in different injection into the organic layer. If this were the case, we would expect to see very asymmetric current-voltage traces when measuring the devices with Au and Al electrodes. However, the current-voltage characteristics of devices with an Al electrode were only slightly asymmetric, similar to devices with two Au electrodes (Fig. 4.13(a)). A more likely source of the decreased conductance of the devices is the reactivity of the metals. Previous work has shown that noble metals (such as Au) that are relatively inert tend to penetrate into the organic layer, while more reactive metals (such as Al) react with the organic surface groups [19, 33-35]. The reaction of Al with the surface of the organic limits its ability to diffuse into the organic layer, leading to lower device conductance than devices with two gold electrodes (Fig. 4.13(b)).

Another possible approach to limiting penetration of the evaporated metal into the organic film is to cool the substrate during deposition to minimize the thermal energy available for diffusion. However, cooling the substrate to 100K during evaporation resulted in only a slight decrease of conductance, by a factor of ~3 (Fig. 4.11(b)). Other workers also report using cooled substrates during metal deposition, although no comparison was made to devices deposited at room temperature [14].

The final variable in top-metal evaporation that we consider is the evaporation rate. Deposition at higher rates lead to a very slight decrease in conductance, although the effect was not statistically significant (Fig. 4.11(c)). This appears to

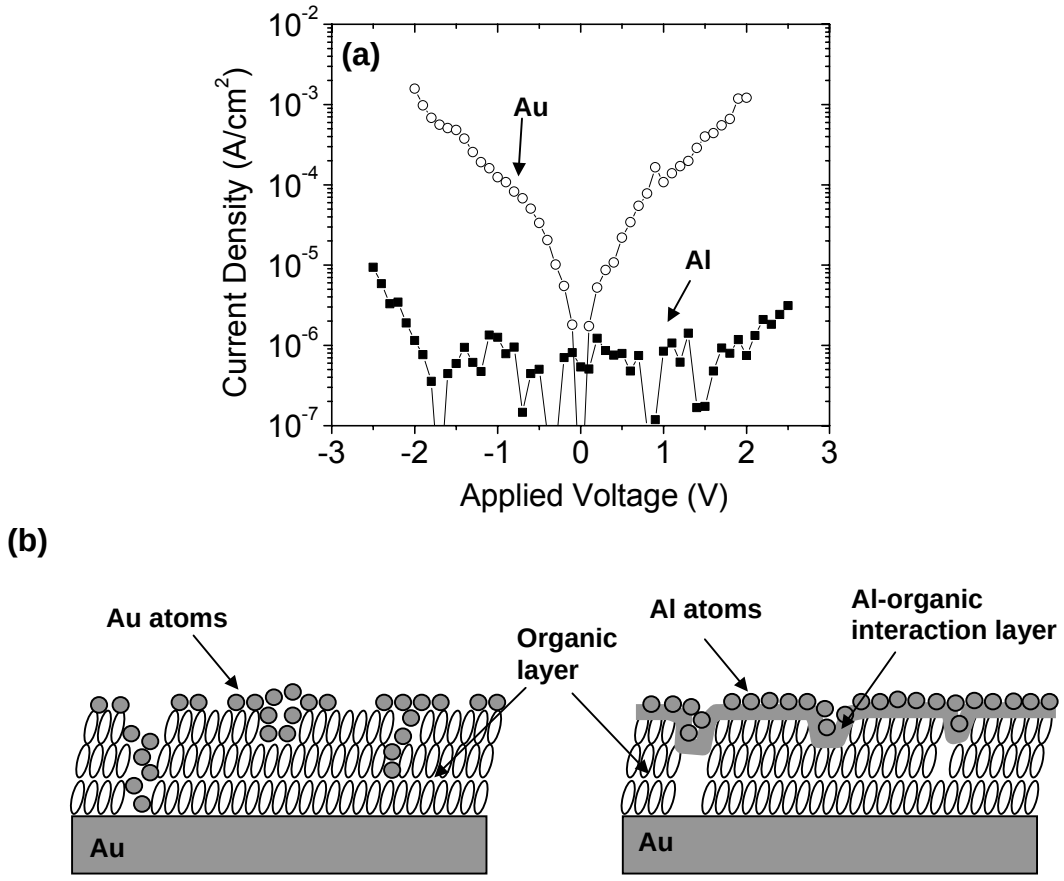


Figure 4.13. (a) Current density vs applied voltage for 11-layer devices with Al or Au top electrodes. (b) Model for the lower current density in devices with an Al electrode. Evaporated Au atoms do not interact with the organic layer and are likely to penetrate it (left). Evaporated Al atoms interact with the surface of the organic, limiting their ability to diffuse into the film (right).

contradict previous work, which reported that very slow evaporation rates were used to minimize thermal damage to the monolayer [14]. However, other studies of deposition of metals onto organic layer found that most metal diffusion into the organic layer occurs during the earliest stage of the evaporation, before the metal atoms can form large clusters [41, 42]. The initially deposited, isolated metal atoms are highly mobile and likely to diffuse into the organic layer. After a sufficient quantity of metal has been deposited, the atoms form large clusters that are stable and unlikely to diffuse into the organic. Higher deposition rates, which minimize the time prior to the formation of

large, stable clusters of metal, are therefore desirable, which may lead to the slight decrease in current density that we observe.

4.4.2 Summary of Optimum Conditions to Minimize Electrical Defects

Table 4.2 summarizes the optimum conditions to fabricate devices with a minimum number of electrical defects (so that these devices best estimate intrinsic transport through the MUA layers). For comparison we also include all the conditions explored and the typical (default) conditions used to fabricate devices (from Table 4.I). In general the default conditions that we chose were the same as the optimum conditions. For two parameters, the topology of the first gold layer (regular or flat) and the evaporation rate (0.01 to 1 nm), no significant differences between the explored conditions was observed. For these parameters the default conditions were thus determined by practical considerations: regular gold substrates were used as a default because it was relatively easy to prepare them, and slow top-electrode deposition rates (0.05 nm/s) were used because these electrodes adhered better to the sample. At fast deposition rates of 1 nm/s we found that many of the top gold electrodes peeled off of the sample (we did not investigate the cause of this peeling). Finally, although Al top electrodes resulted in much lower currents, we generally used gold as a top electrode so that both top and bottom electrode would be the same material.

For reference, we note that several workers have reported the fabrication of monolayer devices with very few defects by evaporating with an alternative technique not explored in this thesis [43-45]. In this approach, the sample is oriented so that it faces away from the evaporation source and the chamber is filled with an inert gas at low pressure (~10^{-3} torr), so that any metal deposited onto the monolayer reaches the sample indirectly and must first scatter off of the inert gas. This reduces the kinetic energy of the metal atoms and eliminates damage due to radiation from the high-temperature evaporation source. A drawback to this approach is that only a small fraction of evaporated metal reaches the organic surface, so that a very large amount of source metal must be consumed to deposit even a thin metal layer.

Fabrication parameter	Conditions explored	Optimal Condition	Typical Conditon
Device structure	PrPM or PoPI	PoPI	PoPI
Bottom gold topology	regular or flat	No difference	regular
# of MUA layers	1 to 11	-	-
Top electrode metal	gold or aluminum	aluminum	gold
Angle of deposition (degrees)	20, 30, 50	20	20
Deposition rate	0.01 to 1 nm/s	No difference	0.05 nm/s
Substrate temperature	100 or 300 K	100 K	100 K

Table 4.2. Fabrication parameters explored (from Table 4.1), as well as the optimal condition that we determined for each. In general, the typical conditions that we used correspond to these optimum conditions. The angle of deposition refers to the deposition angle (with respect to the substrate) of the second metal layer. Similarly, deposition rate refers to the deposition rate of the second metal layer, and substrate temperature is the temperature at which the sample was held during this deposition.

4.4.3 Comparison to Previous Results

In this section we compare conduction in PoPI devices with gold top and bottom devices, which formed the bulk of tested devices, to previous results. We first consider unshorted devices fabricated under all conditions (excluding only those devices fabricated with the PrPM structure or an Al electrode). We therefore include those devices classified as high- and medium-current devices ((Fig. 4.5 (a) and (b)), even though it is likely that the current in these devices is primarily carried through defects. We will later focus on only low-current devices fabricated with the optimum conditions described in Section 4.4.2; these devices provide the best estimate of intrinsic current through the MUA layer.

Previous work has shown that transport in alkanethiol monolayers is due to direct tunneling, so that the device current decreases exponentially with molecule

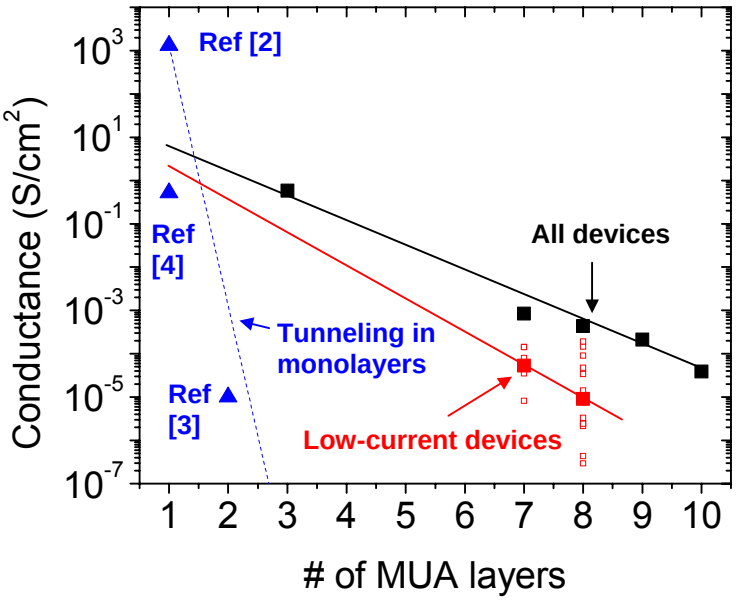


Figure 4.14. Geometric mean of the conductance/area (at 2 V) for all PoPI devices vs # of MUA layers. These results are extrapolated to a monolayer for comparison to previous work. Due to the limited data available in previous work, the conductance/area for these devices was estimated at 1 V. When necessary, monolayers of different thicknesses were adjusted to an effective thickness of 11 carbon atoms by decreasing the current density by one decade/2 carbon atoms; this factor is derived from the tunneling coefficient in alkane monolayers [6]. Also shown are the conductance/area of the 7 and 8 layer lowest-current devices (hollow red squares) and the geometric means of these devices (solid red squares).

length by a factor of one decade/2 carbon atoms [3, 4, 8, 46]. We compare our results to previous work by taking the geometric mean of the conductance/area of all devices at each thickness and extrapolating to a single layer (Fig. 4.14). Because the previous results are for alkane chains of different length, each was corrected by the factor of one decade/2 carbon atoms so that all alkane chains had an effective thickness of 11 carbon atoms before plotting in Figure 4.14 [6]. However, there was still considerable variation in the previous results. One of the main reasons for this scatter is that although thiol-gold chemistry was used self-assemble each layer, the workers used different functional groups (on the top of the monolayer) and different top metal electrodes, resulting in different charge injection barriers. Encouragingly, our extrapolated results lie relatively near the previous work (Ref [4] in Figure 4.14) that used a contact chemistry similar to ours (a carboxyl group in contact with a top gold electrode, with voltage applied to the top gold electrode). However, in our devices the current decreased relatively gradually with increased film thickness. We measure a slope of one decade/1.6 layers (= one decade/18 carbon atoms), much lower than the observed dependence on chain length in alkane monolayers. The transport mechanism in these multilayer MUA devices is therefore clearly different than the mechanism in alkane monolayers.

4.4.4 Conduction Mechanism in Low-Defect devices

For further study of conduction in MUA films, we now consider only devices prepared following the default fabrication conditions. These conditions correspond to the optimum fabrication conditions, as summarized in Section 4.4.2, with one exception. Although Al top electrodes resulted in much lower current densities than gold top electrodes, we still used gold top electrodes (so that both top and bottom electrode would be the same material). Even with these optimized conditions, fabricated devices had a wide range of device characteristics. We therefore further limit our focus to the group of devices with the lowest conductance. These low-conductance devices represent our best devices, in that (we believe) they have a minimum number of defects so that they best represent intrinsic current through the MUA film. Devices with low conductance and characteristics closely resembling the device in Fig. 4.5(c) (i.e. a predominantly exponential dependence of current on voltage) were found only in devices with 7 to 8 MUA layers. The (geometric) mean conductance of these devices was ~10x lower than the mean of all the devices, but

significant device-to-device variation of up to ~100x was still observed (Fig. 4.14). This may indicate the presence of residual defects, even in these lowest-conductance devices. An extrapolation of the conductance of this group of devices to a monolayer device yields a result similar to the extrapolation of all of the devices (Fig. 4.14).

Although a Landauer-Buttiker formalism based on first-principles calculations (Section 1.3) might be used to describe transport in devices based on single monolayers at temperatures near 0 K, here we examine devices with multiple layers, at higher temperatures. It is similarly difficult to justify using approaches that have been developed to describe transport in bulk organic films based on conjugated molecules (Section 1.4), as our films consist of MUA films interspersed with Cu layers. We therefore adopt an empirical approach, considering a number of different possible transport models and discriminating between these models based on their predicted dependence on voltage and temperature. After determining the model that best fits our results empirically, we will compare our findings with the type of charge transport that might be expected based on the UPS measurements in Section 3.4.4.

To begin this study, the electrical characteristics were measured as a function of temperature. An Arrhenius plot of the current at different voltages vs 1/*T* reveals that transport is thermally activated (Fig. 4.15). As the temperature is decreased from 325 to 200 K, the current at each voltage decreases by a factor of almost 100. At

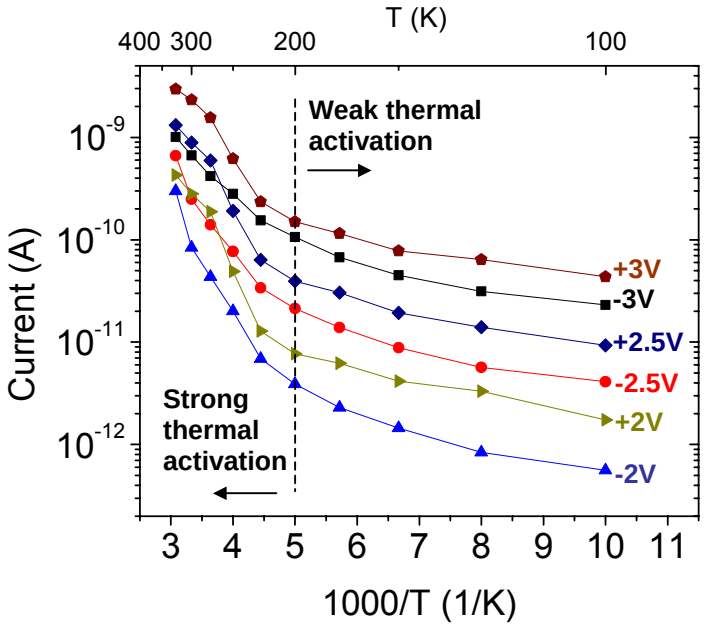


Figure 4.15. Current at different voltages vs 1000/T for 8 MUA layer device.

Conduction Mechanism	Voltage Dependence	Temperature Dependence	Thickness Dependence
Direct Tunneling [46, 48]	J~V (low V)	None	J~exp(-βd)
Hopping [46, 48]	J~V (low V)	J~exp(-a/T)	J~1/d
Poole-Frenkel (PF) [46, 48]	J~exp(bV^{½})	J~exp(-a/T)	J~exp(c/d^{½})
Richardson-Schottky emission (RS) [46, 48]	J~exp(bV^{½})	J~T^2 exp(-a/T)	J~exp(c/d^{½})
Fowler-Nordheim tunneling [46, 48]	J~V^2 exp(-b/V)	None	J~exp(-cd)
Space-charge limited [49]	J~V^2	None (first order)	J~1/d^3

Table 4.3. The most common conduction mechanisms in organic thin films, and their predicted dependence on voltage, temperature, and device thickness.

lower temperatures, a more shallow decrease is observed, and the current decreases by a factor of ~2 between 200 and 100 K. A gradual leveling of the temperature dependence at low temperatures is common in organic semiconductor devices [47].

Table 4.3 lists the voltage, temperature, and thickness dependence of some models commonly applied to organic thin films. The strong temperature dependence and nonlinear current-voltage characteristics allow the direct tunneling, hopping, Fowler-Nordheim tunneling, and space-charge limited mechanisms to be discarded, leaving Poole-Frenkel (PF) conduction and Richardson-Schottky (RS) emission as the most likely possibilities. A semilog plot of current vs $V^{½}$ results in a straight line at large voltages, further confirming the likelihood of PF conduction or RS emission (Fig. 4.16).

Although the PF and RS mechanisms have slightly different temperature dependences, it can be difficult to distinguish between them on this basis alone because the shared exponential factor dominates the T^2 pre-exponential factor in thermionic emission. From a physical perspective, both mechanisms are field (rather than voltage) dependent, and involve the lowering of a barrier to allow transport of thermally excited carriers over the barrier. In the PF effect, the relevant barrier is the coulombic potential of a charged trap in the bulk of the material (Fig. 4.17(a)) [50]. In RS emission, the barrier between the electrode and insulator is lowered by the field and the image potential of the emitted charge (Fig. 4.17(b)). RS emission is electrode-

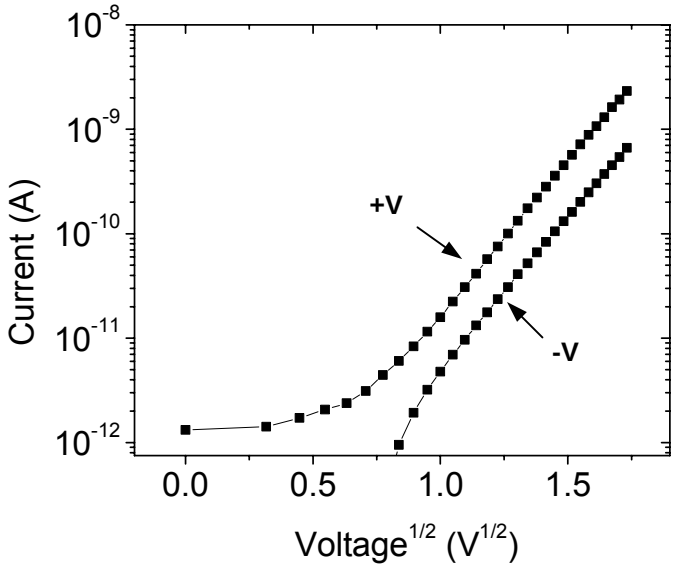


Figure 4.16. Current vs square root of voltage applied to the top electrode on an 8-layer MUA device at 300 K.

dependent, while PF conduction is bulk-limited. In both mechanisms, after the charge is emitted from the electrode or trap, it is assumed to undergo band-like transport through the film. This is clearly inappropriate for conduction in most organic solids (including the MUA film that we are studying). Nevertheless, these models (or variations of these models) are often used to describe transport in organics even though it can be difficult to strictly justify their use [47, 51]. As we will discuss in the context of our results, it is thus important to be careful when assigning physical meaning to the parameters that are used to fit the models to the observed characteristics.

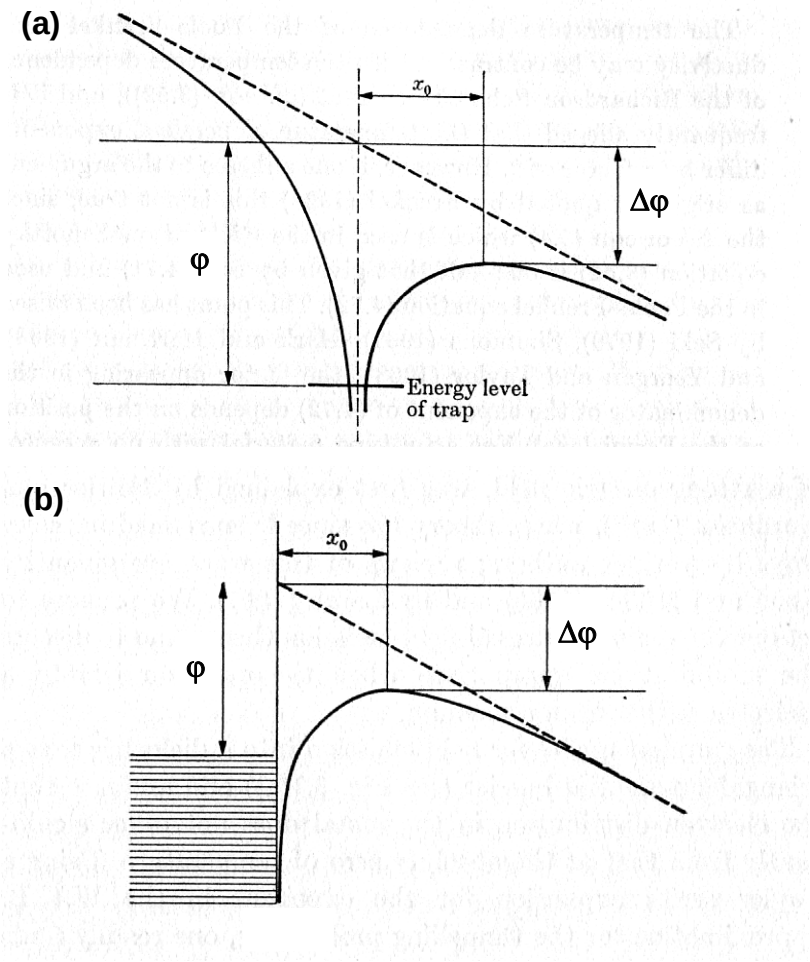


Figure 4.17. Schematic of (a) Poole-Frenkel and (b) Richardson-Schottky conduction mechanisms (from Ref [1]). A zero-field barrier φ due to a trap in the bulk of the film (PF) or the injection barrier from an electrode (RS) exists. When an electric field is applied, the potential due to electric field (dotted line) and coulombic potential (from the charged trap in PF or an image charge in RS) combine to lower the barrier by Δφ at a distance x_0 from the trap or electrode. A charge-carrier can then be thermally excited over the reduced barrier (φ-Δφ).

Because of the very thin nature of the films as well as the asymmetry of the current-voltage characteristics (Fig. 4.16), the contact-limited RS mechanism is a more likely conduction mechanism than bulk-limited PF conduction. The current predicted by RS theory is exponentially related to the square root of the electric field [52]:

$$J = AT^2 \exp[-\frac{\varphi - (e^3 / 4\pi\varepsilon\varepsilon_0)^{1/2}(V/d)^{1/2}}{kT}], \quad (1)$$

where *J* is the current density, *A* is a constant known as Richardson's constant, φ is the zero-field barrier between the metal and insulator, ε is the dielectric constant of the insulator, and *d* is the thickness of the insulator. Note that in (1) we have assumed that the electric field is equal to *V/d*. Neglecting Richardson's constant (which prior work has shown to be up to 10 orders of magnitude lower than its theoretical value when this model is applied to organic films [47, 49]), we wish to extract values for the coefficients φ and ε.

To determine φ, we first plot ln (J/T^2) vs *1/T* (for 200 K < *T* < 325 K) for different values of *V*. The slopes of these plots (multiplied by *k*) as a function of $V^{½}$ are shown in Figure 4.18. Each slope is equal to the quantity $\varphi - (e^3 / 4\pi\varepsilon\varepsilon_0)^{1/2}(V/d)^{1/2}$, so by linear extrapolation to V = 0, we obtain φ = 0.38 V for positive bias on the top electrode and φ = 0.43 eV for negative bias. The value of ε can be determined from a plot of ln(*J*) vs $V^{½}$, the slope of which is equal to $(e^3 / 4\pi\varepsilon\varepsilon_0)^{1/2} / kTd^{1/2}$. By measuring the film thickness *d* with ellipsometry, we find an average value for all of the low-conductance devices of ε = 4.4±0.9.

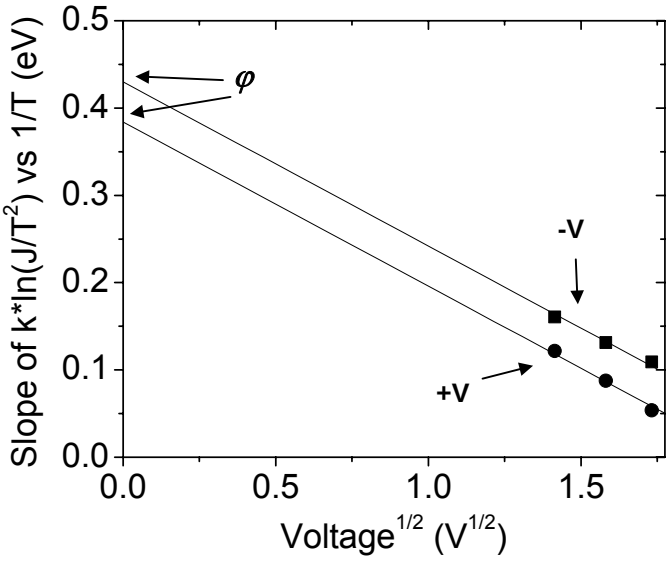


Figure 4.18. Slope of plot of ln(J/T^2) vs 1/*T* plotted against the square root of voltage. The slope is multiplied by k to convert to units of eV. Linear extrapolation of the plot to *V* = 0 yields the zero-field injection barrier φ (= 0.38 eV for positive bias on the top electrode and 0.43 eV for negative bias). To extrapolate to 0 V, a best-fit slope for both data sets was determined.

The slight offset between the injection barriers for positive and negative bias on the top electrode (0.38 V compared to 0.43 V) is expected due to the different chemistries on the top electrode (where evaporated gold contacts the COOH group in the MUA) and the bottom electrode (where S binds to predeposited gold). Measurements of tunneling in monolayers revealed a barrier height of 1.4 eV for transport from a gold electrode through alkane chains, much higher than observed here [46]. Moreover, because we believe the injection is contact-limited, it is reasonable to compare this extracted barrier height with the barrier height predicted by UPS (Section 3.4.4). We adapt the speculative energy-level diagram (Fig. 3.13(b)) here as Figure 4.19 for easy comparison. From the UPS measurements, we determined a barrier of Φ_{HOMO}= 4.4 eV for hole-injection from the gold Fermi level into the MUA HOMO, and estimate a barrier as low as Φ_{FTS}= 2.4 eV for injection into filled trap states above the HOMO. Both of these barriers are much larger than the RS barrier that we measure (φ ~ 0.4 eV). Alternatively, the charge may be injected into the LUMO, or empty trap states. Because UPS cannot detect these states, we speculate that the position of the LUMO is 7 to 9 eV above the HOMO (based on previous work on alkane chains [21, 22]). This results in an injection barrier of Φ_{LUMO} = 2.7 to 4.7 eV.

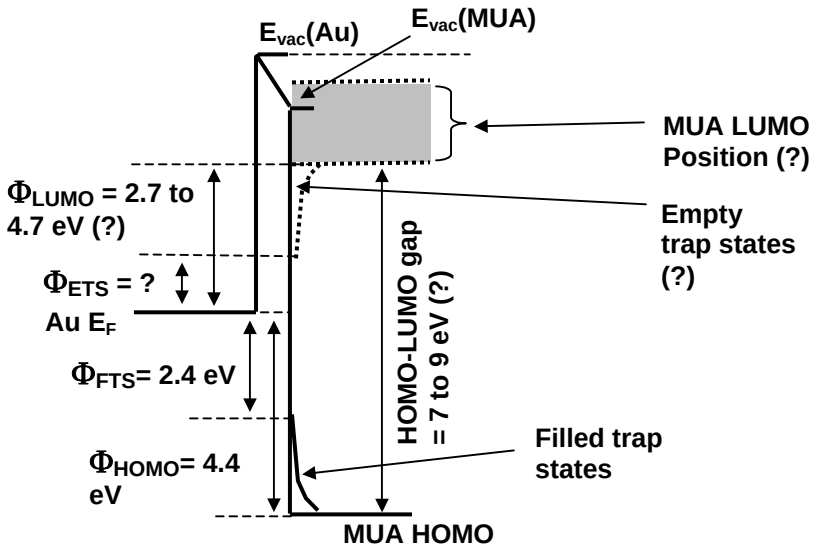


Figure 4.19. Speculative energy-level diagram of Au-MUA (monolayer or multilayer) system determined by UPS and assuming a HOMO-LUMO gap of 7 to 9 eV (adapted from Fig. 3.13, with some details removed for clarity).

It is also reasonable to believe that empty trap states also exist [22]; if these states are symmetric to the filled states and extend ~2 eV below the LUMO, then we find a much lower injection barrier Φ_{ETS} = 0.7 to 2.7 eV. The lower end of this estimate approaches our RS value of φ ~ 0.4 eV.

Apart from the speculated existence of empty trap states that may enable an injection barrier similar to the one we observe, our RS estimate of the barrier is much lower than would be expected based on the alignment of HOMO and LUMO levels of the MUA with the gold electrode. However, it is relatively common to observe much lower RS barriers than would be expected for injection into large HOMO-LUMO gap organics [22]. This is likely due in part to the fact that, as mentioned earlier, the RS model used to derive the barrier height was developed for crystalline materials with band-like conduction and so is not directly applicable to disordered organic films. Numerical modeling of charge injection from a metal into an organic film indicates that direct fitting with the RS equation can result in barriers that severely underestimate the true barrier [49, 53, 54]. Modeling also suggests that in injection-limited transport, the charge may be injected into intermediate states (with smaller barriers) before entering the bulk of the film [47, 49]. The intermediate levels could result in a lower effective barrier in the RS transport that we obtain. Indeed, we do measure levels above the HOMO in UPS (shown as filled trap states in Fig. 4.19), although as we have discussed earlier even injection into these levels involves a large barrier of Φ_{FTS}= 2.4 eV. However, it is important to recognize that it is unlikely that thermal excitation over a barrier (as in the RS model) is the sole active transport mechanism in the films. Tunneling also may play an important role: for example, charge carriers might tunnel into states within the HOMO-LUMO gap, then be thermally excited into other traps or the HOMO or LUMO [22]. Finally, although we did not observe states that we could attribute to the Cu layers in a multilayer MUA film during UPS (which may be due to the limited escape depth of photoemitted electrons, as discussed in Section 3.4.4), it seems likely that these layers contribute states with energies that would lie within the HOMO-LUMO gap of MUA, potentially decreasing the barrier to charge injection.

There is also a discrepancy between the dielectric constant that we obtain (4.4±0.9 V) and those of previous measurements on alkane monolayers (2.4 to 3.0) [9]. However, estimating the dielectric constant from the RS model often results in inaccuracies, so that agreement even within an order of magnitude can be considered

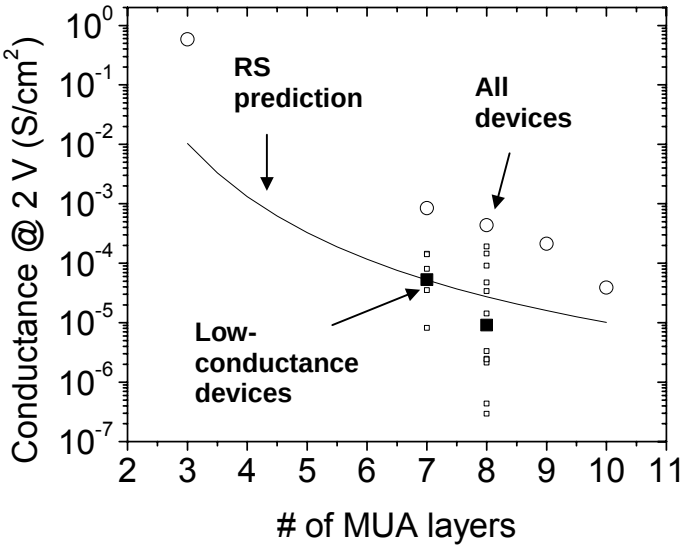


Figure 4.20. Predicted dependence of conductance on # of MUA layers (based on RS theory) compared to measured dependence in low-conductance devices (squares, with solid squares representing geometric mean and hollow squares representing data) and measured dependence in all insulating devices (solid circles represent geometric mean conductance of all devices at each thickness). The RS prediction was normalized to the mean conductance of the low-conductance 7-layer devices.

reasonable [14, 49, 55]. One likely source of error in our estimate is that the electric field is calculated using the average film thickness *d*. Because of the surface roughness of the film and electrodes, the local field will be significantly higher than this estimate in some regions. When fitting, an underestimation of the field results in an overestimation of the dielectric constant.

If the Richardson constant is chosen so that the RS equation yields the correct average current for the low-conductance 7-layer devices, it predicts a conductance for the 8-layer devices that is slightly too shallow (Fig. 4.20). The relatively shallow $J \sim \exp(1/d^{½})$ dependence predicted by the RS equation more closely matches the relationship between conductance thickness obtained by averaging all of the PoPI devices (also shown in Fig. 4.20).

4.5 Summary

In this chapter, we have described the fabrication and electrical testing of two-terminal devices with MUA as the active layer. These devices used an evaporated top metal electrode so that they are compatible with integration into circuits. Due to the very thin nature of the MUA active layer, a key challenge was minimizing the diffusion of the evaporated metal into the MUA, which led to electrically shorted devices with very high current densities (10^7 A/cm^2 at 1 V) or in some cases insulating devices with large leakage currents (up to 10^2 A/cm^2 at 1 V).

We found that devices made with a post-patterned insulator (PoPI) structure had higher yields and lower conductances than those fabricated with a pre-patterned metal layer (PrPM). The growth of MUA on the edge of the pre-patterned metal layer may have resulted in an increased number of defects, leading to the lower performance of the PrPM devices. The optimal condition for depositing the top metal electrode was at a shallow angle at low temperature. The shallow angle evaporation allowed the areas surrounding pinholes to mask these defects during evaporation. When aluminum (which reacts with the surface of the organic) was used as the top metal layer, much lower current densities were observed than when gold (which is relatively inert and therefore more likely to diffuse into the organic) was used. Other fabrication conditions, such as the topology of the bottom gold layer and the evaporation rate of the top metal, had much lower or negligible effects on device performance.

Device conductance depended strongly on the number of MUA layers, decreasing by one decade/1.6 MUA layers. Device yield also increased, and yields near unity could be obtained for devices having more than 7 MUA layers. A group of 7 and 8 layer MUA devices with very low conductance (corresponding to very few electrical defects) were chosen for further study. It was found that charge transport in these devices was injection-limited, and could be described as Richardson-Schottky emission over an injection barrier of ~0.4 eV.

References

[1] J. J. O'Dwyer, *The Theory of Electrical Breakdown in Solid Dielectrics*. 1973, Oxford: Clarendon Press.

[2] X. D. Cui, A. Primak, X. Zarate, J. Tomfohr, O. F. Sankey, A. L. Moore, T. A. Moore, D. Gust, G. Harris and S. M. Lindsay, "Reproducible Measurement of Single-Molecule Conductivity" *Science* **294** (5542), 571-574 (2001).

[3] M. A. Rampi and G. M. Whitesides, "A Versatile Experimental Approach for Understanding Electron Transport through Organic Materials" *Chemical Physics* **281** (2-3), 373-391 (2002).

[4] J. K. N. Mbindyo, T. E. Mallouk, J. B. Mattzela, I. Kratochvilova, B. Razavi, T. N. Jackson and T. S. Mayer, "Template Synthesis of Metal Nanowires Containing Monolayer Molecular Junctions" *Journal of the American Chemical Society* **124** (15), 4020-4026 (2002).

[5] B. A. Mantooth and P. S. Weiss, "Fabrication, Assembly, and Characterization of Molecular Electronic Components" *Proceedings of the IEEE* **91** (11), 1785-1802 (2003).

[6] D. J. Wold and C. D. Frisbie, "Fabrication and Characterization of Metal-Molecule-Metal Junctions by Conducting Probe Atomic Force Microscopy" *Journal of the American Chemical Society* **123** (23), 5549-5556 (2001).

[7] R. Haag, M. A. Rampi, R. E. Holmlin and G. M. Whitesides, "Electrical Breakdown of Aliphatic and Aromatic Self-Assembled Monolayers Used as Nanometer-Thick Organic Dielectrics" *Journal of the American Chemical Society* **121** (34), 7895-7906 (1999).

[8] R. E. Holmlin, R. F. Ismagilov, R. Haag, V. Mujica, M. A. Ratner, M. A. Rampi and G. M. Whitesides, "Correlating Electron Transport and Molecular Structure in Organic Thin Films" *Angewandte Chemie-International Edition* **40** (12), 2316 (2001).

[9] M. A. Rampi, O. J. A. Schueller and G. M. Whitesides, "Alkanethiol Self-Assembled Monolayers as the Dielectric of Capacitors with Nanoscale Thickness" *Applied Physics Letters* **72** (14), 1781-1783 (1998).

[10] C. J. Muller, B. J. Vleeming, M. A. Reed, J. J. S. Lamba, R. Hara, L. Jones and J. M. Tour, "Atomic Probes: A Search for Conduction through a Single Molecule" *Nanotechnology* **7** (4), 409-411 (1996).

[11] M. A. Reed, C. Zhou, C. J. Muller, T. P. Burgin and J. M. Tour, "Conductance of a Molecular Junction" *Science* **278** (5336), 252-254 (1997).

[12] J. Chen, M. A. Reed, A. M. Rawlett, D. W. Price and J. M. Tour, "Large on-Off Ratios and Negative Differential Resistance in a Molecular Electronic Device" *Science* **286**, 1550-1552 (1999).

[13] M. A. Reed, J. Chen, A. M. Rawlett, D. W. Price and J. M. Tour, "Molecular Random Access Memory Cell" *Applied Physics Letters* **78** (23), 3735-3737 (2001).

[14] C. Zhou, M. R. Deshpande, M. A. Reed, L. Jones and J. M. Tour, "Nanoscale Metal Self-Assembled Monolayer Metal Heterostructures" *Applied Physics Letters* **71** (5), 611-613 (1997).

[15] I. Amlani, A. M. Rawlett, L. A. Nagahara and R. K. Tsui, "Hybrid Assembly Technique Using Alternating Current Field for Molecular Electronic Measurements" *Journal of Vacuum Science & Technology B* **20** (6), 2802-2805 (2002).

[16] J. G. Kushmerick, D. B. Holt, J. C. Yang, J. Naciri, M. H. Moore and R. Shashidhar, "Metal-Molecule Contacts and Charge Transport across Monomolecular Layers: Measurement and Theory" *Physical Review Letters* **89** (5), 086802 (2002).

[17] R. P. Andres, T. Bein, M. Dorogi, S. Feng, J. I. Henderson, C. P. Kubiak, W. Mahoney, R. G. Osifchin and R. Reifenberger, ""Coulomb Staircase" at Room Temperature in a Self-Assembled Molecular Nanostructure" *Science* **272** (5266), 1323-1325 (1996).

[18] Y. L. Loo, R. L. Willett, K. W. Baldwin and J. A. Rogers, "Interfacial Chemistries for Nanoscale Transfer Printing" *Journal of the American Chemical Society* **124** (26), 7654-7655 (2002).

[19] B. de Boer, M. M. Frank, Y. J. Chabal, W. R. Jiang, E. Garfunkel and Z. Bao, "Metallic Contact Formation for Molecular Electronics: Interactions between Vapor-Deposited Metals and Self-Assembled Monolayers of Conjugated Mono- and Dithiols" *Langmuir* **20** (5), 1539-1542 (2004).

[20] M. T. Lee, C. C. Hsueh, M. S. Freund and G. S. Ferguson, "Air Oxidation of Self-Assembled Monolayers on Polycrystalline Gold: The Role of the Gold Substrate" *Langmuir* **14** (22), 6419-6423 (1998).

[21] A. Salomon, D. Cahen, S. Lindsay, J. Tomfohr, V. B. Engelkes and C. D. Frisbie, "Comparison of Electronic Transport Measurements on Organic Molecules" *Advanced Materials* **15** (22), 1881-1890 (2003).

[22] G. Teyssedre and C. Laurent, "Charge Transport Modeling in Insulating Polymers: From Molecular to Macroscopic Scale" *IEEE Transactions on Dielectrics and Electrical Insulation* **12** (5), 857-875 (2005).

[23] *Normal Probability Plot Interpretation*. Statit Software Services [cited 11-11-2005; webpage]. Available from: http://www.statit.com/support/quality_practice_tips/normal_probability_plot_interpre.htm.

[24] G. E. P. Box, W. G. Hunter and J. S. Hunter, *Statistics for Experimenters: An Introduction to Design, Data Analysis, and Model Building*. Wiley Series in Probability and Mathematical Statistics, ed. V. Barnett, R. A. Bradley, N. I. Fisher, J. S. Hunter, J. B. Kadane, D. G. Kendall, A. F. M. Smith, S. M. Stigler, J. Teugels and G. S. Watson. 1978: John Wiley and Sons.

[25] B. De Boer and Z. Bao, Personal Communication (2003).

[26] A. J. Black, K. E. Paul, J. Aizenberg and G. M. Whitesides, "Patterning Disorder in Monolayer Resists for the Fabrication of Sub-100-Nm Structures in Silver, Gold, Silicon, and Aluminum" *Journal of the American Chemical Society* **121** (36), 8356-8365 (1999).

[27] H. Yang, J. C. Love, F. Arias and G. M. Whitesides, "Electroforming of Copper Structures at Nanometer-Sized Gaps of Self-Assembled Monolayers on Silver" *Chemistry of Materials* **14** (3), 1385-1390 (2002).

[28] K. Al-Baidhawi, M. J. Howes and D. V. Morgan, "The Modelling of Edge Current in Schottky Barrier Devices" *Journal of Physics D-Applied Physics* **11**, 1203-1210 (1977).

[29] E. A. Schiff, R. A. Street and R. L. Weisfield, "Reverse Bias Currents in Amorphous Silicon nip Sensors" *Journal of Non-Crystalline Solids* **198-200**, 1155-1158 (1996).

[30] J. Vanhellemont, E. Simoen and C. Claeys, "Extraction of the Minority Carrier Recombination Lifetime from Forward Diode Characteristics" *Applied Physics Letters* **66** (21), 2894-2896 (1995).

[31] M. Mulato, C. M. Hong and S. Wagner, "Size and Etching Effects on the Reverse Current of a-Si:H P-I-N Diodes" *Journal of the Electrochemical Society* **150** (12), G735-G738 (2003).

[32] N. Majumdar, N. Gergel, D. Routenber, J. C. Bean, L. R. Harriott, B. Li, L. Pu, Y. Yao and J. M. Tour, "Nanowell Device for the Electrical Characterization of Metal-Molecule-Metal Junctions" *Journal of Vacuum Science & Technology B-Microelectronics and Nanometer Structures* **23** (4), 1417-1421 (2005).

[33] D. R. Jung and A. W. Czanderna, "Chemical and Physical Interactions at Metal Self-Assembled Organic Monolayer Interfaces" *Critical Reviews in Solid State and Materials Sciences* **19** (1), 1-54 (1994).

[34] D. R. Jung, A. W. Czanderna and G. C. Herdt, "Interactions and Penetration at Metal/Self-Assemble Organic Monolayer Interfaces" *Journal of Vacuum Science & Technology A-Vacuum Surfaces and Films* **14** (3), 1779-1787 (1996).

[35] A. V. Walker, T. B. Tighe, O. M. Cabarcos, M. D. Reinard, B. C. Haynie, S. Uppili, N. Winograd and D. L. Allara, "The Dynamics of Noble Metal Atom Penetration through Methoxy-Terminated Alkanethiolate Monolayers" *Journal of the American Chemical Society* **126** (12), 3954-3963 (2004).

[36] G. L. Fisher, A. V. Walker, A. E. Hooper, T. B. Tighe, K. B. Bahnck, H. T. Skriba, M. D. Reinard, B. C. Haynie, R. L. Opila, N. Winograd and D. L. Allara, "Bond Insertion, Complexation, and Penetration Pathways of Vapor-Deposited

Aluminum Atoms with HO- and CH_3O-Terminated Organic Monolayers" *Journal of the American Chemical Society* **124** (19), 5528-5541 (2002).

[37] G. L. Fisher, A. E. Hooper, R. L. Opila, D. L. Allara and N. Winograd, "The Interaction of Vapor-Deposited Al Atoms with CO_2H Groups at the Surface of a Self-Assembled Alkanethiolate Monolayer on Gold" *Journal of Physical Chemistry B* **104** (14), 3267-3273 (2000).

[38] G. L. Fisher, A. Hooper, R. L. Opila, D. R. Jung, D. L. Allara and N. Winograd, "The Interaction between Vapor-Deposited Al Atoms and Methylester-Terminated Self-Assembled Monolayers Studied by Time-of-Flight Secondary Ion Mass Spectrometry, X-Ray Photoelectron Spectroscopy and Infrared Reflectance Spectroscopy" *Journal of Electron Spectroscopy and Related Phenomena* **99**, 139-148 (1999).

[39] K. Konstadinidis, P. Zhang, R. L. Opila and D. L. Allara, "An in-Situ X-Ray Photoelectron Study of the Interaction between Vapor-Deposited Ti Atoms and Functional-Groups at the Surfaces of Self-Assembled Monolayers" *Surface Science* **338** (1-3), 300-312 (1995).

[40] C.-C. Kuo, C. V. Baiocco, J. K. N. Mbindyo and T. N. Jackson, "Large Area Metal/SAM/Metal Devices by Oblique Evaporation" *44th Electronic Materials Conference Digest*, 2-3 (2002).

[41] M. Scharnberg, J. Hu, J. Kanzow, K. Ratzke, R. Adelung, F. Faupel, C. Pannemann, U. Hilleringmann, S. Meyer and J. Pflaum, "Radiotracer Measurements as a Sensitive Tool for the Detection of Metal Penetration in Molecular-Based Organic Electronics" *Applied Physics Letters* **86** (2), 024104 (2005).

[42] M. Scharnberg, J. Kanzow, K. Ratzke, R. Adelung, F. Faupel, S. Meyer and J. Pflaum, "Radiotracer Diffusion Measurements of Noble Metal Atoms in Semiconducting Organic Films" *Materials Research Society Symposium Proceedings* **871E**, I6.31.1 (2005).

[43] H. Haick, M. Ambrico, J. Ghabboun, T. Ligonzo and D. Cahen, "Contacting Organic Molecules by Metal Evaporation" *Physical Chemistry Chemical Physics* **6**, 4538-4541 (2004).

[44] S. Lodha and D. B. Janes, "Enhanced Current Densities in Au/Molecule/Gaas Devices" *Applied Physics Letters* **85** (14), 2809-2811 (2004).

[45] R. M. Metzger, T. Xu and I. R. Peterson, "Electrical Rectification by a Monolayer of Hexadecylquinolinium Tricyanoquinodimethanide Measured between Macroscopic Gold Electrodes" *Journal of Physical Chemistry B* **105** (30), 7280-7290 (2001).

[46] W. Y. Wang, T. Lee and M. A. Reed, "Mechanism of Electron Conduction in Self-Assembled Alkanethiol Monolayer Devices" *Physical Review B* **68** (3), 035416 (2003).

[47] M. A. Baldo and S. R. Forrest, "Interface-Limited Injection in Amorphous Organic Semiconductors" *Physical Review B* **64** (8), 085201 (2001).

[48] R. L. McCreery, "Molecular Electronic Junctions" *Chemistry of Materials* **16** (23), 4477-4496 (2004).

[49] S. Barth, U. Wolf, H. Bassler, P. Muller, H. Riel, H. Vestweber, P. F. Seidler and W. Riess, "Current Injection from a Metal to a Disordered Hopping System. Iii. Comparison between Experiment and Monte Carlo Simulation" *Physical Review B* **60** (12), 8791-8797 (1999).

[50] J. G. Simmons, "Poole-Frenkel Effect and Schottky Effect in Metal-Insulator-Metal Systems" *Physical Review* **155** (3), 657 (1967).

[51] N. Tessler and Y. Roichman, "Amorphous Organic Molecule/Polymer Diodes and Transistors-Comparison between Predictions Based on Gaussian or Exponential Density of States" *Organic Electronics* (In press)(2005).

[52] D. Braun, "Electronic Injection and Conduction Processes for Polymer Devices" *Journal of Polymer Science Part B-Polymer Physics* **41** (21), 2622-2629 (2003).

[53] U. Wolf, V. I. Arkhipov and H. Bassler, "Current Injection from a Metal to a Disordered Hopping System. I. Monte Carlo Simulation" *Physical Review B* **59** (11), 7507-7513 (1999).

[54] V. I. Arkhipov, U. Wolf and H. Bassler, "Current Injection from a Metal to a Disordered Hopping System. Ii. Comparison between Analytic Theory and Simulation" *Physical Review B* **59** (11), 7514-7520 (1999).

[55] L. B. Schein, A. Peled and D. Glatz, "The Electric-Field Dependence of the Mobility in Molecularly Doped Polymers" *Journal of Applied Physics* **66** (2), 686-692 (1989).

Chapter 5

Edge Device Fabrication and Electrical Measurements

5.1 Introduction

A drawback of the planar devices described in Chapter 4 is their relatively large device areas (10 to > 1000 μm^2) due to the exclusive use of shadow masks for patterning the metal layers. Shadow masks were used to pattern the metal layers because of the limited compatibility of self-assembled films with the solvents used in photolithography. Smaller device areas are desirable, both to decrease the possibility of metal penetration through the organic layer and for application in highly scaled circuits. In this chapter, we describe an approach for making molecular-scale devices with areas of 0.1 to 0.5 μm^2. As in the preparation of planar devices in Chapter 4, we use vacuum evaporation to deposit all of the metal films used to contact the layers, so that our devices structures are compatible with the fabrication of large numbers of devices with integrated metal wiring for practical application. We test the structure by using it to make measurements on MUA in this chapter, and later use it to fabricate molecular-scale memory devices in Chapter 7.

Our approach to prepare minimal-area devices was conceived in collaboration with Dr. Zhenan Bao. Device development, processing, and characterization were done at Princeton University. The approach that we developed for minimizing device area takes advantage of the relative ease with which most vertical dimensions in semiconductor processing (such as layer thickness) can be controlled. For example, the UV photolithography tools that are widely available to university research laboratories (like the Karl Suss MA-6 and MJB-3 mask aligners in the cleanroom at the Princeton Institute for the Science and Technology of Materials) can pattern features down to ~500 nm. In manufacturing, advanced photolithography tools can reach much higher resolutions (<100 nm); but at prohibitive costs [2]. Alternatively, e-beam lithography can be used to achieve even higher resolutions below 20 nm, but again are very costly [3]. In contrast, metal layers are routinely deposited in (relatively

inexpensive) thermal evaporators with thickness controlled to ~1 nm. A number of previous workers have exploited this precision in the vertical dimension to pattern device features [3-5]. A critical difference between this work and most previous efforts is that in our work we do not require any polishing or cleaving steps when using the deposited layer to define device dimensions [4]. Our approach is therefore more compatible with low-cost, large-scale integration.

This chapter is organized as follows. Initial development of the structure is described in Section 5.2, and then device fabrication is described in Section 5.3. In Sections 5.4 we present electrical characterization of these devices with self-assembled MUA as the active organic layer. We discuss these results in Section 5.5. Section 5.6 suggests a promising approach to further developing this structure to make molecular-scale, three-terminal devices in a FET geometry. The chapter is summarized in Section 5.7.

5.2 Development of the Edge-Structure Device

We sought to minimize device area by growing the self-assembled organic layer on the edge of a vacuum-deposited metal film (so that the device area would be limited by the thickness of the metal film). To ensure that the device area is kept to the metal edge, the top of the metal layer must be covered by an insulator. A second metal electrode can then be evaporated to contact the organic layer, as envisioned in Figure 5.1(a).

The main challenge to developing the device shown in Figure 5.1(a) is the alignment of the first metal and subsequent insulating layer. The insulating layer must be aligned precisely to the edge of the metal layer: if it extends too far then it will cover the metal (and prevent the growth of the organic layer), and if it does not reach the edge of metal layer this will lead to an undesired increase in device area. We first sought to fabricate this structure by using an e-beam evaporator to deposit both the 1st metal (Au) and insulator (SiO_x) layers through the same shadow mask. However, even though the Au and SiO_x sources were rotated (and the location of the electron beam kept constant) to allow evaporation from the same point, slight differences in the precise location of the evaporation sources led to misalignment of the metal and insulator layers (Fig. 5.1(b)). For example, in the vacuum chamber the substrate is held ~30 cm from the e-beam evaporation source. Even if the shadow mask is in

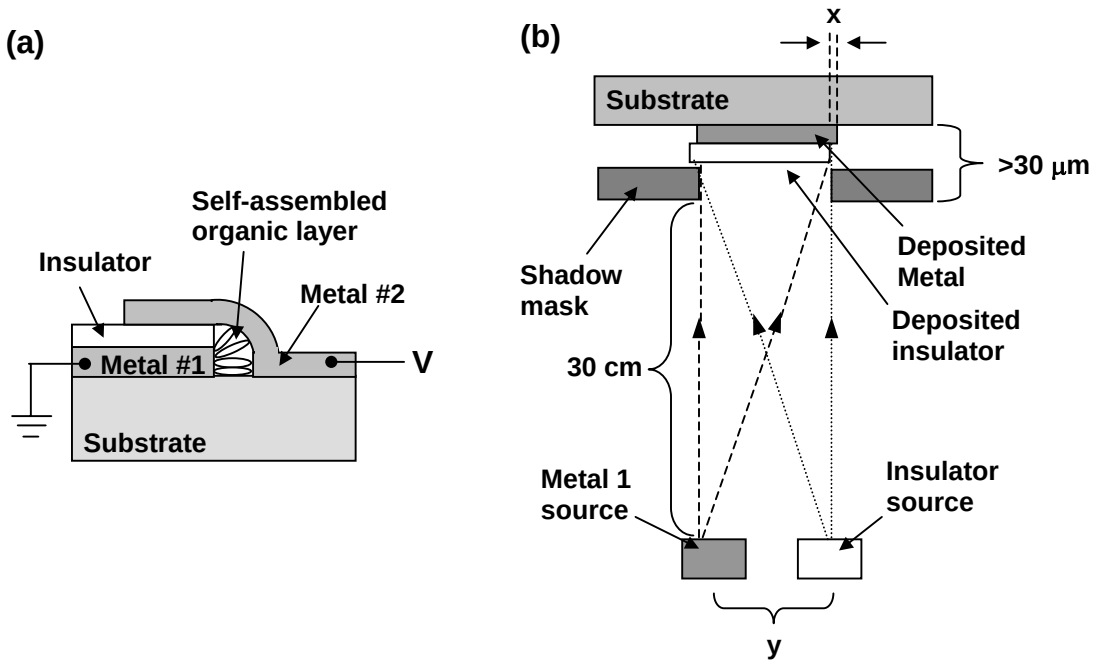


Figure 5.1. (a) Schematic of desired structure where the device area is limited by the thickness of an evaporated metal film. (b) Illustration of the geometry in the e-beam deposition of self-aligned metal and insulator layers. Any misalignment (*y*) in the insulator and metal sources led to misalignment of the deposited layers (*x*). The drawing is not to scale.

contact with the substrate everywhere, its thickness of ~30 μm results in a misalignment *x* of 30 μm * (*y* / 30 cm), where *y* is the difference in locations of the evaporation sources (as shown in Fig. 5.1(b)). It was difficult to align the sources to better than ~0.5 cm, leading to a misalignment of insulating and metal layers of 0.5 μm. Microscope images of deposited layers often indicated misalignments even higher than this, up to ~5 μm, which were probably a result of the shadow mask not maintaining intimate contact with the substrate. After growing self-assembled MUA layers (as described in Chapter 3) and depositing a second gold electrode, we found that devices either had very low current (in cases where the insulating layer was observed to extend past and hence cover the edge of the metal layer) or were mostly shorted (in cases where the insulating layer did not completely cover the top of the 1st metal layer, so that the devices had relatively large areas).

To ensure alignment of the 1st metal layer and insulating layer despite small differences in evaporation geometry, we developed another fabrication approach in

which the layers were self-aligned by deposition onto pre-patterned islands on a silicon substrate. We describe this fabrication in the next section.

5.3 Fabrication of Edge Devices*

Silicon substrates were patterned with photolithography and plasma-etched to form 2 to 3 μm deep trenches. A ~30 nm thermal oxide was then grown (conformally) on the Si wafer (Fig. 5.2(a)). Next, an e-beam evaporator was used to deposit a layer of Au (25 nm) followed by an insulating layer of layer of silicon oxide (SiO_x) (30-50 nm) (Fig. 5.2(b)). Thin adhesion layers of Ti (~5 nm) were evaporated prior to both Au and SiO_x deposition. The evaporation direction was normal to the surface, and all evaporations were done at room temperature. The evaporation geometry was kept similar for every layer by rotating the source materials between evaporations while maintaining the same focal point for the electron beam so that each film was evaporated from the same location. The sequential deposition of the Au layer followed by the insulating SiO_x in similar evaporation geometries ensures that although the top of the Au layer is covered by SiO_x, a small fraction of the Au (on the edge of the mesa adjacent to the etched trench) remains exposed. Layers of MUA were then grown on this exposed Au (as described in Section 3.3) (Fig. 5.2(c)). Finally, a second Au layer (50 nm at ~0.05 nm/s) was deposited onto the sample at an angle (~30° from horizontal) to form a top contact to the organic (Fig. 5.2(d)). The azimuthal angle was chosen to be incident towards the site of the etched step. This layer was patterned by a shadow mask to limit the area of the second gold layer on top of the mesa, so that the first gold layer could be electrically contacted later with a probe (this first gold layer was accessed by using the needle probe to scrape away the thin SiO_x in the probing area) (Fig. 5.2(e)). During the second Au evaporation, the sample stage was cooled to temperatures of 100 K to minimize metal diffusion through the MUA layer, as discussed in Chapter 4. As in the planar devices of Chapter 4, to achieve a variety of device sizes the top electrodes were evaporated at angle (with respect to the mesa edge) so that in addition to different electrode sizes (determined by the shadow-mask pattern) some electrodes randomly overlapped the mesa edge by a large amount while others by only a small amount (Fig. 5.2(f)).

* For additional fabrication details please refer to Appendix B.

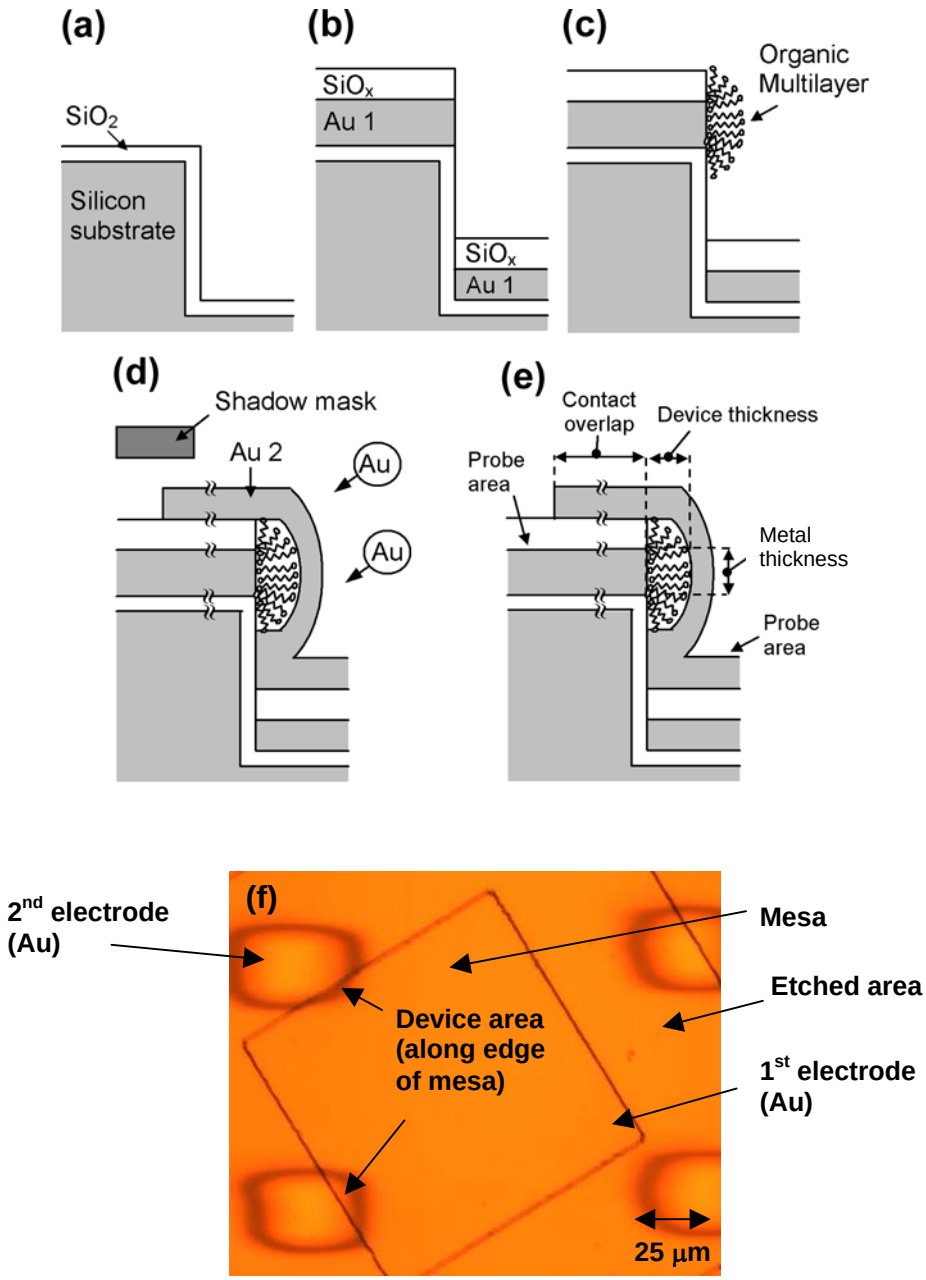


Figure 5.2. Schematic of device fabrication, and top view of devices. (a) A silicon wafer is patterned by photolithography, plasma-etched to define 2-3 μm tall mesas, and thermally oxidized (30 nm). (b) A thin gold layer (25 nm) and SiO_x layer (30 nm) are deposited sequentially by e-beam evaporation, with 5-nm Ti layers used for adhesion (not shown). (c) Organic multilayer is grown on the exposed gold edge. (d) Second gold layer (50 nm) is deposited at an angle of ~ 30° with respect to the horizontal and through a shadow mask to limit the area of the contact. (e) Probe areas are much larger than effective device width, which is defined by the thickness of the first gold layer. (f) Microscope image of devices (top view). The background is the 1st gold electrode, the large square is a mesa (defined by etching), and the small rectangles are the second metal layer. Parts (a) through (e) are from Ref [1].

Similar to the planar PoPI structure (described in Chapter 4, with the structure reproduced here in Fig. 5.3(b)), the insulating SiO_x layer plays a critical role in limiting the device area. As indicated in Fig. 5.3(c), this self-aligned layer allows the use of large electrode contact pads (typically 25 x 50 μm^2) and large electrode overlap areas (25 x 50 μm^2) while maintaining small device areas. The accuracy of the shadow-mask

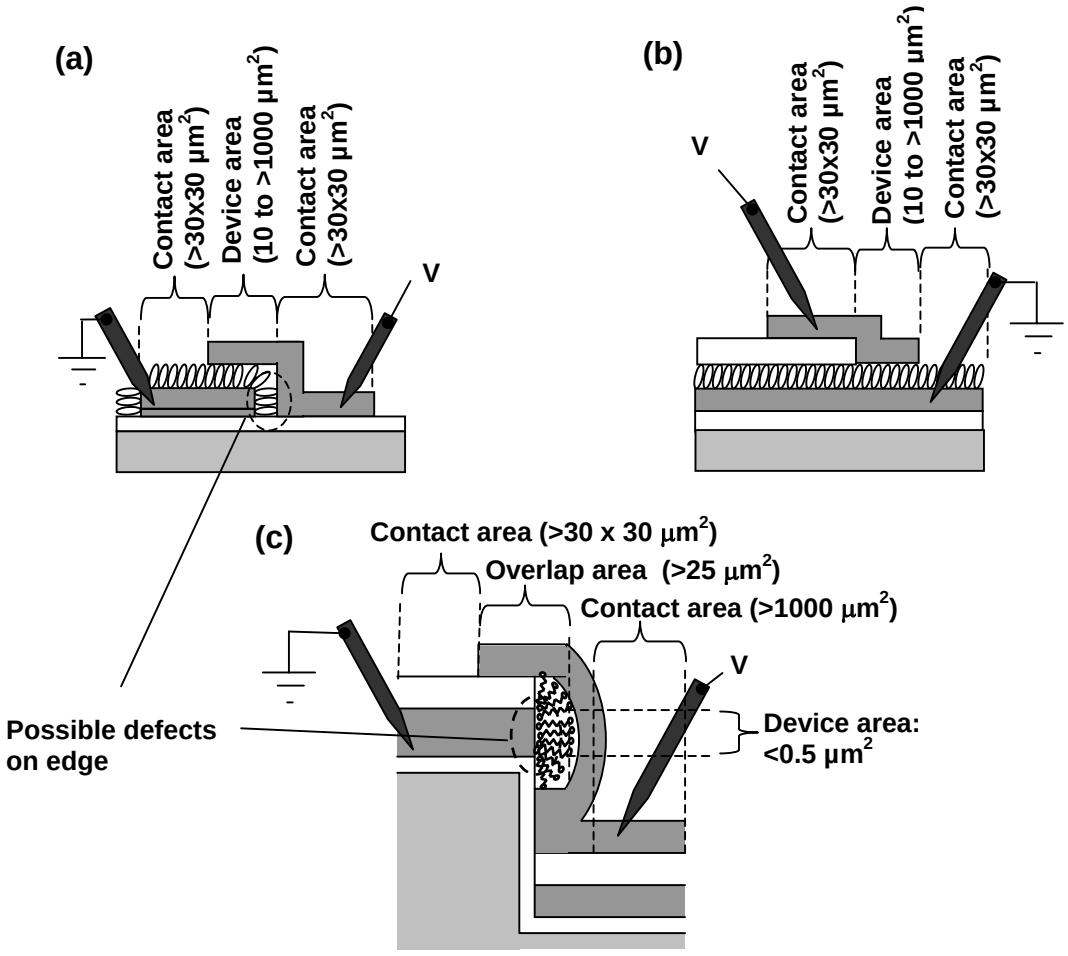


Figure 5.3. Comparison of (a) planar PrPM, (b) planar PoPI, and (c) edge structures. Planar PrPM and PoPI structures are from Figures 4.2 and 4.3. In the PrPM structure, the MUA is grown on a pre-patterned gold layer, then a second, shadow-masked top electrode is deposited. In the PoPI structure, the MUA is grown on a uniform gold layer; the device area is then defined by a patterned SiO_x and patterned top metal electrode, both deposited through shadow masks after MUA growth. In both PrPM and edge structures, the growth of the MUA layer on the edge of the first gold film may lead to increased defects and thus increased currents.

alignment of the second gold layer to the mesa edge was not critical, typically being 5 – 50 μm. In the area where the two metals overlap the deposited oxide insulator prevents any conduction between the electrodes, and the device area is limited to the metal edge. This device area is defined as the product of the thickness of the gold layer and the width of the second shadow-masked Au layers to obtain 25 nm x (5 to 25) microns ≅ 0.1 to 0.5 μm^2. (Note that in the active device, the distance between the metal electrodes is still defined by the thickness of the self-assembled MUA layer). For comparison, planar PrPM and PoPI devices (Chapter 4, reproduced in Fig. 5.3(a) and (b)) had areas of at least 10 μm^2, and more typically 100 to over 1000 μm^2. We also note that the device areas in this edge structure could be readily decreased by an order of magnitude or more (to <0.02 μm^2) by using photolithography to define the width of the device instead of a shadow mask.

The geometry of the edge of the thin Au and SiOx films, and the MUA layer that is grown on this region, may play a critical role in determining device characteristics. To characterize the device structure, cross-section scanning electron microscope (SEM) images were taken after cleaving the sample (Fig. 5.4). In this image, the dark Si substrate is clearly visible, as well as the first Au layer and SiOx layer (although it is

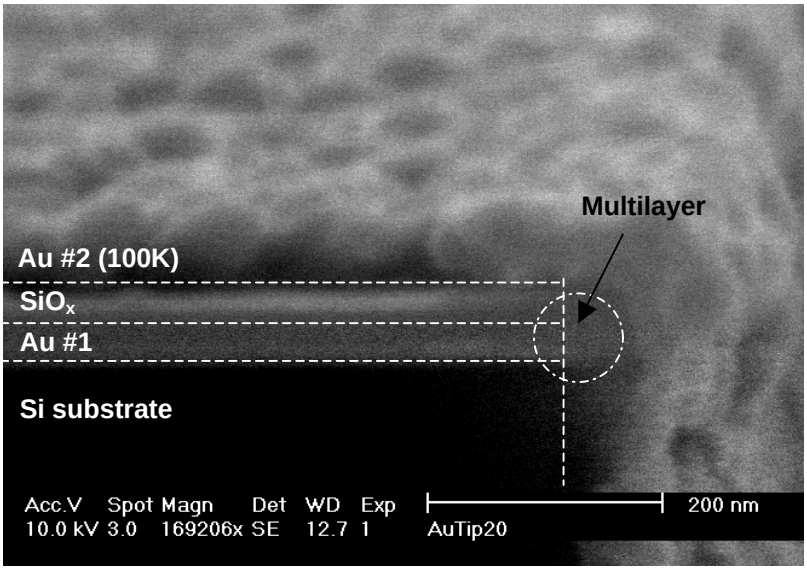


Figure 5.4. Cross-section SEM image of edge device with 12 layer (20 nm) MUA film. The roughness of the second gold layer is due to the low substrate temperature (100 K) during deposition. The location of the MUA layer is circled.

difficult to distinguish between them). The second Au layer appears separated from the gold layer, presumably by the MUA layer. The visible roughness of the second gold layer is likely due to the low temperature (100 K) of the substrate during deposition; AFM measurements of gold deposited directly onto a silicon substrate revealed that gold deposited at low temperature (100 K) is significantly rougher (2 to 5 times larger peak-to-valley variation) than gold deposited at room temperature. Overall, due to the very small dimensions and unique geometry of the structure, the more detailed structure of this region is very difficult to discern.

5.4 Edge Device Characteristics

Electrical measurements were performed using the setup described in Section 4.3. Devices were either insulating, with low current densities (up to a factor of 10^7 smaller than control samples prepared without an organic layer between the gold electrodes) (Fig. 5.5(a)), or shorted, with high current densities and ohmic current-voltage traces. The resistances of the shorted devices were comparable to those of devices fabricated without an organic layer, indicating the presence of conducting pathways between the gold electrodes. The current-voltage characteristics of

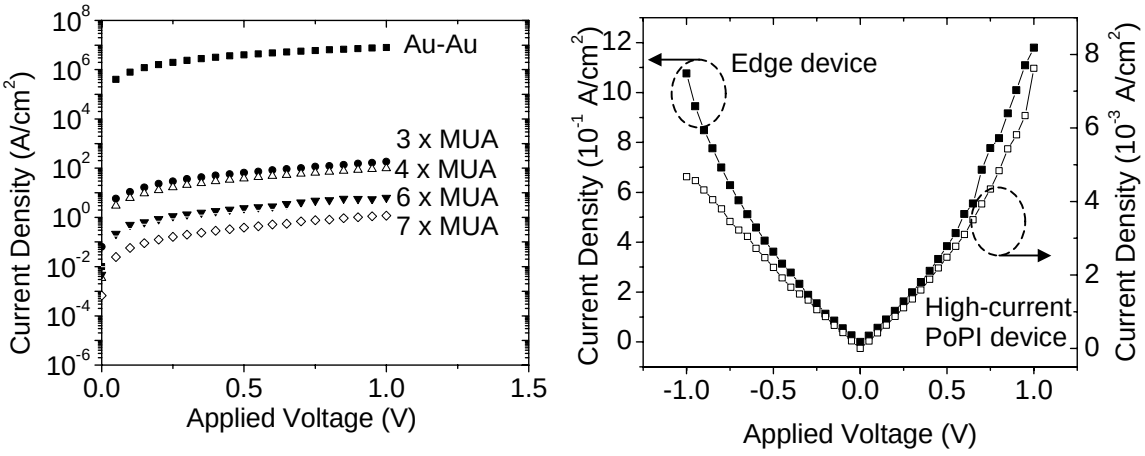


Figure 5.5. (a) Average current densities vs voltage of devices with three to seven MUA layers. Also shown for reference is the current density of devices without any MUA layers (Au-Au contact). Each curve represents the geometric average of 6 to 22 devices (from Ref. [1]). (b) Current densities vs. voltage (applied to the top electrode) for edge device and high-current PoPI device (from Figure 4.5(a)) with 7 MUA layers. Note that the y-axis for each device is scaled differently.

insulating devices were roughly linear, similar to those of the high-current planar devices (Fig. 5.5(b)). As in the planar devices, large variations in the current densities (up to a 10^3) of insulating devices fabricated at the same time were observed. Current-voltage characteristics were stable for voltages below 1 V, and did not depend on scan direction or speed.

As the number of MUA layers was increased from 3 to 7 layers, the yield of insulating devices increased to as high as ~90% for 7 layers of MUA (devices made with 1-2 MUA layers were typically shorted) (Fig. 5.6). These yields were similar to the PoPI devices and much higher than the PrPM (the PrPM and PoPI structures were described in Chapter 4 and are reproduced in Figure 5.3). The geometric mean of the conductance of the unshorted devices decreased exponentially with the number of MUA layers, by a factor of one decade/1.8 layers, which is comparable to the trends observed in planar PrPM and PoPI structures (one decade/1.2 layer and one decade/1.6 layers) (Fig. 5.7). The conductances at each thickness were considerably larger than those in the PoPI devices (by a factor of ~1000), but were comparable to the PrPM structures.

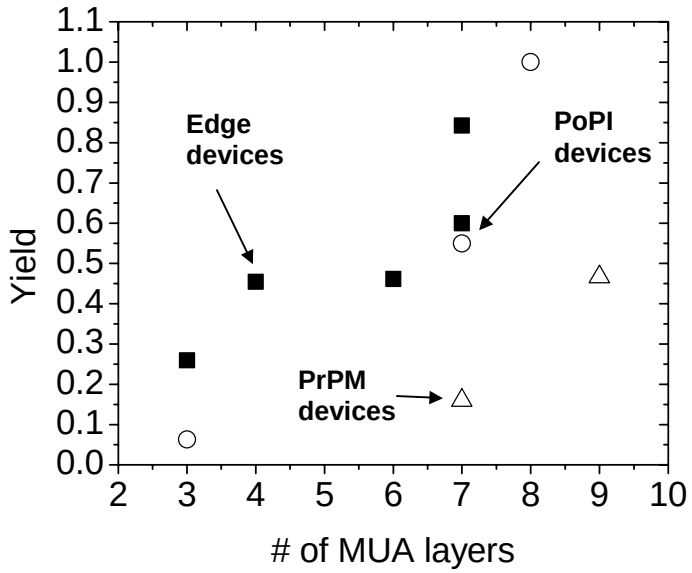


Figure 5.6. Yield (= fraction of unshorted devices) of edge devices (solid squares). Each point corresponds to at least 15 measured devices. Yield of planar PoPI devices (on regular gold) (hollow circles) and planar PrPM devices (hollow triangles) are also shown (from Figure 4.9).

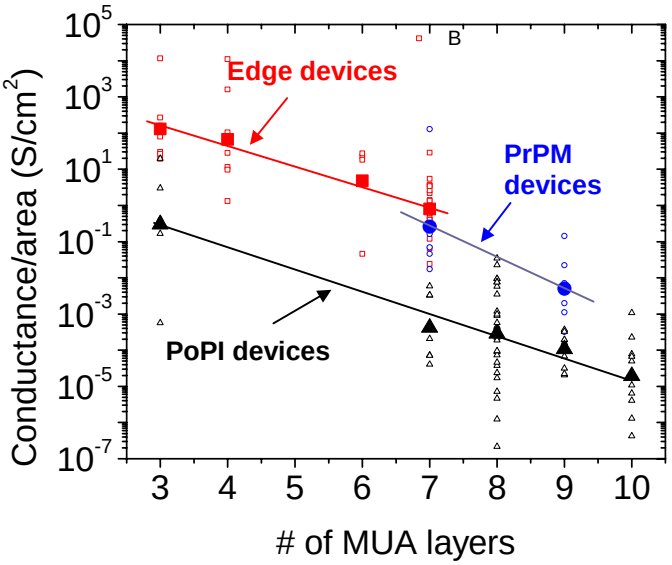


Figure 5.7. Conductance/area vs # of layers for unshorted edge, PrPM, and PoPI structures. The conductance of the edge and PrPM devices was measured at 0.5 V, while the conductance of the PoPI devices was measured at 2 V. Hollow points represent data and solid points their geometric mean. Fitting indicates slopes of one decade per 1.8 layer, 1.2 layer, and 1.6 layer for the edge, PrPM, and PoPI structures, respectively. The PrPM and PoPI data is from Figure 4.8.

5.5 Discussion

We first consider the possibility that the measured electrical characteristics are not due to the MUA film. For example, if the SiOx layer is not aligned to the first Au layer, a thin portion of the SiOx may cover the edge of the Au film, so that the electrical characteristics are due to this layer and not the MUA film. Although it was not possible to achieve the necessary resolution in the SEM to check this directly (Fig. 5.4), the very large current densities (10^7 A/cm^2) in devices fabricated without MUA layers, and the dependence of current density on the number of MUA layers (Fig. 5.7), indicate that this is not occurring. A second possibility is that current transported through the SiO_x covering the top of the gold. However, this is also unlikely, as control measurements on large-area SiO_x films contacted by gold electrodes revealed very low currents, below the noise level of our apparatus (Section 4.3).

The exponential dependence of conductance on the thickness of the film of one decade/1.8 layers was very similar to the relationship observed in planar devices (one decade/1.6 layers for PoPI devices) (Fig. 5.7), further confirming that the charge transport in these device occurs in the MUA layer. The electrical characteristics of edge devices bore close resemblance to planar devices fabricated in the PrPM structure. Conductances of these two structures were similar (Fig. 5.7), and current-voltage traces of all the devices in both structures were roughly linear (Fig. 5.5(b)). As discussed in Section 4.4, roughly linear (instead of exponential) current-voltage characteristics are ascribed to electrical conduction by metal (from the top electrode) that partially penetrates the MUA layer, but in insufficient quantities for shorting.

In the PrPM structure, the increased number of electrical defects (with respect to the PoPI structure) was attributed to poor MUA growth along the edge of the first gold layer (Section 4.4, and indicated in Fig. 5.3(a)). This could be due to the nonplanar geometry of the gold near its edge [6], or the presence of the Ti adhesion layer, to which thiols are not known to bind [5]. Similar arguments are applicable to MUA growth in the edge structure (Fig. 5.3(c)). It is likely that the nonplanar geometry of the exposed gold edge and the nearby Ti layer lead to poorer MUA growth, which in turn increased the likelihood of metal from the top electrode penetrating the MUA film. In both the PrPM and edge structure, the poorer MUA growth on the gold edge is thus the likely cause of the increased current densities in these devices in comparison to the PoPI structure, where the active device area did not include MUA grown on a gold edge (Fig. 5.3(b)).

An additional factor contributing to an increased possibility of metal penetration through the edge structure was the angle at which the top metal layer was deposited. As discussed in Section 4.4, a shallow deposition angle (with respect the MUA layer) is desirable to allow pinhole defects in the film to be physically masked by adjacent molecules (Fig. 4.12). However, to ensure good coverage of the sidewall of the trench so that the device could be contacted, it was necessary to evaporate the second electrode at angle that was almost normal to the MUA film (Fig. 5.2(d)). This relatively direct metal deposition may have led to the penetration of gold through the MUA film.

Despite the poorer MUA growth along the edge of the gold and the direct deposition of the top metal electrodes, which likely led to higher defect currents in edge devices, we observed similar yields of unshorted devices for both edge devices and the planar PoPI devices (Fig. 5.6). Both of these device structures had higher yields than

the planar PrPM structure. This was likely because the much smaller areas of the edge devices mitigated the problem of poorer MUA growth along the gold edge, resulting in yields comparable to the larger-area PoPI devices that did not have MUA growth along a film edge.

Metal penetration into the organic layer could be minimized by several different approaches. The first would be to further decrease the device area, to <0.02 μm^2, by etching the trenches so that they define the device width instead of the second, shadow-masked metal layer. In addition, a different top metal (such as Al) that would react with the organic surface groups would decrease the possibility of metal diffusion into the organic layer. Finally, more careful control of the evaporation angle, so that the top electrode is deposited at a shallower angle with respect to the MUA, may also lead to few electrical defects.

5.6 Further Development of Edge Structure for Three-Terminal Measurements

In addition to its minimal area and compatibility with integrated metal wiring, an attractive feature of this approach is that with further development it may allow fabrication of molecular-scale devices in a FET structure. The geometries of most of the structures that have been used to make two-terminal measurements on monolayers are incompatible with the addition of a third terminal (this is clear from examination of Fig. 4.1, which summarizes a number of reported two-terminal structures) [7]. To further illustrate this incompatibility, we consider the planar PrPM and PoPI structures described in Chapter 4 (Fig. 5.3(a) and (b)). To make a meaningful three-terminal measurement, these structures would require the addition of a third electrode that could modulate the potential in the molecular-layer. Even if it were possible to add a third terminal to the structure, a second challenge must be faced: the fraction of molecules not modulated by the gate must be minimized so that the gate-modulated current can be distinguished from the bulk current. As discussed in Chapter 2, only the few molecular layers nearest to the gate insulator (corresponding to a distance of 1-2 nm into the channel for a 2 nm thick monolayer) will be modulated by the gate potential. Because of the large area of these planar devices, these molecules would represent a tiny fraction (~1 nm/10^4+ nm) of the total layer, so that even if the source-drain current in the molecules near the gate insulator of a

hypothetical FET could be modulated, the ON/OFF ratio of the FET would remain very poor. For comparison, in a typical long-channel MOSFET, the doped channel region extends ~5 μm into the more lightly doped substrate [8]. If the channel has a doping of ~10^{16} /cm^3, this yields a Debye length of ~ 40 nm [9]. The Debye length is a measure of the spatial extent of any potential variation, so that to first order the gate of MOSFET can modulate 40 nm/5 μm ≅ 0.01 of the silicon channel, several orders of magnitude higher than in the molecular layer.

Because the thickness of a deposited metal layer is used to define the device area in the edge structure, this problem can be avoided. The simplest FET geometry that would utilize this approach is the bottom-gate FET shown in Figure 5.8. This structure resembles the two-terminal edge structure that we originally envisioned in Fig. 5.1(a) (and a motivation for the development of this structure was our initial interest in three-terminal devices). In a FET, the self-aligned metal and insulator layers would be deposited directly onto the gate insulator (so that the substrate would act as the gate electrode). The molecular-layer channel could then be grown on the edge of the first metal layer (which would act as the drain), and a second metal layer could be deposited to act as the source. If the first metal layer has a typical thickness of ~25 nm, this results in a much larger fraction of surface current (that can be modulated) to bulk current (that cannot be modulated) of ~1 nm/25 nm.

Unfortunately, fabrication of this three-terminal structure on a planar substrate is limited by the same layer alignment problems described in Section 5.2: if the first metal layer and insulating layer are patterned with a shadow mask, small misalignments between the evaporation sources during the e-beam evaporation lead to misalignment of the metal and insulator layers (Fig. 5.1(b)) and poor device

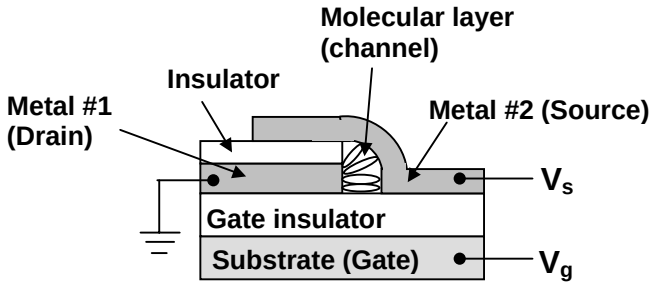


Figure 5.8. (a) Schematic of edge structure in three-terminal configuration (the substrate acts as a gate).

performance. Self-alignment of the first metal and insulator layers by depositing onto pre-patterned islands (as we do to make two-terminal devices) is not a viable option as this results in poor gate-to-channel coupling if the substrate is used as a gate.

A potential solution to this problem would be to use photoresist (followed by lift-off) to pattern the metal and insulator layers instead of a shadow mask. Due to the much thinner nature of photoresist (~1 to 2 μm) and its intimate contact with the substrate, the problem of small misalignments in the evaporation sources as in Fig. 5.1(b) would be drastically reduced. A challenge in utilizing this approach is that the photoresist would then have to be removed prior to the growth of the self-assembled organic film along the gold edge, which could result in contamination of the gold film, making growth of the organic layer more difficult.

5.7 Summary

In this chapter, we have described the fabrication of an edge structure device that allows minimal-area, molecular-scale devices. Our approach utilized an insulating layer of SiO_x that was self-aligned to a metal layer to limit the device area to the edge of the metal layer. Following growth of the self-assembled organic layer on the edge of the metal layer, a second electrode was deposited on top of the metal by thermal evaporation. A key feature of this approach is that in addition to having minimal area (<0.5 μm^2) it is compatible with integrated metal wiring, as the metal electrodes are deposited by vacuum evaporation. The edge structure is also appealing because with further development it may enable three-terminal measurements of the molecular layer.

In Table 5.1, we summarize the characteristics of devices made with the edge structure described in this chapter, as well as the planar PoPI and PrPM devices described in Chapter 4. Overall, the PoPI structure had the lowest current density (i.e., lowest defect density), which was likely due to the fact that in the other structures MUA was grown along the edge of the first gold layer, resulting in poorer quality films. Because of this poorer MUA growth along a metal edge as well as a relatively large device area, the PrPM structures had the lowest yield. The yield in edge structures was much higher despite the lower-quality MUA film, most likely due to the small device area.

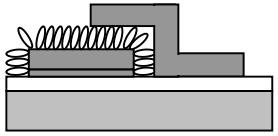
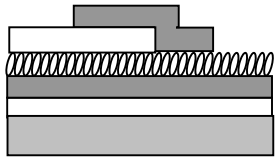
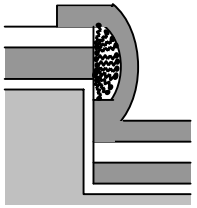
	Planar PrPM	Planar PoPI	Edge
Structure			
J (7 layers of MUA) (A/cm^2)	0.1	8×10^{-4}	0.8
Yield (7 layers of MUA)	0.16	0.55	0.6
Area ($microns^2$)	10 to >1000	10 to >1000	< 0.5
MUA on metal edge	Yes	No	Yes
MUA on large planar area	Yes	Yes	No
Applicable to FETs?	No	No	Yes
Summary	Worst yield and high J due to large device area + defects in MUA grown on edge	No MUA growth on metal edge leads to good yield and lowest J	Good yield because of smallest area, but defects in MUA grown on edge lead to high J

Table 5.1. Summary of device structures and characteristics from Chapters 5 and 6. The (geometric) mean current density J (of the unshorted devices) was measured at 0.5 V for the PrPM and edge structures, and 2 V for the PoPI structure. The yield was defined as the fraction of unshorted devices. We also note whether there was MUA growth on the edge of the first gold electrode or over large planar areas.

References

[1] T. Graves-Abe, Z. N. Bao and J. C. Sturm, "Self-Aligned, Insulating-Layer Structure for Integrated Fabrication of Organic Self-Assembled Multilayer Electronic Devices" *Nano Letters* **4** (12), 2489-2492 (2004).

[2] Y. Xia, J. A. Rogers, K. E. Paul and G. M. Whitesides, "Unconventional Methods for Fabricating and Patterning Nanostructures" *Chemical Reviews* **99**, 1823-1848 (1999).

[3] N. A. Melosh, A. Boukai, F. Diana, B. Gerardot, A. Badolato, P. M. Petroff and J. R. Heath, "Ultrahigh-Density Nanowire Lattices and Circuits" *Science* **300** (5616), 112-115 (2003).

[4] H. L. Stormer, K. W. Baldwin, L. N. Pfeiffer and K. W. West, "GaAs Field-Effect Transistor with an Atomically Precise Ultrashort Gate" *Applied Physics Letters* **59** (9), 1111-1113 (1991).

[5] H. Yang, J. C. Love, F. Arias and G. M. Whitesides, "Electroforming of Copper Structures at Nanometer-Sized Gaps of Self-Assembled Monolayers on Silver" *Chemistry of Materials* **14** (3), 1385-1390 (2002).

[6] A. J. Black, K. E. Paul, J. Aizenberg and G. M. Whitesides, "Patterning Disorder in Monolayer Resists for the Fabrication of Sub-100-Nm Structures in Silver, Gold, Silicon, and Aluminum" *Journal of the American Chemical Society* **121** (36), 8356-8365 (1999).

[7] B. A. Mantooth and P. S. Weiss, "Fabrication, Assembly, and Characterization of Molecular Electronic Components" *Proceedings of the IEEE* **91** (11), 1785-1802 (2003).

[8] J. D. Plummer, M. D. Deal and P. B. Griffin, *Silicon VLSI Technology: Fundamentals, Practice and Modeling*. Prentice Hall Electronics and Vlsi Series, ed. C. Sodini. 2000, Upper Sadle River: Prentice Hall.

[9] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*. 2nd ed. 1986, New York: John Wiley and Sons.

Chapter 6

Integrated Organic Nonvolatile Memory

6.1 Introduction

The increasing demand for electronic memory, driven by sales of personal computers and mobile electronic devices, provides a significant incentive for the continued development of high-performance memory. Although some data-storage technologies, such as digital video disks (DVDs), offer almost limitless, inexpensive data storage, their ability to alter data after it is stored is limited. For most applications, memory in which the stored data can be readily altered (programmed) is desirable. Currently, the programmable-memory market is dominated by four technologies. The first technology is the hard disk drive, which stores data in the local polarization of a paramagnetic disk. This data is accessed and programmed by a miniature antenna (or head) as the disk is rotated. Hard disks are nonvolatile, meaning that a stored state is retained without applied power. Although very inexpensive, the mechanical rotation limits the hard disk's operating speed and ability to withstand physical vibrations and shocks.

Solid-state memories, which have no moving parts, therefore offer a potential advantage over hard disks. The remaining technologies are all silicon-based, solid-state memories because of this increased reliability and the ease of integration with silicon-based logic technologies. In flash memory, which was developed from erasable programmable read only memory (EPROM), the charge on the floating gate of a metal-oxide-semiconductor field-effect transistor (MOSFET) determines the state of a memory cell (Fig 6.1(a)). The current in the channel of the transistor (for a fixed source-drain voltage) depends on the amount of charge on the floating gate, so can be used to read the stored state. Because the floating gate is embedded in a high-quality silicon dioxide insulating layer, it can take many years for the charge to leak out of the floating gate [7]; flash memory is therefore nonvolatile. Dynamic random-access memory (DRAM) also utilizes charge to store data. In DRAM this charge is stored on a silicon capacitor that is accessed by a transistor (Fig 6.1(b)). The memory state is read by measuring the charge stored on the capacitor. Unlike flash memory, this stored charge can leak out of

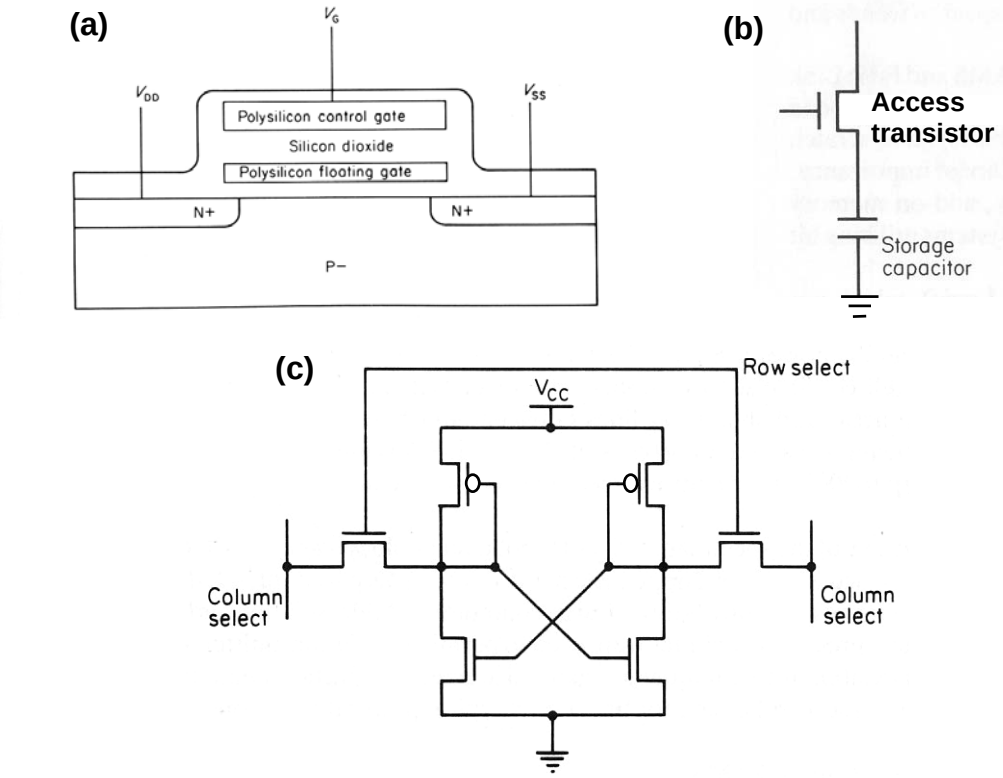


Figure 6.1. Schematics of solid-state memory technologies (from Ref [1]). (a) Basic structure of flash memory, in which charge stored on a floating gate determines the current through the channel of a FET. Charge is stored on the gate by the injection of hot carriers and removed by Fowler-Nordheim tunneling. (b) A DRAM cell, where charge is stored on a capacitor (accessed through a FET). (c) A six-transistor SRAM circuit, with cross-coupled CMOS inverters and select transistors.

the capacitor through the channel of the access transistor (which has a finite impedance even when off) very quickly (~100 ms) [8]. Since this charge must constantly be refreshed to retain data, DRAM is a volatile memory technology. Finally, in static random access memory (SRAM), each memory cell consists of two cross-coupled complementary metal-oxide-semiconductor (CMOS) inverters that form a flip-flop (Fig 6.1(c)). The stored memory state is determined by the voltage on the inverters. Although SRAM does not need to be refreshed, it is volatile because stored data is lost if power is removed.

Despite the success of these technologies, there is considerable interest in developing new forms of memory to improve on some of their characteristics. We consider several of these characteristics in Section 6.2, and discuss why there are

promising opportunities for the introduction of new memory technologies. In Section 6.3, we focus on the performance characteristics and limitations of flash memory, and then review the different organic memory technologies that have been demonstrated in Section 6.4. In Section 6.5, we discuss integration of devices into active-matrix and passive matrix architectures, and describe the requirements on device performance for this integration in Section 6.6. The chapter is summarized in Section 6.7.

6.2 Opportunities for New Memory Technologies

From a performance perspective, four attributes of memory technologies are of particular interest: cost per bit, programming speed, access speed, and whether the memory is nonvolatile or volatile. The program and access times for nonvolatile (hard disk and flash) and volatile (DRAM and SRAM) memory technologies are plotted vs cost per MB (for the year 2004) in Figure 6.2. The hard disk is the cheapest of the technologies (10^{-3} $/MB), but its access and program times are limited to several ms due to mechanical rotation of the disk. Flash memory offers a considerable decrease in access times, to 100 ns, but program times remain long (~ 1 ms) and cost/bit is increased by a factor of 500 to 0.5 $/MB . DRAM is even faster, with program and access times in the 10-ns range, and it is cheaper than flash memory (0.15 $/MB). However, this advantage in speed and cost are offset by DRAM's volatility. Finally, SRAM is the fastest technology (1 ns program/access times), but is also volatile and the most expensive (2.7 $/MB). The disparity of performance and cost characteristics between the memory technologies allows each to fill an application niche (or niches) without significant competition from the other technologies. For example, SRAM is used in applications that require extremely high data turnover and therefore short access/program times (such as the in cache memory of a computer processor), while a computer hard disk is used as a large, long-term repository for files that are used infrequently.

In mobile electronic devices, which represent a fast-growing segment of the memory market, nonvolatile memory is especially appealing because it allows long-term data storage without drawing battery power. Other advantages include the ability to withstand unexpected power outages without data loss, and the potential to bypass the lengthy boot sequences upon startup that are required by volatile memories. Eliminating lengthy boot sequences enables further decreases in power usage by

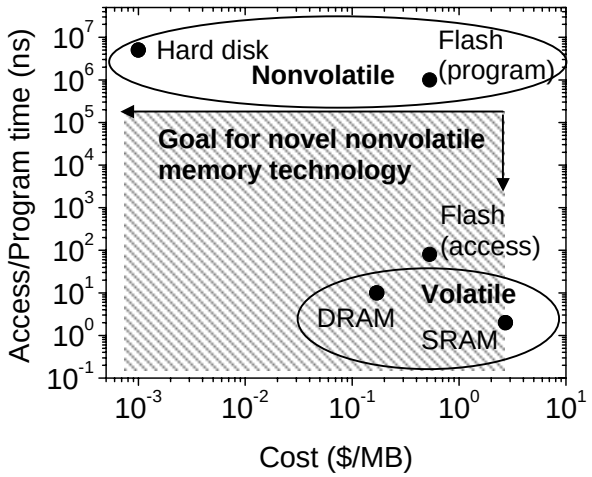


Figure 6.2. Access and program times vs cost/bit for different memory technologies in 2004 [2, 4-6]. For hard disk, DRAM, and SRAM technologies, access and program times are similar and are represented by single points on the plot. For flash memory, program times and access times differ by 10^4 and are represented by two different points. Also indicated on the plot is whether the technology is volatile or nonvolatile, and the program-time/price range open to a new nonvolatile memory technology (shaded region). For the hard disk technology, the access/program time shown in the figure is primarily determined by the time required for the head to seek the correct sector of the magnetic disk.

making frequent transitions to and from power-saving standby modes possible without disrupting the user [9, 10]. Examination of Figure 6.2 reveals that, due to the slow program times and/or high cost of hard disks and flash memory, a very large program-time/price space is available to new nonvolatile memory technologies. This open program-time/price space can be further divided into several regions of interest, based on the hypothetical specifications of a novel nonvolatile memory (Fig. 6.3). Region I, which combines the lowest price at the highest access and program speeds, represents the ultimate goal for a memory technology. A technology with these attributes could potentially be used for any memory application, replacing all other technologies and acting as a "universal" memory [9]. In region II, the hypothetical memory could compete with DRAM, SRAM, and flash memory, potentially replacing these technologies. However, the relatively high-cost of the technology would prevent it from competing with hard disks. Finally, in region III, the new technology's slow speed (and relatively high-cost) could limit its impact to only those applications currently dominated by flash memory.

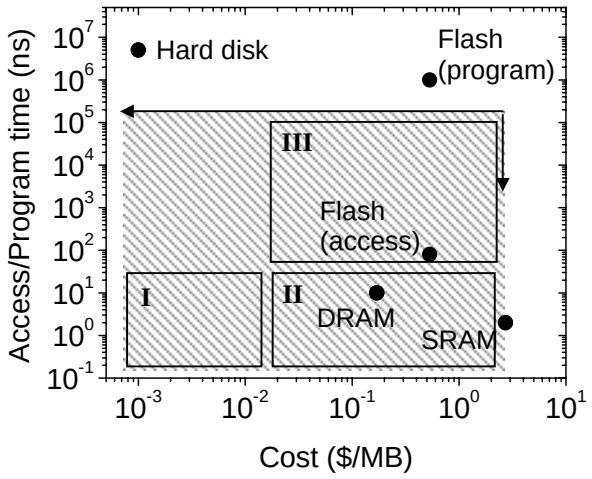


Figure 6.3. Program-time and price range open to new nonvolatile memory technologies, subdivided into regions I, II, and III as discussed in text.

Although a technology in region III might only complete with flash memory, the region still attractive because it represents a potential market that is very large (total sales of flash memory in 2005 are forecast to be $20 billion), diverse, and growing [11]. In addition to the size of the potential market, this region is attractive because other technological requirements (in addition to program/access times) are less stringent. For example, DRAM and SRAM are rated for over 10^{15} programming cycles and operate at voltages of ~1 V [2]; any new memory targeting DRAM and SRAM applications would almost certainly need comparable characteristics. In contrast, the main competitor in region III, flash memory, has a number of drawbacks that will be discussed further in Section 6.3. Hence, even though there is much interest in developing an ambitious, universal memory that could be used in all applications, the best opportunity for novel memory technologies is in region III, where a new memory might overcome many of the current limitations of flash memory.

6.3 Performance Limitations of Flash Memory

Flash memory comes in two architectures: NOR and NAND. NOR flash memory generally has lower densities, longer programming times, and faster read times than NAND [12-14]. However, in recent years new NAND architectures and controllers have reduced the differences between the two. Because of the wide variety of flash

memories available and the rapidly progressing state of the art, it is unreasonable to describe performance characteristics with precision of more than an order of magnitude. Since NOR and NAND are comparable (to within an order of magnitude), in this section we focus primarily on NOR flash.

Although cost/bit, program times, and access times are key characteristics of memory technologies, a much longer list of characteristics are relevant in most applications. Some of these characteristics are shown in Table 6.1, along with the current characteristics of NOR flash memory and the desired characteristics for a nonvolatile memory. In most categories the performance of flash memory is somewhat limited. Memory state storage times of >10 years are one of the few areas in which flash memory is more than adequate. CMOS compatibility is also reasonable. As discussed in more detail in Section 6.6.4, CMOS compatibility is desirable for integration with high performance access and sense circuits. CMOS compatibility involves both manufacturing and logic compatibility. Flash memory is readily integrated into CMOS manufacturing processes; its only drawback is that it requires relatively large voltages for programming, which limits its compatibility with CMOS logic (which operates near 1 V) [2]. Cell size is also larger than desired. The primary quantity of interest here is the cell size in units of F^2, where F is the minimum lithography feature size. As discussed further in Section 6.5, a minimal cell size translates into minimal cost and corresponds to 4 F^2 ; NOR flash is typically at least 2x larger than this. Flash access times (80 ns) could also be improved (DRAM has access times <15 ns).

Flash-performance is most limited in the last three categories of Table 6.1. As discussed earlier, one of the most critical drawbacks of flash memory is its 1 ms program time, much longer than desired. Durability is also relatively low, as flash memories are typically rated for 10^6 programming cycles (in comparison to $>10^{15}$ for DRAM and SRAM). Finally, flash memories require large programming voltages (>10 V), due to the voltage needed to remove charge stored on the floating gate (by tunneling through the gate insulator). It is hard to reduce this voltage, as this would require reducing the insulator thickness (which would decrease the ability of the gate insulator to store charge on the gate without leakage). It is probable that this tradeoff between operating voltage and gate insulator thickness will limit the opportunities for continued scaling of flash memory [15]. These large programming voltages also lead to increased power consumption and limit compatibility with CMOS logic circuits.

Characteristic	Flash NOR	Desired
Storage time (years)	> 10 years	> 10 years
Compatibility w/CMOS?	Okay	Very good
Cell size (F^2)	8 -12.5	4
Cell size (m^2)	0.1	0.03
Access time	80 ns	<15 ns
Program time	1 ms	<15 ns
Program cycles	10^6	$>10^{15}$
Program Voltage (V)	10	<2

Table 6.1. Characteristics of NOR flash memory in 2004, compared with desired characteristics. The units of F^2 in the cell size are based on the minimum lithography feature size F. 4 F^2 represents the minimal possible cell size as discussed in Section 6.5.2, (0.03 μm^2 corresponds to 4 F^2 for F = 90 nm). Other desired characteristics represent the state of the art in DRAM [2, 3].

These limitations of flash memory, and in particular the long program times, limited durability, and large programming voltages, have led to a considerable amount of research activity in search of new nonvolatile memory technologies. A (nonexhaustive) list of the approaches that have been proposed and/or are under development includes phase-change memory, nano-floating-gate memory, single-electron memories, ferroelectric random access memories and field-effect transistors, magnetoresistance random access memories, programmable resistance cells, and molecule-based memories [2, 16, 17]. Although this list includes both inorganic and organic technologies, in this thesis we will limit our discussion to those that are based on organic materials.

6.4 Organic Nonvolatile Memories

In this section we provide an overview of recent experimental results on organic memory devices. Although several experimental results on organic memory devices were reported between 1960 and 2000 (e.g. [18-21]), they received relatively little attention. However, the last 5 years have seen a significant increase in the number of papers published on organic memories, with over 21 articles (excluding conference presentations) on organic memories published in 2004 alone. This interest is motivated

by the wide variety of functionality available in organic materials, which may enable high-performance devices, coupled with the traditional organic strength of potentially low fabrication costs.

The reported results encompass a variety of memory mechanisms and include two- and three-terminal device structures. However, the bulk are two-terminal, programmable-resistance devices with the organic layer sandwiched between metal electrodes. This structure is appealing because its simplicity may minimize fabrication costs. The organic layer can be deposited by vacuum evaporation (small molecules), spin coating (polymers), or self-assembly (molecular films), so that device areas and organic layer thicknesses vary widely, from ~50 x 50 nm^2 to ~ 5 mm^2, and 2 nm to greater than 500 nm, respectively [17, 22, 23]. A wide variety of molecules have also been employed, as well as organic-inorganic hybrid layers, and authors attribute their results to a number of different mechanisms.

Despite these differences, the operation of most organic devices is usually quite similar, with relatively large voltages (> 1 V) used to program the devices into different resistance states, and lower voltages (<1 V) used to probe the states (i.e. device resistance) nondestructively. Generally, the low-resistance state is referred to as ON (and programming into this state as a “write” operation); the high-resistance state is referred to as OFF (and programming into it an “erase” operation), and probing the stored state (device resistance) is known as a “read” operation. For most devices, writing is accomplished with a forward bias; a reverse bias is then used to erase the device. However, in some devices only a single voltage polarity is required to program the device ON and OFF. For example, in electroformed organic devices voltages of ~3 V write the device, while voltages of ~6 V erase the device [24]. In these devices, after erasing with a large voltage it is generally necessary to return the applied bias to 0 V quickly (10^{-3} to 10^{-6} s) to avoid inadvertently writing the device ON.

We now consider the characteristics of the organic memory devices that have recently been demonstrated. Because of the large number of publications in recent years, we do not seek to catalog all results and instead report only a representative sample. Selected results and their characteristics appear in Table 6.2. For each technology, we report the type of organic layer (self-assembled molecular layer, small molecule, or organic), the memory mechanism, and a number of performance characteristics, including program time, the voltage used to program the device, the

Technology	Type of organic	Mechanism	Program time (s)	Program voltage (V)	Retention time	ON/OFF ratio	Program polarity	ON resistance (Ω cm^2)	Refer-ence
Organic Bistable Device	small molecule	polarizing embedded metal clusters	$<10^{-8}$	2	>weeks	10^5	Bipolar	10^3	[25]
Organic electroformed	small molecule	charge trapping on embedded metal	?	2.5-6	?	10^3	Unipolar	10^2	[24]
Polystyrene w/gold nanoparticles	polymer	charge transfer to gold particles	10^{-8}	< 3	years (?)	10^4	Bipolar	10^3	[26]
Polystyrene w/C60	polymer	charge transfer to C60	?	4-6	> months	10^4	Bipolar	10^2	[27]
polythiophene	polymer	charge storage	?	1-2	>hours	10^5	Bipolar	10^4	[28]
Rose Bengal film	self-assembled	molecular reduction + conformation change (?)	?	4	>hours	10^3	Bipolar	10^4	[29]
Molecular SAM	self-assembled	redox leading to localization of orbitals (?)	$<10^{-7}$	0.25-0.5	>15 min	?	Bipolar	10^{-1}	[30]
[2]rotaxanes	self-assembled	oxidation leading to conformation change	?	2-7	> 4 months	4 to 10^2	Bipolar	10^{-1} to 10^{-4}	[31]
1-D molecular chain	self-assembled	Field displacement of ions	10^{-6}	3-10	>months	10^2	Bipolar	10^{-1}	[32]
Cu-organic device	small molecule	movement of Cu+ ions	10^{-3}	2	>months	10^7	Unipolar	1	[33]
CuTCNQ	small molecule	charge transfer (?)	?	10	?	10^4	Bipolar	10^3	[34]
WORM (write once)	polymer	PEDOT redox	10^{-6}	4-10	years	10^3	N/A	10^{-2}	[35]

Table 6.2. Examples of recently demonstrated two-terminal, programmable-resistance organic nonvolatile memory devices. The ON/OFF ratio refers to the ratio between the highest-resistance and lowest-resistance state. The program polarity refers to whether or not the device can be programmed with voltages of a single polarity (unipolar), or if it requires both negative and positive biases for programming (bipolar). We estimate the resistance of the ON state at 1 V (and obtain it by taking the inverse of the current density, so that we report the product of the resistance and device area).

retention time of stored states, the ON/OFF ratio, the polarity of the programming operation (unipolar or bipolar voltages), and the resistance of the ON state.

The enormous variety of organic compounds that can be purchased or synthesized is exploited by workers in the field, who use a number of different organic layers. Still, several approaches share some similarity. One of the most common approaches is to mix dilute amounts of a small bandgap (or HOMO-LUMO gap) phase (often metal nanoparticles) into a large bandgap (insulating) matrix. The organic bistable devices, organic electroformed devices, and the polystyrene with gold nanoparticles or $C_{60}H_{60}$ all share this structure. Most workers attribute the memory mechanism in these devices to charge transferred to and stored on the small bandgap phase (so that structural changes in the film do not play an important role in the change in resistance), however the details of this mechanism generally differ from device to device (and in some cases alternative explanations exist). Most of the devices with self-assembled layers switch between bistable states that appear to correspond to different charge or conformation (i.e. structural) states of the molecules in the layer. Another previously reported approach involves ions embedded in the organic phase; this approach is used in the 1-D molecular chain and the Cu-organic devices. Here, the memory mechanism is attributed to the field-induced movement of ions, although again there is some ambiguity. Indeed, for most devices completely satisfying models for the observed characteristics have not yet been developed, and the extent to which different technologies share a common mechanism remains unclear. We also note that the final approach in Table 6.2, the Write-Once Read Many times (WORM) device, is not reprogrammable so would not be a potential replacement for flash memory. We include it in this table because it and other write-once devices have nevertheless attracted attention for use in archiving applications.

Most devices have program times that (when reported) are below flash memory's program time of 1 ms; in some instances the program times of ~10 ns are similar to even those of SRAM. However, it is important to note that these program times are for individual devices; in an actual memory array program times may increase considerably beyond this lowest estimate (we will study a related effect in Section 6.6.1 when we consider how the device resistance affects its access time when operated in an array). Low program voltages are desirable (for low power operation and compatibility with CMOS); here the molecular SAM devices do very well (0.25 – 0.5 V), and almost all of the devices use lower voltages than flash memory (10

V). Given the recent nature of most investigations, no devices have proven data retention times longer than flash memory's 10+ year retention. The extrapolated retention times of many devices often suggest values near this goal, although some devices (mostly those consisting of self-assembled monolayers) have poor retention times (as short as 15 minutes in the molecular SAM). As discussed further in Section 6.6.2, large ON/OFF ratios are desirable for application in large memory arrays. Reported values range from 10^2 to 10^7. We will discuss the importance of the polarity of the program voltage and the resistance of the ON state in Sections 6.6.1 and 6.6.3, when their relevance will become more apparent. Finally, durability of the devices and their rectification ratios are important issues but were not addressed by most authors so were not included in the table. The one device for which durability was reported, the organic bistable device, showed very encouraging results of 10^6 write/erase cycles [25].

Based on the performances of individual devices, many of these initial results appear promising for nonvolatile memory application, as program times and voltages generally compare favorably to flash memory. Clearly, retention times may be a concern in some of these approaches, and durability issues must also be addressed. However, for significant commercial application these devices must be integrated into large arrays (with support circuits), which places many more demands on the devices. In the next sections we consider these integration issues more carefully, and show that the requirements that they impose may severely limit the utility of most of the previously reported organic nonvolatile memory devices.

6.5 Integration of Organic Memory into Large-Scale Arrays with Support Circuits

In this section, we describe two alternative memory architectures, active-matrix and passive-matrix, that can be used to integrate devices into memory arrays. We describe the advantages and disadvantages of each.

6.5.1 Active-Matrix Arrays

For widespread commercial application, organic memory elements must be fabricated in large arrays to create memories capable of storing data at greater than Gb densities. Moreover, to meet the performance demands on modern memory chips

(i.e. that they be high speed and density), the array of memory cells must be integrated with high-speed circuits to program and read the individual cells. It is almost certain that these support circuits will be based on CMOS transistors for the foreseeable future, as no other transistor technology approaches CMOS in terms of performance, cost, and availability.

In addition to these CMOS support circuits, adoption of the commonly used active-matrix (AM) architecture would also likely require integration of organic memory elements with CMOS transistors directly within each memory cell. In an AM architecture, access to an individual programmable-resistance memory device would be controlled by a transistor (Fig. 6.4), similar to the transistor used to control access to the capacitor in a DRAM cell (Fig. 6.1(b)). This access transistor must be capable of high-speed operation to minimize the time needed to program and read the device, and have large ON/OFF ratios to minimize parasitic currents from inactive memory cells. As in the support circuits, a FET based on CMOS technology is thus the best option for this access transistor.

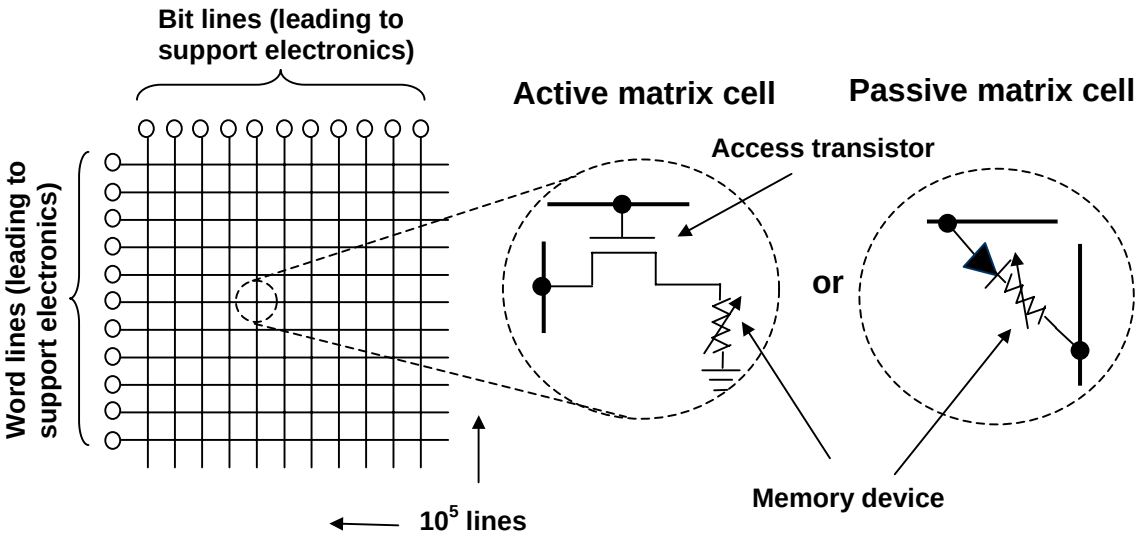


Figure 6.4. Memory cells in AM and PM architectures. In both architectures, the memory array requires support electronics (likely CMOS-based). In the AM array, access transistors (likely CMOS-based) must also be integrated directly into the memory cells. In the PM architecture, the memory device must be rectifying (or in series with a rectifier, such as a silicon diode). To make a 10 Gb memory, a square array would require 10^5 word and bit lines.

This implies that even if the memory cells can be fabricated with minimal expense, the cost of the memory chip will be largely due to the cost of the integrated access FETs that must be fabricated on a single-crystal Si wafer. This potentially removes much of the cost advantage enjoyed by organic materials in large-area electronics applications. For example, in electronic displays, where organic light-emitting diodes (OLEDs) have already achieved commercial success [36], the less stringent performance requirements on the backplane transistors used to drive the OLEDs allow the use of alternative, lower cost thin-film technologies such as amorphous and polycrystalline Si.

To first order, the cost to fabricate a circuit on single-crystal Si is proportional to its area. This trend is illustrated in Figure 6.5, which shows the cost/MB of the dominant solid-state technologies (SRAM, DRAM, and flash) vs their cell size (in units of F^2, where F is the minimum lithography feature size). SRAM requires 6 transistors in each cell, leading to relatively large areas (90 to 150 F^2) and therefore high costs ($2.72/MB). DRAM, with a much simpler one-transistor/one-capacitor structure, utilizes a much smaller area (6 to 12 F^2) and has the lowest cost ($0.17/MB). Because a similar AM architecture is used in DRAM (Fig. 6.1(b)), to first order (neglecting development costs) an organic programmable-resistance memory would remain similar

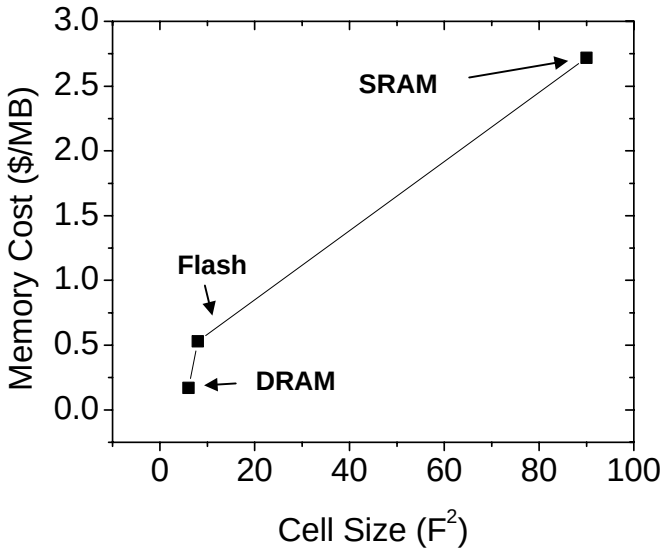


Figure 6.5. Relationship between 2004 cost of silicon solid-state memory and cell size [2, 4-6].

to this technology in cost, which represents a small (~5x) cost advantage over flash memory (Fig. 6.2). An organic AM memory may actually achieve even lower costs than DRAM, as the size of the access transistor will remain similar to the one in a DRAM cell, while the organic device could have a smaller area and be simpler to fabricate than the relatively large-area (or complicated-structure) DRAM charge-storage capacitor [37].

6.5.2 Passive-Matrix Arrays

To achieve even further cost reduction, it is desirable to remove the CMOS access transistor from the memory cell. This is done with a passive-matrix (PM) architecture (Fig. 6.4). The main appeal of the PM architecture is that without the need for CMOS transistors within each cell, the memory array could be fabricated on an inexpensive (non-crystalline) substrate, then later bonded or integrated with CMOS support circuits outside of the array itself. Indeed, a key motivation for the investigation of two-terminal organic memories has been their potential for fabrication in a passive-matrix "crosspoint" array [10, 17]. In this array, the unpatterned active organic layer is sandwiched between two perpendicular sets of conductive lines (Fig. 6.6). In addition to the potential for fabrication on low-cost substrates, this approach also requires relatively few patterning steps to allow further cost reduction.

An additional feature of the crosspoint array is that it results in a minimal-area cell (even though reduction of cell size is not as critical if the array is fabricated on a

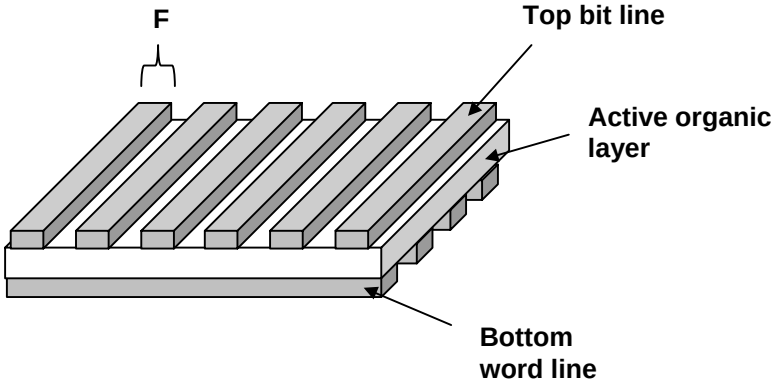


Figure 6.6. Crosspoint memory architecture. This array could be fabricated on an arbitrary substrate. Additionally, the cell area is minimized in this structure and is equal to 4 F^2.

noncrystalline substrate). The perpendicular electrode (word and bit) lines, with a width of F (and separated by F) define the cell size of only 4 F^2 (compared to 8 to 12.5 F^2 in flash memory). Because of this minimal-area cell, this array would impose the smallest possible cost penalty if it were necessary to fabricate the array directly on a silicon substrate (although this would still likely be more expensive than fabrication on a separate, lower-cost substrate).

Although clearly appealing from a cost perspective, PM arrays have several disadvantage in comparison to AM arrays. For example, in display applications (where one can also choose between AM and PM architectures), PM arrays are relative rare for high-resolution displays with large numbers of pixels. This is because in a PM display with N rows, each row is only powered for only 1/N of the time, so that during this time the individual pixels must be driven at very high currents to achieve a reasonable brightness (when averaged over all time). This results in high drive voltages, leading to resistive voltage losses, decreased device lifetimes and lower power efficiencies [38, 39]. As we will discuss in the following sections, for large memory arrays the PM architecture faces comparable problems. For example, as we discuss in Section 6.6.3, in PM displays it is necessary for the device to have a large rectification ratio. If the device is not intrinsically rectifying, it will be necessary to include a diode in series with the device, as shown in Fig. 6.4.

It is important to note that even with the low-cost PM array, the cost of the support circuits will significantly increase the cost of an organic memory beyond what naïve projections (based only on fabricating the organic array itself) would indicate. Even in silicon memories, the support electronics represent a substantial portion of the total cost (for example, in DRAM the support circuits represent ~40% of the total cost [10]). One way to minimize the cost of the support circuits is to fabricate memories that consist of a few, relatively large arrays of devices (instead of multiple smaller arrays). In large arrays, some of the support circuits are shared by a larger number of memory cells, reducing the cost penalty imposed by these circuits [10]. Assuming a square array, if we wish to fabricate a 10 Gb device using only 1 array, this implies 10^5 word and bit lines, and one set of (complicated) support circuits. If the array size is reduced to 10^4 word and bit lines, 100 arrays (and sets of support circuits) would be required for the same memory size.

For the best chance of widespread commercial application, organic memories should therefore be fabricated in large crosspoint arrays with integrated CMOS

electronics. We now consider the requirements on device performance that are imposed by this goal.

6.6 Requirements for Integration of Devices

In this section we consider several of the characteristics organic memory devices must have for integration into large-scale memory arrays. Our focus is on integration into PM arrays, as these are most desirable in terms of cost. We will also discuss integration into AM arrays; although more costly, we will see that AM arrays place less stringent demands on device performance so represent a viable alternative to PM arrays.

6.6.1 ON-Resistance

We first examine the device characteristics that are necessary to achieve fast read times in large memory arrays in PM and AM architectures. To do this we develop a circuit model to determine how the time required to perform a read operation depends on different parameters. We will use this model to show that the resistance of the device in the ON state plays a critical role in determining how long it takes to read the device in a large array. To first order, the read delay corresponds to the time it takes to charge (or discharge) the capacitance of the interconnect line through the device resistance (however, in our model we also include the resistance of the interconnect line for completeness). To estimate these delays, circuit simulations of devices in PM and AM architectures were performed. All simulations were performed using Circuitmaker software (which uses Berkeley's SPICE3f5/XSpice-based simulator) or with PSPICE software. The simulations in PSPICE were performed with the help of Tse-Jen Jerome Ku (Princeton University, Class of 2005).

The model for the memory cell and interconnect lines during a read operation is shown in Figure 6.7. We first consider the PM array (Fig. 6.7(a)). Here, the memory device is modeled as a resistor in series with a diode. For a read operation, we apply V_{supply} = 2 V to the bit line at time t = 0. As the wordline is charged through the device resistance, this leads to an increase in the voltage ($V_{S.A.}$) across the sense amplifier, which we model as a resistor ($R_{S.A.}$). Because $R_{S.A.}$ is chosen so that $R_{OFF}>>R_{S.A.}>>R_{ON}$, if the device is OFF $V_{S.A.}$ will remain near 0 V, while if it is ON $V_{S.A.}$ will begin to rise, eventually approaching V_{supply} (if we ignore the diode voltage and

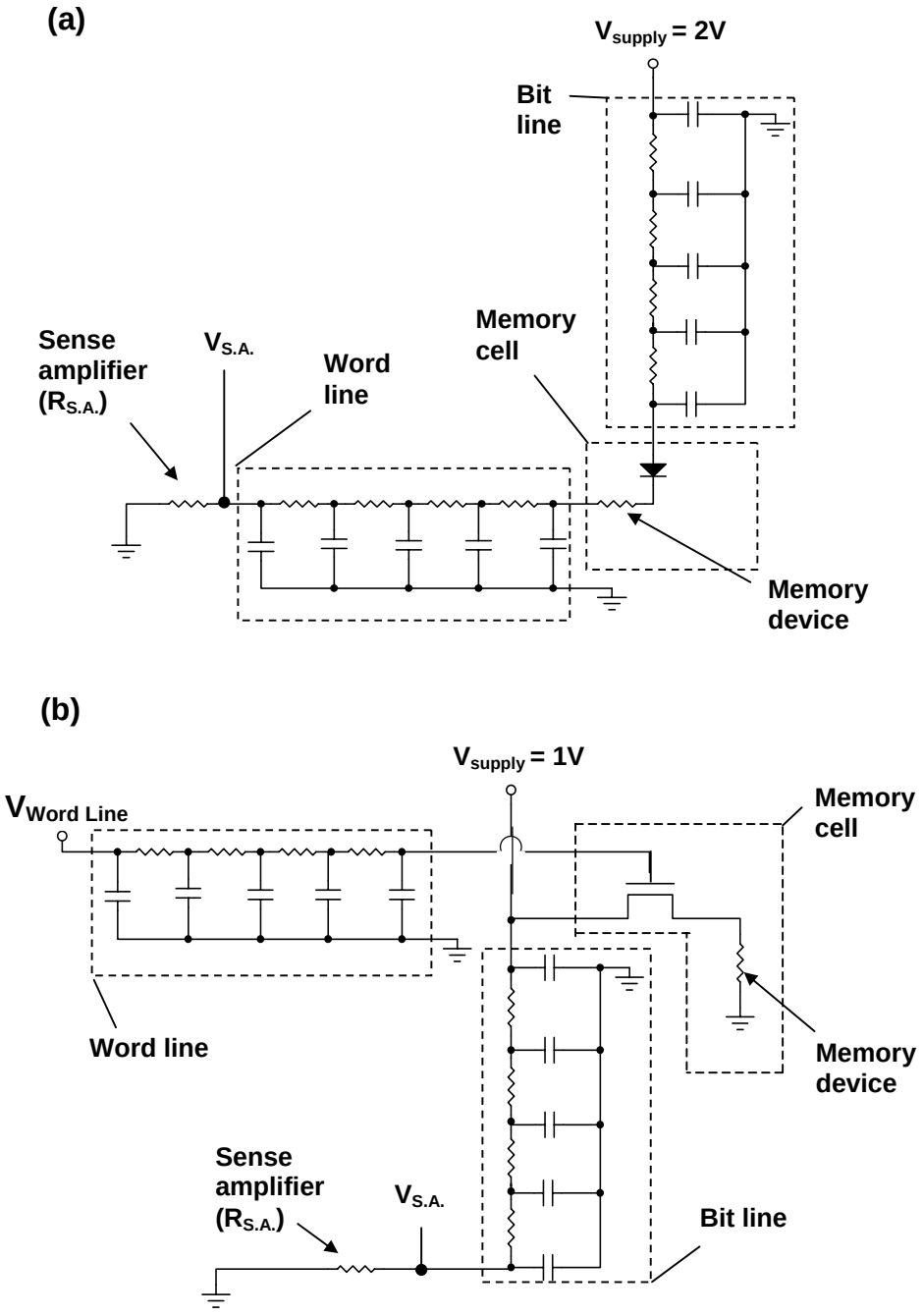


Figure 6.7. Model for memory cell, sense amplifier, and interconnect lines used in PSPICE simulations of read delays due to RC effects (R of memory device, C from interconnect capacitance) in (a) a passive-matrix array and (b) an active matrix array.

interconnect resistance). To maintain a reasonable noise margin, we require $V_{S.A.}$ to reach at least 50 mV before we can declare that the device is ON [40]. A dynamic read operation must therefore last as long as the maximum amount of time it takes for $V_{S.A.}$ to reach 50 mV in the case that the device is ON. If $V_{S.A.}$ reaches 50 mV during this allotted time, the device can be considered ON; if it is below this level, the device is OFF. The worst-case scenario (or maximum amount of time for $V_{S.A.}$ to reach 50 mV) occurs when we measure a device that is at the corner of the array that is farthest from the supply voltage and sense amplifier, which results in the largest possible interconnect capacitance.

The AM array operates similarly (Fig. 6.7(b)). Here, the access transistor starts OFF, and the bitline starts at 1 V. 2 V is then applied to the wordline to turn the access transistor ON, and the bitline is allowed to float. $V_{S.A.}$ (initially 1 V) begins to decrease as the bitline is discharged through device resistance. If it discharges quickly, the device is ON; otherwise, it is OFF. Quantitatively, we determine the maximum amount of time it takes $V_{S.A.}$ to decrease by 50 mV in the case that the device is ON; this delay defines the time necessary for a read operation.

In both AM and PM arrays, it is the device ON resistance that is relevant to determining the delay. We performed calculations for devices with areas of 50 x 50 nm^2 and 250 x 250 nm^2. This corresponds to a minimum feature size of 50 nm and 250 nm, respectively. In a PM crosspoint array, this implies that the width of each interconnect line is also 50 (or 250 nm), with an interline spacing of 50 nm (or 250 nm) and an overall cell size of 100 x 100 nm^2 or 500 x 500 nm^2 (= 4 F^2, as in Figure 6.6). For comparison, the current cell size of flash memory is 10^5 nm^2 (Table 6.1), while some molecular-scale memory arrays with cell sizes of 40 x 40 nm^2 have already been reported [41]. For the same device sizes of 50 x 50 nm^2 and 250 x 250 nm^2, the AM array will have a larger cell size than the PM array, and also have wider and/or more widely spaced interconnects. To simplify the calculation of interconnect resistance and capacitance (and make it easier to compare results for AM and PM arrays), we instead assumed that the cell size of the AM architecture was the same as the PM array (i.e. 100 x 100 nm^2 or 500 x 500 nm^2), and that the interconnects had the same width (50 nm or 250 nm) and spacing (50 nm or 250 nm) as in the PM array. For a given device area, PM and AM arrays with the same size (in bits) therefore had identical interconnect resistance and capacitance.

We used a 4-segment lumped Pi model to model the resistance and capacitance of the interconnect lines [14]. The largest possible delay will correspond to the longest interconnect length, which is given by the square root of the product of the number of bits in the array times the cell size (in the case of a square array). Next, we need to determine values of for interconnect resistance/length and capacitance/length. To calculate the resistance/length, we assumed aluminum interconnect lines with a resistivity of 2×10^{-6} Ω cm and a height to width ratio of 2:1 [7]. This resulted in a resistance of 4×10^{4} Ω/cm for the 50 nm line and 1.6×10^{3} Ω/cm for the 250 nm line.

Estimation of the interconnect capacitance/length requires careful consideration because simple one-dimensional parallel-plate capacitance models can severely underestimate the true capacitance. A cross-section of the interconnect geometry that we used is shown in Figure 6.8. Because we have assumed identical interconnect geometries for both AM and PM arrays (as discussed above) the diagram is relevant to both architectures. The metal interconnects have width W and height H (which is equal to 2 W) and are spaced by L (= W in our calculations). They are separated from a

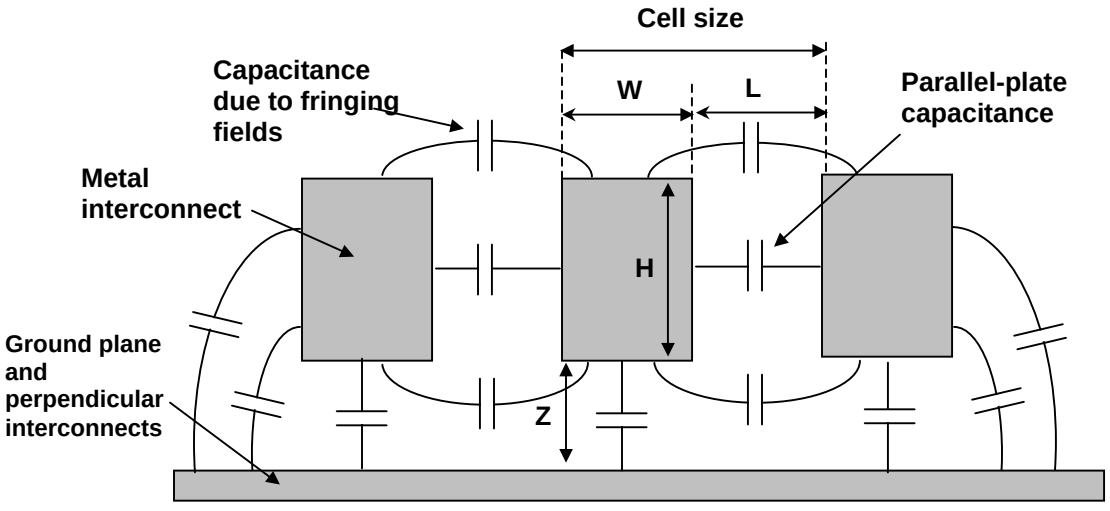


Figure 6.8. Cross-section model of interconnects showing parallel-plate capacitance and capacitance due to fringing fields. Of critical importance is the capacitance between parallel interconnects; the capacitance to the ground plane and perpendicular interconnects is much lower. When calculating the capacitance, we assume that SiO_2 is used to insulate the interconnects.

ground plane (and perpendicular metal interconnects) by a distance Z. We treated the perpendicular metal interconnects and wafer ground plane as a single plane at a distance Z. This assumption should have little effect because the capacitance between parallel interconnects plays the dominant role in determining the overall capacitance for this geometry [14]. We assumed that SiO_2 ($\varepsilon = 3.9$) was used to insulate the lines.

In a parallel-plate model, the capacitance/length between parallel interconnect lines would not depend on W and would be given by $\varepsilon\varepsilon_0 H/L$. Similarly, the capacitance to the ground plane would not depend on H and would be given by $\varepsilon\varepsilon_0 W/Z$. However, the fringing fields shown in Figure 6.8 significantly increase the capacitance beyond this simple formula, so that the capacitance between parallel interconnects depends on W and the capacitance to the ground plane depends on H. To obtain a better estimate of the capacitance (including fringing effects), we referred to S. M. Kang and Y. Leblebici [14], where the total capacitance is reported a function of feature size for a design geometry similar to Figure 6.9 (in the geometry used by Kang and Leblebici, H is set to W, instead of 2 W as in our case). From this reference, we estimate a capacitance of ~3 pF/cm, for both the 50 nm and 250 nm lines (and both PM and AM architectures).

In the PM array, the diode was treated as an ideal Si diode (with an ON slope of 60 mV/decade) (the results were insensitive to the specific parameters used in the diode model over a wide range of values). In the AM array, the access transistor was modeled as a standard Si transistor with an oxide thickness of 1 nm and width = channel length = 45 nm. A Spice Level 1 model was used. This model ignores velocity saturation, so we accounted for short-channel effects by reducing the mobility to 35 cm^2/Vs and setting L_d to 2 nm (these characteristics were chosen so that the simulated output characteristics matched the 45 nm MOSFET characteristics reported by Chan et al for drain voltages below 1 V [42]). The resistance of the sense amplifier for both arrays was kept several orders of magnitude higher than the device ON resistance.

The ON resistance necessary to achieve read times of 10 ns or 100 ns in devices with active areas of 50 x 50 nm^2 or 250 x 250 nm^2 for PM and AM arrays of different sizes is shown in Figure 6.9. In small arrays ($<10^4$ bits) with large device areas, relatively large ON resistances $>10^{-2}\ \Omega\ cm^2$ still allow fast access times (10 ns, comparable to SRAM) for both architectures. However, even in 10^4 bit arrays, when

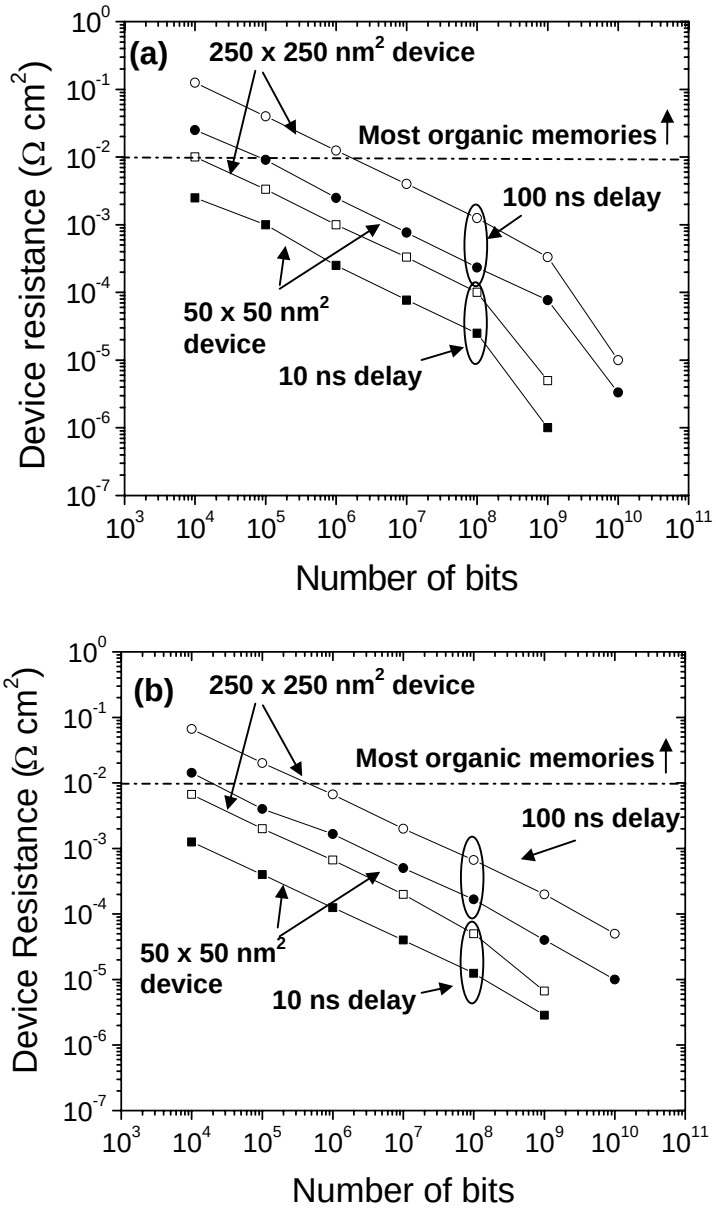


Figure 6.9. Required device resistance in circuit simulations to achieve access times of 10 ns and 100 ns for different size memory arrays in (a) a passive matrix architecture and (b) an active matrix architecture. Results for 50 x 50 nm^2 and 250 x 250 nm^2 device areas are shown. Also shown is a typical resistance range for most organic memory devices.

the device area is scaled to 50 x 50 nm^2 relatively low ON resistances of 10^{-3} Ω cm^2 are necessary for a 10 ns delay. Furthermore, as the number of bits increases the required ON resistance decreases rapidly, so that for a 1 Gb array an ON resistance near 10^{-6} Ω cm^2 is required for a 10 ns read time, regardless of the architecture. Overall, the trend is as expected: for a constant access time the product of device ON-resistance and interconnect capacitance must be kept constant, so that as the number of bits (and thus array capacitance) increases, the device resistance must decrease.

We note that our estimates of the ON-resistance needed to achieve these read times are relatively robust despite the simplifying assumptions made in their derivation. Delays could be decreased slightly by using rectangular (instead of square) arrays, to minimize the length of the interconnect line that must be charged (or discharged) through the device resistance (e.g. the word line in the PM architecture). The capacitance could also be decreased by using an insulator with a lower dielectric constant than SiO_2 between the metal interconnects. But this would again result in only slight decreases in the read time. Furthermore, in this model, we have neglected any parasitic leakage currents through inactive devices. Inclusion of these leakage currents would result in even lengthier read times.

Most organic devices have large ON resistance, much greater than 10^{-2} Ω cm^2 and as high as 10^4 Ω cm^2 (Table 6.2), so they would be compatible with fast read times only in very small arrays. For example, a memory with an ON resistance of 10^{-1} Ω cm^2 would be limited to a relatively large device area of 250 x 250 nm^2 in a relatively small array of 10^4 bits to have a read time of 100 ns, which is comparable to flash memory (80 ns). For comparison, alternative technologies such as inorganic phase-change memories (which would use a similar array architecture and read operation) have a much lower ON-state bulk resistivity of ~10^{-2} Ω cm, which translates (for a ~100 nm device thickness) into an ON-resistance of 10^{-7} Ω cm^2, allowing operation in much larger (>10^9 bit) arrays [43]. For higher-resistance organic memories, dividing large memory arrays into numerous small arrays is not economical, as this requires increased numbers of (relatively expensive) support circuits. This is a fundamental problem that can severely limit the potential for application of these devices, particularly in the highly-scaled applications for which these devices have attracted considerable interest.

6.6.2 Large ON/OFF Ratio

A large ON/OFF ratio is desirable to offset the effects of statistical variation in the resistances of the ON and OFF states of memory cells during read operations. The difference in the ON and OFF resistances of devices should be much larger than the typical variation in the resistance of these states to minimize the possibility of a state being read incorrectly. Organic devices perform very well in this regard, and have relatively large ON/OFF ratios between 10^2 to 10^7 (Table 6.2). In comparison, inorganic magnetic tunnel junction random access memories, which would operate in similar arrays, typically have much lower ON/OFF ratios of ~1.5 (although they are also expected to have much more reproducible ON and OFF states) [44].

A large ON/OFF ratio becomes even more critical in large arrays. In a read operation in an array, a voltage is applied to the active word line, and the resistance of a memory device is measured on the relevant bit line to determine the state of the device. This operation is often represented in a simplified form as attaching a load resistor to the bit line, so that the memory device and load resistor form a voltage divider, with the voltage across the load resistor used to determine whether the device is ON or OFF (as in the read operations in Section 6.6.1). Other word and bit lines are held at ground (or may be reverse-biased in the PM architecture) to minimize parasitic leakage currents. Nevertheless, in large arrays these leakage paths and the resistance of the interconnect lines can become significant. In addition to the resistance of the memory device, the voltage on the load resistor then becomes dependent on the location of the device within the array, as measurements on devices located a large distance from the support circuits will include significant interconnect resistance and parasitic current leakage [44]. This effect is true for both PM and AM architectures, although leakage current plays a more prominent role in the PM array. The ON/OFF ratio can thus limit the size of the array, although the exact limitations for large arrays are difficult to model (and depend on a number of additional factors, such as interconnect resistance) [44].

6.6.3 Rectification Ratio and Bipolar vs Unipolar operation

In a large memory array, there are an enormous number of indirect electrical paths between any two devices on the array. To write and read single memory elements (and to decrease the power consumed during this operation) it is necessary

to reduce the effect of these indirect pathways by maximizing their electrical resistance. In an AM architecture, this is accomplished with the access transistor, so that the only connections between word and bit lines are through the (very high) gate-channel impedance of the FET (and all devices on the same bit line are isolated by the OFF resistance of the FET channels) (Fig. 6.4). In a PM architecture, the devices themselves form connections between word and bit lines. To reduce parasitic leakage in the PM architecture, it is necessary to reverse bias inactive interconnect lines during program and read operations. The rectification ratio of the device then determines the size of the PM array. A rule of thumb (from work on PM displays) is that the number of devices on a word or bit is limited to this ratio (i.e., a rectification ratio of 100 allows an array with 100 devices on each word and bit line, for a total size of ~10 kbits) [10].

In most previous work on organic memory, the rectification ratio of the device is not reported. However, in instances where it is reported (or when it can be estimated based on presented data) it is generally less than 1000, and often close to unity [24, 26, 32, 45-53], severely limiting the size of any memory array. The extent to which the rectification ratio of these devices could be increased (without affecting the memory mechanism) is unclear. An alternative, more straightforward approach is to integrate devices with a high-performance Si diode. A Si diode, with a rectification ratio greater than 10^9 (at $\pm$0.6 V), would in principle allow a $10^9 \times 10^9$ array [54]. This would increase the complexity (and cost) of the fabrication process, although it would still likely remain cheaper than the AM architecture. In fact, if the memory devices were deposited directly on top of thin-film Si diodes it would not necessarily increase the cell area above $4F^2$, and this approach to integrating a silicon diode with an organic memory device has already been demonstrated in the WORM memories [35, 55].

Integration with a diode to achieve large array sizes presents a new problem for most organic memory technologies. Most technologies in Table 6.2 are bipolar, and require opposite voltage polarities for write and erase operations. In series with a high-performance diode, these devices could no longer be reprogrammed, as any applied reverse bias would be dropped almost entirely across the diode. To maintain compatibility with a series diode, device writing and erasing must be unipolar, a requirement satisfied by only two of the previously reported technologies (the organic electroformed device and Cu-organic device). The limited rectification ratio and bipolar nature of most other organic devices at present restricts their compatibility with large PM arrays that have the best potential for low-cost fabrication.

6.6.4 Compatibility with CMOS Circuits

Devices must be compatible with CMOS fabrication processes and CMOS operation. We consider fabrication compatibility first. Fabrication compatibility requires that the organic process be integrated with the silicon process without damaging the silicon process, and vice versa. Because organic memory is still in early stages of research and development, it is difficult to evaluate the devices reported in Table 6.2 in this regard, as few authors have addressed this issue. We will instead discuss several general concerns.

The main potential source of degradation of the silicon processes is contamination, particularly from metals (such as gold or copper) that are commonly used as electrodes (or in the active layer) of many organic memories [16]. Even minute quantities of these metals, which generally diffuse readily into silicon, can cause undesired doping of silicon FETs leading to loss of control over their electrical characteristics. Metal contamination has thus traditionally been a critical issue in CMOS manufacture [17, 56]. However, with the move to Cu interconnects in manufacturing in the late 1990's, techniques for depositing barrier layers (to prevent metal diffusion into the silicon) have been developed, so that this aspect of materials compatibility is less of a concern than previously [57, 58].

Protection of the organic materials during silicon processing represents a more difficult challenge due to the extremely high temperatures (>1000° C) and harsh chemical environments used in typical CMOS fabrication [59]. One solution that is often proposed is to add organic materials to the "back end" of the silicon process, since temperatures generally decrease to only 200 to 300 °C in the last CMOS process steps [60]. This reduces the challenge, although temperatures of several hundred degrees can still degrade many organic materials. Still, recent demonstrations of organic capacitors (based on self-assembled monolayers of porphyrin) that can withstand temperatures of 400 °C, and polymer OLEDs based on PPV that were fabricated with a number of conventional MOS process steps indicate that it should be possible to integrate appropriately designed organic devices with CMOS processes [37, 61].

Devices must also be compatible with CMOS operation. This generally implies low voltage (~1 V) operation to match CMOS logic levels. Though most organic devices have much lower program voltage requirements than flash memory (>10 V),

only one (the molecular SAM), with program voltages of ~0.5 V, is completely compatible. Additional circuits to interface with CMOS logic may therefore be necessary. A second requirement is stable operation at high temperatures, as CMOS circuits can reach 140 °C during normal operation [62]. No reported organic programmable-resistance memory devices have been tested in this temperature range so their stability remains a concern.

6.7 Summary

The market for solid-state nonvolatile memory is currently dominated by flash memory. However, there is great interest in developing novel memory technologies because of the performance limitations of flash memory, the most important being its slow program times (~ 1 ms), large programming voltages (>10 V) and limited durability (10^6 cycles). Organic programmable-resistance memory devices are one promising technology that has recently attracted significant attention. Organic memories are based on a number of different compounds and utilize a variety of different physical mechanisms, although in most cases more work needs to be done to better understand these mechanisms. Initial measurements suggest that many organic devices have attributes, including fast programming times (10^{-3} to 10^{-8} s) and low programming voltages (0.25 to 10 V) that may enable them to overcome some of the performance limitations of flash memory.

For fast program and read times in commercial application it will be necessary to integrate these devices with CMOS support circuits. In a PM architecture, exemplified by the crossbar array, these CMOS circuits could remain outside the array, so that the organic devices could be fabricated on a low-cost substrate then later interfaced with the higher-cost CMOS circuits. A drawback is that for use in PM arrays, devices must have very large rectification ratios to minimize parasitic leakage currents. Alternatively, devices could be fabricated (at higher cost) in AM arrays, with a CMOS transistor integrated within each cell to minimize parasitic leakage. In either case, large arrays are desirable, to obtain large memory densities (> Gb) with a minimal number of expensive support circuits.

Fabrication in large PM or AM arrays with CMOS support circuits places very stringent additional demands on the performance of memory devices. One of the most important issues is the need for low-ON resistance. Modeling of the dynamics of a

read operation indicate that devices should have an ON-resistance of 10^{-5} Ω cm^2 to 10^{-6} Ω cm^2 for fast (10 ns) read times in large (10^9 bits) arrays. This required resistance is much below the resistance of previously reported organic programmable-resistance memories, most of which have ON-resistance that is greater than 10^{-2} Ω cm^2. Because most demonstrated technologies are limited in at least one of the requirements (particularly the need for low ON resistance), new organic memory devices are desirable to meet the goal of a commercially successful organic memory.

References

[1] B. Prince and G. Due-Gundersen, *Semiconductor Memories*. 1983, New York: John Wiley & Sons.

[2] *The International Technology Roadmap for Semiconductors: 2004 Update*. 2004 [cited 11/20/2005; webpage]. Available from: http://public.itrs.net/.

[3] Y. Nakagome, M. Horiguchi, T. Kawahara and K. Itoh, "Review and Future Prospects of Low Voltage Ram Circuits" *IBM Journal of Research and Development* **47** (5/6), 525-552 (2003).

[4] E. Grochowski and R. D. Halem, "Technological Impact of Magnetic Hard Disk Drives on Storage Systems" *IBM Systems Journal* **42** (2), 338-346 (2003).

[5] K. Kim and G.-H. Koh, "Future Memory Technology Including Emerging New Memories" *Proc. 24th International Conference on Microelectronics* **1**, 377-383 (2004).

[6] L. Mason. *Memory for the Consumer Electronics Market*. 2004 [cited 11/18/2005; webpage]. Available from: http://www.denalisoft.co.jp/memcon-tokyo/docs/0915-002.pdf.

[7] B. G. Streetman and S. Banerjee, *Solid State Electronic Devices*. 5th ed. 2000, Upper Saddle River, NJ: Prentice Hall.

[8] W. Kuhr, A. R. Gallo, R. W. Manning and C. W. Rhodine, "Molecular Memories Based on a CMOS Platform" *MRS Bulletin* **29** (11), 838-841 (2004).

[9] H. Goronkin and Y. Yang, "High-Performance Emerging Solid-State Memory Technologies" *MRS Bulletin* **29** (11), 805-808 (2004).

[10] J. C. Scott, "Is There an Immortal Memory?" *Science* **304** (5667), 62-63 (2004).

[11] M. LaPedus. *Samsung Losing Share in Flash Rankings*. 2005 [cited 11/18/2005; webpage]. Available from: http://www.eetimes.com/showArticle.jhtml?articleID=173500390.

[12] B. Kumagai and S. Beekman. *Choosing Flash Memory*. [cited 11/18/2005; webpage]. Available from: http://www.electronicproducts.com/ShowPage.asp?SECTION=3700&PRIMID=&FileName=TOSHIBA.apr2004.HTML.

[13] A. Tal. *Two Technologies Compared: NOR Vs NAND Whitepaper*. 2003 [cited 11/18/2005; webpage]. Available from: http://www.m-sys.com/NR/rdonlyres/05334F84-C86D-4925-AE56-7ED0CEEC7321/229/NOR_vs_NAND.pdf.

[14] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*. 3rd ed. 2003, Boston: McGraw Hill.

[15] S. Tehrani, E. Chen, M. Durlam, M. DeHerrera, J. M. Slaughter, J. Shi and G. Kerszykowski, "High Density Submicron Magnetoresistive Random Access Memory (Invited)" *Journal of Applied Physics* **85** (8), 5822-5827 (1999).

[16] C. U. Pinnow and T. Mikolajick, "Material Aspects in Emerging Nonvolatile Memories" *Journal of the Electrochemical Society* **151** (6), K13-K19 (2004).

[17] Y. Yang, L. P. Ma and J. H. Wu, "Organic Thin-Film Memory" *MRS Bulletin* **29** (11), 833-837 (2004).

[18] L. F. Pender and R. J. Fleming, "Memory Switching in Glow-Discharge Polymerized Thin-Films" *Journal of Applied Physics* **46** (8), 3426-3431 (1975).

[19] R. S. Potember, T. O. Poehler and D. O. Cowan, "Electrical Switching and Memory Phenomena in Cu-Tcnq Thin-Films" *Applied Physics Letters* **34** (6), 405-407 (1979).

[20] H. K. Henisch and W. R. Smith, "Switching in Organic Polymer-Films" *Applied Physics Letters* **24** (12), 589-591 (1974).

[21] H. Carchano, R. Lacoste and Y. Segui, "Bistable Electrical Switching in Polymer Thin Films" *Applied Physics Letters* **19** (10), 414-& (1971).

[22] C. N. Lau, D. R. Stewart, R. S. Williams and M. Bockrath, "Direct Observation of Nanoscale Switching Centers in Metal/Molecule/Metal Structures" *Nano Letters* **4** (4), 569-572 (2004).

[23] Y. Luo, C. P. Collier, J. O. Jeppesen, K. A. Nielsen, E. Delonno, G. Ho, J. Perkins, H. R. Tseng, T. Yamamoto, J. F. Stoddart and J. R. Heath, "Two-Dimensional Molecular Electronics Circuits" *ChemPhysChem* **3** (6), 519-525 (2002).

[24] L. D. Bozano, B. W. Kean, V. R. Deline, J. R. Salem and J. C. Scott, "Mechanism for Bistability in Organic Memory Elements" *Applied Physics Letters* **84** (4), 607-609 (2004).

[25] L. P. Ma, J. Liu and Y. Yang, "Organic Electrical Bistable Devices and Rewritable Memory Cells" *Applied Physics Letters* **80** (16), 2997-2999 (2002).

[26] J. Y. Ouyang, C. W. Chu, C. R. Szmanda, L. P. Ma and Y. Yang, "Programmable Polymer Thin Film and Non-Volatile Memory Device" *Nature Materials* **3** (12), 918-922 (2004).

[27] H. S. Majumdar, J. K. Baral, R. Osterbacka, O. Ikkala and H. Stubb, "Fullerene-Based Bistable Devices and Associated Negative Differential Resistance Effect" *Organic Electronics* **6**, 188-192 (2005).

[28] H. S. Majumdar, A. Bolognesi and A. J. Pal, "Switching and Memory Devices Based on a Polythiophene Derivative for Data-Storage Applications" *Synthetic Metals* **140**, 203-206 (2004).

[29] A. Bandyopadhyay and A. J. Pal, "Multilevel Conductivity and Conductance Switching in Supramolecular Structures of an Organic Molecule" *Applied Physics Letters* **84** (6), 999-1001 (2004).

[30] M. A. Reed, J. Chen, A. M. Rawlett, D. W. Price and J. M. Tour, "Molecular Random Access Memory Cell" *Applied Physics Letters* **78** (23), 3735-3737 (2001).

[31] Y. Chen, G. Y. Jung, D. A. A. Ohlberg, X. M. Li, D. R. Stewart, J. O. Jeppesen, K. A. Nielsen, J. F. Stoddart and R. S. Williams, "Nanoscale Molecular-Switch Crossbar Circuits" *Nanotechnology* **14** (4), 462-468 (2003).

[32] J. H. Krieger, S. V. Trubin, S. B. Vaschenko and N. F. Yudanov, "Molecular Analogue Memory Cell Based on Electrical Switching and Memory in Molecular Thin Films" *Synthetic Metals* **122** (1), 199-202 (2001).

[33] L. P. Ma, Q. F. Xu and Y. Yang, "Organic Nonvolatile Memory by Controlling the Dynamic Copper-Ion Concentration within Organic Layer" *Applied Physics Letters* **84** (24), 4908-4910 (2004).

[34] T. Oyamada, H. Tanaka, K. Matsushige, H. Sasabe and C. Adachi, "Switching Effect in Cu : Tcnq Charge Transfer-Complex Thin Films by Vacuum Codeposition" *Applied Physics Letters* **83** (6), 1252-1254 (2003).

[35] S. Moller, C. Perlov, W. Jackson, C. Taussig and S. R. Forrest, "A Polymer/Semiconductor Write-Once Read-Many-Times Memory" *Nature* **426** (6963), 166-169 (2003).

[36] G. Parthasarathy, J. Liu and A. R. Duggal, "Organic Light Emitting Devices: From Displays to Lighting" *The Electrochemical Society Interface* **12** (2), 42-47 (2003).

[37] W. Kuhr, "Integration of Molecular Components into Silicon Memory Devices" *The Electrochemical Society Interface* **13** (1), 34-38 (2004).

[38] T. N. Jackson, Y. Y. Lin, D. J. Gundlach and H. Klauk, "Organic Thin-Film Transistors for Organic Light-Emitting Flat-Panel Display Backplanes" *IEEE Journal on Selected Topics in Quantum Electronics* **4** (1), 100-104 (1998).

[39] M. Kimura, I. Yudasaka, S. Kanbe, H. Kobayashi, H. Kiguchi, S.-I. Seki, S. Miyashita, T. Shimoda, T. Ozawa, K. Kitawada, T. Nakazawa, W. Miyazawa and H. Ohshima, "Low-Temperature Polysilicon Thin-Film Transistor Driving with Integrated Driver for High-Resolution Light-Emitting Polymer Display" *IEEE Transactions on Electron Devices* **46** (12), 2282-2288 (1999).

[40] A. Yamazaki, F. Morishita, N. Watanabe, T. Amano, M. Haraguchi, H. Noda, A. Hachisuka, K. Dosaka, K. Arimoto, S. Wake, H. Ozaki and T. Yoshihara, "A Study of Sense-Voltage Margins in Low-Voltage-Operating Embedded Dram Macros" *IEICE Transactions on Electronics* **E88C** (10), 2020-2027 (2005).

[41] Y. Chen, D. A. A. Ohlberg, X. M. Li, D. R. Stewart, R. S. Williams, J. O. Jeppesen, K. A. Nielsen, J. F. Stoddart, D. L. Olynick and E. Anderson, "Nanoscale Molecular-Switch Devices Fabricated by Imprint Lithography" *Applied Physics Letters* **82** (10), 1610-1612 (2003).

[42] V. Chan, R. Rengarajan, N. Rovedo, W. Jin, T. Hook, P. Nguyen, J. Chen, E. Nowak, X.-D. Chen, D. Lea, A. Chakravarti, V. Ku, S. Yang, A. Steegen, C. Baiocco, P. Shafer, H. Ng, S.-F. Huang and C. Wann, "High Speed 45nm Gate Length Cmosfets Integrated into a 90 Nm Bulk Technology Incorporating Strain Engineering" *IEDM '03 Technical Digest*, 3.8.1-3.8.4 (2003).

[43] A. Pirovana, A. L. Lacaita, A. Benvenuti, F. Pellizzer, F. Hudgens and R. Bez, "Scaling Analysis of Phase-Change Memory Technology" *IEDM '03 Technical Digest.*, 29.6.1- 29.6.4 (2003).

[44] C. J. Amsinck, N. H. D. Spigna, D. P. Nackashi and P. D. Franzon, "Scaling Constraints in Nanoelectronic Random-Access Memories" *Nanotechnology* **16**, 2251-2260 (2005).

[45] T. Tsujioka, "Electrical Molecular Memory Using Diarylethene Derivatives" *Molecular Crystals and Liquid Crystals* **431**, 391-395 (2005).

[46] J. Y. Ouyang, C. W. Chu, D. Sieves and Y. Yang, "Electric-Field-Induced Charge Transfer between Gold Nanoparticle and Capping 2-Naphthalenethiol and Organic Memory Cells" *Applied Physics Letters* **86** (12), 123507 (2005).

[47] D. Tondelier, K. Lmimouni, D. Vuillaume, C. Fery and G. Haas, "Metal/Organic/Metal Bistable Memory Devices" *Applied Physics Letters* **85** (23), 5763-5765 (2004).

[48] C. Jiangshan and M. Dongge, "Single-Layer Organic Memory Devices Based on N,N'-Di(Naphthalene-L-Yl)-N,N'-Diphenyl-Benzidine" *Applied Physics Letters* **87** (2), 23505-1 (2005).

[49] O. Jianyong, C. Chih-Wei, D. Sieves and Y. Yang, "Electric-Field-Induced Charge Transfer between Gold Nanoparticle and Capping 2-Naphthalenethiol and Organic Memory Cells" *Applied Physics Letters* **86** (12), 123507-1 (2005).

[50] J. Y. Ouyang, C. W. Chu, R. J. H. Tseng, A. Prakash and Y. Yang, "Organic Memory Device Fabricated through Solution Processing" *Proceedings of the IEEE* **93** (7), 1287-1296 (2005).

[51] J. S. Chen and D. G. Ma, "Single-Layer Organic Memory Devices Based on N,N '-Di(Naphthalene-L-Yl)-N,N '-Diphenyl-Benzidine" *Applied Physics Letters* **87** (2), 023505 (2005).

[52] Anon, "Organic Memory Device" *IEEE Micro* **22** (4), 13-13 (2002).

[53] L. P. Ma, J. Liu, S. Pyo, Q. F. Xu and Y. Yang, "Organic Bistable Devices" *Molecular Crystals and Liquid Crystals* **378**, 185-192 (2002).

[54] S. Sze, *Physics of Semiconductor Devices*. 2nd ed. 1981, New York: John Wiley and Sons.

[55] S. Moller, S. R. Forrest, C. Perlov, W. Jackson and C. Taussig, "Electrochromic Conductive Polymer Fuses for Hybrid Organic/Inorganic Semiconductor Memories" *Journal of Applied Physics* **94** (12), 7811-7819 (2003).

[56] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*. 2nd ed. 1986, New York: John Wiley and Sons.

[57] T. Eltringham. *Big Blue Goes Copper*. 1997 [cited 11/18/05; Available from: http://www.copper.org/innovations/1997/Nov1997/bigblue.htm.

[58] R. J. Luyken and F. Hofmann, "Concepts for Hybrid CMOS-Molecular Non-Volatile Memories" *Nanotechnology* **14**, 273-276 (2003).

[59] J. D. Plummer, M. D. Deal and P. B. Griffin, *Silicon VLSI Technology: Fundamentals, Practice and Modeling*. Prentice Hall Electronics and Vlsi Series, ed. C. Sodini. 2000, Upper Sadle River: Prentice Hall.

[60] J. R. Sheats, "Manufacturing and Commercialization Issues in Organic Electronics" *Journal of Materials Research* **19** (7), 1974-1989 (2004).

[61] L. M. H. Heinrich, J. Muller, U. Hilleringmann, K. F. Goser, A. Holmes, D.-H. Hwang and R. Stern, "CMOS-Compatible Organic Light-Emitting Diodes" *IEEE Transactions on Electron Devices* **44** (8), 1249-1252 (1997).

[62] Z. M. Liu, A. A. Yasseri, J. S. Lindsey and D. F. Bocian, "Molecular Memories That Survive Silicon Device Processing and Real-World Operation" *Science* **302** (5650), 1543-1545 (2003).

Chapter 7

Molecular-scale Nonvolatile Memory Device: Experimental Characteristics

7.1 Introduction

For a high-density and high-speed organic memory, the results of Chapter 6 indicate that a device with both fast switching times and extremely low ON resistance (for fast read times) is desirable. In this chapter, we describe the experimental characteristics of the first organic memory device that appears capable of meeting these requirements. Our approach is based on MUA films and we utilize the two-terminal structures described in Chapters 4 and 5.

This chapter is organized as follows. In Section 7.2 we describe device fabrication and provide an overview of the experimental setup. The process used to place devices into a programmable-resistance state, called forming, is described in Section 7.3. Next, we describe pulsed measurements on formed devices (Section 7.4) then current-voltage scans that revealed negative differential resistance (NDR) (Section 7.5). In Section 7.6 we describe how devices changed appearance after forming. Section 7.7 summarizes the chapter.

7.2 Device Preparation and Experimental Setup*

Two-terminal devices with self-assembled multilayers of MUA sandwiched between metal electrodes were prepared as described in Chapters 4 and 5. Most devices utilized the edge structure or planar PoPI structure, although a few utilized the planar PrPM structures (Fig. 7.1).

Low-frequency current-voltage scans (<20 V/s) and pulsed measurements (> 1 ms pulse length) were performed with an Agilent semiconductor parameter analyzer. In measurements with voltage pulses, and in high frequency current-voltage scans, an Agilent 33220A arbitrary waveform generator was used to generate the applied

* For additional experimental details, please refer to Appendix B.

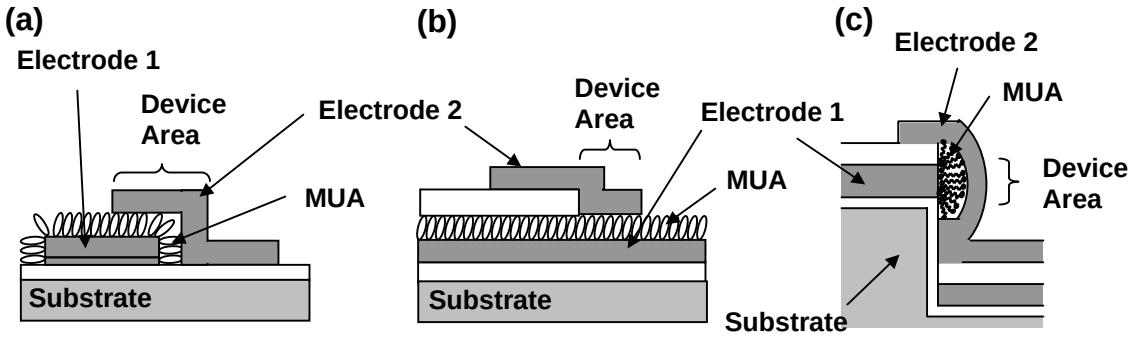


Figure 7.1. Schematics of two-terminal (a) PrPM, (b) PoPI, and (c) edge structures. The PrPM and PoPI structures are reproduced from Figures 4.2 and 4.3, and the edge structure is reproduced from Figure 5.2.

voltage. Time sequences of the circuit voltage were recorded with a Tektronix TDS 2014 digital storage oscilloscope. Current was determined by measuring the voltage across a resistor placed in series with the device. The size of the resistor was chosen so that the voltage drop over the resistor remained a small fraction (<10%) of the voltage applied to the circuit. All measurements were done in a nitrogen-filled glovebox.

7.3 Forming of Devices

As fabricated, most devices were insulating, with current-voltage characteristics that were stable for voltages below 2 to 3 V (these insulating characteristics were described previously in Chapters 4 and 5). When the voltage was scanned over larger ranges, we typically observed a rapid increase in current at a certain voltage (Fig. 7.2(a)), after which the device conductance permanently increased, typically by many orders of magnitude. Following convention, we defined the voltage at which this rapid increase in current occurred the breakdown voltage of the device. Because the breakdown voltage is another way (besides its conductance) to characterize the quality of an insulating layer [2], after measuring the electrical currents in devices (as reported in Chapters 4 and 5) we often applied a large-range voltage sweep (i.e. larger than the ± 3V range over which most devices had stable current-voltage traces) (2V/s) to determine their breakdown voltage.

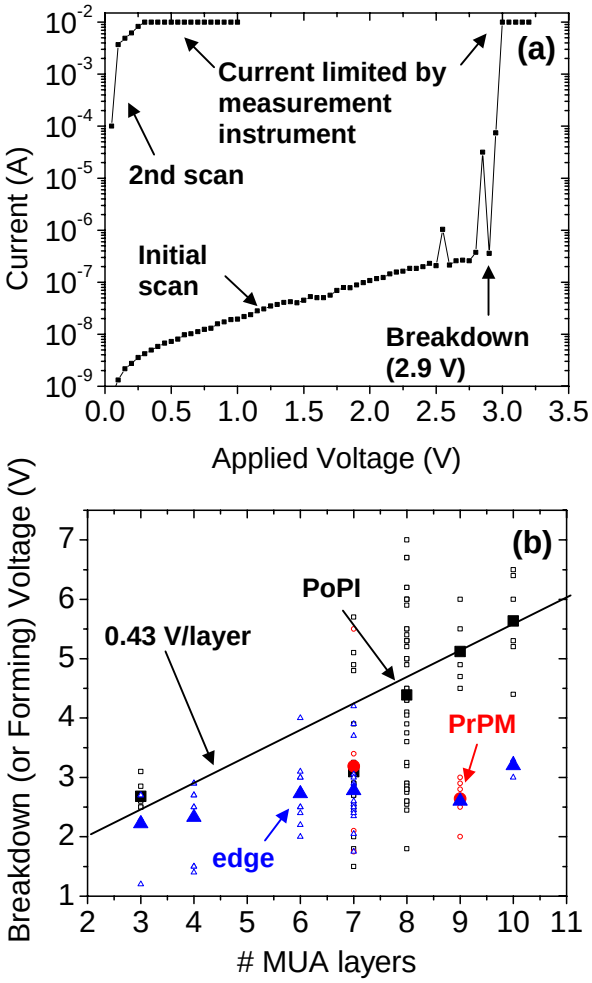


Figure 7.2. (a) Current vs voltage scan on 8-layer device in PoPI structure showing breakdown voltage (2.9 V) in first scan. In subsequent scans the device was shorted. (b) Breakdown (or forming) voltage vs number of MUA layers for PrPM (red circles), PoPI (black squares), and edge (blue triangles) structures. Data are smaller, hollow points and averages at each thickness are larger, solid points. A slope of 0.43 V/layer was determined by fitting the average of the PoPI data.

We did not observe this breakdown voltage to vary significantly with most fabrication parameters (i.e. top metal deposition angle, rate, etc., as described in Chapter 4). Therefore we only distinguished between devices based on their structure (PrPM, PoPI, or edge) and number of MUA layers (Fig. 7.2(b); in this plot we refer to the voltage as breakdown or forming, a distinction that we will make clear later). We observed significant scatter in the breakdown voltage, reflecting the statistical nature of

the breakdown process (previous measurements on insulating monolayers found that breakdown voltages varied by over 1.5 V for identical samples [2]) as well as the variation in quality of our devices. Nevertheless, several trends can be observed. First, the average breakdown voltage of MUA films in the PoPI structure increased with thickness, as expected since dielectric breakdown is generally considered a field-dependent process. A linear fit to the PoPI structure resulted in a slope of 0.43 V/layer, from which we obtain an average breakdown field of 2.7 MV/cm by dividing by the average thickness of a MUA layer (1.6 nm, from Chapter 3). This value is lower than previous measurements on alkanethiol monolayers that found breakdown fields in the 8 to 35 MV/cm range [2, 3]. In these experiments, the monolayers were contacted by top mercury electrodes or gold electrodes deposited electrolessly; these approaches to contacting the layers likely resulted in less damage to the organic film (and thus a higher breakdown field) than our evaporated top contacts. Nevertheless, we still measure a very high breakdown field close to that of SiO_2 (~10 MV/cm). In fact, breakdown fields as high as 6.5 MV/cm were measured in some devices.

Unlike the PoPI structure, the breakdown voltages of edge and PrPM structures were found to be ~2.5 V, roughly independent of the number of MUA layers. The lower breakdown voltage of most of these devices (in comparison with the PoPI structure) and the lack of a dependency on the number of MUA layers is likely because both of these devices contain MUA films grown on the edge of a metal film. As discussed in Chapters 4 and 5, both of these structures typically had higher current densities than the PoPI structure. The higher current densities were attributed to increased defects because of the poorer MUA growth along the vertical edge of the 1st gold layer. This poorer quality MUA layer is likely to also lead to the lower breakdown voltages and the weak dependence of the breakdown voltage on film thickness that we observe here.

Although the electrical characteristics after breakdown were initially considered of little importance, we discovered that the properties of many of these “post-breakdown” devices were very interesting. In addition to having an increased conductance (typically by 10^2 to 10^6), the low-voltage conductance of some devices could be programmed with voltage pulses (Section 7.4), and depending on the scan speed, could display NDR (Section 7.5). We also often observed a change in device appearance (Section 7.6).

Application of a voltage sweep (typically from 0 to 8 V) to an insulating device could lead to one of two conditions. The first possibility is that the device could enter a

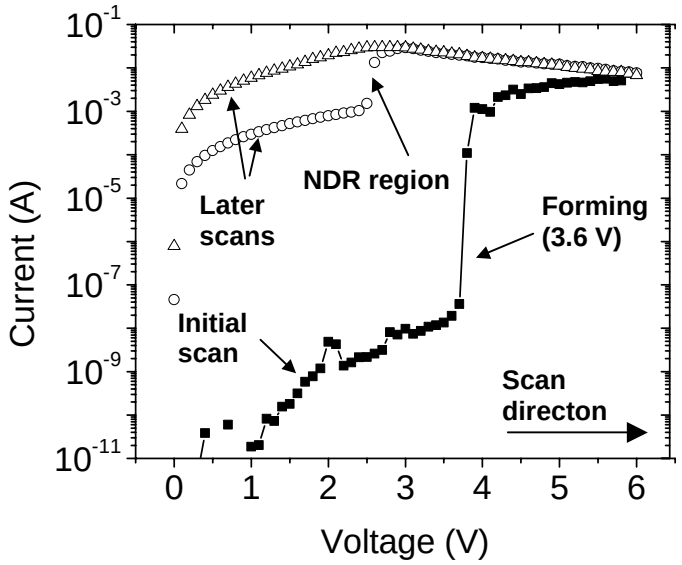


Figure 7.3. Several scans on a 7-layer MUA device in the edge structure. The device is initially insulating, but after increasing the voltage above 3.7 V, the device is formed and its conductivity increases by ~10^5. Later scan reveals a much larger conductance, NDR, and programmable low-voltage conductivity (in this example we show two scans in which the device's low-voltage conductance is 2 x 10^{-4} S or 6 x 10^{-3} S at 1 V. The voltage was scanned at 2 V/s.

very high conductance state (10^7 S/cm^2 at 1 V) that could not be programmed- we refer to this as breakdown, and the device as shorted (Fig. 7.2(a)). The second possibility is that after the voltage sweep the device could have a high conductance (ranging between 10 to 10^6 S/cm^2 at 1 V) that was programmable (Fig. 7.3). For reasons that will become apparent in Chapter 8, we call these programmable-conductance devices "formed" devices, the transition to the programmable, high-conductance phase forming, and the voltage at which it occurs the forming voltage. The forming process (Fig. 7.3) was often indistinguishable from the conventional breakdown process that resulted in a shorted device (Fig. 7.2(a)). In both of the initial voltage sweeps, a large, sudden increase in current is observed (at 2.9 V in Fig. 7.2(a), and 3.6 V in Fig. 7.3), so that the forming and breakdown processes could only be distinguished by measuring the subsequent device characteristics.

After further investigation, we found that there was considerable variation in the conditions under which devices could enter the formed state. On some edge devices, by applying a large current (>10^6 A/cm^2) to an initially shorted device we could reduce

its conductance and cause it to enter a programmable state. In other instances, edge devices that were not shorted but had relatively large currents (~10^3 A/cm^2 at 1 V) were programmable even without the application of a forming voltage. However, the most commonly used approach (and the most consistent one) was to apply a forming voltage to a device that was initially insulating (for further details on the approaches that we used to form devices, please refer to Appendix B).

When forming an initially insulating device, the dependence of the forming voltage on MUA thickness and device structure was identical to trends observed for the breakdown voltage, so we show both of these voltages in Fig. 7.2(b) without distinguishing between them. In any batch of identically prepared devices, large-range (0-8 V) voltage sweeps could result in both shorted and formed devices. However, the undesired breakdown process that led to shorted devices occurred most frequently in devices with a large area or a small number (< 6) of MUA layers. Devices with small areas and larger numbers of MUA layers were more likely to be formed then shorted. Due to the relatively low yields of insulating devices for samples with 2 to 6 MUA layers, and the increased likelihood of these devices to short when we attempted to form them, we focused primarily on devices with more than 6 MUA layers. We also note that the forming process did not depend on the voltage polarity, so devices could be formed with either positive or negative bias.

In future sections, we discuss the characteristics of devices after forming. Unless explicitly stated otherwise, all devices that we consider have already been formed

7.4 Pulsed Voltage Measurements

We found that formed devices could be programmed into different conductance states by applying voltage pulses, as illustrated in Figure 7.4. Here the device is initially in a low-conductance state (which we define arbitrarily as OFF) with a current of ~10 μA at 1 V (Fig. 7.4(a)). This OFF state still has a conductance that is often more than 10^4 higher than the pre-formed, insulating device, as is clear from examining the post-formed scans in Fig. 7.3. Next, a 4-V, 10 ms voltage pulse is applied to the device to program it into a high-conductance state (which we define as ON) (Fig. 7.4(b)). The current in this state is ~10 mA at 1 V, a factor of 10^3 larger than before. Finally, a 10 V, 10 ms pulse returns the device to its original OFF state (Fig. 7.4(c)).

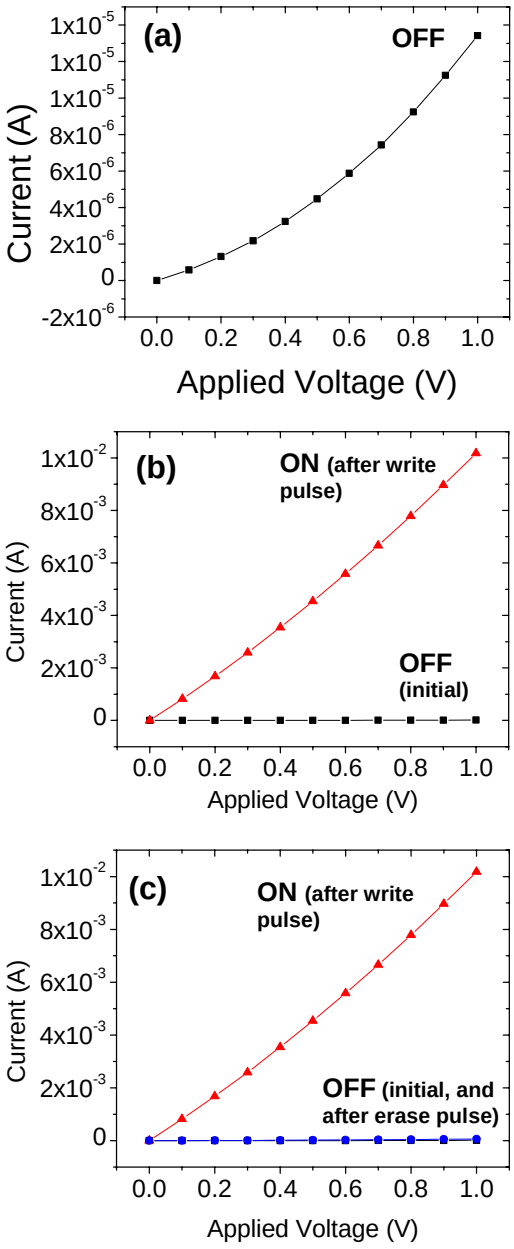


Figure 7.4. Low-resistance (~10^{-5} Ω cm^2) (ON) and high-resistance (10^{-2} Ω cm^2) (OFF) states of a device. (a) The device was initially OFF. (b) A 4-V, 10-ms pulse wrote the device ON. (c) A 10-V, 10-ms pulse erased the device OFF.

The 10 mA current at 1 V in the ON state corresponds to an enormous conductance/area of 10^5 S/cm^2 (or ON resistance of 10^{-5} Ω cm^2), which was common for edge devices (conductances as high as 10^6 S/cm^2 were observed). Although planar devices had qualitatively similar characteristics, they typically had smaller conductance/area (by 10^2 to 10^4). As we discuss further in Section 7.6, this could be because the active area of the planar devices is much less than the apparent area that we used in calculating conductance/area. Programming depended only on the magnitude of the voltage pulse (and not its polarity), so that devices could be programmed with either positive or negative voltage pulses.

A typical programming/read sequence using only voltage pulses is shown in Figure 7.5. Initially, the device is in the OFF state so that the 1-V, 7-ms "read" pulse causes a current in the μA range. Next, a 4-V write pulse is applied. The subsequent read pulse measures a current of 100 μA (corresponding to a current density of 2 x 10^4 A/cm^2) in the ON state, 100x higher than the OFF state. A 10-V erase pulse then returns the device to the OFF state that is read by the final 1-V pulse. Using a similar sequence of voltage pulses to those shown in Figure 7.5, devices endured over 10^4 write/erase cycles, maintaining very high current densities (10^5 A/cm^2 at 1 V in the ON state) without failing (Fig. 7.6).

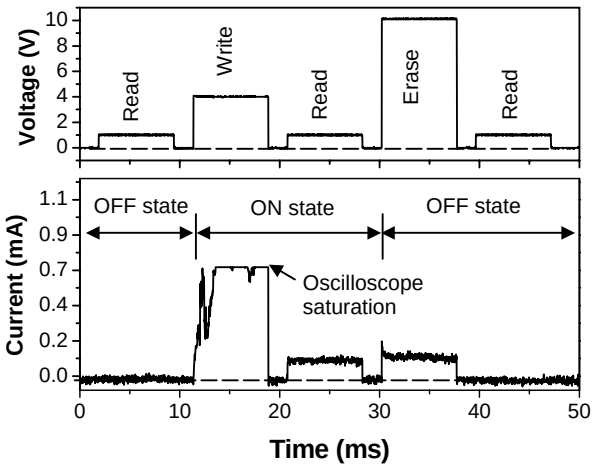


Figure 7.5. Typical programming sequence for 11-nm MUA film in edge structure where applied voltage pulses to program the device ON or OFF (4 or 10 V for write or erase operations, respectively) are alternated with 1 V pulses to read the state of the device. The current during the write pulse (actually ~1.2 mA) exceeds the measurement range of the oscilloscope and is cut off. From Ref. [1].

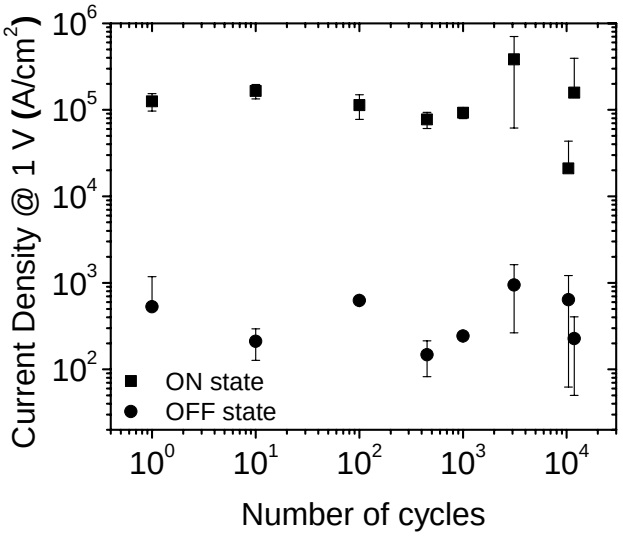


Figure 7.6. Evolution of the current density (measured at 1 V) of ON and OFF memory states following multiple write/erase cycles. The device consists of a 7 MUA layer film in the edge structure. The write pulse was 4 V, 8 ms, and the erase pulse was 10 V, 1.5 ms. Error bars represent variations in current density measured in four consecutive write/erase cycles. From Ref. [1].

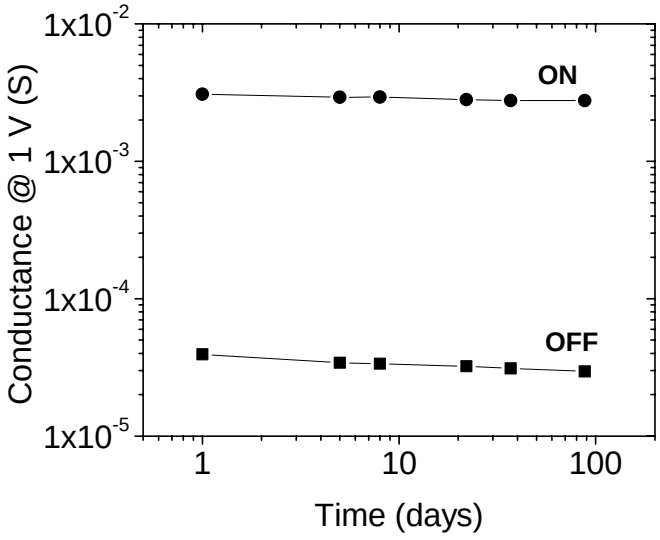


Figure 7.7. Evolution vs time of the conductance of the ON and OFF states of 6-MUA layer edge devices stored in an inert atmosphere.

Programmed states were generally stable (without applied voltage) for many months (Fig. 7.7). When kept in an inert atmosphere (<1 ppm water and oxygen in a nitrogen glove box) both ON and OFF states decayed slightly, to 90% and 75% of their initial conductance, after 88 days. Due to the large difference in conductivities (100x in this case), they remained easily distinguishable.

To determine the relationship between pulse voltage and programmed conductance, a series of increasing or decreasing voltage pulses was applied to a device that was initially in its OFF state. After each voltage pulse, the device conductance was measured at 1 V (Fig. 7.8). For increasing voltage pulses starting at 1 V, no change in device conductance was measured until a 2.5 V pulse was applied, after which the conductance increased rapidly to its maximum value near 4 V. As higher voltage pulses were applied, the conductance then decreased, reaching its lowest value near 9 V. If a sequence of decreasing-voltage pulses was applied (starting at 9 V), a similar trend of increasing conductance was observed, until 2.5 V, after which the device no longer changed conductance. It is clear from Figure 7.8 that the device is not bistable but instead its conductance can be programmed over a range of ~10^3. We therefore arbitrarily take the geometric average of the highest and lowest

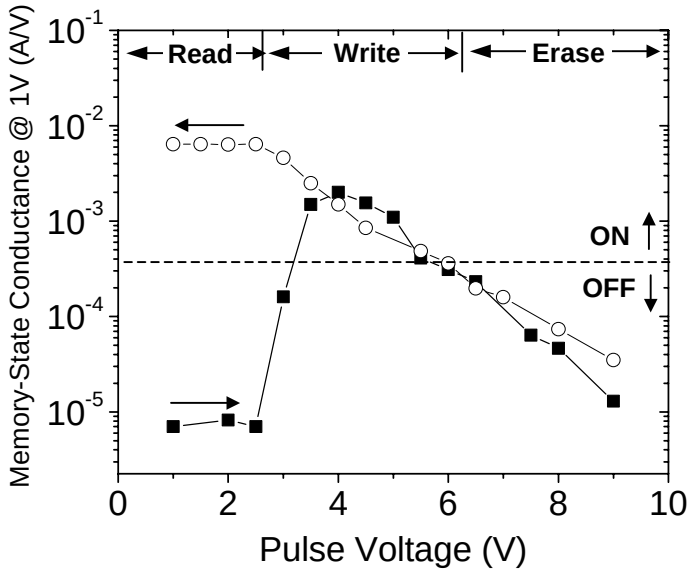


Figure 7.8. Dependence of programmed conductance on pulse voltage. Increasing (solid squares) and decreasing (hollow circles) sequences of 1-ms voltage pulses were applied to a 6 layer edge device initially in OFF state. After each voltage pulse, the resulting conductance at 1 V was measured.

conductance states, and define anything above this as ON and below as OFF. Thus we can think of the device as a digital (binary) storage device, although in practice it can be programmed over a continuous range of states. Pulse voltages in the range of 2.5 V to 6 V thus write the device ON, while voltages > 6 V erase the device. Voltages below 2.5 V have no effect on the conductance so can be used to read the device nondestructively. Similar voltage ranges for writing, erasing, and reading were observed for all devices, regardless of the MUA thickness.

7.5 Current-Voltage Scans and Negative Differential Resistance

Low-speed voltage scans of formed devices revealed symmetric negative differential resistance (NDR) with very large peak current densities (up to almost 10^7 A/cm^2 for edge devices) (Fig. 7.9). Characteristics for both planar and edge structures were qualitatively similar, the main difference being that edge structure devices typically had much higher current densities (by a factor of 10^2 to 10^4). Large peak-to-valley ratios (PVRs) of up to 140:1 were observed, although ratios of ~10:1 were more common. The position of the peak current varied slightly, between 2 to 4 V, for different devices; however, this position did not depend on the thickness of the MUA film. The peak current also varied, by a factor of up to 10, for repeated scans on the

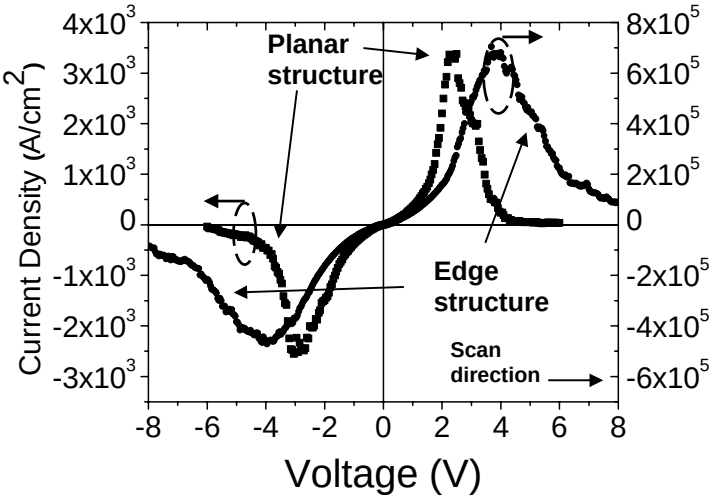


Figure 7.9. Current-density vs voltage (with applied voltage) of 11-nm MUA films in planar (left vertical axis) and edge structures (right vertical axis). The voltage was scanned from negative to positive at 2 V/s. From Ref. [1].

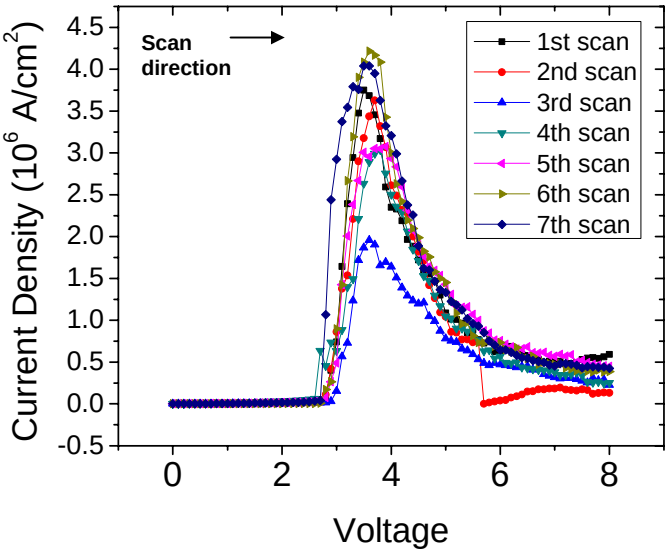


Figure 7.10. Current density vs applied voltage for repeated 2V/s scans on edge-structure device with 8 MUA layers.

same device (Fig. 7.10). However, electrical characteristics were repeatable (apart from some variation in the peak current) when the voltage was kept below 10 V. Voltages above 10 V generally placed the device into a permanent low-conductance or high-conductance (shorted) state that no longer displayed NDR.

The most studied family of devices in which NDR is observed consists of tunneling diodes. In these devices the NDR characteristics are due to enhanced charge tunneling through a barrier when energy levels adjacent to the barrier are aligned by a bias voltage (without storage of a nonvolatile state). This mechanism is unlikely to be responsible for the NDR characteristics we observe, because if the voltage was scanned at rates higher than ~10V/s, the NDR was replaced by insulating characteristics (Fig. 7.11). If the NDR were due to a tunneling through an aligned energy level, it should be observed independent of scan speed (except for capacitance limitations).

The NDR in our devices instead reflects a dynamic programming of the device into the high-conductance state at voltages near the peak current, followed by programming into the low-conductance state at higher voltages. The relationship between the NDR and programming is apparent if a current-voltage scan is compared

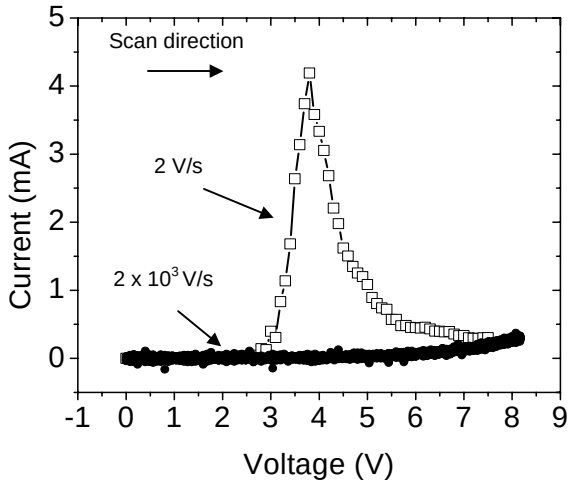


Figure 7.11. Current vs applied voltage for scan speeds of 2 V/s (hollow squares) and 2 x 10^3 V/s (solid squares) on planar device with 8 MUA layers.

to the dependence of the device conductance on programming voltage (Fig. 7.12). The conductance of the programmed state, measured by applying 1-ms voltage pulses to an initially OFF device and measuring the resulting conductance at 1 V, remains low until after a voltage greater than 2.5 V is applied, then rises rapidly to a peak near 3 V

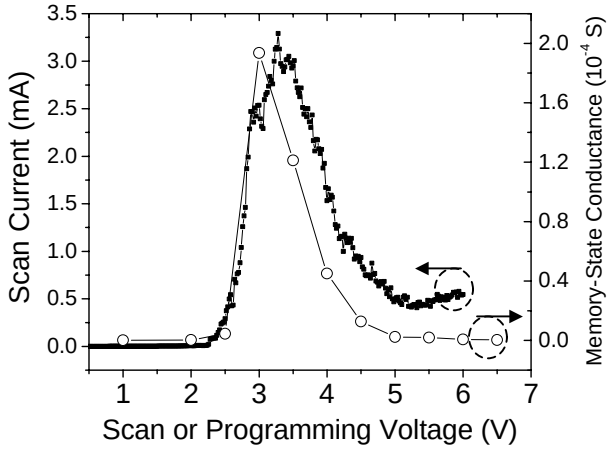


Figure 7.12. Comparison of a current-voltage scan to the conductance of memory state (at 1 V) vs programming voltage. During the current-voltage scan, the voltage was swept at 2V/s; for programming, 1-ms voltage pulses were used to program an initially OFF device and the resulting conductance was measured at 1 V. The device was planar with 8 MUA layers.

and then returns to its original (low) value at higher voltages. This characteristic traces out a curve that almost exactly overlays the NDR in a current-voltage scan of the same device.

Dynamic programming of the device also leads to repeatable hysteresis during current-voltage scans (Fig. 7.13). Starting with a (post-formed) device that was OFF, the voltage was scanned from 0 to 6.5 V, then returned to 0 V. Because the device is initially OFF, during the initial 0 to 6.5 V scan, low currents (<10^3 A/cm^2) are obtained until the NDR region is reached at 2.5 V. However, during the 6.5 to 0 V scan, the device is programmed into the ON state at 3 V and then left in this state as the voltage decreases to 0 V, resulting in much larger currents of up to 5 x 10^5 A/cm^2 in the 0 to 2.5 V region. Because the device was programmed ON by the 6.5 to 0 V scan, the subsequent voltage scan retraced this high-current characteristic. The device could be returned to the low current (OFF) characteristic by scanning from 0 to 6.5 V, then rapidly reducing the applied voltage to 0 V (in less than ~10^{-3} s). Indeed, it was the low-frequency NDR characteristics that we first observed in these devices, and investigation of these characteristics led to our discovery of the resistance programming.

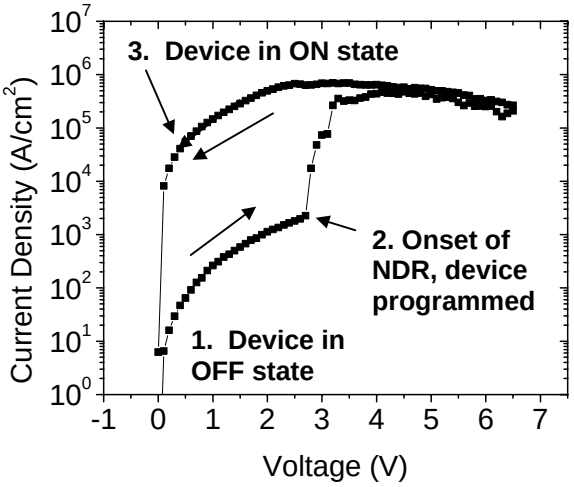


Figure 7.13. Hysteresis in current-voltage scan of edge-structure device with 7 MUA layers. The device was formed and then programmed OFF. Next, the voltage was scanned from 0 to 6.5 V. At ~2.5 V, we observe NDR and begin to program the device. Finally, the voltage is returned from 6.5 to 0 V; the device is programmed ON as the voltage is swept through 3 V then left ON as voltage is returned to 0 V.

7.6 Device Appearance after Forming

The application of forming voltages to (and subsequent electrical testing of) devices frequently caused a change in their appearance. In planar devices, this change was visible in a microscope image (Fig. 7.14), and suggested a roughening of the electrode. SEM images confirmed that significant changes had occurred. After forming and prolonged electrical testing, the top gold electrode was significantly damaged, and in some cases was no longer continuous (Fig. 7.15(a) and (b)). For comparison, magnified images of the top electrode of a pristine device suggest that it may contain small gaps but is otherwise continuous (Fig. 7.15(c) and (d)). AFM measurements on the top electrode of formed devices found height variations of 50 nm (for a 30 nm thick electrode on top of a 10 nm MUA layer), much larger than the ~5 nm variations of a pristine top electrode.

The degree of roughness and damage to the electrode typically depended on the number of electrical measurements done on the device, and the size of the current during these measurements. In planar devices where the voltage was scanned only a few times and low currents were measured, electrode damage was minimal and only

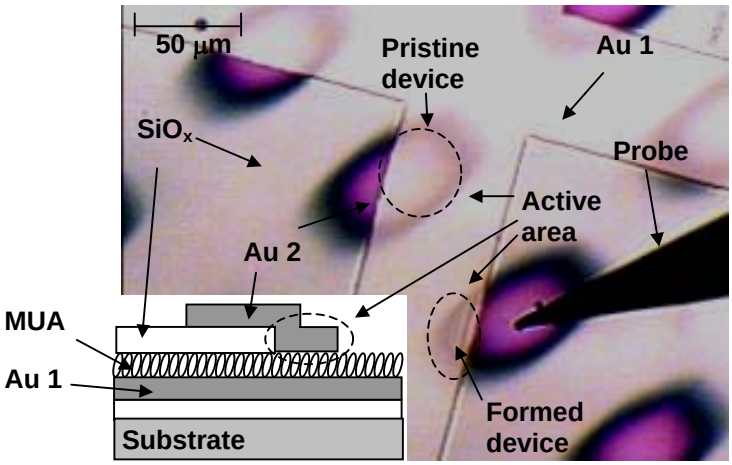


Figure 7.14. Microscope image of formed and pristine 8-MUA layer planar (PoPI) devices, with schematic of device cross-section (inset). The visible portions of larger squares are SiO_x layers. The light regions between these squares are the top gold layer (covered by the transparent MUA film), and the small purple ovals are the top gold electrodes. These electrodes were deposited at an angle with respect to the SiO_x layer to create devices with a variety of overlap areas. The active area of a formed device is visibly rough in comparison with a pristine device.

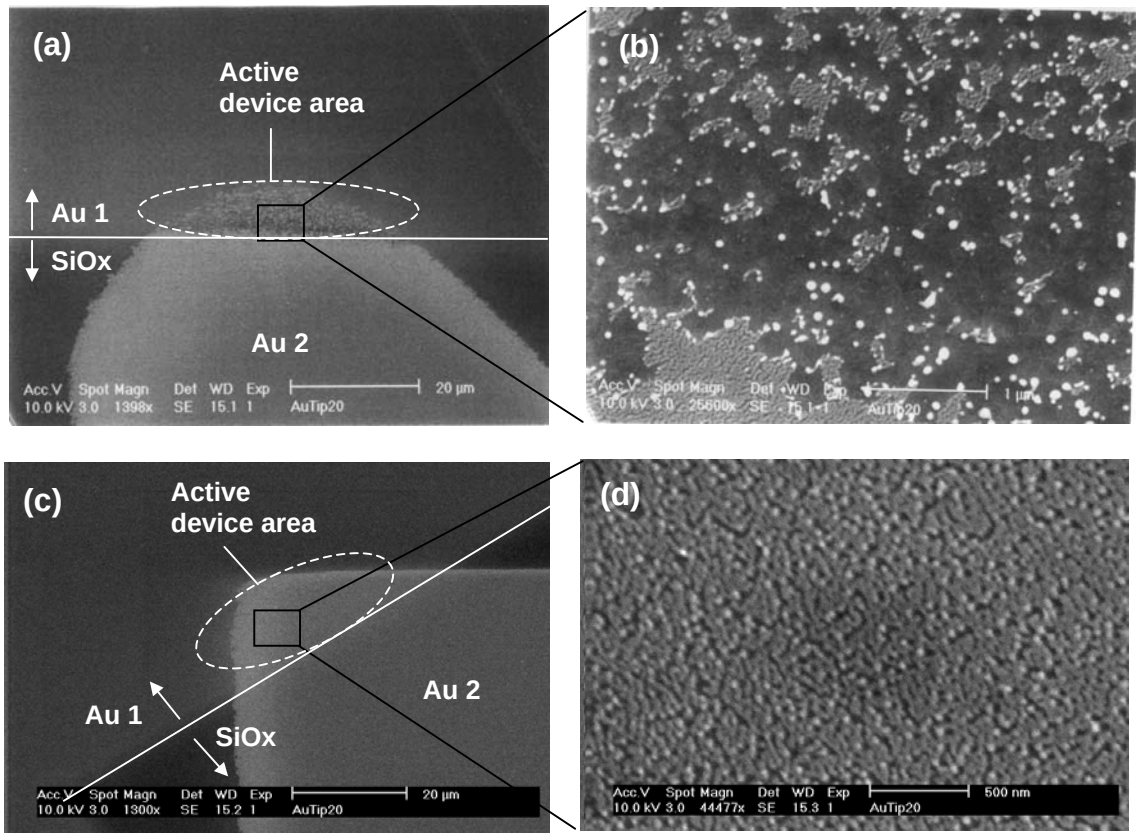


Figure 7.15. SEM images of planar (PoPI) devices with 8 MUA layers. In the large-area images ((a) and (c)), the light Au 1 region is separated from the dark SiOx region by a white line. The second gold layer is the lightest region in the SEM; the active device area is where it overlaps the Au 1 layer. (a) Large-area view of device after forming and electrical testing. (b) Close view of formed device showing that the top electrode is no longer continuous. (c) Large-area view of pristine device. (d) Close view of pristine device. The dark regions may indicate small gaps in the electrode, but it is otherwise continuous.

visible in the SEM at high magnifications (however, we always observed some damage after devices had been formed, regardless of how little testing was done). Electrode roughening in edge devices was less common, and only visible in the SEM after relatively lengthy electrical testing (~20+ current-voltage scans).

It is very likely that this increased roughening in the top electrode of planar devices is what led to their reduced current densities with respect to edge devices (by a factor of 10^2 to 10^4). The roughness (and gaps) in the electrodes of planar devices led to a decreased effective device area of these devices, and therefore lower current densities when the apparent electrode area (before forming) was used to estimate the

device area. Indeed, in some planar devices the initial measurements after forming revealed current densities that approached those of edge devices; however the current tended to decrease to much lower values after several scans as the top electrode became visibly roughened. Despite this roughened appearance, devices could still endure over 10^4 write/erase cycles without failing.

7.7 Summary

We have reported the characteristics of two-terminal programmable-resistance memory devices based on MUA films. Devices displayed nonvolatile, programmable conductance switching and NDR with extremely high current densities (up to 10^7 A/cm^2). In addition to low ON resistance (to allow fast read times in large memory arrays), we observed a number of other promising characteristics, including low programming voltages (<10 V), long data storage times (> 3 months with no applied power), durability (>10^4 write/erase cycles), and unipolar operation (to allow integration with diodes for operation in a passive-matrix memory array).

These characteristics, especially the low ON resistance, are uniquely promising among organic memory technologies for application in high speed and density memory arrays. In the next chapter, we discuss the physical mechanism responsible for the characteristics observed in this chapter, and also show that devices can be programmed very quickly (~100 ns).

References

[1] T. Graves-Abe and J. C. Sturm, "Programmable Organic Thin-Film Devices with Extremely High Current Densities" *Applied Physics Letters* **87**, 133502 (2005).

[2] R. Haag, M. A. Rampi, R. E. Holmlin and G. M. Whitesides, "Electrical Breakdown of Aliphatic and Aromatic Self-Assembled Monolayers Used as Nanometer-Thick Organic Dielectrics" *Journal of the American Chemical Society* **121** (34), 7895-7906 (1999).

[3] J. K. N. Mbindyo, T. E. Mallouk, J. B. Mattzela, I. Kratochvilova, B. Razavi, T. N. Jackson and T. S. Mayer, "Template Synthesis of Metal Nanowires Containing Monolayer Molecular Junctions" *Journal of the American Chemical Society* **124** (15), 4020-4026 (2002).

Chapter 8

Molecular-scale Nonvolatile Memory Device: Physical Mechanisms

8.1 Introduction

In this chapter we consider several possible mechanisms to explain the programmable resistance and other electrical characteristics of the MUA -based devices reported in Chapter 7. We will show that a mechanism based on the formation and destruction of conducting paths (consisting of metal injected from the electrodes into the MUA film) best explains these observed characteristics. As we study the physical mechanism, we will also report the programming times of MUA devices, which we found could be written and erased very quickly (100 ns).

This chapter is organized as follows. In Section 8.2, we describe device preparation and experimental setup. In Section 8.3, we distinguish between several possible mechanisms for the observed behavior, and show that the programmable conductance is due to the formation and destruction of conducting paths in our device. We then study the device characteristics and this conducting-path mechanism in more detail in Sections 8.4 through 8.7, and summarize the chapter in Section 8.8.

8.2 Device Preparation and Experimental Setup*

MUA device fabrication and characterization followed the procedures described in Section 7.2. Almost all devices used gold for both electrodes, although in some cases aluminum was used for the top electrode. As in Chapter 4, an MMR Technologies LTMP-4 variable-temperature probe station was used for variable-temperature measurements.

In some experiments, the MUA layer was replaced by the hole-transporting polymer poly(9-vinlycarbazole) (PVK) (M_w ca. 1,100,000 g/mole, obtained from Aldrich). 65-nm films of PVK were deposited by spin-casting at 1.9 kRPM from a solution of 90 mg PVK in 7.5 mL of chlorobenzene. 30-nm films of PVK were

* For additional experimental details, please refer to Appendix B.

deposited by spin-casting at 4 kRPM from a solution of 90 mg PVK in 7.5 mL of chlorobenzene. 16-nm films of PVK were deposited by spin-casting at 4 kRPM from a solution of 45 mg PVK in 7.5 mL of chlorobenzene. These PVK devices utilized a PoPI structure, and all other fabrication conditions were identical to MUA devices.

8.3 Determination of the Mechanism for Programmable Conductance and NDR

The electrical characteristics described in Chapter 7 most closely resemble those of a class of devices typically referred to as electroformed metal-insulator-metal (MIM) devices. Work on these devices, which began in the 1960's, has focused mostly on inorganic insulating films, such as Al_2O_3 and SiO_x, although more recently some results on organic films have been reported [2-16]. After the application of a forming voltage (generally ranging between 5 to 20 V), these insulating films become more conducting and displayed programmable conductance and NDR, in many cases similar to what is observed in our devices [3]. Increased roughness (and gaps) in the top electrode are also often observed. In most previous work, the NDR characteristics were the main interest, rather than the programmable conductance that is our primary focus.

We note that although SiO_x was often used as the active layer in previous work, the electrical characteristics of our devices are due to the MUA film and not the SiO_x layer present in the edge and planar PoPI devices. There are two reasons for this. First, we can observe similar characteristics in devices (such as the planar PrPM structure) that do not have an SiO_x layer. Second, whenever samples were prepared with an SiO_x layer, we also measured control devices (fabricated on the same wafer) in which the top electrode pattern was changed to contact only above the SiOx layer. Most of the time these control devices displayed only insulating characteristics (with negligible current) for voltages well above the range used to test MUA devices. In several instances, some NDR was observed in the SiO_x film. In these cases the wafer was discarded. It is likely that the occasional variations in electrical characteristics of the SiO_x layer were due to the sensitivity of e-beam-deposited SiO_x to the conditions during its evaporation.

Most authors have attributed NDR (and programmable conductance) in electroformed devices to one of two models. In the first model, conducting paths (e.g.

paths consisting of metal from the electrodes) are formed in the film at voltages between 3-5 V, causing the device to enter its high-conductivity state; these paths are destroyed by joule heating at higher voltages, leading to the low-conductivity state [4, 5, 13, 17]. In the second model, charges trapped within the film tend to be released at voltages between 3-5 V, resulting in higher-conductances; at higher voltages charges are more likely to be trapped, causing an electric field that suppresses current [2, 7]. It is believed that these charges are trapped on metal atoms or clusters that have been embedded in the film during fabrication, or diffuse into the film from the metal electrodes during the initial forming step [16]. We will later refer to these as the "conducting-path" and "charge-trapping" models, respectively.

Our fabrication process also leads to embedded metal atoms, in the form of the Cu layers that form linkages between MUA molecules. To investigate the possibility that the programmable conductance was due to movement of the Cu (as in the first model) or charge being trapped on these atoms (as in the second model), we conducted two experiments. In the first, we fabricated MUA devices in which the top Au electrode was replaced by Al. For positive bias on the bottom gold electrode, these devices could be formed and displayed characteristics that were similar to devices with two gold electrodes. However, devices could not be formed if positive bias was applied to the aluminum electrode, regardless of the applied voltage. We also found that the electrical characteristics of devices that had been formed (by applying positive bias to the gold electrode) were no longer symmetric (Fig. 8.1). For positive bias on the gold electrode, regular NDR characteristics were observed. When voltage was applied to the Al electrode, on the first scan greatly diminished NDR (by a factor of 10x) was observed. If we continued to scan the voltage on the aluminum electrode, this NDR peak decreased rapidly and disappeared after several scans. Similarly, devices could be programmed into ON and OFF states with positive voltage pulses on the Au electrode, but could only be programmed OFF when voltage was applied to the Al electrode.

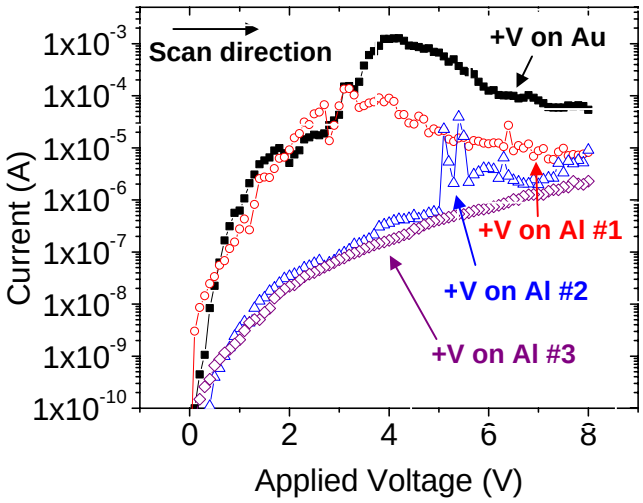


Figure 8.1. Current-voltage scans of a formed 11-layer planar device with an Al (40 nm) top electrode. For positive bias applied to the bottom gold electrode, regular NDR characteristics are observed. For positive bias on the Al electrode, the first scan reveals an NDR characteristic that is 10x smaller than for bias on the gold electrode. The NDR characteristic is smaller still in the second scan, and disappears completely in the third.

In the second experiment, we used two gold electrodes but replaced the MUA with a layer of the polymer PVK (using the planar PoPI structure). In these devices, when the polymer layer was 65 nm thick, the characteristics of all devices remained insulating for applied voltages up to 25 V. When the thickness of the PVK layer was reduced to 16 nm, after scanning the voltage to 10 V, on subsequent current-voltage scans we observed NDR characteristics that were comparable to MUA devices (although they were much less repeatable) (Fig. 8.2).

The hypothesis that the Cu atoms are responsible for the NDR and programmable conductance is not compatible with these observations. If this were the case, NDR and programming would still be observed when MUA was contacted by an Al electrode, and would not be observed when the MUA was replaced by PVK. (We can also rule out another possible mechanism, that the NDR is due to a phase change in the MUA, for similar reasons). These measurements instead reveal that the gold electrodes, common to the NDR observed in both experiments, play a critical role. More specifically, these results strongly suggest that when a positive bias is applied to the gold electrode during the forming step, this causes positive gold ions (or positively

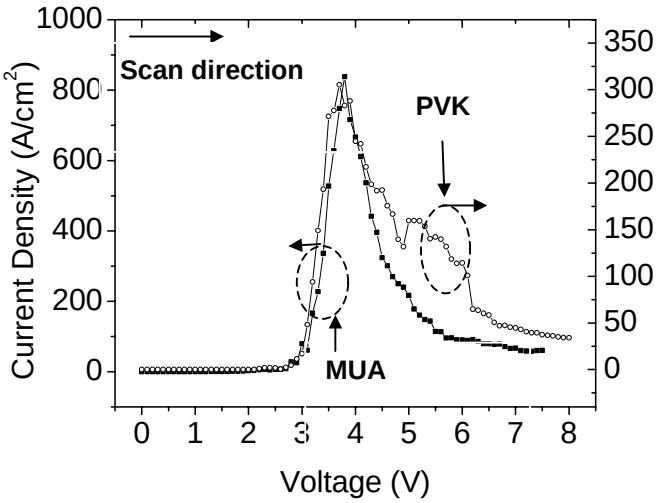


Figure 8.2. Comparison of current-voltage scans on planar devices in which the organic layer was 8 layers of MUA (12 nm) or spin-cast PVK (16 nm).

charged gold clusters) to be injected into the organic film. It is this injected gold that is then responsible for the electrical characteristics of the formed device. This injected gold might move through the film to form conducting paths as in the first model, or serve as a charge trapping location in the second model.

Fortunately, the measurements on the device with an Al top electrode can also distinguish between these two possibilities, and indicate that charge-trapping on gold injected into the film (leading to the NDR and programmable conductance) is unlikely. If this were the case, after forming the device by applying positive bias to the gold electrode to inject gold into the film, we should be able to observe NDR for positive bias on either electrode (although the exact voltage at which it occurs could differ due to the different Au and Al work functions). Instead, as we apply voltage to the Al electrode, we observe a diminished NDR characteristic that disappears after several scans. This behavior is much more consistent with a model in which conducting paths (based on injected gold) are formed for voltages between 3 to 5 V (then destroyed at higher voltages) for positive bias on the gold electrode. When bias is applied to the Al electrode, no Al is injected (we discuss why this is the case in Section 8.5.2), so the NDR is much lower and is due only to residual gold that is removed from the film after several voltage sweeps.

The long-term retention of the states (>3 months) (Fig. 7.7) is also incompatible with charge storage in thin films. Trapped charge can be stored for many years in high-quality SiO_2 (as is the case for flash memories). However, the relatively large current densities observed in these films even in the OFF state (10^{-1} to 10^{2} A/cm^2 at 1 V, compared to less than 10^{-12} A/cm^2 for a 10-nm film of SiO_2) reveal that the MUA film is a much poorer insulator, with many pathways that would allow trapped charge to leak out of the films relatively quickly [18].

In later sections we will also show that the current during a write operation increases in step-like jumps that suggest the formation of individual conducting paths, lending further experimental support to the conducting-path model. In addition to these experimental inconsistencies, several other features of the charge-trapping model are not satisfactory. First, we have shown that any charge trapping must occur on gold that has moved into the film during application of the forming voltage (> 6 V). It is not clear why this gold would then remain immobile to serve as a charge-trapping center in later operation, during which we often apply even greater voltages of up to 10 V. Second, we are not aware of any discussion of the charge-trapping model that proposes a satisfactory mechanism to explain how charge would be trapped at high voltages to lead to the OFF state, then released at lower voltages to turn the device ON. Because of these inconsistencies, we discard the trapped-charge model, and examine the conducting-path model in more detail, and show that this model satisfactorily explains most of the observed device characteristics.

8.4 Overview of the Conducting-Path Model

Experimental observations of conductance switching in insulating films have often been explained by a model based on the growth and destruction of conducting paths. Although a number of variations of this model exist [4, 6, 13, 19], most use the framework established to describe electroformed films by Dearnaley et al in 1970 [5, 17]. Qualitatively, application of a medium-range voltage (3 to 5 V in our work) to a device that is initially OFF (Fig. 8.3(a)) causes the formation of conducting paths in the film (Fig. 8.3(b)) and places the device in the ON state (Fig. 8.3(c)). To return to the OFF state, a larger voltage (>5 V in our work) is applied, which leads to the rupture of these paths due to joule heating (Fig. 8.3(d)).

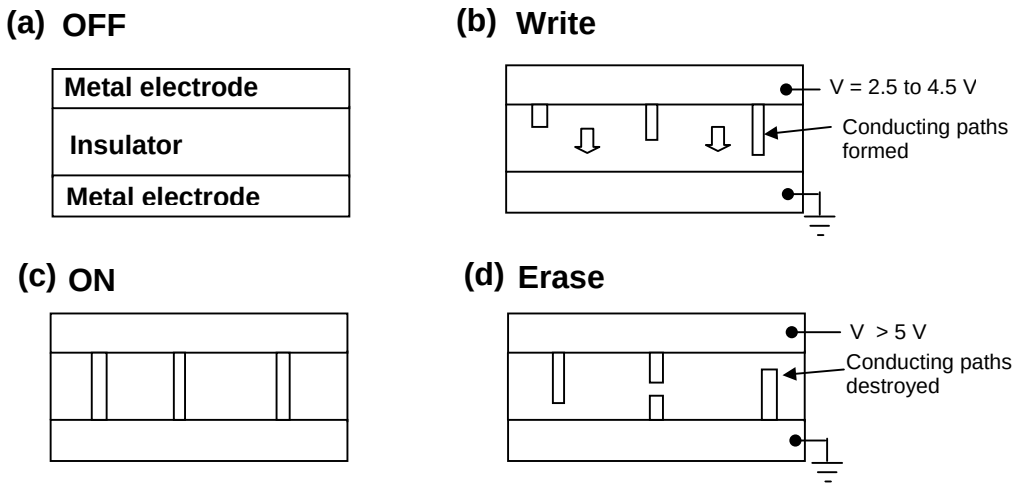


Figure 8.3. Schematic of conducting-path model. (a) Device begins OFF. (b) Write voltage (2.5 to 4.5 V) causes the voltage-assisted formation of conducting paths in insulating film. (c) Device in ON state is characterized by conducting paths in insulating film. (d) Erase voltage (> 5 V) ruptures conducting paths with joule heating, leading to OFF state

As originally conceived, the conducting path model of Dearnaley et al is concerned primarily with the NDR characteristics observed in low-frequency current-voltage scans. We consider the model in this quasi-equilibrium context first, and in later sections discuss its extension to non-equilibrium (pulsed) measurements in which the state of the device varies rapidly with time. In Dearnaley's model, the exact mechanism for the formation of the paths is left unspecified other than to state that conducting paths are formed for voltages above a (loosely-defined) threshold voltage. This threshold voltage corresponds to the onset of programming (~2.5 V in our devices, Fig. 7.13), so that (neglecting joule-heating) if the voltage is above this threshold, the device will contain a distribution of paths with different resistances (Fig. 8.4(a)). The exact shape of the distribution can be determined by fitting to measured characteristics. To first order, the paths can be treated as parallel resistors, so that the current in the device is given by

$$I = V\sum \frac{1}{R_p} \tag{1}$$

where R_p is the resistance of an individual path.

As the voltage is increased, joule-heating causes some of these paths to rupture. We are interested in quantifying which of these paths are ruptured. Without

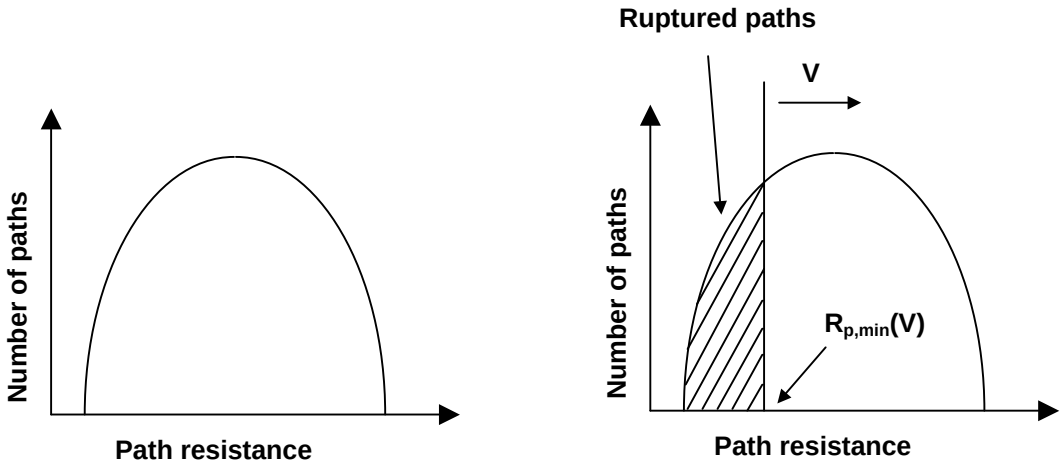


Figure 8.4. (a) Population of paths in device held slightly above threshold voltage. (b) Increasing the voltage causes paths with a resistance below $R_{p,min}(V)$ to rupture.

rigorously defining a coordinate system, the temperature T ($= T(\vec{x},t)$), a function of three-dimensional position and time) in the conducting path and surrounding region is given by the heat diffusion equation:

$$\partial T \big/ \partial t = \frac{Q}{C\rho} + \frac{1}{C\rho}\nabla(k(\nabla T)) \tag{2}$$

where Q is the heat production per unit volume (and so is proportional to V^2), C is the specific heat, ρ is the density, and k is the thermal conductivity (all of which can also vary as a function of position) [20]. At steady state,

$$Q = -\nabla(k(\nabla T)). \tag{3}$$

The solution of equation (3) will depend on the exact geometry of the conducting path and surrounding insulator. Solutions for several geometries have been provided by R. D. Gould [21], who reports them in the form

$$T_{path} = T_0 + \alpha \frac{V^2}{R_p}, \tag{4}$$

where T_{path} is the maximum temperature in the path, T_0 the ambient temperature, and α is a constant that depends on material constants and the geometry of the path and surrounding insulator. This equation simply states that the temperature of the path is equal to the ambient temperature plus some term proportional to the joule-heating in the path (so that the detailed physics is hidden in the proportionality constant α).

Assuming some maximum temperature $T_{path,max}$ that the path can withstand before rupture and solving equation (4), we find that any paths with resistance less than

$$R_{p,\min}(V) = \frac{\alpha V^2}{T_{path,\max} - T_0} \tag{5}$$

will rupture.

If we assume that the distribution of conducting paths remains constant above the threshold voltage, then as the voltage is increased the current is primarily determined by how many of these paths rupture, as illustrated in Figure 8.4(b). As more paths rupture, at some voltage the overall current decreases, resulting in the observed NDR. In reality, it is probable that the overall distribution of conducting paths will also change as the voltage is increased (i.e. more paths may be created), so that the overall process is more complicated than in Figure 8.4(b), although the basic trends remain similar. This model also easily accounts for storage of different conductivity states. If a (large) voltage sufficient to rupture most of the paths is applied to the device then removed abruptly, this leaves very few paths in the device, resulting in the OFF state. Application of smaller voltages (near the onset of NDR) creates conducting paths without causing many to rupture, leading to the ON state.

Although the model of Dearnaley et al presents a physical mechanism for how paths rupture, it does not address how they are formed, or their composition In the next sections, we consider the composition of these conducting paths, then study how they are formed before finally discussing in more detail how they are destroyed.

8.5 Composition of and Conduction in the Conducting Paths

In this section we discuss the nature of the conducting paths in our devices. For most formed devices to which the conducting-path model has been applied, the composition of the material in the conducting path remains a subject of some controversy [4-6, 13, 17]. Because qualitatively similar effects have been observed in a variety of different insulating materials but often using electrodes based on noble metals (such as Au or Ag), it is tempting to conclude that the paths are metallic filaments that extend from the electrodes [22, 23]. Alternatively, these conducting paths may consist of other materials, such as carbonaceous filaments [6]. It is also possible that the paths consist of a mixture of several phases (i.e. hopping pathways due to discrete metallic clusters in the insulator) [5, 21]. In our devices, we rule out the

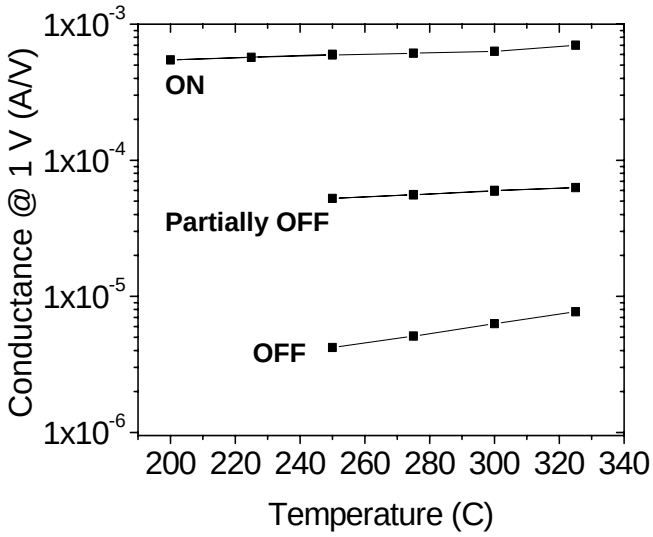


Figure 8.5. Conductance (at 1 V) of memory states in edge device (11 nm MUA) as a function of temperature. The device was programmed with pulses with amplitudes of 3.5 V (leading to the ON state, top trace in figure), 6 V (leading to the partially OFF state, middle trace), and 10 V (OFF, bottom trace).

formation of carbonaceous filaments, as this mechanism would not be expected to lead to the asymmetry that we observed when we replaced a gold electrode with aluminum. We will instead show that it is more likely that the conducting paths consist of metallic clusters embedded in the MUA film.

We first consider temperature-dependent measurements of the conductance of the memory states. All memory states were observed to decrease in conductivity as the sample temperature was lowered (Fig. 8.5). A decrease in conductance with decreasing temperature for the OFF state is expected: in an insulating device, the current is generally due to charge carriers that are thermally excited over transport barriers. The similar increase in conductance for the ON state is more informative, as it indicates that the conducting paths are not metallic filaments. In metals, conduction decreases with increased temperature because scattering of the free carriers with lattice phonons becomes more likely [24]. (For nanoscale conducting filaments, scattering along walls of the filament can sometimes dominate lattice scattering so that the conductance does not depend on temperature [25]; however for the case of gold filaments this only occurs at very low temperatures less than 100 K, below the range we studied [26]).

Even though the conductance of the ON state increases with temperature, its dependence on temperature is smaller than for the higher resistance states. The temperature coefficient of resistance (*TCR*), defined as

$$TCR = \frac{1}{R}\frac{dR}{dT}, \tag{6}$$

is often used to compare the (normalized) change in resistance of different materials with temperature [1]. In our devices, the TCR depends on the resistance of the state, decreasing from values near zero in the low-resistance (ON) state to more negative values as the resistance of the programmed state is increased (Fig. 8.6(a)). As expected, devices that were shorted (and were not programmable) had a positive TCR, indicating metallic conduction.

The dependence of the TCR on the resistance of the memory state is analogous to trends observed in discontinuous metal films or ceramic-metal composites (cermets) (Fig. 8.6(b)) [1]. For very discontinuous metal films, very large sheet resistance with large negative TCR is measured because the metal (deposited on an insulating substrate) exists only in isolated clusters, so that conduction is thermally activated. As the amount of deposited metal is increased, the film becomes

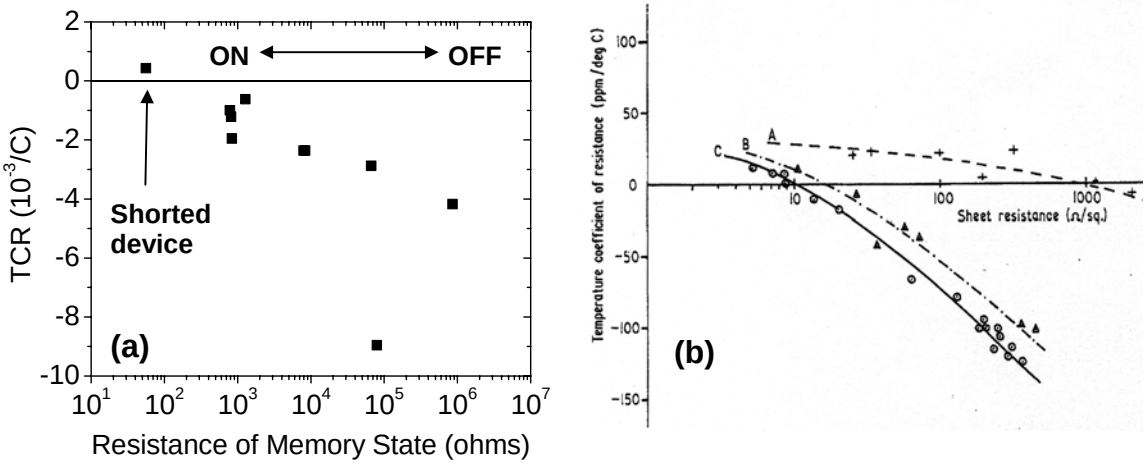


Figure 8.6. (a) Temperature coefficient of resistance (TCR) vs resistance of memory state. The resistances of the different memory states of edge devices (8 MUA layers) were measured as a function of temperature between 100 and 400 K. Each point represents the average TCR over this range. Also shown is a device that was shorted. (b) TCR vs sheet resistance of discontinuous NiCr films deposited on insulating substrates. The different lines represent data from different substrates (A: rough ceramic, B: crystalline ceramic, and C: glass) (from Ref [1]).

more continuous, its sheet resistance decreases and its TCR is increased to less negative values. Eventually the film becomes continuous and a very low sheet resistance (and positive TCR, corresponding to metallic conduction without activation) is measured. A similar trend is observed as the concentration of metal in an insulating ceramic is increased.

The analogous relationships between TCR and resistance observed in our devices and in cermets suggest that it is appropriate to think of the conducting paths as local regions in the insulator with increased quantities of metal (in our case gold from the electrodes). It is most likely that any gold present in the MUA is the form of clusters, due to the relative instability of isolated gold atoms or ions [27]. The OFF state of the device then corresponds to the presence of isolated metallic clusters in the MUA film (Fig. 8.7(a)). Application of voltages between 2-5 V causes the field-assisted diffusion of the gold ions (or charged clusters) into the film, leading to the formation of conducting regions with large numbers of gold clusters (Fig. 8.7(b) and (c)). Larger

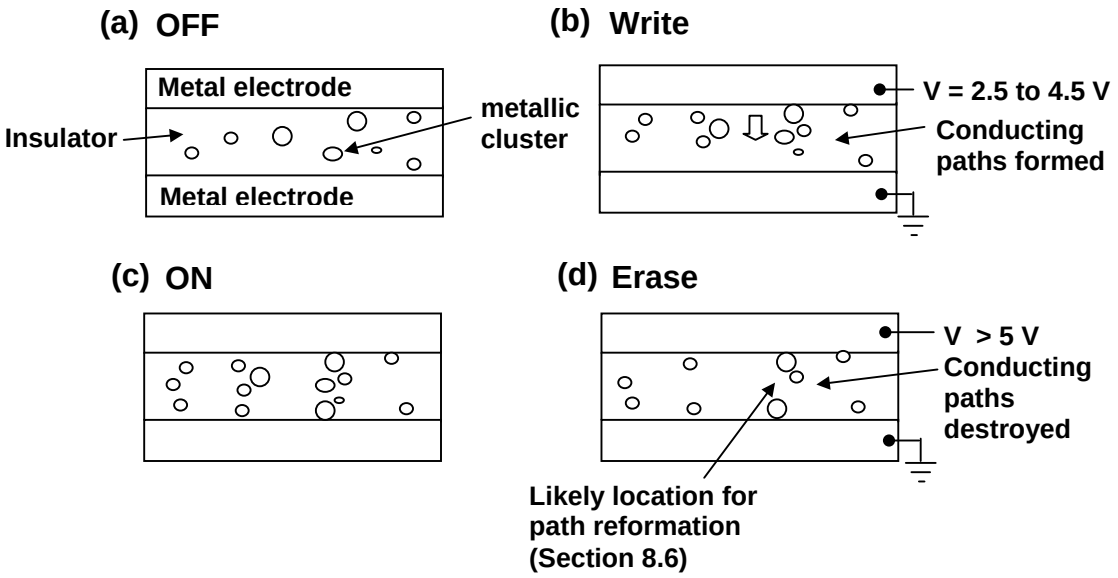


Figure 8.7. Schematic of gold-island conducting-path model (a) Device begins OFF, with isolated gold clusters. (b) Write voltage (2.5 to 4.5 V) causes the movement of gold clusters into the film. (c) Device in ON state is characterized by hopping paths formed by gold clusters in insulating film (d). Application of voltages larger than 5 V leads to destruction of the paths due to joule heating, returning the device to the OFF state. Some conducting paths may be only partially destroyed, leaving areas with much lower effective insulator thickness that may result in a high probability of path formation during a subsequent write operation (Section 8.6).

voltages cause the diffusion of gold out of these regions due to joule heating, reducing their conductivity (Fig. 8.7(d)). In fact, other workers have reported conductance switching in thin, discontinuous “gold island” films [28].

To confirm the presence of gold within the organic layer when the device was formed and/or programmed ON, we developed a device structure to allow us to program the device and then remove the top electrode, as envisioned in Figure 8.8. In this structure, we deposited a thin (30 nm) silver layer (to serve as a bottom electrode) onto a silicon wafer. The silver layer was patterned by a shadow mask during evaporation. We then spin cast a 30 nm PVK film onto the silicon wafer. Top electrodes were prepared by evaporating 300 nm gold films through a shadow mask onto a separate silicon wafer with a thin (30 nm) oxide layer. Because the gold did not adhere well to the oxide, we could contact a gold electrode with a needle probe and use the probe tip to remove the electrode from the oxidized silicon wafer and transfer it to the top of the PVK film. This resulted in the structure of Figure 8.8(a) (for additional experimental details, please refer to Appendix B). We applied bias by contacting the top gold electrode with a flexible gold wire (and the bottom silver electrode with a needle probe). Although many devices made in this manner were shorted or broke down upon application of voltages greater than 2 V (likely due to scratching when we deposited the top electrode), in some cases we were able to apply voltages up to 10 V

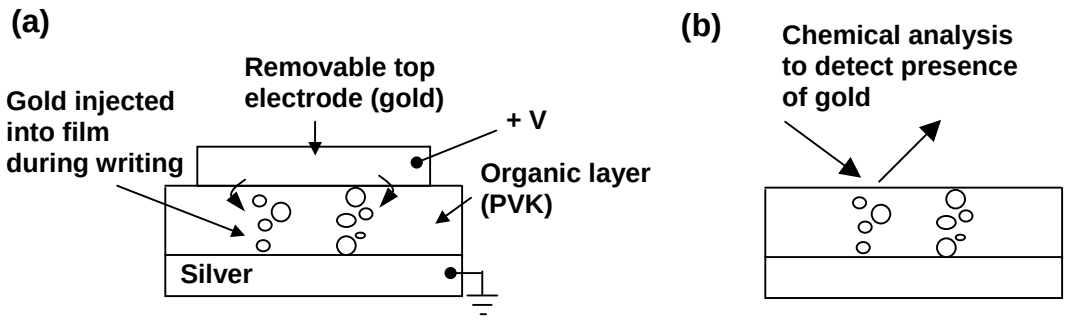


Figure 8.8. Schematic of structure with removable top electrode to allow chemical analysis of organic layer after programming. (a) The device consists of a PVK layer sandwiched between a bottom silver electrode and a removable top gold electrode. The device is formed and programmed by applying positive bias to the gold electrode with the silver electrode grounded. In the hypothesized mechanism, programming the device leads to the injection of gold into the organic layer (b) After removing the top electrode, chemical analysis of the organic layer can be done to determine if gold is present.

and cause the devices to form. They could then be programmed in the usual manner. After programming, we removed the top gold electrode (by physically manipulating it with the needle probe) to allow chemical analysis of the PVK film (Fig. 8.8(b)).

Because the bottom electrode was silver, any gold detected in this analysis would have been injected from the top gold electrode. (The need to make the bottom electrode silver to allow the identification of gold in the organic layer required us to use PVK rather than MUA, as we had little experience with MUA growth on silver). We anticipated being able to measure small concentrations of gold in devices that had been formed but programmed OFF, and higher concentrations of gold in devices that had been programmed ON. To perform the chemical analysis, we used both SEM with an energy-dispersive x-ray (EDX) detector (this was done with the help of Jane Woodruff using the Philips XL-30 FEG-SEM in the Princeton Institute for the Science and Technology of Materials) and scanning Auger analysis (this was done with the help of Dr. Pat. McKeown, using a Physical Electronics 660 Scanning Auger Microprobe at Evans East Laboratories in East Windsor, NJ). Both of these techniques can identify the presence of elements at concentrations as low as ~0.1 atomic % at lateral resolutions below 1 μm (simultaneous imaging of secondary electrons in both techniques allows the precise positioning of the sampling area) [29].

Unfortunately, we were not able to identify gold in any of the devices that we had formed and programmed. This was likely due to experimental limitations, rather than the absence of gold in the organic film. Because we had to use relatively large gold electrodes (> 50 x 50 μm^2) to allow manipulation with our needle probe, this resulted in relatively large device areas (>20 x 20 μm^2, defined where the gold and silver electrodes overlapped). We had hoped that the secondary electron images would reveal likely locations for formation of conducting paths (as discolorations or other apparent damage to the organic layer) but we were not able to find any consistent markings on formed devices. We therefore had to scan the entire device area during the chemical analysis. As we will discuss later, it is likely that any conducting regions are localized and have cross-sectional areas of ~10 to 100 nm^2. Therefore, even if these regions were entirely gold, they would represent a very small fraction of the scan area, corresponding to 100 $nm^2/100\ \mu m^2 = 10^{-6}$, well below the resolution of either technique. We also tried conducting smaller, multiple scans, each

covering a portion of the device area, but this does not adequately increase the resolution unless impractically small (~1 μm^2) scans are used.

The development of smaller area (~1 μm^2) device structures in which the top electrode can still be removed may lead to chemical analysis with higher elemental resolution, allowing more direct confirmation (or rejection) of our hypothesis that the conducting paths are due to gold. This is a promising avenue for future work. In the remainder of this chapter we will find that there is additional circumstantial evidence that our hypothesis is correct. Furthermore, in other work on electroformed Al_2O_3 devices with gold and aluminum electrodes, workers have been able to show that, after forming, the Al_2O_3 layer contains gold by using repeated etching followed by chemical analysis [30]. The considerable circumstantial evidence in our work and previous results on an alternative film give us reasonable confidence that the conducting paths in our devices are due to gold (and not an alternative material, such as a carbonaceous filament). We next examine several implications of the gold-clusters model.

8.5.1 Forming Voltage

The need to apply a forming voltage to most insulating devices to increase their electrical conductivity and place them in a programmable state (Section 7.3) is consistent with the metallic clusters model. In this viewpoint, the relatively large voltage in the forming step is necessary for the initial injection of metal atoms or clusters from the electrode into the film [2]. The increased roughness of the electrodes following forming (Section 7.6) is also reasonable in this context, and may be a result of the partial breakdown of the film and removal of portions of the electrode.

The physical basis for the ionization of gold in the electrode and injection of it into the electrode is less clear. In particular, gold is notable for its resistance to oxidation [31]. Still, the presence of other atoms (such as S) can help stabilize ionized gold, increasing the likelihood of oxidation [32]. Furthermore, experiments have shown that two gold electrodes held in close proximity (~50 nm) in air can form interconnecting metallic bridges at sufficient voltages (10 to 100 V) [22]. Removal of gold from an electrode due to an applied voltage is therefore clearly plausible, even if the exact mechanism is unclear.

We now consider the variation in forming voltage with MUA thickness (shown in Fig. 7.2(b)) for PoPI, PrPM, and edge devices. Examining first the PoPI devices, we

find that the average forming voltage increases as the number of MUA layers increased. This suggests that the injection of ionized gold into the film is field dependent, as we might expect. The large variations the voltage required for forming are also not surprising, as AFM measurements (Chapter 3) indicated significant variations in the MUA film thickness (with peak to valley distances comparable to the thickness) regardless of the number of MUA layers. Injection of gold into the film is likely to occur in valleys in the MUA film where the electrode already partially penetrates the film. The roughness of the MUA layer thus results in large variations in forming voltage for a given thickness but does not obscure the overall trend of larger forming voltages for thicker devices, reflecting the field dependence of the process.

In contrast, forming of edge and PrPM devices occurs near 2.5 V (with significant scatter), independent of MUA thickness. This lack of voltage dependence on MUA thickness can be understood in the context of our discussion of the different device structures in Chapters 4 and 5. In the edge and PrPM structures, devices include MUA grown on the edge of metal layer. These MUA layers are of poorer quality, which led to partial metal penetration into these devices resulting in higher current densities and (in the case of PrPM devices) lower yields of insulating devices. It is likely that partial penetration of the top gold electrode into the MUA layers in the edge and PrPM layers also leads to the large scatter in forming voltage and its apparent independence from device thickness observed here. In support of this hypothesis, we found that in some cases the conductance of edge devices could be programmed without the need to apply a forming voltage, implying that metal clusters may have already penetrated the film to the extent necessary for formed behavior. Furthermore, by applying large currents to some edge devices that were initially shorted, we could reduce their conductivity and induce a programmable-resistance state similar to the one obtained by forming initially insulating devices. In these devices, it is probable that the shorting was due to metallic filaments penetrating the MUA film. By applying large currents, we may have ruptured these filaments (in a similar fashion to the destruction of the conducting paths in formed devices) so that the device resistance could then be programmed in the usual manner.

8.5.2 Choice of Electrode and Insulator Material

As discussed in Chapter 4, studies of metal evaporated onto organic films indicate that while gold is relatively inert and tends to diffuse into films (often as

clusters), highly-reactive Al bonds to the surface of the organic, limiting its ability to diffuse into the film [33]. We would therefore not expect devices contacted by an Al electrode to form or display programmable characteristics and NDR for positive bias on the Al, which is what we observe (Fig. 8.1).

We would also expect that devices made with an alternative organic layer (other than MUA) would nevertheless be capable of forming and programming when contacted by gold electrodes; this is again what we observe with devices made of PVK (Fig. 8.2). Still, we found MUA devices could be formed much more consistently and also displayed much more consistent NDR and programming after forming. The reason for this increased reliability is not clear. One possibility is that the self-assembly process enables increased film uniformity in comparison to spin coating. A second advantage of MUA is that because it self-assembles it is compatible with the edge structure, which enabled much lower ON resistance (10^{-6} Ω cm^2 instead of 10^{-3} Ω cm^2 for planar devices).

8.5.3 Electrical Transport in the Conducting Paths

The conducting paths most likely consist of a complicated network of gold clusters of varying sizes embedded within the insulating MUA. As we have seen, the temperature dependence of the current in these paths resembles that observed in discontinuous metal films (Fig. 8.6). Despite considerable experimental and theoretical effort, it has been difficult to determine the exact mechanism for conduction in discontinuous metal films, and it is likely that, depending on the exact size of the metal clusters and their separation, several different modes of charge transfer may dominate. The two most important mechanisms are thermally-assisted tunneling and thermionic emission [1].

In thermally assisted tunneling, electrons are transported between metallic clusters by tunneling through the thin insulating barrier between them. Depending on the size of the metal clusters the addition (or subtraction) of an electron can result in significant coulombic energy [34]. Additional energy must be added to the system to overcome the coulombic barrier, so that the process is thermally activated, unlike direct tunneling between metal electrodes. In thermionic emission, an applied electric field lowers the barrier to charge injection, so that thermally excited carriers in a metal cluster can be transported through the conduction band of the insulator to an adjacent

metal cluster [35]. Generally, thermionic emission is expected to dominate for lower barrier heights and increased separation between metal clusters, while thermally assisted tunneling dominates at larger barrier heights and smaller separations [35]. However, models based on both mechanisms predict similar dependences on voltage and temperature so it is difficult to distinguish between them, and there are discrepancies between all models and some experimental characteristics [34]. Still, although the detailed conduction is difficult to model, it is likely that one or both of these mechanisms dominate charge transport in the conducting paths.

8.6 Write times and the Formation of the Conducting Paths

The model of Dearnaley et al presents a physical mechanism for the destruction of the conductive paths (joule heating) but does not address the mechanism for their formation. How these conducting paths are formed, and in particular how fast they are formed, are critical questions for our work because the write time of the memory device will be limited by this process.

To study the write time, we applied voltage pulses to devices in the OFF state and monitored the time required to increase the current from its initial low value to a

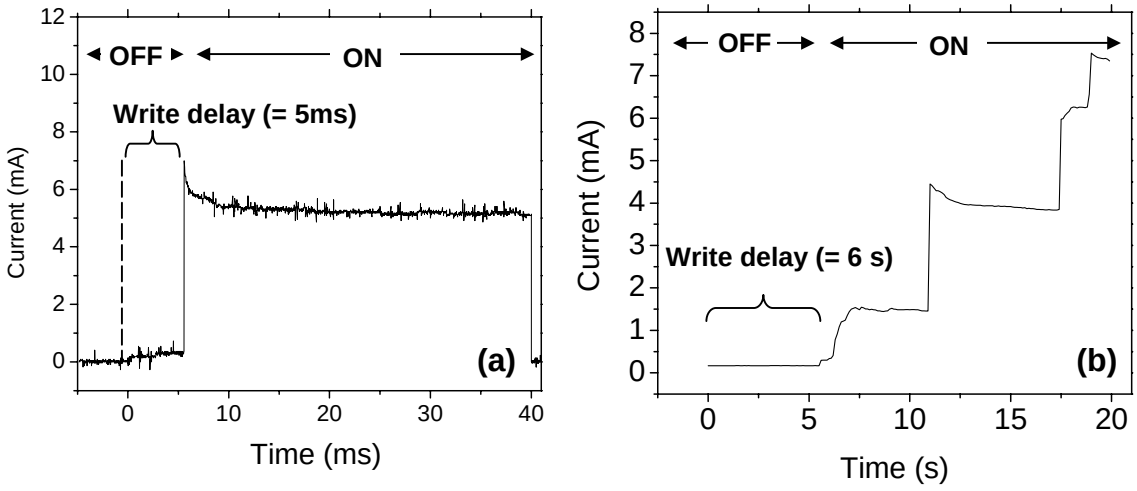


Figure 8.9. (a) Time evolution of current during a 40 ms, 3.5 V pulse (applied at time = 0 s) to an edge device (6 MUA layers) that had been programmed OFF with a 1 ms, 8 V pulse. (b) Time evolution of current during a 20s, 2.25 V pulse (applied at time = 0 s) to an edge device (7 MUA layers) that had been programmed OFF with a 1 ms, 8 V pulse.

larger value corresponding to the ON state. A typical measurement of the current during a 3.5 V, 40 ms write pulse on a device that is initially OFF is shown in Figure 8.9(a). After a delay of 5 ms, a sudden jump in the current, from near 0 mA to its final value of 6 mA, is observed. We also often observed multiple steps (Fig. 8.9(b)). In this case, a 2.25 V pulse was applied. Interestingly, at the lower write voltage we measure a much longer delay (prior to the increase in current) of 6 s rather than the 5 ms delay observed for the 3.5 V write voltage.

For fast programming times, it is necessary to minimize this delay time (which we define as the elapsed time between the application of voltage and the first current jump). We therefore determined this delay time as a function of device thickness and write voltage. Although the programming time was independent of the device thickness, the trend of decreased write delay with increased voltage was observed over a wide range of write voltage (Fig. 8.10). We found that the write delay decreased from greater than 10 s at a write voltage of 2.25 V to a delay of 1 μs at a write voltage of 5 V, corresponding to a slope of one decade/0.4 V. For write voltages above 4 V, the device write time was well below the 1 ms time required to write flash memory.

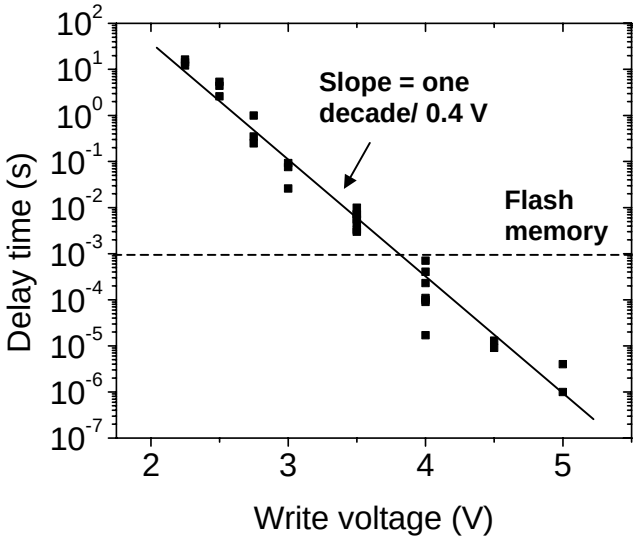


Figure 8.10. Dependence of write delay time (prior to the formation of the first conducting path) on write voltage. Prior to writing, devices were erased OFF with an 8 V, 1 ms pulse. Devices had 7 to 9 layers of MUA, and data was collected in both planar and edge structures. For comparison, flash memory's typical program time of ~ 1 ms is also shown.

We attribute the write delay to the time required to diffuse gold in such a way that conducting paths in the MUA film are formed. Similar delay times have been observed in other memory devices that utilize the field-assisted diffusion of Cu into an organic layer to modulate the device conductance [36]. In these devices, Cu electrodes were deposited onto an organic film (such as tris-8-(hydroxyquinoline), Alq_3) and the authors found that upon application of a small bias (~1 V), after a short (~30 ms) delay the device current increased rapidly to a final value (the device could then be returned to a low-current state by the application of larger bias). This delay time prior to the current increase was attributed to the time needed to diffuse Cu into the film.

In our devices, we also expect the diffusion process to be field-assisted (i.e. we assume that the gold or gold cluster is charged). It likely involves very high electric fields (at least 2 V/10 nm = $2x10^6$ V/cm, and probably greater as the effective insulator thickness may be even less than the device thickness, as we discuss later). Although previous work on the field-assisted diffusion of ions in amorphous solids (e.g. Ta, Nb, or Ni ions in metallic oxides) at low fields has indicated that the ionic current is linearly dependent on voltage, at high electric fields an exponential dependence of ionic current on the electric field has been observed [1, 37]. This current can be fit to the equation

$$j = j_0 \exp(-\frac{(Q - \lambda\theta E)}{kT/q}), \quad (7)$$

where *j* is the ionic current, Q the diffusion barrier (measured inV), λ is ½ the distance the ion moves in a typical jump (between potential minima), θ is the charge of the ion (in units of q), and E is the applied field [38]. This equation simply implies that the ionic current is carried by ions that are thermally excited over a diffusion barrier (*Q*) that is reduced by the applied electric field (multiplied by the ionic charge and λ, the distance over which it acts, corresponding to half the total movement distance in each jump). In our devices, the charge of the ion is not known, and the nonuniform nature of the MUA film after forming makes it unlikely that the electric field is simply given by the applied voltage divided by the device thickness. To better fit our work, we use a modified form of equation (7):

$$t = t_0 \exp(\frac{Q - \alpha V}{kT/q}), \quad (8)$$

where *t* is the time required to write the device into the ON state (and is proportional to the inverse of the ionic current), and the dimensionless constant $\alpha = \lambda\theta / d_{eff}$, where d_{eff} is the effective insulator thickness (so that V/d_{eff} is the electric field). Fitting this equation to the data Figure 8.10 (assuming that the temperature is equal to the room temperature of 25 °C), we find a value of α = 0.15. If we assume that the ions (or clusters) have a single positive charge, and that the effective insulator thickness is simply the device thickness (~10 nm), this implies that the ions move a distance of 3 nm with each jump. This is much larger than in previous work on ion diffusion at high electric fields, where metallic ions in tantalum oxide typically moved ~0.5 nm with each jump, corresponding to the typical distance between interstitial locations in tantalum oxide [38]. However, as noted previously it is likely that the effective insulator thickness is much lower than the device thickness (Fig. 8.7(d)), which would result in lower jump distances.

Surprisingly, although equation (8) predicts a decrease in write time at higher temperatures, we observed no significant dependence of write time on device temperature (Fig. 8.11(a)). This may be because in locations where conducting paths

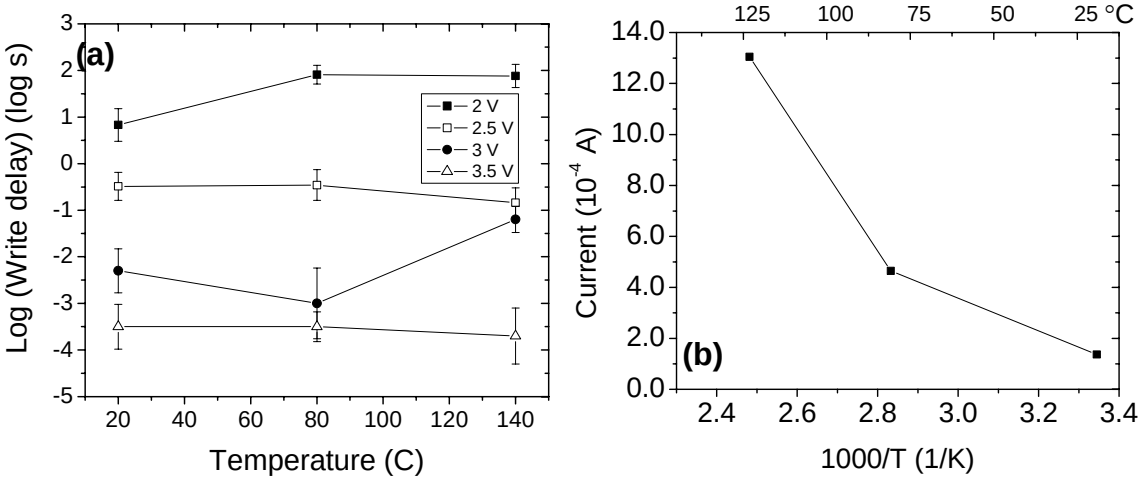


Figure 8.11. (a) Write delay time vs temperature for a different write voltages on a 6 MUA layer edge device. The device was erased with 8 V, 1 ms voltage pulses prior to each write cycle. Each point is the average of at least three measurements. (b) ON state current (measured at 0.5 V) after a 2 V, 20 s write as a function of temperature during programming (top) and 1000/T (bottom). The device was an 8 MUA-layer planar device and was erased with 6 V, 1 ms voltage pulses prior to each write cycle. Each point is the average of three measurements.

are formed, significant local heating may occur (prior to path formation), so that the actual temperature at which the diffusion occurs is higher than ambient temperature. Currents in devices were relatively high even in the OFF state (~10^2 A/cm^2), and similar to the ON state, it is possible that these currents were localized in certain areas of the device. This would result in significant localized heating. Indeed, locations where the alignment of metallic clusters within the film lead to very thin effective insulator thickness (e.g. Fig. 8.7(d)) are likely to carry large portions of the OFF current in addition to corresponding to locations in which very large electric fields are present; the relatively large temperatures and high fields in these locations make diffusion in these areas very likely.

Interestingly, if instead of measuring the write delay time vs temperature we apply a write voltage for a fixed time then measuring the resulting current in the ON state, we observe a clear temperature dependence (Fig. 8.11(b)). This reflected a larger increase in current with each step at elevated temperatures, even though the delays prior to the steps were similar. In this experiment we heated a device to different temperatures, applied a 6 V, 1 ms pulse to erase the device, next applied 2 V for 20 s to write the device ON, then measured the resulting current in the ON state. (In contrast, for the data in Fig. 8.5 we programmed the device at room temperature, then varied the temperature and measured the device conductance). For different programming temperatures, we found that after a 20 s write pulse the average ON current (measured at 0.5 V) increases from 2x10^{-4} A at 26 °C to 1.3x10^{-3} A at 130 °C. This increase of 6x in the ON current is too large to be due to the increase in ON conductance with temperature, which would result in a ~10% increase in conductance (Fig. 8.5). Instead, the larger ON-conductance of devices programmed at higher temperatures may be due to increased gold diffusion at elevated temperatures, even though the delay time does not decrease. Gold diffusion into the film is clearly a complicated process, so that in some cases it may not be sufficient to characterize it solely in terms of the delay time. The lack of a decrease in write time at higher temperatures may thus be due to either self-heating effects or because the write delay time does not fully capture the physical process.

We also note that in a field-assisted process, we might expect the MUA thickness to have an effect on the voltage necessary to write the device. However, we found that the MUA thickness also had little effect on write delay times at a fixed write voltage. Still, after the forming process has already introduced gold into the film, it is

likely that the effective thickness of the MUA layer is highly variable through the film. Gold diffusion will occur primarily in areas with the thinnest insulator thickness (corresponding to highest electric field for a given voltage). For example, a likely location for gold diffusion (and formation of a conducting path) is illustrated in Figure 8.7(d), where a conducting path is only partially destroyed by joule heating. The thickness of these areas will tend to have little correlation with the original device thickness.

As we have discussed previously, the step-like increases in current during writing (Fig. 8.9) are very suggestive of the formation of individually localized conducting paths. Using the size of this conductance step as well as the temperature dependence of the conductance states (Fig. 8.6), we can speculate on the size of the conducting paths (i.e. the cross-sectional area of the localized conducting regions). We typically observe an increase of current of 2 to 3 mA for an applied voltage of 2 to 3 V, implying a path resistance of ~ 1 kΩ. If we model the path as a simple resistor, its cross-section area is given by $A = \rho L / R$, where ρ is the resistivity of the path, L is its length (equal to the device thickness, or ~ 10 nm), and R is its resistance. The resistivity of pure gold is 2.6 μΩ cm, but because the conducting paths consist of isolated gold clusters, they will have a higher resistance than bulk gold. Still, if we extrapolate the TCR of the different states of our device to lower resistances, we obtain a TCR very close to that measured in a shorted device (Fig. 8.6(a)). This suggests that, just as the resistance of the ON state of our devices is ~20 times higher than in shorted devices, so the resistivity of the conducting paths in the devices is likely ~20 times higher than the resistivity of the metallic filaments in the shorted device. Assuming that the metallic filaments in the shorted device have a resistivity of ~ 30 μΩ cm (because nanoscale wires typically have resistivity that is ~10x higher than the bulk metal [39]), we obtain a path resistivity of ~600 μΩ cm. This resistivity implies an area of only ~60 nm^2, although given the assumptions that have been used to derive this area it is more reasonable to state that the cross-sectional area of the conducting paths is likely on the order of 10 to 100 nm^2.

This estimate is similar to the results of other recent work, where the size of a conducting filament in a programmable-conductance memory device based on an insulating organic monolayer was measured directly by AFM [40]. The authors found that the localized conducting regions (which also had a resistance of ~1 kΩ) had a

diameter of less than 40 nm. Even in edge devices, a path area of 10 to 100 nm^2 represents a very small fraction ($<10^{-3}$) of the total device area, so that conduction is very localized.

In our work, there is some evidence that these conducting paths are repeatedly formed in the same location. We found that, in addition to the write voltage, the write delay time also depended on the voltage used to erase the device prior to writing (Fig. 8.12). Decreasing the erase voltage by 2 V typically lead to a decrease in the write time by a factor of 10 to 100 for all write voltages. We attribute this dependence to a partial destruction of filaments at lower voltages. The partial destruction leaves metallic clusters near to the original path location (as in Fig. 8.7(d)), so that the formation of a conducting path in the same location on the next write operation occurs quickly. (Lower erase voltages result in increased OFF currents (Fig 7.8) for similar reasons.)

After erasing with a voltage of 6 V, we could then write (with delays of ~10 s) at voltages as low as 1.75 V. The higher threshold for writing of 2.5 V observed as the beginning of the NDR peak in current voltage scans is due to the (relatively) fast scan rates of ~2 V/s in these measurements (Fig. 7.13). Extrapolating the observed trend to voltages of 1 V, which is a typical read voltage, we estimate apparent write delays of ~1000 s. Inadvertent writing of the device during a read operation is therefore unlikely.

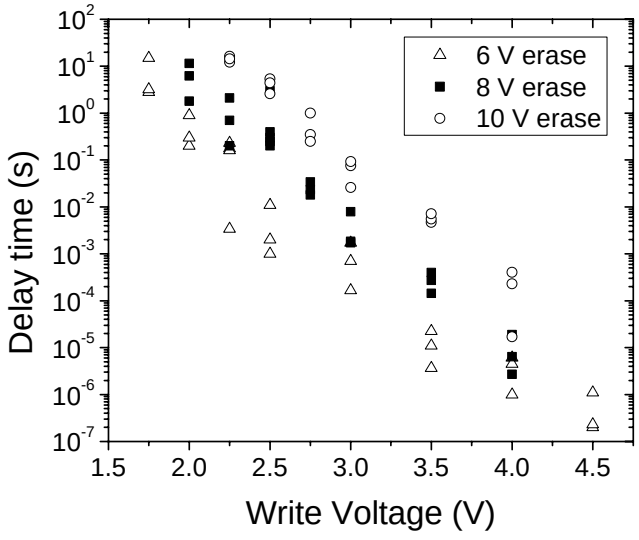


Figure 8.12. Write delay time vs write voltage for different erase voltages. Data from edge and planar devices with 7 to 9 layers of MUA are shown. All erase pulses were 1 ms, while write pulses of varying lengths were used.

Moreover, we were not able to write devices at or below 1.5 V with any consistency, even if very long write times were used (500 to >1000 s). The mechanism for programming at larger voltages may therefore not be relevant for very low voltages.

We finally note that for an erase voltage of 6 V and a write voltage of 4.5 V, we observed very fast write times of ~100 ns. This short programming time is very promising for use of the device in memory applications.

8.7 Erase times and Destruction of the Conducting Paths

We now examine the erase operation. As in previous work on formed inorganic devices, we found that devices could be returned to the OFF state very quickly [3, 5, 40]. Upon application of an erase voltage (6 to 10 V), we observed a brief delay of 40 ns, followed by a rise in device current to its peak value at 75 ns (Fig. 8.13). The current then rapidly returned to negligible values (< 5 mA in this experiment) after ~100 ns. Devices could thus be erased in less than 125 ns, roughly independent of erase voltage. These measurements were limited by the experimental apparatus, so that even quicker erase times are very probable.

As described earlier in Section 8.4, in the model of Dearnaley et al the physical mechanism for returning the device to the low-conductance state is joule heating that

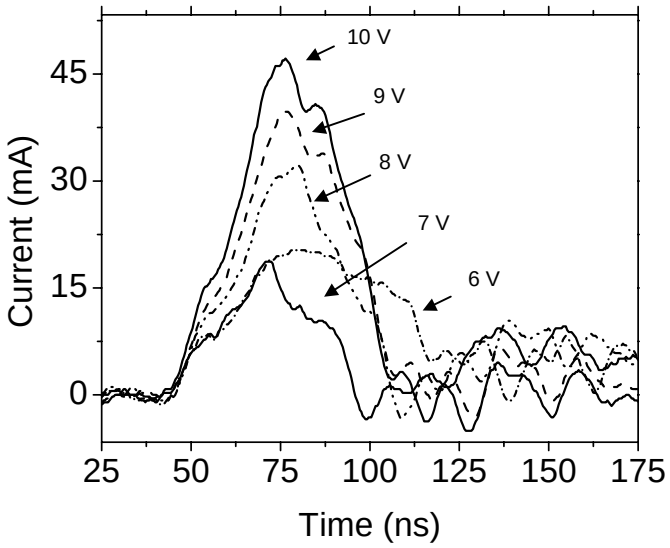


Figure 8.13. Erase (OFF to ON) response of edge devices with 6 MUA layers to voltage pulses of different amplitudes. The erase pulses were applied at t = 0 ns. Prior to erasing, devices were programmed ON with a 4 V, 2 ms pulse.

causes the destruction of the conducting paths. Previous workers have developed numerical and analytical models to determine the steady-state temperature in the conducting paths for different geometries, path resistances, and applied voltages [4, 13]. In these models, for paths with comparable diameters and resistances to the ones estimated in our work (~20 nm and 1 kΩ), steady state path temperatures easily reach over 2000 K for voltages above 5 V [21]. Although the temperature at which a path is destroyed is difficult to determine exactly, estimates range from 600 to 1300 K (the melting temperature of gold, 1340 K, corresponds to this upper limit) [21]. The steady state temperatures in the paths are therefore clearly sufficient to cause destruction of these paths and return the device to the OFF state.

Very little effort has been made to model the transient temperature in conducting paths to estimate the time required to reach temperatures sufficient to destroy the paths. Fortunately, some comparable modeling has been done to study phase change memory [41]. In these memories, an alloy (GeSbTe, for example) is placed into a low-conductance state by a very short, high-current pulse so that the material is rapidly heated then cooled, causing the atoms to freeze in an amorphous phase. Alternatively, the device can be programmed into a high-conductance state by a longer, medium current pulse that anneals the alloy into a crystalline phase. Simulations of the transient temperatures in these memory cells, which have dimensions (10^4 nm^2) much larger than we estimate for our conducting paths (10 to 100 nm^2), indicate that application of a 1 V, 2 mA pulse (corresponding to ~10^7 A/cm^2) leads to temperatures greater than 700 K within 10 to 30 ns [41]. The very fast erase times that we observe are therefore expected, and devices can probably be erased even faster than the ~100 ns timescale that we are limited to by our experimental apparatus.

8.8 Summary

In this chapter we have discussed the physical mechanisms in a molecular-scale programmable-resistance memory device based on multiple self-assembled layers of MUA sandwiched between gold electrodes in planar and edge device structures. The electrical characteristics of these devices (initially described in Chapter 7) can be explained within the framework of the model proposed by Dearnaley et al to describe similar characteristics in electroformed inorganic devices. In our case, the

application of write voltages causes the field-assisted diffusion of gold ions or ionized clusters into the film, leading to the formation of conducting pathways. Temperature-dependent measurements revealed that these pathways were not purely metallic but instead likely consisted of a complex network of gold clusters embedded in the MUA. During write operations, after small delays we observed step-like increases in the device current. These steps were attributed to the formation of individual nanometer-scale conducting regions with typical areas of 10 to 100 nm^2. As expected for the diffusion of gold ions in high electric fields, the delay time prior to the formation of these conducting pathways could be decreased exponentially by increasing the write voltage, to achieve write times as low as ~ 100 ns at 4.5 V. By application of larger erase voltages, these paths were destroyed very quickly (~100 ns) by joule-heating to return the device to the OFF state.

References

[1] D. S. Campbell and A. R. Morley, "Electrical-Conduction in Thin Metallic, Dielectric and Metallic-Dielectric Films" *Reports on Progress in Physics* **34** (4), 283 (1971).

[2] J. G. Simmons and R. Verderber, "New Conduction and Reversible Memory Phenomena in Thin Insulating Films" *Proceedings of the Royal Society of London Series a-Mathematical and Physical Sciences* **301** (1464), 77 (1967).

[3] A. K. Ray and C. A. Hogarth, "A Critical-Review of the Observed Electrical-Properties of MIM Devices Showing VCNR" *International Journal of Electronics* **57** (1), 1-77 (1984).

[4] A. K. Ray and C. A. Hogarth, "A Novel Description of Polyfilamentary Conduction in an Electroformed Insulating Film" *Journal of Physics D-Applied Physics* **20** (4), 552-554 (1987).

[5] G. Dearnaley, A. M. Stoneham and D. V. Morgan, "Electrical Phenomena in Amorphous Oxide Films" *Reports on Progress in Physics* **33** (11), 1129-1191 (1970).

[6] H. Pagnia and N. Sotnik, "Bistable Switching in Electroformed Metal-Insulator-Metal Devices" *Physica Status Solidi A-Applied Research* **108** (1), 11-65 (1988).

[7] R. E. Thurstans and D. P. Oxley, "The Electroformed Metal-Insulator-Metal Structure: A Comprehensive Model" *Journal of Physics D-Applied Physics* **35** (8), 802-809 (2002).

[8] W. Rodgers, R. E. Thurstans and D. P. Oxley, "The Forming Process in Electroformed MIM Structures" *Thin Solid Films* **90** (4), 391-391 (1982).

[9] R. E. Thurstans, P. C. Wild and D. P. Oxley, "Enhanced Forming in Al-SiO_x-Au Structures under Pulsed Bias" *Thin Solid Films* **20** (2), 281-286 (1974).

[10] R. D. Gould and M. G. Lopez, "Electrical Conductivity and Dynamics of Electroforming in Al-Siox-Al Thin Film Sandwich Structures" *Thin Solid Films* **433** (1-2), 315-320 (2003).

[11] A. L. Pergament, V. P. Malinenko, O. I. Tulubaeva and L. A. Aleshina, "Electroforming and Switching Effects in Yttrium Oxide" *Physica Status Solidi A-Applied Research* **201** (7), 1543-1550 (2004).

[12] S. Gravano, E. Amr, R. D. Gould and M. Abu Samra, "Monte Carlo Simulation of Current-Voltage Characteristics in Metal-Insulator-Metal Thin Film Structures" *Thin Solid Films* **433** (1-2), 321-325 (2003).

[13] A. K. Ray and C. A. Hogarth, "Recent Advances in the Polyfilamentary Model for Electronic Conduction in Electroformed Insulating Films" *International Journal of Electronics* **69** (1), 97-107 (1990).

[14] R. E. Thurstans, "Structure and Electrical-Properties of the Electroformed MIM Structure" *Thin Solid Films* **57** (1), 153-156 (1979).

[15] D. P. Oxley, R. E. Thurstans and P. C. Wild, "Pulse Experiments on Electroformed MIM Structures" *Thin Solid Films* **20** (1), 23-31 (1974).

[16] L. D. Bozano, B. W. Kean, V. R. Deline, J. R. Salem and J. C. Scott, "Mechanism for Bistability in Organic Memory Elements" *Applied Physics Letters* **84** (4), 607-609 (2004).

[17] G. Dearnaley, D. V. Morgan and A. M. Stoneham, *Journal of Non-Crystalline Solids* **4**, 493-611 (1970).

[18] S. Sze, *Physics of Semiconductor Devices*. 2nd ed. 1981, New York: John Wiley and Sons.

[19] R. R. Sutherland, "Theory for Negative Resistance and Memory Effects in Thin Insulating Films and Its Application to Au-ZnS-Au Devices" *Journal of Physics D-Applied Physics* **4** (3), 468-& (1971).

[20] S. J. Farlow, *Partial Differential Equations for Scientists and Engineers*. 1993, New York: Dover Publications.

[21] R. D. Gould, "The Effects of Filamentary Conduction through Uniform and Flawed Filaments in Insulators and Semiconductors" *Journal of Non-Crystalline Solids* **55** (3), 363-386 (1983).

[22] G. L. Pearson, "The Formation of Metallic Bridges between Separated Contacts" *Physical Review* **56**, 471-474 (1939).

[23] N. R. Couch, B. Movaghar and I. R. Girling, "Electromigration Failure in Filaments through Langmuir-Blodgett-Films" *Solid State Communications* **59** (1), 7-9 (1986).

[24] N. W. Ashcroft and N. D. Mermin, *Solid State Physics*. 1976, Fort Worth: Saunders College Publishing.

[25] S. Banerjee, A. Dan and D. Chakravorty, "Review: Synthesis of Conducting Nanowires" *Journal of Materials Science* **37**, 4261-4271 (2002).

[26] D. Natelson, R. L. Willett, K. W. West and L. N. Pfeiffer, "Molecular-Scale Metal Wires" *Solid State Communications* **115**, 269-272 (2000).

[27] R. Willecke and F. Faupel, "Diffusion of Gold and Silver in Bisphenol A Polycarbonate" *Macromolecules* **30**, 567-573 (1997).

[28] R. Blessing and H. Pagnia, "Forming Process, IV Characteristics and Switching in Gold Island Films" *Thin Solid Films* **52** (3), 333-341 (1978).

[29] *Choosing the Appropriate Analytical Technique*. [cited 11/29/05; Available from: http://www.eaglabs.com/en-US/services/choosetechnique-92005.pdf.

[30] R. Rahman, "Scanning Electron Microscopy and X-Ray Photoelectron Spectrometry Studies of Electroformed Al/Al_2O_3/Au Structures" *Thin Solid Films* **71**, 7-13 (1982).

[31] R. J. Puddephatt, *The Chemistry of Gold*. 1978, Amsterdam: Elsevier.

[32] R. L. McCarley, Y.-T. Kim and A. J. Bard, "Scanning Tunneling Microscopy and Quartz Crystal Microbalance Studies of Au Exposed to Sulfide, Thiocyanate, and N-Octadecanethiol" *Journal of Physical Chemistry* **97**, 211-215 (1993).

[33] F. Faupel, R. Willecke and A. Thran, "Diffusion of Metals in Polymers" *Materials Science & Engineering* **R22**, 1-55 (1997).

[34] T. J. Coutts, *Electrical Conduction in Thin Metal Films*. 1974, Amsterdam: Elsevier.

[35] D. Braun, "Electronic Injection and Conduction Processes for Polymer Devices" *Journal of Polymer Science Part B-Polymer Physics* **41** (21), 2622-2629 (2003).

[36] L. P. Ma, Q. F. Xu and Y. Yang, "Organic Nonvolatile Memory by Controlling the Dynamic Copper-Ion Concentration within Organic Layer" *Applied Physics Letters* **84** (24), 4908-4910 (2004).

[37] D. A. Vermilyea, *Anodic Films*, in *Advances in Electrochemistry and Electrochemical Engineering*, P. Delahay, Editor. 1963, Interscience Publishers: New York.

[38] C. P. Bean, J. C. Fisher and D. A. Vermilyea, "Ionic Conductivity of Tantalum Oxide at Very High Fields" *Physical Review* **101** (7), 551-554 (1956).

[39] Y.-J. Chen, J. H. Hsu and H.-N. Lin, "Fabrication of Metal Nanowires by Atomic Force Microscopy Nanoscratching and Lift-Off Process" *Nanotechnology* **16**, 1112-1115 (2005).

[40] C. N. Lau, D. R. Stewart, R. S. Williams and M. Bockrath, "Direct Observation of Nanoscale Switching Centers in Metal/Molecule/Metal Structures" *Nano Letters* **4** (4), 569-572 (2004).

[41] S. Lai, "Current Status of Phase Change Memory and Its Future" *IEDM '03 Technical Digest*, 10.1.1-10.1.4 (2003).

Chapter 9

Summary and Future Work

9.1 Summary

In this thesis we have addressed several challenges to achieving highly scaled electronic devices based on self-assembled organic films and demonstrated a molecular-scale programmable-resistance device that is promising for application in integrated nonvolatile memory.

Electrostatic modeling of the geometry of a monolayer FET revealed that, although gate-channel coupling is very poor due to their large source-drain capacitance, the gate could modulate the channel potential by up to 1 V for devices with a 5 nm long molecular channel and (counter-intuitively) a relatively thick (greater than 10 nm) gate insulator.

We developed several structures that allow the fabrication of two-terminal molecular-scale devices with minimal defects and integrated metal wiring. The structures included large-area (10 to >1000 μm^2) planar structures that were patterned by evaporating metal contacts or insulating layers through shadow masks, as well as a minimal-area (<0.5 μm^2) structure where a self-aligned insulating layer was used to keep the device area to the vertical edge of a deposited metal layer. These structures were used to make the first reported electrical measurements on self-assembled multilayers of MUA. As expected for the insulating molecule, currents were low and decreased as the number of MUA layers increased. Charge transport through the MUA film was characterized as Richardson-Schottky emission.

Finally, by applying larger voltages we could operate the devices as programmable-resistance memories. Memory devices had fast programming times (100 ns), long data retention times (> 3 months), reasonable durability (>10^4 write/erase cycles), and low ON resistance (10^{-6} Ω cm^2). These characteristics are promising in comparison to other organic memory technologies and silicon-based flash memory (Table 9.1). In particular, simulations of read operations in memory arrays indicated that the very low resistance of the ON state (10^{-6} Ω cm^2) in these memory

Characteristic	These devices	Flash memory	Other organic memories
Program time	100 ns	1 ms	100 ns to 1 ms
Program voltage	< 10 V	10 V	0.5 to 10 V
Retention time	> 3 months	> 10 years	> months
Write/erase cycles	$> 10^4$	10^6	?
ON/OFF ratio	10^3	-	4 to 10^7
Program Polarity	Unipolar	-	Mostly bipolar
ON resistance (ohm cm^2	10^{-6}	-	$>10^{-4}$ (mostly $>10^{-2}$)

Table 9.1. Typical characteristics of MUA devices in comparison with flash memory and other organic memories (from Tables 6.1 and 6.2).

devices would enable fast read times (10 ns) even in large memory arrays with up to 10^9 bits. For comparison, most other organic memories, with an ON resistance greater than 10^{-2} Ω cm^2, would be limited to arrays of less than 10^3 bits for comparable read times. We found that a model based on the formation and destruction of conducting paths that consist of metal clusters injected into the MUA film from the electrodes best explained the programmable resistance.

9.2 Future Work

The work presented in this thesis suggests several possible avenues for future work. Here, we review several specific directions mentioned earlier in the text and propose several additional, more long-term research areas.

For further MUA characterization, inverse photoemission spectroscopy (IPES), which measures empty energy levels and hence complements the UPS measurements that we performed, would allow a more complete picture of the energy levels in the MUA-Au system. This more complete picture may lead to a better understanding of the electrical transport in MUA films (Chapter 4).

Further development of the two-terminal edge structure into a bottom-gate three-terminal FET (Chapter 5) would also be of interest. By employing a relatively thick gate insulator (>10 nm) and a multilayer self-assembly process to ensure a channel length of greater than 5 nm, the results of Chapter 2 indicate that the gate should be able to modulate the channel potential by 1 V. Even though this may not be

sufficient to align molecular levels in MUA to source-drain Fermi levels for enhanced source-drain current (because of the large HOMO-LUMO gap of alkane chains), it should be possible to grow self-assembled multilayers of conjugated molecules (with smaller energy gaps) using chemistry similar to that used in the MUA growth [1] or alternative approaches [2].

Additional characterization of the physical mechanisms in the programmable-resistance memory devices based on MUA films is desirable. In particular, it would be interesting to do an experiment that could detect the presence of gold within the organic layer to confirm our argument that the programmable resistance of the devices is due to injected metal clusters (Chapter 8).

More broadly, the goal of large-scale integration of molecular-scale devices with or without CMOS circuits presents a number of interesting challenges. For example, although we have seen that the problem of damage to the organic layer due to vacuum-deposited metal can be decreased, preparation of integrated metal wiring with evaporation processes will likely remain difficult. Alternative techniques, such as electroless metal deposition, are worth further investigation [3].

A second challenge to the integration of molecular-scale devices is the incompatibility of most organic layers with most photolithography processes. The ability to photolithographically pattern organic layers (or metal layers deposited after organic growth) would make fabrication of highly scaled organic devices significantly easier. This goal should be more attainable with organic layers grown by self-assembly, as the chemical bonding between the molecular layers and substrate enhances the stability of these films with respect to bulk organic layers (which have weaker van der Waals binding between molecules). Indeed, the stability of self-assembled monolayers has already led to their application as resists for chemical and even plasma etching [4, 5].

Finally, even though the discovery of programmable resistance in the MUA devices was fortuitous, the hypothesized programming mechanism (i.e. the physical movement of metal in an insulating film) is appealing for future generations of nonvolatile memory. Penetration of metal into a thin organic film, a process we initially sought to avoid during metal evaporation, may in fact sometimes have useful application. This is because nonvolatile memories that depend on charge storage (such as flash memory) will likely face fundamental limits on scaling, due to the likelihood of charge tunneling at small dimensions. In contrast, memories that rely on

the physical movement of atoms should in principle have higher stability, even when highly scaled. Furthermore, as we have seen in our devices, this mechanism can allow the very large current densities needed for fast read times. One potential drawback to devices based on this mechanism is the larger programming energies needed for atomic motion. Still, by further engineering of the metals and insulator, it should be possible to fabricate devices that operate similar to gold-MUA-gold devices but at lower programming voltages, resulting in lower power consumption and increased durability. In fact, memory devices that appear to be based the field-assisted diffusion of metal through an organic matrix (the Cu-organic devices in Chapter 6, Table II) have already been shown to operate at low voltages (< 1 V), although the slow switching times in these devices will require more work [6]. The further development of memory devices based on the field- (and/or thermally) assisted movement of metal atoms in an insulating matrix is therefore a very interesting avenue for future investigation.

References

[1] T. L. Brower, J. C. Garno, A. Ulman, G. Y. Liu, C. Yan, A. Golzhauser and M. Grunze, "Self-Assembled Multilayers of 4,4 '-Dimercaptobiphenyl Formed by Cu(II)-Catalyzed Oxidation" *Langmuir* **18** (16), 6207-6216 (2002).

[2] A. Ulman, "Formation and Structure of Self-Assembled Monolayers" *Chemical Reviews* **96** (4), 1533-1554 (1996).

[3] J. K. N. Mbindyo, T. E. Mallouk, J. B. Mattzela, I. Kratochvilova, B. Razavi, T. N. Jackson and T. S. Mayer, "Template Synthesis of Metal Nanowires Containing Monolayer Molecular Junctions" *Journal of the American Chemical Society* **124** (15), 4020-4026 (2002).

[4] A. J. Black, K. E. Paul, J. Aizenberg and G. M. Whitesides, "Patterning Disorder in Monolayer Resists for the Fabrication of Sub-100-Nm Structures in Silver, Gold, Silicon, and Aluminum" *Journal of the American Chemical Society* **121** (36), 8356-8365 (1999).

[5] M. J. Lercel, H. G. Craighead, A. N. Parikh, K. Seshadri and D. L. Allara, "Plasma Etching with Self-Assembled Monolayer Masks for Nanostructure Fabrication" *Journal of Vacuum Science & Technology a-Vacuum Surfaces and Films* **14** (3), 1844-1849 (1996).

[6] L. P. Ma, Q. F. Xu and Y. Yang, "Organic Nonvolatile Memory by Controlling the Dynamic Copper-Ion Concentration within Organic Layer" *Applied Physics Letters* **84** (24), 4908-4910 (2004).

Appendix A

Solvent-Enhanced Dye Diffusion in Polymer Thin Films for Polymer Light-Emitting Diode Application

A.1 Introduction

In this appendix we study the solvent-enhanced diffusion of dye in a polymer film. Solvent-enhanced dye diffusion is a key step in a process that was developed in our group to locally tune the emission color of polymer light-emitting diodes (PLEDs) for use in full-color displays. Most of the development of the patterning process was done by Florian Pschenitzka (PhD 2002, now at Cambrios Technologies, Mountain View, CA). In this work we focus on the physical basis of the dye-diffusion step used in the developed approach. The experimental work reported here was carried out with the help of Florian Pschenitzka, Hongzheng Jin (currently a PhD candidate in our group), and Brent Bollman (Class of 2003, now at Nanosolar, Palo Alto, CA). Modeling was carried out with the help of Brent Bollman and in collaboration with Prof. Richard Register (Department of Chemical Engineering, Princeton University). Most of this work is reported in Ref [1] and all of the figures in this appendix are from this reference.

PLEDs have emerged as a very promising candidate for commercial displays, and first-generation PLED displays can already be found in the marketplace [2]. PLEDs are appealing in part because the polymer layer can be deposited by a low-cost spin-coating process. In most cases, further patterning is then necessary if the polymer is to be used in a full-color display, because the as-deposited uniform film is generally limited to emission of only one color.

Several groups have suggested the use of a dry dye transfer from a large-area dye source to pattern the local emission color of the polymer film as a route towards the integration of red, green, and blue (RGB) PLEDs [3-6]. These dry transfer processes are attractive compared to inkjet printing of the dye because they can in principle cover large areas in one step, and because they avoid film nonuniformity and lateral redistribution problems which occur during the drying of printed droplets [7-10].

In dry printing, the dye can be thermally transferred to the emissive polymer by printing from a pre-patterned polymer stamp containing the dye (Fig. A.1(a)) [11]. However, the transferred dye tends to accumulate on the surface of the polymer film where it is mostly inactive due to the lack of energy transfer from the host polymer or inefficient due to dye concentration quenching (Fig. A.1(b)). Treating the sample in solvent vapor after the initial dye transfer was found to promote the rapid diffusion of the transferred dye throughout the thickness of the polymer at room temperature (Figs. A.1(c), A.1(d)). This redistribution process otherwise required annealing at temperatures near the polymer glass transition temperature (T_g), where the polymer could degrade.

This appendix is organized as follows. In Section A.2, an overview of the process and past work is given. Section A.3.1 presents experimental results for the increase in thickness of the device polymer as a function of solvent, vapor-exposure time, vapor pressure, and temperature, and Section A.3.2 presents a model for these effects. Finally, Section A.4.1 describes experimental results for actual dye diffusion in the presence of solvent vapor, and Section A.4.2 describes the increase in dye diffusion as due to the free volume increase caused by the solvent.

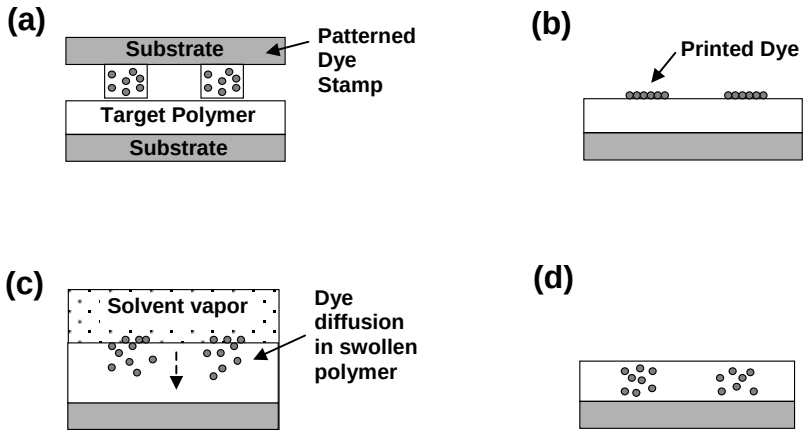


Figure A.1. Schematic overview of patterned dye printing and subsequent dye diffusion. (a) Dye is printed onto target device polymer from pre-patterned polymer containing dye. (b) Printed dye remains at or near surface of the polymer. (c) Polymer is exposed to solvent vapor and swells; dye diffuses rapidly into film. (d) Polymer returns to original thickness after solvent vapor is removed. Vertical dimensions are exaggerated vs. lateral dimensions.

A.2 Background on Solvent-Enhanced Dye Diffusion in Poymers

In this section, we describe our group's development of a solvent-enhanced diffusion process. Most of this work was carried out by Florian Pschenitzka.

A.2.1 Dye Transfer

Spin-coating or blade-coating of the emissive polymer in PLED displays is desirable because both are simple and low cost. A patterning process must then generally be used to locally introduce dye into the polymer film to obtain a full-color, RGB display (alternatively, there have also been reports of selectively deactivating globally-distributed dyes through patterned UV radiation [12]). Initial work to locally introduce a dye utilized a shadow mask placed between the dye source and the target polymer layer [4]. However, this approach resulted in damage to the polymer layer due to physical contact between the metal mask and soft polymer. An alternative soft printing process was therefore developed [13]. In this procedure, a "stamp" is prepared by spin-coating the polymer Vylon 103 (obtained from Toyoba, M_w ~20,000- 25,000 g/mole, 98% by weight) doped with a dye, in this case coumarin-6 (C6, emission peak at 495 nm, 2% by weight), onto a glass substrate. The device polymer consists of a thin (80 – 120 nm) film of the hole-transport polymer poly(9-vinlycarbazole) (PVK) (M_w ca. 1,100,000 g/mole, 71% by weight in the final film) mixed with the electron transport molecule 2-(4-Biphenylyl)-5-(4-tert-butyl-phenyl)-1,3,4-oxadiazole (PBD) (29% by weight) deposited by spin-coating from solution (100 mg PVK, 40 mg PBD, 7.5 mL chlorobenzene) onto an ITO-coated glass substrate [14]. After patterning the stamp, the dye is printed onto the top of the device polymer by placing the target and source films in direct contact in vacuum at elevated temperatures (60 ºC - 80 ºC) for 20 - 60 minutes.

Following printing, the dye is concentrated at the polymer surface, where its photoluminescence efficiency is limited by a lack of energy transfer from the polymer and/or dye concentration quenching. Secondary ion mass spectrometry (SIMS) was used to measure the initial dye distribution [15]. Because only the C6 contains sulfur, the sulfur signal is used to mark the position of the C6 in the polymer film. Prior to annealing, the sulfur signal from the as-printed sample shows a peak near the surface of the sample and extends 40 nm into the sample, dropping to negligible levels

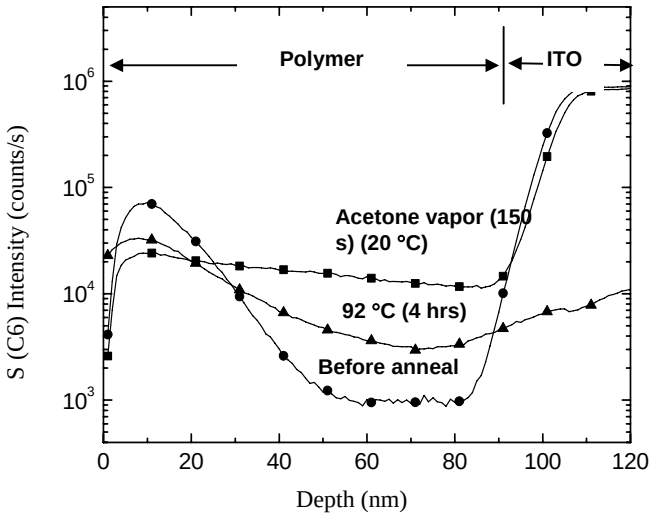


Figure A.2. SIMS profiles of sulfur (from C6 dye) in a 90-nm PVK/PBD film with printed C6 layer before annealing (circles), after a 4-hour anneal at 92 ºC in vacuum (triangles) and a 150 s anneal at 20 ºC in acetone vapor (90 torr) (squares). The rise of all signals beyond 80 nm is a SIMS artifact. From Florian Pschenitzka.

between 40 - 80 nm and then rising rapidly after 80 nm (Fig. A.2). Both the exponentially-decaying tail of the profile into the sample and the rise of the signal at 80 nm are SIMS artifacts. The rise at 80 nm is from a $^{16}O_2^+$ signal (oxygen from the ITO) being misinterpreted as $^{32}S^+$. Spurious signals within the polymer could also arise if the sample was not sufficiently outgassed in the SIMS chamber to remove O_2 (or water) that had been absorbed by the polymer prior to loading. The exponentially decaying tail near the surface does not represent any initial diffusion of the dye into the film during the printing step, and is instead due to well-known “knock-on” effects. These effects occur when the Cs^+ primary ion (for sputtering the surface) displaces the lighter sulfur atoms towards deeper locations during the measurement. This was confirmed by a control sample consisting of a thin layer of C6 that was evaporated directly onto the PVK/PBD layer (without heating); SIMS measurements on this sample revealed a similar profile to the printed dye. The 70 °C printing step is therefore not adequate to diffuse the dye into the polymer and instead leaves C6 accumulated on its surface.

A.2.2 Dye Diffusion

The dye can be diffused into the polymer by annealing in vacuum at elevated temperatures for long time periods. Figure A.2 shows that after 4 hours at 92 ºC, the C6 has diffused but is still far from uniformly dispersed. Annealing at higher temperatures is not practical, as the glass transition temperature T_g for this blend is only 120 ºC (measured by X. Jiang and Prof Richard Register in the Department of Chemical Engineering at Princeton University). Furthermore, the use of a polymer with a lower T_g is not a viable approach because device polymers with high T_g are desired for OLED reliability.

A process to temporarily enhance the dye diffusion without later compromising the device performance was therefore developed. Following dye printing, the polymer is exposed to solvent vapor, which it absorbs. The absorption of the solvent vapor causes an increase in the polymer's free volume. The increase in free volume dramatically enhances diffusion of the dye into the film, allowing the diffusion to take place at low temperature (e.g. room temperature) without damage to the polymer film. Finally, the polymer is dried in nitrogen, causing it to return to its original thickness and slow-diffusion condition.

Only 150 s in acetone vapor (partial pressure = 90 torr) at room temperature is necessary to ensure that the printed C6 is distributed nearly uniformly throughout the PVK/PBD (Fig. A.2). Thus the 150-s room-temperature treatment in acetone vapor causes a far larger amount of diffusion than the 4-hour anneal at 92 ºC, demonstrating that the solvent vapor causes a remarkable increase in the diffusion coefficient of the dye. The next two sections seek to fundamentally understand and characterize this enhanced diffusion.

A.3 Polymer Thickness and Index of Refraction Changes Under Solvent Vapor Exposure

Because it was expected that the enhancement of dye diffusion in solvent vapor would depend on the amount of solvent imbibed by the film, we investigated in detail the thickness increase of PVK/PBD films upon exposure to solvent vapor under various conditions. In this section, we present experimental results (Section A.3.1) and a model (Section A.3.2) for the dependence of PVK/PBD thickness and index of refraction on choice of solvent, solvent vapor pressure, and sample temperature.

A.3.1 Measurement of Changes in Polymer Thickness and Index of Refraction

A Filmetrics F20 reflectance spectrometer was used for *in situ* monitoring of polymer thickness and optical constants under solvent vapor exposure. For such measurements, PVK/PBD films of varying thickness were deposited by spin-coating onto silicon substrates. The normal-incidence reflectance spectrum from a tungsten-halogen bulb was recorded over a range of 450-850 nm, where absorption in PVK is negligible [16]. By measuring the bare silicon reflectance and assuming the polymer extinction coefficient in the wavelength range is zero, it is straightforward to extract the film thickness t_f and index of refraction n_f by fitting the measured reflectance profile to that expected from a simple interference model [17]. For this, we assumed the three-parameter Cauchy model for the wavelength dependence of n_f:

$$n_f(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} \tag{1}$$

The three parameters *A, B*, and *C,* along with t_f, were used as four adjustable parameters to fit the reflectance spectrum (Fig. A.3). Some caution was necessary for

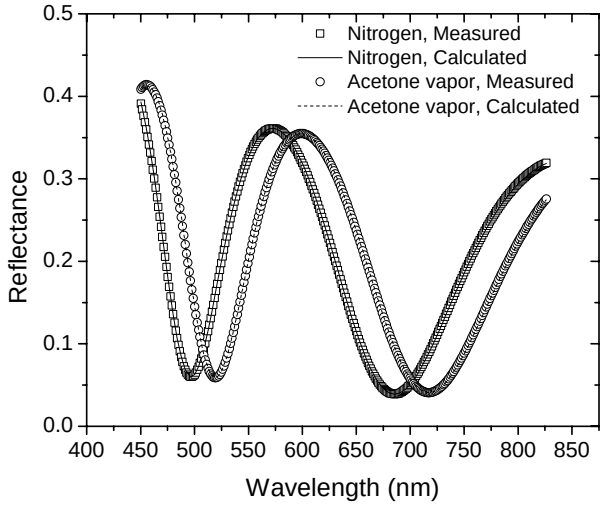


Figure A.3. Measured and fitted reflectance spectra of a PVK/PBD film on silicon in nitrogen (squares) and in acetone vapor (120 torr, 20 °C) (circles). The best 4-parameter fit to the reflectance spectrum in nitrogen corresponds to t_f = 536 nm, A = 1.58, B = 6980 nm^2, and C = 8.05x10^8 nm^4, and in acetone vapor t_f = 567 nm, A = 1.56, B = 7140 nm^2, and C = 8.14x10^8 nm^4. From Brent Bollman.

thin films (<80 nm for PVK/PBD) in which the number of extrema in the reflectance spectrum was not sufficient for unique determination of all parameters. In these cases, *A*, *B*, and *C* calculated from measurements of thicker PVK/PBD layers under similar conditions were used to ensure an accurate determination of t_f. Upon exposure of the film to solvent vapor, the film absorbs the vapor, causing an increase in t_f and decrease in n_f that can be measured by the change in the reflectance spectrum (Fig. A.3). Exposure of a bare silicon wafer to solvent vapor caused no change in the reflectance, so all changes under solvent vapor were due to changes in the polymer.

Measurements of the increase of PVK/PBD thickness at saturated vapor pressure for several different solvents were taken in small-volume chambers (60-1000 cm^3) by placing a small quantity of the solvent in the nearly closed chamber and allowing the solvent to partially evaporate over a long period of time (10 - 40 minutes) at room temperature. The thickness increases are plotted versus the solvents' Hildebrand solubility parameters in Figure A.4. Hildebrand solubility parameters are derived from the square root of the cohesive energy density of the solvent and provide a simple estimate of their relative solvency behaviors [18]. The trend depicted in Figure A.4 resembles the observed solvency behavior of PVK, with the saturated vapor of chloroform (which readily dissolves PVK) yielding the highest thickness increase of 48%. The rest of the measured solvents do not dissolve PVK and correspondingly have lower thickness increases that decrease in magnitude for solubility parameters that are increasingly dissimilar to that of chloroform. Because PVK is soluble in chloroform, the film thickness in saturated chloroform vapor should theoretically increase without limit as chloroform condenses into solution in the film. Although some instability in the thickness of the film in chloroform vapor was observed, the thickness remained finite, suggesting that the actual chloroform partial pressure may have remained slightly below the saturation pressure. The instability of the PVK/PBD thickness in chloroform due to its strong solvency behavior led us to choose acetone, which does not dissolve PVK but still had a relatively large thickness increase, as a candidate for more detailed study.

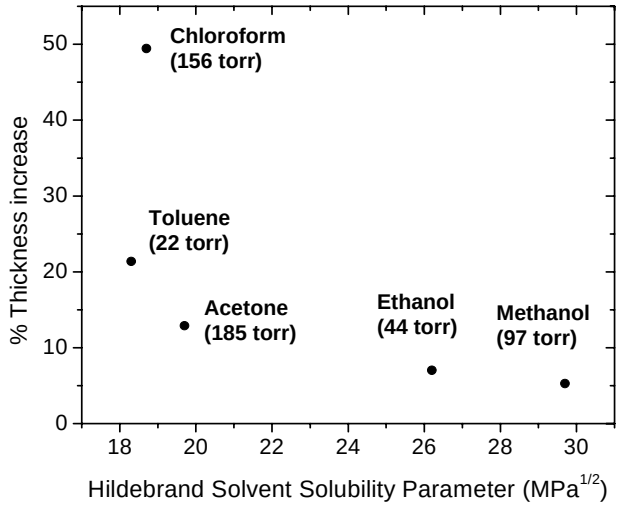


Figure A.4. PVK/PBD thickness increase in various solvents at saturated vapor pressures at 20 °C.

For measurements at different acetone partial pressures and sample temperatures, PVK/PBD films were placed in a chamber consisting of a temperature-controlled sample stage mounted in a glass cylinder connected to a gas supply and exhaust (Fig. A.5). The partial pressure of the solvent vapor in the gas supply was varied by mixing pure nitrogen with nitrogen bubbled through a wash bottle containing liquid solvent. This wash bottle was kept in a water bath to maintain a constant temperature as the solvent evaporated. Partial pressures were calculated by

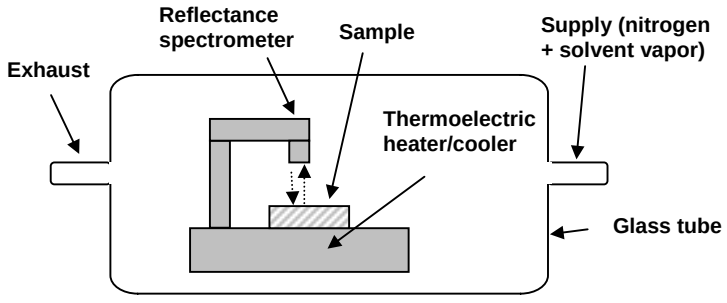


Figure A.5. Schematic of experimental apparatus used for dye diffusion at different sample temperatures and solvent vapor partial pressures. A Filmetrics F20 reflectance spectrometer was used for *in situ* measurement of the polymer thickness.

measuring the amount of liquid solvent evaporated and the nitrogen flow rate.

Figure A.6 shows how the thickness of a PVK/PBD film changes upon exposure to solvent vapor at room temperature. Initially a thickness of 91 nm was measured in a flow of dry nitrogen. Acetone vapor (~120 torr) was then added to the nitrogen and the thickness of the film rapidly increased to 99 nm. After 5 minutes, the acetone vapor was removed and the film returned to its original thickness as it was dried by the flow of pure nitrogen. Fitting the increase and decrease of the thickness vs time with an exponential function yields time constants of 79 s and 255 s, respectively. A rough estimate of the time constant is determined by dividing the chamber volume (8.6 L) by the gas flow rate (~ 4 L/min for each case) to obtain 130 s, which shows that a large part of the time constants are simply due to gas residence times and not to delays in the uptake of the solvent. The discrepancy between the experimental time constants for increasing and decreasing thickness (79 s and 255 s) and the estimated time constant (130 s) is not completely understood. The likely reason for the increased time constant during desorption is that during desorption the polymer surface is relatively depleted of the solvent. As will discuss in Section A.4, a lower solvent concentration reduces the diffusion constant of species within the polymer, so that it is more difficult for solvent in the bulk of the film to diffuse to the surface and evaporate [19]. During adsorption, the solvent concentration is relatively high at the surface, so this effect is

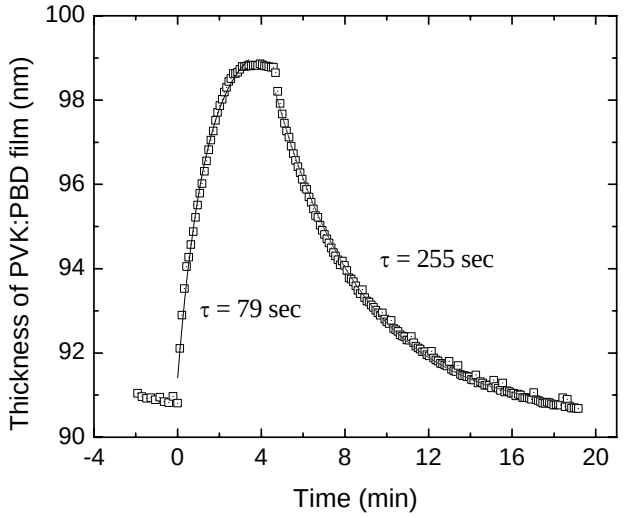


Figure A.6. Time dependence of PVK/PBD swelling upon exposure to acetone vapor (120 torr) in nitrogen at 0 minutes, followed by drying in pure nitrogen after acetone vapor was turned off at 5 minutes. From Hongzheng Jin.

not observed.

That much of the time constants are due to the gas dynamics was further confirmed by an experiment using a much smaller (34 cm^3) volume where only the thickness-increase time constant was measured. Using this smaller volume, a time constant of 1 s was observed, confirming that gas mixing in the larger chamber dominates the measured time constants.

Further measurements of film thickness increases under various conditions were taken by waiting for 5 minutes after solvent vapor exposure to ensure that the film had reached equilibrium. At room temperature (19 ºC), the equilibrium increase in PVK/PBD thickness was roughly linear with respect to acetone partial pressure up to 130 torr, where its thickness increase was 8% (Fig. A.7(a)). Similar trends were observed at higher (45 ºC) and lower (10 ºC) temperatures. Interestingly, the thickness increase in the PVK/PBD film becomes larger at lower sample temperatures (for a constant acetone vapor pressure), and a roughly inverse dependence on temperature was measured (Fig. A.7(b)). Qualitatively, this inverse temperature

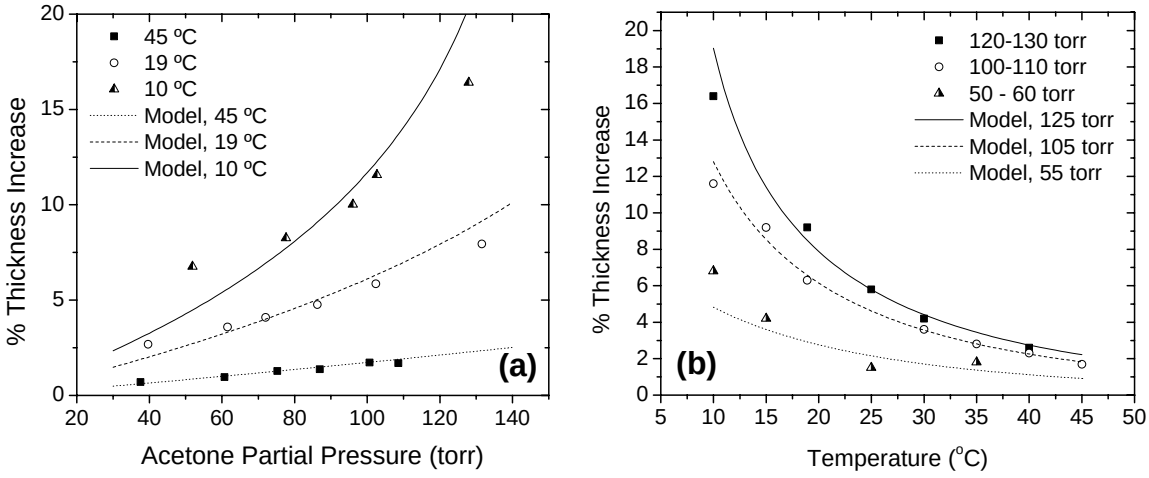


Figure A.7. (a) Experimental and modeled PVK/PBD thickness increases plotted vs acetone partial pressure for several different sample temperatures. (b) Experimental and modeled PVK/PBD thickness increases plotted vs sample temperature for different acetone partial pressures. Due to the difficulty in maintaining a constant partial pressure, each experimental partial pressure corresponds to a range of 10 torr. Dry film thickness ranged from 80 – 100 nm. The model contains one adjustable fitting parameter: the Flory-Huggins interaction parameter χ, set equal to 1.53 for all the calculations shown. Data at partial pressures other than 120-130 torr are from Brent Bollman.

dependence is due to the solvent's tendency to evaporate from the PVK/PBD film at elevated temperatures, where its saturation vapor pressure is higher. Over the pressure and temperature range shown in Fig. A.7, the polymer could be returned to its original thickness by removing the acetone vapor and drying with nitrogen.

As the polymer film absorbed acetone vapor, its index of refraction decreased. This decrease was roughly uniform over the 450-850 nm range that we studied, and is shown in Fig. A.8 for an acetone vapor pressure of 120 torr at 19 °C, corresponding to a film thickness increase of 7%. A decrease in index of refraction is expected as acetone (with a low *n*) is absorbed into the higher-*n* film and is modeled in the next section.

We should note that despite considerable effort, we observed that the measured thickness change could vary significantly (up to even a factor of two) when similar experiments were conducted months apart. This variation may be due to changes in the temperature calibration, adjustments in the experimental apparatus, variations in the acetone temperature (and evaporation rate), leaks in the chamber apparatus, or perhaps heating from absorption of the white light source used in the reflectometry measurements. The problem was especially severe for acetone partial pressures near the saturated vapor pressure and low temperatures (<10 °C), which led

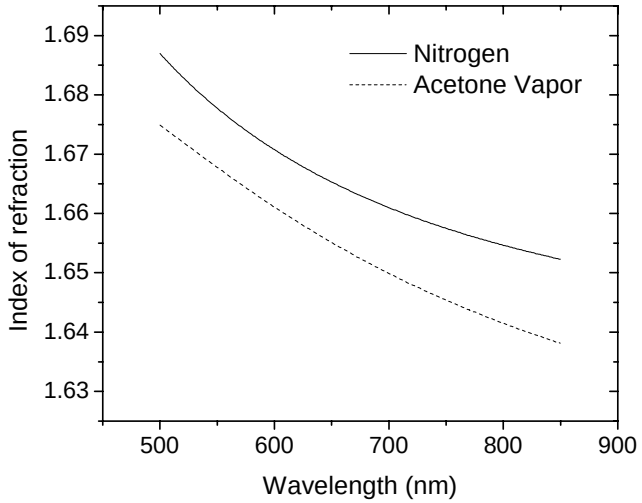


Figure A.8. Index of refraction vs wavelength for PVK/PBD in pure nitrogen (solid line) and during exposure to acetone vapor (120 torr) (dashed line) at 19 °C (thickness increase of 7%, from 89 nm to 95 nm). The addition of acetone, with a lower *n*, decreases n_f of the film. From Brent Bollman.

to large solvent absorption and thickness increases (up to 30%). In some cases near the saturated vapor pressure, large and irreversible increases in film thickness were measured, along with significant roughening of the polymer layer. Micrographs of the roughened polymer layers indicated that some crystallization of the PBD had occurred (the PVK is atactic and cannot crystallize). The possibility of PBD crystallization led us to generally restrict measurements to film thickness increases below 15%. To examine the possibility of other changes in the microstructure of the PVK/PBD film caused by lesser solvent vapor exposures, cathodes (1:10 Mg:Ag to a thickness of 50 nm, followed by 50 nm of Ag) were deposited by thermal evaporation onto PVK/PBD devices (with C6 present in the spun-on film) after exposing the PVK/PBD/C6 layer to acetone vapor (120 torr for 10 minutes at 19 °C, corresponding to a thickness increase of ~10%). The forward-bias and electroluminescent characteristics of devices exposed to acetone vapor remained similar to control devices fabricated without vapor exposure. Because the current-voltage and electroluminescent characteristics of these devices are intimately dependent on the microstructure of the organic layer, this suggests that no significant changes in the PVK/PBD microstructure take place during absorption of solvent vapor for thickness increases below ~15%.

A.3.2 Modeling of the Change in Polymer Index of Refraction and Film Thickness Due to Solvent Vapor

The decrease in index of refraction of the PVK/PBD films upon exposure to acetone vapor (as measured by reflectance spectroscopy and parameter fitting) was modeled by using the Lorentz-Lorenz relationship [20]. In this approximation, the effective index of refraction of the binary mixture (n_f) is related to the indices of refraction n_s and n_p of the solvent and polymer, and the volume fraction ϕ_s of the solvent:

$$\frac{n_f^2 - 1}{n_f^2 + 2} = \phi_s \frac{n_s^2 - 1}{n_s^2 + 2} + (1 - \phi_s) \frac{n_p^2 - 1}{n_p^2 + 2}. \quad (2)$$

The polymer index of refraction n_p for the PVK/PBD blend (with no solvent) was measured to be 1.677 (at λ = 589 nm, corresponding to the D line of sodium) and for n_s the index of refraction of liquid acetone of 1.36 (at 589 nm) was used. The volume

fraction ϕ_s of acetone can be estimated by assuming that it is equal to the measured thickness increase of the PVK/PBD film:

$$\phi_s = \frac{t_{solv} - t_{dry}}{t_{solv}}, \tag{3}$$

where t_{solv} is the thickness in solvent vapor and t_{dry} the original thickness. With these values, the calculated n_f from Eq. (2) agrees very well with n_f obtained by reflectometry over a range of polymer film thickness increases with no adjustable parameters (Fig. A.9). The correspondence between model and data indicates that our assumption that the extra volume of the film is equal to that occupied by acetone at its liquid density is reasonable. Furthermore, it gives us confidence that the reflectance spectroscopy and parameter-fitting procedure is yielding correct information on film thickness and index of refraction.

A model was developed to express the PVK/PBD thickness increase as a function of solvent partial pressure and sample temperature. In this model, we first approximate the mixture of high-molecular-weight PVK and small-molecule PBD as a uniform, high- molecular-weight polymer. Flory-Huggins theory [21] can then be used to describe the excess Gibbs free energy (G^E) of the polymer-solvent mixture:

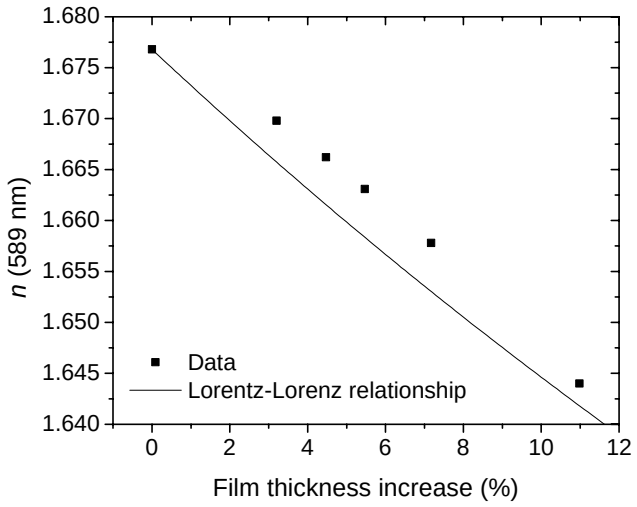


Figure A.9. Measured index of refraction (at λ = 589 nm) for a PVK/PBD film (dry thickness of 100 nm) vs the film thickness change at 17 °C in acetone vapor (partial pressures up to 130 torr) (squares). Also shown is the index of refraction calculated from the Lorentz-Lorenz relationship by using the measured increase in film thickness (with no adjustable parameters) (solid line). From Hongzheng Jin.

$$G^E/RT = (x_s \ln(\phi_s/x_s) + x_p \ln(\phi_p/x_p)) + \chi(x_s + m x_p)\phi_s\phi_p . \quad (4)$$

Here, ϕ_p is the polymer volume fraction, x_s and x_p are the mole fractions of the solvent and polymer in the mixture, R is the ideal gas constant, T is the temperature, and m is the ratio of the polymer molar volume to the solvent molar volume. The Flory-Huggins polymer-solvent interaction parameter, χ, is a parameter that represents the strength of the solvent-polymer interaction. Equation (4) can be used to derive an expression for the solvent activity coefficient (γ_s) from the relation [22]

$$\ln(\gamma_s) = [\frac{\partial(nG^E/RT)}{\partial n_s}]_{P,T,n_p} . \quad (5)$$

Here, n is the total number of molecules in the mixture so that $n_s = x_s n$. Evaluation of Eq. (5) leads to

$$\ln(\gamma_s) = \ln(\phi_s/x_s) + (1 - m^{-1})\phi_p + \chi(\phi_p)^2 . \quad (6)$$

Next, we assume that an equilibrium exists between the composition of the solvent-swollen polymer phase and the solvent vapor phase, and that they can be related by a modified Raoult's Law:

$$P_s = x_s \gamma_s P_s^{sat} , \quad (7)$$

where P_s is the partial pressure of the solvent vapor and P_s^{sat} is the saturated vapor pressure of the solvent. Combining Eqs. (3), (6), and (7) leads to an implicit relationship for t_{solv}:

$$\ln\left(\frac{t_{solv} - t_{dry}}{t_{solv}}\right) + (\frac{t_{dry}}{t_{solv}}) + \chi(\frac{t_{dry}}{t_{solv}})^2 = \ln\left(P_s/P_s^{sat}\right). \quad (8)$$

In obtaining Eq. (8), we make use of the fact that m>>1, so that $m^{-1} \cong 0$. Although in this expression the polymer thickness appears to depend only on χ and the solvent vapor partial pressure P_s, there is an implicit dependence on temperature through P_s^{sat}. P_s^{sat} can be expressed by the Antoine vapor-pressure correlation:

$$P_s^{sat} = \exp[AntA - \frac{AntB}{T + AntC}] \text{ torr}, \quad (9)$$

where for acetone $AntA$ = 16.65, $AntB$ = 2940.46 K, and $AntC$ = -25.93 K [23].

In general, the polymer-solvent interaction parameter χ can depend on both temperature and composition (ϕ_p, ϕ_s) for a given system. However, since the composition dependence is often weak, and only a modest range of temperatures (~35 °C) is employed in our experiments, we determined a single average value of χ = 1.53 by adjusting it to fit Eq. (8) to data at different temperatures and pressures. A higher value of χ corresponds to a weaker polymer-solvent interaction, and for a polymer with high molecular weight χ > 0.5 indicates the existence of a miscibility gap over some composition (ϕ_p, ϕ_s) where a homogeneous solution is not formed [21]. Indeed, acetone will not dissolve the PVK/PBD film, as expected for a value of χ = 1.53. The dependence of polymer swelling on χ is made apparent by taking the exponential of Eq. (8) and expanding the left side for small $t_{solv} - t_{dry}$. To first order in thickness increase $t_{solv} - t_{dry}$ (corresponding to small solvent content ϕ_s << 1) we find

$$\frac{t_{solv} - t_{dry}}{t_{dry}} \cong e^{-(1+\chi)} \frac{P_s}{P_s^{sat}}. \tag{10}$$

This more intuitive relationship indicates that for small polymer swelling, the fractional increase in thickness $\frac{t_{solv} - t_{dry}}{t_{dry}}$ is linear with solvent vapor pressure and depends exponentially on χ. A low χ corresponds to strong solvent-polymer interactions, leading to greater swelling. As noted before, the temperature dependence enters through P_s^{sat}, which increases with temperature according to Eq. (9).

Figures A.7(a) and A.7(b) compare the model (Eq. (6), with χ = 1.53) to the experimentally determined film thickness increases at different acetone partial pressures and sample temperatures. The model, which has only a single fitting parameter χ, matches experimental measurements reasonably well, reproducing the linear dependence of thickness on vapor pressure at low vapor pressures. The dependence on temperature is also well modeled. The predicted thickness increase with vapor pressure is very large at high vapor pressures and low temperatures. This may partially explain the difficulties in reproducing data in this range as noted in the previous section.

A.4 Dye Diffusion

A.4.1 Dye Diffusion Experiments

The absorption of solvent vapor by a polymer film results in a thicker film with greater free volume in which the diffusion of dye molecules is greatly enhanced. In this section we present experimental results for dye diffusion in solvent-swollen polymers.

Dye source plates containing the dye C6 were prepared as described in Section A.2.1. The dye source plate was not patterned in these experiments, although extensive experiments have been done with patterned plates to make multiple regions of different emitting colors on a single substrate. Details of these experiments are reported elsewhere [24].

SIMS measurements presented earlier (Fig. A.2) showed that far more diffusion occurred at room temperature in acetone vapor (90 torr) than at 92 °C without solvent. Straightforward modeling of these curves shows that at room temperature with acetone vapor the C6 diffusion coefficient was > 10^{-13} cm^2/s, while it was ~10^{-17} cm^2/s without solvent vapor at 92 °C.

To observe the optical activity of the dye as a function of depth, a solution of PVK/PBD mixed with the dye coumarin-47 (C47, emission peak at 420 nm, 0.2% by weight) was spun onto a UV-transparent sapphire substrate, resulting in a film with C47 (a blue-emitting dye) distributed uniformly throughout the depth of the film. After C6 printing and solvent exposure, the PVK/PBD/C47 films were exposed to UV (254 nm) light either directly or through the sapphire substrate. The resulting PL spectrum was recorded from the side that was illuminated. Each spectrum was normalized to the peak of the C47 signal. The absorption length in PVK/PBD at this wavelength is only 50 nm [16], so the height of the C6 emission peak (relative to the C47 peak) measures the quantity of C6 present in the top portion of the film (for direct UV exposure) or in the bottom portion (for exposure through the substrate).

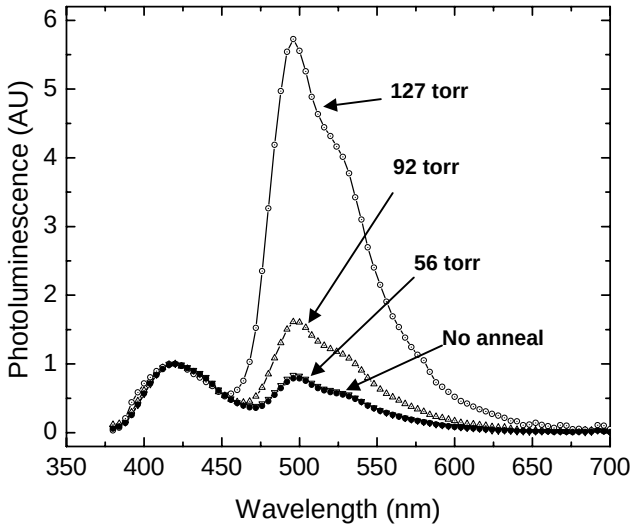


Figure A.10. Photoluminescence spectra of PVK/PBD/C47 samples with printed layer of C6 dye after 10-minute acetone-vapor anneals at different partial pressures at 18 °C. Also shown is an as-printed spectrum, which is indistinguishable from the 56-torr spectrum. All spectra have been normalized to the C47 emission peak at 420 nm. From Hongzheng Jin.

The PL spectra of PVK/PBD/C47 samples (with printed C6 layer) before and after acetone anneals at various partial pressures are shown in Fig. A.10. Each sample was held at 18 ºC during the 10-minute acetone-vapor exposure, and then illuminated from the front by a UV source to obtain the PL spectra. Initially C6 emission is minimal, which indicates that the C6 is primarily on the polymer surface, making it inactive. Annealing at low partial pressure (56 torr), corresponding to a polymer thickness increase of ~3%, is not sufficient to increase C6 emission. As the partial pressure is raised to 92 torr (~5% thickness increase) or 127 torr (~9% increase), the C6 is able to diffuse into the polymer and the C6 emission peak is enhanced dramatically.

Similar results are obtained when the sample temperature is varied and the acetone partial pressure (120 torr) is kept constant (Fig. A.11). In this measurement, PL spectra were obtained by illuminating the sample through the UV-transparent substrate. Each spectrum is therefore dominated by dye present in the bottom of the film. As in the PL from the top surface in Fig. A.10, the anneal at 35 °C (~3% thickness increase) is not sufficient to diffuse dye into the film and increase the magnitude of the

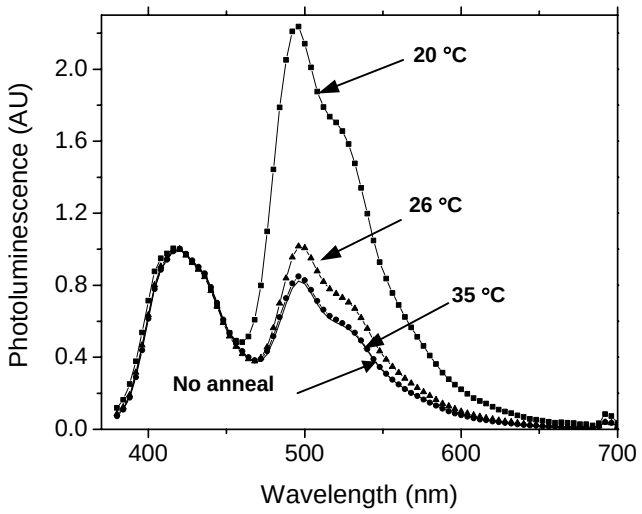


Figure A.11. Photoluminescence spectra of PVK/PBD/C47 films (illuminated through the sapphire substrate) that have been annealed in acetone vapor (120 torr) for 10 minutes at different sample temperatures after dye printing. Also shown is an as-printed spectrum, which is indistinguishable from the 35 °C spectrum. All spectra have been normalized to the C47 emission peak.

C6 peak relative to the as-printed value. However, lower temperatures of 26 °C and 20 °C, corresponding to 6% and 10% thickness increases, result in enhanced dye diffusion to the bottom of the film as reflected by the increase of the C6 peak. This data confirms that solvent vapor can greatly increase the dye diffusion, and, most surprisingly, that in the presence of a solvent vapor, more diffusion occurs as the temperature is lowered.

SIMS measurements (done at Evans East Laboratories, West Windsor, NJ) on similarly treated samples were used to confirm this trend. Figure A.12 plots sulfur (C6) profiles in 90-nm PVK/PBD samples as-printed and after 2-minute anneals at 35 °C and 19 °C (acetone partial pressure = 120 torr). It is evident that the 35 °C (~4% thickness increase) anneal leads to minimal dye diffusion into the film, while the 19 °C anneal (~10 % thickness increase) leads to a uniform dye distribution throughout the layer in only a few minutes. We note that other workers who also employed a dye diffusion process in solvent vapor observed a more conventional trend of increased diffusion at elevated temperatures [6]. In their work, dye source and target films were exposed to solvent vapor and then placed in contact and heated (using relatively high

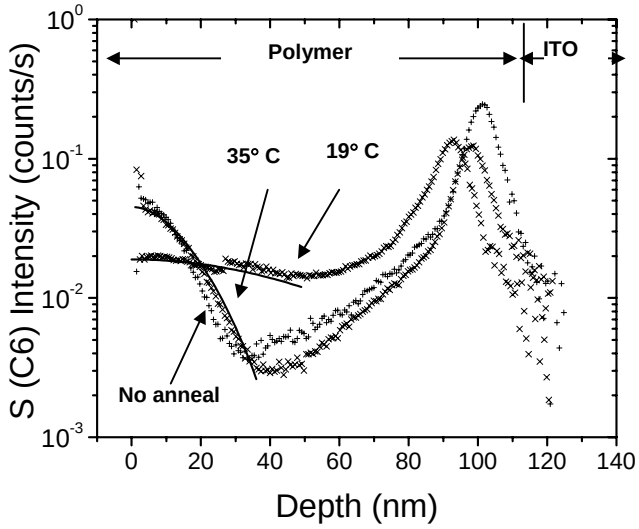


Figure A.12. SIMS analysis of PVK/PBD films following printing of C6 dye and 2-minute acetone vapor (120 torr) anneals at 19 °C and 35 °C. The sulfur-signal rise in two samples starting at a depth of 50 nm is thought to be O_2 from the substrate. Also shown are fits to the 19 °C and 35 °C anneals derived from numerical modeling of the C6 diffusion (solid lines); the fits correspond to diffusion coefficients of 5 x 10^{-13} cm^2/s and 3 x 10^{-15} cm^2/s, respectively.

temperatures of 80-200 °C) to transfer and diffuse the dye while maintaining the solvent vapor atmosphere. The contact between the dye and source plates may have limited solvent evaporation at elevated temperatures, leading to a trend opposite to that observed in our work.

Dye diffusion coefficients were estimated from the SIMS data by numerical modeling. Constant diffusion from a finite plane source was assumed.[1] Fits to the 19 °C and 35 °C anneals in solvent vapor are shown in Fig. A.12. Due to the uncertainty in the as-printed and annealed profiles caused by the "knock-on" effects during SIMS

[1] The assumption of a constant diffusion coefficient implies that there is a stable, uniform concentration of acetone already present in the film. Measurements of the time dependence of the PVK/PBD thickness increase upon exposure to acetone vapor (Section A.3) indicate that the acetone does indeed diffuse rapidly throughout the film (on time scales of less than 1 s). However, in the large-volume chamber used in the diffusion experiments, a larger thickness-increase time constant of 79 s was measured due to the longer time necessary for the acetone vapor to reach equilibrium pressure. The assumption of constant diffusion is therefore not entirely justified. This leads to some additional error in the estimate of the dye diffusion coefficient but the predominant source of error is the uncertainty in the initial and final dye profiles.

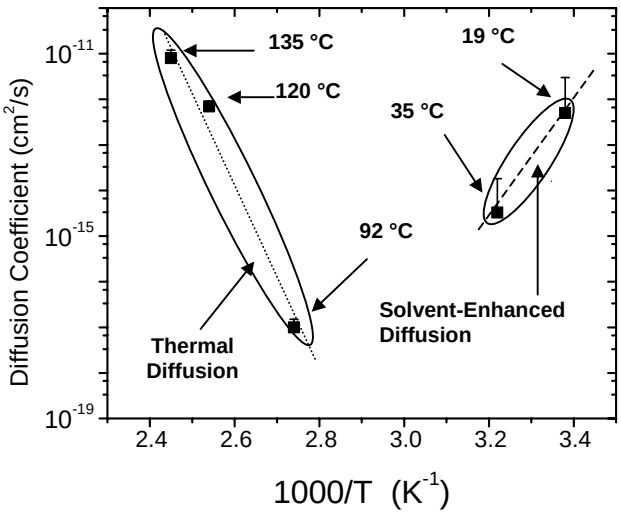


Figure A.13. Diffusion coefficients of C6 in PVK/PBD vs inverse temperature for thermal diffusion and solvent-enhanced diffusion (acetone vapor, 120 torr).

measurement discussed in Section A.2, the absolute error in diffusion coefficients could be as large as a factor of 5. The diffusion coefficients are plotted in Fig. A.13, along with diffusion coefficients from thermally-annealed samples [13]. The enhancement of diffusion by acetone vapor is enormous. If the thermal diffusion coefficients from the 90-130 °C are extrapolated to 20 °C, we would expect a diffusion coefficient of ~10^{-30} cm^2/s, which is nearly 10^{18} times less than solvent-enhanced diffusion at the same temperature. Furthermore, in the presence of the solvent vapor, the dye diffusion decreases as the temperature is increased, a most peculiar circumstance. This occurs because the solvent effect is so pronounced. At higher temperatures, the film absorbs less solvent, as discussed in Section A.3. The resulting decrease in solvent-enhanced diffusion at higher temperatures more than offsets the relatively smaller increase in conventional thermal diffusion.

A.4.2 Dye Diffusion Discussion

Diffusion of small molecules in polymers is generally characterized by two regimes. At low temperatures, the polymer film is in a glassy state with very limited diffusion. As the polymer is heated above a certain temperature (T_g), it enters a rubbery state and diffusion is rapidly increased. Conceptually, the diffusion of

molecules into a polymer film requires the existence of voids into which the molecules can move. Above T_g, polymer relaxation processes are relatively quick, leading to the ready formation of voids and rapid diffusion of small molecules [25]. Below T_g, these relaxation processes require long time scales, which limits the amount of free volume available for diffusion. From Section A.2.2, the PVK/PBD blend (100:40 by weight) (with no solvent present) has been measured to have a T_g = 120 °C . This indicates that process temperatures greater than 120 °C are desirable to diffuse dye into this blend; however, these temperatures are sufficient to cause significant degradation of the PVK. Lowering T_g is therefore preferable to raising T.

The introduction of acetone into the PVK/PBD blend has the effect of lowering the effective glass transition temperature, $T_{g,eff}$ of the film. It is well known that T_g of a polymer can be changed by mixing it with a material having a different T_g. The Fox equation [26] can be used to estimate $T_{g,eff}$ of a blend with components having mass fractions w_i and glass transition temperatures T_{gi}:

$$\frac{1}{T_{g,eff}} = \sum_i \frac{w_i}{T_{gi}}. \tag{11}$$

A common approximation is to estimate T_g of a solvent as two-thirds its melting temperature [27]. For acetone, the melting temperature is 178 K, so that T_g ~ 120 K. $T_{g,eff}$ of the solvent-swollen polymer blend can be estimated by assuming that the measured thickness increase is equal to the volume of acetone present in the film (as was confirmed by modeling the change in index of refraction in Section A.3.2). For example, an increase of thickness of 10% in acetone vapor implies an acetone volume fraction of 0.1/1.1 = 0.09, and a PVK/PBD volume fraction of 1/1.1 = 0.91. The densities of acetone (~0.8 g/cm^3) and PVK and PBD (both ~1.2 g/cm^3) are used to convert these volume fractions into weight fractions; we can then use Eq. (11) to find a decrease in T_g of the PVK/PBD blend of 50 °C.

We call the glass transition temperature of the mixture (polymer and solvent) an effective glass-transition temperature $T_{g,eff}$. This is because it is not actually possible to raise the temperature of the mixture in practice to reach this lowered $T_{g,eff}$ because as the temperature is raised the solvent uptake decreases, thus increasing $T_{g,eff}$. Defining a lower $T_{g,eff}$ for the films is still a useful concept, however, because $T_{g,eff}$ represents the increased free volume which enables dye diffusion, so that ($T - T_{g,eff}$) should correlate with the enhanced diffusion.

Figure A.14(a) shows $T_{g,eff}$ calculated from Eq. (11) as a function of vapor pressure for temperatures of 10 °C, 19 °C, and 45 °C (using data from Fig. A.7). Although the decrease in $T_{g,eff}$ is minimal at 45 °C, at a lower temperature of 19 °C $T_{g,eff}$ can be reduced by 40 degrees to 80 °C, while at a temperature of 10 ºC, it can be reduced by up to 70 degrees to lower $T_{g,eff}$ to 50 °C.

In Fig. A.14(b), the difference between the process temperature and the effective glass transition temperature (T- $T_{g,eff}$) is plotted as a function of temperature for different acetone vapor pressures. In all cases, T_g remains well above the process temperatures (implying that the polymer remains in a glassy state), yet still we know experimentally that extensive diffusion can occur. For quantitative modeling of D, a

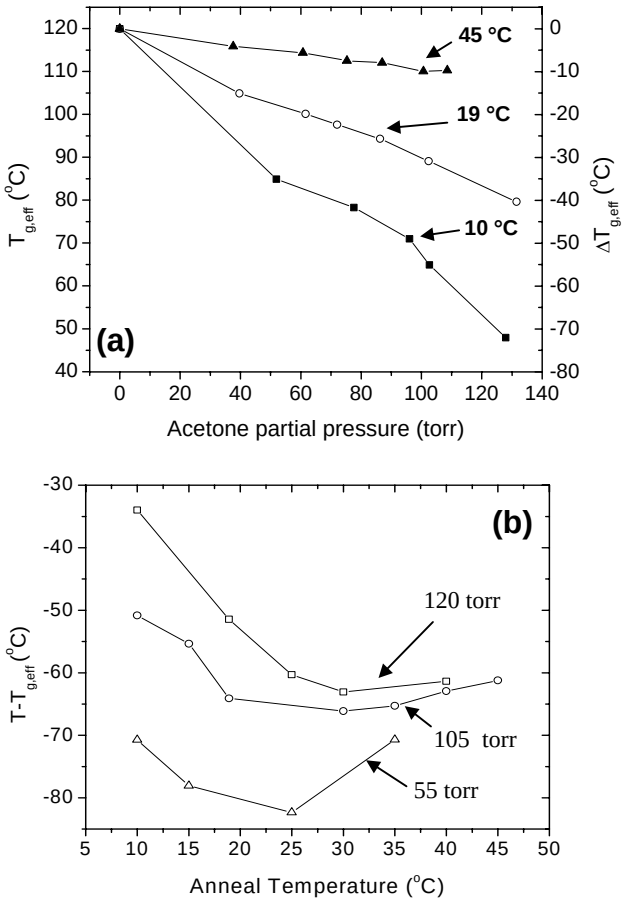


Figure A.14. (a) Calculated effective glass transition temperature $T_{g,eff}$ of PVK/PBD film (based on measured thickness increase) as a function of acetone partial pressure for various annealing temperatures. (b) T-$T_{g,eff}$ as a function of T for various acetone partial pressures.

diffusion model that is valid for $T < T_{g,eff}$ would be necessary. Although several models for diffusion above and around T_g have been proposed [28-33], diffusion in glassy polymers is complicated and difficult to model quantitatively [34]. Nevertheless, it is clear that reducing $T_{g,eff}$ of the polymer film to approach the process temperature leads to dramatically enhanced diffusion. This dependence of dye diffusion on (T- $T_{g.eff}$) is illustrated by the trends depicted in Fig. A.14(b). Here, (T- $T_{g.eff}$) is highest at low sample temperature, where the decrease in $T_{g,eff}$ due to enhanced absorption of solvent vapor more than offsets the relatively low temperature. (T- $T_{g.eff}$) actually decreases as T is raised to ~35 °C due to evaporation of the solvent, and then begins to increase slightly as negligible amounts of solvent absorption occur and the system enters a normal, thermally-activated diffusion regime. This plot correctly explains the observed dye diffusion trend, which in contrast to conventional diffusion is highest at low temperatures, where (T- $T_{g.eff}$) is largest.

A.5 Summary

Through exposure to solvent vapor, the diffusion of printed dye on a polymer surface through the film can be completed at room temperature. Thus thermal damage to the active polymer can be avoided while still employing a polymer layer with a high T_g for device stability. The enhancement of the dye diffusion in acetone vapor is dependent on the amount of solvent vapor absorbed by the polymer, which causes it to increase its thickness. This thickness increase is largest at low temperatures and high solvent vapor pressures and can be modeled based on Flory-Huggins theory. The absorbed solvent increases the dye diffusion coefficient by many orders of magnitude. At high acetone partial pressures and/or low sample temperatures, diffusion times of only a few minutes were necessary to diffuse C6 dye throughout a 100-nm polymer layer. This enhancement is attributed to the reduction of $T_{g,eff}$ of the PVK/PBD blend as it absorbs acetone vapor, although it appears that lowering $T_{g,eff}$ to the process temperature (near room temperature) was not necessary.

References

[1] T. Graves-Abe, F. Pschenitzka, H. Z. Jin, B. Bollman, J. C. Sturm and R. A. Register, "Solvent-Enhanced Dye Diffusion in Polymer Thin Films for Polymer Light-Emitting Diode Application" *Journal of Applied Physics* **96** (12), 7154-7163 (2004).

[2] G. Parthasarathy, J. Liu and A. R. Duggal, "Organic Light Emitting Devices: From Displays to Lighting" *The Electrochemical Society Interface* **12** (2), 42-47 (2003).

[3] A. Nakamura, T. Tada, M. Mizukami, S. Hirose and S. Yagyu, "Three-Color Polymer Light-Emitting Diodes by Stamped Dye Diffusion" *Applied Physics Letters* **80** (12), 2189-2191 (2002).

[4] F. Pschenitzka and J. C. Sturm, "Three-Color Organic Light-Emitting Diodes Patterned by Masked Dye Diffusion" *Applied Physics Letters* **74** (13), 1913-1915 (1999).

[5] K. Tada and M. Onoda, "Three-Color Polymer Light-Emitting Devices Patterned by Maskless Dye Diffusion onto Prepatterned Electrode" *Japanese Journal of Applied Physics Part 2-Letters* **38** (10A), L1143-L1145 (1999).

[6] C. C. Wu, S. W. Lin, C. W. Chen and J. H. Hsu, "Solvent-Assisted Dye-Diffusion Thermal Transfer for Electronic Imaging Applications" *Applied Physics Letters* **80** (7), 1117-1119 (2002).

[7] J. Bharathan and Y. Yang, "Polymer Electroluminescent Devices Processed by Inkjet Printing: I. Polymer Light-Emitting Logo" *Applied Physics Letters* **72** (21), 2660-2662 (1998).

[8] S. C. Chang, J. Bharathan, Y. Yang, R. Helgeson, F. Wudl, M. B. Ramey and J. R. Reynolds, "Dual-Color Polymer Light-Emitting Pixels Processed by Hybrid Inkjet Printing" *Applied Physics Letters* **73** (18), 2561-2563 (1998).

[9] T. R. Hebner, C. C. Wu, D. Marcy, M. H. Lu and J. C. Sturm, "Ink-Jet Printing of Doped Polymers for Organic Light Emitting Devices" *Applied Physics Letters* **72** (5), 519-521 (1998).

[10] C. F. Madigan, T. R. Hebner, J. C. Sturm, R. A. Register and S. Troian, "Lateral Dye Distribution with Ink-Jet Dye Doping of Polymer Organic Light Emitting Diodes" in *Materials Research Society Symposium Proceedings* **624**, San Francisco, CA, USA, 211-16 (2000).

[11] F. Pschenitzka and J. C. Sturm, "Solvent-Enhanced Dye Diffusion in Polymer Thin Films for Color Tuning of Organic Light-Emitting Diodes" *Applied Physics Letters* **78** (17), 2584-2586 (2001).

[12] S. Shirai and J. Kido, "Fabrication of Multi Color Polymer El Devices Using the Photo-Bleaching Method" *Journal of Photopolymer Science and Technology* **14** (2), 317-22 (2001).

[13] F. Pschenitzka and J. C. Sturm, "Patterned Dye Diffusion Using Transferred Photoresist for Polymer Oled Displays" *Proceedings of the SPIE - The International Society for Optical Engineering* **4105**, 59-68 (2001).

[14] C. C. Wu, J. C. Sturm, R. A. Register, J. Tian, E. P. Dana and M. E. Thompson, "Efficient Organic Electroluminescent Devices Using Single-Layer Doped Polymer Thin Films with Bipolar Carrier Transport Abilities" *IEEE Transactions on Electron Devices* **44** (8), 1269-1281 (1997).

[15] F. Pschenitzka, K. Long and J. C. Sturm, *Mat. Res. Soc. Symp. Proc.* **665**, C9.5.1 (2001).

[16] J. M. Pearson and M. Stolka, *Poly(N-Vinyl Carbazole)*. 1981, New York: Gordon and Breach.

[17] O. Heavens, *Optical Properties of Thin Solid Films*. 1965, New York: Dover Publications.

[18] J. Brandrup and E. H. Immergut, *Polymer Handbook*. 1989, Wiley: New York.

[19] R. A. Register, Personal Communication (2004).

[20] P. Brocos, A. Pineiro, R. Bravo and A. Amigo, *Physical Chemistry Chemical Physics* **5**, 550 (2003).

[21] P. Flory, *Principles of Polymer Chemistry*. 1953, Ithaca: Cornell University Press.

[22] J. M. Smith and H. C. Van Ness, *Introduction to Chemical Engineering Thermodynamics*. 4th ed. 1987, New York: McGraw-Hill.

[23] R. Reid, J. M. Prausnitz and T. K. Sherwood, *The Properties of Gases and Liquids*. 1987, New York: McGraw-Hill.

[24] K. Long, F. Pschenitzka and J. C. Sturm, "Three-Color Passive-Matrix Pixels Using Dye-Diffusion-Patterned Trilayer Polymer-Based Led" in *Materials Research Society Symposium Proceedings*, Boston, MA, USA, 205-10 (2002).

[25] T. E. Shearmur, D. W. Drew, A. S. Clough, M. G. D. VanderGrinten and A. T. Slark, "Study of Dye Diffusion in Polymers Using Rutherford Backscattering" *Polymer* **37** (13), 2695-2700 (1996).

[26] T. G. Fox, *Bulletin of the American Physical Society* **1**, 123 (1956).

[27] D. W. V. Krevelen, *Properties of Polymers: Their Correlation with Chemical Structure, Their Numerical Estimation and Predictions from Additive Group Contributions*. 3rd ed. 1990, Amsterdam: Elsevier.

[28] M. H. Cohen and D. Turnbull, "Molecular Transport in Liquids and Glasses" *Journal of Chemical Physics* **31** (5), 1164-1169 (1959).

[29] D. Ehlich and H. Sillescu, "Tracer Diffusion at the Glass-Transition" *Macromolecules* **23** (6), 1600-1610 (1990).

[30] H. Fujita, *Fortschr. Hochpolym. Forsch.* **3**, 1 (1961).

[31] J. S. Kim and K. R. Lee, "Prediction of Mutual Diffusion Coefficient in Polymer Solution" *Polymer* **41** (23), 8441-8448 (2000).

[32] J. S. Vrentas and J. L. Duda, "Diffusion in Polymer - Solvent Systems .1. Re-Examination of Free-Volume Theory" *Journal of Polymer Science Part B-Polymer Physics* **15** (3), 403-416 (1977).

[33] M. L. Williams, R. F. Landel and J. D. Ferry, "Mechanical Properties of Substances of High Molecular Weight .19. The Temperature Dependence of Relaxation Mechanisms in Amorphous Polymers and Other Glass-Forming Liquids" *Journal of the American Chemical Society* **77** (14), 3701-3707 (1955).

[34] A. C. Dubreuil, F. Doumenc, B. Guerrier and C. Allain, "Mutual Diffusion in Pmma/Pnbma Copolymer Films: Influence of the Solvent-Induced Glass Transition" *Macromolecules* **36** (14), 5157-5164 (2003).

Appendix B

Additional Experimental Details

In this appendix we provide additional experimental details. Many of the details are specific to the equipment used in rooms C405 and the Princeton Institute for the Science and Technology of Materials (PRISM) cleanroom.

B.1 Thermal Evaporation

The four-source thermal evaporator (purchased from Angstrom Engineering) in C405 was used for all thermal evaporations in this thesis. Base pressures were 10^{-6} torr. Although this system allows the evaporation to be controlled entirely by a computer, we generally allowed the computer to run a pre-conditioning routine but then switched to manual control for the actual evaporation. Additional metal-specific details are shown in Table B.1 Although we specify a typical power, after pre-conditioning it we preferred to slowly increase the evaporation power (by ~1% every 10 s) while monitoring the deposition rate until the desired rate is achieved, then open the sample shutter to allow coating.

Metal	Evaporation program	Typical power	Typical rate (nm/s)	Boat	Metal purity	Metal Vendor
Au	gold s1	~30%	0.01 to 0.5	S42B-AO-W	5N	Williams Advanced Materials
Ti	Ti S2	~40%	0.1 to 0.5	S4-.015W	4N	ESPI
Al	Al source1	~30%	0.05 to 0.5	S9C-.010MO	4N	?

Table B.1. Evaporation program, power, rates, source boat, metal purity, and metal vendor used in thermal evaporations. All boats were purchased from R. D. Mathis Co (Long Beach, CA).

For cooled evaporations, we began cooling the hollow stage with liquid nitrogen after the vacuum reached below 10^{-5} torr. Because of the thin feedthrough tubing, it typically required at least 1 hour before the shallow-angle sample holder and sample reached 100 K. After evaporation, we usually left the sample in the chamber overnight to allow the sample and stage assembly to warm to room temperature (to avoid ice formation on the sample and in the chamber when unloading). Alternatively, a resistive heater on the sample stage (with power source adjacent to the cryopump coldhead) could be used to heat the assembly for quicker sample removal. However, this required great care (as the heater temperature was not controlled automatically so had to be monitored manually). The heater did not heat the liquid nitrogen feedthroughs or tubing, so these had to be heated by blowing house nitrogen through the feedthroughs.

B.2 Electron-Beam evaporation

All e-beam evaporations were carried out in the Denton DV-502A e-beam evaporator in the cleanroom. Source materials and crucibles were provided by cleanroom personnel (primarily Joe Palmer). Base pressures were below 10^{-5} torr. Evaporation rates were specified in the text. The electron-beam currents necessary to achieve these evaporation rates could vary dramatically, depending on the quantity of source material left in the crucible and the type of crucible (for gold, the type of crucible was changed several times over the course of this thesis). For example, although we initially (in 2003 and 2004) evaporated gold at currents of ~50 mA, in 2005 currents as high as 200 mA were required. It was therefore necessary to refer to the logbook before each evaporation to determine the current used by previous users. Finally, we note that very low currents (<15 mA) were usually sufficient for SiO_x evaporations.

B.3 MUA Growth

In addition to the description provided in Chapter 3, we note one additional problem that we encountered when growing MUA on template-stripped (flat) gold substrates. With these substrates, we found that if the samples were left immersed in MUA solution for longer than two to three days, the gold surface began to be coated by a foreign substance, visible in the microscope as a discoloration of the gold (and with a thickness on the order of a micron when measured with a profilometer). Because this

was never observed when growing MUA on regular gold substrates, we hypothesize that the foreign material was epoxy that had been dissolved by the solution and re-deposited (even though the epoxy was expected to be resistant to solvents). We do not think that this foreign material contaminated the gold film prior to its becoming visible in the microscope, as ellipsometric measurements on MUA films on flat and regular gold revealed similar optical constants until the flat gold was visibly contaminated. To avoid contamination of the flat gold samples, we kept the growth time for each MUA layer to only ~2 hours, so that samples as thick as 10 MUA layers could be grown in a time frame of less than two days. With this precaution we did not observe any contamination.

B.4 Plasma (Reactive-ion) Etching

All plasma etching was done with the Plasmatherm 720/SLR in the cleanroom. The following recipe, obtained from Richard Huang, was used to etch silicon (masked by photoresist): 60 sccm SF_6, 15 sccm CCl_2F_2, 100 mT, 200 W. The etch rate was ~500 nm/min (silicon) and <100 nm/min (photoresist).

B.5 Electrical Measurements

As described in Chapter 4, 5, 7, and 8, all room-temperature electrical measurements were done using a probestation located inside a Vacuum Atmospheres glovebox. Three types of needle probes were used. The first was a standard needle probe (0.6 μm radius, Model #72T-H3/06, purchased from Creative Devices Inc, Neshanic Station, NJ). This probe was usually used to contact the bottom gold electrode. To contact the top gold electrode, which was relatively delicate because it was deposited without an adhesion layer (and on a thin SiO_x layer in the PoPI structure), we initially used a “whisker” tip probe (model 7x, purchased from MicroManipulator, Carson City, NV). However this tip still caused damage to the top electrode and could completely destroy it during extended testing. We thus began using a 0.001” gold wire that was wrapped around and soldered to a standard probe. The gold wire was much gentler than the whisker-tip probe and caused no visible damage to the top gold electrode.

B.5.1 Forming of Memory Devices

As discussed in Section 7.3, most memory devices were formed by applying a large voltage to an initially insulating device. However, in some cases with the edge structure, it was not necessary to form devices before we could observe programmable resistance. Alternatively, by applying a large current to initially shorted edge devices, we were sometimes able to place them into a programmable-resistance state.

For some of the initially insulating devices, it was necessary to scan the voltage (typically 0 to 8 V) several times before the devices became programmable and displayed NDR. In some other instances, after application of a forming voltage, devices could still not be programmed, even though they were not shorted (i.e., current densities remained well below the 10^7 A/cm^2 at 1 V common for a shorted device). Upon review of the literature, we found that in inorganic electroformed devices it was sometimes necessary to apply a large voltage (5 to 10 V) for a long period (1 minute to many hours) to cause devices to enter a programmable-resistance state [1]. We tried this technique by applying voltages of 6 to 10 V on devices for periods between 5 to 10 minutes on devices that were not shorted but could not be formed with a simple voltage scan. We had limited success, and about ~25% of the devices that could not be formed with a single voltage scan displayed programmable-resistance and NDR after a longer application of voltage.

B.5.2 Removable-Top-Electrode Memory Devices

Experiments in which we sought to form and program Ag/PVK/Au devices and then remove the top Au electrode for chemical analysis of the PVK were described in Section 8.5.2. Here we provide additional experimental details.

To transfer the gold films from the silicon sample on which they were originally deposited to the top of the PVK film for electrical testing, we used a whisker-tip probe. By poking the gold electrode with this probe, it was possible to cause it to adhere to the probe so that it could be repositioned. The probe and gold electrode were then moved to the silver/PVK sample, and the whisker tip was lowered adjacent to a silver electrode so that the gold electrode overlapped a portion of the silver electrode (Fig. B.1). Because the gold electrode was usually not uniformly flat, a gold wire was gently lowered onto the top of the gold electrode to place it in contact with the PVK film. This gold wire was also used to apply bias to the gold electrode. A third, standard needle

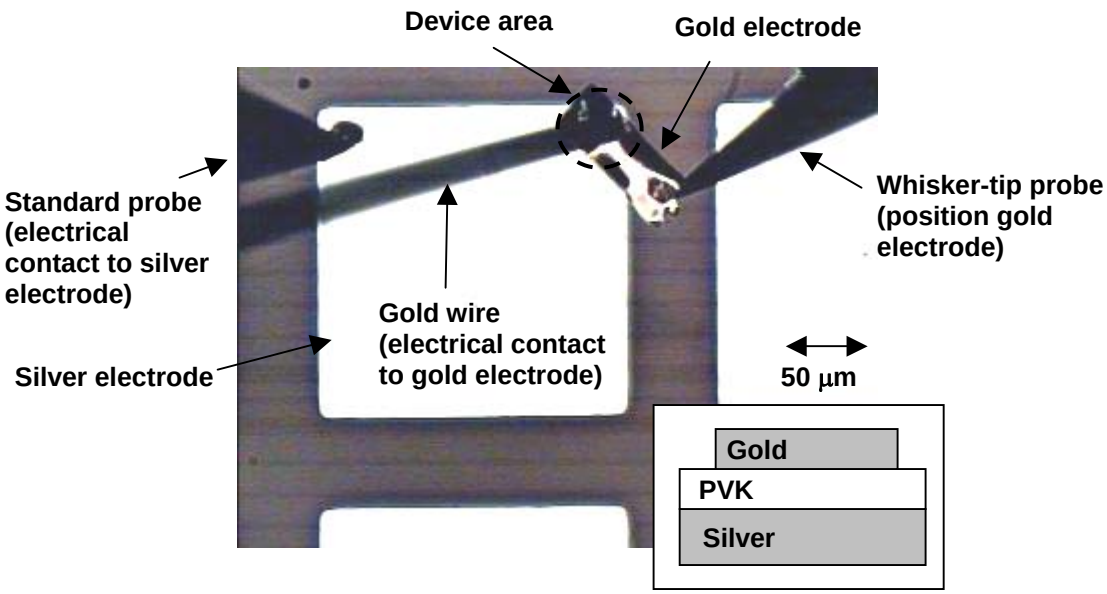


Figure B1. Microscope view of removable-top-electrode device during testing. The top gold electrode adhered to the whisker tip probe, which was used to position it. A gold wire was used to (gently) press the gold wire against the silver/PVK during testing, and apply bias. A standard probe was used to ground the silver electrode.

probe was used to poke through the PVK layer and ground the silver electrode during electrical testing. After testing, the gold wire was removed, and the gold electrode (which was still adhered to the whisker tip) could be repositioned. Devices with a bottom gold electrode and MUA layer (instead of PVK) could be formed and programmed with a similar approach

We could also form and program devices by gently lowering the gold wire until it directly touched the PVK layer (and then applying bias to the gold wire). This approach was in principle more straightforward, but depended on the gold wire being smooth. In some cases, this approach repeatedly resulted in shorted devices, which we attributed to the gold wire having a sharp defect that poked through the thin (~30 nm) PVK layer.

References

[1] A. K. Ray and C. A. Hogarth, "A Critical-Review of the Observed Electrical-Properties of MIM Devices Showing VCNR" *International Journal of Electronics* **57** (1), 1-77 (1984).

Appendix C

Publications and Presentations Resulting from this Work

Journal papers and Refereed Conference Proceedings

Troy Graves-Abe and J. C. Sturm, “Mechanism for Programmable Resistance in a Molecular-Scale Memory Device with Very Large Conductance”, manuscript in preparation.

Troy Graves-Abe and J. C. Sturm, “Fabrication of Organic Self-Assembled Multilayer Devices with a Vacuum-Evaporated Top Electrode”, manuscript in preparation.

Troy Graves-Abe and J. C. Sturm, “Programmable Organic Thin-Film Devices with Extremely High Current Densities” *Applied Physics Letters* **87**, 133502 (2005).

Troy Graves-Abe and J. C. Sturm, “Programmable Conductance Switching and Negative Differential Resistance in Nanoscale Organic Films” Mat. Res. Soc. Symp. Proc. **871E**, I9.34 (2005).

Troy Graves-Abe, Florian Pschenitzka, H. Z. Jin, Brent Bollman, J. C. Sturm and R. A. Register, “Solvent-enhanced dye diffusion in polymer thin films for polymer light-emitting diode application” *Journal of Applied Physics* **95** p. 7154 –7163 (2004).

Troy Graves-Abe, Zhenan Bao, and J.C. Sturm, “Self-Aligned, Insulating-Layer Structure for Integrated Fabrication of Organic Self-Assembled Multilayer Electronic Devices” *Nano Letters* **4** p. 2489-2492 (2004).

Troy Graves-Abe, F. Pschenitzka, and J.C. Sturm, "Anomalous temperature dependence in solvent-enhanced dye diffusion in polymer films" *Mat. Res. Soc. Symp. Proc.* **725**, P3.1.1 (2002).

Conference Presentations

Troy Graves-Abe and J. C. Sturm, "Conductance Requirements for Arrays of Organic Programmable-Resistance Memory Devices” submitted to Mat. Res. Soc. Symp., San Francisco, CA, April 2005

J. C. Sturm and Troy Graves-Abe, “Reversible Electrically-Programmable Organic Memory from Self-Assembled Polymer Monolayers” submitted to Mat. Res. Soc. Symp., San Francisco, CA, April 2005 (invited).

Troy Graves-Abe and J. C. Sturm, “Physical Mechanisms in Programmable Nanoscale Organic Nonvolatile Memory Devices**”** American Vacuum Society 52nd International Symposium, Boston, MA, November 2005.

Troy Graves-Abe and J. C. Sturm, “Dynamics of Write and Erase Mechanisms in a Novel Nonvolatile Organic Memory With Extremely Low ON Resistance” Device Research Conference, Santa Barbara, CA, June 2005.

Troy Graves-Abe and J. C. Sturm, “Programmable Conductance Switching and Negative Differential Resistance in Nanoscale Organic Films” Mat. Res. Soc. Symp., San Francisco, CA, April 2005.

Troy Graves-Abe, Zhenan Bao, and J. C. Sturm, “Electrical Transport Through Self-Assembled Multilayers of a Mercaptoalkanoic Acid in a Self-Aligned Structure for Low Parasitic Leakage” Mat. Res. Soc. Symp., Boston, MA, December 2003.

J. C. Sturm, Ke Long, Troy Graves-Abe, F. Pschenitzka, “Physics and Technology of Patterned Dry Dye Printing for Full Color OLED Integration” SID/MAC OLED Research and Technology Conference, Princeton, NJ, October 2002.

Troy Graves-Abe, F. Pschentizka, and J.C. Sturm, "Anomalous temperature dependence in solvent-enhanced dye diffusion in polymer films" Mat. Res. Soc. Symp., San Francisco, CA, April 2002.

Patent Applications

Z. Bao, J. Zheng, J.C. Sturm, T. Graves-Abe, “Forming Closely Spaced Electrodes” Application # 20050014357, Filed March 18, 2004 serial # 803244,