# ADVANCED SILICON-BASED MATERIALS AND DEVICES USING CHEMICAL VAPOR DEPOSITION

**XIANG-ZHENG BO**

A DISSERTATION

PRESENTED TO THE FACULTY

OF PRINCETON UNIVERSITY

IN CANDIDACY FOR THE DEGREE

OF DOCTOR OF PHILOSOPHY

RECOMMENDED FOR ACCEPTANCE

BY THE DEPARTMENT OF

ELECTRICAL ENGINEERING

November 2004

The fear of the LORD is the beginning of knowledge.

PROVERB  1: 7

# ABSTRACT

Novel silicon-based materials ($a$-Si, poly-Si, SiGe) based on chemical vapor deposition have been used to fabricate poly-Si thin film transistors (TFTs), and Si three-dimensional photonic bandgap crystals, and SiGe single-hole transistors.

Polysilicon films created by solid-phase crystallization of $a$-Si are of great interest. The low transport mobility of poly-Si TFTs relative to single-crystalline Si MOSFETs is due to scattering from grain boundaries and intragranular defects in poly-Si films. To remove grain boundaries, we used a hydrogen plasma treatment of an $a$-Si film through an opening hole ($\leq 0.6$ μm in diameter). Subsequent anneals at 600 °C lead to a single-grain silicon film in the hole. By removing the underlying $SiO_2$ of $a$-Si film, the intra-grain defect density in poly-Si was reduced by one-order of magnitude from $\sim 10^{11}$ cm$^{-2}$ to $\sim 10^{10}$ cm$^{-2}$. These improvements are thought to be able to improve the electrical performance of poly-Si TFTs.

Photonic crystals prohibit light propagation in a specific wavelength range. 3-D periodic face-centered-cubic structures made of $SiO_2$ spheres by self-assembly cannot form a photonic bandgap. We used $a$-Si chemical vapor deposition and wet chemical etching to successfully invert the periodic structures from $SiO_2$/air into air/Si with a relatively higher refractive index contrast. The key deposition condition is the extremely low partial pressure of $SiH_4$ gas, which leads to a long mean free path of Si atoms and conformal growth on silica spheres. Unity reflectance occurs at a wavelength of 1.3 μm in <100> and <111> directions.

The usefulness of Si-based quantum dot devices is limited by the existence of defect states related to the $SiO_2$ passivation, resulting in irreproducible and undesired characteristics. A new nanopatterning technique of Si/SiGe heterostructures based on the AFM local oxidation and selective wet etching has been developed to fabricate SiGe quantum dot devices. To remove the negative effects of $SiO_2$, the surface of patterned SiGe dots was passivated by silicon epitaxial regrowth with in-situ hydrogen pre-baking

at $T \leq 800$ °C.  The regrowth interface was epitaxial, characterized by SIMS, photoluminescence, and cross-section TEM.   In contrast with the unpassivated SiGe quantum dot device, the passivated SiGe single-hole transistor exhibits reproducible Coulomb blockade oscillations.

# ACKNOWLEDGEMENTS

First of all, I would like to thank my advisor, Prof. James Sturm, for his guidance and support of this research. His aggressive optimism, deep insight, and passionate attitude to both research and teaching always inspire me and whole group. I feel very lucky to be able to work with such a professor.

Acknowledgements are specially given to Prof. Daniel Tsui who not only allowed me to use low-temperature measurement facility in his group, but also helped me to clarify the basic concept in physics. I want to thank Prof. Sigurd Wagner for allowing me to use his group's PECVD equipment and many helpful discussions. That he and Prof. Mansour Shayegan took their cost time in reading my thesis is also appreciated. Dr. Nan Yao helped me for high-resolution TEM observations and cross-section TEM sample preparation. At the beginning of QD research, Dr. Leonid Rokhinson (now at Purdue University) showed me how to do AFM nanolithography and low-temperature measurements. The collaborators of NEC research Labs at Princeton, Dr. David Norris (now at University of Minnesota) and Dr. Yuri Vlasov (now at IBM), provided state-of-art self-assembly samples. They are all cordially appreciated.

I would like to thank the colleagues in our group (Prof. Sturm) and Prof. Tsui's group for their help and discussions. Among them, special thanks go to Dr. Kiran Pangal, who showed me the fabrication process of poly-Si TFTs at the beginning. Dr. Eric Stewart showed me how to operate RTCVD. Rebecca Peterson maintains the good condition of our RTCVD and also proofread my thesis draft. Troy Graves-Abe upgrades our group computer and software and read my thesis. Dr. Gabor Csathy, Wangli Li, and Keji Lai helped my low-temperature measurements. Dr. Iris Hsu, Dr. Malcolm Carroll, Dr. Richard Huang, Haizhou Yin, Ke Long, and Kun Yao spent many time with me together in the lab. They make the lab a wonderful environment and a lot of fun.

I feel really fortunate to be surrounded with the talented faculty and students of Princeton University, who create a friendly and instructive research atmosphere. Special mention goes to Dr. Helena Gleskova and Joseph Palmer who keeps the instruments in the cleaning room well operated. I am also indebt to Karen Williams and Carolyn Amesen for their kind help during my study.

Finally, I want to thank my parents. It's their love, encouragement, and sacrifice that bring me, a little boy in Northeast of China, up to Princeton University. I also want to express my deepest appreciation to my wife, Qingjuan. Her constant love, support, patience and sacrifice helped me through the difficult time and make this thesis to be real. This thesis is dedicated to them.

# CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

# Chapter 1

# INTRODUCTION

## 1.1    Motivation

Since the electrical transistor was invented in December 1947 by John Bardeen, Walter H. Brattain and William Shockley [1], and the 1st commercial silicon transistor was announced in May 1954 by Texas Instrument [1], silicon-based materials have been the dominant semiconductor in the integrated circuit (IC) industry. This success is due to their relatively high temperature stability, excellent insulator interface, and low cost. In one Intel Pentium IV CPU chip there are more than 60,000,000 transistors on a silicon substrate [2].  Silicon, which is next to oxygen the most common element in Earth's crust, accounts for 98.6% of the 2002 IC market, and will continue to be the dominant semiconductor material in the near future (see Table 1-1).

**Table 1-1**. Semiconductor materials in IC market [3]

| Global IC market by material | 2002 IC market | Predicted 2007 IC market |
|---|---|---|
| Silicon | 98.6% | 97.6% |
| GaAs and other III-Vs | 1.2% | 1.6% |
| SiGe | 0.2% | 0.8% |
| Total value ($ billion) | 120.5 | 190.8 |

Alloys of Column IV elements silicon and germanium (referred to a SiGe), have larger lattice constant and lower energy bandgap than Si.  The lower energy bandgap of SiGe leads to a higher current gain in Si/SiGe heterojunction bipolar transistors (HBTs)

[4]. Tensile strain in silicon, introduced by epitaxially growing Si on a relaxed SiGe layer, can enhance the electron mobility in metal-oxide-semiconductor field-effect-transistors (MOSFETs) [5]. All these may explain why SiGe is expected to be the fastest growing semiconductor material in IC industry, with a four-fold increase in IC market share from 2002 to 2007 (Table 1-1).

Therefore, the study to improve performance of Si-based materials and devices and to expand their applications to new fields is important, and will significantly benefit the IC industry. In this thesis, we will study the solid-phase crystallization (SPC) of amorphous Si (*a*-Si) for thin film transistors (TFTs), *a*-Si deposition for three-dimensional photonic bandgap crystals (PBCs), and Si/SiGe heterostructure nanopatterning, leading to quantum dot devices.

## 1.2    Si-Based Thin Films
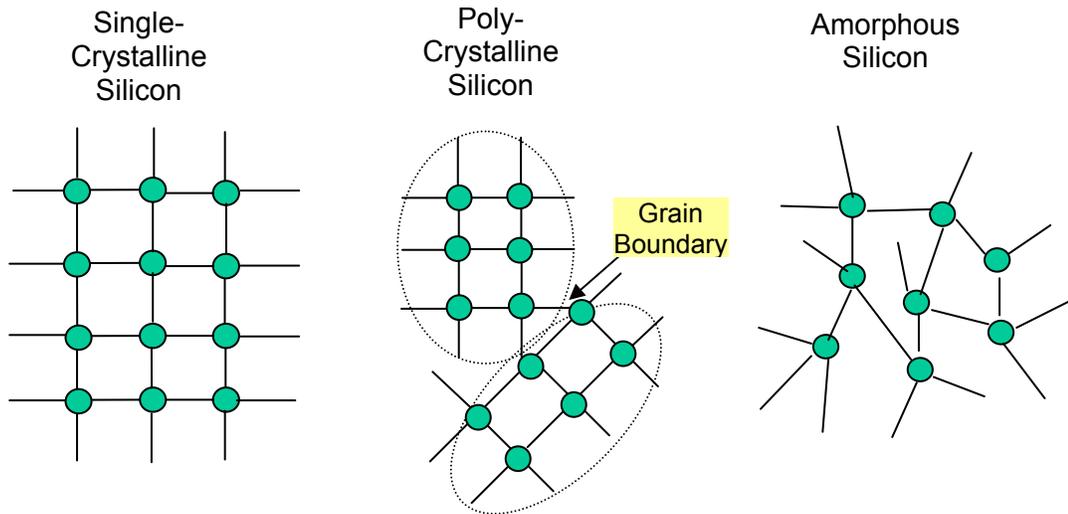


**Figure 1-1.** Crystalline structure of c-Si, poly-Si and *a*-Si.

According to crystallinity, silicon materials are divided into three groups: single-crystalline silicon (c-Si), poly-crystalline silicon (poly-Si), and amorphous silicon (*a*-

Si). Their structures are schematically shown in Fig. 1-1. In c-Si, silicon atoms are periodically arranged, forming the diamond cubic lattice structure. Poly-Si has crystalline domains, called grains, which have different crystalline orientations, forming grain boundaries. In *a*-Si films, silicon atoms are randomly situated without long-range crystalline order, although most atoms are still four-fold coordinated. Silicon atom dangling bonds lead to localized states in the energy bandgap of *a*-Si, resulting in lower transport mobilities of *a*-Si films than those of poly-Si and c-Si.

All these thin films are commonly grown by chemical vapor deposition (CVD) from gas sources. Plasmas are sometimes used to enhance the generation of precursor species, and thus increase the deposition rate.

### 1.2.1   CVD Growth of *a*-Si and Poly-Si

Silicon TFTs are widely used in active matrix liquid-crystal displays (AMLCDs) on glass substrates to address pixels. Large-area, 54-inch LCD displays [6] are an example of this technology. Flexible electronics are fabricated on thin substrates of plastic and steel. When substrates are amorphous, silicon thin films grown by CVD are *a*-Si or poly-Si, depending on the parameters of CVD processes, such as gas composition, gas flow rate, substrate temperature, chamber pressure, plasma power, etc. For example, using $SiH_4$ gas in low-pressure chemical vapor deposition (LPCVD), deposited films are *a*-Si for growth temperatures below 550 °C, and are poly-Si for growth temperatures above 625 °C, as will be shown in Chapter 3. This is because *a*-Si clusters deposited on amorphous surface crystallize to form poly-Si nuclei at temperatures above 600 °C. This is called "as-deposited" poly-Si or "direct deposition". CVD has the advantage of conformal growth compared to evaporation and other methods. Thus we can fill voids and cover complex surfaces. This will be exploited in Chapter 3 to form "inverted opals", which are 3-D PBCs in Si-based materials [7].

### 1.2.2 Crystallization of *a*-Si

Poly-Si can also be obtained by the crystallization of precursor *a*-Si thin films. Compared with crystallized poly-Si, poly-Si films by "direct deposition" tend to exhibit rough surfaces and smaller grain sizes [8], thus resulting in a relatively low field-effect mobility. The crystallization of *a*-Si can be accomplished by solid-phase crystallization (SPC) or laser crystallization. During laser crystallization, substrate is kept at a low temperature, the top *a*-Si film is melted by a pulsed or continuous laser, and then crystallized in subsequent cooling. TFTs made in laser-crystallized poly-Si films have field-effect mobilities up to 640 cm$^2$/Vs for n-channel TFTs and 400 cm$^2$/Vs for p-channel TFTs [9], close to those of c-Si. However, laser crystallization requires sophisticated optical instruments for beam uniformity, and has low reproducibility. SPC of *a*-Si by furnace annealing at temperatures above 600 °C is the simplest and most widespread technique. SPC poly-Si has a higher defect density (microtwins and dislocations) in grains than laser-crystallized poly-Si, resulting in lower mobilities of TFTs. The reduction of intragranular defect density and the removal of grain boundaries in poly-Si by SPC will be studied in detail later in Chapter 2.

### 1.2.3 Epitaxial Growth of Si and SiGe

When the substrate is a single-crystalline silicon wafer, epitaxial CVD growth can occur, leading to a c-Si thin film. Relaxed Si$_{1-x}$Ge$_x$ has a greater lattice constant than that of Si. The lattice constant depends on the concentrations of Si and Ge: $a_{SiGe} = (1-x)a_{Si} + xa_{Ge}$. Thin pseudomorphic SiGe layers which are epitaxially grown on c-Si substrate are under compressive strain in the plane parallel to the surface of Si substrate. This results in the increase of the vertical lattice constant of the strained-SiGe, $a_{SiGe}^{\perp}$.

$$a_{SiGe}^{\perp}(x) = a_{Si} \cdot \left[ 1 + \frac{C_{11}(x) + 2C_{12}(x)}{C_{11}(x)} \cdot \frac{a_{SiGe}(x) - a_{Si}}{a_{Si}} \right],$$

(1.1)

where $C_{11}(x)$ and $C_{12}(x)$ are elastic constants of Si$_{1-x}$Ge$_x$, which can be linearly interpolated between their values for Si and Ge [10,11].
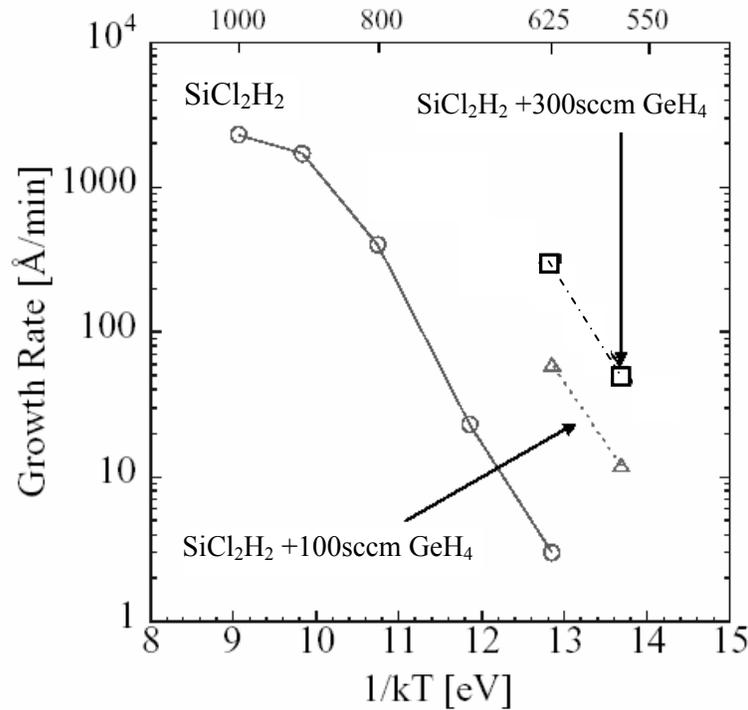
**Figure 1-2.**  Growth rates of single-crystalline Si and $Si_{1-x}Ge_x$ *vs.* inversed growth temperatures.  Si growth parameters include a gas flow of 26 sccm DCS and 3 lpm $H_2$ at a pressure of 6 torr.  $GeH_4$ (0.8 vol.% in $H_2$) is added for $Si_{1-x}Ge_x$ growth [14].

At Princeton, high-quality <100> Si and <100> SiGe epi-layers have been grown on <100> Si substrates by rapid thermal chemical vapor deposition (RTCVD) [12,13].  The reactor setup is described in Dr. Malcolm Carroll's Ph.D. thesis [13].  Typical growth conditions of epi-Si are: a hydrogen flow rate of 3 lpm, dichlorosilane (DCS) flow of 26 sccm, pressure of 6 torr, and temperature from 700°C to 1000°C.  Germane (0.8 vol.% in hydrogen) is introduced to the reactor for $Si_{1-x}Ge_x$ layer growth at a decreased growth temperature of 625 °C.  The resulting growth rates are summarized in Fig. 1-2 [14].

## 1.3    Si-Based Quantum Devices

To date, Moore's Law has been followed by the semiconductor industry for close to half of a century. It has now reached "90-nm technology" with transistor channel lengths equal to about 50 nm. As the semiconductor device feature size enters the sub-100-nm range, phenomena related to quantum mechanics (wave and particle duality) appear. Quantum effects in ultra-small electronic devices are unavoidable. One kind of quantum effect, which is rooted in the wave nature of the charge carriers, is resonant tunneling and quantum interference. Another is related to the quantized nature of the electronic charge, the so-called single-electron tunneling.

Single-electron devices have attracted much attention, with proposed applications of memory, logic and quantum computing in the future. Their operation relies solely on the Coulomb interaction and the quantized nature of the electron charge. Electrons tunnel in and out of a quantum dot one by one, resulting in conductance oscillations of the transistor with varying gate voltage. In the past decade, people have made extensive studies of quantum dot devices on GaAs/AlGaAs, but little on Si or Si/SiGe, though silicon is the dominant material in the IC industry. Most of the demonstrated Si-based quantum dot devices have a MOSFET structure with a $Si/SiO_2$ interface. Due to the amorphous nature of $SiO_2$, defect states at the $Si/SiO_2$ interface can trap electrons and act as parasitic extra quantum dots, resulting in undesired electrical characteristics. Eliminating the interface states in Si-based quantum dot devices is the goal of Part II of this thesis. We first developed a low-energy technique of nanopatterning Si/SiGe heterostructures: AFM nano-lithography and selective wet etching. With silicon epitaxial regrowth to passivate the patterned quantum dot device, a SiGe single-hole transistor without $Si/SiO_2$ interface states has been demonstrated, exhibiting reproducible Coulomb blockade oscillations.

## 1.4    Thesis Outline

This thesis is divided into two parts.

Part I focuses on improving the quality of solid-phase-crystallized poly-Si thin films and the *a*-Si chemical vapor deposition on a self-assembled opal structure to form a 3-D photonic bandgap.  In chapter 2, SPC of *a*-Si is investigated.  The electrical characteristics of poly-Si TFTs are significantly dependent on the microstructure of poly-Si: grain-boundaries and intragranular defects.  First, using a hydrogen plasma exposure to *a*-Si in a selective small region, we achieved single-grain silicon film at designed locations by subsequent furnace annealing.  To reduce the intragranular defect density of crystallized poly-Si films, *a*-Si cantilever structures without underlying silicon oxide were fabricated before SPC, which also enlarged the grain size of poly-Si. Chapter 3 presents 3-D silicon PBCs fabricated from self-assembled opals inverted by *a*-Si deposition and subsequent wet etching.  Different CVD deposition conditions of *a*-Si have been studied to fill the interstitial space of opals.  Optical measurements indicate a near unity reflectance at the wavelength of 1.3 μm, indicating that a true photonic bandgap has been achieved.

Part II investigates the fabrication of Si-based quantum-dot devices.  Chapter 4 outlines the history and development of local anodic oxidation (LAO) by atomic force microscopic (AFM) nanolithography.  The instrumentation in our lab for AFM local oxidation is presented.  In chapter 5, two methods of nanopatterning Si/SiGe heterostructures by AFM local oxidation are introduced.  With AFM nanolithography and selective wet etching, we can electrically isolate a 10-nm-thick SiGe layer.  To electrically passivate the pattered SiGe quantum devices, we studied silicon epitaxial regrowth on strained SiGe layers.  With pre-baking in hydrogen at a relatively low temperature (800 °C instead of 1000 °C), Si regrowth on strained SiGe layer at 700 °C achieves an interface comparable to that without growth interruption.  In chapter 6, we demonstrate a SiGe single-hole transistor fabricated by AFM local oxidation and silicon epitaxial regrowth.  The electrical characteristics, Coulomb blockade oscillations, are reproducible over the different measurement scans and at different temperatures, in contrast with those of unpassivated SiGe quantum-dot devices.

Finally in chapter 7, we summarize our contributions.

# References

[1] B. Donlan and D. Pricer, "Pushing the limits: looking forward...looking back", *Microelectronic Design*, **Vol. 1** (1987).     <http://www.icknowledge.com/history/history.html>.

[2] R. Chau, B. Doyle, M. Doczy, S. Datta, S. Hareland, B. Jin, J. Kavalieros, and M. Metz, "Silicon nano-transistors and breaking the 10nm physical gate length barrier", *Device Research Conference*, Salt Lake City, June (2003).     <http://www.intel.com/research/silicon>

[3] http://www.compoundsemiconductor.net.

[4] J. C. Sturm and H. Yin, "Si/SiGe/Si heterojunction bipolar transistors", in Properties of Silicon Germanium and SiGe:Carbon, edited by E. Kasper and K. Lyutovich, p. 305-318, INSPEC Publication, 2000.

[5] K. Rim, J. L. Hoyt, J. Gibbons, "Fabrication and analysis of deep submicron strained-Si n-MOSFET's", *IEEE Trans. Electron Devices*, **47**: 1406-1415 (2000).

[6] J. Virginia, "The future looks bight for LCD TV", *Information Display*, **19**: 10-14 (2003).

[7] Y. A. Vlasov, X.-Z. Bo, J. C. Sturm, D. J. Norris, "On chip assembly of silicon photonic bandgap crystals", *Nature*, **414**: 289-293 (2001).

[8] M. Ino, J. Miyano, H. Kurogi, Y. Nagatomo, and M. Yoshimaru, "Rugged surface polycrystalline silicon film deposition and its application in a stacked dynamic random access memory capacitor electrode", *J. Vac. Sci. Techn. B*, **14**: 751-756 (1996).

[9] A. Kohno, T. Sameshima, N. Sano, M. Sekiya, and M. Hara, "High performance poly-Si TFTs fabricated using pulsed laser annealing and remote plasma CVD with low temperature processing", *IEEE Transactions on Electron Devices*, **42**: 251-256 (1995).

[10] J. Dismukes, L. Ekstrom, and R. Paff, "Lattice parameter + density in germanium-silicon alloys", *J. Phys. Chem.*, **68**: 3021 (1964).

[11] C. Van de Walle and R. Martin, "Theoretical calculations of heterojunction discontinuities in the Si/Ge system", *Phys. Rev. B*, **34**: 5621-5634 (1986).

[12] J. C. Sturm, P. V. Schwartz, E. J. Prinz, and H. Manoharan, "Growth of $Si_{1-x}Ge_x$ by rapid thermal chemical vapor deposition and application to heterojunction bipolar transistors", *J. Vac. Sci. Tech. B,* **9**: 2011-2016 (1991).

[13] J. C. Sturm, H. Manoharan, L. Lenchyshyn, M. Thewalt, N. Rowell, J. P. Noel, and D. Houghton, "Well-resovled band-edge luminescence of exitons confined in strained $Si_{1-x}Ge_x$ quantum wells", *Phys. Rev. Lett.*, **66**: 1362-1365 (1991).

[14] M. S. Carroll, "The interaction of silicon self-interstitials and substitutional carbon in silicon based heterostructures", Ph.D. thesis, Princeton University, June 2001.

# SOLID PHASE CRYSTALLIZATION OF AMORPHOUS SILICON

## 2.1    Introduction

Amorphous Si (*a*-Si) and poly-Si TFTs are widely used in active matrix liquid crystal displays (AMLCDs) [1].  They are used because they can be made on glass substrates, which are clear to visible light required for displays.  Amorphous silicon is in more widespread use, but poly-Si is of increasing interest due to its high mobility.  Recently, *a*-Si and poly-Si TFTs have been used for active matrix addressing for organic light emitting diode (OLED) displays [2,3].  In this chapter, we study the solid-phase crystallization of *a*-Si to poly-Si.

### 2.1.1   Why Poly-Si TFTs?

Current AMLCDs are based on *a*-Si TFT technology.  A-Si TFTs are used to achieve ON/OFF switching of each image pixel.  Hydrogenated *a*-Si can be deposited directly on glass substrates by CVD.  The low process cost and low OFF current makes *a*-Si TFTs dominant in active-matrix addressing of displays.  However, compared with *a*-Si TFTs, poly-Si TFTs have a higher electron field-effect mobility ($\sim 10 - 300$ cm$^2$/Vs).   Furthermore, no p-channel device is available in *a*-Si, so CMOS circuits require poly-Si.  In active-matrix circuits, the higher carrier mobility of poly-Si TFTs results in a smaller transistor size than *a*-Si TFTs for same ON current.  This will

increase the display aspect ratio between the optical windows and the total pixel size, and thus reduce the power consumption or increase the display resolution.  In addition, p-channel poly-Si TFTs can provide electronic circuits to control OLED operation [4].

Poly-Si could also be used to integrate the driver circuits for the active-matrix arrays.  Drivers are difficult to fabricate from *a*-Si TFTs because of the low electron mobility and the extremely low mobility in p-channel transistor in *a*-Si.  Usually, drivers are made of c-Si circuits, which are then bonded to the matrix-addressing array.  This is the primary cost of electronics for AMLCDs.  To reduce the cost, one can develop TFT active-matrix displays with fully integrated poly-Si driver circuits [5,6].

### 2.1.2    Solid-Phase Crystallization of *a*-Si

As described in Sec. 1.2.1, poly-Si can be obtained by direct deposition or by crystallization of *a*-Si.  Due to the smoother surface and larger grain size of crystallized poly-Si, the crystallization of *a*-Si has attracted more interest.  Solid-phase crystallization (SPC) of *a*-Si, accomplished by furnace annealing, produces highly uniform poly-Si films over large areas, and is a proven batch process.  Because the strain points of affordable glass substrates lie near 600 °C, crystallization and further processing are restricted to temperatures at or below ~ 600 °C.  However, the full crystallization of *a*-Si by furnace annealing at 600 °C historically has required a long anneal time, on the order of 20-60 hr [7].

Solid-phase crystallization involves two steps: nucleation and grain growth.  During nucleation, silicon atoms rearrange themselves from a disordered to an ordered state, forming small crystalline clusters.  The crystal cluster spontaneously grows until it reaches a critical size.  The critical size of crystal clusters has been estimated to be around 2-4 nm at a temperature of 650 °C [8].  Once the critical size is reached, grain growth will start.  The grain growth mechanism is very similar to solid phase epitaxy (SPE).  Since the activation energy of nucleation is ~ 4.9 eV [9], greater than that of grain growth 2.3-2.7 eV [10-11-12], the crystallization rate at low temperatures is primarily limited by the nucleation step.  To reduce the crystallization time, various techniques

have been used to create crystalline "seeds" in an *a*-Si matrix to enhance the nucleation. They include metal-induced crystallization [13,14], germanium-induced crystallization [15], and plasma-induced crystallization [16,17].  For example, the hydrogen plasma treatment of *a*-Si enhances SPC by reducing the crystallization time from 20 hr to 4 hr at 600 °C [17].  In this chapter, we will show that a single nucleus is formed by exposing a hydrogen plasma to a small area of the *a*-Si film, leading to single-grain silicon films at a designed location, as opposed to a random one [18].

### 2.1.3    Fabrication of Polysilicon TFTs
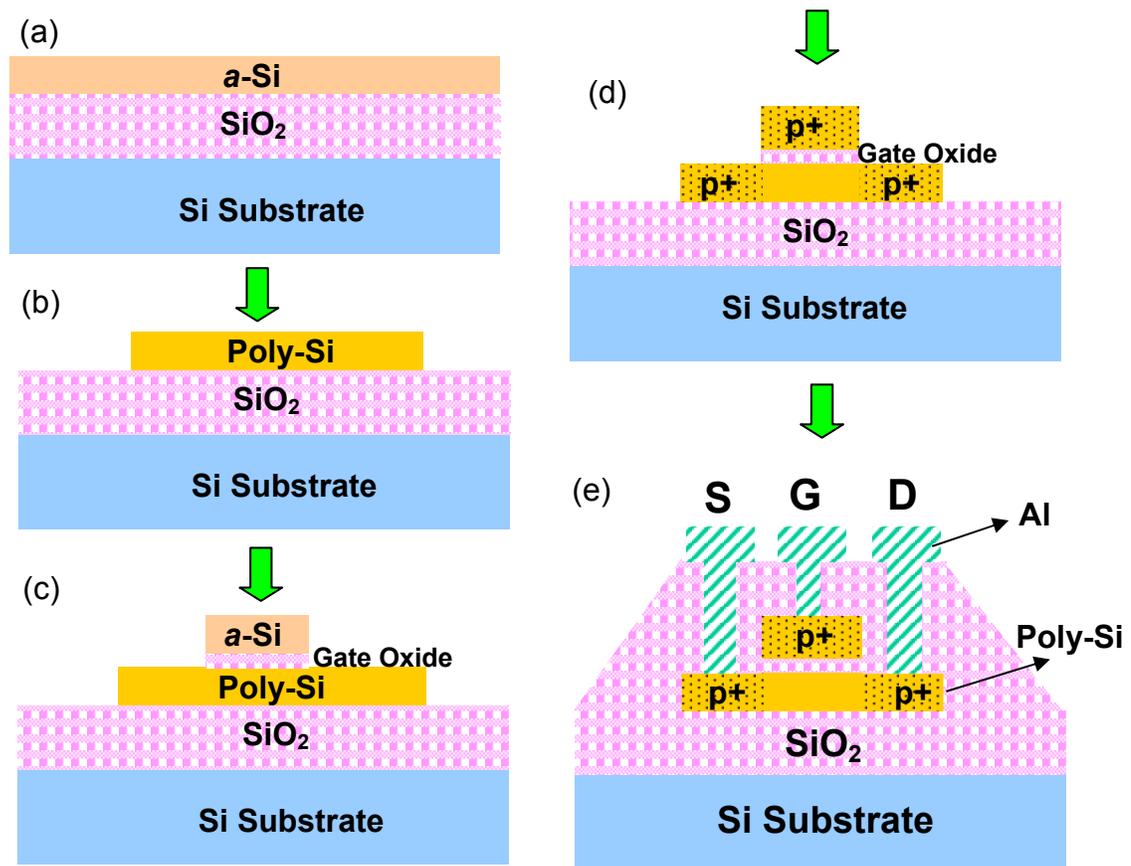


**Figure 2-1.**  Fabrication process of p-channel poly-Si TFTs.  (a) a-Si film deposition; (b) SPC of a-Si and active island patterning; (c) gate oxide and *a*-Si gate deposition and patterning; (d) boron ion implantation and activation; (e) passivation oxide deposition with subsequent hole opening and aluminum metal contact.

P-channel poly-Si has been fabricated with the process flow shown in Fig. 2-1. Ultimate applications would be on glass, but our experiments were done on $SiO_2$ on Si substrates for compatibility with the process lab.  First, a 150-nm-thick $a$-Si film is deposited on an oxidized Si substrate at 150 °C by plasma enhanced chemical vapor

(a)



(b)
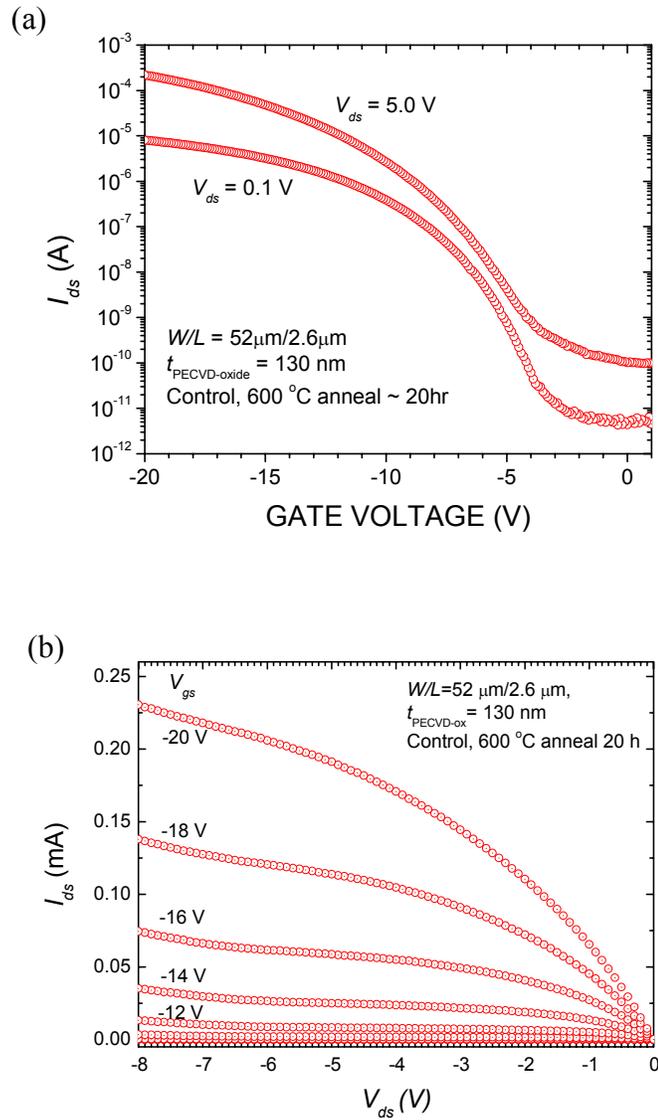


**Figure 2-2.** Electrical characteristics of (a) drain current $vs$. gate voltage and (b) drain current $vs$. drain voltage for p-channel TFTs.

deposition (PECVD). The deposition recipe is shown in Appendix A. Then, *a*-Si film is fully crystallized at 600 °C by furnace annealing for 20 hr, and subsequently patterned into active islands by optical lithography and reactive ion etching (RIE). The gate oxide (~ 130 nm) is deposited at 250 °C by PECVD, followed by a 250-nm-thick *a*-Si deposition for the gate. After gate patterning, source/drain and gate are ion implanted by boron ($B^+$) with a dose of $2\times10^{15}$ $cm^{-2}$ and energy of 35 keV. The dopants were activated by furnace anneal at 600 °C for 20 hr. RF hydrogenation at a temperature of 350 °C and power of 0.6 $W/cm^2$ was then performed in the PECVD chamber in order to passivate the silicon dangling bonds at poly-Si grain boundaries [19]. After hydrogenation, a 250-nm-thick passivation oxide is deposited, followed by contact hole opening in the oxide. Finally, aluminum was thermally evaporated and then patterned by optical lithography and wet etching. The sample was annealed in forming gas (mixture of 10% $H_2$ in $N_2$) at ~ 250 °C for 90 s in a rapid thermal annealer. The whole fabrication process has been optimized, with details given in Ref. [20].

**Table 2-1.** Electrical characteristics of polycrystalline silicon n-channel and p-channel TFTs (W/L = 50μm/2μm) with gate oxides of 250°C PECVD oxide and 1000°C thermal oxide.

| Electrical Characteristics | N-MOSFET | | P-MOSFET | |
|:---:|:---:|:---:|:---:|:---:|
| | *250°C PECVD oxide* | *1000°C thermal oxide* | *250°C PECVD oxide* | *1000°C thermal oxide* |
| $\mu_{field}$ **(cm²/Vs)** | 38 | 110 | 19.2 | 75.6 |
| $V_{th}$ **(V)** | 0.8 | 0.1 | -11.8 | -2.8 |
| **Subthreshold Slope (V/Dec)** | 1.6 | 0.5 | 1.4 | 0.4 |
| $I_{on}/I_{off}$ | $> 1\times10^6$ | $1\times10^7$ | $> 1\times10^6$ | $1\times10^7$ |

The electrical characteristics of the TFTs are well behaved.  Typical characteristics of drain current *vs.* gate voltage and drain current *vs.* drain voltage are shown in Fig. 2-2(a) and (b) respectively.  TFTs with channel length from 2 μm to 50 μm were fabricated, showing results with field-effect mobilities of 10-20 $cm^2$/Vs, subthreshold slopes of 1.2-2 V/Dec., and ON/OFF current ratios of $10^6$-$10^7$.

TFTs with a thermal gate oxide grown at 1000 °C were also fabricated.  The oxide thickness was ~ 35 nm.  The electrical characteristics of TFTs are summarized in Table 2-1, including n-channel TFTs from Ref. [20] by a similar process (prior work in our lab).  It is not surprising that n-channel TFTs have slightly higher field-effect mobilities than p-channel TFTs.  However, TFTs with a high-temperature thermal gate oxide have much higher field effect mobilities than those with low-temperature PECVD gate oxide.  This may be attributed to the low density of interface states between the thermal oxide and poly-Si, or to the decreasing of the intragranular defect density in poly-Si grains during high temperature annealing [21].  The high-temperature process is not fit for glass substrates with strain point of ~ 600 °C.  A method to reduce the intragranular defect density of SPC poly-Si films with process temperatures not greater than 600 °C is required, and will be studied in Sec. 2.3.

### 2.1.4   Microstructure of SPC Polysilicon

Compared with the electron and hole mobilities of *c*-Si transistors, for example, ~ 700 $cm^2$/Vs for electrons and ~ 250 $cm^2$/Vs for holes in silicon-on-insulator (SOI) MOSFETs [22], the carrier mobilities in the above poly-Si TFTs are much smaller.  Figure 2-3(a) shows the microstructure of poly-Si films under TEM.  The difference between c-Si and SPC poly-Si is that SPC poly-Si contains many grain boundaries and intragranular defects, as indicated in Fig. 2-3(b).
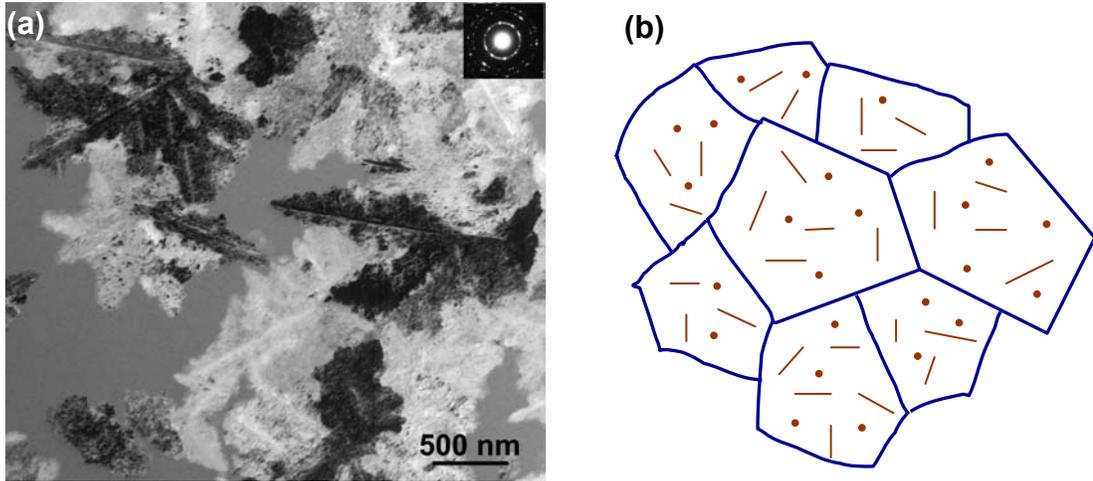
**Figure 2-3.** (a) TEM observation of polysilicon film after anneal at 600 °C for 16 hr without hydrogen plasma treatment (control sample) shows grain size 0.3−0.8 μm. Inset is the diffraction pattern. (b) Schematic of poly-Si microstructure composed of grain boundaries and intragranular defects.
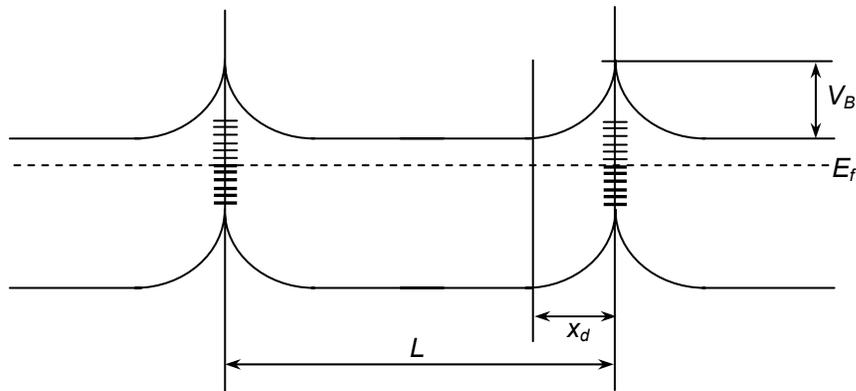


**Figure 2-4.** Potential barriers in poly-Si, which are due to the charge trapping at the grain boundaries [23].

In poly-Si, defects at grain boundaries are trapping centers. Free carriers are trapped at the grain boundaries, forming depletion regions and leading to energy band curvature (see Fig. 2-4 [23]). The resulting potential barriers at the grain boundaries will make it difficult for carriers to cross grain boundaries, which results in low field-effect mobilities. Furthermore, it has been reported that intragranular defects, such as micro-twins and dislocations, exist in SPC poly-Si [21,24], as seen in Fig. 2-3(a). They can also trap carriers and decrease the mobilities of poly-Si TFTs. Therefore, to improve the poly-Si TFTs, the number of grain boundaries and intragranular defects in the transport channel of TFTs should be reduced. This is our goal for this research.

## 2.2    Single-Grain Silicon Film at Designed Locations

### 2.2.1    Motivation

The electrical characteristics of polysilicon TFTs are strongly dependent on the polysilicon microstructure. Grain boundaries are scattering centers which decrease carrier mobility and also serve as midgap states to increase leakage current. To improve the performance of polysilicon TFTs, one would want to locate the TFTs within a single grain of the polysilicon between grain boundaries. Therefore, it is of great interest to control the location of single grain regions [25,26,18,27,28].

The solid-phase crystallization (SPC) of amorphous silicon involves two steps, *i.e.* nucleation and growth. A single nucleus induced during the nucleation stage is the prerequisite for the formation of a single-grain island. To date, several methods have been demonstrated to enhance the nucleation of *a*-Si:H SPC, such as metal-induced SPC [13,14], germanium-induced SPC [15], and plasma-induced SPC [16,17]. Although the original motivation of these methods was to reduce the thermal budget of SPC, they can be used to induce a single nucleus and increase grain size by lateral growth from seeding sites into the amorphous matrix. The formation of single-grain islands at designed locations has been reported by methods of silicon ion implantation [25] and nickel-induced crystallization [26-28]. Single-grain silicon islands by plasma seeding

16

have not been reported. Compared with the seeding by ion implantation and metals, plasma-induced SPC has possible advantages of low metal contamination and less radiation damage.

### 2.2.2 Experimental Details

It has been reported that a hydrogen plasma treatment (HPT) of amorphous silicon films at room temperature enhances the rate of SPC, and thus can reduce the crystallization time from 20 hr to 4 hr at 600 °C [17]. Surprisingly, the hydrogen plasma actively abstracts hydrogen from the amorphous silicon and creates seed nuclei in the top 30 nm of the film. This process can be spatially masked by covering the surface of *a*-Si: H with a silicon nitride film and then opening holes in the nitride where the hydrogen seeding process will occur. There is no accelerated crystallization under the nitride films.
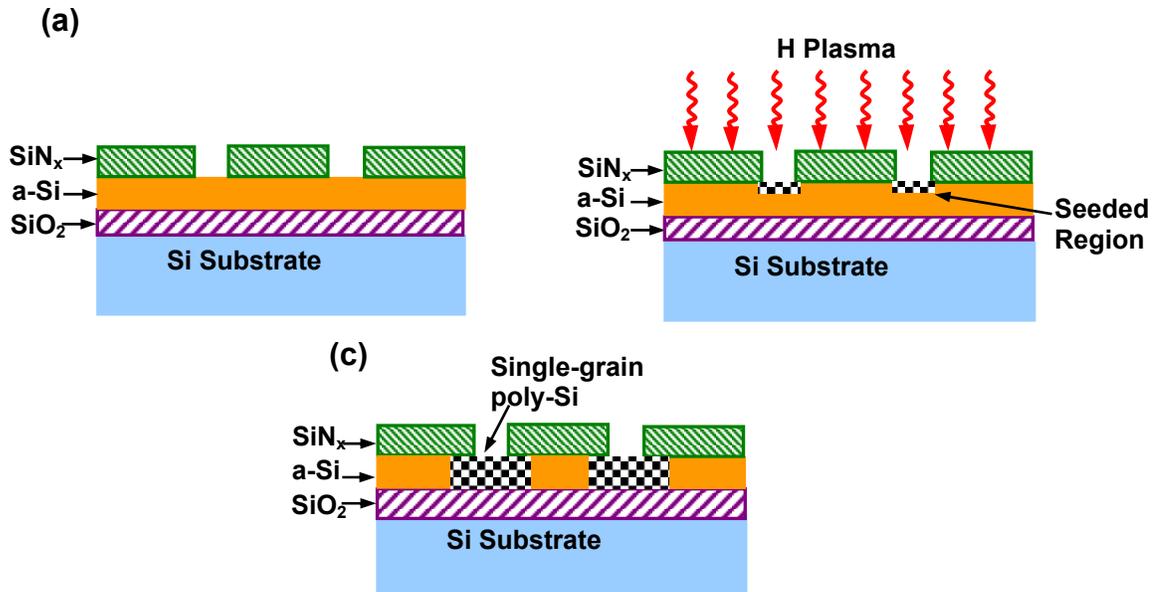


**Figure 2-5.** Experimental processes of selective polysilicon formation induced by masked hydrogen plasma and subsequent crystallization: (a) formation of seeding window in the deposited SiN$_x$, (b) nucleation by hydrogen plasma, and (c) lateral growth /crystallization during subsequent anneal.

Figure 2-5 shows the experimental steps for the formation of single-grain islands. First, 100-nm-thick amorphous silicon was deposited on an oxidized silicon substrate at 150°C with RF power of 18 mW/cm$^2$ by PECVD. During deposition, the flow rate of silane is 50 sccm and pressure stabilizes at 500 mtorr. The hydrogen concentration is ~ 17 % (atomic) in the amorphous silicon. Silicon nitride with 200-nm-thickness was then deposited by PECVD at 200 °C, which has been demonstrated not to reduce the hydrogen concentration in a-Si:H [29] and has little effect on the hydrogen-plasma enhancement of SPC. Holes with diameters from 0.4 μm to 1.8 μm were opened in the silicon nitride film by electron-beam lithography and dry etching. The samples were then exposed to a hydrogen plasma in a parallel-plate reactive ion etcher (RIE) at the optimum condition with an RF power of 0.8 W/cm$^2$, hydrogen flow rate of 50 sccm, and pressure of 50 mtorr [17]. The low pressure and high power are designed to give a high hydrogen ion energy. Finally, the nitride films were removed by wet etching and the samples were annealed at 600 °C in nitrogen. The crystallinity of the silicon film was monitored by ultraviolet reflectance (λ=276 nm).
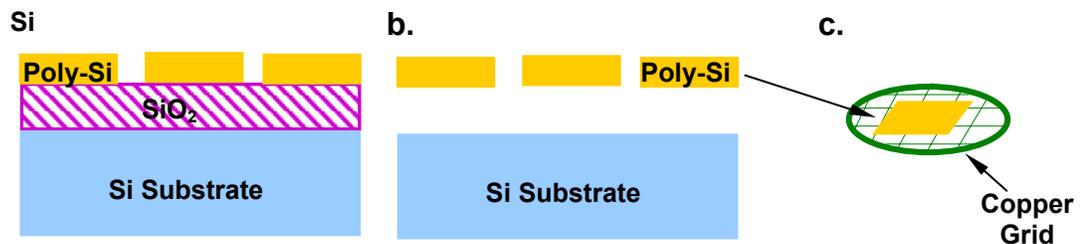


**Figure 2-6.** TEM sample preparation: (a) active island patterning, (b) film lift off by selective wet etching, and (c) film after pick-up with a copper grid.

Samples for transmission electron microscope (TEM) observation were prepared by a lift-off process, as indicated in Fig. 2-6 [30]. Silicon films, first pattered into 1 × 1 mm$^2$ islands, were lifted off from the oxidized silicon substrate by an HF solution. The peeled-off films were placed onto copper grids for TEM observation. The grain size is

characterized by an effective diameter $d = \sqrt{4A/\pi}$, where $A$ is the grain area. TEM observations were performed in the Princeton Materials Institute. High-resolution lattice images were under assistance of Dr. Nan Yao.

### 2.2.3 Results and Discussion
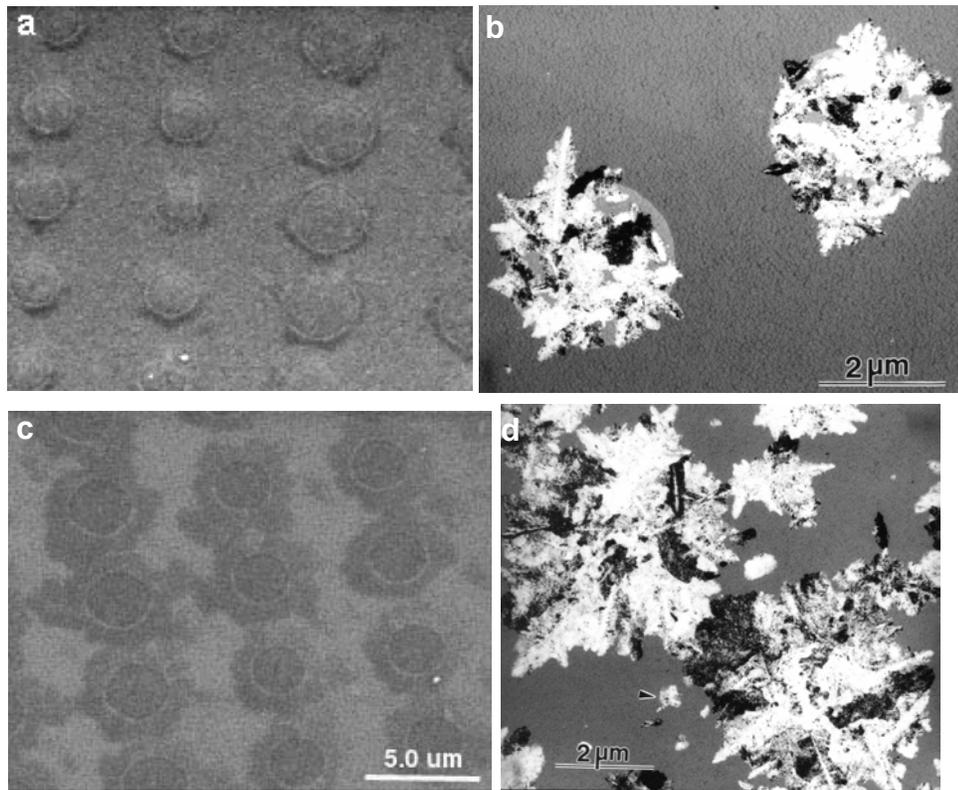


**Figure 2-7.** SEM (a & c) and TEM (b & d) micrographs of lateral growth from the nucleation sites induced by hydrogen plasma treatment after 600 °C annealing for (a) (b) 6 hr and (c) (d) 10 hr.

TEM observations on polysilicon films without hydrogen plasma treatment (HPT) are shown in Fig. 2-3(a). The grains locate randomly on the film with a size of $0.3 - 0.8$ μm. Fig. 2-7 shows the selective crystallization and lateral growth through

scanning electron microscope (SEM) and TEM for samples with large seeding holes (~3 µm) which were annealed for (a) (b) 6 hr and (c) (d) 10 hr.  The dark areas in the Fig. 2-7 (a) and (c) are fully crystallized polysilicon, but the white areas are still amorphous, which has been confirmed by UV reflectance.  The films in the holes seeded by the hydrogen plasma are not only completely crystallized, but also laterally grow outward to the surrounding amorphous matrix with a lateral growth rate of 0.5 µm/hr. Comparing TEM observations between Fig. 2-7(b) and Fig. 2-7(d), we can see no grains formed in the area without HPT (control area) until the anneal time increases to 10 hr. The grain size at the control area of Fig. 2-7(d) is ~ 0.4 µm (indicated by an arrow), in contrast with the grain size of ~ 2.5 µm in the area which nucleated from the HPT hole and laterally grew outward of the hole.  This result shows that the nucleation site can be controlled by selective exposure to the hydrogen plasma, and lateral growth from this site will increase the grain size.
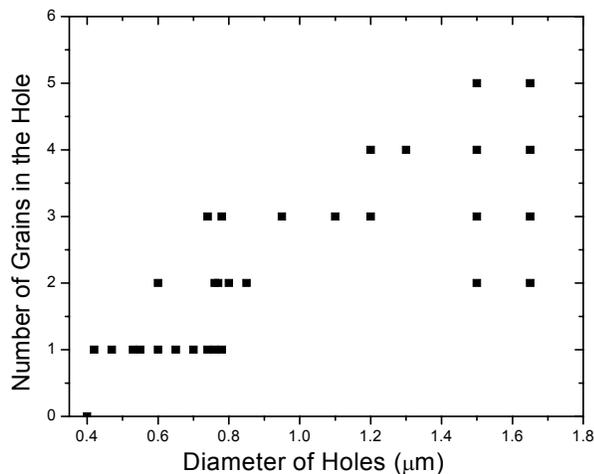


**Figure 2-8.** The relationship between the number of nuclei and the hole size, after hydrogen plasma treatment and annealing at 600 °C for 3 hr [18].

Multiple polysilicon grains were also observed by TEM in a hole with a 1.0-μm-diameter annealed at 600 °C for 5 hr.  Although the crystallization occurs only within the hole region exposed to the hydrogen plasma, multiple grains are formed, presumably resulting from multiple nucleation sites within the hole.  To reduce the number of nuclei, holes with diameters from 0.4 μm to 1.8 μm were opened in silicon nitride prior to the HPT.  After annealing for 3 hr at 600 °C, the number of grains in the holes was counted under the TEM (Fig. 2-8).  When the hole diameter is greater than 0.8 μm, multiple grains exist in the exposed hole; when the hole diameter is between 0.6 μm and 0.8 μm, single or multiple grains are observed in the hole.  When the hole diameter is less than 0.6 μm, a single grain island is formed.  In the silicon ion implantation approach [25], the minimum hole size needed to produce single grain is ~ 0.66 μm, which is close to our result.
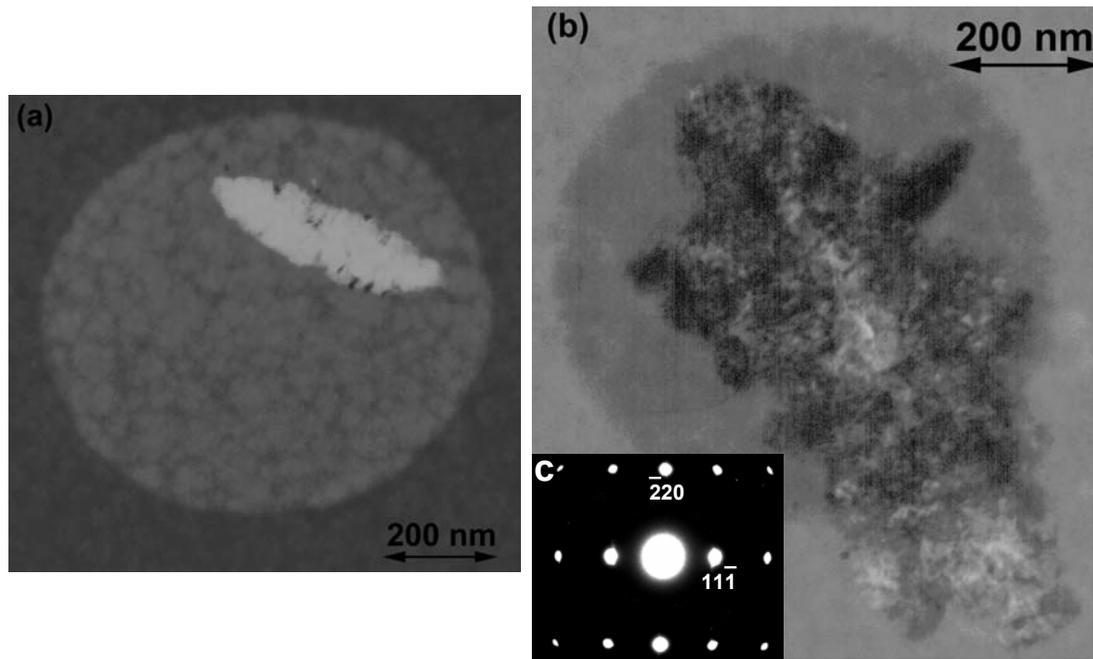


**Figure 2-9.**  TEM micrograph of a single nucleus in a hole with a diameter of 0.55μm, induced by hydrogen-plasma exposure and then annealing at 600 °C for (a) 3.0 hr, (b) 8.0 hr, and (c) the SADP of the grain of (b).

Figure 2-9(a) shows a single grain within a 0.55 μm diameter hole after annealing for 3 hr, with approximate dimensions of 0.13 μm × 0.4 μm. No other grains exist either in the hole or outside of the hole. For longer anneals (8hr, Fig. 2-9b), the grain grows laterally outside of the seeding hole to the amorphous matrix, with the grain size increasing to ~ 0.25 μm × 0.8 μm. The grain size can be as large as 2.5 μm after a 16 hr anneal, which is large enough for TFT fabrication. We did not make TFTs in such grains. However, it is a promising direction for future work. The selective area diffraction pattern (SADP) (Fig. 2-9c) of the silicon grain of Fig. 2-9(b) confirms the single crystalline nature of the grain. The zone axis of the SADP is the [112] of a face-centered-cubic crystalline structure. The grains are not defect-free, however, and the intra-grain defects appear by TEM to be similar to those in other polycrystalline silicon films formed by low temperature crystallization of amorphous silicon.

## 2.3 Polysilicon Films with Large Grain Size and Low Intragranular Defect Density by Removal of Underlying Oxide

### 2.3.1 Introduction

As we mentioned above, the electrical characteristics of polysilicon TFTs are strongly dependent on the polysilicon microstructure. Grain boundaries and intragranular defects form electrical potential barriers and impede the carrier transport of poly-Si TFTs. Polysilicon films with larger grain sizes and fewer intragranular defects have been a continual goal [31,32,33,34]. Recent low-temperature (≤ 600 °C) SPC techniques can achieve a grain size as large as 3.0 microns deposited by disilane gas [31]. TFTs made with channel lengths smaller than the grain size still have a mobility only on the order of 100 cm$^2$/Vs, even though there should be no grain boundaries within the channel. However, the residual intragranular defects reduce the defect-free area of polysilicon film down to 30 nm, and it is thought that they become the limiting factor in

device performance [7].  Therefore, reducing the density of intragranular defects becomes very important to improve the electrical performance of TFTs.

To date, two methods have been suggested to reduce the density of intragranular defects: high-temperature annealing [21,35] and laser crystallization [36].  Haji *et al* [21] reported that the main intragranular defects in polysilicon films after crystallization at 600 °C are microtwins, and that they are not stable above 750 °C, so they can be eliminated with further high-temperature annealing.  However, high-temperature processing cannot be applied to AMLCD TFTs fabricated on glass substrates with a strain point less than 650 °C.  Compared with the furnace annealing, laser crystallization has disadvantages of high-cost and poor film uniformity.  Reducing this intragranular defect density of SPC polysilicon films at a temperature below 650°C is a motivating factor for this research. In this work, a free-standing cantilever of amorphous silicon film without underlying silicon dioxide was fabricated.  The absence of underlying oxide is found to decrease the intragranular defect density and increase the grain size [37].


### 2.3.2   Experimental Details

Figure 2-10 shows the fabrication process of the cantilever structure and its layer structure.  Before amorphous silicon (*a*-Si) film deposition, 100-nm-thick silicon nitride was deposited by low-pressure chemical-vapor-deposition (LPCVD) on a <100> silicon substrate.  The purpose of $Si_3N_4$ here is to alleviate "stiction" problem during the cantilever release process.  Two-micrometer-thick silicon dioxide at 250 °C and subsequently amorphous silicon at 150 °C were deposited by PECVD with the same deposition condition as above.  The amorphous silicon was then patterned into islands (Fig. 2-10(b)) by optical lithography and dry etching.  Oxide wet etching in buffered oxide etch 10: 1 ($H_2O$: HF) for 30 min was used to release the cantilevers, which have a typical length and width of 20 μm and 10 μm, respectively.  Stiction was avoided by rinsing in DI water, soaking in isoproponal, and finally heating on a hot plate at 200 °C for 20 sec to evaporate isopropanol.  SEM observation (Fig. 2-11(a)) confirmed that the

*a*-Si cantilevers did not collapse onto the substrate. Samples were then annealed at 600 °C for various periods in nitrogen to crystallize the amorphous films to polysilicon. SEM again confirmed the suspension of the polysilicon cantilevers (Fig. 2-11(b)). The effect of the cantilever was determined by comparing the polysilicon properties on them with those in areas on the same sample when the underlying SiO$_2$ was not removed (control area). TEM samples were prepared by the lift-off process, described in Figure 2-6.

The Raman scattering spectra of polysilicon films were measured at room temperature from 400 cm$^{-1}$ to 600 cm$^{-1}$ wavenumbers, using an argon laser source with a wavelength of 514.5 nm. To prevent further heating and crystallization of silicon films during the experiment, the laser power was kept below 50 mW. The Raman data were fitted to a combination of Lorentzian and Gaussian modes for peak parameters.
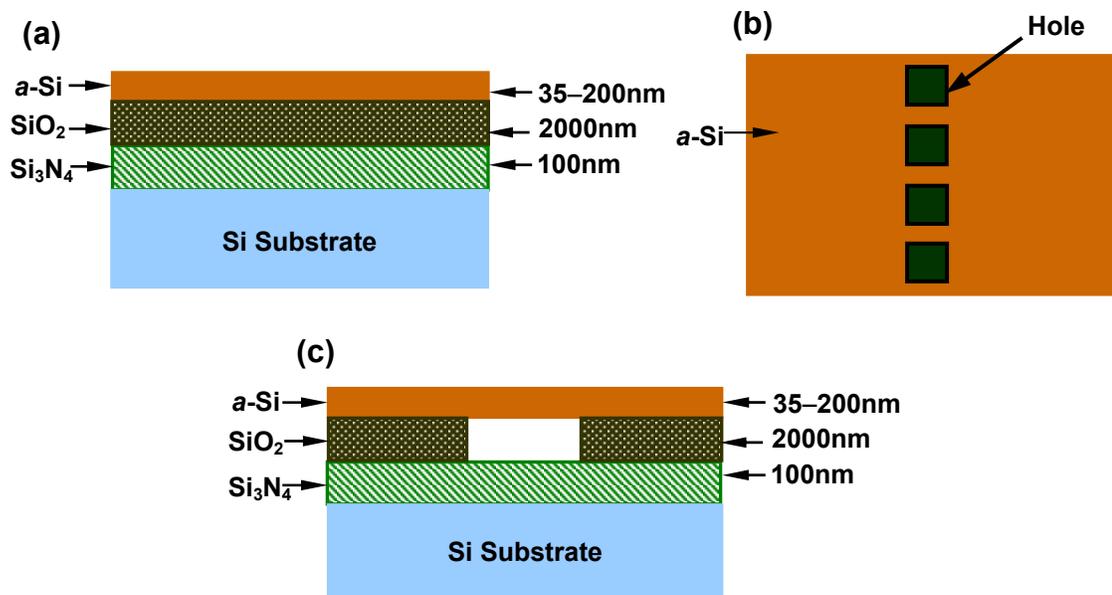
**Figure 2-10.** Fabrication process of amorphous silicon cantilever structure: (a) layer structure; (b) top view before silicon dioxide etching; (c) cross section of cantilever structure after wet etching in buffered oxide etch (10:1).
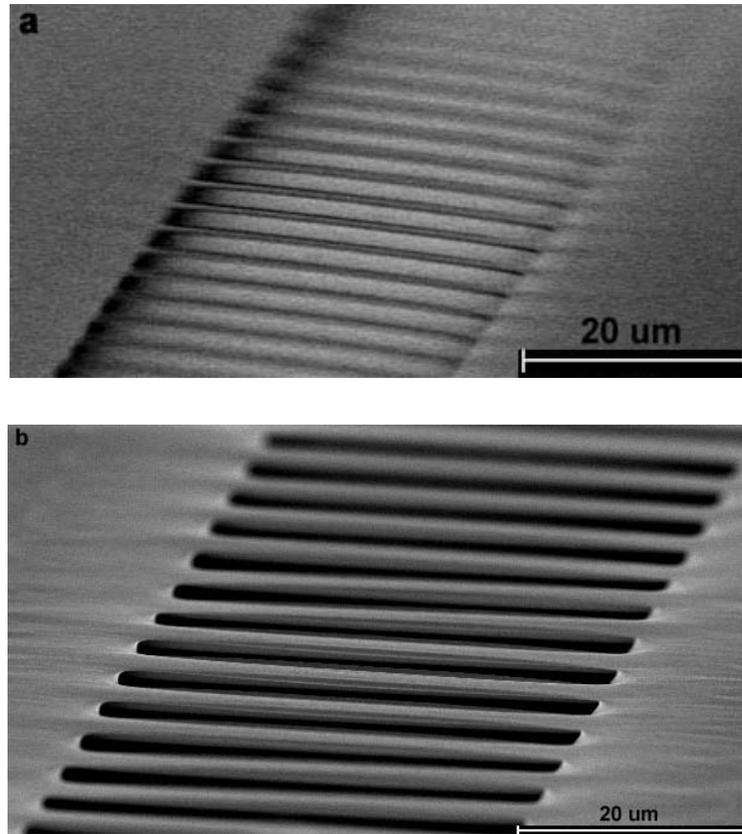
**Figure 2-11.** SEM observations to show the silicon cantilever suspended above the substrate (a) before annealing and (b) after annealing.

### 2.3.3   Effect of Underlying Oxide Removal on Grain Size Enhancement

*Grain-Size Observations*

Figure 2-12 shows TEM observations of fully-crystallized polysilicon grains in (a) control regions with underlying $SiO_2$ and (b) cantilever regions without underlying
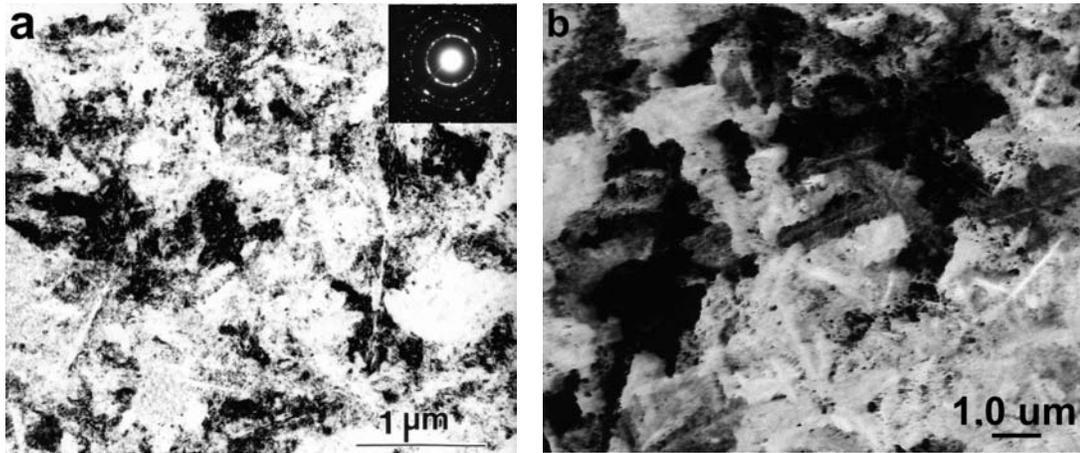
**Figure 2-12.** Plan-view TEM micrographs to show the grain size of fully-crystallized polysilicon films after annealing at 600 ºC for 24 hr in (a) control region with underlying $SiO_2$ (grain size ~ 0.6 μm) and (b) cantilever region without underlying $SiO_2$ (grain size ~ 3.0 μm). Inset of (a) is the diffraction pattern of polysilicon films.
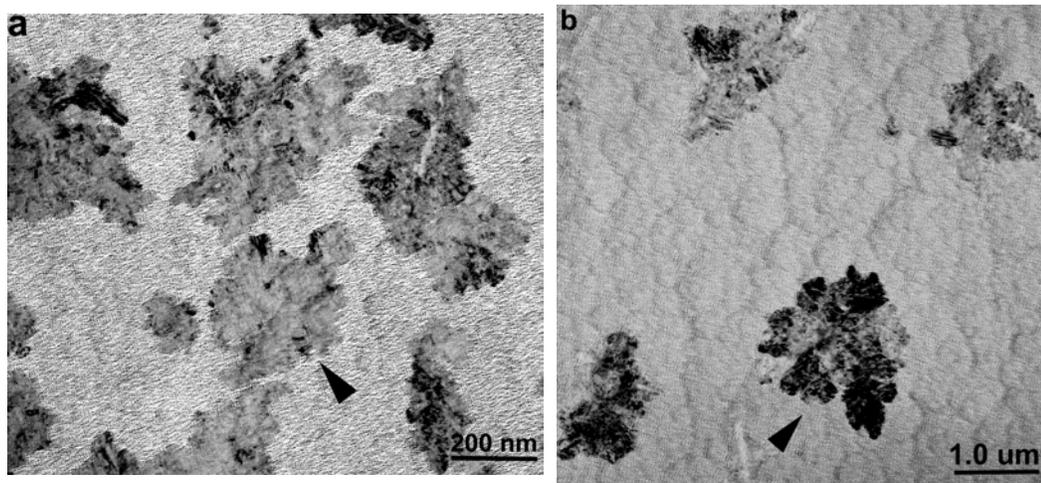


**Figure 2-13.** TEM observations of the grain density and grain size in (a) the control area and (b) suspended films after annealing at 600 ºC for 14 hr before complete crystallization. Note the different length scales.

$SiO_2$ after annealing at 600 ºC for 24 hr.  The inset of (a) is the diffraction pattern of the polysilicon films.  The average grain size is ~ 3.0 μm in (a), and 0.6 μm in (b).  This indicates that the removal of $SiO_2$ under the amorphous silicon layer before annealing increases the grain size of polycrystalline silicon.

*Nucleation Rate Reduction*

The solid-phase crystallization (SPC) of amorphous silicon involves two steps, *i.e.* nucleation and growth.  The increase in grain size can be explained by a decrease in the nucleation rate or an increase in the grain growth rate, both leading to fewer but larger grains.  A theoretical analysis by Iverson and Reif [38] gave the final grain size *d* by

$$d \propto \left[ v_g \middle/ N \right]^{1/3} , \tag{2.1}$$

where $N$ is the nucleation rate, and $v_g$ is the grain growth rate.  It has been pointed out that the interface of the precursor amorphous film/substrate (*a*-Si/$SiO_2$) is the preferred site for SPC nucleation [39].  A large number of nucleation sites at the interface of *a*-Si/$SiO_2$ in the typical SPC films results in small silicon grains due to their impingement during grain growth.  Ryu *et al.* [32] claimed that when the nucleation at the interface between the *a*-Si: H and the underlying $SiO_2$ is suppressed by adding oxygen to the initially growing *a*-Si, the resulting slower top surface nucleation of amorphous silicon can increase the polysilicon grain size from 0.3 ~ 1 μm to 3 ~ 5 μm.  In our case, instead of incorporating of oxygen atoms into the initial growing *a*-Si: H, we etched away the underlying $SiO_2$ to completely remove the interface associated with the nucleation.  Figure 2-13 shows the difference of grain densities within *a*-Si: H matrix after heating at 600 ºC for 14 hr before complete crystallization in (a) the control region and (b) the cantilever region.  The grain density in the free-standing films is ~ 10 times lower than in the control films (~$10^8$ cm$^{-2}$ *vs.* ~$10^7$ cm$^{-2}$).  This smaller nucleation rate $N$ in the cantilever sample is one reason leading to the final larger grains.

*Enhanced Growth Rate*

Besides the difference of grain density before full crystallization, the grain size in the control film before the merging of the grains is smaller than that in the cantilever film. An average grain in the control film (pointed by an arrow in Fig. 2-13a) has a size ~ 0.4 μm, while that in the cantilever films (Fig. 2-13b) is ~ 1.0 μm. Therefore, the growth rate of polysilicon grains can be increased by the removal of the underlying $SiO_2$ before crystallization. Thus the larger grain size in the fully crystallized suspended film than the control film as shown in Fig. 2-12 is attributed not only to the lower nucleation density $N$, but also to the higher growth rate $v_g$.

Growth rate $v_g$, during the growth stage of SPC, has been expressed as [38]

$$v_g \propto \exp\left[-\left(E_d + \Delta G/2\right)/kT\right]$$
.                                                                                              (2.2)

$E_d$ is the activation energy of silicon atom self-diffusion, and $\Delta G$ is the net change in free energy during SPC.

$$\Delta G = -V\Delta G_v + A\gamma + V\Delta G_s$$
,                                                                                              (2.3)

where $\Delta G_v$ is Gibbs-free-energy difference between $a$-Si and polysilicon per unit volume $V$, $\gamma$ is the interface energy per unit surface area $A$, and $\Delta G_s$ is strain energy per unit volume $V$ related to the phase transition. Stress can accumulate during SPC due to volume contraction on the $a$-Si to poly-Si phase transition, or due to the inability of silicon atoms to freely rearrange near the a-Si/$SiO_2$ interface due to the bonding of $a$-Si atoms to the oxide. The strain energy $\Delta G_s$ results from this stress during SPC. The difference of the final stress in the SPC films was measured by Raman scattering, which detects the energy of optical phonons that interact with a probe photon beam. The shift in phonon energy (Raman shift) depends on the stress in the material, with biaxial tension leading to a smaller Raman shift [40-41].
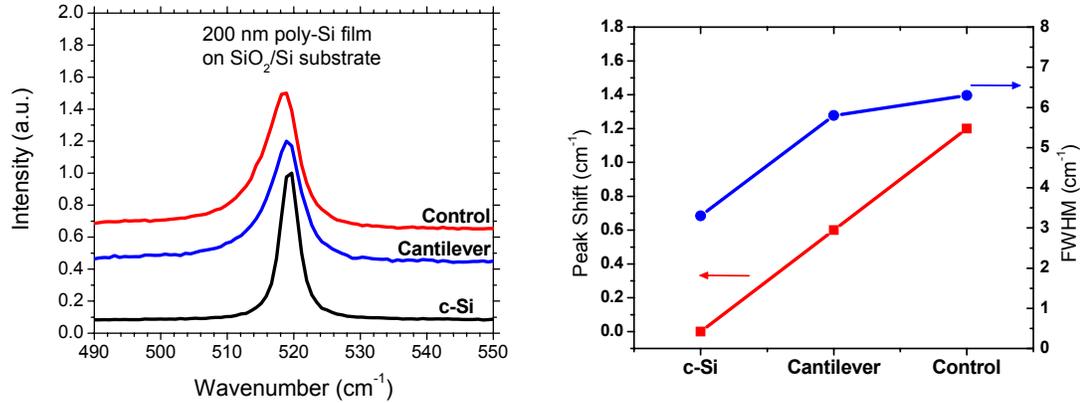
**Figure 2-14.** (a) Raman spectra and (b) absolute value of peak-shift and FWHM of polysilicon films in the control region and cantilever region, and of <100>-oriented single-crystalline silicon substrate.

Figure 2-14(a) shows the Raman spectra of 200-nm-thick polysilicon films crystallized with and without underlying $SiO_2$ and of <100>-bulk silicon. The Raman peak for both free-standing cantilever films and the films on oxide are at smaller wavenumbers than that in the single-crystal silicon (519.5 cm$^{-1}$), confirming tensile stress in poly-Si films, as would be expected from a volume contraction. By curve-fitting, the Raman shift and the full width at half magnitude (FWHM) of the spectra are plotted in Fig. 2-14(b). The Raman scattering energy is lower in the cantilever films than in the control SPC films, indicating the higher residual stress existing in the control polysilicon films. According to the following equation [41]:

$$\sigma\,(\text{MPa}) = -250\,\Delta\omega\,(\text{cm}^{-1}), \tag{2.4}$$

where $\sigma$ is the in-plane stress and $\Delta\omega = \omega_s - \omega_0$, the tensile stress in the control polysilicon film is ~300 MPa, whereas the stress in the cantilever film is only ~ 150 MPa. This reduction of tensile stress in the cantilever structure could result either because the cantilever film can laterally relax in the direction perpendicular to the cantilever length to relieve tensile stress due to the volume contraction, or because

removal of the underlying $SiO_2$ leads to a free motion of silicon atoms at the bottom surface of silicon films.  Less stress in the cantilever films should result in a lower strain energy $\Delta G_s$, and thus increase the driving force for the grain growth and grain growth velocity.

### 2.3.4    Effect of Underlying Oxide Removal on Intragranular Defect Density

The main defects within polysilicon grains crystallized by furnace annealing are microtwins and dislocations [21,24].  Microtwins in polysilicon grains occur on {111} planes [21,42].  Therefore, observation under <110> orientation will make the microtwins clearly visible in TEM, where the intersection line between the twin plane {111} and the surface plane {110} denotes the microtwin.  The difference in intragranular defect density between the control and the cantilever structures was measured in 60-nm-thick samples annealed at 600 C for 20 hr.  Figure 2-15 shows the dark-field images of silicon grains and their selected area diffraction patterns (from regions ~ 300 nm in diameter) in (a, b) control regions and (c, d) cantilever regions.  The observed grain orientations are <110> (indexed from the diffraction patterns) in both cases.  The high density of microtwins in the control-film grains is very obvious, giving rise to the extra spots and streaks in its diffraction pattern.  Although the polysilicon grains in the cantilever film (Fig. 2-15(c)) are not free of defects, the density of intragranular defects is much lower, and therefore, there are fewer extra spots and streaks in the diffraction pattern of Fig. 2-15(d) than in Fig. 2-15(b).  In the control sample (Fig. 2-15(a)), the defect-free area between defects observable under high resolution is ~ 25 nm in diameter on average, which is consistent with the previous work on polysilicon from SPC at 600 °C [21].  However, the defect-free area in the cantilever film reaches ~ 100 nm.  Defining a defect density as the inverse of the defect-free area, the intragranular defect density in the cantilever samples is almost one order of magnitude lower than that in the control samples (~ $10^{10}$ cm$^{-2}$ *vs.* ~ $10^{11}$ cm$^{-2}$).
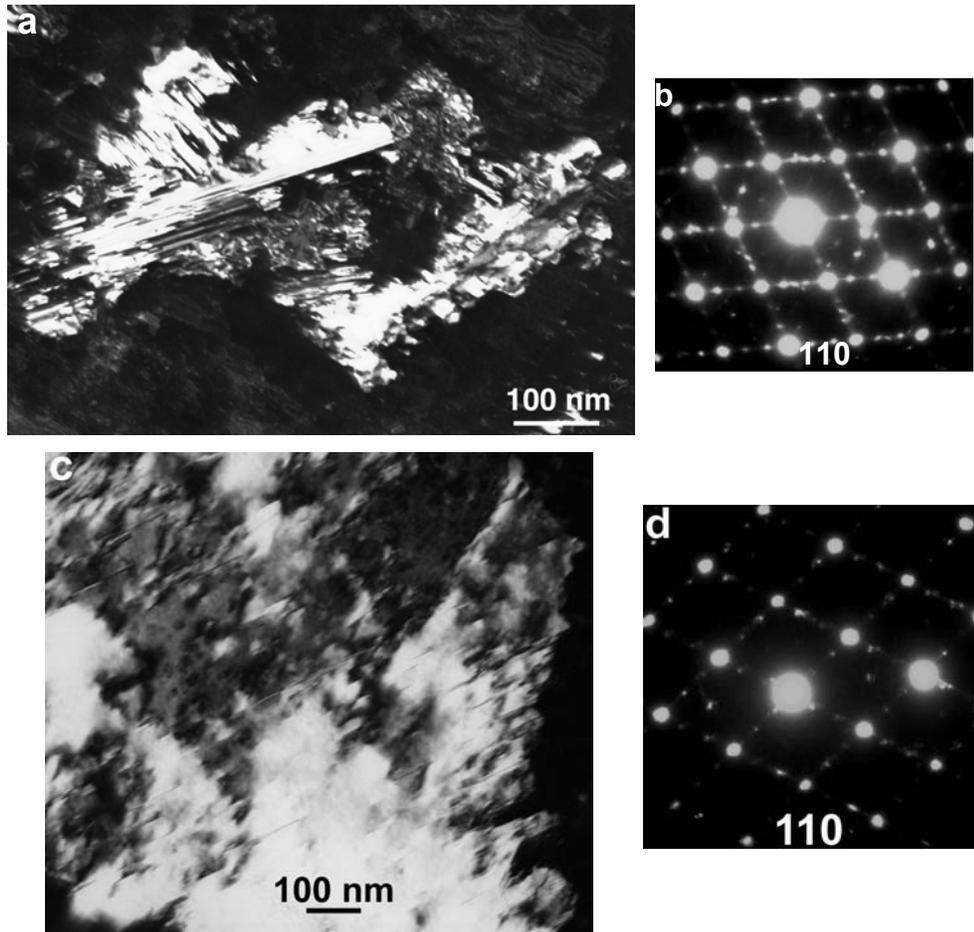
**Figure 2-15.** Dark-field TEM micrographs and their selected area (~ 300 nm in diameter) diffraction pattern in the control sample (a and b) and in the cantilever sample (c and d). Streaks and extra spots in the SADP of (b) and (d) with <110> crystallographic orientations parallel to the electron beam result from the intragranular defects.

High-magnification TEM observations on the intragranular defect density are shown in Fig. 2-16 with the electron-beam aligned to the <110> orientation of the grain. The microtwin lines are clearly visible, and the defect-free area in the control region (Fig. 2-16(a)) is much smaller than that in the cantilever region (Fig. 2-16(b)). A high-resolution TEM micrograph [Fig. 2-16(c)] on a very small area marked in Fig. 2-16(b) shows the atomic arrangements around the microtwins. On both sides of the microtwins, periodic (111) planes are clearly seen.
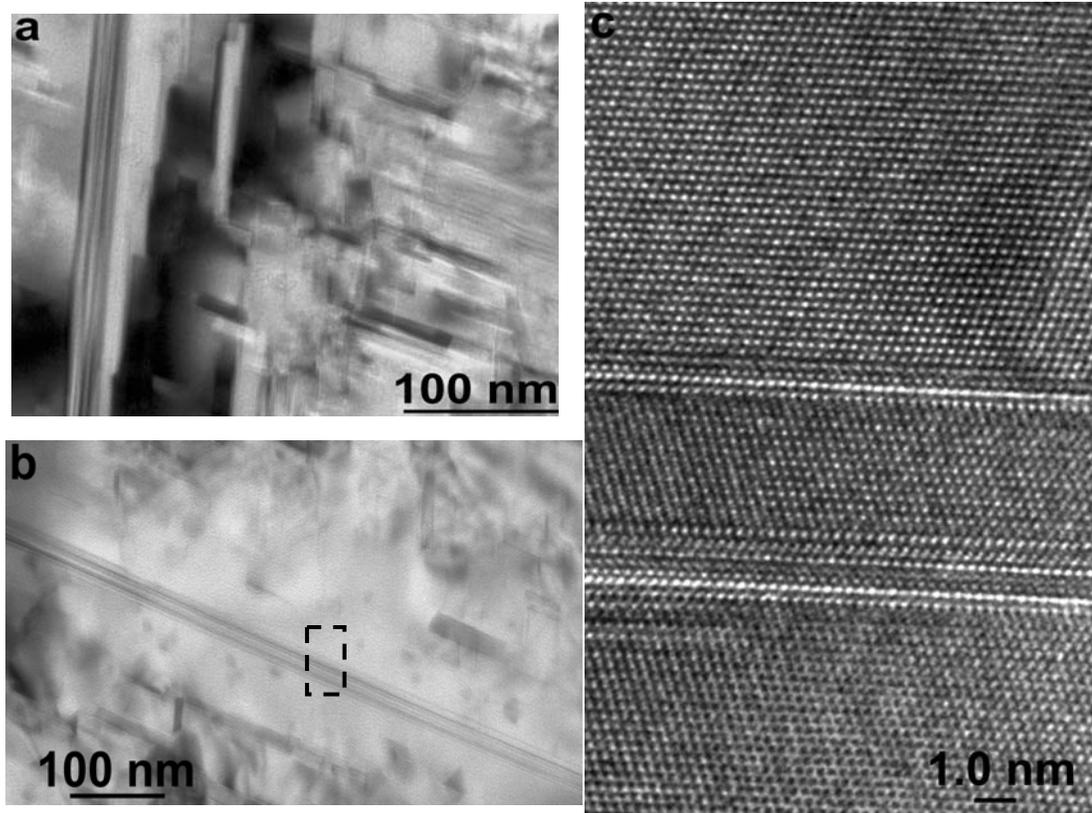


**Figure 2-16.** High-magnification bright-field TEM observations on polysilicon grains in (a) the control region and (b) the cantilever region. The electron beam was parallel to <110> crystallographic orientation of the silicon grains. (c) High-resolution TEM image of polysilicon films in the cantilever area marked by the dashed-lines in (b). Very regular lattice fringes with $d_{111}$ spacing around microtwins are very evident.

It is well known that small crystallites and high defect densities in polysilicon films cause asymmetry and broadening of the Raman peak of ~ 519.5 cm$^{-1}$ due to phonon scattering from the microcrystallite boundaries [43,44,45]. The crystallite size for this effect can be defined by both grain boundaries as well as intragranular defects [46]. The defect scattering destroys the lattice translational symmetry and relaxes the crystal momentum conservation rule governing the creation and decay of phonons, so that a smaller size of the microcrystallites increases the Raman FWHM [43-47]. In Fig. 2-14(b), the values of FWHM of Raman spectra in various regions are: cantilever polysilicon region, 5.8 cm$^{-1}$; control polysilicon region, 6.3 cm$^{-1}$; and single-crystalline silicon substrate, 3.3 cm$^{-1}$. This narrower peak in the cantilever region suggests a lower density of intragranular defects compared with that in the control region in qualitative agreement with our TEM observations.

The reason for reduced intragranular defect density is now discussed. As mentioned earlier, SPC of *a*-Si to polysilicon requires the rearrangement of silicon atoms at the interface of *a*-Si/SiO$_2$ and an accompanying volume contraction, both leading to tensile stress in the silicon films. To relieve this stress, crystalline defects (microtwins, dislocations, etc) develop during the nucleation stage [48] and growth stage [42]. This stress is largest at the *a*-Si/SiO$_2$ interface as the silicon atoms in the *a*-Si are strongly bound to the surface atoms of the underlying SiO$_2$ layer after deposition [49]. As the nucleation predominantly occurs at the interface, defect density is quite high in the typical SPC films. However, Morimoto *et al* [33] have demonstrated the formation of a nearly defect-free crystalline silicon film by removing the underlying SiO$_2$ before annealing during lateral solid-phase epitaxy (SPE) seeded from a [100] silicon substrate. In this work, removing the SiO$_2$ underlying the *a*-Si suppressed *a*-Si/SiO$_2$ interface nucleation, although the dominant nucleation is still expected to be at the top or bottom free surfaces of *a*-Si. Since the silicon atoms at the surface are only loosely bound to the native SiO$_2$ layer on a cantilever, the stress generated upon nucleation can be easily relieved, so fewer defects can be expected. During the subsequent lateral growth of grains in the cantilever, the easier rearrangement of silicon atoms at the surfaces and the

relaxation of stress from volume contraction in the silicon films during SPC also result in fewer intragranular defects being created.

## 2.4 Summary

Because of higher field-effect mobilities in poly-Si TFTs than in *a*-Si TFTs, SPC of *a*-Si films has been investigated. The fabricated SPC poly-Si TFTs with process temperature $\leq 600$ °C exhibit well-behaved electrical characteristics with field-effect mobilities of 30-40 cm$^2$/Vs for n-channel and 10-20 cm$^2$/Vs for p-channel TFTs, and a current ON/OFF ratio greater than $10^6$. However, midgap states and scattering centers from grain boundaries and intragranular defects in poly-Si films make poly-Si carrier mobilities much lower than single-crystalline silicon

It has been found that hydrogen plasma exposure of *a*-Si creates a seeding layer on top of the *a*-Si films and thus enhances SPC. This was used to control the location of poly-Si grains by spatially selective exposure to a hydrogen plasma. When the exposure area is smaller than 0.6 μm in diameter, a single grain is formed at the designed location. A further anneal causes the grain to grow laterally, and reach a 2.5-μm-diameter grain size.

By fabricating a free-standing silicon film without an underlying silicon dioxide, the quality of polysilicon films resulting from unseeded SPC of *a*-Si at 600 °C has been improved. The nucleation density has been decreased and the grain growth rate increased, leading to an average grain size up to 3.0 μm, 5 times larger than that in the films with underlying oxide. Furthermore, the intragranular defect density has been reduced by one order magnitude from $\sim 10^{11}$ cm$^{-2}$ to $\sim 10^{10}$ cm$^{-2}$. Intragranular defects (microtwins and dislocations) form to release the stress generated during SPC, which is due to atom rearrangements and volume contraction. The reduced intragranular defect density in a free-standing crystallized silicon film is thought to result from the easy release of this stress in the films.

## 2.5 Future Work

### 2.5.1 Gate-All-Around TFTs

By combining selective hydrogen plasma seeding with the underlying oxide removal, gate-all-around TFTs could be fabricated. The TFT channel would be located at the single-grain silicon film with a low density of intragranular defects by combining the two main advances we found in this chapter. The fabrication process is briefly shown in Fig. 2-17. First, a small hole is opened in a $SiN_x$ mask so that the $a$-Si in the hole is selectively exposed to a hydrogen plasma (Fig. 2-17a). After the underlying oxide is removed, the $a$-Si film for the TFT channel is crystallized into single-grain silicon with low density of intragranular defects, while the source/drain are still composed of "normal" poly-Si films (Fig. 2-17b). The subsequent process is similar to that of gate-all-around MOSFETs [50]. A CVD oxide will be deposited on both surfaces of transistor channel, followed by a poly-Si film as gate. The next steps are gate patterning, dopant ion implantation and formation of metal contacts. Due to the improved poly-Si quality in the transport channel, high performance in this gate-all-around poly-Si TFT is expected.
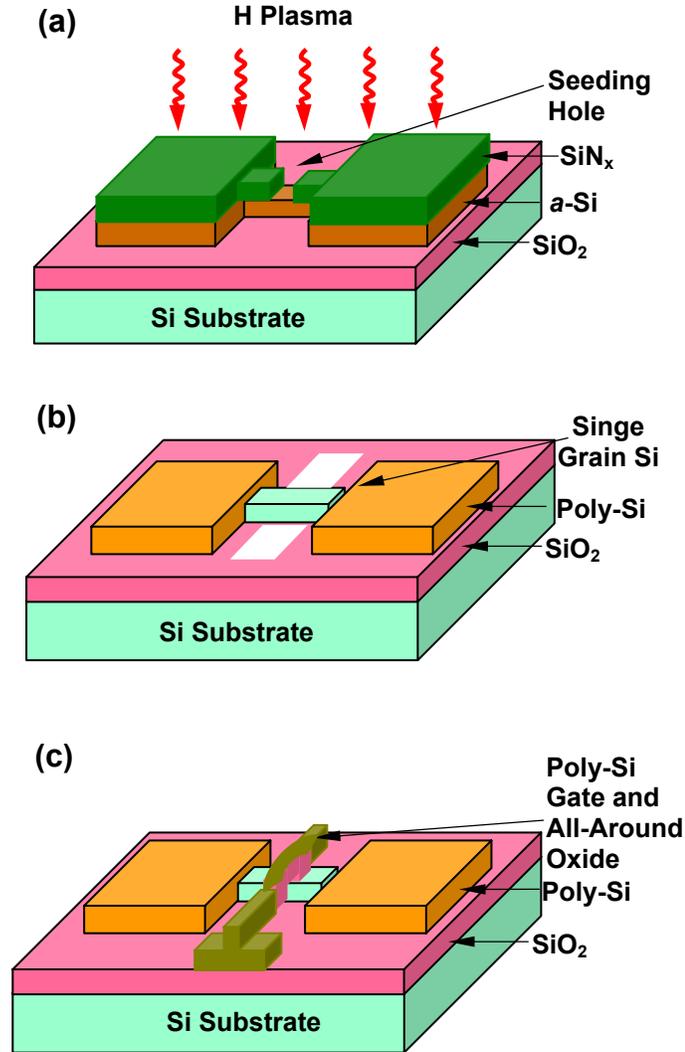
**Figure 2-17.**  Fabrication process of gate-all-around TFTs with channel on a single-grain poly-Si film with less intragranular defects.  (a) Selective hydrogen plasma seeding to a small area of a-Si; (b) underlying oxide removal and furnace anneal; (c) deposition of all-around gate oxide and poly-Si gate.

# References

[1] T. Morita, S. Tsuchimoto, and N. Hashizume, "The low temperature polysilicon TFT technology for manufacturing of active matrix liquid crystal displays", *Mater. Res. Soc. Symp. Proc.*, **345**: 71-80 (1994).

[2] Y. He, R. Hattori, and J. Kanicki, "Improved A-Si : H TFT pixel electrode circuits for active-matrix organic light emitting displays", *IEEE Trans. Elec. Dev.*, **48**: 1322-1325 (2001).

[3] J. C. Goh, H. J. Chung, J. Jang, C. H. Han, "A new pixel circuit for active matrix organic light emitting diodes", *IEEE Elec. Dev. Lett.*, **23**: 544-546 (2002).

[4] K. Long, Private communication.

[5] J. S. Im and R. S. Sposili, "Crystalline Si films for integrated Active-Matrix Liquid-Crystal displays," *Mat. Res. Soc. Bulletin*, pp. 39-48, March, 1996.

[6] P. Mei, J.B. Boyce, D.K. Fork, G. Anderson, J. Ho, J. Lu, M. Hack and R. Lujan, "Hybrid amorphous and polycrystalline silicon devices for large-area electronics," *Mat. Res. Soc. Symp. Proc.*, **507**: 3-12 (1999).

[7] M. K. Hatalis and D. W. Greve, "Large grain polycrystalline silicon by low temperature annealing of low-pressure deposition amorphous silicon films", *J. Appl. Phys.*, **63**: 2260-2266 (1988).

[8] R. Sinclair, J. Morgiel, A. S. Kirtikar, I. W. Wu, and A. Chiang, "Direct observation of crystallization in silicon by in-sity high-resolution electron-microscopy", *Ultramicroscopy*, **51**: 41 (1993).

[9] K. Zellama, P. Germain, S. Squelard, J. C. Bourgoin, and P. A. Thomas, "Crystallization in amorphous silicon," *J. Appl. Phys.*, **50**: 6995-7000 (1979).

[10] L. Csepregi, E. F. Kennedy, J. W. Mayer, and T. W. Sigmon, "Substrate-orientation dependence of the epitaxial regrowth rate from Si-implanted amorphous Si," *J. Appl. Phys.*, **49**: 3906-3911 (1978).

[11] R. B. Iverson and R. Reif, "Recrystallization of amorphized polycrystalline silicon films on SiO2: Temperature dependence of the crystallization parameters," *J. Appl. Phys.*, **62** 1675-1681 (1987).

[12] C. Licoppe and Y. I. Nissim, "Impurity-induced enhancement of the growth rate of amorphized silicon during solid-phase epitaxy: A free-carrier effect", *J. Appl. Phys.,* **59**: 432-438 (1986).

[13] S.-W. Lee and S.-K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Letters*, **17**: 160-162 (1996).

[14] Z. Jin, G. A. Bhat, M. Yeung, H. S. Kwok, and M. Wong, "Nickel induced crystallization of amorphous silicon films," ", *J. Appl. Phys.*, **84**: 194-200 (1998).

[15] V. Subramanian and K. C. Saraswat, "High-performance germanium-seeded laterally crystallized TFT's for vertical device integration," *IEEE Transactions on Electron Devices*, **45**: 1934-1939 (1998).

[16] A. Yin and S. J. Fonash, "Oxygen-plasma-enhanced crystallization of *a*-Si:H films on glass," *J. Vac. Sci. Techn. A*, **12**: 1237-1240 (1994).

[17] K. Pangal, J. C. Sturm, S. Wagner, and T. H. Buyuklimanli, "Hydrogen plasma-enhanced crystallization of hydrogenated amorphous silicon films", *J. Appl. Phys.*, **85**: 1900-1906 (1999).

[18] X.-Z. Bo, N. Yao, S. Wagner, and J. C. Sturm, "Spatially selective single-grain silicon films induced by hydrogen plasma seeding", *J. Vac. Sci. Techn. B*, **20**: 818-821 (2002).

[19] T. I. Kamins and Marcoux, "Hydrogenation of transistors fabricated in polycrystalline silicon films," *IEEE Electron Device Letters*, **1**: 159-161 (1980).

[20] K. Pangal, "Hydrogen-plasma-enhanced crystallization of hydrogenated amorphous silicon films: fundamental mechanisms and applications", Ph.D. thesis, Princeton University, Nov. 1999.

[21] L. Haji, P. Joubert, J. Stoemenos, and N. A. Economou, "Mode of growth and microstructure of polycrystalline silicon obtained by solid-phase crystallization of an amorphous silicon film", *J. Appl. Phys.,* **75**: 3944-3952 (1994).

[22] J. Kedzierski *et al*, IEDM, p. 247, 2002.

[23] T. Kamins, "Polycrystalline silicon for integrated circuit applications", Kluwer Academic Publishers, p. 159, (1988).

[24] J. H. Kim, J. Y. Lee and K. S. Nam, "High-resolution transmission electron microscopy study of solid phase crystallized silicon thin films on $SiO_2$: Crystal growth and defects formation", *J. Appl. Phys.*, **77**: 95-102 (1995).

[25] H. Kumomi, and T. Yonehara, "Manipulation of nucleation sites in solid-state Si crystallization", *Appl. Phys. Lett.*, **59**, 3565-3567 (1991).

[26] K. Makihira, and T. Asano, "Enhanced nucleation in solid-phase crystallization of amorphous Si by imprint technology", *Appl. Phys. Lett.*, **76**, 3774-3776 (2000).

[27] J. Gu, S. Y. Chou, N. Yao, H. Zandbergen, and J. K. Farrer, "Single-crystal Si formed on amorphous substrate at low temperature by nanopatterning and nickel-induced lateral crystallization", *Appl. Phys. Lett.*, **81**: 1104-1106 (2002).

[28] Y. C. Liu, M. D. Deal, K. C. Saraswat, and J. D. Plummer, "Single-crystalline Si on insulator in confined structures fabricated by two-step metal-induced crystallization of amorphous Si", *Appl. Phys. Lett.*, **81**: 4634-4636 (2002).

[29] K. Pangal, J. C. Sturm and S. Wagner, "Integration of amorphous and polycrystalline silicon thin-film transistors through selective crystallization of amorphous silicon", *Appl. Phys. Lett.*, **75**: 2091-2093 (1999).

[30] X. –Z. Bo, N. Yao, and J. C. Sturm, "A novel method for direct TEM study of microstructure of polysilicon films crystallized with and without underlying oxide", *Microsc. Microananl.*, **8**: 1210-1211 (2002).

[31] K. Nakazawa, "Recrystallization of amorphous silicon films deposited by low-pressure chemical vapor deposition from $Si_2H_6$ gas", *J. Appl. Phys.*, **69**: 1703-1706 (1991).

[32] M.-K. Ryu, S.-M. Hwang, T.-H. Kim, K.-B. Kim, and S.-H. Min, "The effect of surface nucleation on the evolution of crystalline microstructure during solid phase crystallization of amorphous Si films on $SiO_2$", *Appl. Phys. Lett.* **71**: 3063-3065 (1997).

[33] Y. Morimoto, Y. Jinno, K. Hirai, H. Ogata, T. Yamada, and K. Yoneda, "Influence of the grain boundaries and intragrain defects on the performance of poly-Si thin film transistors", *J. Electrochem. Soc.* **144**: 2495 (1997).

[34] F. Petinot, F. Plais, D. Mencaraglia, P. Legagneux, C. Reita, O. Huet, and D. Pribat, "Defects in solid phase and laser crystallised polysilicon thin film transistors", *J. Non-Crystalline Solids*, **227-230**: 1207 (1998).

[35] S. Girginoudi, D. Girginoudi, A. Thanailakis, N. Georgoulas, and V. Papaioannou, "Electrical and structural properties of poly-Si films grown by furnace and rapid thermal annealing of amorphous Si", *J. Appl. Phys.* **84**: 1968-1972 (1998).

[36] T. Serikawa, "Low-temperature fabrication of high-mobility poly-Si TFTs for large-area LCDs", *IEEE Trans. Electron Devices*, **36**: 1929-1933 (1989).

[37] X.-Z. Bo, N. Yao, R. Shieh, T. S. Duffy, and J. C. Sturm, "Large-grain polycrystalline silicon films with low intragranular defect density by low-temperature solid-phase crystallization without underlying oxide", *J. Appl. Phys.*, **91**: 2910-2915 (2002).

[38] R. B. Iverson and R. Reif, "Recrystallization of amorphized polycrystalline silicon films on $SiO_2$: Temperature dependence of the crystallization parameters", *J. Appl. Phys.*, **62**: 1675-1681 (1987).

[39] C. Spinella, and S. Lombardo, "Crystal grain nucleation in amorphous silicon", *J. Appl. Phys.*, **84**: 5383-5414 (1998).

[40] I. De Wolf, "Micro-Raman spectroscopy to study local mechanical stress in silicon integrated circuits", *Semicond. Sci. Technol.*, **11**, 139-154 (1996).

[41] S. Boultadakis, S. Logothetidis, and S. Ves, "Comparative study of thin poly-Si films grown by ion implantation and annealing with spectroscopic ellipsometry, Raman spectroscopy, and electron microscopy", *J. Appl. Phys.*, **72**: 3648-3658 (1992).

[42] R. Drosd and J. Washburn, "Some observations on the amorphous to crystalline transformation in silicon", *J. Appl. Phys.*, **53**: 397-403 (1982).

[43] Z. Iabal, S. Vepĭek, A. P. Webb, and P. Capezzuto, "Raman scattering from small particle size polycrystalline silicon", *Solid State Commun.*, **37**: 993 (1981).

[44] H. Richter, Z. P. Wang, and L. Ley, "The one phonon Raman spectrum in microcrystalline silicon", *Solid State Commun.*, **39**: 625 (1981).

[45] I. H. Campbell, and P. M. Fauchet, "The effects of microcrystal size and shape on the one phonon Raman spectra of crystalline semiconductors", *Solid State. Commun.*, **58**: 739 (1986).

[46] J. Gonzalez-Hernandez, G. H. Azarbayejani, R. Tsu, and F. H. Pollak, "Raman, transmission electron microscopy, and conductivity measurements in molecular beam deposited microcrystalline Si and Ge: A comparative study", *Appl. Phys. Lett.*, **47**: 1350-1352 (1985).

[47] J. Macía, E. Martín, A. Pérez-Rodríguez, J. Jiménez, J.R. Morante, B. Aspar, and J. Margail, "Raman micro structural analysis of silicon-on-insulator formed by high dose oxygen ion implantation: As-implanted structures", *J. Appl. Phys.*, **82**: 3730-3735 (1997).

[48] D. Pribat, P. Legagneux, F. Plais, C. Reita, F. Petinot, and O. Huet, "Low temperature polysilicon materials and devices,", *Mater. Res. Soc. Symp. Proc.*, **424**: 127-139 (1997).

[49] H. Kawarada, T. Ueno, and I. Ohdomari, "Characterization of roughness and defects at an Si/SiO$_2$ interface formed by lateral solid phase epitaxy using high-resolution electron microscopy", *J. Appl. Phys.*, **63**: 2641-2644 (1988).

[50] E. Leobandung, J. Gu, L. J. Guo, and S. Y. Chou, "Wire-channel and wrap-around-gate metal-oxide-semiconductor field-effect transistors with a significant reduction of short channel effects", *J. Vac. Sci. Techn. B*, **15**: 2791-2794 (1997).

# Chapter 3

---

# A-SI DEPOSITION FOR 3-D SILICON PHOTONIC BANDGAP CRYSTALS

## 3.1　Introduction

Photonic bandgap crystals (PBCs) are composed of materials with periodic dielectric constants, which create a range of "forbidden" frequencies called a photonic bandgap. Photons with energy lying in the bandgap cannot propagate in any direction through the medium [1,2]. Similar to an electronic bandgap, which is due to a periodic potential in atoms, a photonic bandgap is caused by periodic refractive indexes in structures. Optical communications systems operate in the near-infrared (1.3 µm and 1.55 µm), which means that a lattice constant of a photonic crystal must have dimensions of roughly a micrometer. This is ~ 2,000 times larger than the lattice constant of semiconductor crystals [3].

PBCs provide opportunities for photonic devices to confine and mold light with applications in optical waveguides, lossless fibers, high-Q lasers and optical integrated circuits. Some of these applications of PBCs require three-dimensional (3-D) photon confinements to hinder light diffraction loss in the $z$-direction perpendicular to the plane of two dimensional (2-D) PBCs [4]. Conventional nanofabrication methods (e-beam lithography and RIE) have been applied to fabricate 3-D PBCs in Si [5] and GaAs [6]. However, the requirement for minimal structure fluctuations to avoid smearing out or weakening photonic bandgap effects [7] is very stringent, which makes alignment of

41

layers in layer-by-layer fabrication complicated and time-consuming. For example, during the fabrication of 3D PBCs in GaAs, 0.7-µm-period stripes are required with an accuracy of 30 nm [6].
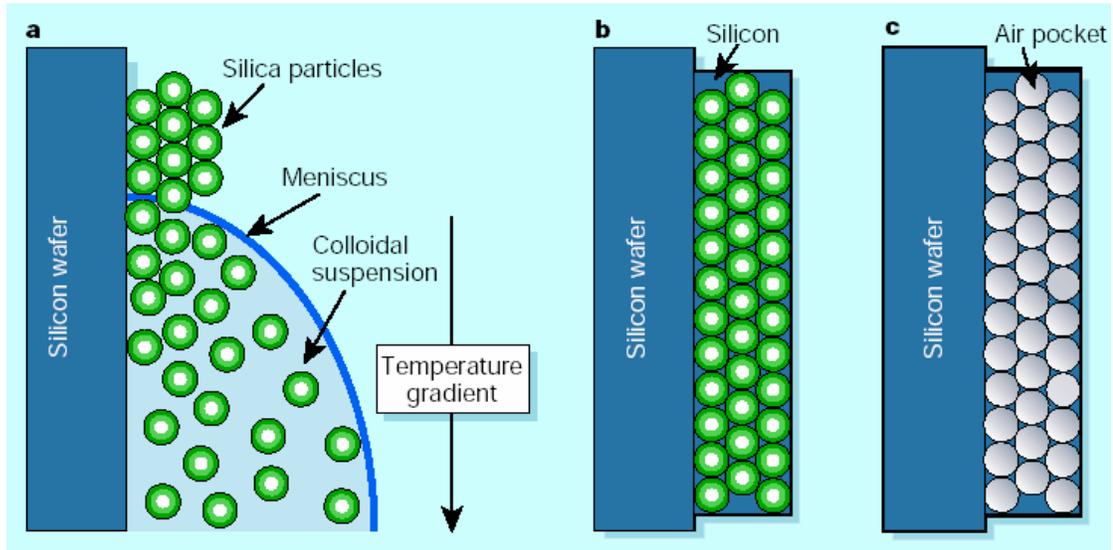


**Figure 3-1.** Fabrication process of 3-D silicon PBCs. (a) Self-assembly of synthetic opals starting from a silica colloid to tan ordered 3-D template, (b) voids between silica spheres filled with silicon by CVD, and (c) removal of the silica spheres by wet etching [11].

A potentially simpler and cheaper approach for creating 3-D periodic structures is the natural assembly of colloidal microspheres [8,9]. Micron-scale colloidal spheres (e.g. polymer or silica) can be induced to spontaneously form a solid, three-dimensionally periodic structure with a face-centered cubic (*fcc*) lattice. In nature, this process leads to gemstone opals. In analogy, sub-micron spheres assembled in the laboratory are referred to as *synthetic opals*. Unfortunately, synthetic opals are not particularly interesting photonic crystals. Silica has a relatively low refractive index (~1.4), which is lower than the requirement for the refractive index ($n > 2.85$) to form a 3-D photonic bandgap in an *fcc* crystal structure [10]. However, synthetic opals can work as a template to construct PBCs. The template contains interstitial spaces between

the SiO$_2$ spheres, which can be filled with a material of high-refractive index, such as Si ($n = 3.5$). The template material SiO$_2$ could subsequently be removed, leading to 3-D periodic structures made of air spheres and semiconductor materials with relative high refractive index. These are called *inverted opals*. The whole process for 3-D Si PBCs is shown in Fig. 3-1 [11].

Bulk-like opals by the sedimentation of silica particles have been demonstrated in Ref. [9]. However, this sedimentation leads to a polycrystalline structure with unwanted boundaries, which can easily close the bandgap because of the localized photonic states within it [7,12]. Bulk opals are also difficult to integrate with devices. In this chapter, we used a self-assembly method to deposit thin-film opals on silicon substrate, details of which can be found in [13] and [14]. The multi-layer opal has much larger single-crystalline area. Inversion of the opals was made by the conformal growth of silicon using a commercial available low-pressure CVD reactor. Patterning of the inverted opals by photolithography and RIE provides a future method to integrate photonic devices with microelectronic circuits on a same silicon wafer. This work was done in collaboration with Dr. David Norris and Dr. Yuri Vlasov of NEC Labs in Princeton.

## 3.2    Self-Assembled Opals

Monodispersed colloidal silica spheres were synthesized by a chemical method. The sphere diameter can be designed from 0.5 μm to 2.0 μm. As shown in Fig. 3-1(a), a silicon wafer is vertically inserted into the silica colloid solution. Due to capillary forces, silica particles spontaneously organize themselves onto the substrate surface at the meniscus. As the meniscus is slowly swept the silicon substrate by solvent evaporation, a thin, planar, well-ordered structure is formed on the silicon substrate. To avoid the problem of particle sedimentation, a temperature gradient from 80 °C at the bottom to 65 °C at the top is applied to allow convection flow that constantly provides particles to the meniscus region. The details are in Ref. [14].
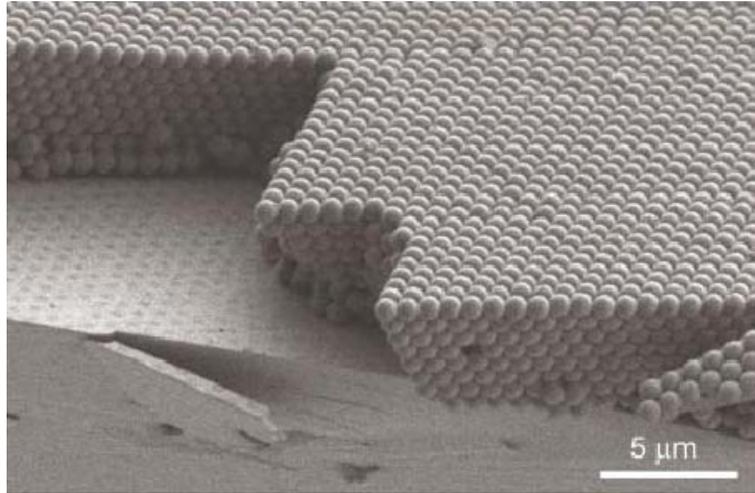
**Figure 3-2.** SEM cross-section image of thin planar opals self-assembled on silicon substrate from silica spheres with diameter of 855 nm.

Self-assembled opals were prepared by Dr. Norris and Dr. Vlasov of NEC labs in Princeton. The SEM image in Fig. 3-2 shows a self-assembled opal made with silica spheres with diameter of 855 nm. Close-packed spheres form an *fcc* structure. Compared with the sedimented opals, it has a much lower defect density, with $\sim 1\%$ stacking faults and $\sim 10^{-3}$ point defects per unit cell. Using this method, centimeter-size opals with 20 close-packed layers were coated on the silicon substrate. The single-crystalline domain size was 1mm $-$ 1 cm, $10 - 100$ times larger than the best sedimented opals.

## 3.3　Infiltration of *a*-Si by CVD

### 3.3.1　A-Si Deposition by PECVD

Due to the low refractive index of silica ($n \sim 1.4$), self-assembled opals cannot form a photonic bandgap. The infiltration of the interstitial space between the spheres

by semiconductor materials with high refractive indices ($n > 2.85$) becomes necessary. Table 3-1 shows conventional semiconductor materials and their refractive index [15]. Since silicon is the primary material in the IC industry, is transparent to light with wavelengths of 1.3 µm and 1.5 µm (as used in telecommunication), and has a large refractive index $n = 3.5$, it was first chosen to fill the voids in the synthetic opals in our experiment.

**Table 3-1.** Semiconductor materials and their refractive index and absorption edge

| Semiconductor | Index of refraction (at specified wavelength) | Absorption Edge (at 300 K) |
|---|---|---|
| CdSe | 2.75 (0.75 µm) | 0.71 µm |
| GaAs | 3.54 (0.95 µm) | 0.87µm |
| InP | 3.33 (1.0 µm) | 0.97 µm |
| Si | 3.53 (1.1 µm) | 1.10 µm |
| Ge | 4.12 (2.0 µm) | 1.87 µm |
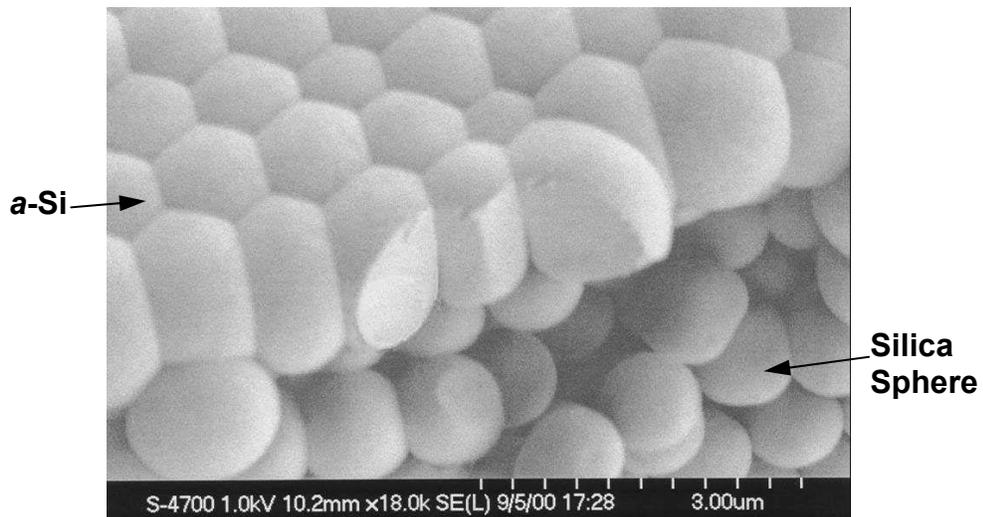


**Figure 3-3.** SEM cross-section image showing PECVD *a*-Si piled up on the top surface, blocking *a*-Si infiltration into the opal template.

Standard PECVD growth of *a*-Si on self-assembly opals was tried initially. SiH$_4$ gas was introduced into the chamber at a rate of 50 sccm. The pressure and temperature were kept at 500 mtorr and 250 °C, respectively. During *a*-Si deposition, the RF power was ~ 18 mW/cm$^2$. The deposition rate was ~ 1.5 nm/s [16]. After *a*-Si deposition, the opals were observed by SEM (Fig. 3-3). It is very clear that the silica particles are not coated by *a*-Si deposition except on the top surface of template. During PECVD growth, the deposition of *a*-Si on top surface first occurred, blocking the diffusion path of SiH$_4$ into rest of the opal.

To enhance the diffusion of the silane during deposition to try to better infiltrate the pores, the silane gas was diluted by hydrogen at 1: 5 and 1: 10 ratios. However, the same phenomenon happened. Amorphous silicon could not fill the interstitial space between silica spheres. This may be due to the high growth rate of *a*-Si enhanced by a plasma.

### 3.3.2 Si Film Deposition by LPCVD

*Grain Size and Growth Rate*

Low-pressure chemical vapor deposition (LPCVD) was then used to attempt infiltration of the opals. The grain size and growth rate with varying deposition temperatures were first characterized for deposition onto an oxidized silicon substrate. A diluted SiH$_4$ (2% in N$_2$) flow at 1500 sccm was used at a pressure of 800 mtorr for 5.5 hr. Because no plasma is used, a higher growth temperature is needed. Cross-section SEM images show silicon growth at 550 °C in Fig. 3-4(a), 600 °C in (b), and 625 °C in (c). As mentioned in chapter 1, silicon films grown at 550 °C from silane without plasmas or special crystallization methods are amorphous, and those grown at 625 °C are polycrystalline. The 600 °C growth is a mixture of *a*-Si and poly-Si. Faceting of poly-Si growth leads to the rugged surface with grain size ~ 200 nm in Fig. 3-4(c), while the *a*-Si film surface in Fig. 3-4(a) is rather smooth.
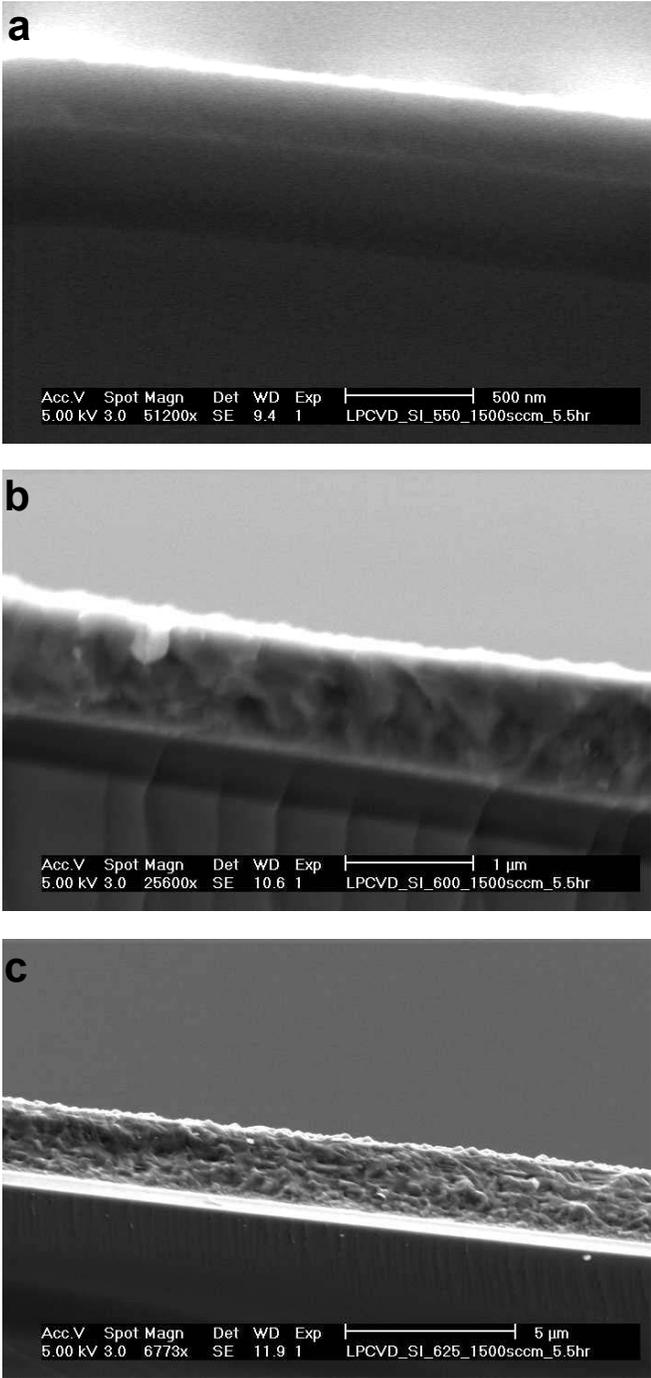
**Figure 3-4.** SEM image of Si films by LPCVD on an oxidized silicon substrate at a temperature of 550 °C in (a), 600 °C in (b), and 625 °C in (c).

The growth rate was characterized by measuring the film thickness from cross-section SEM images, and is summarized in Fig. 3-5. The growth rate exponentially increases from 0.9 nm/min at 550 °C to 7.6 nm/min at 625 °C. The activation energy of the growth rate was found to be ~ 1.8 eV.
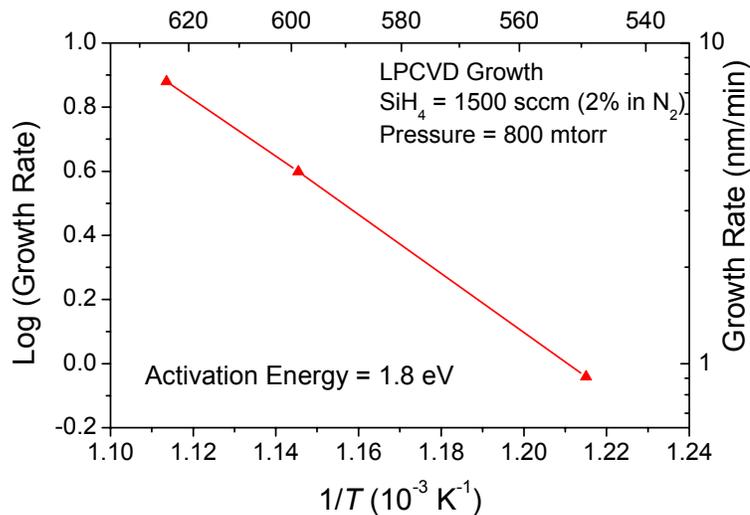


**Figure 3-5.** Growth rate of LPCVD Si films *vs.* growth temperature, keeping $SiH_4$ (2% in $N_2$) flow at 1500 sccm and pressure at 800 mtorr.

*Si Growth on Opal Templates*

The deposition of LPCVD Si on synthetic opal templates was performed at different temperatures. Top-view SEM observations (Fig. 3-6) on opal surfaces show not only surface roughness varying with deposition temperatures but also conformity to the opal spheres. Poly-Si grown at 625 °C exhibits a rough surface (Fig. 3-6c), and premature deposition on the top surface obstructs gas transport to the inner most layers of the 3-D opals. The surface of *a*-Si grown at 550 °C (Fig. 3-6a) is smooth, and conformal growth to silica spheres was achieved. This homogeneous infiltration of Si is demonstrated in Fig. 3-7.
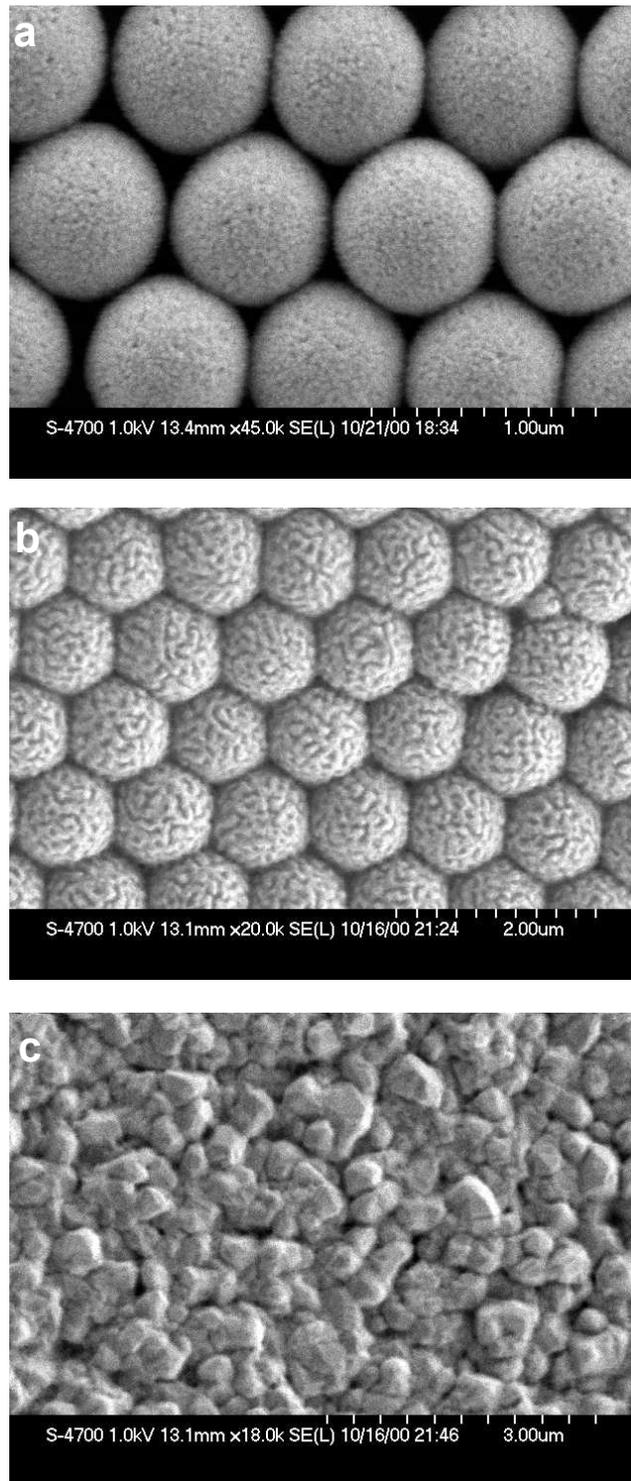
**Figure 3-6.** SEM image of Si films grown by LPCVD on opal templates at temperature of (a) 550 °C, (b) 600 °C, and (c) 625 °C.
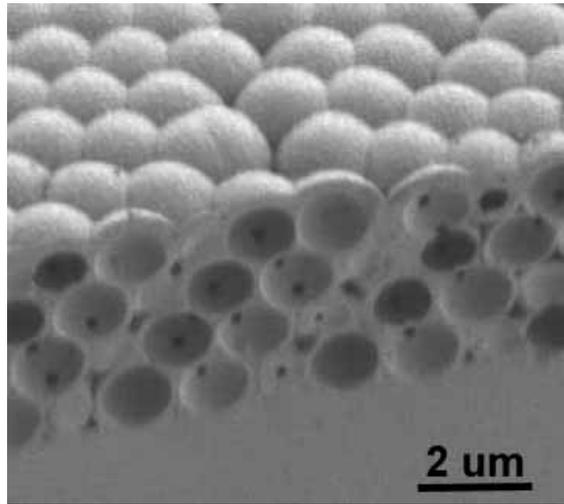
**Figure 3-7.** SEM cross-section image of opal structure after Si CVD infiltration at 550 °C.
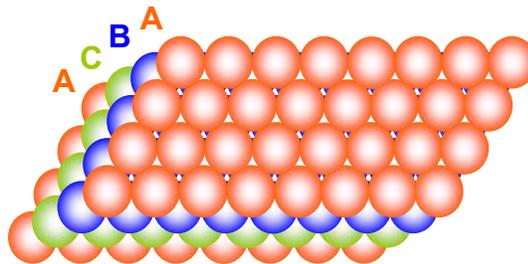


**Figure 3-8.** Close-packed <111> planes in *fcc* structure.

In our deposition process, the highly diluted $SiH_4$ gas (2% in $N_2$) results in extremely low silane partial pressure (~ 16 mtorr). It is the low partial pressure of $SiH_4$ gas and the low growth rate at 550 °C that result in a long mean free path of Si diffusion and finally the conformal infiltration of *a*-Si into opal templates. Figure 3-8 shows *fcc* closed-packed <111> planes, arranged in the order of ABCABCA…. The shortest

length from top layer A to another A through B and C layers is ~ 3.2$d$, where $d$ is the diameter of spheres.  This suggests, for a 4-layer opal template with 1-μm-diameter silica spheres, that the mean free path should be greater than 3.2 μm for silicon diffusion before the deposition occurs, otherwise initial deposition will block the infiltration to the bottom of Si substrate.

Since self-assembled opals are fragile, care should be taken during the Si deposition.  The thermal impact from the thermal expansion at the beginning of the deposition from room temperature to 550 °C not only causes the opal to crack, but also leads to stacking faults and boundaries within single-crystalline opal domains. Therefore, during the CVD growth, the opal samples were laid horizontally on a silicon carrier wafer.  The loading temperature of furnace was reduced to 250 °C instead of 550 °C, and then slowly increased to 550 °C with inert $N_2$ flowing.  The process is reversed for sample unloading.  Due to the variance of refractive index with the concentration of hydrogen in hydrogenated $a$-Si films [17], SPC was performed in the same furnace by heating to 600 °C after $a$-Si deposition,.  A smooth surface was maintained.

In the previous work of Ref. [9], the CVD of silicon was used to fill the bulk-opals prepared by silica sphere sedimentation.  In a custom-built apparatus, disilane gas was first condensed into the pores of the opal at cryogenic temperatures and subsequently decomposed by heating to 250 °C − 350 °C at a pressures of 200 torr. Although homogeneous infiltration was demonstrated for sedimented opals, this process is not compatible with conventional silicon fabrication process.  Chemical reaction time was ~ 24 hr.  Furthermore, the optical characteristics of their structures did not conclusively show the presence of photonic bandgap.  In our process, a commercially available LPCVD reactor was used.  An advantage of LPCVD is that it is the standard Si deposition technique for the microelectronics industry.  We have achieved conformal growth of silicon on silica spheres, filling ~ 40-layer opals in ~ 5.5 hr.

## 3.4    Inversion of Opal Structures
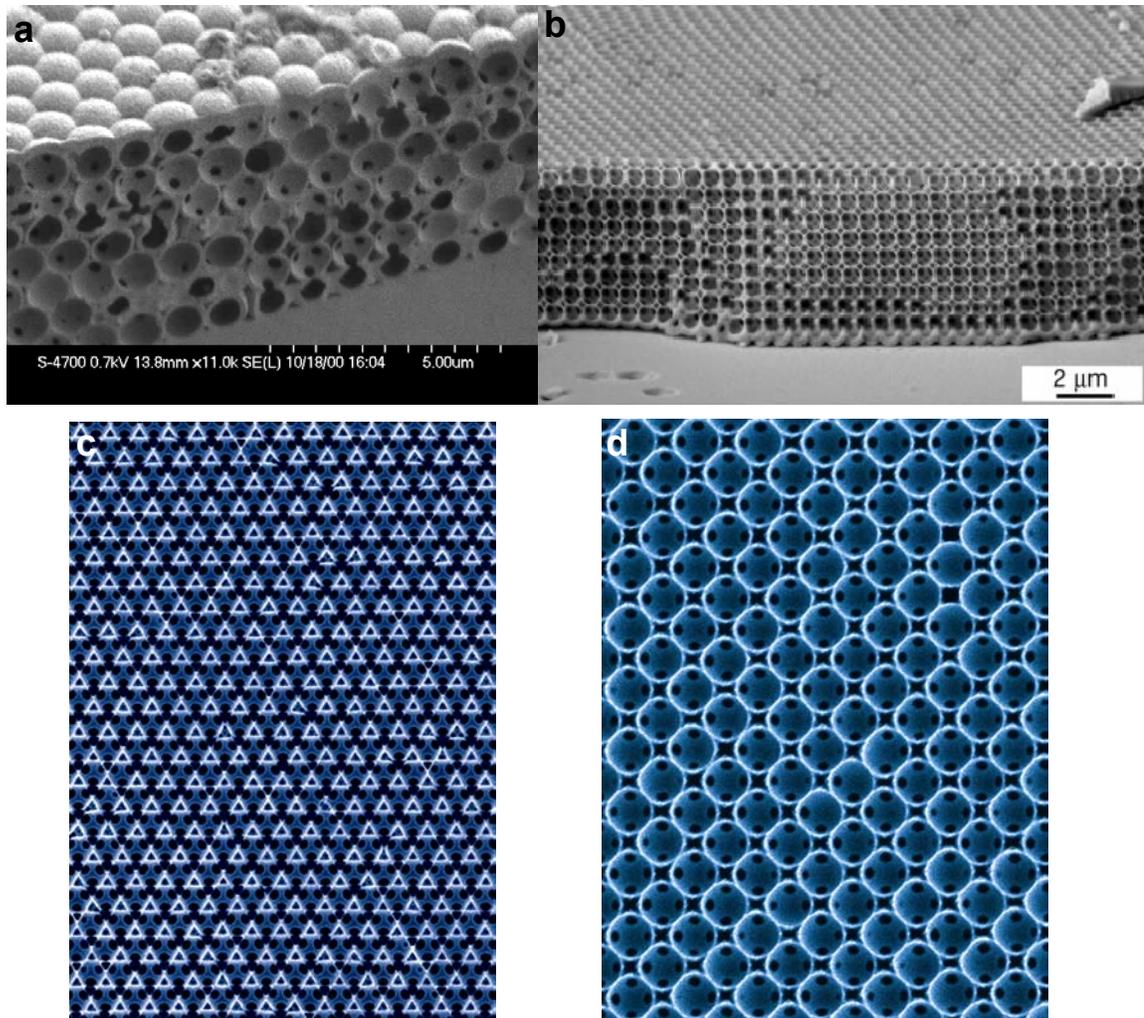


**Figure 3-9.**  SEM images of silicon photonic crystals with inverted opal stuctures.  (a) and (b) are cross-sections and (c) and (d) are top-views of PBCs along *fcc* [111] (a and c) and [100]  (b and d) orientations.

To form inverted opals, the silica spheres must be removed from the opal templates. After silicon CVD growth, the outer surface of the planar opal template is covered by silicon. 10: 1 buffered oxide etchant (BOE) etches $SiO_2$ fast with a rate of ~ 1nm/s for thermal oxide, but the etch rate for Si is much slower. In order to open the etching path to the $SiO_2$, the silicon coating on top of the template surface was first selectively removed by RIE with $SiO_2$ spheres as an "etch-stop". Subsequent 10:1 BOE soaking for 1 hr removes the silica template completely, forming planar inverted opals on the silicon wafer. Their cross-section and top-view SEM images are shown in Fig. 3-9 for *fcc* crystals with a [111] vertical orientation in (a) and (c) and a [100] vertical orientation in (b) and (d). [100] surface-oriented opals have been created in our samples by changing self-assembly condition [18,19], although usually a [111] surface is resulted. From the cross-section SEM image, we can see that the silicon of the thin planar inverted opals was attached to the Si substrate, which provides significant mechanical stability.

## 3.5    Optical Characteristics of Inverted Opals [19]

The optical spectra of the inverted opals were obtained either by a monochromator or a Fourier transform infrared spectrometer to explore the existence of a photonic bandgap [19]. The apparatus was attached to an optical microscope, allowing transmission spectra to be obtained with a spatial resolution ~ 2 μm [20]. The absolute reflectance was determined with an experimental accuracy of ± 5% by comparing the sample reflection with that from a silver mirror. Typical reflectance spectra, measured normal to the (111) surface for 8-layer-thick samples, are presented in Fig. 3-10(a). Near-unity reflectance is observed both at a waverlength of ~1.46 μm and at a wavelength of ~ 1.3 μm, in good agreement with calculations [19,21].
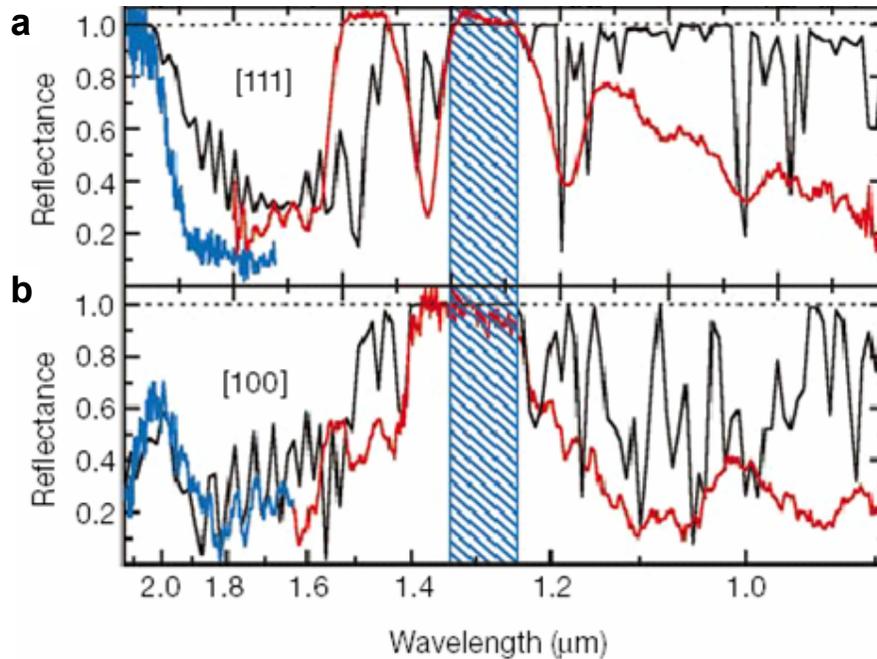
**Figure 3-10.** Optical reflectance spectra of silicon inverted opals with incident light normal to [111] in (a) and [100] in (b) directions. The red and blue lines are experimental results from *fcc* samples with *a* =1040 nm and *a* = 841 nm, respectively. For comparison a calculation is shown in black for a silicon coating sphere radius of 458 nm and an air sphere radius of 354 nm [19].

The crucial test of a photonic bandgap is to examine whether this high reflectance is maintained for directions other than [111]. Fortunately, crystalline regions of [100] surface orientation can be found in our samples (Fig. 3-9 b and d). In Fig. 3-10(b), reflection spectra are presented for such [100]-oriented regions, 8 layers thick. As in the [111] data (Fig. 3-10a), the bandgap region is characterized by a broad 'square-top' reflection peak with near-unity reflectance at wavelength ~ 1.3 μm. Comparison of the spectra for both [111] and [100] directions indicates that near-unity reflectivity is maintained for both directions at a broad range of frequencies around 1.3 μm, which is expected by theory for the bandgap. Thus, 3-D planar silicon PBCs have

been obtained directly on a Si wafer. This is the first time that a 3-D photonic bandgap has been clearly shown in self-assembled structures.
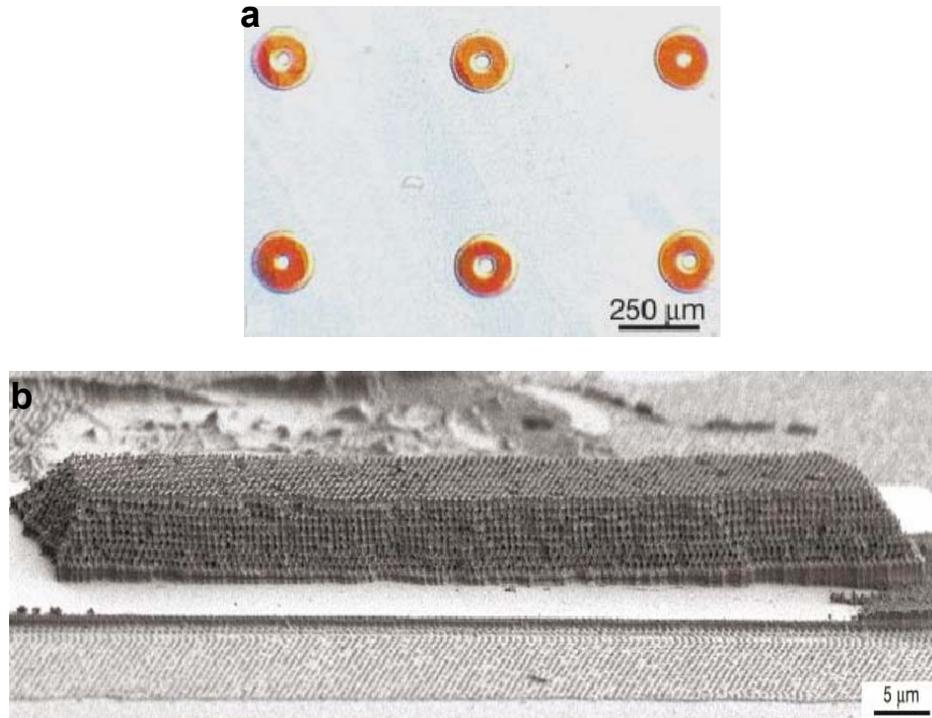


**Figure 3-11.** (a) Optical and (b) SEM cross-section images of patterned silicon photonic crystals by photolithography and RIE. Rings in (a) are 3-layer-thick photonic crystals, and their red color arises from the crystal diffraction.

## 3.6    Patterning Inverted Opals

Planar inverted opals can be patterned by conventional photolithography and RIE. The patterning of PBCs allows the integration of photonic devices and microelectronic circuits on the same silicon substrate. Since the porous silicon of inverted opals is fragile, photolithography, especially in the step of mask contact for

exposure, may damage the photonic crystals. A new process step has been developed to avoid the crack and collapse of the photonic crystals. Instead of removing the silica template first soaking by BOE, we performed photolithography on the planar opals filled with silicon. Then, the sample with patterned photoresist was dipped into 10: 1 BOE. The etching solution flows through the top surface area which was not masked, and etches away the silica templates. Subsequent RIE removed the unmasked porous silicon, and the remaining photoresist was cleaned by solvent rinse and oxygen plasma. The silica in the remaining region was then removed with BOE. Using this approach, 3-D silicon photonic crystals were patterned, as shown in Fig. 3-11. The photograph of Fig. 3-11(a) shows an array of 100-μm-diameter 'rings' of photonic crystals that are three layers thick. The array covers a 1-mm-area of the wafer. Photonic crystals over 10-layer-thick were patterned into the mesa-shape in Fig. 3-11(b). The periodic arrangements of the air spheres and the silicon shells are clearly seen.


## 3.7    Summary


Photonic crystals made of periodic dielectric materials can exhibit a photonic bandgap at a specific wavelength. The fabrication complexity of 3-D PBCs by conventional microelectronic techniques was replaced by a cheaper and simpler self-assembly approach. The planar synthetic opals are spontaneously assembled on silicon wafers with a periodic *fcc* structure, but no photonic bandgap exists in them due to the low refractive index of silica ($n \sim 1.4$). Inverted opals created by filling silicon ($n \sim 3.45$) into opal interstitial space and then removing the silica opals do have a 3-D photonic bandgap. In this chapter, we have investigated the whole fabrication process, and focused on the silicon CVD growth to infiltrate opal templates.

Conventional PECVD *a*-Si deposition condition could not infiltrate the 3-D opals, because the *a*-Si deposition on the outmost opal obstructed deposition-gas transport into the inner most layers. Highly diluted $SiH_4$ (2% in $N_2$) and low deposition temperature 550 °C in LPCVD leads to a long mean free path of silicon diffusion and

lower deposition rate, which are key requirements to achieve the full infiltration of silicon into opal templates. A further anneal at 600 °C crystallized *a*-Si into poly-Si with smooth surface, unlike as-deposited poly-Si.

Planar inverted opals on Si wafer were then made by wet etching to remove the silica spheres. The optical spectra with the incident normal to [111] and [100] *fcc* directions exhibit near-unity reflectance at the wavelength of ~ 1.3 μm, confirming that 3-D silicon PBCs have been achieved for the first time. Photolithography and RIE were successfully used to pattern inverted opals. This provides a path to the integration of photonic devices and microelectronic circuits on the same silicon wafer.

# References

[1] E. Yablonovitch, "Inhibited spontaneous emission in solid-state physics and electronics", *Phys. Rev. Lett.*, **58:** 2059-2062 (1987).

[2] S. John, "Strong localization of photons in certain disordered dielectric superlattices", *Phys. Rev. Lett.*, **58**: 2486-2489 (1987).

[3] J. D. Joannopoulos, R. D. Meade, and J. N. Winn, "Photonic crystals: molding the flow of light", Princeton University Press, Princeton, 1995.

[4] J. D. Joannopoulos, P. R. Villeneuve, and S. Fan, "Photonic crystals: putting a new twist on light", *Nature*, **386**: 143-149 (1997).

[5] S. Y. Lin, J. G. Fleming, D. L. Hetherington, B. K. Smith, R. Biswas, K. M. Ho, M. M. Sigalas, W. Zubrzycki, S. R. Kurtz and J. Bur, "A three-dimensional photonic crystal operating at infrared wavelengths", *Nature*, **394**: 251-253 (1998).

[6] S. Noda, K. Tomoda, N. Yamamoto, and A. Chutinan, "Full three-dimensional photonic bandgap crystals at near-infrared wavelengths", *Science*, **289**: 604-606 (2000).

[7] Y. A. Vlasov et al, "Manifestation of intrinsic defects in optical properties of self-organized opal photonic crystals", *Phys. Rev. E*, **61**: 5784-5793 (2000).

[8] J. E. G. J. Wijnhoven, and W. L. Vos, "Preparation of photonic crystals made of air spheres in titania", *Science*, **281**: 802-804 (1998).

[9] A. Blanco, E. Chomski, S. Grabtchak, M. Ibisate, S. John, S. W. Leonard, C. Lopez, F. Meseguer, H. Miguez, J. P. Mondia, G. A. Ozin, O. Toader, and H. M. van Driel, "Large-scale synthesis of a silicon photonic crystal with a complete three-dimensional bandgap near 1.5micrometres", *Nature*, **405**: 437-440 (2000).

[10] K. Busch and S. John, "Photonic band gap formation in certain self-organizing systems", *Phys. Rev. E*, **58**: 3896-3908 (1998).

[11] John D. Joannopoulos, "Self-assembly lights up", *Nature*, **414**: 257-258 (2001).

[12] Z.-Y. Li, and Z.-Q. Zhang, "Fragility of photonic band gaps in inverse-opal photonic crystals", *Phys. Rev. B*, **62**: 1516-1519 (2000).

[13] P. Jiang, J. F. Bertone, K. S. Hwang and V. L. Colvin, "Single-crystal colloidal multilayers of controlled thickness", *Chem. Mater.*, **11**: 2132-2140 (1999).

[14] D. J. Norris, Y. A. Vlasov, X.-Z. Bo, and J. C. Sturm, "Self-assembled photonic crystals and methods for manufacturing same", US patent: US22062782A1 (2002).

[15] E. D. Palik, "Handbook of Optical Constants of Solids", vols. I and II, Academic Press, Boston, 1991.

[16] K. Pangal, "Hydrogen-plasma-enhanced crystallization of hydrogenated amorphous silicon films: fundamental mechanisms and applications", Ph.D. thesis, Princeton University, Nov. 1999.

[17] C. M. Fortmann, E. L. Jaen, N. Hata, W. A. Anderson, A. H. Mahan, "Hot-wire deposition of photonic-grade amorphous silicon", *Thin Solid Films*, **395**: 142-146 (2001).

[18] C. D. Dushkin, G. S. Lazarov, S. N. Kotsev, H. Yoshimura, and K. Nagayama, "Effect of growth conditions on the structure of two-dimensional latex crystals: experiment", *Colloid. Polym. Sci.*, **277**: 914-930 (1999).

[19] Y. A. Vlasov, X.-Z. Bo, J. C. Sturm, D. J. Norris, "On chip assembly of silicon photonic bandgap crystals", *Nature*, **414**: 289-293 (2001).

[20] Y. A. Vlasov, M. Deutch and D. J. Norris, "Single domain spectroscopy of self-assembled photonic crystals", *Appl. Phys. Lett.*, **76**: 1627-1629 (2000).

[21] P. M. Bell, J. B. Pendry, L. Martin-Moreno, and A. J. Ward, "A program for calculating photonic band structures and transmission coefficients of complex structures", *Comput. Phys. Commun.*, **85**: 306-322 (1995).

# Chapter 4

REVIEW OF AFM NANOLITHOGRAPHY

## 4.1    History and Development

The invention of scanning tunneling microscopy (STM) [1] and atomic force microscopy (AFM) [2] in the 1980's opened a new page of surface science, enabling people to image surfaces at a nanometer scale.  STM works by scanning an atomically sharp metal tip over a surface.  When the tip is brought very close to the surface and an electrical voltage is applied to the tip or sample, electron tunneling between the tip and the sample occurs.  The detected tunneling current is related to the distance between the tip and the sample surface, which can be used with an electrical feedback loop to image the surface at an extremely small scale.  To overcome a basic drawback of STM ⎯⎯ that it can only image conducting or semiconducting surfaces ⎯⎯ AFM was developed. Instead of detecting tunneling current, AFM "feels" the van der Waals force between the tip and the sample to image any type of surface, including polymers, ceramics, composites, glass, and biological samples.

With the advantage of high lateral (~ 1Å) and vertical (~ 0.1Å) resolutions, scanning probe microscopy (SPM) has begun to be used in nanopatterning semiconductor surfaces, a process which is called SPM nanolithography.  The first experiments on surface modification were performed in the 1990's by Dagata *et al.* [3,4], using STM with the technique of local anodic oxidation (LAO) on a silicon surface in air.  The minimum width of oxidation features was ~ 45 nm with an oxidation height of ~ 2 nm.  This technique can be used for writing very fine oxide patterns on both

metallic and semiconductor surfaces, and thus has attracted the interest of semiconductor device developers as well as the rest of the scientific community. AFM nanolithography promises to become a useful addition to the well-established methods of electron-beam lithography. It is slower than e-beam lithography, but has the advantage of avoiding radiation damage.

This chapter will review AFM nanolithography on semiconductor and metal surfaces, including AFM LAO mechanisms, the effects of writing parameters on AFM LAO, and typical examples of nano-electronic devices patterned by AFM nanolithography. AFM nanolithography on soft materials by nano-scratching and local-electron exposure is systematically discussed in Ref. [5].

*AFM Nanolithography on Semiconductor Surfaces*
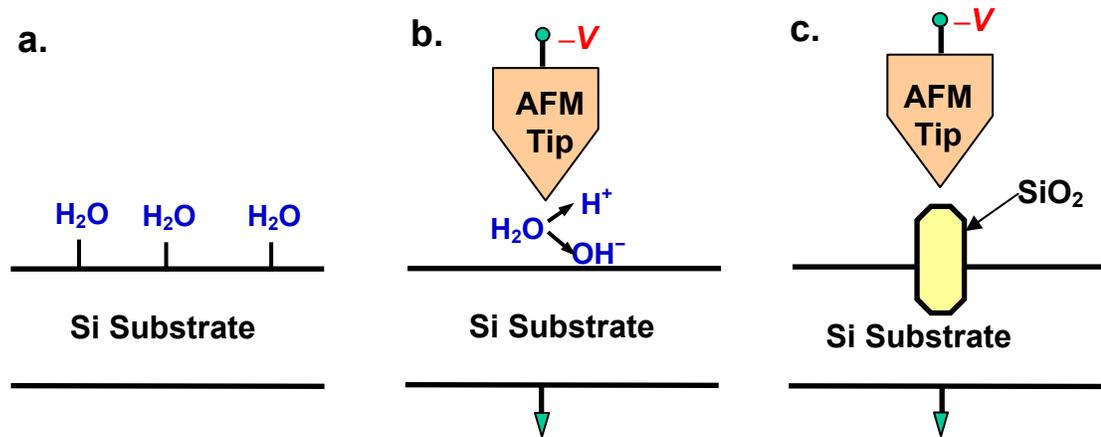


**Figure 4-1.** Process of AFM local oxidation: (a) water vapor adsorbed on silicon surface; (b) water dissociated into $H^+$ and $OH^-$ ions by electrical field between AFM tip and Si substrate; and (c) formation of $SiO_2$ by the reaction $OH^-$ with Si.

The phenomenon of SPM anodic nano-oxidation has proven to be of electrochemical nature [6]. The simplified mechanism is as follows (Fig. 4-1). A thin water film adsorbed on the sample surface under a controlled ambient humidity serves

as an electrolyte between a sample (anode) and the tip (cathode). The negatively biased tip imposes an external electric field which dissociates water molecules into an oxidizing species, presumably OH$^-$. The field further enhances vertical drift of these species away from the tip towards the surface where they react with underlying atoms to form a localized oxide beneath the tip. The field strength decays across the growing oxide film and the oxide growth process self terminates at/below the critical electric field, which is on the order of $10^7$ V/cm.

During STM nanolithography, bias voltages applied to the tip or sample are needed both for LAO processes and subsequent image scanning, whereas AFM surface imaging does not require bias voltages. Snow *et al*. [7] supposed that using AFM with a conductive tip offers an advantage over STM in that the exposure and imaging mechanism are decoupled. This guarantees independent writing and subsequent imaging of written patterns without risk of additional electrical exposure. A side-gate transistor was fabricated on an SOI substrate by AFM LAO with a minimum feature size of 10-20 nm, and showed that gate voltage could modulate source-drain current [8].

Avouris *et al*. [9] investigated the effects of ambient relative humidity (RH) on the AFM LAO of silicon within the range of 10-95%, and found the aspect ratio of the writing patterns were dramatically affected by RH. The adsorbed water layer not only supplies the oxidizing species, but its finite conductance also leads to a defocusing of the electric field, which degrades the lateral resolution of the process. The highest aspect ratio structures formed at about 14% RH.

Fontaine *et al*. [10] wrote a series of lines on the silicon surface by AFM LAO under different bias voltages on the AFM tip. They found that AFM LAO is strongly dependent on the tip voltage. The LAO cannot occur until the tip bias voltage is greater than a threshold value. The height of oxidation lines is approximately linearly proportional to the tip voltages.

Using AFM LAO of *a*-Si as an etching mask, a MOSFET gate was defined with length ~ 0.1 µm by RIE [11]. The hydrophilicity of the silicon surface was controlled by submersion in various chemical solutions, which is another way to control water layer parameters besides ambient humidity [12]. The average height (width) of LAO feature

increased from 1.9 nm (330 nm) to 4.8 nm (550nm). Si/SiGe heterostructures with thickness ~ 10 nm were nanopatterned by AFM nanolithography and selective wet etching [13], the details of which will be discussed later.

AFM LAO on GaAs can reach an oxidation height of 10−15 nm, greater than on silicon. Held *et al*. [14] demonstrated that the LAO of a GaAs surface could deplete a two-dimensional electron gas (2DEG) ~ 35nm underneath the surface in the modulation doped GaAs/AlGaAs heterojunctions, forming a potential barrier with high-resistivity. The delta-doping which supplied the carriers of a 2DEG was partially oxidized. Antidots and quantum point contacts as in-plane gate transistors have been fabricated and their performance at liquid nitrogen temperatures was discussed. The high specularity of electron scattering at the depletion boundaries was confirmed in Ref. [15]. AFM nanolithography provides smaller lateral depletion lengths (less than 20 nm) compared to those for electron-beam lithography (~ 100 nm). Thus the steep potential walls of defined patterns give strong lateral quantum confinement, and result in a high sub-band energy splitting spacing [16,17].

*AFM Nanolithography on Metals*

SPM-based nanolithography has also been successfully applied to metal surfaces, such as Ti [18,19,20], Cr [21,22], Al [23,24], and Au [25,26]. Sugimura *et al*. [18] first applied STM to anodically oxidize a Ti surface, achieving ~ 30 nm spatial resolution. STM LAO was also used to pattern Cr surfaces with 25-nm resolution [21]. Others have used AFM nanolithography to locally oxidize metals due to the advantage of AFM over STM in nanolithography, which was mentioned above.

Snow *et al*. [19,23] made nanowires on Ti and atomic point contacts on Al films by AFM LAO patterning. The width of the wire was controlled by real-time measurement of device resistance as a feedback to the bias voltage on the AFM tip during fabrication. Structures with critical dimensions of less than 10 nm were fabricated. A quantized decrease in conductance of Al nanowires during the final stages of anodic oxidation in discrete steps of $\sim 2e^2/h$ was observed.

A single-electron transistor (SET) was fabricated on a Ti thin film by STM LAO [20].  Two titanium oxidation lines with widths of 15-25 nm served as potential barriers to separate a quantum dot from source and drain.  A Coulomb staircase of source/drain current *vs.* source/drain voltage was observed at room temperature.

Boisen *et al*. [24] used aluminum and aluminum oxide written by AFM nanolithography as masks for the reactive ion etching (RIE) for the fabrication of suspended submicron silicon and silicon oxide structures. Aluminum is a commonly used metal in complementary metal-oxide-semiconductor (CMOS) electronics fabrication.  Hence, this patterning technique is CMOS compatible, making it possible in principle to fabricate advanced nano-mechanical structures with integrated microelectronics.

Schmidt *et al*. [27] investigated current-induced local oxidation (CILO), another route for oxidizing thin metal Ti and Nb films with nanometer-scale resolution.  High in-plane current densities were applied to a narrow metal strip on order of 100 nm in width, which was surrounded by oxide regions previously fabricated by means of the "usual" AFM nano-oxidation.  This resulted in the formation of an insulating oxide barrier.  Towards the end of the barrier formation, only atomic-scale channels in Nb remain unoxidized.  A reduction in conductance in steps of $2e^2/h$ with the oxidation was observed.

These results on metal and semiconductor surfaces show that AFM nanolithography by local oxidation is a viable tool for patterning experimental device structures.

*Development of AFM Nanolithography*

There are several critical issues which need to be addressed for AFM nanolithography to progress from a tool for research to a tool for commercial applications.

First, the wear of an SPM tip during the nanolithography process is one of them. The AFM tips for nanolithography are typically made of doped silicon.  They are damaged by the writing process.  Dai *et al*. [28] believe the remedy is to use carbon

nanotube probes.  Reliable ~ 10-nm-wide oxidation lines with high uniformity over large area were achieved without noticeable wear.  They claimed that nanotube tips are impervious to high compressive and lateral forces and breakdown at high electric field. A high writing speed of 0.5 mm/s was also achieved using nanotube tips.

Another obstacle to commercialization of AFM nanolithography is its slow rate of writing.  Snow and Campbell [29] declared successful experiments on AFM oxidation of metal silicide processes with a minimum exposure time of ~ 300 ns for a 30 nm size pixel which corresponds to a maximum write speed of ~ 10 cm/s.  To increase the writing speed of AFM, multi-probe AFM with parallel operation at high-speed has been developed [30,31].  An array of 50 probes with 200-μm-pitch was designed to be controlled by a personal computer (PC).  Automatic parallel imaging was demonstrated by using four cantilevers within the array of 50 cantilevers.  Later, they successfully used two AFM probes to simultaneously pattern polymer resist by *in-situ* varying the bias voltage on each tip to ensure that a constant current was emitted.  The writing speed reached ~ 1 mm/s.

Advances in AFM nano-oxidation allowed for the demonstration of an extra dense data storage media having capacity of 1.6 Tera-bit per square inch [32].  Using a single-walled carbon nanotube with 2-5nm diameter, 8-nm-bits on 20-nm-pitch were written on a flat titanium surface at a rate of 5 kbit/s.  Areas up to 16 $\mu m^2$ can be written several times by a single nanotube tip without degradation of resolution or uniformity. While there are a number of technical issues that still need to be addressed, this work shows the promise and necessities of commercial development for AFM nanolithography.

## 4.2    Instrumentation Issues

The operation of AFM nanolithography is different from that of AFM imaging. During AFM imaging, the movement of the AFM tip covers the entire surface within the region of interest by a means of a raster scan.   In contrast, during AFM

nanolithography, the tip scans only in the specific area for local oxidation with the applied bias voltage on at the same time. Therefore, AFM nanolithography relies on the fact that state-of-the-art AFM equipment allows for direct scripting of the pattern and the tip is to follow the surface in a very accurate manner.

Since the wear of an AFM tip in tapping-mode is less than in contact-mode, AFM operates in tapping-mode during our AFM LAO experiments. Tapping-mode AFM operates by scanning a tip attached to the end of an oscillating cantilever across the sample surface. The cantilever is oscillated at or near its resonance frequency with an amplitude ranging typically from 20 nm to 100 nm. The tip lightly "taps" on the sample surface during scanning, contacting the surface at the bottom of its swing. A laser beam (Fig. 4-2 [33]) shines on the tip cantilever, and is reflected into a split photodiode detector. The tip movement in the z-direction is monitored by the root-mean-square (RMS) of the oscillation signal acquired by the photo-detector. A feedback loop maintains the oscillation amplitude at a constant "setpoint" during AFM scanning. The vertical position of the scanner at each (x,y) data point is thus stored by computer to form the topographic image of the sample surface.
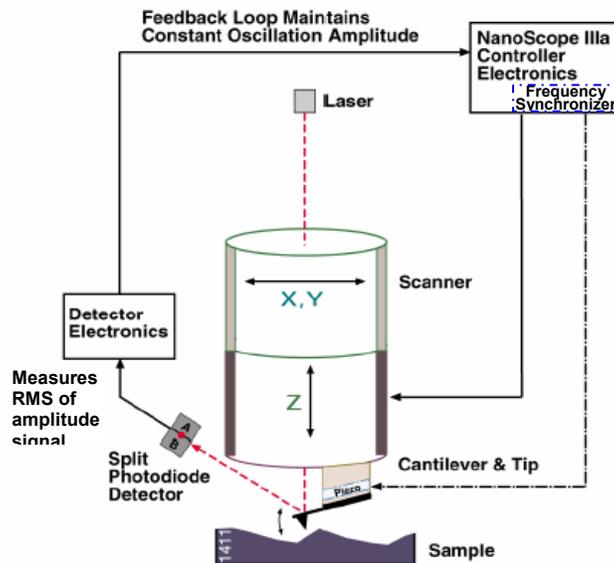


**Figure 4-2.** Schematic diagram of tapping-mode AFM of Digital Instruments [33].

To achieve AFM nanolithography, three functionalities are added to the above:
(1) a script program which manipulates AFM tip movement, (2) a DC bias-voltage
applied to AFM tip to promote LAO, (3) a humidity-controlled environment which
supplies water-vapor as the electrolyte for anodic oxidation.
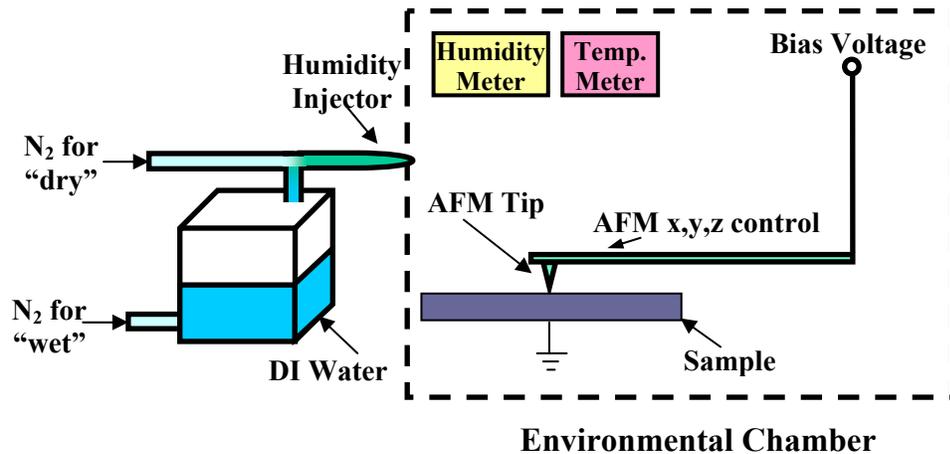


**Figure 4-3.**  AFM set-up for local anodic oxidation.

The NanoMan system from Digital Instrument (in Fig. 4-4) provides software to
directly control the AFM probe to draw dots, lines and polygons.  The interface allows
the user to control writing parameters needed for nanolithography and naomanipulation,
including probe velocity, vertical (Z) position, amplitude setpoint, applied voltage, and
pulse strength and duration.  To write complex patterns with accurately defined in-plane
coordinates, we used script language to write a recipe.  One example is listed in
Appendix B.

The bias voltage applied on AFM tips is supplied by an AFM electronic
controller with a range of $-10V$ to $+10V$.  Higher bias voltage on tip can be obtained
with a voltage amplifier in order to enhance the AFM local oxidation.  As shown in Fig.

4-3, the humidity of the homemade environmental chamber is controlled by a homemade water-bubbler.  Nitrogen is injected into water reservoir, and blows out water vapor.  Another nitrogen injection for "dry" is mixed with the water vapor to provide a controlled-humidity atmosphere.  The flow rates of the two nitrogen injections are controlled individually by adjustable flow meters.  The humidity and temperature around the sample surface are monitored by humidity and temperature sensors.  Figure 4-4 is a picture of the AFM instrument setup.  During AFM operation, the dome is closed in order to reduce mechanical noise and maintain the desired humidity level.
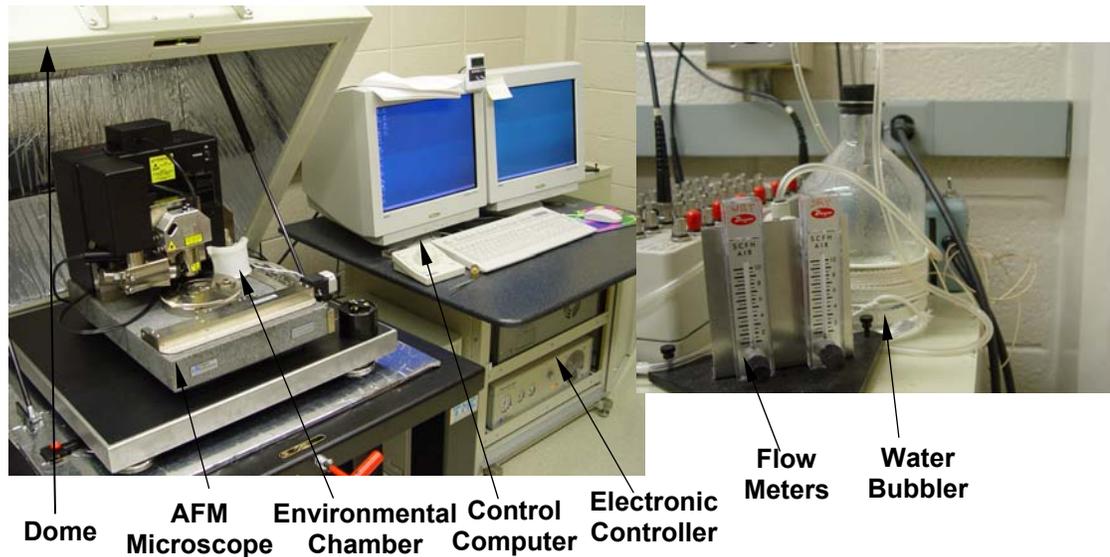


**Figure 4-4.**  Photo picture of NanoMan system and water bubbler.

## 4.3    AFM Nanolithography Examples

AFM local oxidation has been successfully performed using our equipment. Figure 4-5 shows the results of AFM local oxidation on silicon surfaces with bias

**a.**



**b.**
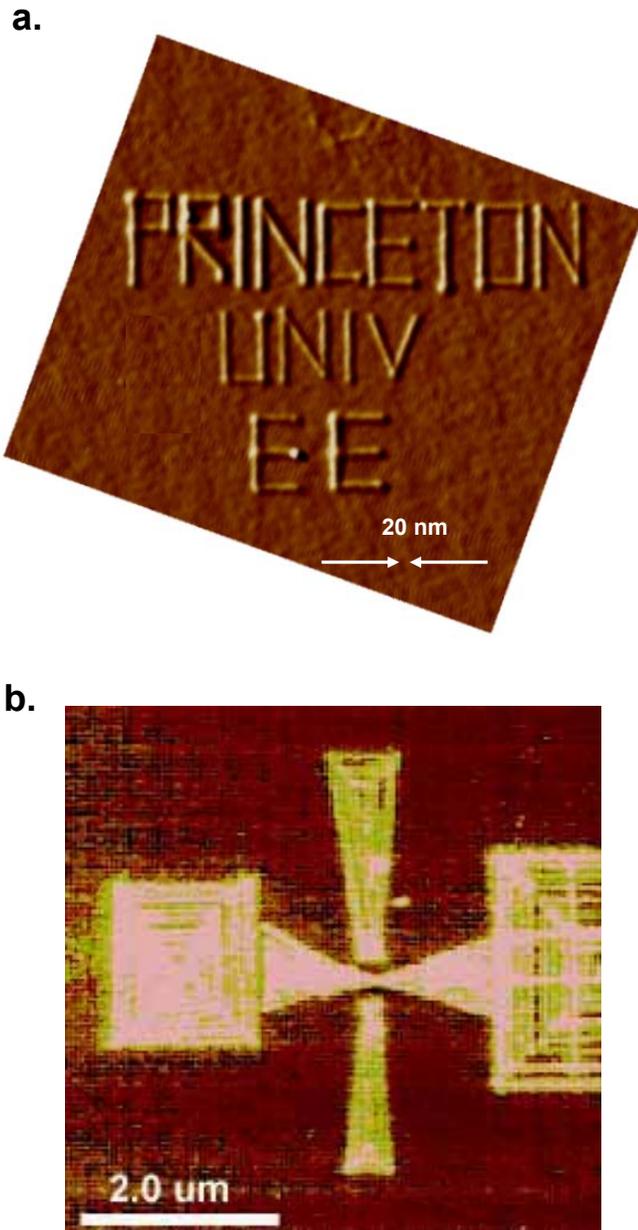


**Figure 4-5.** AFM local oxidation on Si surface.
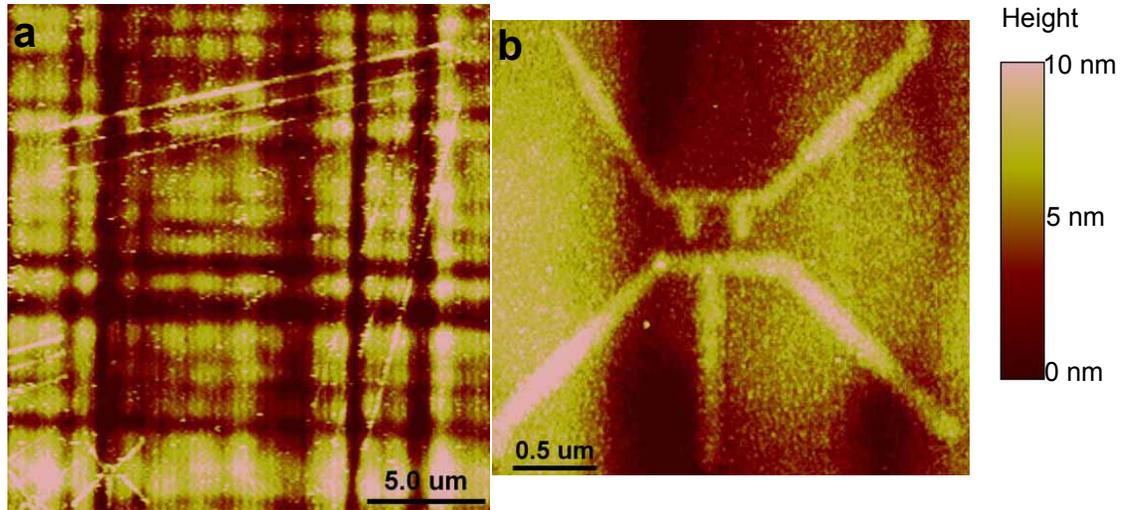
**Figure 4-6.** AFM LAO on a Si grown on a relaxed SiGe buffer with RMS roughness ~ 3.0 nm in (a) of 20×20 μm$^2$ area.  (b) A high resolution image of the bottom-left corner of (a).
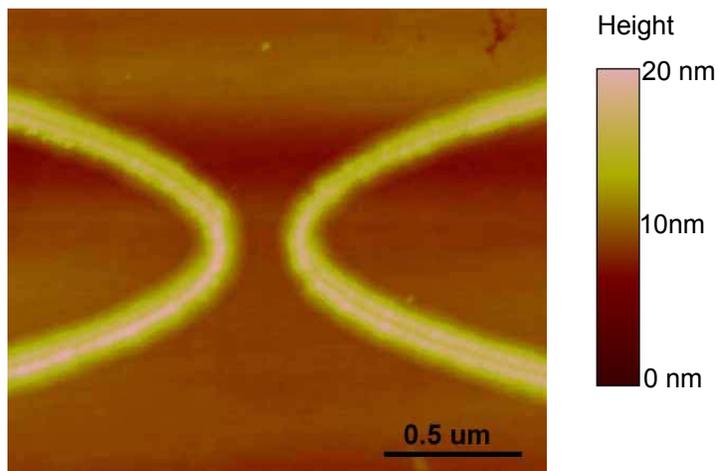


**Figure 4-7.** AFM LAO on GaAs with oxidation height ~ 10 nm.

voltages of (a) −8V and (b) −12V applied to the tip with the respect to the substrate.  In Fig. 4-5 (a), the oxidation line width is ~ 20 nm, and oxidation height is ~ 0.75 nm.  The oxidation pads in Fig. 4-5(b) are written line-by-line with AFM LAO.  They can be used as etching-mask to fabricate nanometer-scale electronic devices.  All these results indicate that the AFM tip can be well manipulated in our experiment set-up to write any kind of patterns.

AFM local oxidation on a rough surface was also performed using our AFM set-up (Fig. 4-6).  A 8-nm-thick Si layer was epitaxially grown on a thick relaxed SiGe buffer.  This tensile-strained Si layer has enhanced electron mobility, therefore such layers have recently attracted much interest.  During growth, the compressive strain in the SiGe layer due to the lattice mismatch with the Si substrate will relax when SiGe layer thickness is greater than the critical thickness, at which point the dislocation energy becomes lower than the strain energy.  The relaxation of the SiGe layer leads to a rough surface.  The RMS roughness in a $20 \times 20$ μm$^2$ area is ~3.0 nm with peak-to-valley roughness of ~ 20 nm.  During AFM nanolithography, a feedback loop was kept on to ensure a constant oscillation amplitude (~0.06 V signal from photodetector).  The AFM wring speed was reduced to 0.5 μm/s.  We can clearly see in Fig. 4-6(a) that the oxidation lines (~ 20-μm in length) cross the peaks and valleys of the rough surface with good unifomity.  An enlarged AFM image in Fig. 4-6(b) shows that approximately 150-nm-wide oxidation lines were formed in the pattern of a quantum dot device.

AFM LAO on a GaAs surface is shown in Figure 4-7.  The oxidation lines with a height of ~ 10 nm deplete the two-dimensional hole gas (2DHG) about 35 nm under the surface, and form potential barrier in it [34].  Two parabolic lines define a quantum point contact.  Electrical measurement shows the conductance of the point contact decreases in steps of ~ $2e^2/h$ as the two palnar gate voltages increase.

We gratefully acknowledge the work of Dr. Leonid Rokhinson, who initially developed the AFM oxidation process for nanopatterning at Princeton.

## 4.4    Summary

The history and development of AFM LAO on semiconductor and metal surfaces have been reviewed.  Using our AFM instrument set-up with a controlled-humidity environment, we have successfully created patterns on a flat Si surface, the rough surface of Si on relaxed SiGe buffer, and GaAs surfaces.  Specific results of linewidth vs. voltage, writing speeds, Si vs. SiGe surface, and transfer of the oxidation patterns to other layers will be discussed in the next chapter.

# References

[1] G. Binnig, H. Rohrer, Ch. Gerber, and E. Weibel, "Surface studies by scanning tunneling microscopy", *Phy. Rev. Lett.*, **49**: 57-61 (1982).

[2] G. Binnig, C.F. Quate, and Ch. Geber, "Atomic force microscope", *Phys. Rev. Lett.*, **56**: 930-933 (1986).

[3] J. A. Dagata, J. Schneir, H. H. Harary, C. J. Evans, M. T. Postek, and J. Bennertt, "Modification of hydrogen-passivated silicon by a scanning tunneling microscope operating in air", *Appl. Phys. Lett.,* **56**: 2001 (1990).

[4] J. A. Dagata, J. Schneir, H. H. Harary, J. Bennett, and W. Tseng, "Pattern generation on semiconductor surfaces by a scanning tunneling microscope operating in air", *J. Vac. Sci. Technol. B,* **9**: 1384-1388 (1991).

[5] J. P. Pickering and G. J. Vancso, "On the formation of oriented nanometer scale patterns on amorphous polymer surfaces studied by atomic force microscopy", *Appl. Surf. Sci.*, **148**: 147-154 (1999).

[6] A. E. Gordon, R. T. Fayfield, D. D. Litfin, and T. K. Higman, "Mechanisms of surface anodization produced by scanning probe microscopes", *J. Vac. Sci. Tech. B*, **13**: 2805-2808 (1995).

[7] E. S. Snow, and P. M. Campbell, "Fabrication of Si nanostructures with an atomic force microscope", *Appl. Phys. Lett.*, 64: 1932-1934 (1994).

[8] P. M. Campbell, E. S. Snow, and P. J. McMarr, "Fabrication of nanometer-scale side-gated silicon field effect transistors with an atomic force microscope", *Appl. Phys. Lett.*, **66**: 1388-1390 (1995).

[9] Ph. Avouris, R. Martel, T. Hertel, and R.L. Sandström, "AFM tip induced and current induced local oxidation of silicon and metals", *Appl. Phys. A*, **66** (suppl. 1): S659-667 (1998).

[10] P.A. Fonaine, E. Dubois, and D. Stiévenard, "Characterization of scanning tunneling microscopy and atomic force microscopy-based techniques for nanolithography on hydrogen-passivated silicon", *J. Appl. Phys.*, **84**: 1776-1781 (1998).

[11] C. Minne, H. T. Soh, P. Flueckiger, C. F. Quate, "Fabrication of 0.1 $\mu$m metal oxide semiconductor field-effect transistors with the atomic force microscope", *Appl. Phys. Lett.*, **66**: 703-705 (1995).

[12] W. C. Moon, T. Yoshinobu and H. Iwasaki, "Enhanced nano-oxidation on a SC1-treated Si surface using atomic force microscopy", *Jpn. J. Appl. Phys.*, **41**:4754-4757 (2002).

[13] X.-Z. Bo, L. P. Rokhinson, H. Yin, D. C. Tsui, and J. C. Sturm, "Nanopatterning of Si/SiGe electrical devices by atomic force microscopy oxidation", *Appl. Phys. Lett.*, **81**: 3263-3265 (2002).

[14] R. Held, T. Vancura, T. Heinzel, K. Ensslin, M. Holland, and W. Wegscheider, "In-plane gates and nanostructures fabricated by direct oxidation of semiconductor heterostructures with an atomic force microscope", *Appl. Phys. Lett.*, **73**: 262-264 (1998).

[15] R. Held, S. Lüscher, T. Heinzel, K. Ensslin, and W. Wegscheider, "Fabricating tunable semiconductor devices with an atomic force microscope", *Appl. Phys. Lett.*, **75**: 1134-1136 (1999).

[16] A. Fuhrer, S. Lüscher, T. Heinzel, K. Ensslin, W. Wegscheider, and M. Bichler, "Transport properties of quantum dots with steep walls", *Phys. Rev. B,* **63**: 125309 (2001).

[17] A. Fuhrer, S. Lüscher, T. Ihn, T. Heinzel, K. Ensslin, W. Wegscheider, and M. Bichler, "Energy spectra in quantum rings", *Nature*, **413**: 822-825 (2001).

[18] H. Sugimura, T. Uchida, N. Kitamura, H. Masuhara, "Tip-induced anodization of titanium surfaces by scanning tunneling microscopy: A humidity effect on nanolithography", *Appl. Phys. Lett.*, **63**: 1288-1290 (1993).

[19] E. S. Snow, P. M. Campbell, "AFM Fabrication of Sub-10-Nanometer Metal-Oxide Devices with in Situ Control of Electrical Properties", *Science* **270**: 1639 (1995).

[20] K. Matsumoto, M. Ishii, K. Segawa, and Y. Oka, "Room temperature operation of a single electron transistor made by the scanning tunneling microscope nanooxidation process for the $TiO_x$/Ti system", *Appl. Phys. Lett.,* **68**: 34-36 (1996).

[21] H. J. Song, M. J. Rack, K. Abugharbieh, S. Y. Lee, V. Khan, D. K. Ferry, D. R. Allee, "25 nm chromium oxide lines by scanning tunneling lithography in air", *J. Vac. Sci. Technol. B*, **12**: 3720-3724 (1994).

[22] W. Wang, T. Tsau, K. L. Wang, and P. Chow, "Nanofabrication of thin chromium film deposited on Si(100) surfaces by tip induced anodization in atomic force microscopy", *Appl. Phys. Lett.*, **67**: 1295-1297 (1995).

[23] E. S. Snow, D. Park, and P. M. Campbell, "Single-atom point contact devices fabricated with an atomic force microscope", *Appl. Phys. Lett.*, **69**: 269-271 (1996).

[24] A. Boisen, K. Birkelund, O. Hansen, and F. Grey, "Fabrication of submicron suspended structures by laser and atomic force microscopy lithography on aluminum combined with reactive ion etching", *J. Vac. Sci. Technol. B*, **16**: 2977-2981 (1998).

[25] H. W. Schumacher, B. Kracke, and B. Damaschke, "Modification of thin gold films with a scanning force microscope", *Thin Solid Films,* **264**: 268-272 (1995).

[26] W. C. Moon, T. Yoshinobu and H. Iwasaki, "Nanoscale patterning of Au films on Si surfaces by atomic force microscopy", *Jpn. J. Appl. Phys.*, **38**: 6952-6954 (1999).

[27] T. Schmidt, R. Martel, R. L. Sandstrom, and Ph. Avouris, "Current-induced local oxidation of metal films: Mechanism and quantum-size effects", *Appl. Phys. Lett.,* **73**: 2173-2175 (1998).

[28] H. Dai, N. Franklin, and J. Han, "Exploiting the properties of carbon nanotubes for nanolithography", *Appl. Phys. Lett.*, **73**: 1508-1510 (1998).

[29] E. S. Snow, P. M. Campbell, and F. K. Perkins, "High speed patterning of a metal silicide using scanned probe lithography", *Appl. Phys. Lett.*, **75**: 1476-1478 (1999).

[30] C. Minne, G. Yaralioglu, S. R. Manalis, J. D. Adams, J. Zesch, and A. Atalar, "Automated parallel high-speed atomic force microscopy", *Appl. Phys. Lett.*, **72**: 2340-2342 (1998).

[31] K. Wilder, H. T. Soh, A. Atalar, and C. F. Quate, "Nanometer-scale patterning and individual current-controlled lithography using multiple scanning probes", *Rev. Sci. Instru.*, **70**: 2822-2827 (1999).

[32] E. B. Cooper, S. R. Manalis, H. Fang, H. Dai, K. Matsumoto, S. C. Minne, T. Hunt, and C. F. Quate, "Terabit-per-square-inch data storage with the atomic force microscope", *Appl. Phys. Lett.*, **75**: 3566-3568 (1999).

[33] "Scanning probe microscopy training notebook", Veeco Metrology Group, Digital Instruments (2000).

[34] L. P. Rokhinson, D. C. Tsui, L. N. Pfeiffer, and K.W.West, "AFM local oxidation nanopatterning of a high mobility shallow 2D hole gas", *Superlattice and Microstructures*, **32**: 99-102 (2002).

# Chapter 5

---

# AFM LITHOGRAPHY
# NANOPATTERNING OF Si/SiGe
# HETEROSTRUCTURES AND EPITAXIAL
# SILICON REGROWTH

## 5.1    Introduction

Bandgap engineering and the ability to control strain in Si/SiGe heterostructures give rise to possibilities for devices with enhanced performance over those in bulk silicon [1,2]. Tensile strain in Si, introduced by growing a Si film on a relaxed SiGe buffer, enhances the electron mobility in Si MOSFETs up to 80% [3]. The current record value of electron mobility in a strained Si 2DEG (in a Si/SiGe modulation doped heterostructures) is $\sim$ 500,000 cm$^2$/Vs at 0.4 K [4]. Si/SiGe nanodevices, such as quantum dots, may offer new device functionality. Therefore, the nanopatterning of Si/SiGe heterostructures has been of great interest. The conventional nano-fabrication approach is electron-beam lithography and reactive-ion etching (RIE). These are high-energy processes which can cause radiation and etching damage, leading to the possibility of interface states or deep levels in quantum devices. Therefore, finding a low-energy patterning process is an important technological challenge for the fabrication of nanostructure devices.

As we mentioned in chapter 4, atomic force microscopy (AFM) with low tip
voltages (~10 V) under a controlled humidity environment can locally oxidize silicon.
The oxide feature size is on a scale of tens of nanometers [5].  Nanoelectronic devices
using AFM local oxidation have been fabricated on silicon [6], metal [7] and gallium
arsenide [8].   However, the patterning of Si/SiGe heterostructures using AFM local
anodic oxidation (LAO) has not previously been demonstrated to the best of our
knowledge.

In this chapter, AFM methods of nanopatterning Si/SiGe heterostructures are
demonstrated [9].  AFM local oxidation has been performed on bulk Si and strained
SiGe.  Two different pattern transfer methods are shown.  A SiGe single-hole transistor,
composed of a quantum dot, was fabricated by AFM local oxidation.  The device
exhibits Coulomb blockade oscillations.  The device characteristics were adversely
affected by the bare dot surface.  Therefore, the epitaxial regrowth of silicon on
nanopatterned SiGe was investigated.

## 5.2     Experimental Details of AFM Local Oxidation

AFM local oxidation was performed at room temperature in tapping mode on a
Dimension 3000 from Digital Instruments.  A heavily-doped silicon tip with nominal
curvature radius smaller than 10 nm was used (MikroMasch Inc.).  In tapping mode, the
AFM cantilever is driven by a piezoelectrode to oscillate at or near the resonant
frequency (~ 350 kHz) of the tip cantilever.  Three kinds of samples were used in our
experiment: a boron-doped p-type silicon wafer with resistivity of 10 $\Omega$·cm,
pseudomorphically compressive-strained $Si_{0.8}Ge_{0.2}$ layer with a thickness of ~ 10 nm
deposited on a silicon (100) substrate by rapid thermal chemical vapor deposition
(RTCVD), and finally a $p^+$-doped $Si_{0.7}Ge_{0.3}$ layer on Si with a thin (~ 2 nm) Si cap
layer.  Before AFM local oxidation, the sample was first submerged in acetone and
isopropanol in an ultrasonic bath for 10 min each, and then dipped into a 10% diluted
aqueous HF solution for 1 min.  A subsequent deionized water rinse for 1 min led to the

Si or SiGe surface being passivated with hydrogen [10].  During AFM writing, a
feedback loop was enabled to keep the tapping amplitude (and thus the average distance
from sample surface to the tip) at the "set-point" of 0.04−0.1 V, which is much lower
than the value ~ 1.0 V for image scanning.  A smaller tapping amplitude leads to a high
electric field for AFM local oxidation.  The relative humidity was kept constant at ~
70% by bubbling nitrogen through water into an environmental chamber surrounding
the tip, as shown in Fig. 4-2.  The bias voltage on the tip with respect to the grounded
sample was varied from −10V to −38 V.  The tip movement was programmed by a
script language.

## 5.3    AFM Local Oxidation of SiGe Alloys
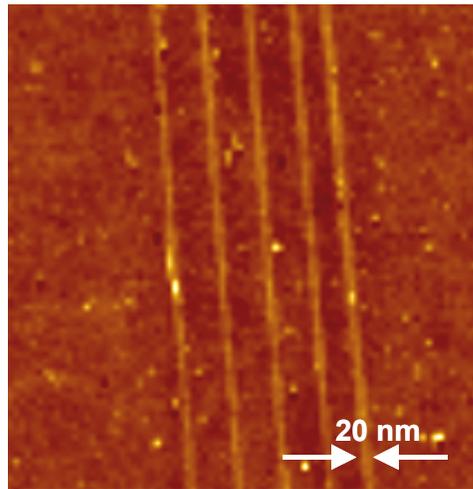


**Figure 5-1.**  Fine oxide lines on strained $Si_{0.8}Ge_{0.2}$ by AFM lithography at the bias
voltage −12V.

The first nanopatterning method used was the direct AFM LAO of the SiGe
layer.  Figure 5-1 shows a set of oxidation lines in strained $Si_{0.2}Ge_{0.8}$ fabricated by AFM
nanolithography created with a tip bias voltage of −12V and tip writing speed of 1.0
μm/s.  Because the oxide has about twice the volume of the silicon or silicon-

germanium consumed, the AFM local oxidation feature is higher than the rest of the
surface, and is readily identifiable in the subsequent regular AFM scans.  The full width
at half magnitude (FWHM) of the oxidized lines is smaller than 20 nm.  AFM LAO on
strained $Si_{0.2}Ge_{0.8}$ layer at different bias voltages before and after the removal of oxide
is shown in Fig. 5-2(a) and Fig. 5-2(b) respectively.  Each of the isolated oxidation lines
had a different bias voltage applied on the tip, ranging from –10 V to –32 V, as labeled
in Fig. 5-2(a).  During AFM LAO, the tip writing speed was ~ 1.6 µm/s.  Subsequent
HF selective wet etching to remove the oxide faithfully transferred the oxidation feature
into the SiGe layer (Fig. 5-2b).  Fig. 5-2(c) shows the topography profile along the
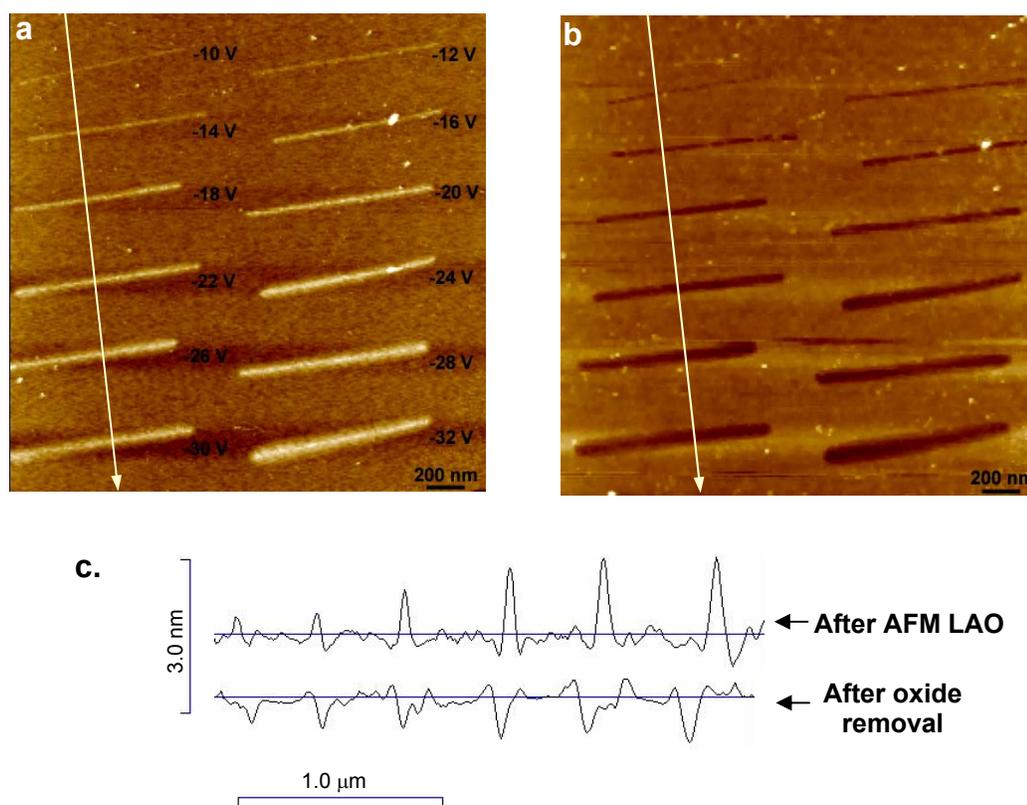


**Figure 5-2.**  AFM oxidation lines of $Si_{0.8}Ge_{0.2}$ with different bias voltages between
the tip and sample.  The scan speed was 1.6 µm/s, and the tapping amplitude setpoint
was 0.04 V. (a) after oxidation; (b) after removing the oxide by HF; (c) height profile
along arrow lines in (a) and (b).
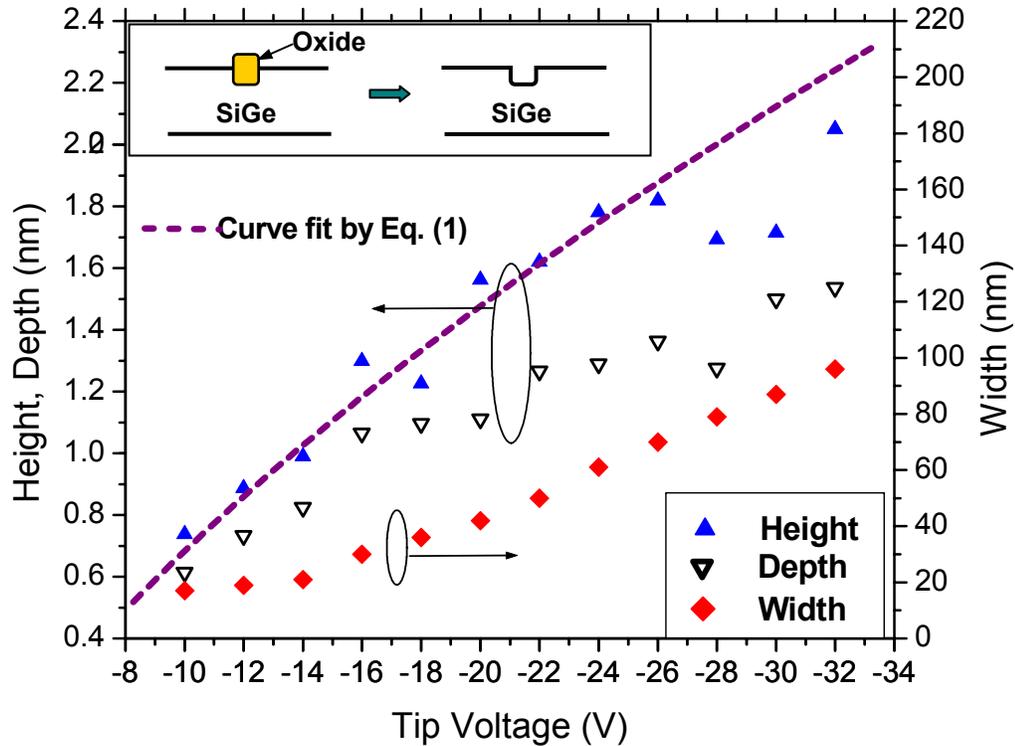
**Figure 5-3.**  Height, depth (after HF etching) and FWHM of AFM oxidation lines on strained $Si_{0.8}Ge_{0.2}$ alloys as a function of different bias voltages between the tip and sample. The writing speed was 2.0 μm/s and amplitude setpoint was 0.04 V. The dashed line is a fit of the height data using Eq. 1. The inset is a schematic of AFM oxidation and oxide removal.

arrow lines indicated in (a) and (b).  The oxide height, depth and width all increase with the bias voltage (Fig. 5-3).  The minimum linewidth (FWHM) of less than 20 nm occurs with a bias voltage −14 V, causing a feature ~ 1.0 nm above the surface after oxidation and a depression of ~ 0.8 nm after oxide removal.  The ratio of peak heights of the oxide lines after oxidation to the valley depths after oxide removal is about 3: 2.  This corresponds to a ratio of SiGe removed to the total oxide thickness of ~ 0.4, which is close to that observed in conventional silicon oxidation of ~ 0.44.  It should be noted that we do not know at present if the oxide that forms has the same ratio of Si to Ge as

in the substrate, or if the oxide is $SiO_2$ with Ge "snowplowing" ahead below the oxide. Both cases have been observed during thermal oxidation under different conditions [11], although the former case is preferred at low temperatures.

Snow and Campbell [5] have proposed field-assisted anodic oxidation as the mechanism of AFM oxidation of silicon, detailed in Sec. 4.1.  This involves three steps: (1) water vapor adsorbs on the silicon surface; (2) the electric field resulting from the voltage between the tip and the sample dissociates water into hydrogen ($H^+$) and hydroxyl ($OH^-$) ions; (3) $OH^-$ ions react with holes ($h^+$) from the Si surface to form silicon dioxide.  The chemical reaction is $Si + 4h^+ + 2H_2O \rightarrow SiO_2 + 4H^+$.  We assume a similar model to describe the oxidation of silicon-germanium.  That the oxidation rate depends on the tip voltage (and thus electric field) suggests that the rate is limited by the formation of $OH^-$.  The step height $h$ was fitted to the following model, which was used to describe the kinetics of AFM oxidation [12]:

$$h(t,V) = \frac{V}{E_0} \ln\left[ \frac{RE_0 t}{V} + 1 \right],$$ (5-1)

where $V$ is the tip bias voltage, $t$ is the exposure time to the electrical field, and $R$ and $E_0$ are constants, representing the maximum oxidation rate and Fowler-Nordheim tunneling parameter respectively.  Using equation $t = w/v$, we can convert the writing speed to the exposure time during AFM LAO, where $w$ is the oxide feature width.  In Fig. 5-3, the average linewidth is $\sim$ 60 nm, so we use exposure time $t = 30$ ms for curve fitting of Eq. 5-1.  The best fit for the experiment results in Fig. 5-3 was given by $E_0 = 45$ V/nm (same as for Si in Ref. 12) and $R = 1050$ nm/s.  The fast writing speed ($v = 2.0$ μm/s) and hydrophobic SiGe surface suggests the source of oxidation should be from water vapor instead of water liquid at a relative humidity $\sim$ 70%.  Note that here the $R$ is much less than that of AFM LAO on a hydrophilic silicon surface treated by chemical solution $\sim 10^7$ nm/s [12].  This further confirms it is the supply of $OH^-$ ions that dominates AFM LAO rate.
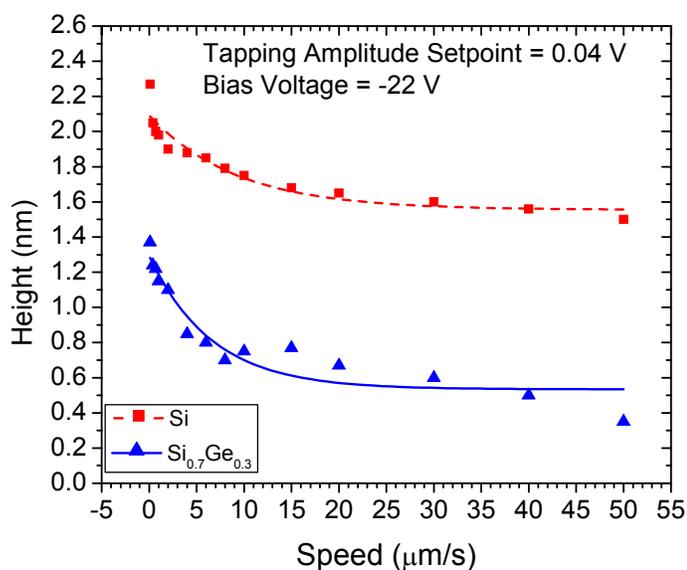
**Figure 5-4.** Feature height of AFM LAO on silicon and $Si_{0.7}Ge_{0.3}$ as a function of writing speed. The scattered marks are experimental data, and the dashed and solid lines are logarithmical fitting.
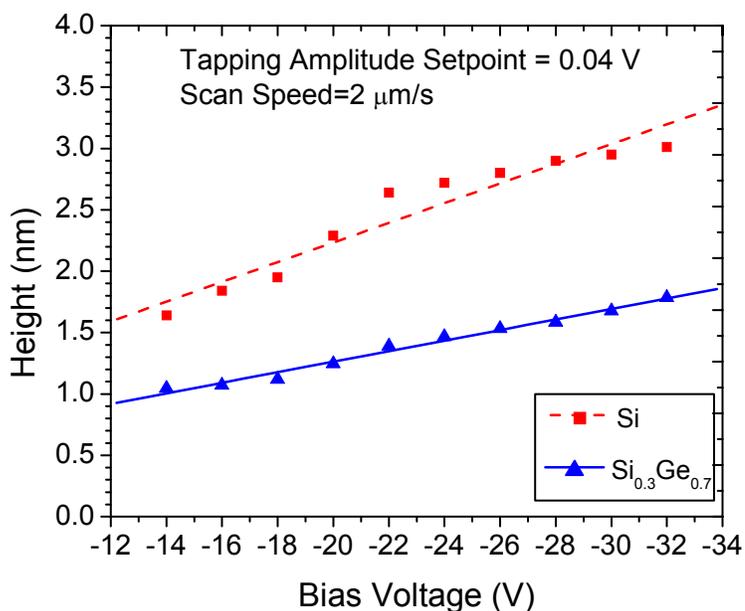


**Figure 5-5.** Comparison of feature heights of AFM oxidation on Si and $Si_{0.7}Ge_{0.3}$ as a function of the bias voltage.

AFM local oxidation is also dependent on the tip writing speed, as shown in Fig.
5-4.  Here, the tapping amplitude was set at 0.04V and bias voltage on AFM tip was
−22 V.  The oxidation rate is almost constant for writing speeds above 20 μm/s, and
increases markedly for slower speeds.  The solid line in Fig. 5-4 is the logarithmical fit
to the experimental data, which is agreeable to the kinetics of AFM LAO quantified in
Eq. (5-1).

In Fig. 5-4 and Fig. 5-5, the AFM local oxidation of $Si_{0.7}Ge_{0.3}$ is compared with
that of Si.  On both silicon and silicon-germanium, the oxide thickness decreases
logarithmically with the increase of writing speed and increases approximate linearly
with the increase of bias voltage.  However, the feature height (and thus the oxide
thickness) on $Si_{0.7}Ge_{0.3}$ is lower than on silicon.  In contrast, under thermal wet
oxidation (~ 800 °C), the oxides grown on SiGe can be 2.5 times thicker than those
grown on silicon [13].  Thus the lower rate of AFM oxidation on SiGe might be
associated with a lower rate of water dissociation, or with differences in the water
adsorption on the sample surfaces, rather than a lower reaction rate of the oxidizing
species with SiGe.  It has been reported that unlike on silicon, water does not stick
easily on a Ge(100) surface at room temperature [14].  The disappearance of the infrared
Ge-H stretching vibration when Ge(100) is exposed to water at room temperature leads
to a conclusion that either absorption does not occur (low sticking coefficient) or
adsorption occurs without dissociation, which is in contrast with Si(100) which has a
higher possibility of water dissociation [15].  However, how this relates to a $Si_{0.7}Ge_{0.3}$
surface, and to the oxide surface which is present once oxidation begins, is not known.

## 5.4    Nanopatterning of Si/SiGe Heterostructures

Our goal is to use AFM local oxidation to pattern nanodevices in Si/SiGe
heterostructures.  From the above experiments, we find the maximum thickness of SiGe
oxidized by AFM LAO is less than 2.0 nm when the absolute bias voltage on the AFM

tip is $\leq 30$V.  A higher voltage $V > 40$ V causes linewidth greater than 300 nm.  Thus
devices with a SiGe layer thickness greater than 2.0 nm cannot be directly patterned by
a single direct AFM LAO step.  Therefore, the layer structure shown in Fig. 5-6(a) was
used with a modified pattern transfer approach.  A 9-nm-thick $p^+$-$Si_{0.7}Ge_{0.3}$ strained
layer with 2-nm-thick i-$Si_{0.7}Ge_{0.3}$ layers on top and bottom of it was first grown on
silicon as a conduction layer for a device, followed by a thin ($\sim 2$ nm) Si cap.  At low
temperature, the holes are confined to the doped SiGe layer by the valence band offset
between Si and compressive-strained SiGe.
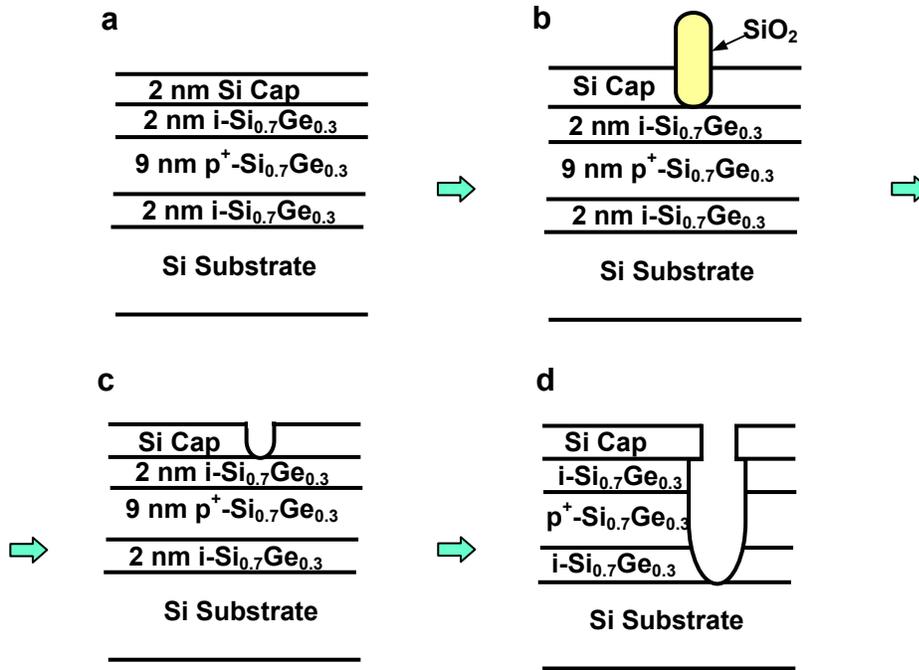


**Figure 5-6.**  Process to pattern Si/SiGe nanostructure: (a) Layer structure; (b) Si cap
AFM local oxidation; (c) HF dip to remove $SiO_2$; (d) selective wet etching to transfer
pattern into thick SiGe layer.  The degree of lateral etching due to the isotropic wet
etch is greater than shown.

One way to define nanostructures is to cut the $p^+$-$Si_{0.7}Ge_{0.3}$ layer laterally.  First,
the 2-nm-thick silicon cap layer was locally oxidized by AFM (Fig. 5-6(b)).  The silicon
oxide was subsequently removed by diluted HF (Fig. 5-6(c)), and finally selective wet

etching (HF: $H_2O_2$: $CH_3COOH$ = 1: 2: 3) of the SiGe with a selectivity ~ 400: 1 over
silicon [16] transferred the oxide pattern into the strained $Si_{0.7}Ge_{0.3}$ layer (Fig. 5-6(d)).
Compared with direct AFM oxidation, this second method reduces pattern resolution
due to the isotropy of the wet etching, and increases the minimum linewidth from 20 nm
to 50 nm.  However, 10-nm-thick SiGe layers were successfully patterned by this
approach.  Demonstration of this nanopatterning technique to create a quantum dot
device is shown in Fig. 5-7(a) and Fig. 5-7(b).
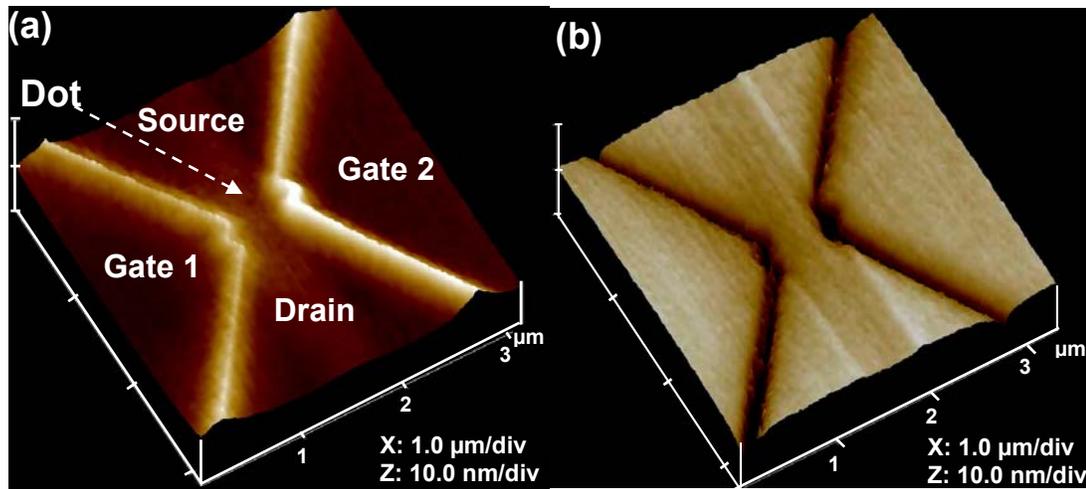


**Figure 5-7.**  AFM images of a SiGe quantum dot fabricated by AFM nanopatterning
approach (a) after AFM oxidation and (b) after selective wet etching.  The device is
discussed in Sec. 5.5.

To confirm the patterning of the SiGe layer, a Hall bar was fabricated by first
etching the Si and SiGe of the sample by optical lithography and RIE before AFM
lithography.  This created a mesa structure with a height of ~ 200 nm.  Ohmic contacts
were made for electrical measurements by Al thermal evaporation and a forming-gas
anneal.  A line was then cut across the current path in the SiGe layer (Fig. 5-8a) by
AFM LAO of silicon and selective wet etching of $Si_{0.7}Ge_{0.3}$ as described above.  The *I-
V* characteristics of the device were measured in liquid helium ($T$ = 4.2 K, Fig. 5-8b).

**(a)**



**(b)**
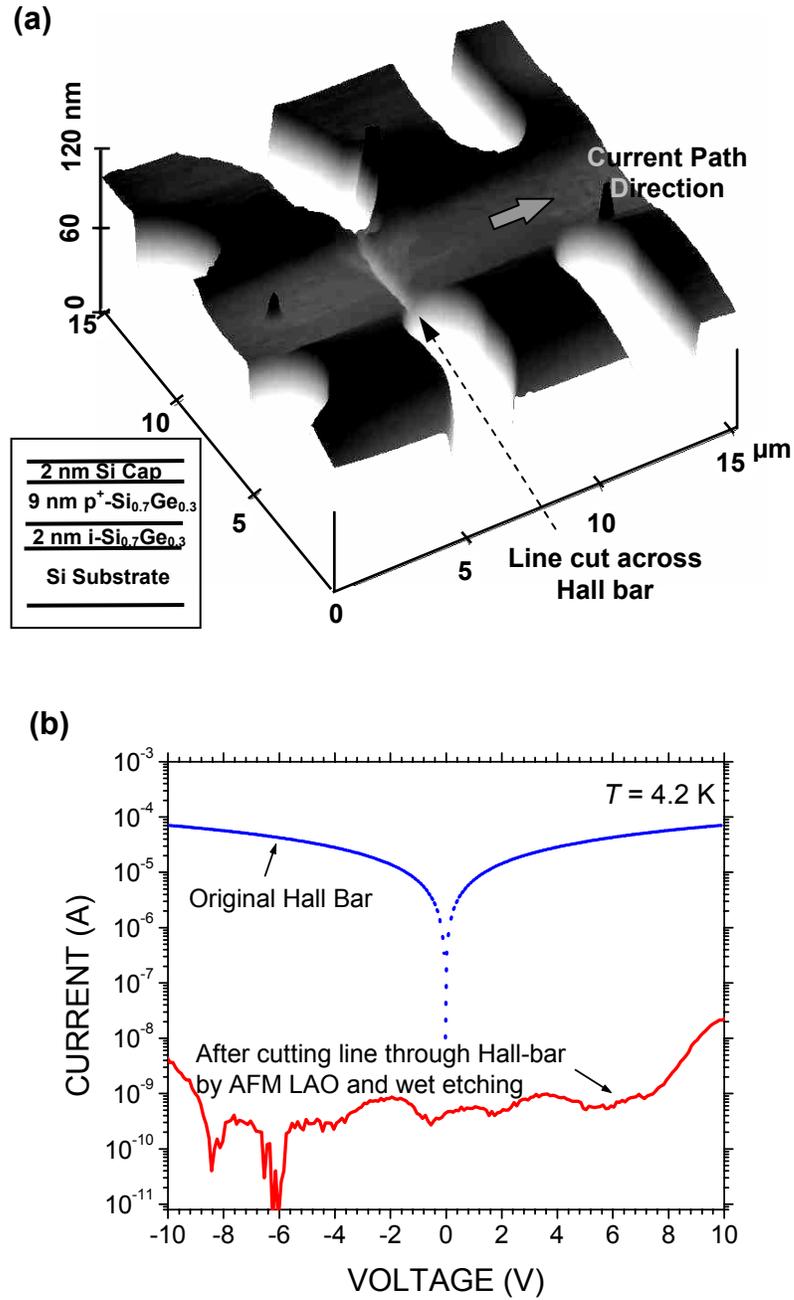


**Figure 5-8.** (a) AFM image of a line cut across Hall bar by AFM local oxidation and selective wet etching in a sample with the layer structure of Fig. 5-6.  The sample was pre-patterned by optical lithography and RIE to create mesa Hall bar structure.  (b) Hall bar resistance measurement at $T$= 4.2 K before and after line cutting the Hall bar.

At this low temperature, all the carriers in the sample were frozen out except holes in

the p$^+$-SiGe layer with boron doping concentration $\sim 1 \times 10^{19}$ cm$^{-3}$, greater than the

metal-insulator transition point [17].  The holes are confined to the SiGe by the valence

band offset.  The resistance of the original Hall bar without cutting line is $\sim$ 130 K$\Omega$,

which increases to $\sim$ 10 G$\Omega$ after the SiGe layer was cut at the line.   This clearly

indicates the complete cutting of the p$^+$-SiGe layers by the wet etch method to transfer

the AFM oxidation pattern in Si to the SiGe. Note that the potential barrier formed by

line cutting starts to leak when applied voltage $|V| > 8$ volts.  This is presumably due to

holes in the SiGe tunneling into the silicon substrate, and then moving across the gap to

the other SiGe section.

## 5.5    SiGe Quantum Dot Device

Quantum dots (QDs) are spatially small regions to which carriers may be

confined in three dimensions.  The number of carriers may range from one to a few

thousand electrons or holes.    Because of the small volume, the allowed electron

energies within the dot are quantized, forming a discrete spectrum of quantum states not

unlike the energy levels of an atom.  When a QD is weakly coupled with two electron

reservoirs (source and drain) and its electrochemical potential is controlled by gate, a

single electron transistor is formed (Fig. 5-9).  Adding one electron to the QD will

increase the energy of the QD by $e^2/C_\Sigma$  due to Coulomb interaction of electrons,

where $C_\Sigma$  is the total capacitance of the QD.  When this Coulomb charging energy

$e^2/C_\Sigma$  is substantially greater than thermal energy $k_BT$, the tunneling of electron to the

QD is prohibited except at certain gate voltages.  This is called a Coulomb blockade.

With the tuning of the electrochemical potential of the QD by applying a gate voltage,

one electron tunnels from the source into the QD and from the QD into the drain as one

empty energy level in the QD is adjusted to be lower than Fermi-energy levels of the
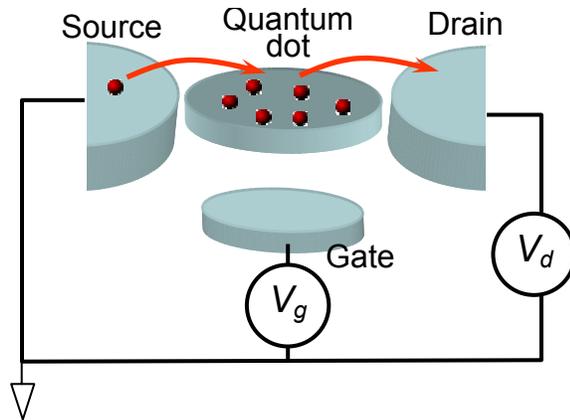
**Figure 5-9.** Schematic diagram of a QD laterally connected to source/drain contacts by tunnel junctions, and to a gate by a capacitor.
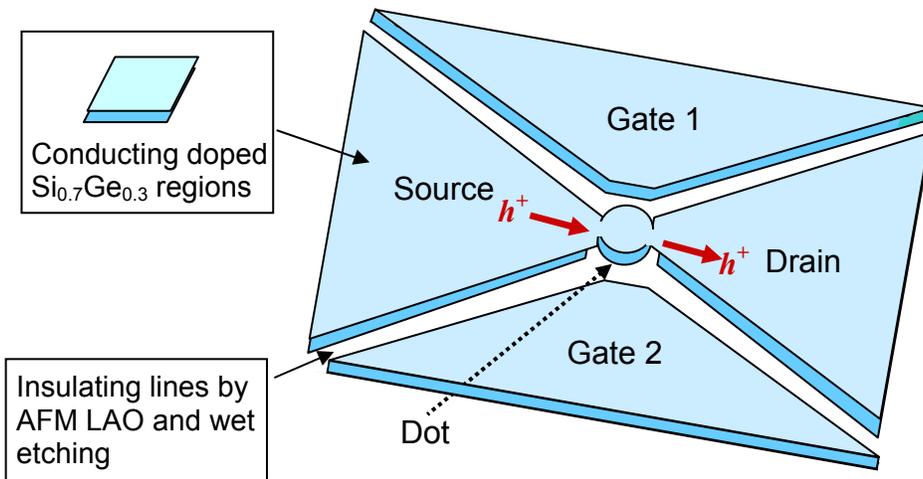


**Figure 5-10.** Schematic diagram of QD fabricated by AFM LAO and wet etching, and path of hole transport in the device.

source and drain.  The number of electrons in the QD changes one by one, alternating
with Coulomb blockade of tunneling.  To observe this phenomenon, the other
requirement is that the tunneling junctions of source/dot and drain/dot are opaque
enough, with the resistance $R_t >> h/e^2$, so that electron is located either in the source, or
in the drain, or on the dot.  Thus the fluctuation of the number of electrons in the QD is
negligible.  The theoretical background of these QD devices will be described detailed
in Chapter 6.

A SiGe quantum dot was fabricated on the Si/$p^+$-SiGe/Si layer structure of Fig.
5-6(a) by AFM local oxidation and wet etching as described above.  Figure 5-7(a)
shows the dot structure after AFM local oxidation.  The dot size was estimated to be ~
160 nm in diameter.  It became smaller after wet etching, and was expected to be ~ 70 −
100 nm.  The small size of the quantum dot leads to a low QD capacitance so that the
charging energy $e^2/C_\Sigma >> k_B T$ at $T = 4.2$ K.  As shown in Fig. 5-10, the dot is directly
connected to the source and drain.  However, at the two laterally narrow regions at the
junctions of source/dot and dot/drain, potential barriers form due to quantum
confinement.  Combined with the Si/SiGe valence band offset below the dot, and the air
interface on the top of the dot, and the dot sides after patterning by AFM, a quantum dot
for holes is formed.  The two co-planar SiGe regions on either side of the dot are
electrically insulated from it (through the cutting of the SiGe layer), and thus serve as
lateral gates, which can modulate the electrical potential in the dot.  Similar structures
have been made in doped SiGe layers on silicon-on-insulator substrates fabricated by
electron-beam lithography and RIE [18].

Electrical measurement on this QD device was first performed at $T = 4.2$ K.  In
Fig. 5-11, we see that the source-drain current decreases with one gate voltage, and goes
to zero at $V_g = 6$ V.  This is the normal behavior of a transistor, which would be seen at
room temperature if parallel conduction through the substrate were shut off.  Most
significantly, the current also exhibits oscillations with gate voltage, which is believed
to be due to Coulomb blockade effects.  However, the oscillations (current peak height
and peak position) are not reproducible at different scans, and the current has
considerable noise.
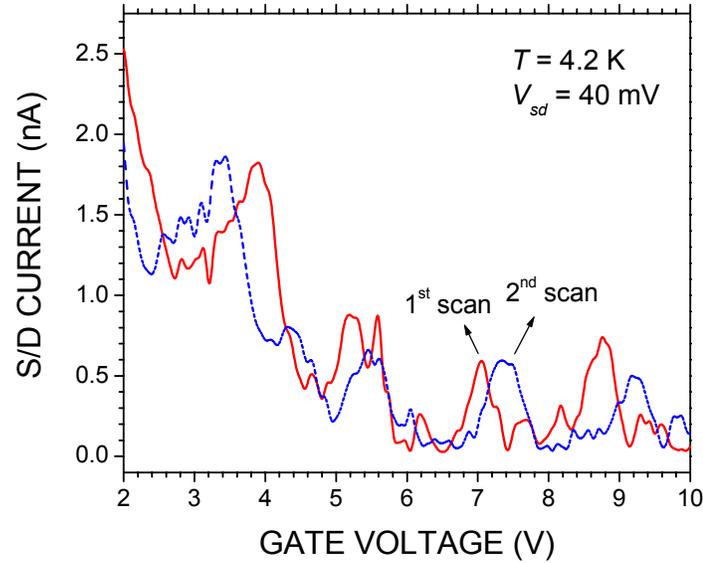
**Figure 5-11.**  Source-drain current *vs.* one planar gate voltage at $T = 4.2$ K and $V_{ds} =$ 40 mV.  The other gate was grounded.  The solid line represents the electrical results for the 1st measurement scan, and the dotted line is for the 2nd scan.

 

The device was further cooled down to 0.53 K.  At this low temperature, the conductance exhibits oscillations as a function of the gate voltage (Fig. 5-12), associated with a Coulomb blockade.  The oscillations are not periodic, and $V_g$ scans in different directions are not reproducible.  Figure 5-12(b) shows differential conductance with one gate voltage of the QD at source-drain voltages from −30 mV to +30 mV with a step of 4 mV.  When source-drain bias voltage is low, source-drain currents are blocked at all gate voltages.  Current peaks do not appear until $|V_{ds}| \geq 18$ mV.  This "stochastic Coulomb blockade" [19] is the typical signature of tunneling through multiple QDs.  The current flows only when the empty energy levels in all multi-QDs are tuned to line with the Fermi-levels of source and drain, which is, of course, accidental.  High source-drain bias voltages (Fig. 5-12b) and high thermal activation (high $T$) enhance the possibility of this line-up.
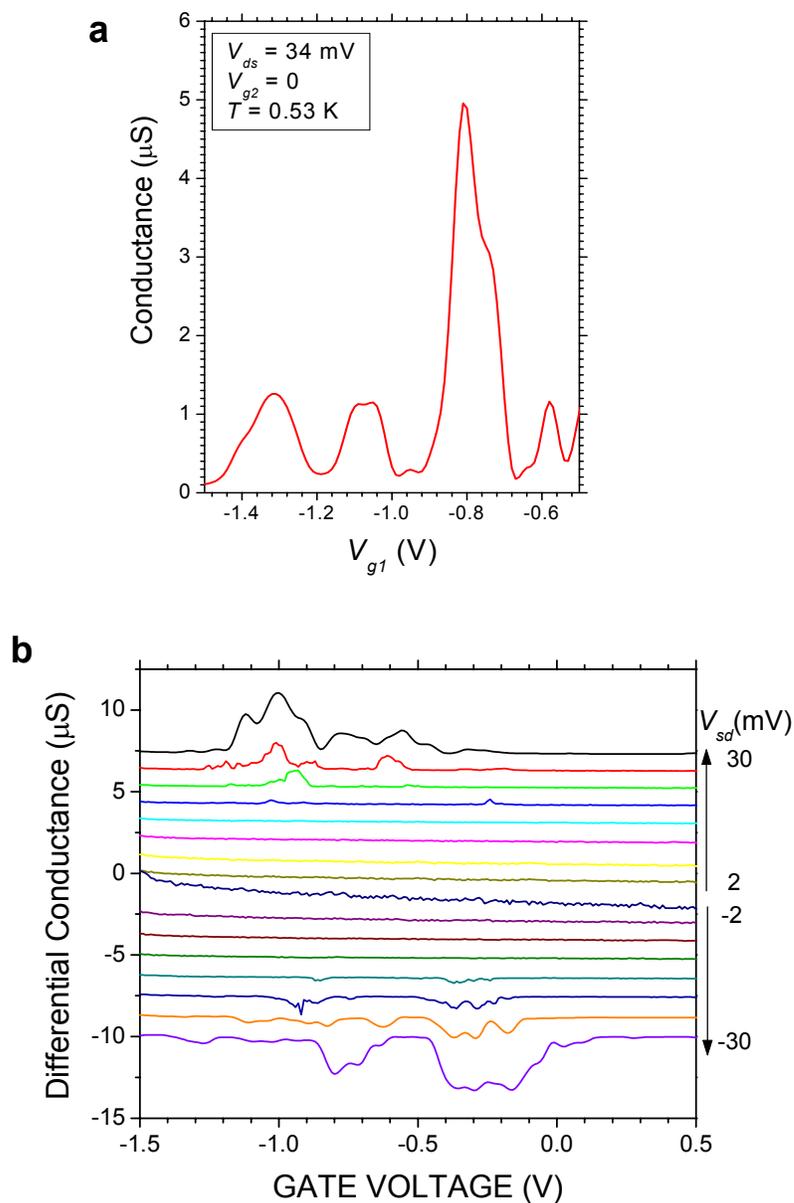
**Figure 5-12.** Electrical characteristics (differential conductance *vs.* gate voltage) of
the SiGe quantum dot fabricated by AFM LAO and selective wet etching, at $T = 0.53$
K with source-drain bias at (a) −34 mV and (b) −30 mV to +30 mV with bias step of 4
mV.  In (b), all curves are offset by 1.2 μS.

The multiple QDs were not created and designed, which are attributed to the large number of trap states at the surface of the SiGe.  In the dot, the electron wavefunction extends to the surface of the etched region, which is not passivated (except by a thin native oxide).  Thus, trapping-detrapping of charges at the surface is expected.  The irreproducibility of the *I-V* curves, such as that in Fig. 5-11 is also attributed to the trapping/detrapping of the carriers by various defect states.  Thus we conclude that the performance of the device is greatly impaired by the unpassivated surface of the dot.

To passivate the SiGe QD device, we plan to use silicon epitaxial regrowth to cover the exposed SiGe surface.  Due to the coherent interface between strained SiGe and Si, the interface states are expected to be removed.  The regrowth process is described in the next three sections, and the device characterization of the passivated device in chapter 6.

## 5.6    Motivation for Hetero-Epitaxial Dot Passivation

As in our devices, QD devices fabricated in unpassivated heavily-doped-silicon on insulator (SOI) exhibit Coulomb blockade oscillations with irreproducible oscillation peak positions and peak amplitudes, which are related to surface defects at the $Si/SiO_2$ interface [20,21].   As we know, the best quality thermal $SiO_2$ has interface defect state density greater than $10^{10}$ cm$^{-2}$ with Si [22].   We think this is why the *I-V* characteristics of Si QD devices with a MOSFET structure have undesired oscillations at low temperatures [23].  To remove the defect states related to $SiO_2$, we propose that the surface of the SiGe QD device should be passivated by silicon epitaxial regrowth after AFM nanopatterning, as shown in Fig. 5-13.  The compressive-strained SiGe (on a Si substrate) has a lattice-matched interface with epitaxial silicon.  Therefore, interface

states are therefore expected to be removed in a SiGe QD device passivated by silicon
epitaxial regrowth.
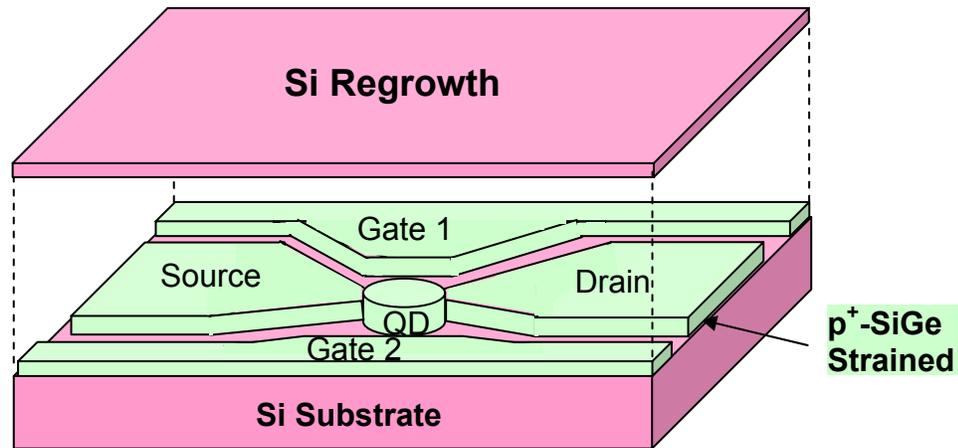


**Figure 5-13.** Schematic drawing of SiGe QD device and Si epitaxial regrowth.

After the surface of epitaxial layers is exposed to the atmosphere and patterned
by lithography, it is covered by native oxide and other impurities. To obtain clean
epitaxial regrowth, the oxide and impurities must be first removed. Preparing a "clean"
Si or SiGe surface for epitaxial growth is very important for high quality structures.
Traditionally, CVD growth requires high temperature *in-situ* cleaning, such as hydrogen
baking at 1000 °C, to remove contamination from the surface. Such temperatures are
often unacceptable if the pre-existing devices have dopant profiles, as is the case in our
devices. Pre-cleaning processes with low thermal budgets have been studied by many
groups [24,25,26]. Recently, Carroll *et al.* [26] has achieved a carbon-free and oxygen-free
silicon surface with hydrogen baking at 800 °C, upon which SiGe was then grown at
625 °C. However, little work has been done to develop process to clean SiGe for
further Si growth. In the next two sections, the epitaxial regrowth process of Si on SiGe
surface will be investigated.

## 5.7    Planar Regrowth Process of Epitaxial Silicon on SiGe and Material Characterization

### 5.7.1    Cleaning and Epitaxial Condition

First experiments were done on an unpatterned SiGe surface.  After first growing a 1-µm-thick silicon buffer at 1000 °C, a pseudomorphically strained $Si_{0.8}Ge_{0.2}$ layer with a thickness of ~ 20 nm was grown at 625 °C by RTCVD.  A silicon capping layer can be directly grown at 700 °C if desired (uninterrupted growth), or the growth can be interrupted.  To simulate the handling of a wafer which will be received from AFM patterning, the wafer was then unloaded from the CVD reactor and left in a fume hood for half an hour.  Before loading back into the CVD chamber, the sample was chemically cleaned by a mixture of $H_2SO_4$: $H_2O_2$ = 1: 1 for 15 min and dipped in diluted HF with DI water (1: 1000) for 2 min [26].  The wafer surface was then cleaned by an in-situ bake in hydrogen with a flow rate of 3 lpm and pressure of 10 torr, at a temperature of ~ 800 °C for 2 min.  Then, 100-nm-thick silicon was subsequently regrown at 700 °C.  The flow rate of dichlorosilane was 26 sccm in a hydrogen carrier at 3 lpm at a pressure of 6 torr.  The growth rate is ~ 26 Å/min.  Note that the diffusivity of boron in SiGe at 800 °C is ~ $2 \times 10^{-17}$ $cm^{-2}s^{-1}$ [27]; thus the diffusion length is < 1 nm for 2 min. The boron diffusion should be insignificant in our regrowth process.  No patterning was done on this sample.

### 5.7.2    SIMS Analysis

The Si/SiGe interface quality was characterized by secondary ion mass spectroscopy (SIMS) and photoluminescence (PL).  All characterization (by SIMS or PL) was done within 20 mm of the wafer center.  SIMS was done at Evans East, NJ, using a 3 keV $Cs^+$ primary ion beam.  The sputtering rate was 5-15 Å/s, characterized
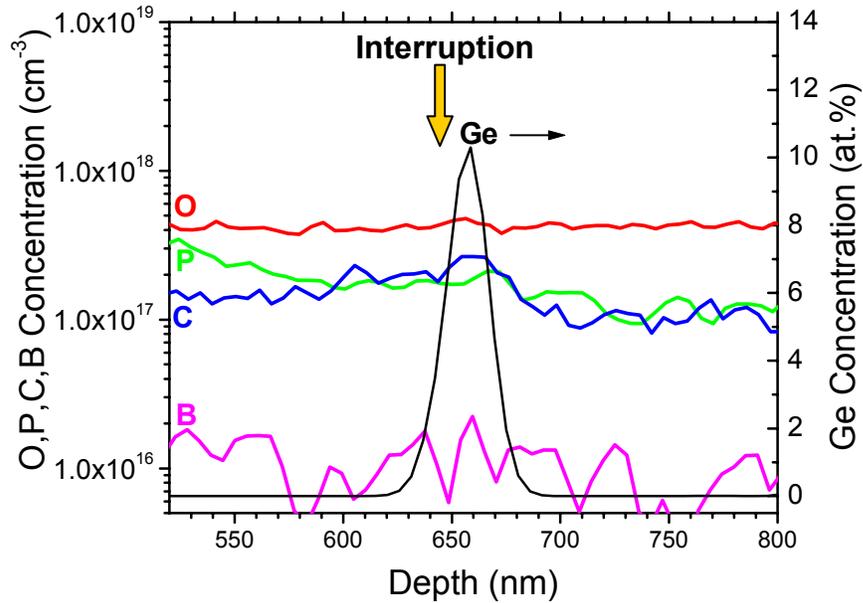
**Figure 5-14.** Oxygen, carbon, phosphorous, boron and germanium SIMS profiles of a
sample with epitaxial regrowth of silicon on strained SiGe layer. Before regrowth, an
*in situ* hydrogen bake at 10 torr and 800 °C for 2 min was performed.

by profilometry, leading to a 5% uncertainty in depth profile. The carbon and oxygen

detection limits are approximately $10^{17}$ and $10^{18}$ cm$^{-3}$, respectively. The chemical

specie concentrations were measured to within 15% error. Figure 5-14 shows SIMS

results on the regrown sample. At the interruption interface between the SiGe and the

Si cap, no increase of oxygen, phosphorous, or boron was detected, which means 800

°C is high enough to remove the native oxide on SiGe surface. The carbon has a slight

increase across the whole SiGe layer, and the integrated concentration is $\sim 1.5 \times 10^{12}$

cm$^{-2}$. We do not know the exact source of the carbon increase in this regrowth process.

It may be due to the lower bake temperature. However, the fact that the carbon

concentration starts increasing at the beginning of SiGe growth instead of the ending

position (*i.e.* the regrowth interface) makes us think that the carbon increase is related to
the SiGe growth rather than the regrowth process.  (We do sometimes find a carbon
increase in the SiGe layer grown at 625 °C immediately after Si growth at 700 °C in our
RTCVD reactor without interruption [28].  It may be because the lower growth
temperature and/or a higher carbon absorption coefficient on SiGe than on Si lead to a
high carbon concentration at the interface when RTCVD growth switches from Si to
SiGe).

### 5.7.3   Photoluminescence

Photoluminescence was performed at 77 K with a pump of an argon laser with a
wavelength of 514 nm, intensity on the sample of ~ 10 W/cm$^2$, and total pump power of
~ 1.0 W.  The PL spectra were detected after a monochromator by a germanium
detector cooled down by liquid nitrogen with an applied negative bias ~ 250 V.  An AC
lock-in amplifier was used to reduce noise.  In our sample, the compressively strained
SiGe layer, from which the PL is emitted, is surrounded by Si layers above and below.
The valence band offset confines holes to the SiGe.  Most of the excited carriers are
generated in the silicon substrate, and then diffuse into the SiGe quantum well, where
radiative recombination of electrons and holes causes SiGe luminescence.  The
luminescence intensity from the strained SiGe quantum well is extremely sensitive to
the carrier lifetime.  Any defects or contamination at the interface will increase the non-
radiative recombination rate, and thus decrease the luminescence intensity emitted from
the strained SiGe.  Therefore, the PL intensity from the SiGe (as well as the ratio of the
PL from SiGe to that from the Si) is used to characterize the regrowth quality.  Figure 5-
15(a) shows the PL spectra from a 20-nm-thick $Si_{0.8}Ge_{0.2}$ sample capped with Si grown
in our RTCVD chamber without interruption [29].  The two strong peaks are related to
the no-phonon (NP) transition and transverse optical (TO) phonon replica (for
conventional momentum conservation).  The randomness of sites of Ge in SiGe alloy
relaxes the crystal momentum-conservation rule during electron-hole recombination,
which makes it possible that luminescence without a phonon accompanying to conserve
momentum is emitted from SiGe layer.  The silicon PL is emitted only via a TO-phonon

mechanism at 77 K. In the sample with a contaminated interface at the Si/SiGe, recombination quenches the two luminescence peaks from SiGe (Fig. 5-15b). Therefore, in our CVD system, a SiGe quantum well grown without interruption and presumably with a "clean" interface has a SiGe/Si intensity ratio of over 15 [26].
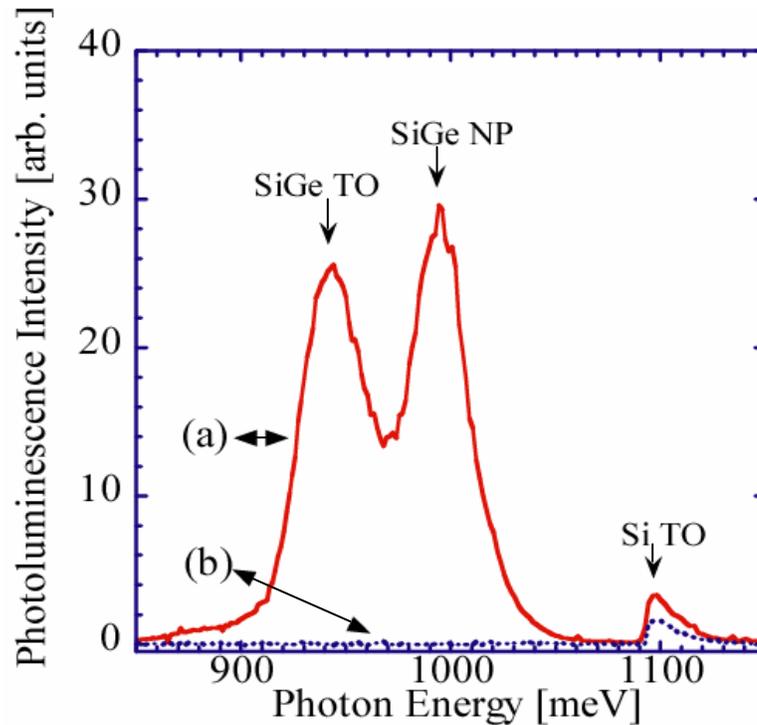


**Figure 5-15.** Photoluminescence spectra of $Si_{0.8}Ge_{0.2}$ samples at $T = 77$ K with (a) a "clean" Si/SiGe interface grown without interruption, and (b) a contaminated Si/SiGe interface. The two strong peaks in (a) are from the no-phonon (NP) transition and transverse optical (TO) phonon replica in SiGe layer [29].

Figure 5-16 shows the PL spectra from the sample of regrown silicon (r-Si) on strained $Si_{0.8}Ge_{0.2}$ with pre-cleaning at 800 °C, as described above. The two strong peaks from SiGe quantum well are clearly seen. The peak intensity is 30 times greater than that from the silicon TO peak, which indicates the regrowth interface between Si and SiGe is comparable to the uninterrupted interface.
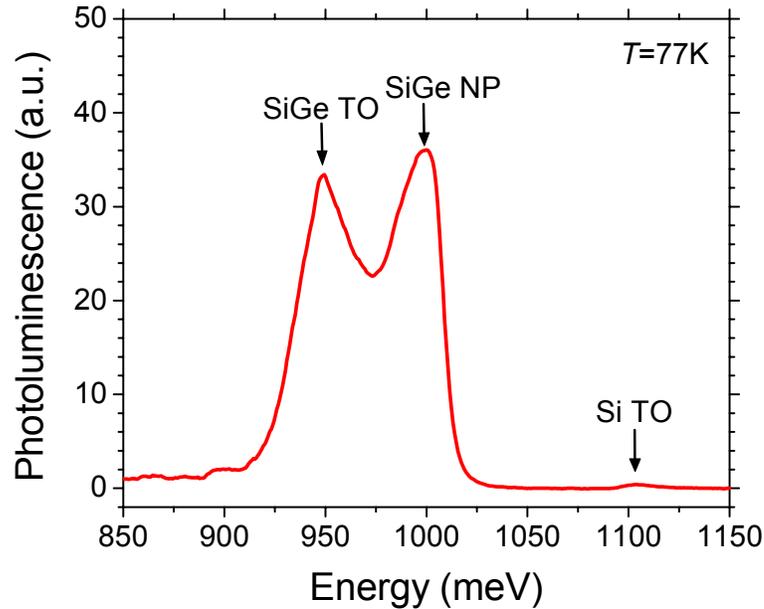
**Figure 5-16.** PL spectrum at $T = 77$ K of regrown silicon on strained $Si_{0.8}Ge_{0.2}$.
During regrowth, *in situ* hydrogen pre-baking was done at 10 torr and 800 °C for 2
min.

## 5.8    Epitaxial Regrowth of Silicon on Nanopatterned Surfaces

### 5.8.1   Growth Procedure

In this section, we describe epitaxial silicon regrowth on nanopatterned SiGe
surfaces and material characterization. The original layer structure was 2-nm-$Si_{0.7}Ge_{0.3}$,
9-nm-$p^+$-$Si_{0.7}Ge_{0.3}$, 2-nm-$Si_{0.7}Ge_{0.3}$, and 2-nm-Si (see Fig. 5-18b). The growth
temperature was ~ 625 °C for $Si_{0.7}Ge_{0.3}$ with $GeH_4$ (0.8% in $H_2$) flow rate at 300 sccm,

$H_2$ at 3 lpm, dichlorosilane at 26 sccm and pressure at 6 torr.  Si was grown at ~ 700 °C with the same condition except no germane.  The intrinsic 2-nm-thick $Si_{0.7}Ge_{0.3}$ layers are used to prevent boron diffusion from $p^+$-$Si_{0.7}Ge_{0.3}$ into the Si substrate and Si cap to make a more effective electrical barrier at the hetero-interfaces.  A Hall bar was first patterned by conventional lithography and RIE to give reference features by which the later nanopatterns could easily be found.  A nanoline was patterned into the $Si_{0.7}Ge_{0.3}$ by AFM local oxidation and selective wet etching (see Fig. 5-6).  Si epitaxial regrowth was performed at 700 °C for 40 min after surface cleaning by wet chemicals and in-situ hydrogen baking for 2 min.  The baking temperature was set at ~ 800 °C, but the real temperature on the sample was estimated to be ~ 775 °C [30].  The temperature of a 100 mm wafer in our CVD reactor decreases from the center to the edge.  In this case, we used a small 1-cm square sample which was supported in a micromachined 100 mm wafer holder and located ~ 25 mm away from the center of the 100 mm wafer (see Fig. 5-17).  Thus the actual sample temperature is < 800 °C.
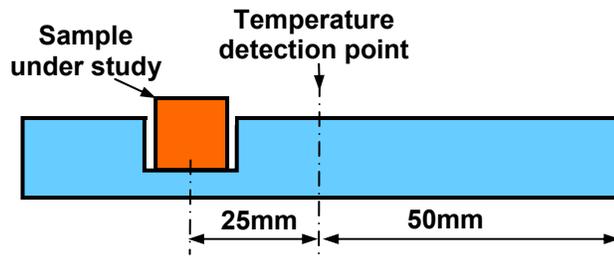


**Figure 5-17.**  Small-piece sample position and temperature monitor position in a 100 mm wafer.

### 5.8.2   Cross-Section TEM Observation

To characterize the regrowth interface, cross-section TEM has been performed on a patterned regrown sample.  This TEM observation was performed by Dr. Nan Yao in Hitachi Labs of California.  A Hall bar was first etched in the initial Si/SiGe structure as in Sec. 5-4.  A nanoline was first patterned in the middle of the Hall bar by AFM

oxidation of the top Si and wet etching of the SiGe as in Fig. 5-6. This was followed by a 20-nm-thick Si epitaxial regrowth (Fig. 5-18), using the above procedure. A cross-section TEM sample is very hard to make in this sample, because the length of the nano-structures we want to examine is fairly short ($\sim$ 30 µm) and the number of the nanolines is one or two due to AFM lithography limitations. Thus conventional sample preparation technique for cross-section TEM cannot be used. A focused ion beam (FIB) was used to prepare the TEM sample. A thin ridge was created along the dotted-line A-A' in Fig. 5-18(a) by removing material on either side of it. Before FIB cutting, the sample surface was protected by depositing iridium and carbon layers. Gallium ion sputtering cut the sample and thinned the ridge down to a final thickness < 500 Å. The TEM observation and FIB sample preparation chambers are connected with each other. Thus, the TEM sample can be transferred back to the FIB chamber for further thinning if necessary.
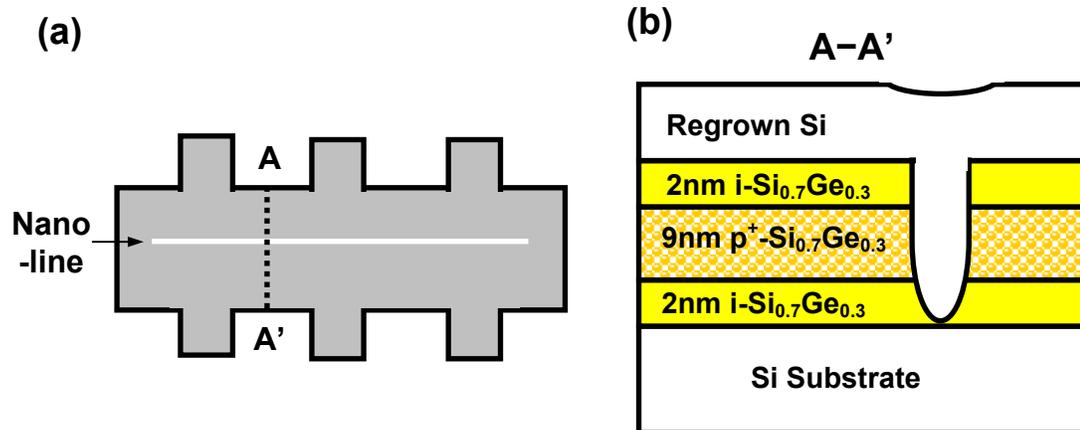


**Figure 5-18.** (a) A nanoline is patterned on a Hall bar by AFM LAO and wet etching; (b) the cross-section of the structure across the line A-A', which was imaged by TEM.
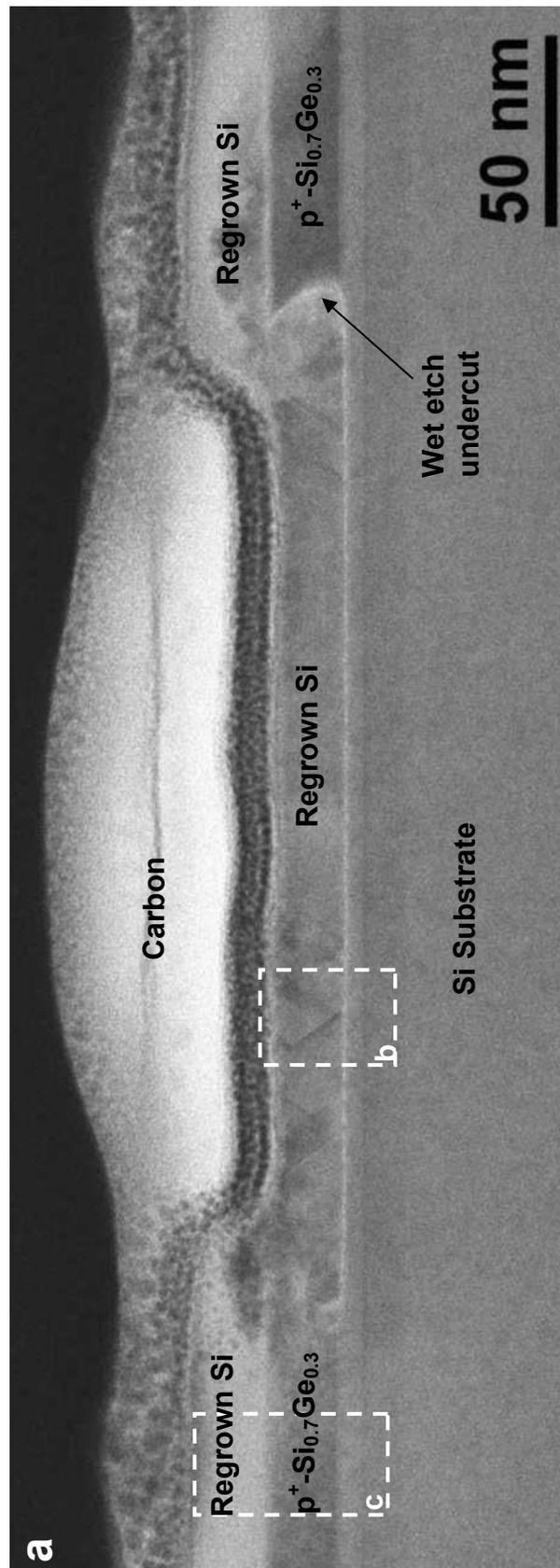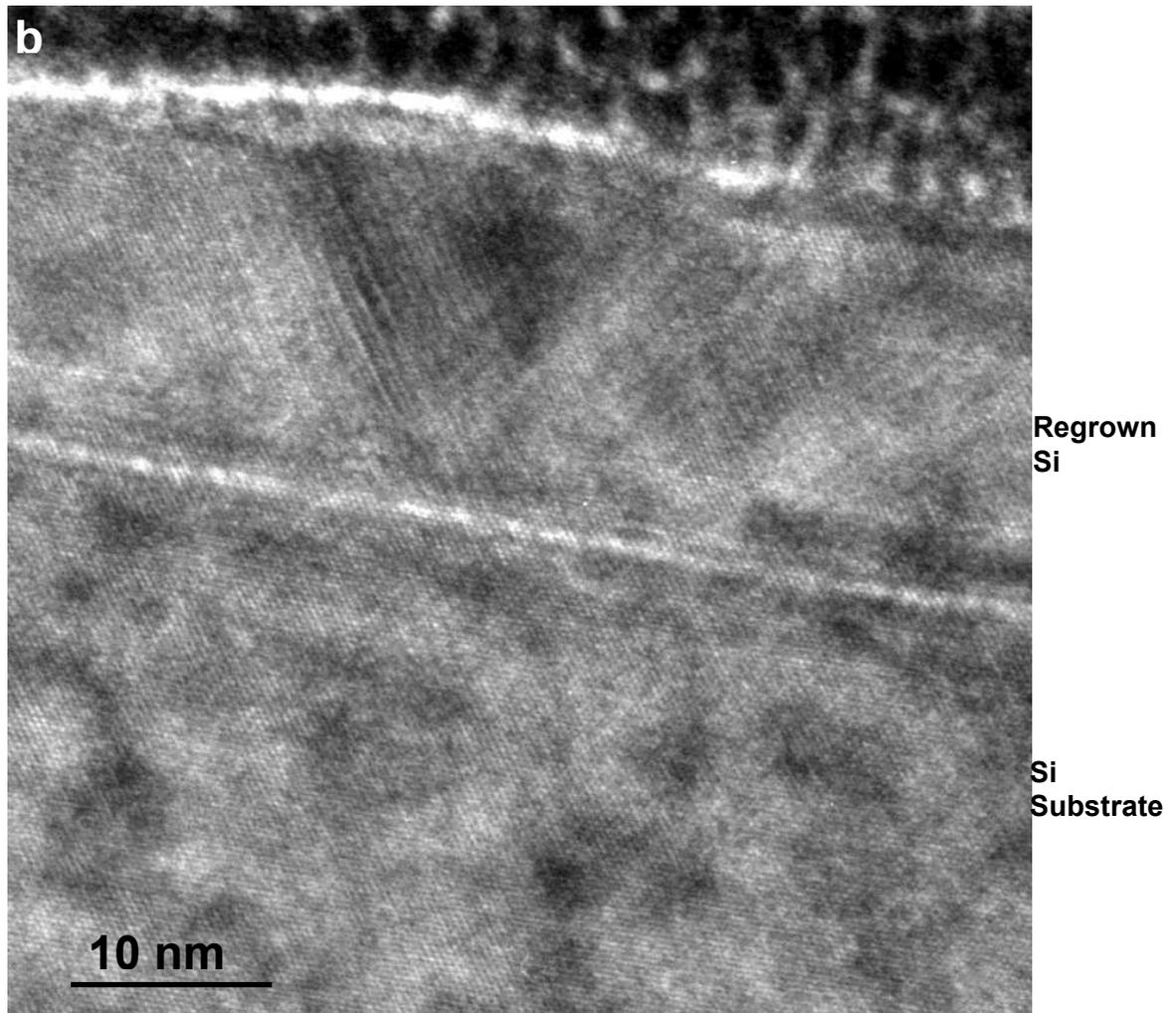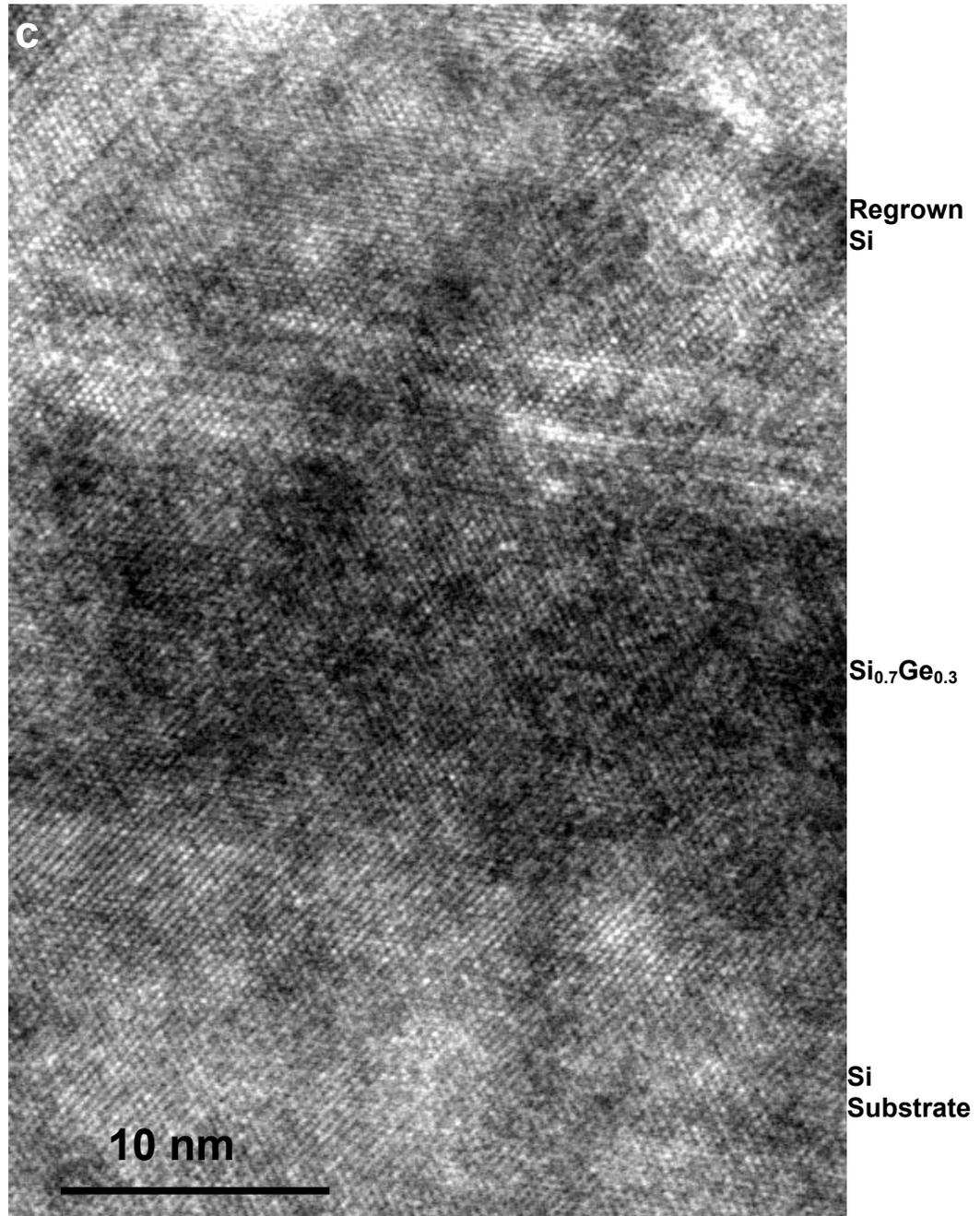
**Figure 5-19.** (a) Cross-section TEM images of regrown Si on a line trench in
$Si_{0.7}Ge_{0.3}$ layer patterned by AFM LAO and wet etching. High-resolution TEM image
of (b) regrown Si on Si substrate in the trench, and (c) regrown Si on strained
$Si_{0.7}Ge_{0.3}$ layer outside of the trench. The regions of (b) and (c) are marked by the
dashed-line rectangles in (a).

Figure 5-19(a) is the cross-section TEM image of the regrowth sample at the nano-trench.  The width of the region where the SiGe was removed is ~ 200 nm.  The interfaces of regrown-Si/Si substrate and regrown-Si/$Si_{0.7}Ge_{0.3}$ (at the left and right of the image) are clearly seen.  At the right edge of the trench, an unusual edge profile of the SiGe is observed ――― SiGe etched more at the bottom than at the top, the opposite of that expected for wet etching.  The silicon clearly conformally surrounds the SiGe on top sides as desired.  High resolution images enlarged from the rectangles b and c in Fig. 5-19(a) are shown in Fig. 5-19(b) and (c), corresponding to the interfaces of the Si regrowth in the trench and outside of the trench, respectively.  First, we can see the regrown Si is single-crystalline.  The lattice continues at the interfaces of regrown Si on Si substrate in the trench and regrown Si on $Si_{0.7}Ge_{0.3}$ layer outside of the trench, which indicates the epitaxial regrowth has been achieved.  However, both of the interfaces are not defect-free.  Stacking faults exist in the regrown Si layer both above the Si substrate and the SiGe.

We do not know the exact reason for the defects, which may be related to an insufficient hydrogen bake temperature, a low growth temperature, or the chemical surface cleaning process.  The possibility of a lower growth and cleaning temperatures than intended was explained in the previous section.  The epitaxial regrowth process needs further development.  However, we hope the electrically active defect density in our regrowth sample should be much less than that at $Si/SiO_2$ interface.  While the $Si/SiO_2$ interface state density within the bandgap on a <100> Si surface can be ~ $10^{10}$ $cm^{-2}$,  it is known to be much higher on other surface planes and on irregular surfaces, as would be the case to surround a quantum dot.  We hope that our devices are improved compared to previous Si or SiGe quantum dot devices with $Si/SiO_2$ passivation.

## 5.9    Electrical Characteristics of Nanolines after Epitaxial Regrowth
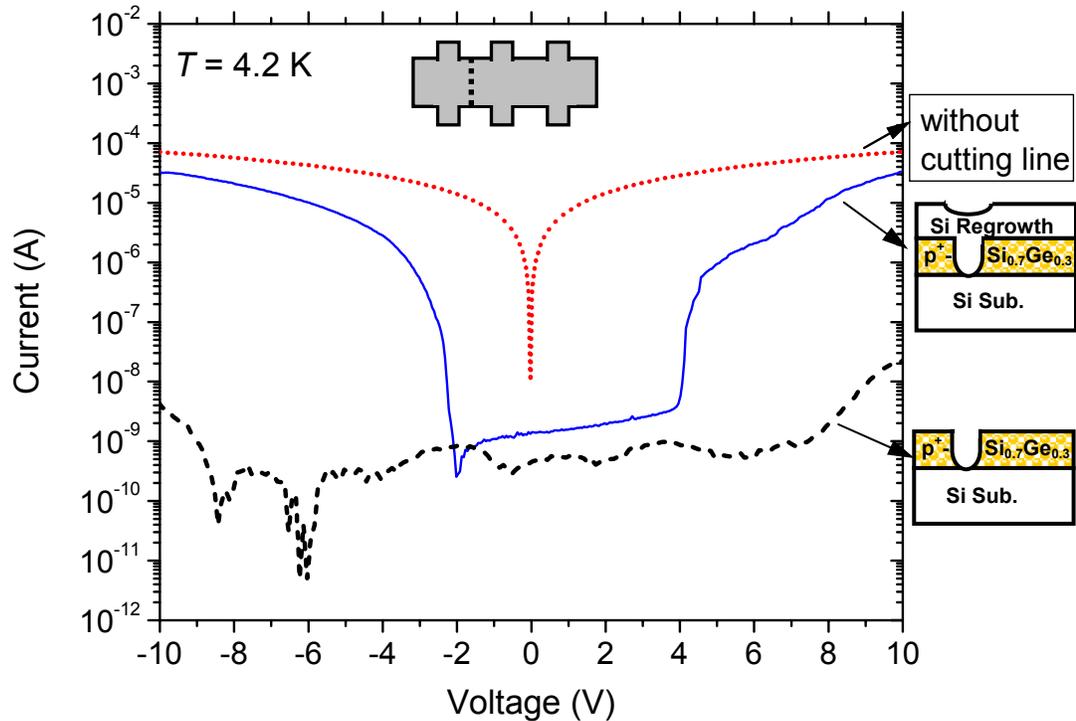


**Figure 5-20.**  *I-V* curves across a nanoline in a Hall bar (inset) with and without
silicon epitaxial regrowth.  After regrowth, the current starts to leak at a lower bias
voltage (compared to Fig. 5-8).

     *I-V* characteristics across a nanoline in a p$^+$-doped SiGe Hall bar pattered by
AFM nanolithography are shown in Fig. 5-20, both before and after epitaxial regrowth.
Two curves (without cutting and after cutting but before regrowth) are the same as those
in Fig. 5-8.  The structure was then passivated by Si regrowth, following the same
procedure as in the previous section.  After the nanoline was passivated by silicon

epitaxial regrowth, the resistance across the nanoline is still more than four orders of magnitude greater than that before the line was cut (Fig. 5-20).  However, the current through the nanoline is much higher at larger bias voltage than before regrowth. Breakdown now occurs at $\sim |V| = 2$ V, instead of $|V| = 8$ V before Si regrowth.  Before regrowth, the leakage path was through the i-$Si_{0.7}Ge_{0.3}$ and the Si substrate (Fig. 5-21a). After regrowth, this path could leak more due to boron diffusion across the i-$Si_{0.7}Ge_{0.3}$ layer, which increases the leakage of the $p^+$-SiGe/i-SiGe uniaxial diode.  The new leakage path could also go from the $p^+$-$Si_{0.7}Ge_{0.3}$ directly to the gap (Fig. 5-21b).  This path has no i-$Si_{0.7}Ge_{0.3}$ setback layer to reduce the leakage of the $p^+$-SiGe/i-Si uniaxial diode [31].

      After regrowth, the patterned nano-lines can still be considered insulating if the voltage across them is less than $\sim 2$ V in magnitude.  This is still high enough for planar gates to be used to modulate the QD electric potentials, as required for single-hole transistors.  This will be shown in chapter 6.
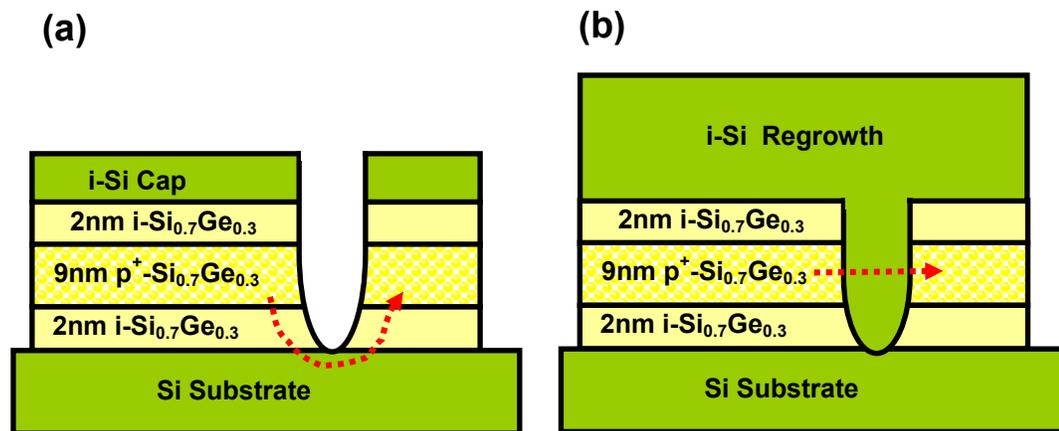


**Figure 5-21.**  Current leakage path marked by dotted lines in the samples (a) before and (b) after Si epitaxial regrowth.

## 5.10  Summary

In summary, two nanopatterning methods of silicon/silicon germanium
(Si/SiGe) heterostructures have been demonstrated: (1) direct AFM LAO on SiGe
layers; and (2) AFM LAO on a thin silicon layer followed by selective wet etching of
SiGe.  When directly oxidizing SiGe alloys, minimum line widths of 20 nm were
achieved by adjusting the bias voltage on the AFM tip.  By AFM LAO and selective
wet etching, a 10-nm-thick conducting SiGe layer was patterned to fabricate Si/SiGe
nanodevices.  Electrical measurement of a SiGe quantum dot shows Coulomb blockade
oscillations, demonstrating the capability of this nanopatterning technique.  However,
the surface passivation of nano-patterned SiGe QDs needs to be improved so that
undesired charging traps at the surface are removed and the QDs have reproducible
electrical characteristics.

To remove the interface states around QD, Si epitaxial regrowth on
pseudomorphically strained SiGe layer has been investigated.  To limit boron dopant
diffusion in the $p^+$-$Si_{0.7}Ge_{0.3}$ layer, the in-situ baking condition in hydrogen to remove
surface impurities was chosen to be 800 °C for 2 min.  The subsequent Si regrowth is at
700 °C using dichlorosilane and hydrogen gases.  SIMS analysis and PL spectra on the
unpatterned regrowth sample indicate the regrowth interface quality is comparable to
that without growth interruption.  However, cross-section TEM observations on the
AFM nanopatterned regrowth sample show stacking faults at the regrowth interfaces of
regrown-Si/Si substrate and regrown-Si/$Si_{0.7}Ge_{0.3}$.  This may be due to a lower
hydrogen baking temperature, and improved epitaxial regrowth processes need to be
developed.  However, the regrowth is epitaxial, which is demonstrated by high-
resolution TEM lattice images.  The electrically active defect density in our regrowth
sample will hopefully be significantly less than that at Si/$SiO_2$ interface, so that
improved *I-V* characteristics of the QD devices may be expected.

# References

[1] K. Ismail, S.F. Nelson, J.O. Chu, and B.S. Meyerson, "Electron transport properties of Si/SiGe heterostructures: Measurements and device implications", *Appl. Phys. Lett.*, **63**: 660-662 (1993).

[2] H. Miyata, T. Yamada, and D. K. Ferry, "Electron transport properties of a strained Si layer on a relaxed Si1-xGex substrate by Monte Carlo simulation", *Appl. Phys. Lett.*, **62**: 2661-2663 (1993).

[3] K. Rim, J. L. Hoyt, J. Gibbons, "Fabrication and analysis of deep submicron strained-Si n-MOSFET's", *IEEE Trans. Electron Devices*, **47**: 1406-1415 (2000).

[4] K. Ismail, M. Arafa, K. L. Saenger, J. O. Chu and B. S. Meyerson, "Extremely high electron mobility in Si/SiGe modulation-doped heterostructures", *Appl. Phys. Lett.*, **66**: 1077-1079 (1995).

[5] E.S. Snow and P.M. Campbell, "Fabrication of Si nanostructures with an atomic force microscope", *Appl. Phys. Lett.*, **64**: 1932-1934 (1994).

[6] P. M. Campbell, E. S. Snow, and P. J. McMarr, "Fabrication of nanometer-scale side-gated silicon field effect transistors with an atomic force microscope", *Appl. Phys. Lett.*, **66**: 1388-1390 (1995).

[7] K. Matsumoto, M. Ishii, K. Segawa, and Y. Oka, "Room temperature operation of a single electron transistor made by the scanning tunneling microscope nanooxidation process for the TiO$_x$/Ti system", *Appl. Phys. Lett.,* **68**: 34-36 (1996).

[8] R. Held, T. Vancura, T. Heinzel, K. Ensslin, M. Holland, and W. Wegscheider, "In-plane gates and nanostructures fabricated by direct oxidation of semiconductor heterostructures with an atomic force microscope", *Appl. Phys. Lett.*, **73**: 262-264 (1998).

[9] X.-Z. Bo, L. P. Rokhinson, H. Yin, D. C. Tsui, and J. C. Sturm, "Nanopatterning of Si/SiGe electrical devices by atomic force microscopy oxidation", *Appl. Phys. Lett.*, **81**: 3263-3265 (2002).

[10] S. R. Kasi, M. Liehr, P. A. Thiry, H. Dallaporta, and M. Offenberg, *Appl. Phys. Lett.*, **59**: 108-110 (1991).

[11] J. Eugene, F.K. Legoues, V.P. Kesan, S.S. Iyer, and F.M. d'Heurle, "Diffusion versus oxidation rates in silicon-germanium alloys", *Appl. Phys. Lett.*, **59**: 78-80 (1991).

[12] E. S. Snow, G. G. Jernigan, and P. M. Campbell, "The kinetics and mechanism of scanned probe oxidation of Si", *Appl. Phys. Lett.*, **76**: 1782-1784 (2000).

[13] F.K. LeGoues, R. Rosenberg, and B.S. Meyerson, "Kinetics and mechanism of oxidation of SiGe: dry versus wet oxidation", *Appl. Phys. Lett.*, **54**: 644-646 (1989).

[14] L. Papagno, D. Frankel, Y. Chen, L.S. Caputi, J. Anderson, and G.J. Lapeyre, "Study of dissociation of water on Ge(100) by high-resolution electron-energy-loss spectroscopy", *Surf. Sci.*, **248**: 343-348 (1991).

[15] Y.J. Chabal, and S.B. Christman, "Evidence of dissociation of water on the Si(100)2 x 1 surface", *Phys. Rev. B*, **29**: 6974-6976 (1984).

[16] T. K. Carns, M. O. Tanner, and K. L. Wang, "Chemical etching of $Si_{1-x}Ge_x$ in $HF-H_2O_2-CH_3COOH$", *J. Electrochem. Soc.*, **142**, 1260 (1995).

[17] N. Mott, "Metal-insulator transitions", Taylor and Francis, 1990.

[18] S. Kanjanachuchai, J. M. Bonar, H. Ahmed, "Single-charge tunneling in n- and *p*-type strained silicon germanium on silicon-on-insulator", *Semicond. Sci. Technol.*, **14**: 1065-1068 (1999).

[19] I. M. Ruzin, V. Chandrasekhar, E. I. Levin, and L. I. Glazman, "Stochastic Coulomb blockade in a double-dot system", *Phys. Rev. B*, **45**, 13469-13478 (1992).

[20] R. A. Smith and H. Ahmed, "Gate controlled Coulomb blockade effects in the conduction of a silicon quantum wire", *J. Appl. Phys.*, **81**: 2699-2703 (1997).

[21] A. T. Tilke, F. C. Simmel, R. H. Blick, H. Lorenz, and J. P. Kotthaus, "Coulomb blockade in silicon nanostructures", *Progress in Quantum Electronics*, **25**: 97–138 (2001).

[22] S. K. Ghandhi, "VLSI fabrication principles : Silicon and Galium Arsenide", 2nd Ed., John Wiley & Sons, p. 478 (1994).

[23] L. P. Rokhinson, L. J. Guo, S. Y. Chou, and D. C. Tsui, "Double-dot charge transport in Si single-electron/hole transistors", *Appl Phys Lett.*, **76**: 1591-1593 (2000).

[24] M. K. Sanganeria, M. C. Öztürk, K. E. Violette, G. Harris, C. A. Lee, and D. M. Maher, "Low thermal budget *in situ* removal of oxygen and carbon on silicon for silicon epitaxy in an ultrahigh vacuum rapid thermal chemical vapor deposition reactor", *Appl. Phys. Lett.*, **66**: 1255-1257 (1995).

[25] K. Oda and Y. Kiyota, "H-2 cleaning of silicon wafers before low-temperature epitaxial growth by ultrahigh vacuum/chemical vapor deposition", *J. Electrochem. Soc.*, **143**: 2361 (1996).

[26] M. S. Carroll, J. C. Sturm, and M. Yang, "Low-temperature preparation of oxygen- and carbon-Free silicon and silicon-germanium surfaces for silicon and silicon-germanium epitaxial growth by rapid thermal chemical vapor deposition", *J. Electrochem. Soc.*, **147**: 4652-4659 (2000).

[27] M. S. Carroll, L. D. Lanzerotti, and J. C. Sturm, ""Quantitative measurement of reduction of boron diffusion by substitutional carbon incorporation", *Proc. Symp. Mat. Res. Soc.*, **527**:  417-422 (1998).

[28] K. Kung, Private communication.

[29] M. S. Carroll, "The interaction of silicon self-interstitials and substitutional carbon in silicon based heterostructures", Ph.D. thesis, Princeton University, June 2001.

[30] L, D. Lanzerotti, "Carbon in $Si_{1-x}Ge_x$ heterojunction bipolar transistors", Ph.D. thesis, Princeton University (1998).

[31] C. L. Chang, L.P. Rokhinson, J.C. Sturm, "Direct optical measurement of the valence band offset of p+ Si1-x-yGexCy /p- Si(100) by heterojunction internal photoemission", *Appl. Phys. Lett.*, **73**: 3568-3570 (1998).

# ELECTRICAL CHARACTERISTICS OF SiGe SINGLE-HOLE TRANSISTORS FABRICATED BY AFM LOCAL OXIDATION AND SILICON EPITAXIAL REGROWTH

## 6.1    Introduction

Since the first demonstration of single electron tunneling in an aluminum film in 1987 [1], quantum dot devices have been of great interest [2,3].  The advances of thin film growth techniques, such as molecular beam epitaxy (MBE) and electron-beam nanolithography make it possible to artificially define a small island with submicron size in semiconductors.  This small island, called a quantum dot (QD), may contain from 0 to several thousand charge carriers.  Three-dimensional confinement leads to a quantized QD energy spectrum.  QD applications such as a DC current standard turnstile [4], a high-resolution electrometer [5], a single-electron memory [6], and digital logic [7] have been demonstrated.  Recently, quantum dots have been proposed to work as a "q-bit" to achieve quantum computing [8].

Extensive studies on electrical characteristics of QDs have been performed on modulation doped GaAs/AlGaAs heterostructures.  However, the study of Si-based QD

devices is less common. Silicon continues to be the dominant material in the IC industry. Therefore, it is desired that new device concepts from quantum physics will enable new circuit design eventually to be realized in Si-based materials. Furthermore, silicon has strong spin effects ($g^* \mu_B B / \hbar \omega_c \sim 1/5$) and weak spin-orbital interactions ($\Delta_{SO} = 0.044 \text{ meV}$) relative to GaAs ($g^* \mu_B B / \hbar \omega_c \sim 1/50$ and $\Delta_{SO} = 0.33 \text{ meV}$)[9]. This leads to a longer spin coherence time in Si than GaAs[10,11], which is one of key parameters for using electron spin in QD's to achieve quantum computing.
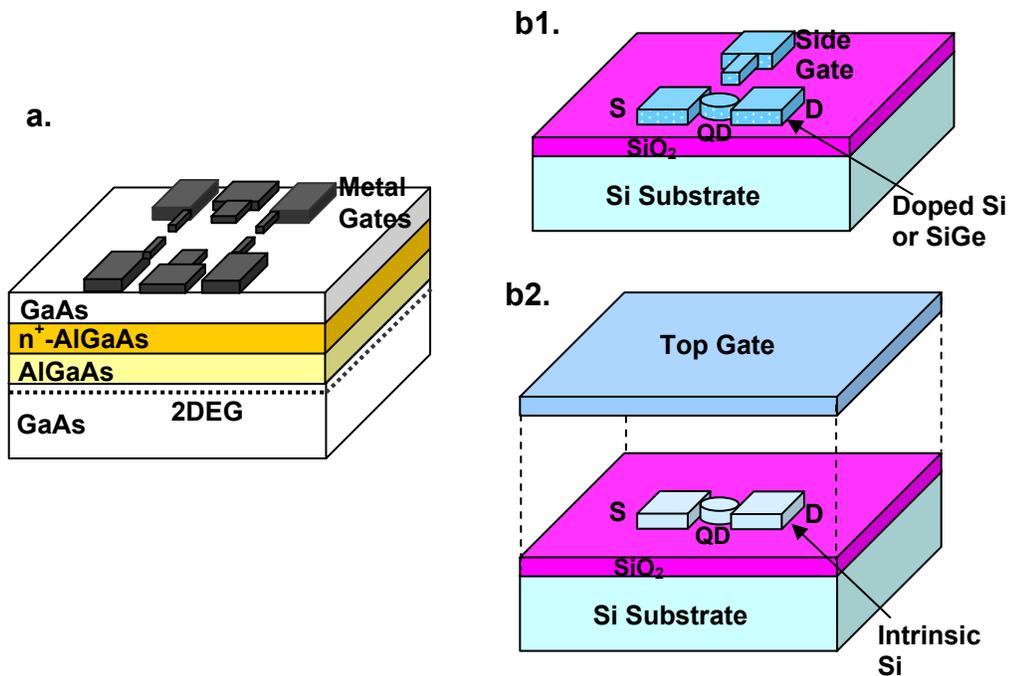


**Figure 6-1.** Two methods of defining QD: (a) surface depletion of 2-D gas by metal gates, and (b1) and (b2) trench isolation using patterned SOI films. In (b1), the conducting layer is doped Si or SiGe, but in (b2) the transport carriers are generated by the top gate, between which is insulator $SiO_2$.

There are two dominant methods used to define planar QDs. One is to use top metal gates to deplete an underlying two-dimensional electron/hole gas (2DEG or 2DHG), as shown in Fig. 6-1(a). Most quantum devices in GaAs-based materials are fabricated by this method. Single-hole transistors made from a 2DHG in modulation-

doped Si/SiGe heterojunctions have been demonstrated [12,13]. The confinement boundaries of QD defined by depletion potential are specular, and no defect states exist around the QD. However, the shape of depletion potentials along the z-direction from the top surface down to the 2D gas is parabolic. This indicates the real size of the QD in the 2D gas is different than the size defined by the top split gates.

A second QD definition method, trench isolation [Fig. 6-1(b1) & Fig. 6-1(b2)], can solve this problem. In this case, doped Si/SiGe thin films are patterned [Fig. 6-1(b1)], or undoped SOI are nanopatterned and a MOS gate on top creates a surface layer of carriers in the Si [Fig. 6-1(b2)]. The steep confinement wall is induced by removing the conducting layer and forming potential barriers between isolated regions. The demonstration of Coulomb blockade oscillations in silicon QDs at room temperature indicated that QDs less than 5 nm have been achieved by trench isolation [14]. This method has been widely adopted to fabricate Si-based QDs.

E-beam lithography and RIE have been widely used to achieve the trench isolation [15,16] with silicon on insulator (SOI). Etching the SOI forms small isolated Si structures. One kind of QD device was fabricated on heavily doped silicon on insulator, in which the transport carriers are from the doped $n^+$ or $p^+$ Si. In heavily-doped SOI, fabricated nanowires (without an intentionally patterned dot) of width ~ 60 nm exhibit Coulomb blockade oscillations as a function of gate voltage [15]. The oscillations are characteristics of QDs, not wires. It is believed the tunneling barriers formed in the nanowires are due to surface charging centers in native oxide and random fluctuations of dopants. The *I-V* characteristics, including oscillation peak position and amplitude in the QDs, are different at subsequent gate scans [17,18]. This is because the carriers in the devices tend to be trapped and detrapped at different sites. QDs in heavily doped $n^+$ and $p^+$ SiGe layers have been demonstrated in Ref. [19] and [20] with similar results.

Another kind of QD in Si has a MOSFET structure [16], as shown in Fig. 6-1(b2). Inversion layer carriers induced by the top gate voltage in SOI work as the conducting layer. QDs were defined by the method of trench isolation. In QD devices with MOSFET structure, the dopant impurity density is low (~$10^{15}$ cm$^{-3}$), and QDs exhibit reproducible *I-V* characteristics at relatively high temperature [16,21]. However,

undesirable conductance oscillations at very low temperature [21] were observed in the Si QDs passivated by amorphous $SiO_2$.  They are thought to be due to defect states at the $Si/SiO_2$ interface that lead to extra parasitic QDs, which interfere with the operation of the designed QD.

To avoid the interface states in Si-based QD devices, in this chapter, we will use silicon epitaxial regrowth to passivate patterned SiGe QDs.  To reduce surface damage and radiation from e-beam lithography and RIE, we use a low-energy nanopatterning technique of AFM local oxidation and wet etching to pattern the QD.  Reproducible Coulomb blockade oscillations have been observed at temperatures down to 0.3 K, which is attributed to the good interface between strained $Si_{0.7}Ge_{0.3}$ and regrown Si. This is the first demonstration of Si-based quantum devices with Si regrowth passivation.  To begin this chapter, the theoretical background of QD physics will be described.

## 6.2    Theoretical Background

Theoretical reviews on single charge tunneling can be found in references [2] and [3].  Here, we will describe the Coulomb blockade effects of QDs.

### 6.2.1   Coulomb Blockade Effect

In Fig. 5-9, we see a planar QD device, in which single charged particles can tunnel one by one from source to dot, and from dot to drain, with the modulation of gate voltage.  The addition of one charge particle into a QD would increase the Coulomb interaction of electrons in the QD, leading to a rise of electric energy of electrons in the QD by $\sim e^2/C_\Sigma$ (Fig. 6-2a), where $C_\Sigma$ is the total capacitance of the QD.  This additional energy between the energy levels $N$ and $N+1$ of the QD prevents new carriers
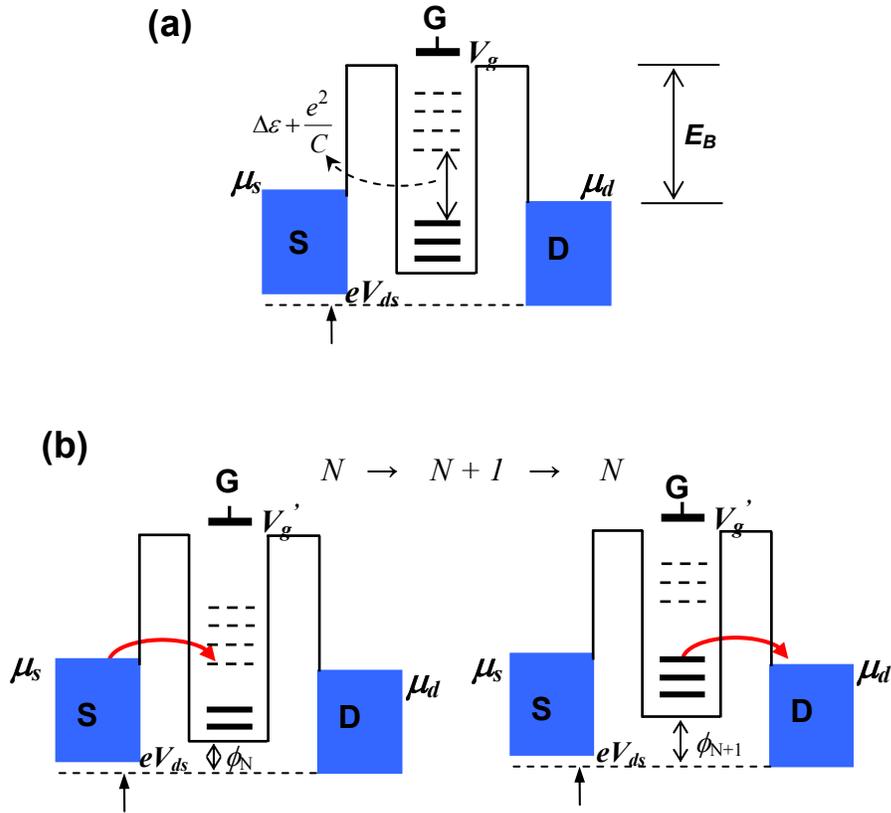
**Figure 6-2.** Energy diagram of a QD device, showing (a) Coulomb blockade and (b) single electron tunneling of $N \rightarrow N + 1 \rightarrow N$. The solid lines in QD represent the quantized energy levels that are occupied by electrons, and the dashed lines represent the energy levels that are empty. $\Delta\varepsilon$ represents the energy level splitting due to quantum confinement, and $\phi_N$ represents the electric potential of the dot with $N$ electrons on it. The states in the source and drain reservoirs are filled up to the electrochemical potentials $\mu_s$ and $\mu_d$ which are related via the external voltage $V_{ds} = (\mu_s - \mu_d)/e$. The gate voltage changes from $V_g$ in (a) to $V_g'$ in (b). The labeled $E_B$ is the electron tunneling barrier. (See Ref. [3])

from being able to move to the dot from the source and then to the drain.  This effect is
called Coulomb blockade, because no energy states of the QD are available for electron
to tunnel with energies between $\mu_s$ and $\mu_d$.  This current blockade can be removed by
applying a gate voltage to change the energy levels in the dot, until the first empty one
aligns parallel to the Fermi energy levels of the source and drain (Fig. 6-2b).  As the
gate voltage changes continuously, the number of charge particles in the QD will
change discretely due to single electron tunneling, and current oscillations will be
observed (Fig. 6-3).
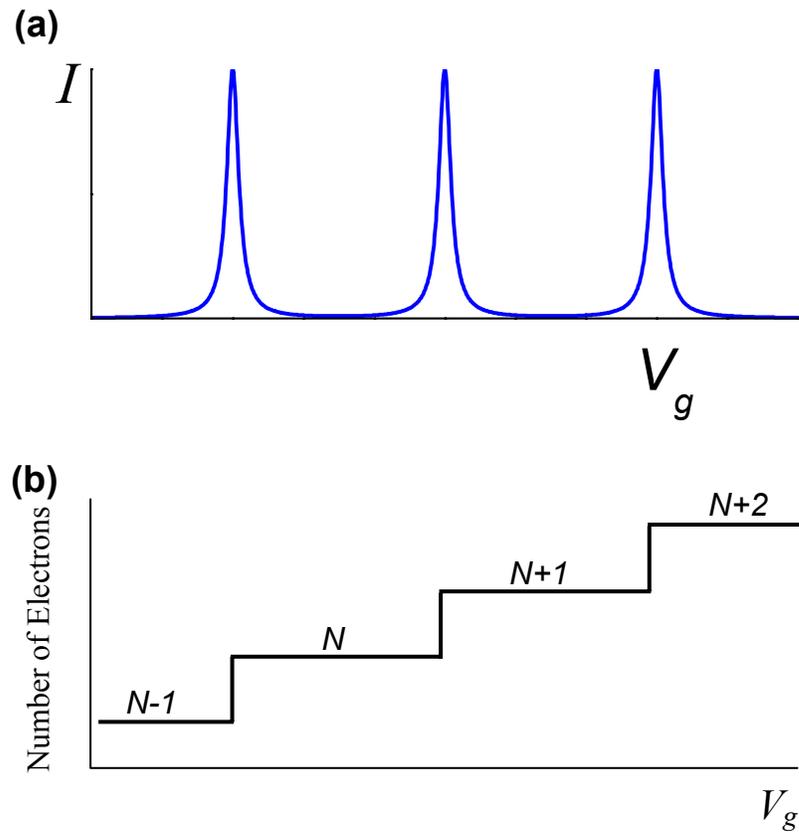


**Figure 6-3.** (a) Current oscillations and (b) electron number in QD as a function of
gate voltage.

To observe Coulomb blockade oscillations, two requirements must be satisfied. One is that the charging energy $e^2/C_\Sigma \gg k_B T$, otherwise the thermal distribution of electrons in the two leads will smear out the discrete tunneling of electrons.  The other requirement is that the tunnel barriers at the junctions of source-dot and dot-drain are high enough, so that the tunneling fluctuation is negligible.  The tunnel resistance $R_t$ must be much greater than $h/e^2 \sim 25.8$ KΩ.

### 6.2.2   Energies in a QD System

The electrochemical potential of the $N^{th}$ particle in a QD, $\mu(N)$, can be calculated by its definition,

$$\mu(N) \equiv E(N) - E(N-1),$$  (6.1)

where $E(N)$ is the total ground state energy for $N$ particles on the dot at zero temperature.  In principle, $E(N)$ can be obtained by solving the many-particle Schrödinger equation

$$\left[ \frac{-\hbar^2}{2m} \sum_i \nabla_i^2 + \sum_i V_i^2 + \frac{1}{2} \sum_{i,j} \frac{e^2}{|r_i - r_j|} \right] \Psi(r_1, r_2 \cdots, r_N) = E(N)\Psi(r_1, r_2 \cdots, r_N).$$

(6.2)

The calculations for above equation are difficult, though numerical solutions have been obtained for a system with a few electrons [22,23,24,25].

To simplify the problem, the constant interaction model has been made with the following assumptions: (1) Coulomb interactions of an electron on the dot with all other electrons in and outside the dot are parameterized by a constant capacitance, which is independent of the number of electrons on the dot; and (2) the discrete single-particle energy spectrum, calculated for non-interacting electrons, is unaffected by interactions. Therefore, the total ground state energy can be written as

$$E(N) = \sum_i \varepsilon_i + U(N),$$  (6.3)

where $\varepsilon_i$ is the single particle energy level due to energy quantization, and $U(N)$ is the electrostatic energy that includes both the Coulomb interaction of the charge inside the dot and the interaction energy between the dot and the electrodes.
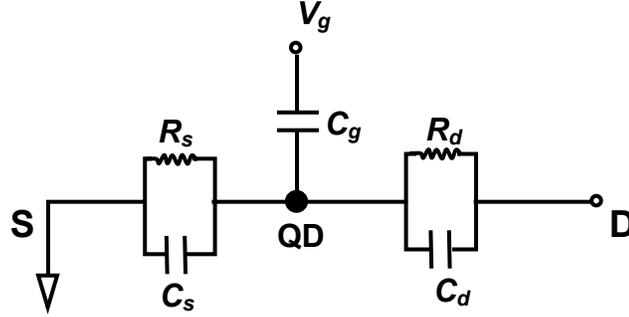


**Figure 6-4.**  Equivalent electrical circuit of a single-electron transistor.  The junctions of source-dot and dot-drain are made of tunnel resistors ($R_s$, $R_d$) and capacitors ($C_s$, $C_d$).  The dot is also connected to the gate through a capacitor $C_g$.

The equivalent electrical circuit of a single-electron transistor (Fig. 6-4) indicates the QD is capacitively coupled to the source, drain and gate.  Assuming the source is grounded, the excess charge $Q_0$ on the dot is related to the capacitances by [26]

$$Q_0 = C_\Sigma \phi - C_d V_{ds} - C_g V_g ,\qquad (6.4)$$

where $C_g$, $C_s$, $C_d$ are the capacitance between gate, source, and drain and the dot. $C_\Sigma = C_g + C_d + C_s$, and $\phi$ is the electrical potential of the QD.  The charge on the dot can only change by integer multiples of $e$, thus the electrostatic energy needed to bring $N$ electrons on to the initially neutral dot island is

$$U(N,V_{ds},V_g) = \int_0^{Ne} \phi(Q_0)dQ_0 = \frac{(Ne)^2}{2C_\Sigma} + \frac{Ne}{C_\Sigma}(C_d V_{ds} + C_g V_g).\qquad (6.5)$$

From Eq. (6.3) and Eq. (6.5),

$$\mu(N,V_{ds},V_g) \equiv E(N,V_{ds},V_g) - E(N-1,V_{ds},V_g)$$

$$= \varepsilon_N + (N - \frac{1}{2})\frac{e^2}{C_\Sigma} + \frac{C_d}{C_\Sigma}eV_{ds} + \frac{C_g}{C_\Sigma}eV_g .\qquad (6.6)$$

Here, $\mu(N)$ is the electrochemical potential of the $N^{th}$ electron added to the dot.  At a

fixed gate voltage, the number of electrons ($N$-$1$) on the dot is the largest integer for

which $\mu(N-1) < \mu_s \cong \mu_d$, where $\mu_s$ and $\mu_d$ are the electrochemical potentials of the

source and drain, respectively.  We assume a small source-drain voltage.

As shown in Fig. 6-2, when the electrochemical potential $\mu(N)$ is tuned to lie

between the source Fermi level $\mu_s$ and the drain Fermi level $\mu_d$, $i.e.,$

$$\mu(N,V_{ds},V_g) = \varepsilon_N + (N - \frac{1}{2})\frac{e^2}{C_\Sigma} + \frac{C_d}{C_\Sigma}eV_{ds} + \frac{C_g}{C_\Sigma}eV_g , \qquad (6.7)$$

$$= \mu_s \cong \mu_d$$

single-electron resonant tunneling will occur.  At a fixed gate voltage, when the number

of electrons is changed by one, the resulting change in electrochemical potential is:

$$\Delta\mu = \mu(N) - \mu(N-1) = (\varepsilon_N - \varepsilon_{N-1}) + \frac{e^2}{C_\Sigma} = \Delta\varepsilon + \frac{e^2}{C_\Sigma} , \qquad (6.8)$$

which is called the *addition energy*.  The *addition energy* is large for a small

capacitance and/or a large energy splitting $\Delta\varepsilon = \varepsilon_N - \varepsilon_{N-1}$ between 0-D dot states.  It

is important to note that the charging energy $e^2/C_\Sigma$ exists only between states at the

Fermi energy.  Below $\mu(N)$, the energy states are only separated by the single-particle

energy differences $\Delta\varepsilon$ [see Fig. 6-2(a)].  It is the $\Delta\mu$, the energy gap between the

highest occupied energy state of QD and the lowest unoccupied state, that results in the

Coulomb blockade effect of the QD.


### 6.2.3   Estimate of QD Energies

In this section, we estimate the addition energy in Eq. 6.8 for a quantum dot

based on its size.  We assume the shape of a QD is a flat thin disk with radius $r$.  If the

dot were isolated in space, its self capacitance would be

$$C = 8\varepsilon_r\varepsilon_0 r , \qquad (6.9)$$

This is the change in dot charge divided by the change in its potential, assuming a

boundary condition of zero potential at infinite distance from the dot.  Although in

devices the dot is not isolated and it has capacitances relative to gate, source and drain, in the limiting case, when the dot radius is small compared with the distance to the electrodes (source, drain and gate), its total capacitance ($C_\Sigma \equiv C_s + C_d + C_g$) can be estimated by the self-capacitance $C$ of an isolated dot. That is, $C_\Sigma \approx C = 8\varepsilon_r\varepsilon_0 r$ (Eq. 6.9).
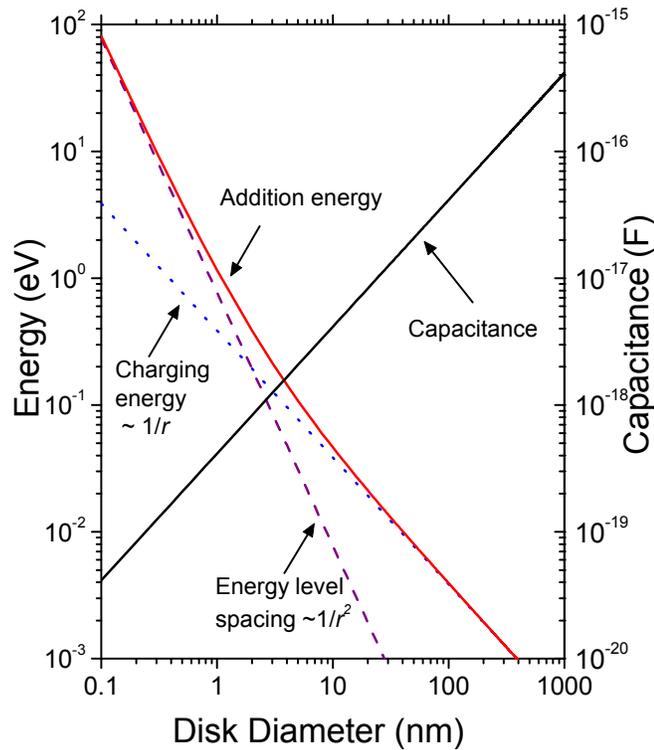


**Figure 6-5.** QD addition energy (solid-line) and its components: charging energy $e^2/C$ (dot-line) and energy level spacing $h/m^* r^2$ in QD (dash-line) vs. disk diameter. The dot is assumed to be a thin disk, with hole $m^* = 0.4m_0$. The QD self capacitance $C = 8\varepsilon_r\varepsilon_0 r$ as a function of disk diameter is also drawn.

The energy level spacing in a two-dimensional system is

$$\Delta\varepsilon = \hbar^2/m^* r^2 , \qquad\qquad\qquad (6.10)$$

when assuming the energy level spacing is a constant.  Here $m^*$ is the effective mass of the charge carriers.

For Si or SiGe, the hole effective mass is $\sim 0.4m_0$.  With these assumptions, Figure 6-5 shows how the energies, including addition energy, charging energy and energy spacing, change as a function of dot size.  The dot capacitance increases with dot size.  For dot sizes over 2 nm, as in our work, the energy spacing $\Delta\varepsilon$ is less than charging energy $e^2/C$, and charging energy dominates the addition energy $\Delta\mu$.  For $r \approx 50$ nm, typical of our work, $\Delta\mu \approx 4.1\,\text{meV}$.

### 6.2.4   Period of Coulomb Blockade Oscillations

In Eq. (6.7), we can see that both gate voltage $V_g$ and drain-source bias $V_{ds}$ can tune the electrochemical potential $\mu(N)$ of the QD.  Define

$$\alpha \equiv \frac{\Delta\mu_{dot}}{e\Delta V_g} = \frac{C_g}{C_\Sigma}, \quad \beta \equiv \frac{\Delta\mu_{dot}}{e\Delta V_{ds}} = \frac{C_{ds}}{C_\Sigma}. \tag{6.11}$$

The Coulomb blockade of the QD can be removed by applying a voltage to the gate or drain so that the dot electrochemical potential matches that of the source and drain $\mu(N) = \mu_s \cong \mu_d$.  With a continuous change in gate voltage and a fixed source-drain bias, the current through the QD oscillates.  From $\mu(N-1, V_{ds}, V_g^{(N-1)}) = \mu(N, V_{ds}, V_g^{(N)}) = \mu_s \approx \mu_d$, the oscillation distance in gate voltage between conductance peaks can be solved as

$$\Delta V_g = V_g^{(N)} - V_g^{(N-1)}$$

$$= \frac{C_\Sigma}{C_g}\left(\frac{\Delta\varepsilon}{e} + \frac{e}{C_\Sigma}\right) = \frac{\Delta\varepsilon}{\alpha e} + \frac{e}{C_g}, \tag{6.12}$$

where $V_g^N$ and $V_g^{N-1}$ are the gate voltages at which single-electron tunneling occurs.

When the charging energy is much greater than energy level splitting, *i.e.*, $e^2/C_\Sigma \gg \Delta\varepsilon_N$, which is the case for most Si-based QD devices (see Fig. 6-5), the classical capacitance-voltage relation for a single electron charge $\Delta V_g = e/C_g$ is

obtained and the oscillations are periodic. On the other hand, if $\Delta\varepsilon \sim e^2/C_\Sigma$, which requires dot size $r < 10$ nm in a Si-based QD device (Fig. 6-5), the oscillations will deviate from this periodicity due to the irregular energy spectrum of the QD [23].

For large dots dominated by charging energy, spin has little effect on the period of conductance peaks. For a small dot, however, spin-degenerate splitting should give rise to two kinds of spacings. One spacing is $e/C_g$, corresponding to electrons $N$ and $N+1$ having opposite spin and being in the same spin-degenerate 0-D state. The next spacing would be $e/C_g + \Delta\varepsilon/\alpha e$, corresponding to electrons $N+1$ and $N+2$ being in different 0-D states.

### 6.2.5   Lineshape of Coulomb Blockade Oscillations

Three kinds of lineshape of Coulomb blockade oscillations can be found, depending on the temperature and the height of the tunnel barriers [3].

Define $R_s$ and $R_d$ as the tunneling resistance from source to dot and that from drain to dot. When the tunneling barriers in a QD cannot satisfy $R_s, R_d \gg h/e^2$, which means there is strong coupling between energy states in the QD and those in two leads (source & drain), the quantum fluctuation in the charge of the dot cannot be ignored. The quantum mechanical broadening of the 0-D energy states $h\Gamma$ is comparable to thermal energy $k_B T$. High-order tunneling via virtual intermediate states in addition to the first-order tunneling must be taken into account. The lineshape of the tunneling conductance is Lorentzian, which can be written as

$$G \sim \frac{(h\Gamma)^2}{(h\Gamma)^2 + \delta^2}, \qquad \text{(for } h\Gamma \sim k_B T \text{)}, \qquad (6.13)$$

where $\delta = \dfrac{C_g}{C_\Sigma} e \cdot |V_g^{peak} - V_g| = \alpha e \cdot |V_g^{peak} - V_g|$, where $V_g^{peak}$ is defined the gate voltage at the position of the conductance peak.

When the temperature is greater than both the broadening of the 0-D energy states $h\Gamma \ll k_B T$ (i.e. $R_s, R_d \gg h/e^2$) and the energy level splitting in the QD but not

greater than the charging energy $\Delta\varepsilon << k_BT << e^2/C_\Sigma$, tunneling will occur through

multiple energy levels due to the thermal fluctuation. This is in so-called *classical*

*Coulomb blockade* regime. The lineshape of the conductance is

$$G \sim \frac{\delta/k_BT}{2\sinh(\delta/k_BT)} \sim \cosh^{-2}\left(\frac{\delta}{2.5k_BT}\right), \qquad (\text{for } h\Gamma, \Delta\varepsilon << k_BT << e^2/C_\Sigma).$$

$$(6.14)$$

When the temperature is greater than the broadening of the 0-D states

$h\Gamma << k_BT$ (i.e. $R_s, R_d >> h/e^2$), but less than the energy level splitting of the QD,

$k_BT << \Delta\varepsilon, e^2/C_\Sigma$, tunneling will occur through a single energy level. In this *quantum*

*Coulomb blockade regime*, the tunnel current through the quantum dot can be expressed

as [27,28]

$$I_D = \frac{e}{h}\int \Gamma(E)D(E)\left[f(E-E_F^{(s)})-f(E-E_F^{(d)})\right]dE , \qquad (6.15)$$

where $f(E-E_F)$ is the Fermi-Dirac distribution function, $\Gamma(E)$ is the energy dependent

tunneling rate which in general depends on $V_{ds}$ and $V_g$, and $D(E)$ is the density of states

inside the dot. Since tunneling is only through the $N^{th}$ energy level, we can approximate

$D(E) = \delta(E - \mu_N)$, where $\mu_N \equiv \mu(N)$. At a finite temperature $T$ and vanishing drain

bias ($V_{ds} \rightarrow 0$), the linear conductance can be calculated:

$$G_D = \frac{e}{h}\Gamma(\mu_N)f'[(E-\mu_N)/k_BT] = \frac{1}{4k_BT}\frac{e^2}{h}\Gamma(\mu_N)\text{sech}^2\left(\frac{\alpha[V_G-V_G^{(N)}]}{2k_BT}\right),$$

$$(\text{for } h\Gamma << k_BT << \Delta\varepsilon, e^2/C_\Sigma). \qquad (6.16)$$

$f'(E/k_BT)$ is the derivative of Fermi-Dirac function. A thermally broadened peak can

be shown to have a full width at half maximum (FWHM) (for $V_g$) $3.5k_BT/\alpha$, and a

height $\propto 1/T$. From the peak width, the capacitance ratio $C_g/C_\Sigma$ (known as $\alpha$ in Eq.

6.11) can be found if the electron temperature in the device is known. In one of our

devices, we expect dot radius $r \sim 20$ nm, so $C_\Sigma \approx 16.6$ aF, $\frac{e^2}{C_\Sigma} \approx 9.7$ meV, and

$\Delta\varepsilon \approx 0.48\,\text{meV}$. So the measurement temperature must be less than 5 K (corresponding $\sim\Delta\varepsilon$) for the observation of quantum Coulomb blockade oscillations in the QD.

### 6.2.6 Conductance Dependence on Drain Voltage

The conductance of a QD device is also dependent on the drain-source voltage. The contour plot of conductance *vs.* drain-source voltage and gate voltage is schematically shown in Fig. 6-6(c). The diamond-shaped Coulomb blockade region with zero conductance can be explained by the band diagram of Fig. 6-6(a) at very small source-drain voltages, and by that of Fig. 6-6(b) at relatively high drain-source biases. Conductance peaks at the bias voltages close to the zero correspond to the tunneling of a single charge from the source through the dot to the drain when an empty energy level in the QD is parallel to the source and drain Fermi energies (Fig. 6-2). At a moderate bias voltage, the conductance peak $O$ splits into $S$ and $D$ (Fig. 6-6a & c), where the energy level $O$ moves up to $\mu_s$ or down to $\mu_d$ respectively with gate voltages. The movements due to drain voltage and gate voltage are $\Delta V_{sd} \cdot \dfrac{C_d}{C_\Sigma} = -\Delta V_g \cdot \dfrac{C_g}{C_\Sigma}$ and

$\Delta V_{sd} \cdot \left(1 - \dfrac{C_d}{C_\Sigma}\right) = \Delta V_g \cdot \dfrac{C_g}{C_\Sigma}$. Thus the slopes of the diamond boundaries are

$$\frac{\Delta V_{sd}}{\Delta V_g} = -\frac{C_g}{C_d} \text{ or } \frac{\Delta V_{sd}}{\Delta V_g} = \frac{C_g}{C_\Sigma - C_d}, \tag{6.17}$$

which are labeled in Fig. 6-6 (c). When the source-drain bias is increased further to the point $\Delta V_{sd}$ equal to the *addition energy* $\Delta\varepsilon + e^2/C_\Sigma$, the electrons can always find empty energy levels in the QD for carrier tunneling at any gate voltages, and thus the Coulomb blockade is lost (Fig. 6-6b). Fig. 6-16(c) indicates that the dot characteristic parameters, such as *addition energy* $\Delta\varepsilon + e^2/C_\Sigma$, capacitances ($C_g, C_s, C_d$) and oscillation period $\Delta V_g$, can be obtained from the "diamond".
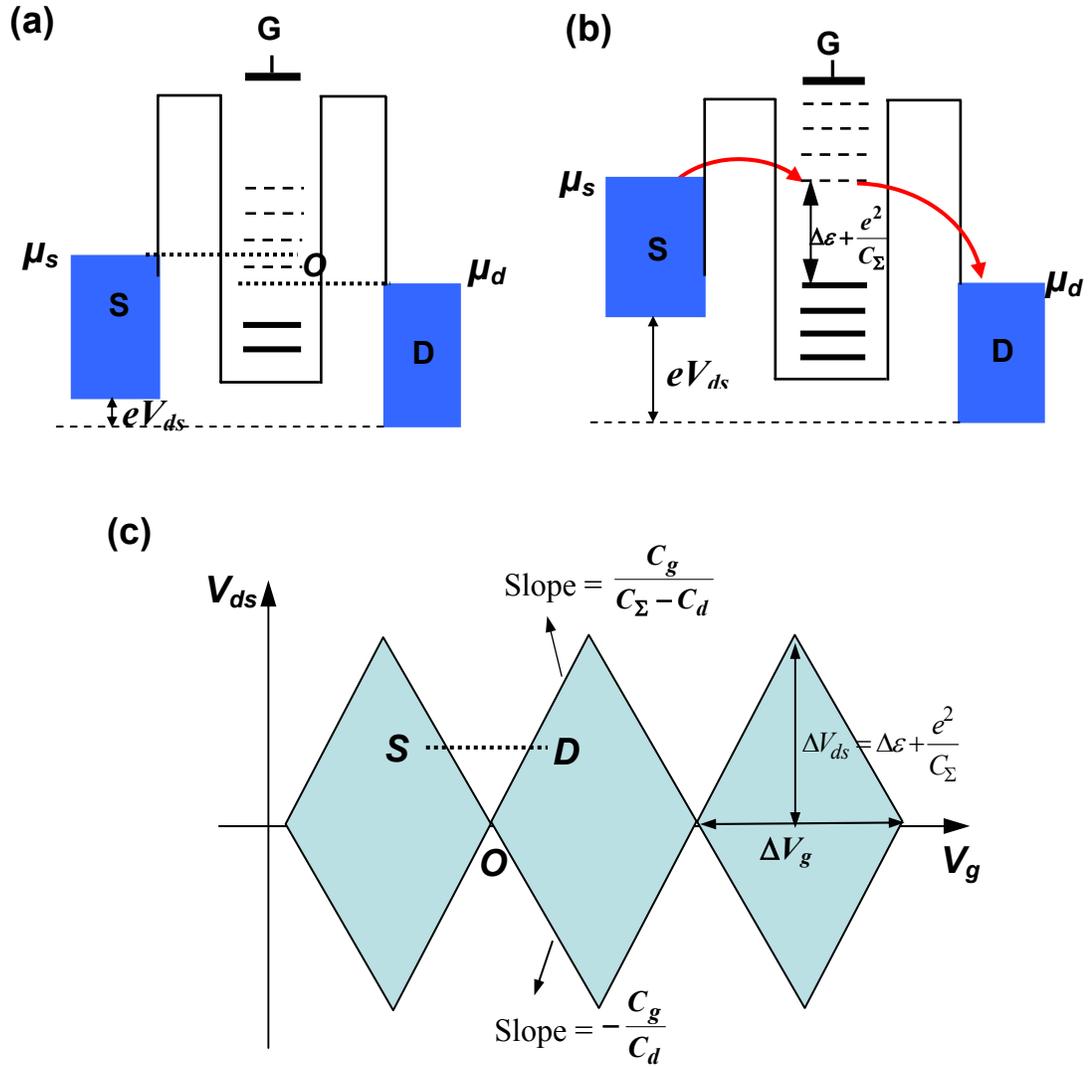
**Figure 6-6.** Energy diagram to explain the diamond-shaped Coulomb blockade oscillations (a) at small drain-source bias and (b) at higher source-drain bias at which the Coulomb blockade region is lost, independent of gate voltages.  In (c), dot parameters extracted from the diamond are marked.

## 6.3    Device Fabrication Process

SiGe quantum dot devices have been fabricated by the AFM nanopatterning technique described in chapter 5 (see Fig. 5-6).  The SiGe and Si epi-layers were grown by RTCVD on an n-type Si substrate (Fig. 6-7).  The atomic concentration of Ge in SiGe layer is ~ 30%, which results in ~ 230 meV valence band offset relative to Si [29]. The doping level in the SiGe was estimated at $6 \times 10^{18}$ cm$^{-3}$. The carrier density in p$^+$-Si$_{0.7}$Ge$_{0.3}$ was ~ $3 \times 10^{12}$ cm$^{-2}$ as obtained by a Hall measurement at $T = 4.2$ K.  The intrinsic Si$_{0.7}$Ge$_{0.3}$ layers adjacent to the doped p$^+$- Si$_{0.7}$Ge$_{0.3}$ were designed to contain any boron dopant diffusion in SiGe during growth.  As the temperature goes below 50 K, the only conducting layer is p$^+$-Si$_{0.7}$Ge$_{0.3}$, and carriers in the other layers freeze out.
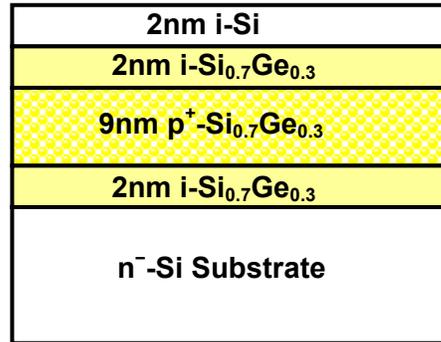


**Figure 6-7.**  Layer structure of sample #3386.

A Hall-bar structure was first patterned down to the Si substrate ~ 200 nm from the surface by optical lithography and RIE.  After the sample surface had been rinsed with solvents and dipped in diluted HF, AFM local oxidation was performed on the 2-nm-thick Si cap to define a quantum dot pattern by the oxidation lines (Fig. 6-8a).  The pattern was transferred into the Si$_{0.7}$Ge$_{0.3}$ layers by two-step selective wet etching (Fig.

6-8b).  The etching rate of SiGe is ~ 1.2 nm/s, so the undercut of the 10-sec wet etching
is estimate to be ~ 12 nm. This isotropic wet etching reduced the dot size further.
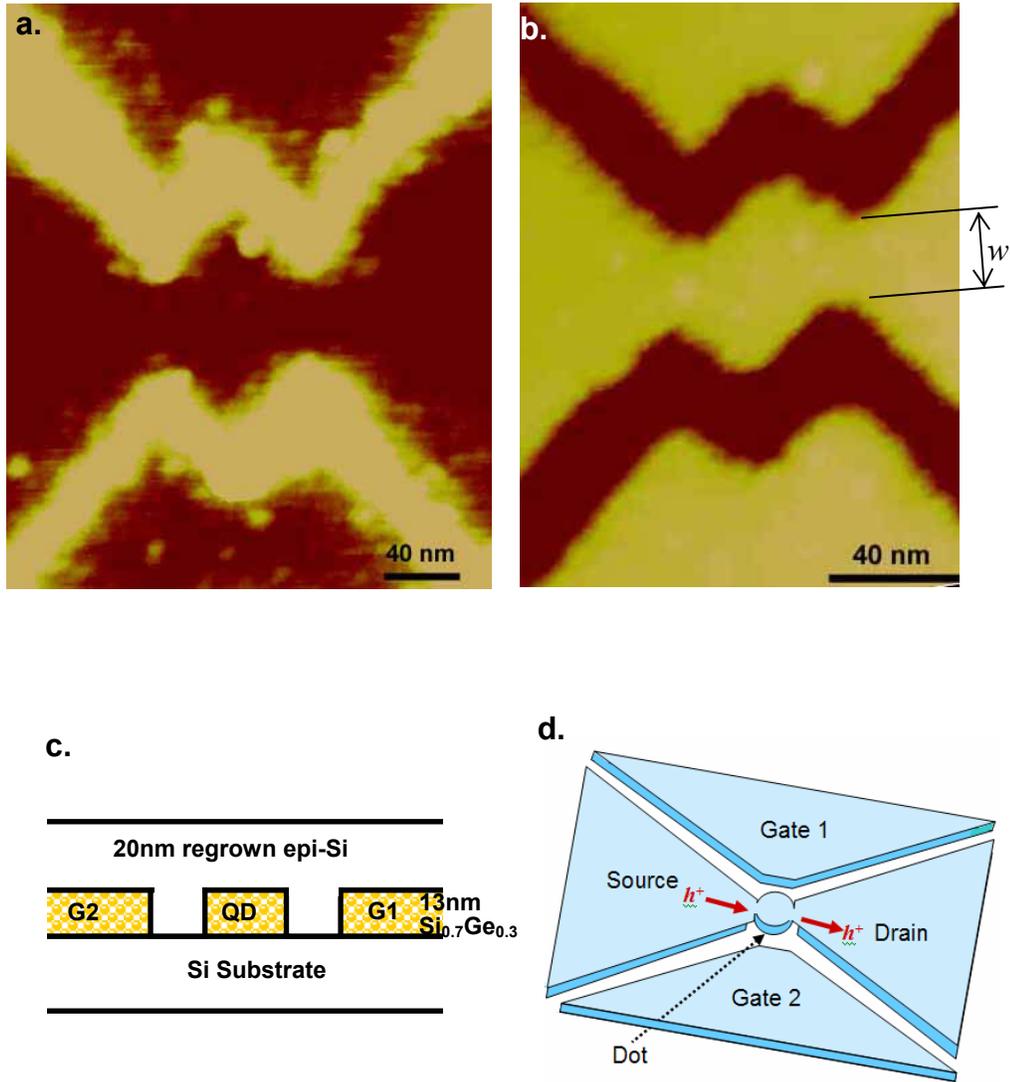


**Figure 6-8.** (a) AFM images of quantum dot device after AFM oxidation of the top
thin Si cap, and (b) after two-step selective wet etching.  The gap distance at the
narrow region is marked by *w*. (c) Cross-section of the QD device after epitaxial
regrowth. (d) Schematic diagram of a QD and the path of hole transport in the device.

During the QD fabrication process, the key control parameter is the gap distance *w* at the narrow junctions of the source-dot and the drain-dot. As mentioned above, in order to see the quantized nature of charge particles in a single-charge transistor, the potential barriers formed at the junctions of the source-dot and the drain-dot must be high enough to prevent the fluctuation of electron number in the QD. The potential barriers at the junctions may be caused by the lateral quantum confinement due to the small gap distance at the junctions, or/and the depletion from the two planar gate voltages. In our quantum dot configuration, we will show later that the potential barriers are primarily due to quantum confinement.

If the gap distance *w* is too large, the potential barrier will be too low or lost altogether. However, if *w* is too close to zero, the conductance of the QD arising from single-charge tunneling is totally shut off. The real gap distance is less than the *w* observed from the top Si-cap by AFM imaging due to the undercut from isotropic wet etching. During our experiment, we found that when *w* was in the range ~ 25-40 nm (observed from the top AFM image after wet etching), the requirement for the potential barriers could be met. Given that undercutting occurs, the actual width is on the order of 5−10 nm. Otherwise, either no Coulomb blockade of the conductance was observed (when *w* was too large), or the conductance was always zero (when *w* was too small), no matter how much gate voltage was applied, up to the point when the gate starts to leak. In the former case, the gate voltage had almost no effect on the current and could not "pinch it off".

After the QD was patterned, silicon epitaxial regrowth was done in our RTCVD reactor to cover the whole device and passivate the patterned surface. Following the procedure developed in Chapter 5, we first cleaned sample surface by "piranha" cleaning and HF dip. In-situ hydrogen baking at $T \sim 800$ °C was performed to remove the impurities on sample surface before the silicon regrowth at the temperature of ~ 700 °C for 20 min. The intended thickness of Si regrowth is ~ 50 nm. Schematic diagrams of cross-section and top-view of the QD device with the passivation of silicon epitaxial regrowth is shown in Fig. 6-8 (c) and (d). At a certain gate voltage, single-hole

tunneling can be observed with the path from the source through the narrow junction to
the dot, and then through another narrow junction to the drain.

Ohmic metal contacts for electrical measurements were achieved by 300-nm-
thick aluminum evaporation, lift-off, and forming gas anneal at $T = 450\ °C$. QD device
with
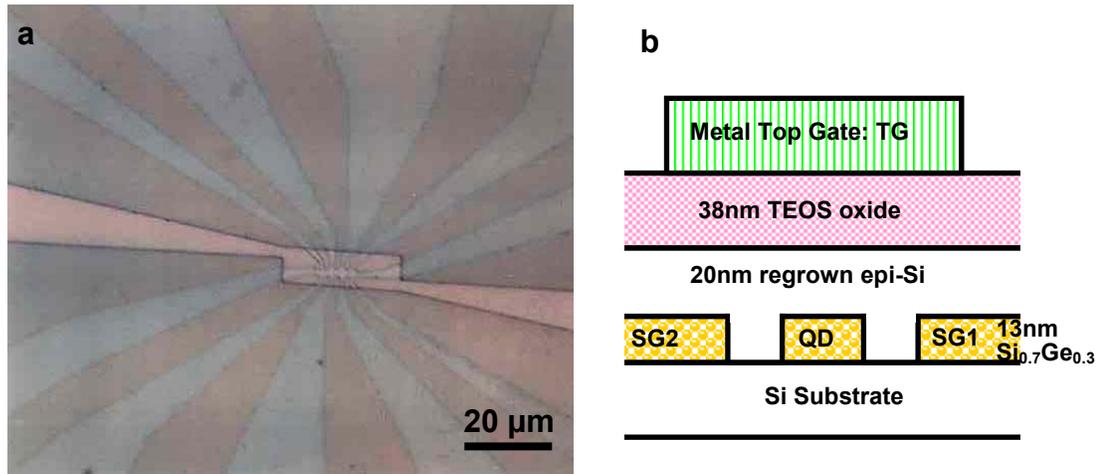


**Figure 6-9.** (a) Photograph of the Hall-bar and the top gate; (b) cross-section of a QD
with the top gate.

In several of our samples, the top gate was added to the fabricated QD (Fig. 6-
9). Tetraethylorthosilicate (TEOS) oxide was deposited on the regrown Si layer at $T = $
575 °C and pressure of 600 mtorr in a LPCVD chamber. The oxide thickness is ~ 38
nm. Two steps of aluminum evaporation were subsequently made. The first one is for
ohmic contacts. After optical lithography, the TEOS oxide in the contact pads was
removed by dilute HF etching before Al evaporation, followed by a forming gas anneal.
A second Al evaporation was then done in some sample to create a top gate, in a region
without prior oxide etching and post forming gas anneal. In both cases, the aluminum
was patterned by lift-off.

## 6.4  Calculations of Tunnel Barriers and Capacitances of the Fabricated QDs

In a planar quantum dot device, the minimum feature is at the source-dot and drain-dot junctions, where tunnel barriers are formed due to lateral confinement and/or the gate voltage.  The electrical potential profile from source to drain through the dot has been schematically shown in Fig. 6-2.  The potential barriers ($E_B$ in Fig. 6-2) at the narrow region of our designed device structure will be calculated analytically and simulated by Medici, a 2-D device simulator.

In the constant interaction model of Sec. 6.2.2, we parameterize the Coulomb interactions among electrons in the dot and between electrons in the dots and those in the coupled leads by the capacitances $C_s$, $C_d$ and $C_g$, as described by Eq. 6.11.  The following 2-D Medici simulation will also supply the values of those capacitances as a function of the gate voltages.

### 6.4.1  Tunnel Barriers at Narrow Regions

*Lateral Quantum Confinement*

At the narrow regions of our QD device (see Fig. 6-8), quantum wells for holes are formed laterally due to the valence band offset $\Delta E_v$ between central $p^+$-$Si_{0.7}Ge_{0.3}$ layer and the regrown Si on either side of it.  There is also quantum confinement in the vertical direction throughout the structure.  We will ignore that here, and focus only on the confinement in the lateral direction, which is the maximum at the narrow gaps.  Assume the quantum well is abrupt.  The well height and width are equal to the valence band offset $\Delta E_v$ ($\sim$ 230 meV) and the gap distance $w$ at narrow regions, respectively (Fig. 6-10).  The energy levels in the quantum well are quantized, and thus the edge of the $Si_{0.7}Ge_{0.3}$ valence band gives rise to $E_1$, forming the potential barriers at the source-dot and the drain-dot junctions.
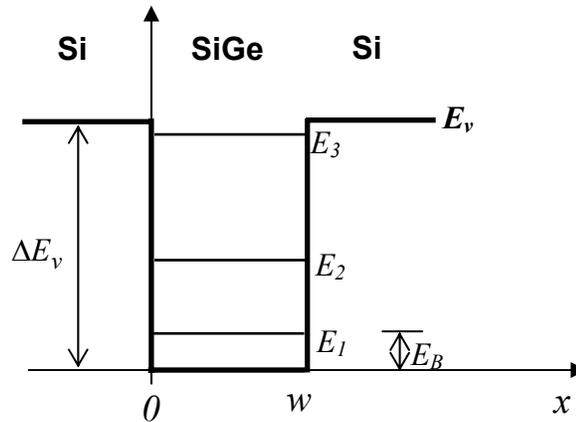
**Figure 6-10.** A quantum well with height of $\Delta E_v$ and width of $w$.  Energies $E_1$, $E_2$
and $E_3$ are quantized energy levels in the well.  The energy barrier $E_B$ is the distance
between the $E_1$ level and the valence band edge in the SiGe.  Note the energy scale for
holes has been inverted in this figure.
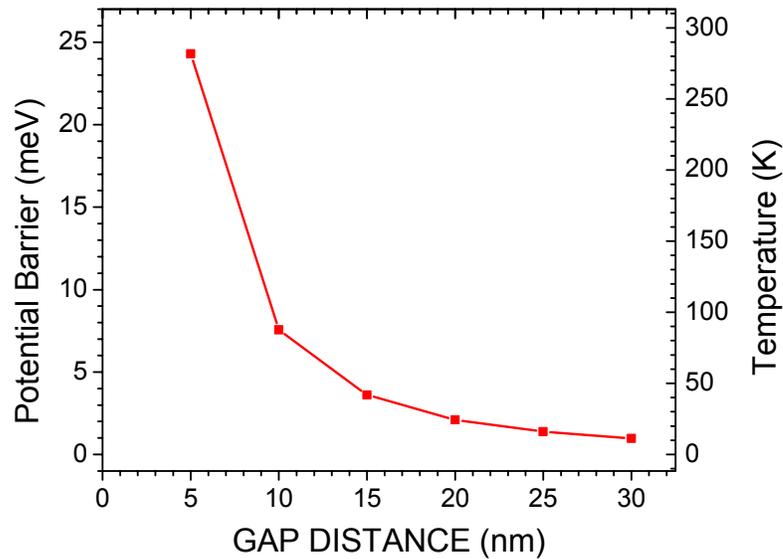


**Figure 6-11.** Potential energy barriers as a function of gap distance at the narrow
regions.

Solving the Schrödinger equations, we can obtain the wave functions for the three regions:

$$\psi_1 = A_1 e^{k_1 x} \qquad\qquad k_1 = \frac{1}{\hbar}\sqrt{2m^*(\Delta E_v - E)}$$

$$\psi_2 = A_2 e^{ik_2 x} + B_2 e^{-ik_2 x} \qquad k_2 = \frac{1}{\hbar}\sqrt{2m^* E} \qquad . \qquad (6.18)$$

$$\psi_3 = B_3 e^{-k_1 x}$$

From the boundary conditions, the quantized energy levels $E$ can be solved from the equation:

$$\frac{2\sqrt{E(\Delta E_v - E)}}{2E - \Delta E_v} = \tan\left(\frac{w\sqrt{2m^* E}}{\hbar}\right). \qquad (6.19)$$

The equation has been solved with varying the gap distance $w$. The first solution $E_1$ is the potential barrier, shown in Fig. 6-11 as a function of $w$. From the fabrication (Sec. 6.3), we estimate the $w$ to be in the range of 5-20 nm. When $w = 10$ nm, the potential barrier is $\sim 7.6$ meV, corresponding to a thermal energy $T = 55$ K. If the gap were 20 nm, the barriers would be $\sim 2.1$ meV.

*Barriers Induced by Gate Voltages*

The tunnel barrier at the narrow regions may also be introduced by two planar gate voltages. This can be simulated by the Medici program from Synopsys® [30]. Using Medici, we can define the device structure in two dimensions, including materials, geometry scales and boundary conditions. By numerically solving Poisson's equation and the continuity equation, Medici provides electrical characteristics of the device, such as potential distributions, output $I$-$V$ curves, and energy band diagrams.
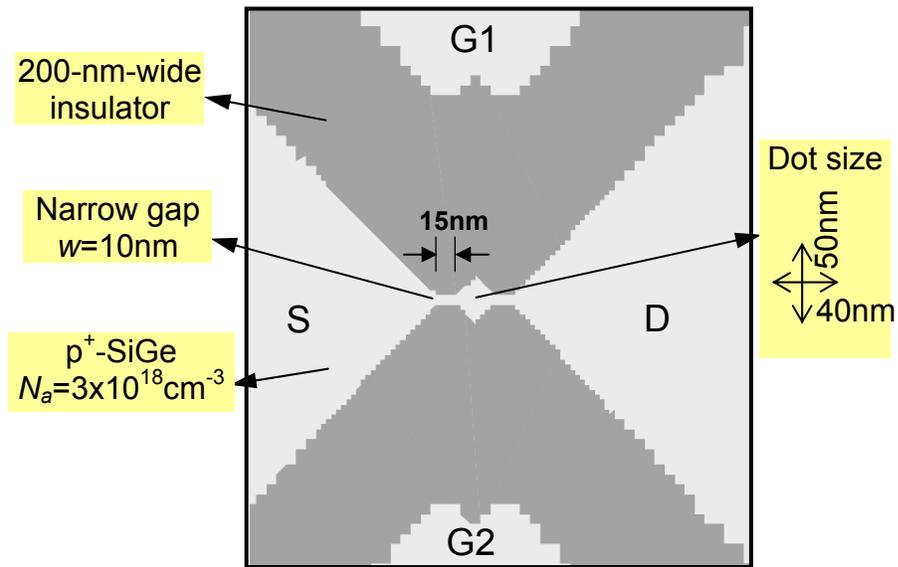
**Figure 6-12.** Top-view of device structure for Medici simulations.
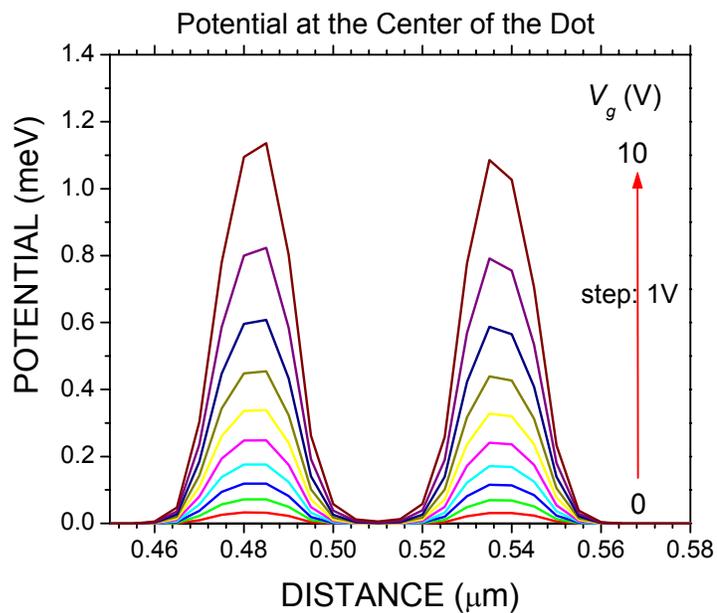


**Figure 6-13.** Potential profile along the device center line from source to drain for different voltages applied to the two planar gates.
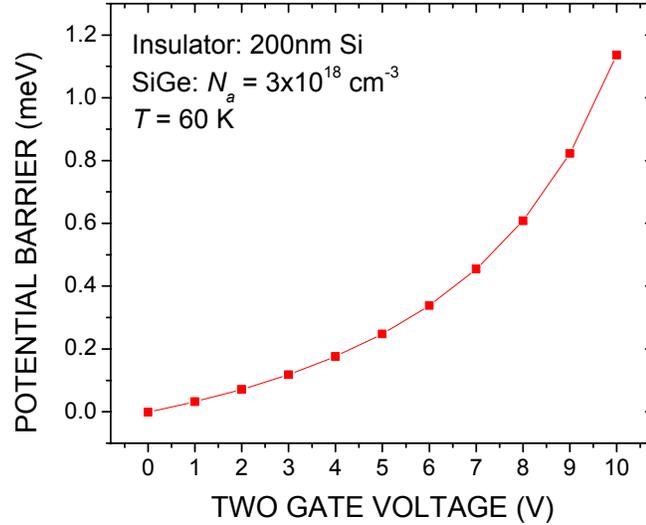
**Figure 6-14.**  Medici simulation results of the potential energy barriers at the 10-nm-
wide gap due to applied-planar gate voltages.  The same voltage is assumed on each of
the two gates.

Using Medici, we first define the device structure according to the fabricated
QD device with an etching line-width ~ 200 nm.  Figure 6-12 is the top-view of the
center part of the QD device to be simulated, in which the gray regions are 200-nm-
thick silicon insulator lines, and white regions are $p^+$-$Si_{0.7}Ge_{0.3}$ with boron doping
concentration $3\times10^{18}$ cm$^{-3}$.  The dot size is defined as ~ 40nm × 50 nm, and the gap
distance $w$ at the narrow regions ~ 10 nm.  During simulation, the source ($S$) and the
drain ($D$) are grounded, and voltages applied to the two planar gates $G1$ and $G2$ are
from 0 V to +10 V.  The lattice temperature is set at 60 K.[†]  Quantum effects, such as
that calculated in the previous section, are ignored.  The simulation file is attached in
Appendix C.  The potential distribution along a horizontal line crossing the center of the
narrow gap is plotted at each gate voltage (Fig. 6-13).   In Fig. 6-14, the potential

[†] Lattice temperatures less than 60 K may result in a divergence of the simulation in Medici.

barriers increase with the gate voltages, but the maximum barrier at the gate voltages $V_g \leq 10\,\mathrm{V}$ is ~ 1.1 meV. This is much less than the barriers arising from the quantum confinement as just calculated in the previous section (10-nm-gap $\rightarrow$ 7.6 meV). Although applying higher voltages to the two planar gates would contribute to higher potential barriers in the simulation, it is not practical, since leakage current cannot be ignored when gate voltages $V_g$ are larger in magnitude than 2.5 V (see Fig. 5-20). The Medici simulation is a 2-D (not 3-D) simulation, and assumes structures of infinite thickness. More detailed 3-D simulation in a few cases showed similar results [31].

In summary, simulation shows that the tunnel barriers for our QD structure are mainly due to the lateral confinement rather than the planar gate voltages. Barriers from 2.1 meV to 7.6 meV may be expected for a gap of 10−20 nm.

### 6.4.2 Capacitance in the QD device

To see Coulomb blockade oscillations, one of the requirements is $e^2/C_\Sigma \gg k_B T$, where $C_\Sigma = C_g + C_s + C_d$, the total capacitance of the dot

Medici simulation can provide values of the capacitances: $C_s$, $C_d$, $C_g$. From the previous section, we know that the potential barriers for carrier tunneling are formed due to lateral confinement instead of planar gate voltages. For capacitance simulation by Medici, narrow gap distance $w$ was set to zero to generate barriers. Similar device structure was used as shown in Fig. 6-12 except $w$ was equal to zero. A small AC voltage $[\tilde{v} = 1.0\sin(2\pi f t)\ \mathrm{mV}]$ was intentionally applied to the dot with a frequency $f =$ 1 kHz. The AC current flowing from the dot to each electrode can be obtained from the Medici simulation. Thus,

$$C_j = \frac{i_j}{2\pi f \tilde{v}},\qquad (6.20)$$

where the subscript $j$ denotes $s$ (source), $d$ (drain), and $g$ (gate), and $i$ is the magnitude of the out-phase current.

Capacitances as a function of the two planar gate voltages are shown in Fig. 6-15.  All the capacitances change slightly with the gate voltage.  The capacitances between source and drain are equal, and both decrease slightly with gate voltage.  They are much greater than the two gate capacitances.  The ratio $\dfrac{C_s}{C_g} = \dfrac{C_s}{C_{g1} + C_{g2}} \approx 7$.

Because a 2-D simulator was used, its calculates a capacitance per unit thickness of the structure.  We assume a thickness of 10 nm, which is the doped SiGe layer thickness.  Note fringing fields would probably lead to larger capacitances in practice, for $C_s$, $C_d$, $C_{g1}$, and $C_{g2}$, than those from calculations here.
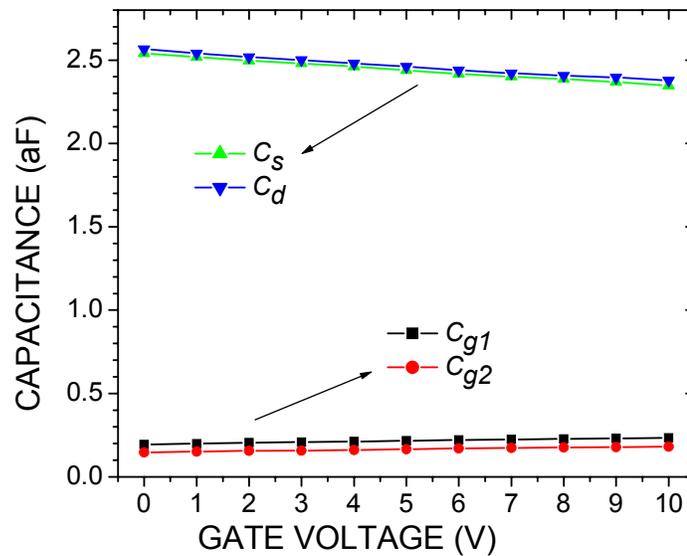


**Figure 6-15.**  Capacitances of source-dot ($C_s$), drain-dot ($C_d$), gate1-dot ($C_{g1}$) and gate2-dot ($C_{g2}$) as the function of gate voltage.  They slightly change with gate voltage.

## 6.5     Electrical Characteristics of SiGe QD Devices


### 6.5.1     Quantum Dot Device without Top Gate


*General Characteristics and Reproducibility*

Typical Coulomb blockade (CB) conductance oscillations *vs.* the two planar gate voltages (held equal) are shown in Fig. 6-16(a).  The temperature $T = 0.3$ K and source-drain bias $V_{ds} = 100$ μV.  The measurements were made in the lab of Prof. Daniel Tsui. The conductance peaks are extremely narrow with FWHM ~ 12 mV.  The slightly broader peak at $V_g \sim 0.67$ V is due to the increased leakage of the planar gates. Although it is difficult to precisely resolve the difference, the oscillation peaks appear to be better fit by $G \propto \cosh^{-2}[\alpha(V_g - V_g{}^{peak})e/2k_BT]$ instead of a Lorentzian function (Fig. 6-16b), where $V_g{}^{peak}$ is the gate voltage at which conductance peak appears.  As described in Sec. 6.2.5, this indicates the potential barriers formed at the narrow regions are high enough to guarantee the weak coupling between the dot and the source/drain leads ($\hbar\Gamma << k_BT << \Delta\varepsilon, e^2/C$) (see Eq. 6.16).  Thus the tunneling resistance $R_t = \frac{1}{T}\frac{h}{e^2} >> \frac{h}{e^2}$, where $T$ is the transmission probability of charging carriers through the potential barriers.  If $T < 0.1$, the barrier height must be greater than 1.5 meV [32]. From Sec. 6.4.1, we know the gap distance $w < 25$ nm.  Note one could also make devices with a single narrow gap instead of two between source and drain.  This would allow direct measurement of the tunnel resistance.

Although the conductance oscillations are not very periodic (~ 0.19 V on average), which will be discussed later in Sec. 6-6, peak positions and peak heights of the oscillations are reproducible at different scans and different scan directions.  This is in sharp contrast with the unpassivated devices (Fig. 5-12), in which the tunneling current is noisy and conductance oscillations are not repeatable due to the defect states at the Si/SiO$_2$ interface.  We ascribe this improvement to the successful passivation of the SiGe dot by the Si epitaxial regrowth.
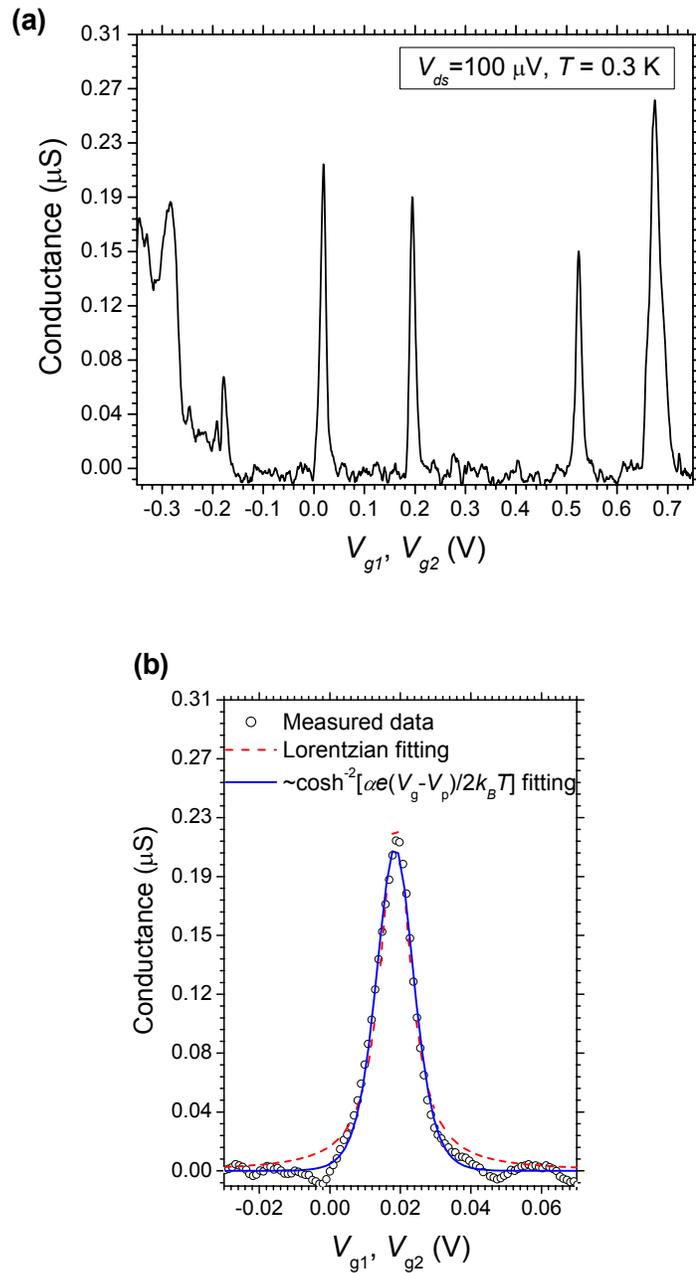
**Figure 6-16.** (a) Quantum dot conductance *vs.* two connected gate voltages at source/drain bias of 100 µV and temperature of 0.3 K; (b) conductance peak (open circle) at $V_g \sim 0.02$ V fitted to Lorentzian (dashed line) and a thermally broadened CB resonance (solid line).

The Coulomb blockade oscillations at different temperatures were measured at $V_{ds} = 1.0$ mV (Fig. 6-17).  The peak positions are identical at the different temperatures from $T = 0.36$ K to $T = 1.26$ K.  The peaks are broadened both thermally and from the source-drain bias.
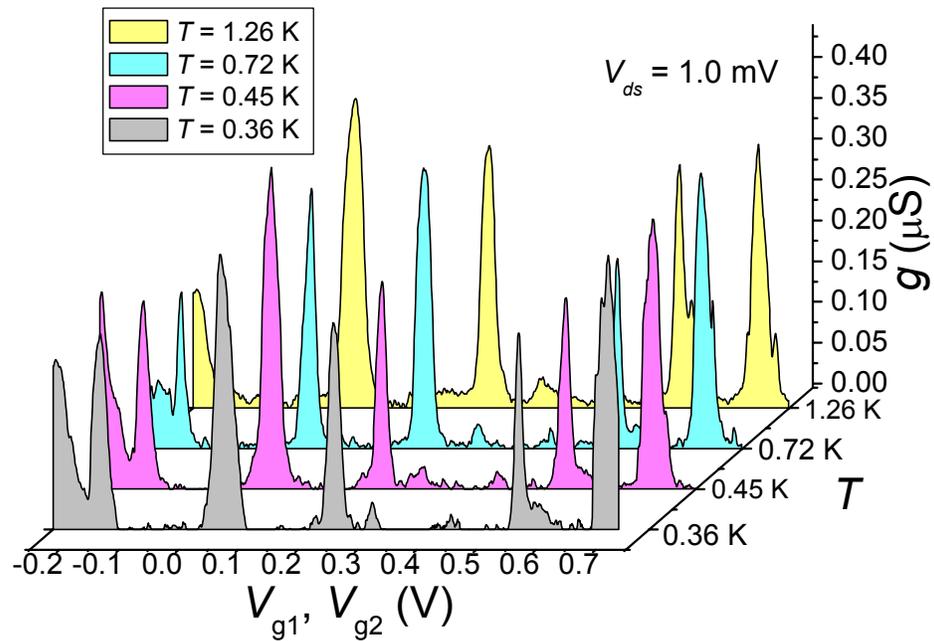


**Figure 6-17.**  Coulomb blockade oscillations of the QD device measured at the different temperatures from 0.3 K to 1.3 K.  The source-drain bias $V_{ds}$ is ~ 1.0 mV.

*Quantitative Analysis*

The differential conductance $g = \partial I / \partial V$ of the QD *vs.* gate and drain voltages is plotted in a gray scale contour scheme (Fig. 6-18), where color represents conductance. The brighter the color, the higher the conductance.  This plot required 121 scans vs. gate voltage and took ~ 20 hrs, showing extreme stability of the dot.  The Coulomb blockade

region with zero-conductance shows the expected diamond shape (dark-color in Fig. 6-18). The zero-conductance begins to be totally lost at a further higher drain voltages, no matter what gate voltages are applied. Note the boundaries of the low conductance regions are not sharp and the diamonds are hard to make out. We think it is probably due to the noise of the DC voltage in our measurements.
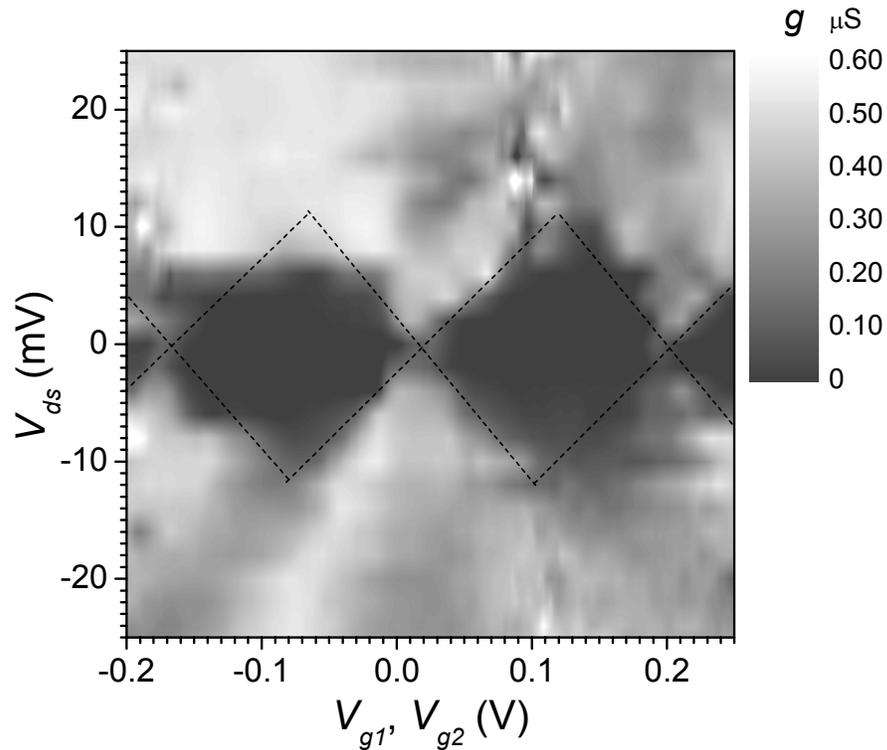


**Figure 6-18.** Differential conductance $\partial I / \partial V_{ds}$ on a linear gray scale as a function of $V_{g1}$, $V_{g2}$ for different bias voltages of $V_{ds}$. Edge bluntness is thought to be due to the noise from gates voltages. The dotted lines are estimated by eye.

Now describe how to get $C_s$, $C_d$ and $C_g$ from the "diamonds" in Fig. 6-18 as mentioned in Sec. 6.2.6. The oscillation period in Fig. 6-16 in gate voltage is ~ 0.19 V. Thus, by equation $\Delta V_g = e / C_g$, we know the gate capacitance (of two gate in parallel)

$C_g = 0.84$ aF. From the height of the diamond, one can find the charging energy

$E_c = e^2/C_\Sigma = 10.8$ meV. Therefore, $C_\Sigma = 14.8$ aF. From the slope of the diamond, we

know $C_d = 7.4$ aF and $C_s = 6.6$ aF.

Assuming dot self capacitance $C \approx C_\Sigma = 14.8$ aF, then the dot size is estimated to

be ~ 35 nm in diameter. Thus the energy level spacing is estimated (Sec. 6.2.3) to be

$\Delta\varepsilon = 0.62$ meV. Here, $C_s \gg C_g$, and $\dfrac{C_s}{C_g} \approx 7.8$, which are consistent with the

capacitance simulation in Fig. 6-15.

### 6.5.2   Quantum Dot Device with Top Gate

Reproducible *I-V* characteristics have been observed in the above passivated QD
device for one cool down. However, the *I-V* peak positions varied from one cool down
to another, which is thought to be due to the variations in top surface charge of the
device (away from the dot as in Fig. 6-19). This will make circuit application difficult.
To overcome this effect, we add a top gate to the QD device, which can shift the overall
potential of the QD so as to compensate for any trapped charges at the surface in
different cool downs.
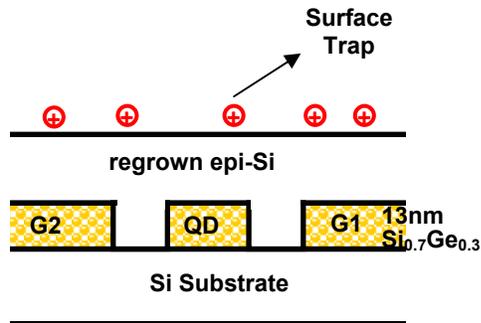


**Figure 6-19.**  Schematic drawing of surface charges on Si passivation layer.
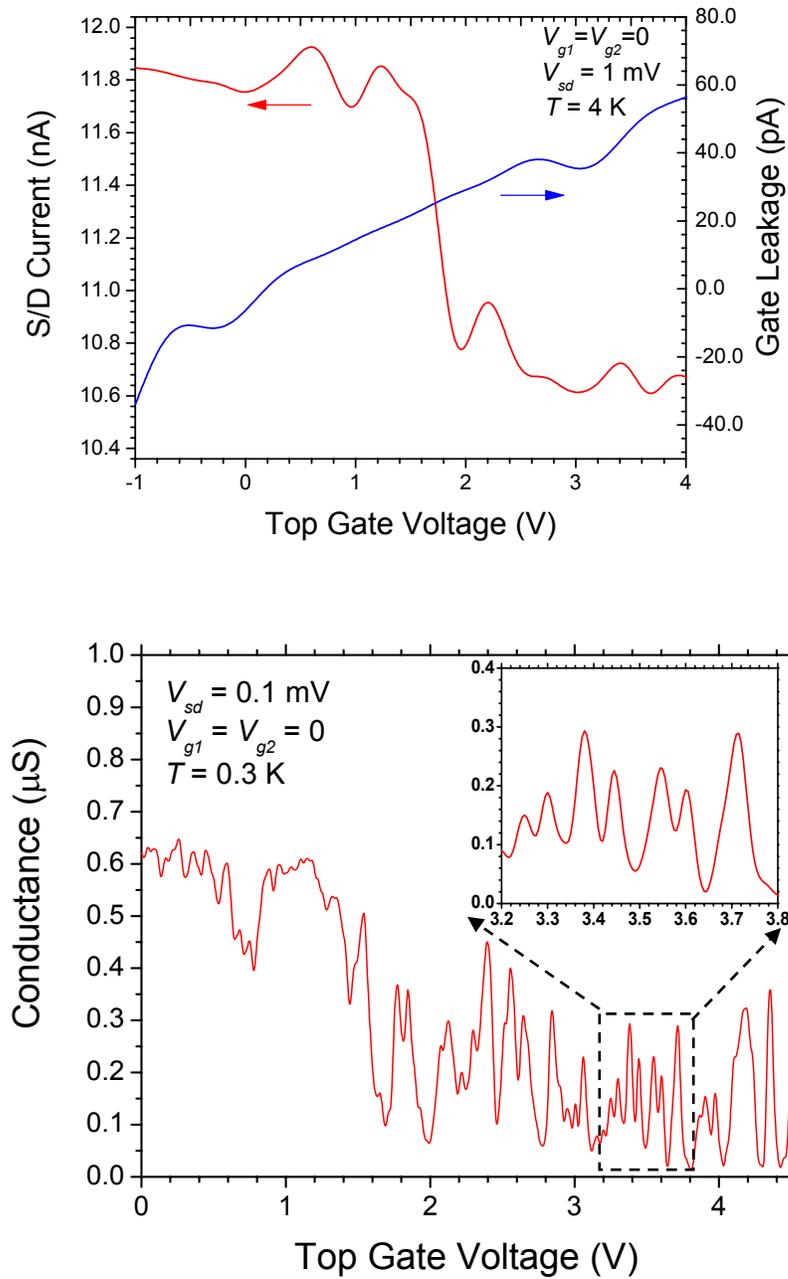
**Figure 6-20.**  Conductance of the QD *vs.* top gate voltage at (a) $T = 4$ K and (b) $T = 0.3$ K.  The two side-gate voltages are zero, and source-drain bias is 0.1 mV. The inset of (b) shows current oscillations at small range of top gate voltages.
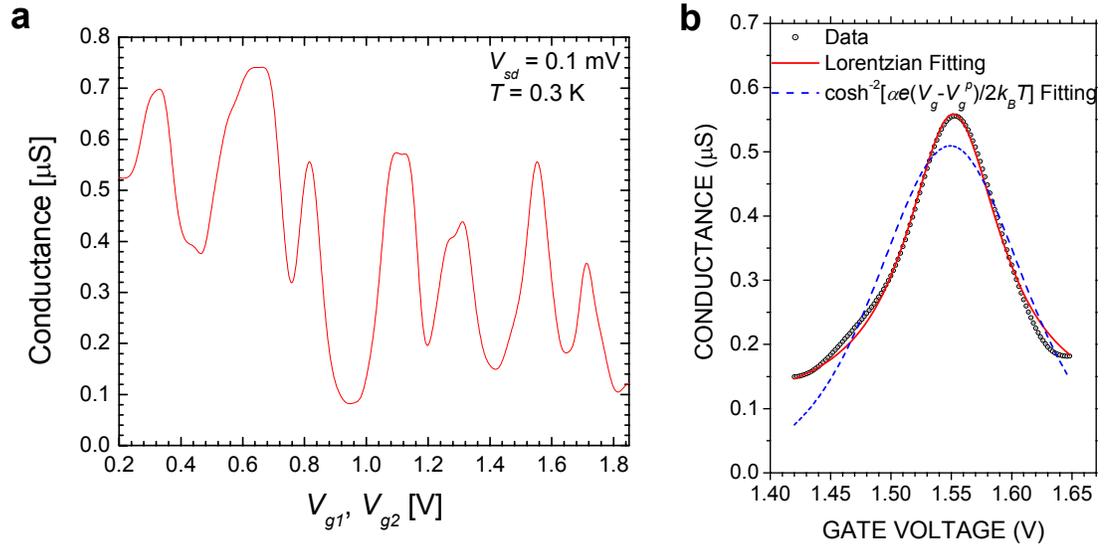
**Figure 6-21.** (a) QD conductance vs. two side-gate voltages (held equal) at $T = 0.3$ K. $V_{ds} = 0.1$ mV, and top gate voltage is zero. (b) Measured conductance peak (scattered circle) fitted by a Lorentzian function (solid line) and a function

$$G \propto \cosh^{-2}[\alpha(V_g - V_g^{peak})e/2k_BT] \quad \text{(dashed line)}.$$
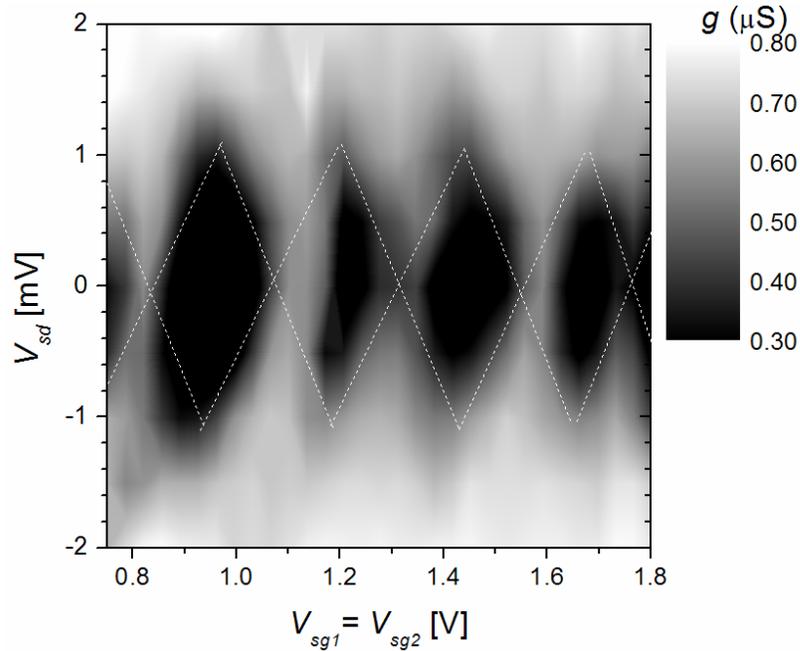


**Figure 6-22.** Differential conductance contour of the QD with drain and two-side gate voltages at $T = 0.3$ K. The top gate voltage is zero.

A QD device with a top gate has been fabricated, as shown in Fig. 6-9. After
silicon epitaxial regrowth, 38-nm-thick TEOS oxide was deposited, and followed by Al
evaporation for metal gate, which covers the whole dot. Note all the conducting carriers
are frozen out in the sample at low temperatures except holes in $p^+$-$Si_{0.7}Ge_{0.3}$ layer. The
current path is confined in the $Si_{0.7}Ge_{0.3}$ by epi-Si layers, and does not come into contact
with the gate oxide, keeping the carrier from device operation out of oxide traps. The
device was measured by varying top gate voltages at temperatures of 4 K and 0.3 K
(Fig. 6-20). In general, the source-drain conductance decreases with the increase of top
gate voltages, which is the normal character of a p-channel transistor. Conductance
oscillations due to Coulomb blockade effects occur as a function of top gate bias of the
QD, showing the top gate ability to modulate the dot potential. Weak and broad
oscillation peaks at $T = 4K$ become sharp at $T = 0.3$ K. The top-gate leakage current at
4 K is less than measured source-drain current by over two orders of magnitude for a
top gate voltage magnitude less than 4 V.

When the top gate was grounded, single-hole tunneling with two planar gate
voltages in the QD device was observed at $T = 0.3$ K (Fig. 6-21a). The peak curve at
$V_{g1} = V_{g2} \approx 1.55$ V is best fit with a Lorentzian function rather than
$G \propto \cosh^{-2}[\alpha(V_g - V_g{}^{peak})e/2k_BT]$ (see Fig. 6-21b), which indicates that the energy
level broadening energy $\hbar\Gamma \sim k_BT$ and potential barriers between source and dot, and
drain and dot are not high enough. This may explain why the conductance of the
oscillation valley does not reach zero. For the device without a top gate at previous
section, the peaks were better fit with $G \propto \cosh^{-2}[\alpha(V_g - V_g{}^{peak})e/2k_BT]$ function,
indicating a higher barrier was formed in that device. We think the difference in the
two devices is due to a difference in the gap width $w$. The barrier is a very sensitive
function of the width $w$ at the SiGe narrow region (as described in Sec. 6.4.1). Since
this width depends on the amount of over-etching on the SiGe, it is hard to control.
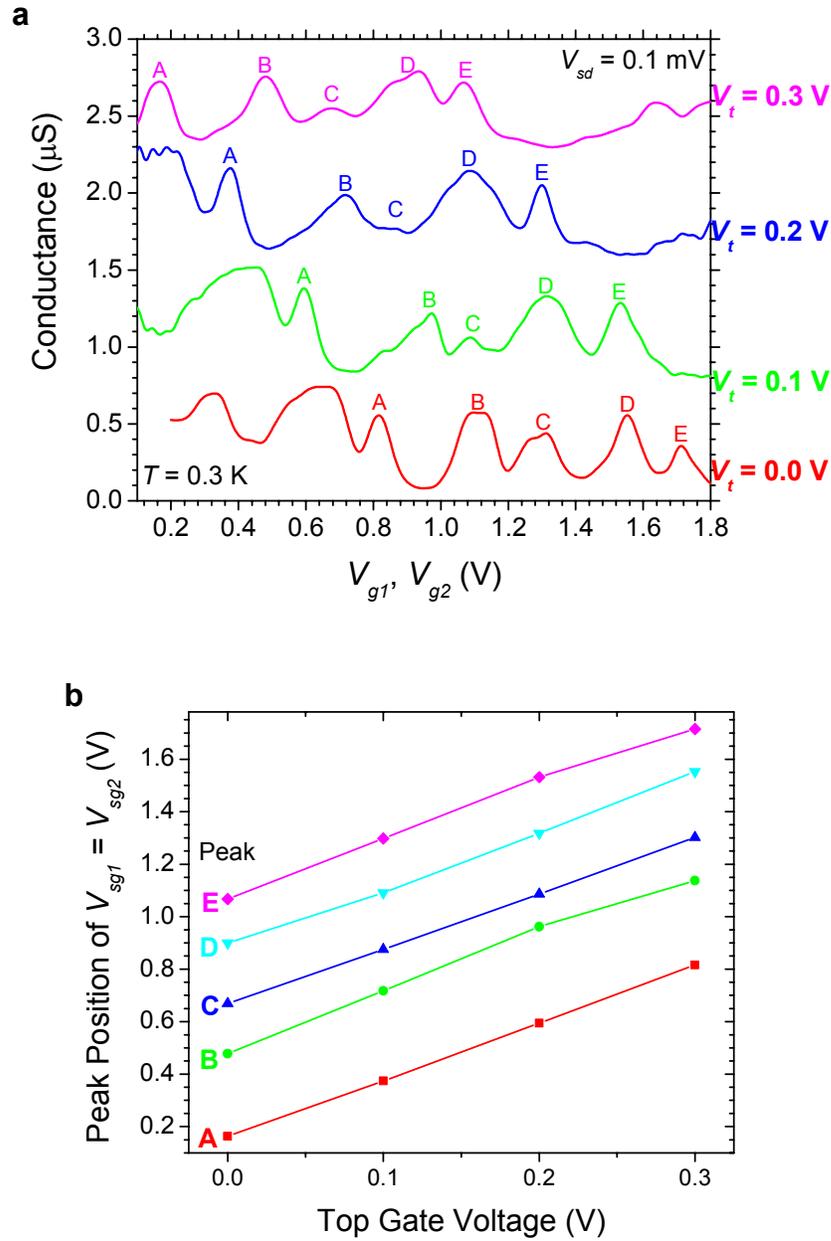
**Figure 6-23.** Conductance oscillations with two side-gate voltages (held equal) for different top gate voltages. The $V_{ds} = 0.1$ mV, and $T = 0.3$ K. The individual curves are offset vertically for different top gate voltages for clarity. (b) Side gate voltage positions for peak A, B, C, D, E $vs.$ top gate voltage.

The Coulomb blockade of conductance at various source-drain biases exhibits a poor diamond shape in a contour map with $V_{ds}$ and $V_g$ (side gates, Fig. 6-22), which can be used to characterize the charging energy. Because the characteristics were not well defined and irregular, further analysis was not done, however. Nevertheless, *I-V* characteristics were stable within one cool down for a long time and multiple scans. For example, Fig. 6-22 took ~ 10 hr and 41 scans.

The desired use of the top gate to shift the oscillation positions of the side gate is shown in Fig. 6-23. The dot conductance exhibits Coulomb blockade oscillations as a function of the double side-gate voltages, with the top gate voltage varying from 0.0 V to 0.3 V with a step of 0.1 V. Positive top gate voltages tend to deplete holes in the dot as the same as the positive side-gate voltages. Therefore, the oscillation peaks labeled by A, B, C, D, E shift to lower side-gate voltages at each increase step of the top gate voltage. The maximum amount we could shift the peaks was ~ 0.7 V. The voltage shift was regular, and was ~ 0.22 V on average (Fig. 6-23b) for a top gate voltage shift of 0.1 V. Thus the ratio $\dfrac{C_{top}}{C_g} \equiv \dfrac{\Delta V_g}{\Delta V_{top}} = 2.2$. The top gate capacitance is calculated to be ~ 6.1 aF from the thickness of epi-Si and TEOS oxide, and thus the side-gate capacitance is ~ 2.8 aF.

In summary, the top gate tuning to the conductance peak positions has been demonstrated, which may be used to adjust for a deviation of peak positions at different cool down measurements.

## 6.6    Discussion

In the passivated SiGe quantum dots of this thesis, Coulomb blockade oscillations were observed as shown in Fig. 6-16 and Fig. 6-23. The oscillations are much more reproducible at different scans than the unpassivated SiGe QDs (chapter 5) and Si QDs [17,18]. This is attributed to the improved interface quality between strained

SiGe and regrown Si.  However, the oscillations are not periodic.  Trapped charges in the $SiO_2$ or the $Si/SiO_2$ interface (or other defects), surface roughness, and random fluctuations in the dopant concentrations can cause discrete bound states or random surface potential fluctuations, leading to parasitic extra QDs.  In our passivated SiGe QDs, the aperiodic oscillations may be resulted from any of the above.  The random fluctuation in doping of the $p^+$-$Si_{0.7}Ge_{0.3}$ layer may be the main cause for the extra QDs.

The nanolines used to define a QD were drawn by AFM local oxidation and wet etching in our experiments.  After the QD was patterned, AFM imaging showed that the nanolines around the dot were continuous and smooth (see Fig. 6-5).  Only one dot was drawn. Therefore, the possibility of extra dots arising from the rough surface can be ruled out.

The interface quality between $Si_{0.7}Ge_{0.3}$ and regrown Si has been investigated in Chapter 5.  Photoluminescence spectra and SIMS analysis demonstrate a "clean" interface within the detection limit.  Cross-section TEM observations (Fig. 5-19) show that stacking fault defects exist at the $Si_{0.7}Ge_{0.3}$/regrown Si interface, but the regrowth is still epitaxial.  The density of the electrically active defect at the $Si_{0.7}Ge_{0.3}$/r-Si interface should be less than that at the $Si/SiO_2$ interface.  Furthermore, the active doping concentration in $p^+$- $Si_{0.7}Ge_{0.3}$ layer is $\sim 3\times10^{12}$ $cm^{-2}$, which is much higher than the density of stacking faults at the regrowth interface.

Figure 6-24 shows a schematic of the potential fluctuations of the valence band edge $E_v$ in a heavily doped $p^+$-SiGe layer.  The random position of dopants leads to fluctuation of the valence band edge (Fig. 6-24a).  The planar gate voltage pulls Fermi-level $E_f$ down, and the fluctuation of the $E_v$ edge results in potential barriers in the transport channel, which confine extra QDs (Fig. 6-24b).  These undesired QDs could be responsible for aperiodic Coulomb blockade oscillations [33].

**a**



**b**
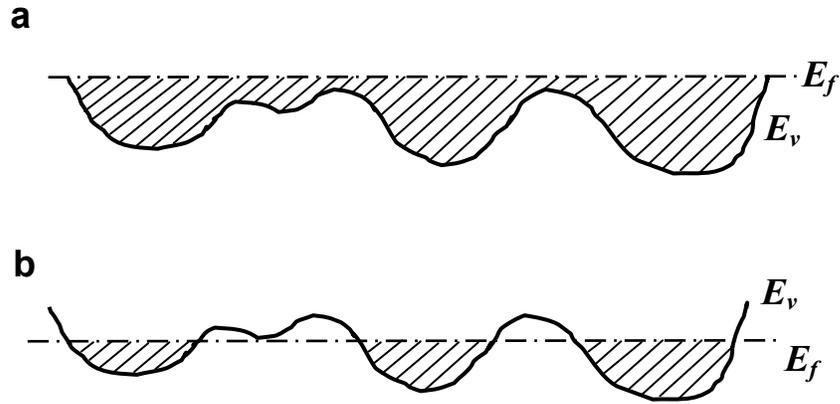


**Figure 6-24.** (a) Schematic drawing of the potential fluctuations along a heavily
doped p$^+$-SiGe line.  (b) The gate voltage pulls the Fermi energy $E_f$ down, and
potential barriers for holes along the fluctuating edge of the valence band $E_v$ define
extra isolated islands (QDs).

## 6.7    Summary

Quantum dot devices in heavily doped p$^+$-SiGe layer have been fabricated by
AFM nanopatterning and silicon epitaxial regrowth for the first time.  Within a single
cool down, the QDs exhibit reproducible Coulomb blockade oscillations at a
temperature of 0.3 K.  Both the peak position and the peak amplitude of the
conductance do not change over multiple scans.    From 0.3 K to 1.3 K the oscillation
peak positions are unchanged.  A diamond-shaped conductance contour map with $V_{ds}$
and $V_g$ was observed.

In a top-gate QD device, the side gate capacitance has been obtained by the
correlation of the oscillation peak shift between the top-gate and the side gates.  The top
gate tuning to the oscillation peak shift may be used to adjust the peak position at
different cool-downs.  All of these observations indicate that the performance of the

SiGe quantum dots passivated by silicon epitaxial regrowth has been significantly improved over that of unpassivated doped SiGe or SOI QDs.  This is because of improved QD interface quality after the passivation by Si regrowth.

We find that the conductance oscillations are not perfectly periodic with the applied voltage to the top gate and the side gates.  This is thought to be due to the random fluctuations of doping in the $p^+$-SiGe layer, which can form extra parasitic QDs.  New device structures await development, which will be proposed as follows.

## 6.8    Future work

We concluded that the existing QD devices had oscillations which were not perfectly periodic due to doping fluctuations in the heavily-doped layers.  We now propose future work to address this issue.

### 6.8.1    QD in Si/SiGe 2DHG

As mentioned in Sec. 6.1, QDs fabricated from a two-dimensional hole gas (2DHG) in modulation-doped Si/SiGe heterostructures have been demonstrated [12,13].  Voltage applied to top metal gates depleted the underneath 2DHG, and defined planar QDs.  The effects of an undesired extra parasitic dot were observed, and parasitic dot was thought to be due to the disorder in 2DHG [13].  Using the AFM nanopatterning technique, we can also fabricate QD device in a Si/SiGe 2DHG.  Compared with the previous work, we think by directly patterning doped supply layer QD device can achieve tighter confinement than with a top metal gate.  We also hope that with a high 2-D gas quality, disorder in the 2-D gas and the parasitic dot effects can be avoided.

Figure 6-25 shows the layer structure designed for QD fabrication and the corresponding energy band diagram.  A 2DHG is generated in the strained $Si_{0.75}Ge_{0.25}$ layer close to the interface with Si spacer (Fig. 6-25a).  Band structure simulation [34] gives the density of the 2DHG $\sim 5.4 \times 10^{11}$ cm$^{-2}$.  The doped $p^+$-$Si_{0.9}Ge_{0.1}$ supply layer can be removed by AFM nanopatterning to electrically isolate the 2DHG (Fig. 6-25b).

Assuming the Fermi level at the bare surface pins at midgap, the energy barrier for
holes to enter this region from the adjacent 2-D gas formed at the nanolines is ~ 0.39
eV.  Since the 2DHG at the etched trench is still passivated by Si spacer, the influence
of the interface states on the QD performance can be suppressed.
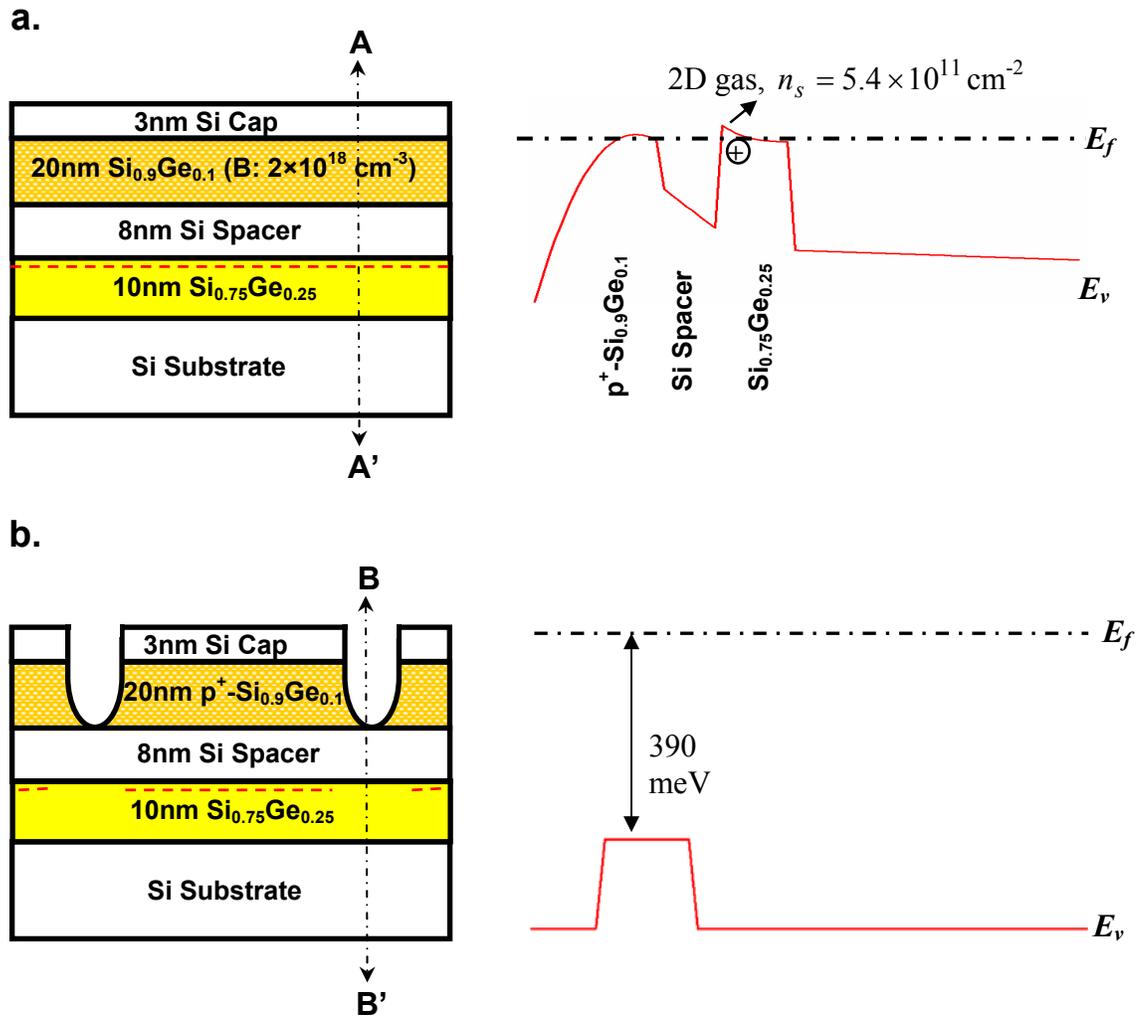


**Figure 6-25.**  Layer structure and vertical energy band diagram (a) before (along A-
A') and (b) after AFM nanopatterning (along B-B'), where the dopant supply layer
was removed.  Note when the supply layer is removed, the valence band is ~ 390 meV
lower than where 2-D gas is present.

### 6.8.2　QD in Si/SiGe 2DEG

To my best knowledge, QD devices in a 2DEG of modulation doped Si/SiGe heterojunctions have never been reported. We propose the following structure to fabricate a QD by AFM nanopatterning as shown in Fig. 6-26. A 2DEG is formed in tensile-strained silicon close to the interface with a top $Si_{0.7}Ge_{0.3}$ spacer. As proposed in previous section, this 2DEG will be depleted due to the removal of the $n^+$-$Si_{0.7}Ge_{0.3}$ layer by AFM nanopatterning technique to pattern potential barriers. One of key elements is how to achieve a high quality relaxed $Si_{0.7}Ge_{0.3}$ layer grown on Si with low density of threading dislocations and a smooth surface. Although we demonstrate that rough strain-relaxed SiGe layers can be locally oxidized by AFM in Fig. 4-5, smooth surfaces are desirable for repeatable device fabrication by AFM. Yin *et al.* [35] have demonstrated flat relaxed SiGe islands with RMS roughness ~ 1nm. The relaxation at $T$ = 850 °C was due to the compliant flow of epitaxial $Si_{0.7}Ge_{0.3}$ films with bonded borophosphorosilicate (BPSG) glass. Using this method, 2DEG in Si/SiGe heterojunctions with flat surfaces and high mobility are expected, on which quantum dot devices can be fabricated by AFM nanolithography.
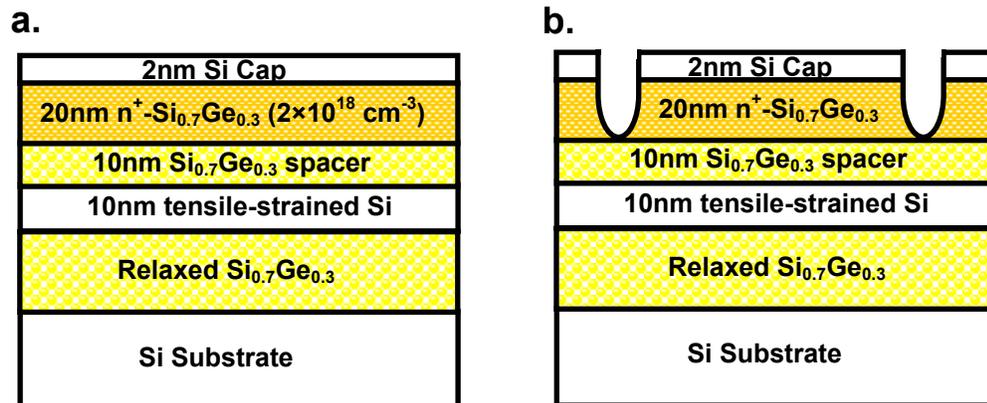


**Figure 6-26.** Layer structure of 2DEG in Si/SiGe heterojunctions (a) before and (b) after (b) AFM nanopatterning.

# References

[1] T.A. Fulton and G.J. Dolan, "Observation of single-electron charging effects in small tunnel junctions", *Phys. Rev. Lett.*, **59**: 109-112 (1987).

[2] "*Single Charge Tunneling*", edited by H. Grabert and M.H. Devoret (Plenum Press, 1991).

[3] L. P. Kouwenhove, C. M. Marcus, P. L. McEuen, S. Tarucha, R. M. Westervelt, and N. S. Wingreen, "Electron transport in quantum dot", Proceedings of the Advanced Study Institute on *Mesoscopic Electron Transport*, edited by L. L. Sohn, L. P. Kouwenhoven, G. Schön (Kluwer 1997).

[4] L. P. Kouwenhoven, A. T. Johnson, N. C. van der Vaart, C.J.P.M. Harmans and C. T. Foxon, "Quantized current in a quantum-dot turnstile using oscillating tunnel barriers", *Phys. Rev. Lett.*, **67**: 1626-1629 (1991).
Y. Nagamune, H. Sakaki, L. P. Kouwenhoven, L. C. Mur, C.J.P.M. Harmans, J. Motohisa, and H. Noge, "Single electron transport and current quantization in a novel quantum dot structure", *Appl. Phys. Lett.*, **64**: 2379-2381 (1994).

[5] G. Zimmerli, T. M. Eiles, R. L. Kautz, and J. M. Martinis, "Noise in the Coulomb blockade electrometer", *Appl. Phys. Lett.*, **61**: 237-239 (1992). D. V. Averin, "Charge sensitivity of the single electron tunneling transistor with discrete energy spectrum", *J. Appl. Phys.*, **73**: 2593-2595 (1993). D. J. Mar, R. M. Westervelt, and P. F. Hopkins, "Cryogenic field-effect transistor with single electronic charge sensitivity", *Appl. Phys. Lett.*, **64**: 631-633 (1994).

[6] L. J. Guo, E. Leobandung, and S. Y. Chou, "Silicon single electron MOS memory", *Science*, **275**: 649 (1997).

[7] Y. Takahashi, A. Fujiwara, Y. Ono, and H. Inokawa, "Silicon Single-Electron Transistors and Single-Electron CCD", *Mat. Res. Soc. Sym. Proc.*, **686**: A7.1 (2002).

[8] D. Loss, and D. P. DiVincenzo, "Quantum computation with quantum dots", *Phy. Rev. A*, **57**: 120-126 (1998).

[9] L. P. Rokhinson, Private communications.

[10] M. Friesen, P. Rugheimer, D. E. Savage, M. G. Lagally, D. W. van der Weide, R. Joynt, and M. A. Eriksson, "Practical design and simulation of silicon-based quantum-dot qubits", *Phys. Rev. B*, **67**: 121301 (R) (2003).

[11] Z. Wilamowski, W. Jantsch, N. Sandersfeld, M. Mühlberger, F. Schäffler and S. Lyon, "Spin relaxation and *g*-factor of two-dimensional electrons in Si/SiGe quantum wells", *Physica E*, **16**: 111-120 (2003).

[12] D. J. Paul, J. R. A. Cleaver, and H. Ahmed, "Coulomb blockade in silicon based structures at temperatures up to 50 K", *Appl. Phys. Lett.*, **63**: 631-632 (1993).

[13] U. Dötsch, U. Gennser, C. David, G. Dehlinger, D. Grützmacher, T. Heinzel, S. Lüscher, and K. Ensslin, "Single-hole transistor in a p-Si/SiGe quantum well", *Appl. Phys. Lett.*, **78**: 341-343 (2001).

[14] L. Zhuang, L. Guo, and S. Y. Chou, "Silicon single-electron quantum-dot transistor switch operating at room temperature", *Appl Phys Lett.*, **72**: 1205-1207 (1998).

[15] D. Ali and H. Ahmed, "Coulomb blockade in a silicon tunnel junction device", *Appl. Phys. Lett.*, **64**: 2119-2121 (1994). R. A. Smith and H. Ahmed, "Gate controlled Coulomb blockade effects in the conduction of a silicon quantum wire", *J. Appl. Phys.*, **81**: 2699-2703 (1997). A. Tilke, R. H. Blick, H. Lorenz, J. P. Kotthaus, and D. A. Wharam, "Coulomb blockade in quasimetallic silicon-on-insulator nanowires", *Appl. Phys. Lett.*, **75**: 3704-3706 (1999).

[16] Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwadate, Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, "Fabrication technique for Si single-electron transistor operating at room temperature", *Electron. Lett.*, **31**: 136-137 (1995). E. Leobandung, L. Guo, Y. Wang, and S. Y. Chou, "Observation of quantum effects and Coulomb blockade in silicon quantum-dot transistors at temperatures over 100 K", *Appl. Phys. Lett.*, **67**: 938-940 (1995). H. Ishikuro and T. Hiramotob, "On the origin of tunneling barriers in silicon single electron and single hole transistors", *Appl. Phys. Lett.*, **74**: 1126-1128 (1999).

[17] R. A. Smith and H. Ahmed, "Gate controlled Coulomb blockade effects in the conduction of a silicon quantum wire", *J. Appl. Phys.*, **81**: 2699-2703 (1997).

[18] A. T. Tilkea, F. C. Simmelb, R. H. Blickc, H. Lorenzc, and J. P. Kotthausb, "Coulomb blockade in silicon nanostructures", *Progress in Quantum Electronics*, **25**: 97–138 (2001).

[19] S. Kanjanachuchai, J. M. Bonar, H. Ahmed, "Single-charge tunneling in n- and *p*-type strained silicon germanium on silicon-on-insulator", *Semicond. Sci. Technol.*, **14**: 1065-1068 (1999).

[20] X.-Z. Bo, L. P. Rokhinson, H. Yin, D. C. Tsui, and J. C. Sturm, "Nanopatterning of Si/SiGe electrical devices by atomic force microscopy oxidation", *Appl. Phys. Lett.*, **81**: 3263-3265 (2002).

[21] L. P. Rokhinson, L. J. Guo, S. Y. Chou, and D. C. Tsui, "Double-dot charge transport in Si single-electron/hole transistors", *Appl Phys Lett.*, **76**: 1591-1593 (2000).

[22] P. A. Maksym and T. Chakaraborty, "Quantum dots in a magnetic field: Role of electron-electron interactions", *Phys. Rev. Lett.*, **65**: 108-111 (1990).

[23] D. Pfannkuche, and S. E. Ulloa, "Selection Rules for Transport Excitation Spectroscopy of Few-Electron Quantum Dots", *Phy. Rev. Lett.*, 74: 1194-1197 (1995).

[24] N. F. Johnson, and M. C. Payne, "Exactly solvable model of interacting particles in a quantum dot," *Phys. Rev. Lett.*, **67**: 1157-1140 (1991).

[25] N. F. Johnson, and L. Quiroga, "Analytic results for N particles with $1/r^2$ interaction in two dimensions and an external magnetic field," *Phys. Rev. Lett.*, **74**: 4277-4280 (1995).

[26] L. Guo, "Semiconductor single-electron transistors and memories", Ph.D. Thesis, University of Minnesota (1997).

[27] Y. Meir, N. S. Wingreen, and P. A. Lee, "Transport through a strongly interacting electron systems: theory of periodic conductance oscillations", *Phys. Rev. Lett.*, **66**: 3048-3052 (1991).

[28] W. Wu, "Applications of nanoimprint lithography for nano-devices and nanofabrication", Ph.D. thesis, Princeton University, Nov. 2003.

[29] F. Schäffler, "High-mobility Si and Ge structures", *Semicond. Sci. Technol.*, **12**: 1515-1549 (1997).

[30] Synopsys, Inc., "Medici: Two-dimensional device simulation program", user manual (2003).

[31] V. Venkataraman, Private Communication.

[32] R. L. Liboff, "Introductory quantum mechanics", Addison-Wesley Press,  3$^{rd}$ Ed (1998).

[33] W. G. van der Wiel, S. De Franceschi, J. M. Elzerman, T. Fujisawa, S. Tarucha, and L. P. Kouwenhoven, "Electron transport through double quantum dots", *Rev. Mod. Phy.*, **75**: 1-22 (2003).

[34] G. L. Snider, I.-H. Tan, and E. L. Hu, "Electron states in mesa-etched one-dimensional quantum well wires", *J. Appl. Phys.*, **68**, 2849-2853 (1990).  Calculations were performed using G. L. Snider's 1D Poisson solver downloaded from http://www.nd.edu/%7Egsnider/.

[35] H. Yin, R. Huang, K. D. Hobart, Z. Suo, T. S. Kuan, C. K. Inoki, S. R. Shieh, T. S. Duffy, F. J. Kub, and J. C. Sturm, "Strain relaxation of SiGe islands on compliant oxide", *J. Appl. Phys.*, **91**: 9716-9722 (2002).

# Chapter 7

# CONCLUSIONS

We have investigated Si-based materials grown by CVD (including *a*-Si, poly-Si, single-crystalline Si and SiGe), and devices focusing on the solid-phase crystallization (SPC) of *a*-Si, the CVD growth of *a*-Si for photonic bandgap crystals, and SiGe quantum dot (QD) single-hole transistors.

The motivation for the study of *a*-Si SPC is to improve the quality of crystallized poly-Si by reducing the density of grain boundaries and defects within them, both of which are thought to be the scattering centers for carrier transport in thin film transistors (TFTs). To control the grain boundaries, a small area of *a*-Si film was selected by silicon nitride masking for hydrogen plasma treatment at room temperature, which has been proven to enhance the SPC of *a*-Si. It was found that when the *a*-Si opening window was $\leq 0.6$ µm, a single grain was formed by furnace anneal at 600 °C. The single grain size can reach ~ 2.5 µm. To reduce the intragranular defect density in poly-Si film, an *a*-Si suspended cantilever without underlying oxide was fabricated. The "free" rearrangement of Si atoms in the *a*-Si cantilever without underlying oxide restriction during the nucleation and growth stages of SPC leads to poly-Si by one order of magnitude reduction in defect density from $10^{11}$ cm$^{-2}$ to $10^{10}$ cm$^{-2}$. A new fabrication process with a combination of the above techniques is proposed to improve the performance of poly-Si TFTs.

In chapter 3, we studied how to invert the self-assembly opals with *fcc* ordered structure to 3-D photonic bandgap crystals by the chemical vapor deposition of *a*-Si. Self-assembled opals cannot form a photonic bandgap due to the lower refractive index

154

contrast between $SiO_2$ and air, but can be used as a template for periodic structure inversion. LPCVD $a$-Si deposition achieved conformal growth with the silica spheres, successfully filling silicon atoms into the interstitial space between them up to 20-layer spheres. The conformal growth is attributed to the long mean free path of Si atoms resulting from the extremely low partial pressure of $SiH_4$ gas and low deposition rate at $T = 550$ °C. 3-D photonic crystals were then formed by removing the $SiO_2$ spheres by wet etching. The reflectivity was measured to be 1 at the wavelength of 1.3 µm from <111> and <100> directions of the crystal. Furthermore, the fabricated crystals were patterned by conventional photolithography and RIE, which demonstrates the feasibility of the integration of photonic components with microelectronic devices on a silicon wafer.

To fabricate nanoelectronic devices, we developed an atomic force microscope (AFM) nanolithography technique to locally oxidize Si and SiGe surfaces by applying a negative bias to the AFM tip in a humid environment. The minimum feature sizes were less than 20 nm. The thickness of oxidized SiGe was under 2 nm with bias voltage less than 20 V. To pattern a relatively thick SiGe layer, 2-nm-thick Si on $Si_{0.7}Ge_{0.3}$ was first locally oxidized by AFM, and selective wet etching transferred the Si pattern into an underlying 10-nm-thick $p^+$-$Si_{0.7}Ge_{0.3}$ layer. SiGe QD devices were fabricated by this nanopatterning technique, showing Coulomb blockade oscillations.

Si-based quantum devices suffer from trapping states related to their surface $SiO_2$ passivations. Charges trapped in $SiO_2$ or defect states at the $Si/SiO_2$ interface can interact with electrons in the dot and also form undesired parasitic QDs, leading to irreproducible $I$-$V$ characteristics or undesired features. The lattice matched interface in Si/SiGe heterojunctions can solve this problem. After the SiGe QD device was patterned by AFM nanolithography, silicon epitaxial regrowth was performed to passivate the patterned SiGe surface. The improved interface leads to reproducible Coulomb blockade oscillations of SiGe QD at $T = 0.3$ K. The oscillation reproducibility exists at different temperatures and for multiple scans within a single cool down. Top gate tuning of single-hole resonant tunneling with planar gates was also demonstrated. The Coulomb blockade oscillations in our fabricated QD are not perfectly periodic.

This is thought to be due to the parasitic extra QDs from the random fluctuations of doping in $p^+$-$Si_{0.7}Ge_{0.3}$ layer. To overcome this effect, a new device structure has been proposed using AFM nanopatterning on 2-D hole and 2-D electron gases.

# RECIPE OF A-SI PECVD GROWTH

(1) 150nm *a*-Si:H at 150 °C with RF power ~ 4.5 W (net): aSi150.rcp

| Step No. | Description | Time (s) | DC Power (mA) | Pressure (mtorr) | Set point temperature ($^o$C) | | | Flow rate (sccm) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Heater 1 | Heater 2 | Heater 3 | Ar | H$_2$ | SiH$_4$ |
| 1 | Ar flush | 60 | | 650 | 150 | 150 | 130 | 50 | | |
| 2 | H$_2$ flush | 120 | | 650 | ,, | ,, | ,, | | 50 | |
| 3 | H$_2$ plasma | 120 | 75 | 650 | ,, | ,, | ,, | | 50 | |
| 4 | H$_2$ flush | 120 | | 500 | ,, | ,, | ,, | | 50 | |
| 5 | SiH$_4$ flush | 120 | | 500 | ,, | ,, | ,, | | | 50 |
| 6 | Si dep. | 1000 | | 500 | ,, | ,, | ,, | | | 50 |
| 7 | SiH$_4$ flush | 120 | | 500 | ,, | ,, | ,, | | | 50 |
| 8 | Ar flush | 120 | | 500 | ,, | ,, | ,, | 50 | | |

# EXAMPLE SCRIPT PROGRAM OF AFM NANOLITHOGRAPHY FOR A QD DEVICE

```
#include <gui.h>
#include "lr-litho.m"

char *t2=" ";

// ====================================
// pattern: dot
//       \        /
//        \      /
//         \/\/
//
//         /\/\
//        /      \
//       /        \
//
// ====================================

void main()
{
   float bias = 0;
   float speed = 0;
   float delay = 0;
   float dZ=0;

bias=-20;
speed=.5;
fspeed=1;
dZ=-0;
delay=0;

LITHO_BEGIN;
```

```
lline(-3.03,2.71,2.93,-2.41,bias,speed,dZ,delay,bias_on | dZ_down);
lline(0,0,.1,0.1,bias,speed,dZ,delay,0);
lline(0,0,0.1,-0.1,bias,speed,dZ,delay,0);
lline(0,0,2.83,2.52,bias,speed,dZ,delay,bias_off);
lline(-0.6,-5.51,-2.72,2.39,bias,speed,dZ,delay,bias_on);
lline(0,0,-.1,-.1,bias,speed,dZ,delay,0);
lline(0,0,-.1,.1,bias,speed,dZ,delay,0);
lline(0,0,-3.07,-2.2,bias,speed,dZ,delay,bias_off | dZ_up);
LITHO_END;
EraseMessage;
}
```

# Medici Simulation of Potential Barrier and Capacitances in QD

```
TITLE      MEDICI Example: Topview of QD

COMMENT    Specify a rectangular mesh
MESH       SMOOTH=1

COMMENT    Specify the width of the mesh and the spacing
COMMENT    is 0.02 micron
X.MESH     X.MAX=0.35 H1=0.01
X.MESH     X.MIN=0.35 X.MAX=0.65 H1=0.005
X.MESH     X.MIN=0.65 X.MAX=1.0 H1=0.01

COMMENT    Specify the spacing between y=0 and y=2um is 0.02um
Y.MESH     Y.MAX=0.35 H1=0.01
Y.MESH     Y.MIN=0.35 Y.MAX=0.65 H1=0.005
Y.MESH     Y.MIN=0.65 Y.MAX=1.0 H1=0.01

ELIMIN     COLUMNS X.MIN=0.35 X.MAX=0.49 Y.MAX=0.35
ELIMIN     COLUMNS X.MIN=0.35 X.MAX=0.49 Y.MIN=0.65
ELIMIN     COLUMNS X.MIN=0.52 X.MAX=0.65 Y.MAX=0.35
ELIMIN     COLUMNS X.MIN=0.52 X.MAX=0.65 Y.MIN=0.65
ELIMIN     ROWS Y.MIN=0.35 Y.MAX=0.48 X.MAX=0.35
ELIMIN     ROWS Y.MIN=0.35 Y.MAX=0.48 X.MIN=0.65
ELIMIN     ROWS Y.MIN=0.51 Y.MAX=0.65 X.MAX=0.35
ELIMIN     ROWS Y.MIN=0.51 Y.MAX=0.65 X.MIN=0.65

ELIMIN     COLUMNS X.MAX=0.25
ELIMIN     COLUMNS X.MIN=0.75
ELIMIN     ROWS Y.MAX=0.25
ELIMIN     ROWS Y.MIN=0.75

COMMENT    Specify oxide and silicon regions
REGION     SILICON

COMMENT    Specify oxide region
```

```
COMMENT    Specify upper part
REGION     OXIDE  POLYGON
+          X.POLY=(0, 0.47, 0.47, 0.20)
+          Y.POLY=(0, 0.49, 0.29, 0)
REGION     OXIDE  POLYGON
+          X.POLY=(0.47, 0.47, 0.49, 0.49)
+          Y.POLY=(0.29, 0.49, 0.49, 0.29)
REGION     OXIDE    POLYGON
+          X.POLY=(0.49, 0.49, 0.51, 0.51)
+          Y.POLY=(0.29, 0.49, 0.47, 0.27)
REGION     OXIDE    POLYGON
+          X.POLY=(0.51, 0.51, 0.53, 0.53)
+          Y.POLY=(0.27, 0.47, 0.49, 0.29)
REGION     OXIDE  POLYGON
+          X.POLY=(0.53, 0.53, 0.55, 0.55)
+          Y.POLY=(0.29, 0.49, 0.49, 0.29)
REGION     OXIDE     POLYGON
+          X.POLY=(0.55, 0.55, 1.0, 0.8)
+          Y.POLY=(0.29, 0.49, 0, 0)
COMMENT    Specify lower part
REGION     OXIDE     POLYGON
+          X.POLY=(0, 0.2, 0.47, 0.47)
+          Y.POLY=(1, 1, 0.7, 0.5)
REGION     OXIDE  POLYGON
+          X.POLY=(0.47, 0.47, 0.49, 0.49)
+          Y.POLY=(0.5, 0.7, 0.7, 0.5)
REGION     OXIDE     POLYGON
+          X.POLY=(0.49, 0.49, 0.51, 0.51)
+          Y.POLY=(0.50, 0.70, 0.72, 0.52)
REGION     OXIDE     POLYGON
+          X.POLY=(0.51, 0.51, 0.53, 0.53)
+          Y.POLY=(0.52, 0.72, 0.70, 0.50)
REGION     OXIDE  POLYGON
+          X.POLY=(0.53, 0.53, 0.55, 0.55)
+          Y.POLY=(0.5, 0.7, 0.7, 0.5)
REGION     OXIDE     POLYGON
+          X.POLY=(0.55, 0.55, 0.8, 1.0)
+          Y.POLY=(0.50, 0.70, 1, 1)

COMMENT    Electrode definition
ELECTR     NAME=Gate1    X.MIN=0.2  X.MAX=0.8   TOP
ELECTR     NAME=Gate2    X.MIN=0.2  X.MAX=0.8   BOTTOM
ELECTR     NAME=Source   LEFT
ELECTR     NAME=Drain    RIGHT

COMMENT    Define a whole 40nm*50nm dot as electrode
ELECTR     NAME=Dot POLYGON
+          X.POLY=(0.49, 0.49, 0.51, 0.53, 0.53, 0.51)
+          Y.POLY=(0.49, 0.50, 0.52, 0.50, 0.49, 0.47)

COMMENT    Specify impurity profiles and fixed charge
PROFILE    P-TYPE  N.PEAK=3E18  UNIFORM

MATERIAL   OXIDE    PERMITTI=11.7
```

```
PLOT.2D    GRID   TITLE=" Initial Grid"  FILL   SCALE
+          DEVICE=POSTSCRIPT PLOT.OUT=GRID.ps

COMMENT    Specify contact parameters
CONTACT    NAME=Gate1   NEUTRAL
CONTACT    NAME=Gate2   NEUTRAL
CONTACT    NAME=Source   NEUTRAL
CONTACT    NAME=Drain    NEUTRAL
CONTACT    NAME=Dot    NEUTRAL

COMMENT    Specify physical models to use
MODELS     CONMOB TEMPERAT=60

COMMENT    Use Newton's method and solve for electrons
SYMB       NEWTON  CARRIERS=1  HOLE

COMMENT    V(Gate)=0.0
SOLVE      V(Gate1)=0.0  V(Gate2)=0.0
PLOT.1D    POTENTIA X.START=0 X.END=1 Y.START=0.495 Y.END=0.495
+          POINTS BOT=-0.6 TOP=-0.5 COLOR=2
+          TITLE="Potential Profile"
+          DEVICE=POSTSCRIPT PLOT.OUT=V0.ps
+          OUT.FILE=P0
LABEL      LABEL="Vg1=0.0, Vg2=0.0V"  X=0.1  Y=-0.5
LABEL      LABEL="center of 10nm gap"
LABEL      LABEL="Na = 3E18 cm^-3"
SOLVE      AC.ANALY  FREQ=1e3 VSS=0.001 TERMINAL=Dot
+          OUT.FILE=AC0  CURRENTS

COMMENT    V(Gate)=1.0
SOLVE      V(Gate1)=1.0  V(Gate2)=1.0
PLOT.1D    POTENTIA X.START=0 X.END=1 Y.START=0.495 Y.END=0.495
+          POINTS BOT=-0.6 TOP=-0.2 COLOR=2
+          TITLE="Potential Profile"
+          DEVICE=POSTSCRIPT PLOT.OUT=V1.ps
+          OUT.FILE=P1
LABEL      LABEL="Vg1=1.0, Vg2=1.0V"  X=0.1  Y=-0.5
LABEL      LABEL="center of 10nm gap"
LABEL      LABEL="Na = 3E18 cm^-3"
SOLVE      AC.ANALY  FREQ=1e3 VSS=0.001 TERMINAL=Dot
+          OUT.FILE=AC1  CURRENTS

COMMENT    V(Gate)=2.0
SOLVE      V(Gate1)=2.0  V(Gate2)=2.0
PLOT.1D    POTENTIA X.START=0 X.END=1 Y.START=0.495 Y.END=0.495
+          POINTS BOT=-0.6 TOP=-0.2 COLOR=2
+          TITLE="Potential Profile"
+          DEVICE=POSTSCRIPT PLOT.OUT=V2.ps
+          OUT.FILE=P2
LABEL      LABEL="Vg1=2.0, Vg2=2.0V"  X=0.1  Y=-0.5
LABEL      LABEL="center of 10nm gap"
LABEL      LABEL="Na = 3E18 cm^-3"
SOLVE      AC.ANALY  FREQ=1e3 VSS=0.001 TERMINAL=Dot
+          OUT.FILE=AC2  CURRENTS
```

```
COMMENT   V(Gate)=3.0
SOLVE     V(Gate1)=3.0  V(Gate2)=3.0
PLOT.1D   POTENTIA X.START=0 X.END=1 Y.START=0.495 Y.END=0.495
+         POINTS BOT=-0.6 TOP=-0. COLOR=2
+         TITLE="Potential Profile"
+         DEVICE=POSTSCRIPT PLOT.OUT=V3.ps
+         OUT.FILE=P3
LABEL     LABEL="Vg1=3.0, Vg2=3.0V"  X=0.1  Y=-0.5
LABEL     LABEL="center of 10nm gap"
LABEL     LABEL="Na = 3E18 cm^-3"
SOLVE     AC.ANALY  FREQ=1e3 VSS=0.001 TERMINAL=Dot
+         OUT.FILE=AC3  CURRENTS

COMMENT   V(Gate)=4.0
SOLVE     V(Gate1)=4.0  V(Gate2)=4.0
PLOT.1D   POTENTIA X.START=0 X.END=1 Y.START=0.495 Y.END=0.495
+         POINTS BOT=-0.6 TOP=-0. COLOR=2
+         TITLE="Potential Profile"
+         DEVICE=POSTSCRIPT PLOT.OUT=V4.ps
+         OUT.FILE=P4
LABEL     LABEL="Vg1=4.0, Vg2=4.0V"  X=0.1  Y=-0.5
LABEL     LABEL="center of 10nm gap"
LABEL     LABEL="Na = 3E18 cm^-3"
SOLVE     AC.ANALY  FREQ=1e3 VSS=0.001 TERMINAL=Dot
+         OUT.FILE=AC4  CURRENTS

COMMENT   V(Gate)=5.0
SOLVE     V(Gate1)=5.0  V(Gate2)=5.0
PLOT.1D   POTENTIA X.START=0 X.END=1 Y.START=0.495 Y.END=0.495
+         POINTS BOT=-0.6 TOP=-0. COLOR=2
+         TITLE="Potential Profile"
+         DEVICE=POSTSCRIPT PLOT.OUT=V5.ps
+         OUT.FILE=P5
LABEL     LABEL="Vg1=5.0, Vg2=5.0V"  X=0.1  Y=-0.5
LABEL     LABEL="center of 10nm gap"
LABEL     LABEL="Na = 3E18 cm^-3"
SOLVE     AC.ANALY  FREQ=1e3 VSS=0.001 TERMINAL=Dot
+         OUT.FILE=AC5  CURRENTS

COMMENT   V(Gate)=6.0
SOLVE     V(Gate1)=6.0  V(Gate2)=6.0
PLOT.1D   POTENTIA X.START=0 X.END=1 Y.START=0.495 Y.END=0.495
+         POINTS BOT=-0.6 TOP=-0. COLOR=2
+         TITLE="Potential Profile"
+         DEVICE=POSTSCRIPT PLOT.OUT=V6.ps
+         OUT.FILE=P6
LABEL     LABEL="Vg1=6.0, Vg2=6.0V"  X=0.1  Y=-0.5
LABEL     LABEL="center of 10nm gap"
LABEL     LABEL="Na = 3E18 cm^-3"
SOLVE     AC.ANALY  FREQ=1e3 VSS=0.001 TERMINAL=Dot
+         OUT.FILE=AC6  CURRENTS

COMMENT   V(Gate)=7.0
SOLVE     V(Gate1)=7.0  V(Gate2)=7.0
PLOT.1D   POTENTIA X.START=0 X.END=1 Y.START=0.495 Y.END=0.495
```

```
+          POINTS BOT=-0.6 TOP=-0. COLOR=2
+          TITLE="Potential Profile"
+          DEVICE=POSTSCRIPT PLOT.OUT=V7.ps
+          OUT.FILE=P7
LABEL      LABEL="Vg1=7.0, Vg2=7.0V"  X=0.1  Y=-0.5
LABEL      LABEL="center of 10nm gap"
LABEL      LABEL="Na = 3E18 cm^-3"
SOLVE      AC.ANALY  FREQ=1e3 VSS=0.001 TERMINAL=Dot
+          OUT.FILE=AC7  CURRENTS


COMMENT    V(Gate)=8.0
SOLVE      V(Gate1)=8.0  V(Gate2)=8.0
PLOT.1D    POTENTIA X.START=0 X.END=1 Y.START=0.495 Y.END=0.495
+          POINTS BOT=-0.6 TOP=-0. COLOR=2
+          TITLE="Potential Profile"
+          DEVICE=POSTSCRIPT PLOT.OUT=V8.ps
+          OUT.FILE=P8
LABEL      LABEL="Vg1=8.0, Vg2=8.0V"  X=0.1  Y=-0.5
LABEL      LABEL="center of 10nm gap"
LABEL      LABEL="Na = 3E18 cm^-3"
SOLVE      AC.ANALY  FREQ=1e3 VSS=0.001 TERMINAL=Dot
+          OUT.FILE=AC8  CURRENTS


COMMENT    V(Gate)=9.0
SOLVE      V(Gate1)=9.0  V(Gate2)=9.0
PLOT.1D    POTENTIA X.START=0 X.END=1 Y.START=0.495 Y.END=0.495
+          POINTS BOT=-0.6 TOP=-0. COLOR=2
+          TITLE="Potential Profile"
+          DEVICE=POSTSCRIPT PLOT.OUT=V9.ps
+          OUT.FILE=P9
LABEL      LABEL="Vg1=9.0, Vg2=9.0V"  X=0.1  Y=-0.5
LABEL      LABEL="center of 10nm gap"
LABEL      LABEL="Na = 3E18 cm^-3"
SOLVE      AC.ANALY  FREQ=1e3 VSS=0.001 TERMINAL=Dot
+          OUT.FILE=AC9  CURRENTS


COMMENT    V(Gate)=10.0
SOLVE      V(Gate1)=10.0  V(Gate2)=10.0
PLOT.1D    POTENTIA X.START=0 X.END=1 Y.START=0.495 Y.END=0.495
+          POINTS BOT=-0.6 TOP=-0. COLOR=2
+          TITLE="Potential Profile"
+          DEVICE=POSTSCRIPT PLOT.OUT=V10.ps
+          OUT.FILE=P10
LABEL      LABEL="Vg1=10.0, Vg2=10.0V"  X=0.1  Y=-0.5
LABEL      LABEL="center of 10nm gap"
LABEL      LABEL="Na = 3E18 cm^-3"
SOLVE      AC.ANALY  FREQ=1e3 VSS=0.001 TERMINAL=Dot
+          OUT.FILE=AC10  CURRENTS
```

# PUBLICATIONS AND PRESENTATIONS RESULTING FROM THIS THESIS

## Journal Publications

1. Y. A. Vlasov, X.-Z. Bo, J. C. Sturm, D.J. Norris, "On-chip natural assembly silicon photonic bandgap crystals", Nature **414**: 289-293 (2001).

2. X.-Z. Bo, N. Yao, S. R. Shieh, T. S. Duffy, J. C. Sturm, "Large-grain polycrystalline silicon films with low intragranular defect density by low-temperature solid-phase crystallization without underlying oxide", Journal of Applied Physics **91**(5): 2910-2915 (2002).

3. X.-Z. Bo, N. Yao, S. Wagner, J. C. Sturm, "Spatially selective single-grain silicon films induced by hydrogen plasma seeding", Journal of Vacuum Science & Technology B **20**(3): 818-821 (2002).

4. X.-Z. Bo, N. Yao, J. C. Sturm, "A novel method for direct TEM study of microstructure of polysilicon films crystallized with and without underlying oxide", Microscopy and Microanalysis **8** (Suppl. 2): 1210-1211 (2002).

5. X.-Z. Bo, L. P. Rokhinson, H. Yin, D. C. Tsui, and J. C. Sturm, "Nanopatterning of Si/SiGe electrical devices by atomic force microscopy oxidation", Applied Physics Letters **81**(17): 3263-3265 (2002)

6.  M. Wu, <u>X.-Z. Bo</u>, J. C. Sturm, S. Wagner, "Complementary metal-oxide-semiconductor thin film transistor circuits from a high temperature polycrystalline silicon process on steel foil substrates", IEEE Trans. Electron Devices, **49**(11): 1993-2000 (2002).

7.  <u>X.-Z. Bo</u>, L. P. Rokhinson, D. C. Tsui, and J. C. Sturm, "SiGe Single-Hole Transistor Fabricated by Atomic Force Microscope Nanolithography and Silicon Epitaxial Regrowth", Applied Physics Letters, (in Preparation).

## Conference Papers

8.  <u>X.-Z. Bo</u>, L. P. Leonid, H. Yin, D. C. Tsui, J. C. Sturm, "Si/SiGe nanostructures fabricated by atomic force microscopy oxidation", Materials Research Society Symposium Proceedings **686**: A6.5 (2002).

9.  <u>X.-Z. Bo</u>, N. Yao, J. C. Sturm, "Large-grain polysilicon films with low intragranular defect density by low-temperature solid-phase crystallization", Materials Research Society Symposium Proceedings **715**: A16.4 (2002).

10. <u>X.-Z. Bo</u>, L. P. Rokhinson, J. C. Sturm, "Silicon epitaxial regrowth passivation of SiGe nanostructures pattered by AFM oxidation", Materials Research Society Symposium Proceedings, **737**: E14.5 (2003).

11. X.-Z. Bo, L.P. Rokhinson, and J. C. Sturm, "SiGe Single-Hole Transistor Fabricated by AFM Oxidation and Epitaxial Regrowth", Third International Conference on SiGe(C) Epitaxy and Heterostructures, p.110-112, Santa Fe, New Mexico, Mar. 2003.

12. <u>X.-Z. Bo</u>, L. P. Rokhinson, D. C. Tsui, and J. C. Sturm, "SiGe single-hole transistor fabricated by AFM oxidation and epitaxial regrowth", Device Research Conference, **61**: 129-130 (2003).