NOVEL APPROACHES TO AMORPHOUS SILICON THIN FILM TRANSISTORS FOR LARGE AREA ELECTRONICS

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A DISSERTATION

PRESENTED TO THE FACULTY

OF PRINCETON UNIVERSITY

IN CANDIDACY FOR THE DEGREE

OF DOCTOR OF PHILOSOPHY

RECOMMENDED FOR ACCEPTANCE

BY THE DEPARTMENT OF

ELECTRICAL ENGINEERING

Adviser: James C. Sturm

November 2011

Abstract

While scaling VLSI devices to ever shrinking dimensions has driven much of the improvement in performance and reduction in cost of electronic intelligence, a new set of challenges and opportunities has emerged in a drastically different regime. As systems become more and more powerful, they are no longer limited by their electronic information processing capability, but by the human-machine interface. For example, the quality and size of a video is limited by the display delivering it. Motivated by the experience of the end users, it is often desirable to make products (e.g. displays) bigger, more flexible and user friendly in general. In this regime, performance improvement and cost reduction cannot be achieved via scaling as in the traditional microelectronics field. They are achieved with novel devices structures, new materials, creative fabrication techniques and innovative functionalities. This thesis will present three such innovations in amorphous-silicon-based large area electronics.

The first is a novel amorphous silicon (a-Si) top-gate thin-film transistor (TFT) with self-aligned silicide source and drain. This structure offers performance that is on par with the best conventional bottom-gate a-Si TFTs, while providing better power efficiency and faster speed by eliminating parasitic capacitances. Furthermore, it can be fabricated with simple two-photomask process at low temperatures (~280°C), which is fully compatible with plastic substrates and less expensive than conventional fabrication processes. This device is ideal for flexible displays on future mobile computing devices. The device physics underlying this structure is explored and a model of the electron tunnel injection contact is presented.

The second is a creative fabrication technique called Self-Aligned Imprint Lithography (SAIL). Originally envisioned by HP labs, SAIL is designed to be a low-cost, high throughput way to manufacture a-Si TFT circuits. The first implementation by Hewlett Packard labs were limited bottom-gate a-Si TFTs, this thesis improved upon their work by developing a process to manufacture our top-gate a-Si TFT with self-aligned silicide source and drain. Our process involves imprinting a three-dimensional, multilayer mask structure, which replaces all photomasks

and the alignment steps. The entire device is fabricated and patterned using this single imprinted mask structure, without any additional lithography. This process is ideal for low cost and high throughput roll-to-roll fabrication of top-gate amorphous silicon TFT with self-aligned silicide source/drain on plastic substrates. The details of the process and device characteristics are presented.

The third is an innovative functionality realized in the form of a non-volatile memory transistor based on a-Si technology. The memory works based on threshold voltage shifts, which result from electrons tunneling in and out of a charge trapping medium, controlled by the applied gate voltage. This device greatly extends the functionality of a-Si TFT based circuitry, by providing fully integrated and cost effective memory. One example, demonstrated in the thesis, is a novel active matrix organic light emitting diode (AMOLED) display architecture that operates without pixel refresh and capable of non-volatile storage of images. This architecture is ideal for low power and low frame rate applications.

Acknowledgement

First of all, I would like to thank my advisor, Prof. Jim Sturm, for his constant encouragement, insightful advice and unwavering support, which were essential to the completion of this thesis. His approach to advising graduate students is not just to guide them to learn the right technical issues, but also, in his words, “to develop the right approach and the confidence in their abilities to be independent researchers”. His never subsiding enthusiasm and optimism made my time at Princeton both enjoyable and fruitful.

I would also like to thank Prof. Sigurd Wagner for the numerous discussions and the invaluable advice and help that I received from him throughout my studies at Princeton University. Also, I greatly appreciate the time spent by Prof. Claire Gmachl and Prof. Andrew Houck for reading this thesis and their valuable comments. I would also like to thank Prof. Sigurd Wagner, and Prof. Stephen Lyon for taking time to serve on my FPO committee.

I would like to thank the present and former members of Prof. Sturm’s and Prof. Wagner’s labs particularly those involved in the large-area projects for their help and cooperation: Hongzheng Jin, Alex Kattamis, Kuni Cherenack, Prashant Mandlik, Bahman Hekmatshoar, Lin Han, Elisabeth Lausecker, Ting Liu, Bahdri Lalgudi and Noah Jafferis. I am also grateful to the other lab members for their help along the way: Kun Yao, Keith Chung, Weiwei Zheng, Sushobhan Avasthi, Jiun-yun Li, Oliver Graudejus, Jane Leisure, Wenzhe Cao and many others. Special thanks to Bahman Hekmatshoar, Lin Han, Ting Liu and Bhadri Lalgudi for their help with the lingering repair and maintenance work on the PECVD tool. I would also like to thank the staff members of PRISM cleanroom, Helena Gleskova, Joe Palmer, Pat Watson and Mike Gaevski for their great efforts to keep the cleanroom up and running. I also appreciate all the help from PRISM and ELE staff, Sheila Gunning, Carolyn Arnesen, Sarah Braude, Roelie Abdi and many others.

Finally, I want to thank my parents for their love, encouragement and support throughout all my years at Princeton.

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Introduction

1.1. Motivation

A good way to understand the motivation behind research in the field of large area electronics is to examine the two extremes of the electronic device scaling. Figure 1.1 depicts this dichotomy with one example from each end of the spectrum. In the small extreme, there is the Intel core I7 processor. It packs over 730 million transistors in merely 263mm^2. With 4 cores and a CPU clock rate up to 3GHz, it is one of the most powerful microprocessors for personal computing on the market. Yet it retails for only about $300. This high performance and low cost have been enabled, in large part, by the continued down-scaling of the device dimension. As the transistor lengths are reduced, the devices run faster and dies get cheaper. As such, in the regime of the I7, smaller is better. This not true, however, at the other extreme of device scaling. As Sharp has shown with their impressive 108” liquid crystal display (LCD) TV, which has an area of over 4 million mm^2 and only about 40 million transistors (a difference in transistor density of ~6 orders of magnitude), bigger is better. This is because LCD is the interface between electronic data and the human user. In this regime, it is the user experience that defines the metrics by which devices, like the LCD, are measured. As a result, it is often desirable to make the devices larger, more flexible, more stretchable, and just more user-friendly in general. With a different set of constraints and priorities in the regime of large-area electronics, down-scaling device dimensions is no longer a useful tool for improving performance and reducing cost. We must look for performance and cost drivers in different places, including novel device structures, creative fabrication techniques, and innovative functionalities. Efforts to discover these drivers are the essence of large-area electronics research.

1.2. Amorphous silicon for large area electronics

Hydrogenated amorphous silicon (a-Si:H) has proved to be the material of choice for large-area electronics for four main reasons. Amorphous silicon has all the useful properties of a

semiconductor including doping, photoconductivity, field-effect modulation of conductivity, junction formation and etc. The plasma-enhanced chemical vapor deposition (PECVD) process allows for low cost and uniform growth of material over large areas. Having similar chemical and atomic structure to crystalline silicon, amorphous silicon device fabrication can take advantage of the extensive knowledge for crystalline-silicon-based processing developed through the microelectronics industry. Lastly, the PECVD process used to deposit amorphous silicon can be easily applied to the deposition of a diverse set of alloy materials which provide dielectrics, passivation layers and semiconductors with different bandgaps needed for electronic device applications. For these reasons amorphous silicon is widely used in active matrix liquid crystal displays [1], scanners [2], position sensors [3], medical imagers [4], and solar cells [5].

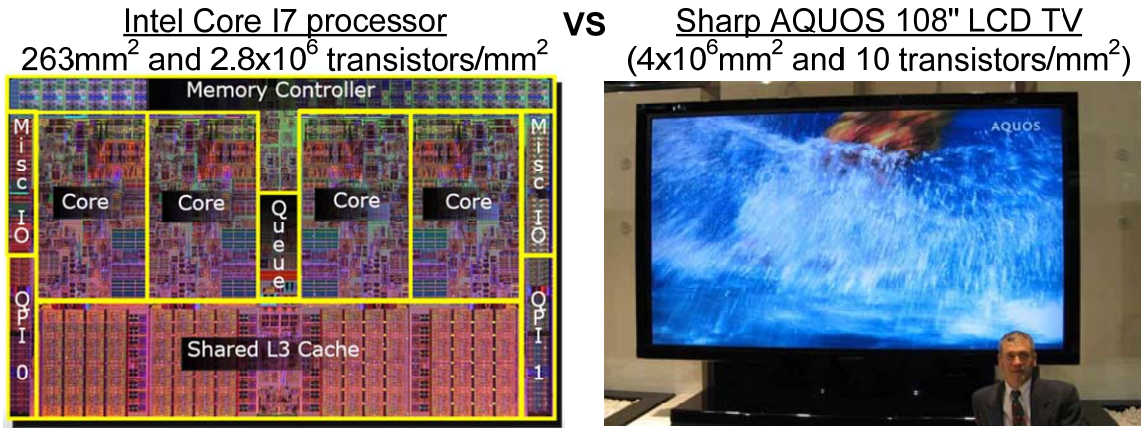

Figure 1.1. Comparison between the two extremes of electronic device scaling.

1.3. Organization of thesis

This thesis will focus on the exploration of novel device structures, creative fabrication techniques, and innovative functionalities for the purpose of enhancing performance and reducing cost of amorphous-silicon-based large-area electronics.

Chapter 2 provides an overview of the basic properties of the amorphous silicon, including atomic structure, electronic structure, transport mechanisms and doping. The plasma-enhanced chemical vapor deposition of amorphous silicon and related alloys are reviewed. The structures of the amorphous silicon TFT and the principles of its operation are briefly discussed.

Chapter 3 is focused on a novel a-Si TFT structure that provides power and speed performance that are superior to the conventional a-Si TFT. The fabrication process and device physics are explored in detail. Compatibility with flexible substrates is also demonstrated.

In Chapter 4, a creative fabrication technique call self-aligned imprint lithography is demonstrated for the fabrication the top-gate amorphous silicon TFT. The potential of this technique to enable low-cost and high throughput fabrication of a-Si circuitry on flexible substrates is explained. The details of the fabrication process and device characteristics are also presented.

In Chapter 5, the development of an innovative functionality of the amorphous silicon TFT as a non-volatile memory is explored. The existing non-volatile memory technologies are briefly reviewed, and found unsuitable for direct integration into large-area electronics applications. The floating-gate amorphous silicon TFT is successfully demonstrated as a non-volatile memory device, which can potentially be directly integrated into amorphous-silicon-based large electronics with a little incremental cost. However, it previously suffered from undesirable drain-voltage-dependences and short retention time. The mechanisms behind the shortcomings of the floating gate TFT are explained and a new device structure is proposed to address them. The characteristics of the new devices structure are studied in detail.

In chapter 6, a novel active matrix organic light emitting diode (AMOLED) display architecture enabled by the a-Si TFT non-volatile memory is presented. The new architecture addresses the problems of the conventional AMOLED of needing excess refresh cycles to maintain a static image, and provides a potentially low power alternative for low-frame applications.

Finally, a summary of this thesis is presented in Chapter 7. Future research directions based on this work are also suggested.

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Amorphous silicon thin film transistors

The amorphous silicon (a-Si) thin film transistor (TFT) was first demonstrated in 1979 by LeComber and Spear [1]. These devices took advantage of the capability to deposit and process a-Si over large areas to dominate applications such as active-matrix liquid crystal display (AM-LCD), optical scanners and radiation imagers. As such, they became the workhorse of what is now the field of large-area electronics. In this chapter, a brief overview of the basic properties of a-Si is presented. The plasma enhanced chemical vapor deposition technique used to grow the a-Si material is also introduced and explained. Lastly, the structure and principle of operation of the a-Si TFTs are discussed.

2.1. Basic properties of hydrogenated amorphous silicon

Prior to the 1960s, amorphous silicon was prepared by sputtering or thermal evaporation. This type of amorphous silicon does not contain hydrogen, and has a very high density of dangling bonds that prevented doping, photoconductivity and other desirable characteristics of a useful semiconductor material. In 1969, Chittick and coworkers succeeded in making hydrogenated amorphous silicon through glow discharge of silane (SiH_4) gas [2]. The hydrogen passivated the dangling silicon bonds in the a-Si material, and significantly reduced the defect density. This enabled a fairly high carrier mobility [3] and also strong photoconductivity [4], making hydrogenated amorphous silicon (a-Si:H) a useful semiconductor. Because of its superior properties, amorphous silicon is almost always used in the hydrogenated form. For simplicity's sake, all occurrences of amorphous silicon or a-Si from this point forward will be referring to hydrogenated amorphous silicon (a-Si:H).

2.1.1. Atomic structure

The atomic structure of amorphous silicon is shown in Figure 2.1. As mentioned before, the hydrogen atoms in the amorphous lattice play a crucial in passivating the silicon dangling

bonds and reducing defect density. Because of their presence, almost all the Si atoms in the amorphous lattice are four-fold coordinated (four bonds per atom), just like in crystalline silicon.

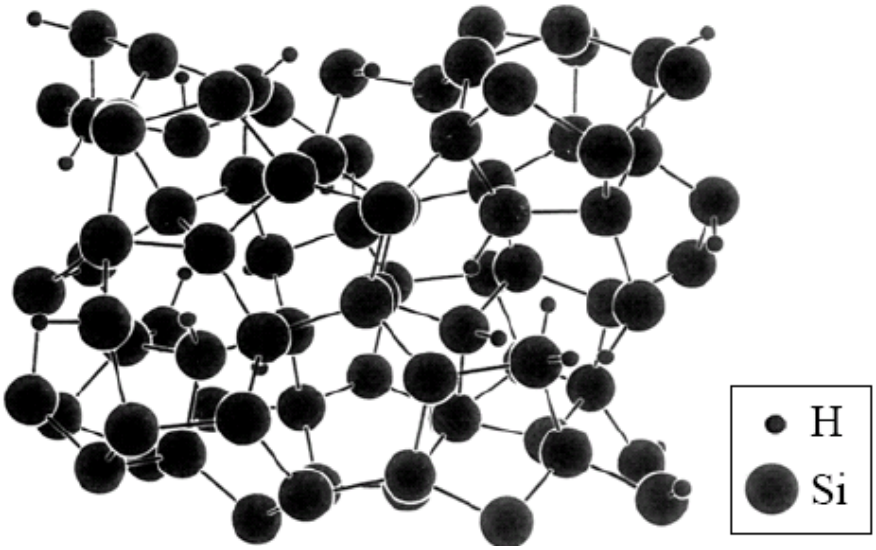

Figure 2.1. The atomic structure of hydrogenated amorphous silicon [5].

While not organized in a perfect crystal lattice, a-Si is not completely disordered. The covalent bonds between silicon atoms are very similar to crystalline silicon, with average bonding angle and length only differing about 10% and 1% from crystalline silicon values, respectively [5]. As such, amorphous silicon has similar short range order as crystalline silicon, but lacks the long range periodicity. This structural disorder influences the electronic and optical properties of a-Si in significant ways. The distortion in bond lengths and bond angles broadens the distribution of states and causes carrier localization and strong carrier scattering, which reduces the effective carrier mobility. Structural defects such as broken bonds result in electronic defect states that lie in the middle of the a-Si bandgap. The possibility of alternative bonding configurations within the amorphous lattice lead to metastable electronic states.

2.1.2.Electronics structure

There has been considerable debate over the reasons why a-Si has a bandgap given its lack of long range disorder. However, if we consider the origin of the bandgap in semiconductors through the principle of linear combination of atomic orbitals, the answer is clear. When two Si

atoms are brought close together, their electron orbitals or electron wave functions interact to form the sp^3 hybridized covalent bond. This interaction results in the splitting of the single orbital into a bonding orbital with lower energy than the original orbital and an anti-bonding orbital with energy higher than the original orbital. The energy difference between the bonding and the anti-bonding orbital gives rise to the forbidden gap that separates the allowed energy states, which are the bonding and anti-bonding orbitals. Since a-Si has covalent bonds that are very similar to crystalline silicon, it will therefore have the same splitting of orbitals and a similar bandgap between the bands of allowed energy states. The lack of long range disorder is simply a small perturbation in the linear combination of atomic orbital, as the electron wave functions of the nearest neighbors have the highest contribution.

In crystalline silicon with well-defined periodicity, solutions to the Schrodinger's equation using the Bloch theorem shows that the wave functions of the electrons in the covalent bonds extend throughout the crystal and have coherent phases at the different lattice sites. As such they are "extended" states that can be anywhere in the crystal and have a precise lattice momentum vector, k. Furthermore, there is an abrupt transition between the forbidden gap and the allowed energy of the extended states described by the E(k) dispersion relationship. These solutions do not apply to a-Si because it has no long range periodicity. The standard treatment for a-Si assumes that the distortions can be modeled by imposing a random potential with average amplitude V_0 to the array of identical atomic potential wells representing crystalline silicon (Figure 2.2) [6]. It has been shown that when V_0/B exceeds a critical value (~3), there is zero probability for an electron at any particular site to diffuse away, where B is the bandwidth of the allowed band of energy states resulting from covalent bonding in the lattice [6]. In such a case, all the electrons would be localized and there can be no electrical conduction.

In crystalline silicon, the bandwith B is approximately 5eV, and therefore a distortion on the order 15eV would be necessary to localize all electronic states in a-Si. Because of the short range order in a-Si, the distortions tend to be very small perturbation to the lattice potential. As a result, the condition for localization of all electronic states is not met in a-Si. However, even when the disorder is insufficient to meet the localization criterion, it has been shown by Mott that

localized states exist in the band of a-Si [7]. The localized states lie near the edges of the bands, because they tend to be states whose energies get affected by bigger potential perturbations. The extended states, on the other hand, are primarily in the center of the bands. The extended states and localized states are separated by the mobility edges at energy E_c in the conduction band and E_v in the valence band, which are so named because at zero temperature only carriers above E_c and below E_v are mobile and can contribution to conduction [7]. The energy difference between the two mobility edges is often referred to as the mobility gap, and is typically about 1.8eV [5]. The localized states below E_c and above E_v are often referred to as the band tail states and they are generally assumed by exponentially distributed in energy [8][9]. In reality, the density of states in the band tails are not strictly exponential, but the departure is small enough to be negligible in the first order [10][11].

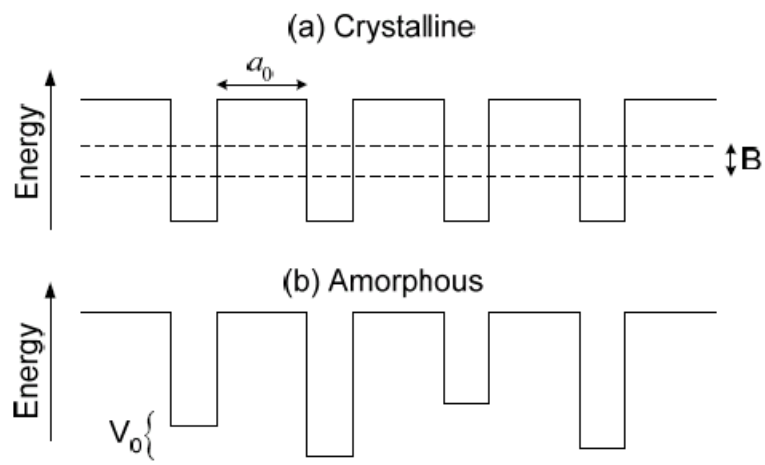

Figure 2.2. The Anderson model of the potential wells for (a) crystalline silicon and (b) amorphous silicon [5].

Given the above discussion, the band structure of a-Si can be schematically represented as in Figure 2.3. The defect states in the middle of the gap are associated with the unpassivated dangling bonds and band tails are associated with the bonding-disorder-induced localized states. The density of midgap defects in a-Si is relatively low (on the order of ~$10^{15}cm^{-3}$) due to the presence of hydrogen passivation. As a result, most of the carrier transport and optical properties of the material are determined by the band tails states.

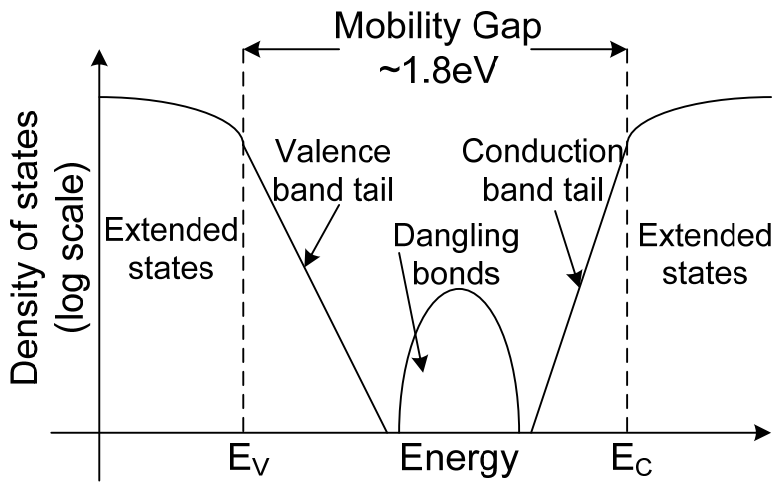

Figure 2.3. The density of electronic states in amorphous silicon.

2.1.3.Transport mechanisms

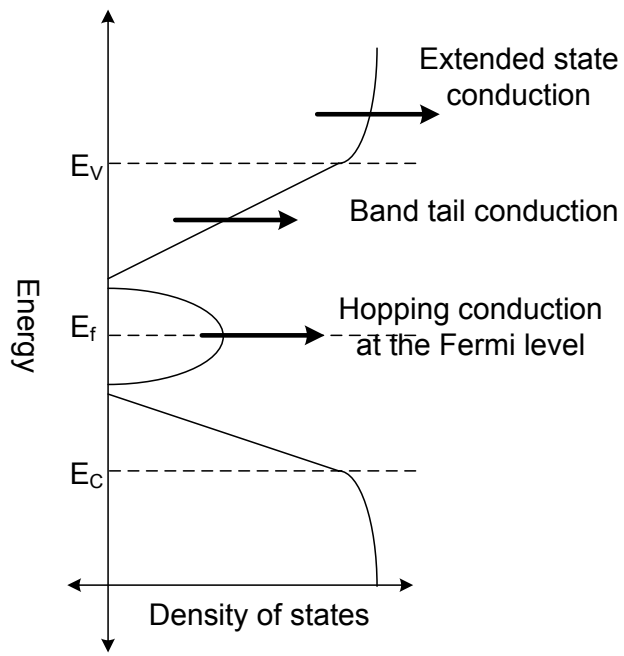

Figure 2.4. The three main mechanisms of transport in amorphous silicon.

Because there are significantly more valence band tail states than conduction band tail states, hole transport is much less efficient than electron transport in a-Si. Therefore, we will focus our discussion on electron transport. The three main mechanisms for electron transport in

a-Si are schematically illustrated in Figure 2.4. Extended state conduction occurs via mobile electrons which are thermally activated into extended states with energy higher than the mobility edge. Localized state conduction occurs via electrons hopping from one localized state to another under elevated temperatures. Hopping conduction at the Fermi level occurs via tunneling of electrons from one mid-gap defect state to another under conditions of high carrier density.

Extended state conduction

Conduction by thermal activation of carriers from E_f to above the mobility edge follows the relation

$$\sigma_{ext} = \sigma_{oe} e^{\left[\frac{(E_C - E_f)}{kT}\right]} \qquad (2.1)$$

where σ_{oe} is the average conductivity above the mobility edge (about $100\Omega^{-1}cm^{-1}$) [5]. The activation energy is the separation between E_C and E_f and varies from ~1eV in undoped a-Si to about ~0.1eV in n-doped a-Si. It is not possible to raise E_f any closer to the mobility edge by doping or by field effect modulation (e.g. increasing the gate voltage on an a-Si transistor), because the high density of band tail states would pin the Fermi level at 0.1eV below the mobility edge [5].

The electron mobility of the extended states in a-Si is much lower than that of crystalline silicon, which is ~$1000cm^2V^{-1}s^{-1}$. There two effects that reduce the mobility in a-Si. One is the fact that disorder in the lattice potential has the effect of scattering electrons. Under conditions of weak scattering, the band mobility μ_0 is given by:

$$\mu_0 = \frac{e\tau}{m} = \frac{eL}{mv_c} \qquad (2.2)$$

where τ is the scattering time, L is the mean free path, m is electron effective mass and v_c is the electron thermal velocity. In crystalline silicon the scattering length is about 1000Å, and in a-Si the mean free path is reduced to about one to two inter-atomic distances. This translates to a band mobility μ_0 of about 5-10 $cm^2V^{-1}s^{-1}$. The second mobility reducing effect is the trapping of electrons in localized band tail states during transport (Figure 2.5). As a result, the apparent drift mobility μ_d is the band mobility μ_0 reduced by the fraction of time the electron spends immobilized in the traps [5]:

$$\mu_d = \mu_0 \frac{\tau_{free}}{\tau_{free} + \tau_{trapped}} \quad (2.3)$$

Statistically speaking, this is equivalent to the band mobility reduced by of the carriers trapped in localized states at any given time:

$$\mu_d = \mu_0 \frac{n_{free}}{n_{free} + n_{trapped}} \quad (2.4)$$

This fraction has been estimated to be approximately 0.1 in a-Si [5]. Therefore the apparent drift mobility for electron conduction in the extended states in a-Si is approximately 0.5-1 $cm^2V^{-1}s^{-1}$.

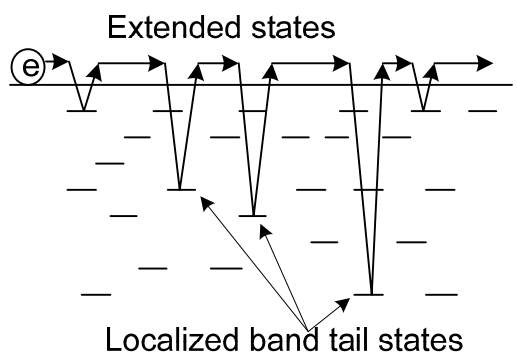

Figure 2.5. Trapping of electrons by localized band tail states during transport.

Band tail conduction

Although the electrons in the localized band tail states are immobile at zero temperature, the tunneling transition between neighboring states of differing energies can give rise to conduction at elevated temperatures. The spatial overlap of the wave functions allows for tunneling between neighboring states to occur as illustrate in Figure 2.6. For states 1 and 2 separated by distance R and energy different E_{12}, the probability for tunneling between from 1 to 2, and vice versa are [5]:

$$P_{12} = \omega_0 e^{-2R/R_0} e^{-E_{12}/kT} \quad (2.5)$$

$$P_{21} = \omega_0 e^{-2R/R_0} \quad (2.6)$$

where ω_0 is the tunneling attempt frequency and R_0 is the localization length. ω_0 has an approximate value of $10^{13}s^{-1}$ [5]. R_0 varies with the binding energy of the state from approximately 5Å to 10Å. Because of the exponential dependence on R_0 of the tunneling probability, tunneling

can only effectively occur for $R < 10R_0$, which is about 50-100Å. Therefore this tunneling conduction can be significant whenever the density of localized state exceeds $10^{18}cm^{-3}$.

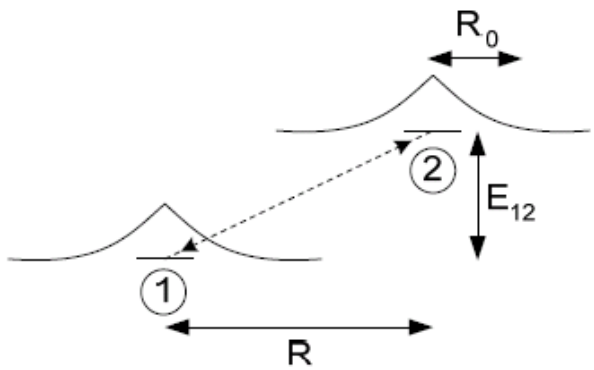

Figure 2.6. model of tunneling between two neighboring localized states.

Hopping conduction at the Fermi level

Hopping conduction occurs between neighboring mid-gap defect states via tunneling, similar to band tail conduction. Therefore, it is also strongly dependent on the defect density. Since the density of midgap defects tend to be low due to hydrogen passivation in a-Si, the contribution of hopping conduction at Fermi level to overall transport is usually negligible. However, it does present a lower bound for the transistor leakage current.

2.2. PECVD growth

Plasma-enhanced chemical vapor deposition (PECVD) is the dominant technique used today for the growth of a-Si and amorphous insulator materials used in large-area electronics applications. The first demonstration of this growth technique in 1969 represented a major breakthrough for a-Si because it allowed for the incorporation of hydrogen into the deposited film, which dramatically reduced the defect density of a-Si. Its relatively low processing temperature and ability to produce uniform growth over large areas has led to widespread adoption by display and photovoltaics industries.

A new technique named hotwire CVD (HWCVD) has since been developed as an alternative to PECVD [12][13][14]. Its main advantage lies in the ability to avoid in-situ plasma damage of the deposited films. Therefore, it can produce films with lower defect density. However,

HWCVD is much more limited in deposition area scale-up than PECVD. As a result, it is mostly a research technique and not used in industrial applications.

The work in this thesis was performed using PECVD and therefore the discussion in the following section will focus the PECVD technique.

2.2.1. Basic concepts

As the name implies, the driving force behind PECVD is the plasma. The plasma is created in a gaseous precursor by the application of a large electric field. The electric field ionizes the gas molecules creating electrons and ions. Because of their smaller mass, the electrons are accelerated to high speeds by the applied field. The high speed electrons can then impart their large kinetic energy to other gas molecules via collision. These collisions create more excited electrons and ions, as well as highly reactive neutral species. The colored glowing that is characteristic of the plasma is associated with release of photons during the relaxation of gas molecules and ions from the excited states. The excited electrons and ions sustain the collision and excitation processes, while the highly reactive species, also known as radicals, are responsible for the growth on the substrate surface. The substrate and the reaction chamber is often heated to moderate temperatures (150°C - 400°C) to aid the dissociation of the precursor gases and increase the surface mobility of the radicals on the growing surface. The properties of the material deposited via PECVD depend the substrate temperature, precursor gas composition and flow rate, chamber pressure and applied electric field [5].

2.2.2.Overview of Princeton tool

The PECVD machine used in Princeton for the deposition of a-Si and related semiconductor/insulator materials is a four-chamber cluster tool. To minimize cross-contamination between the various materials, it has a chamber for the deposition of intrinsic semiconductor films, a chamber for the deposition of doped semiconductor films, a chamber for the deposition of insulator films and a load lock chamber to minimize air exposure of the deposition chambers. The schematic cross section of one of the PECVD chambers is shown in

Figure 2.7. The chamber is kept under high vacuum (10^{-6}Torr) by a turbo molecular pump when there are no active deposition processes running. During depositions the gate valve is closed, sealing off the turbo molecular pump from chamber. The inlet and process valves are opened to allow the process gases to enter and leave the deposition chamber. The flow rate of the precursor gases are set by an array of mass flow controllers calibrated for the specific gases. The gas pressure within the chamber is set by a PID-controlled butterfly valve that regulates the rate of exhaust. The temperature of the chamber and substrate is set using three independent resistive heaters controlled by external PID controllers.

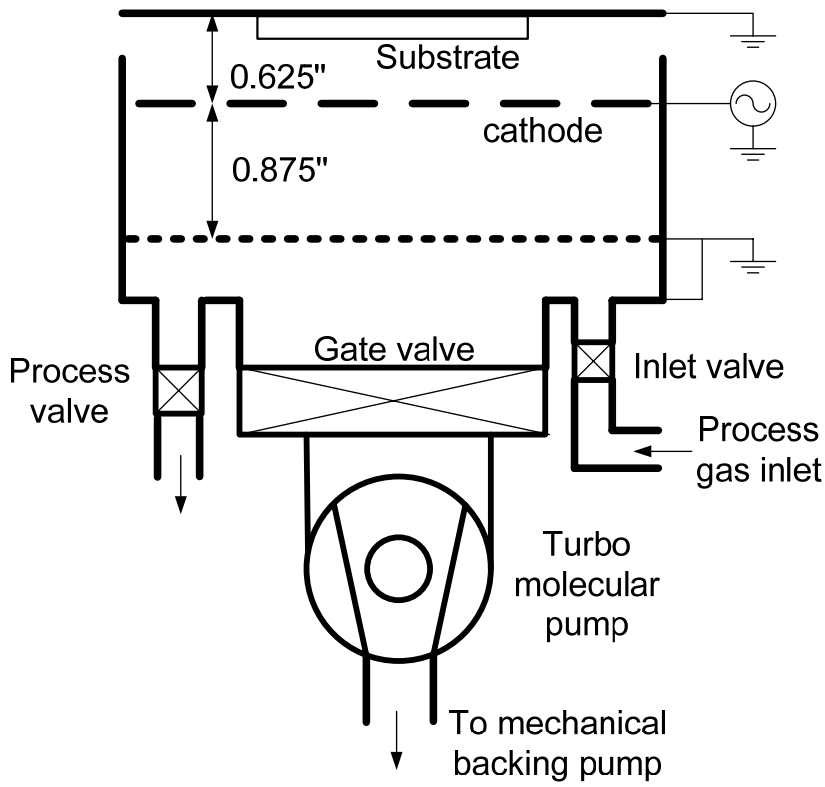

Figure 2.7. Schematic of one of the Princeton PECVD chamber. The cathode and bottom electrodes have shower head configurations with different sized openings, illustrated with different dashed lines.

The plasma is created in the reaction chamber by applying a RF (13.56MHz) signal to the cathode, while grounding the top and bottom anodes. The spacing between the bottom electrode and the cathode is 0.875” and the top anode (substrate holder) is 0.625” above the cathode. The cathode has an area of 225cm^2. The three-electrode (also known as triode) configuration is

design to generate plasma primarily between the bottom electrode and the cathode. This minimizes in-situ ion bombardment of the growing film surface. The reactive species are created in the plasma, they then diffuse through the holes in the cathode to reach the substrate. Both the cathode and bottom anode have a shower head profile (uniformly distributed openings throughout the surface of the electrode) that promote uniform introduction of source gas to the plasma and uniform distribution of reactive species to the substrate.

2.2.3. Growth mechanism of amorphous silicon

Intrinsic films

Intrinsic a-Si is used as the channel material in a-Si TFTs. PECVD growth of this material is done with pure silane gas (SiH_4). Without the plasma, temperatures higher than 450°C would be necessary to decompose Silane to form the necessary reactive species. At these elevated deposition temperatures, hydrogen is released from the a-Si, and resulting material has very high defect densities. As a result, PECVD growth of a-Si is typically done at around 250°C, with the plasma providing the necessary energy to decompose silane. The dominant silane decomposition reactions (the ones that require the lowest decomposition energy) in PECVD growth are [17]:

$SiH_4 \rightarrow SiH_2 + H_2$ 2.2eV

$SiH_4 \rightarrow SiH_3 + H$ 4.0eV

$SiH_4 \rightarrow Si + 2H_2$ 4.2eV

Various other dissociation reactions are also possible during PECVD growth of a-Si using silane. For example, the silane molecules may also react with the radicals produced by the dissociation reaction to form larger molecules such as Si_2H_6 and Si_3H_8, which may in turn decompose and form additional radicals [15]. Given that the mean free path the radicals and gas molecules are on order of ~100μm at the typical deposition pressures (0.1-1Torr), the probability of collision and secondary reactions is very high. As a result, it is rather difficult to clearly identify the key radicals and the associated reactions responsible for the growth of a-Si [16]. However, it is believed that at the relatively low RF power density used during PECVD of a-Si, SiH_3 radicals are responsible for material growth [18][19]. The process by which growth is believed to occur at the surface of a-

Si via SiH_3 radical is schematically illustrated in Figure 2.8. The growing surface of a-Si is generally hydrogen-terminated, and as such the SiH_3 radical is not able to directly bond to the surface. A silicon dangling bond must be made available by the release of H_2 from either incoming H radical reacting a surface H-termination or two surface H-termination reacting with each other. Then, the SiH_3 radical is then able to attach to the free silicon dangling bond and add to the growth of a-Si.

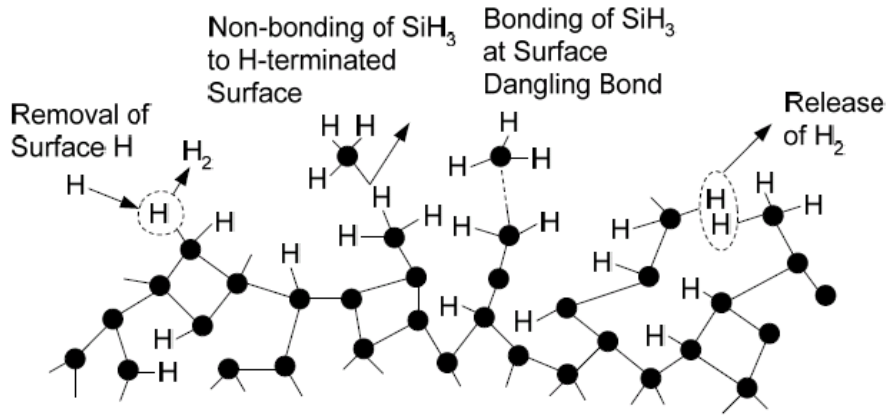

Figure 2.8. a-Si growth via SiH_3 radicals [20].

The dependence of a-Si material properties on the deposition condition is shown in Figure 2.9. The optimum deposition temperature is between 200°C and 300°C [21]. Lower deposition temperature leads to low surface mobility of the reactive radicals at the growth surface, which results in a large number of highly strained and broken bonds in the a-Si. Higher deposition temperature leads to loss of hydrogen passivation in the film, which also results in high defect density. The defect density in a-Si also increases with increasing RF power density of the plasma. This is generally attributed to the in-situ ion bombardment of the growth surface. One way to reduce ion bombardment is to use a three electrode configuration, like the one in the Princeton PECVD system, which keeps the plasma away from the growth surface. Another way to reduce defect density is to reduce RF power density of the plasma, but that also reduces the growth rate of a-Si, which results in higher cost for the material. There is also a minimum threshold for power density, below which it is not possible to create the ionization reactions necessary to sustain the

plasma. Therefore, there is trade-off between defect density and practical constraints on PECVD plasma power density.

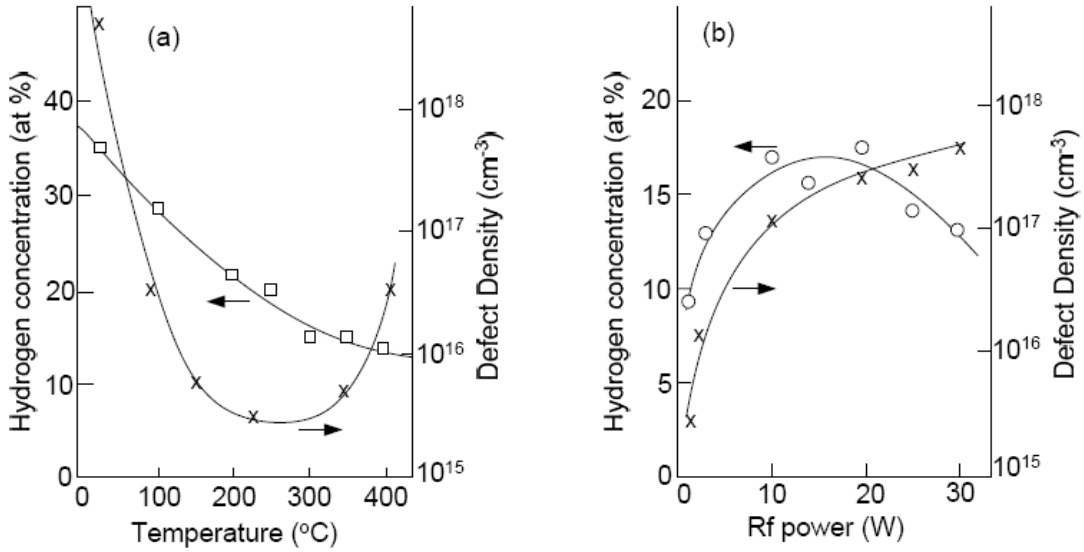

Figure 2.9. The effect of substrate temperature (at RF power = 4W) and the effect of RF plasma power (at T = 250°C) on defect density and hydrogen concentration of PECVD a-Si [21].

Silane gas is often diluted with hydrogen gas in the plasma to change the growth condition and material properties of a-Si. Hydrogen is the most widely used to improve the stability of a-Si for solar cell applications [22][23]. Hydrogen has also been reported to reduce the defect density in a-Si grown at temperature <200°C, which is important for applications using plastic substrates with low working temperature [24][25][26]. Most recently, hydrogen has been shown to reduce threshold voltage instability in a-Si TFTs [27]. Because of these observations, hydrogen dilution is believed to promote the formation of “strong” bonds and energetically favorable amorphous networks.

Doped films

Substitutional doping in c-Si is made possible by the constraint of the periodic lattice. The dopant atom (e.g. boron or phosphorous) is forced to conform to the lattice coordination and take on the 4-fold coordination like the Si atom. This leaves a free electron in the anti-bonding orbital in the case of phosphorous and an unoccupied bonding orbital state in the case of boron, which result in additional free carriers. In the case of a-Si, there is no periodicity to force the dopant

atoms to take on a 4-fold coordination and create free carriers. However, substitutional doping is still possible due to a “defect compensation” effect in a-Si [28]. While it is not energetically favorable for a dopant atom to take on a 4-fold coordination in the amorphous network, the pair of a 4-fold coordinated dopant atom and a dangling bond defect is a much lower energy configuration. This gain comes from the transfer of the free electrons in the anti-bonding orbital to the defect state (in the case of a phosphorous dopant) or the transfer of the single electron in the defect state to the unoccupied bonding orbital (in case of a boron dopant). However, the energy of the dopant-defect pair is still slight higher than that of a 3-fold coordinated (inactive) dopant. Therefore, while substitutional doping is possible in the form of dopant-defect pairs, the fraction of activated dopant atoms to total incorporated dopant atoms is low. Furthermore, doping also increases the defect density in a-Si by an amount roughly equal to the activated dopant density.

Doped a-Si films are used as the contacts for a-Si TFTs. Doping of plasma deposited a-Si is done by adding phosphine (PH_3) and diborane (B_2H_6) to silane as precursor gases. The dopant gas molecules are dissociated by the plasma, like Silane, forming reactive radicals and ions that bond to the growing surface. The concentration of activated dopants (or 4-fold coordinated impurities) and therefore conductivity of the film is roughly proportional to the square root of the molecular concentration of the dopant gas (e.g. $[PH_3]/[SiH_4+PH_3]$) up to 1% [5]. The conductivity and free electron density of an n+ doped film at room temperature is typically around10^{-2} $(\Omega cm)^{-1}$ and $10^{18}cm^{-3}$ for a dopant gas concentration of 1%. For activated dopant concentration great than 1%, the conductivity saturates due to increase in defect densities that causes in wider band tails and lower mobility [5]. Typical concentrations of dopant gas for deposition of n^+ and p^+ a-Si are on order of a few ppm.

2.2.4. Growth mechanism of SiN_x dielectric

Silicon nitride (SiN_x) is used as the gate insulator in a-Si TFTs. Growth with PECVD is typically done with a mixture of silane and ammonia. Like a-Si, PECVD SiN_x also incorporates a significant amount of hydrogen into its amorphous network, which again has the effect of passivating defects. The ratio of nitrogen to silicon (N-to-Si ratio) in PECVD SiN_x can deviate from

the standard 4 to 3 stoichiometric ratio depending on the deposition condition and ratio of precursor gases. Films with N-to-Si ratio higher than 4 to 3 are called nitrogen-rich and films with N-to-Si ratio lower than 4 to 3 are called silicon-rich. Nitrogen-rich gate SiN_x are known to provide better TFT characteristics, such as sharper subthreshold slope and less threshold voltage shift [30][31].

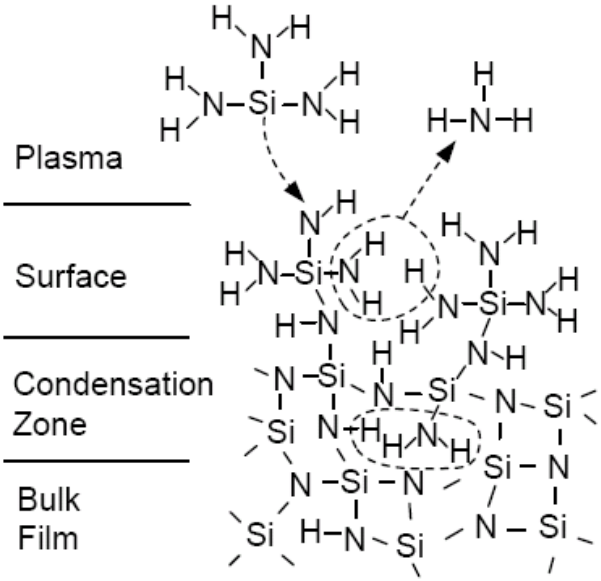

Figure 2.10. Model of the PECVD growth of SiNx [32].

Direct mass spectroscopy methods used to study the active species in the plasma during PECVD of SiN_x have shown that the dominant reactive radicals in the plasma are $(SiH_3)_2$ (disilane) and $Si(NH_2)_3$ (triaminosilane) [32] . The ratio of triaminosilane to disilane concentrations in the plasma is observed to increase with increasing RF power, along with an increase in growth rate of the SiN_x film. This correlation suggests that the triaminosilane radical is directly involved in the growth of SiN_x. The reactions by which growth via triaminosilane occur has been proposed to be:

$SiH_4 + 4NH_3 \rightarrow Si(NH_2)_3 + 4H_2$

$Si(NH_2)_3 \rightarrow Si_3N_4 + 8NH_3$

The first reaction represents the formation of the dominant reactive radical responsible for growth in the plasma. The second reaction represents the condensation reaction that bonds the radical to the growing surface. It involves the formation and evolution of NH_3 from the nitrogen and

hydrogen atoms at the surface to free up a Si bond. The triaminosilane radical then attaches to the dangling Si bond and adds to the growing film. This sequence is schematically illustrated in Figure 2.10.

2.3. Thin film transistor structures

Unlike the VLSI field effect transistor where the channel material is doped to control the threshold voltage of the device, a-Si thin film transistors (TFTs) use intrinsic channel material. The main reason behind this is the fact that doping increases defect density and reduces mobility of carriers in the amorphous semiconductor. Also, the resistivity of the intrinsic a-Si is high enough to keep the drain-source leakage current low, without a reverse biased substrate-drain junction. It was noted earlier that because the wider valence band tail, hole mobility is about 100 times smaller than electron mobility in a-Si. As a result, all a-Si TFTs are n-channel devices working in accumulation mode.

2.3.1. Bottom-gate devices

The most widely used a-Si TFT structure in industry is today is the bottom-gate staggered TFT. This structure also has two different flavors – back-channel etched (BCE) and back-channel passivated (BCP). The cross sectional schematic of these two structures are shown in Figure 2.11.

PECVD SiN_x has been shown to provide the best semiconductor-to-insulator interface to a-Si in the bottom-gate structures. TFTs made with PECVD SiN_x as the gate dielectric generally outperform other candidates such as PECVD silicon oxide or atomic-layer deposited aluminum oxide. This is why PECVD SiN_x is the gate dielectric of choice in most industrial applications of a-Si TFT.

In BCE TFTs, the metal gate electrode is deposited and patterned first, at the bottom of the TFT. As such, they are inverted from conventional VSLI transistor structure. The gate dielectric is deposited on top the gate electrode. This is followed by the deposition of intrinsic a-Si channel material, doped a-Si and metal contact layers. The active area of the TFT is patterned to

isolate individual devices. The metal layers and then the doped a-Si are patterned to define source and drain contacts of the transistor. This structure is called back-channel etched because the n+ a-Si film is etched to expose the back (top) of the undoped a-Si channel layer. The width of the TFT is equal to the width of the source/drain contacts, and the length of the TFT is equal to the spacing between the source/drain contacts. A relatively large amount of overlap between the gate electrode and the source/drain contact is usually included to prevent device failure due to misalignment and to ensure a low resistance contact to the channel [33].

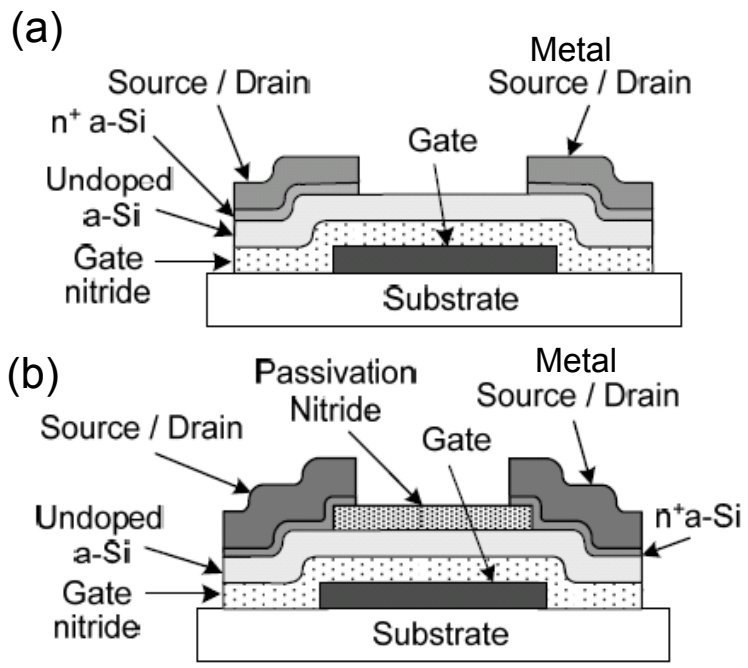

Figure 2.11. Cross section schematic of (a) back-channel etched (BCE) and (b) back channel passivated (BCP) a-Si TFT structures.

In BCP devices, the fabrication process is identical with the BCE devices up through the deposition of the intrinsic channel material. Instead of depositing the doped a-Si layer, a layer passivation SiN_x is deposited on top the intrinsic a-Si channel. The doped a-Si and metal contact layers are deposited after the passivation SiN_x is patterned. As result, the length of the channel is defined by the length of the passivation SiN_x instead of the spacing between the contacts. For more details on the fabrication processes of the BCP and BCE a-Si TFTs, refer to Appendix A.

The advantage of the BCE structure is the fact that it needs one less photolithography step than the BCP structure. Having fewer mask steps in the process significantly reduces the manufacturing cost at the industrial scale [34]. However, the BCE structure requires a thicker intrinsic channel layer because the etch used to pattern the doped a-Si layer is not selective against intrinsic a-Si. A sufficient amount of buffer is necessary to prevent channel damage due to over-etching. In the BCP structure, on the other hand, the doped a-Si etch stops on the passivation SiN_x. Therefore a much thinner a-Si can be used. A thick channel layer increases the light sensitivity of the TFT and the overall material cost of fabrication, which are not desirable for many industrial applications. Furthermore, without the passivation SiN_x, the intrinsic a-Si channel is exposed to ambient air and possible processing damages, which adversely affect the TFT threshold stability [27].

2.3.2.Top-gate devices

The top-gate staggered contact TFT structure is shown in Figure 2.12. In this structure, the source/drain metal and the doped a-Si contact layers are first deposited and patterned. Then the stack of intrinsic a-Si channel, SiNx gate dielectric and gate metal is deposited on top. Finally, the active area and gate electrode are patterned to complete the TFT.

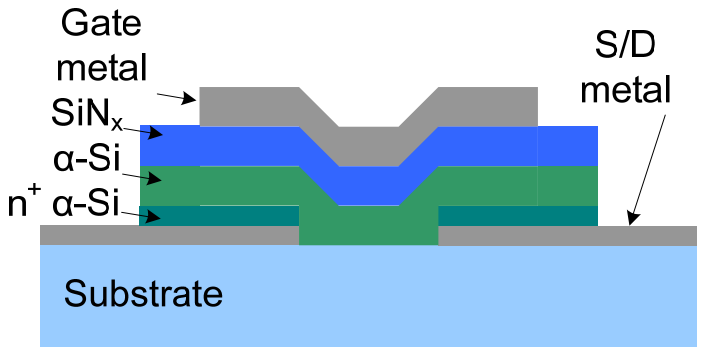

Figure 2.12. Cross section schematic of the top-gate staggered contact a-Si TFT.

There are many benefits to using a top-gate structure over a bottom gate structure including: (i) the fabrication process allows for the use of thin a-Si layer that can reduce light induced leakage current, (ii) the gate-lines, being deposited at the top of the gate insulator, can be thick to reduce the RC-delay in a large circuit applications without having to worry about step

coverage issues, and (iii) TFTs can be fabricated with a fewer number of photomask steps. Despite these attractive features, top-gate structures are not widely used today mainly because initial demonstrations of top-gate TFTs exhibited poorer electrical performance than bottom-gate TFTs [35]. This was caused by the poorer interface between the SiN_x gate dielectric and the a-Si channel in the top-gate TFTs. However, later experiments showed that it is possible to improve the interface quality in top-gate TFTs to get electrical performance comparable to bottom-gate TFTs [35]. However, by that time, the bottom-gate structure had already become the dominant technology and the top-gate structure simply fell out of favor.

2.4. Device operation and characterization

The basic operation of the a-Si TFT can be understood via a band diagram similar to that of the c-Si MOS field effect transistors (Figure 2.13). The biggest difference is that the space charge in a-Si TFT is not ionized dopant atoms, but filled midgap trap states and localized band tail states. At zero gate bias, the a-Si TFT is fairly close to the flatband condition with the Fermi level close to midgap. The drain-source current in the device, at this point, is dominated by hopping conduction at the Fermi level, which is typically low because hydrogen passivation of midgap defects. This is often referred to as the “off current” (I_{off}) of the TFT. As the gate voltage is increased, the energy bands bend downward and the Fermi level moves through the gap states. The space charge is dominated by filled gap states, and the occupancy of the band tails increases exponentially with increasing gate bias. The increase in drain-source current is due to the small fraction of the band tail electrons that are thermally excited above the mobility edge. Consequently the drain-source current also has an exponential dependence on increasing gate voltage bias. This is referred to as the subthreshold region. As the gate voltage is increased further, the Fermi level crosses a threshold where the space charge in the tail states exceeds that of the gap states and the total space charge increases linearly with the gate voltage. After this point, the free electrons above the mobility edge, and therefore the drain-source current, also increase linearly with the applied gate-source voltage. The gate voltage at which this transition occurs is called the “threshold voltage” (V_T) of the TFT. The drain-source current beyond for gate

voltage higher than V_T is called the "on current" (I_{on}). The typical drain-source current vs gate-source voltage transfer characteristics of an a-Si TFT is shown in Figure 2.14, along with the various parameters discussed above.

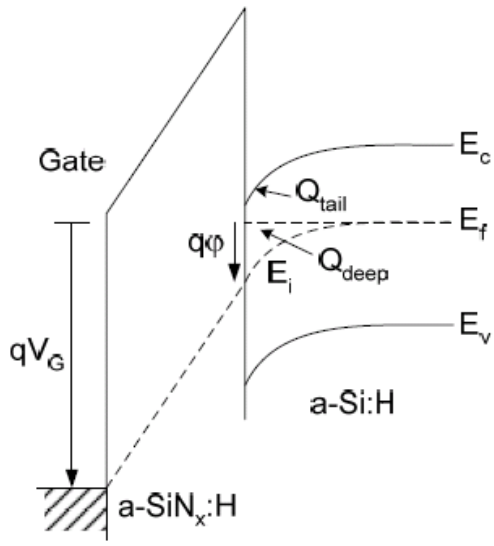

Figure 2.13. Band diagram of the a-Si TFT under positive gate voltage bias. The space charge in the a-Si is divided between tails states and midgap defect states.

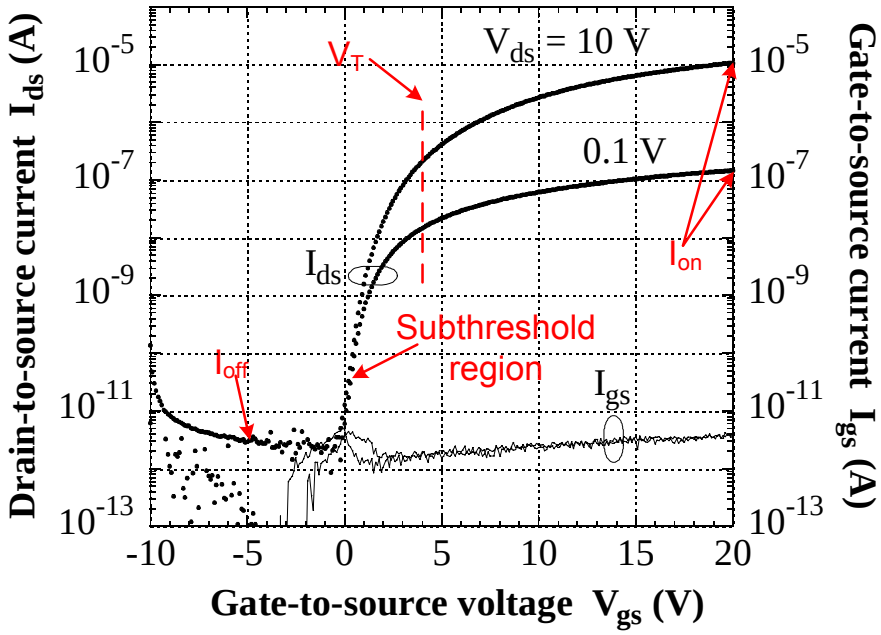

Figure 2.14. Typical drain-source current vs gate source voltage transfer characteristics of an a-Si TFT.

The field effect modulation of free electron density in a-Si TFTs is very similar to that of the c-Si MOS transistors. As such, its electrical characteristics can also be described with the conventional MOS equations:

$$I_{DS,saturation} = \frac{1}{2}\frac{W}{L}\mu_{FE}C_{SiNx}\left(V_{GS} - V_T\right)^2 \tag{2.7}$$

$$I_{DS,linear} = \frac{W}{L}\mu_{FE}C_{SiNx}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \tag{2.8}$$

where μ_{FE} is the effective field-effect mobility, V_T is the effective threshold voltage, C_{SiNx} is the capacitance of the gate dielectric SiN_x, W is the channel width and L is the channel length. V_{DS} is the drain-source voltage bias and V_{GS} is the gate-source voltage bias.

The effective field-effect mobility and threshold voltage can be extracted from the device transfer characteristics by performing least-squares linear fitting of the drain-source current to the gate-source voltage in the linear curve, and square root of the drain-source current to the gate-source voltage in the saturation curve (Figure 2.15). The transconductance obtained from the fit (slope of the fit) can be used to calculate the mobility, and the extrapolation of the fit can be used to calculate the threshold voltage using:

$$\mu_{FE,saturation} = 2\left(\frac{\partial\sqrt{I_{DS,sat}}}{\partial V_{GS}}\right)^2 \Bigg/ \left(\frac{W}{L}C_{SiNx}\right) \tag{2.9}$$

$$\mu_{FE,linear} = \frac{\partial I_{DS,lin}}{\partial V_{GS}} \Bigg/ \left(\frac{W}{L}C_{SiNx}V_{DS,lin}\right) \tag{2.10}$$

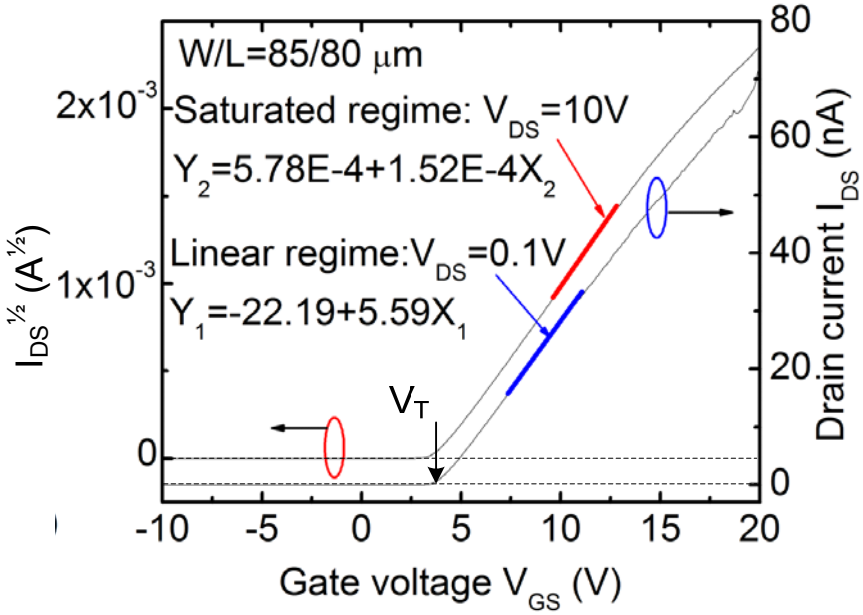

Figure 2.15. Least-squares linear fits of the linear and saturation drain-source current vs gate-source voltage curves.

Typical a-Si TFT performance metrics are summarized in Table 2.1. On/off ratio is defined as the ratio of the device on current at V_{DS} = 10V and V_{GS} = 20V, to the device off current at V_{DS} = 10V and V_{GS} = -5V.

Performance metric	Typical value
μ_{FE} (cm^2/Vs)	0.5 – 1
V_T (V)	1 – 3
Subthreshold slope (mV/dec)	300 – 1000
I_{off} (pA)	0.1 – 1
On/Off ratio	10^5 – 10^7

Table 2.1 Typical values for a-Si TFT performance metrics

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Top-gate amorphous silicon TFT with self-aligned silicide source and drain

This chapter will describe a novel top-gate device structure for an a-Si TFT. This structure provides a potentially low-cost, easy-to-fabricate method to overcome the inherent parasitic capacitances associated with the conventional bottom-gate a-Si TFT device structure. As such, it can potentially provide better performance in terms of power efficiency and speed. In the following sections, the inherent challenges associated with the conventional a-Si TFT device structure are explained. The solution to these challenges is then presented in the form of the novel device structure. The device electrical characteristics and corresponding device physics are studied in detail. Finally, fabrication on flexible substrate is demonstrated. The work presented in this chapter was described in references [1] through [7].

3.1. Motivation

As described in Chapter 2, the source and drain (S/D) contacts of the conventional a-Si TFT, in both top-gate and bottom-gate structures, are formed by first depositing layers of n+ a-Si and metal, then lithographically patterning the contact regions. The S/D contact must be in contact with the channel, in order to allow electrons to flow during TFT operation. As such, a certain amount of overlap (exact amount depends on process conditions) is required between the (S/D) contacts and gate electrode, to prevent device failure due to mis-alignment. This overlap, however, creates parasitic capacitance between the S/D and gate electrodes of the TFT (Figure 3.1). This parasitic capacitance is detrimental to device power consumption and speed performance [8].

To avoid the undesirable parasitic capacitance, self-alignment techniques have been developed to perfectly align the S/D contact to the edge of the channel without any overlaps. To self align the bottom-gate of a-Si TFT [8][10], the fabrication starts with the deposition of the gate stack consisting of SiN_x, intrinsic a-Si and n^+ a-Si, over the patterned gate electrode. Up to this

point, the process is identical to that of the conventional bottom-gate fabrication. The next lithography step is performed by exposing the photoresist through the back of the substrate (Figure 3.2(a)). Acting as an addition to the normal photomask, the gate electrodes of the TFTs also prevent UV light from reaching the photoresist. As such, only the photoresist that is directly adjacent to the gate will be exposed and developed away. The remaining photoresist forms the lift-off mask for defining the S/D metal (Figure 3.2(b)). After blanket evaporation and lift off, the S/D metal is used as the mask to pattern the n+ a-Si layer to isolate the S/D contacts (Figure 3.2(c)). The resulting S/D contacts are perfectly lined up to the gate edge (channel edge).

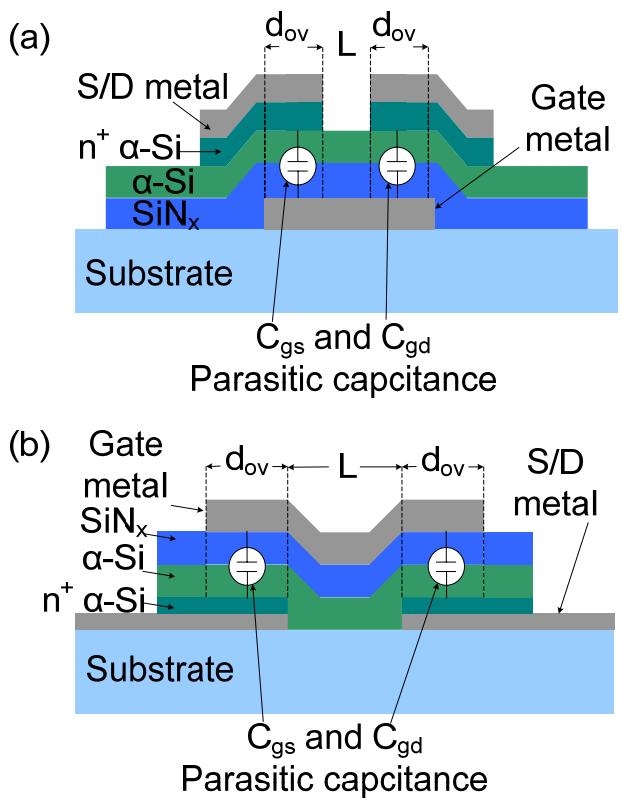


Figure 3.1. Parasitic capacitances between the S/D and gate due to alignment tolerance overlaps – (a) bottom gate structure (b) top gate structure.

Bottom gate a-Si TFTs fabricated with this self-alignment technique exhibit excellent electrical performance, with mobility and contact resistance comparable to the conventional bottom gate a-Si TFT. However, there are also significant disadvantages associated with this self-alignment technique. Backside UV exposure requires a substrate material which is transparent in the UV regime, which precludes the use of many flexible substrates. This implies that it might be

difficult to use this process for flexible electronics applications. Furthermore, backside UV exposure also requires very thin layers of intrinsic and n^+ a-Si (< 30nm combined), because thick layers of a-Si will absorb too much UV and prevent proper exposure of the photoresist [8]. It is known that the a-Si TFT with thin intrinsic a-Si layer (< 50nm) are more susceptible to threshold voltage instabilities under DC gate and drain voltage bias, when compared with a-Si TFT with thicker intrinsic a-Si layers [11].

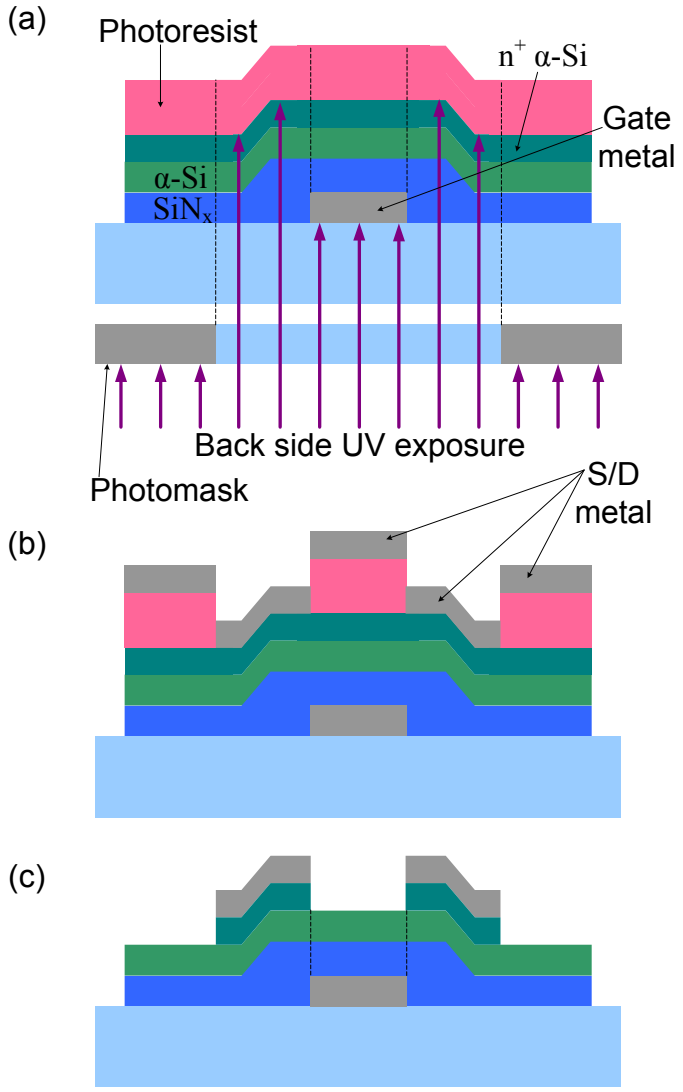


Figure 3.2. The self-aligned fabrication process for the bottom gate a-Si TFT. (a) Backside exposure using the gate electrode as part of the photomask to define the S/D region. (b) Blanket deposition and liftoff of S/D metal. (c) Reactive ion etch to define the n+ a-Si layer, using S/D metal as the mask.

Backside exposure also requires unconventional lithography equipment for backside alignment and projecting UV light from the bottom. This can result in a high-cost and low throughput production process that is undesirable at the manufacturing scale.

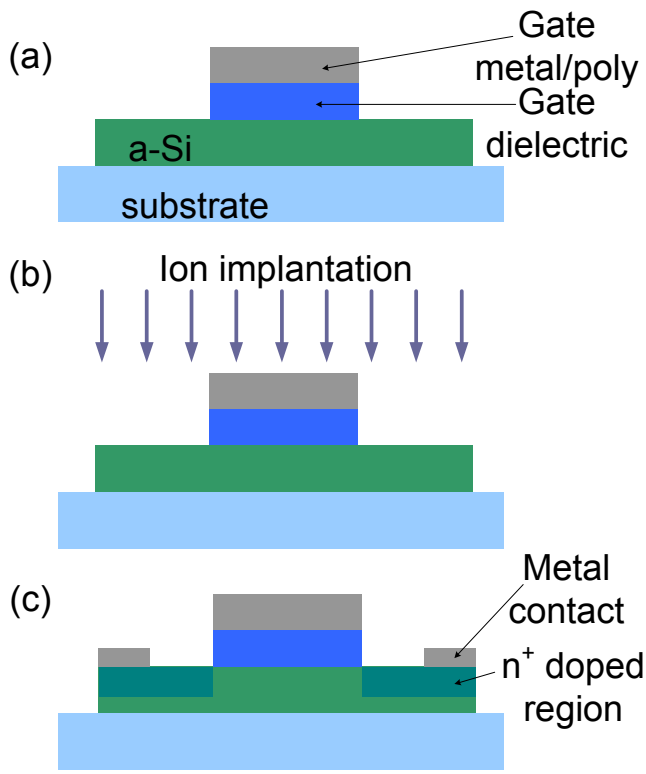


Figure 3.3. The self-aligned fabrication process for the coplanar top-gate amorphous silicon TFT. (a) Gate metal and gate dielectric layers are patterned (b) Ion implantation is performed to form the doped S/D regions, using the gate electrode as the shadow mask (c) Selective laser anneal is used to activate dopants and the metal contact are deposited to complete the S/D.

The staggered bottom-contact structure is difficult to self align, because the S/D electrodes are deposited before the gate electrode. As a result, self-alignment with the bottom-gate amorphous silicon TFT is typically done with a coplanar structure that is similar to the standard VLSI MOSFET [12][13][14][15]. The process starts with the deposition of the a-Si semiconductor layer, SiN_x gate dielectric layer and gate metal layer. The gate metal and gate dielectric layers are patterned form the gate contact (Figure 3.3(a)). Ion implantation is performed form the source and drain regions, using the patterned gate electrode as the shadow mask (Figure 3.3(b)). The gate electrode prevents implanted ions from reaching the channel region,

and therefore the doped S/D regions are directly adjacent to the channel edge. Typically, after implantation high temperature annealing (>600°C) is required to activate the dopants and repair damages to the material [13]. However, the process temperature for a-Si is typically constrained to < 300°C, by a-Si material property and substrate requirements [16]. As a result, laser anneal must be performed to selectively anneal the contact region (Figure 3.3(c)) [15]. Finally, metallization is deposited to complete the S/D contact region.

The self-aligned top-gate a-Si TFT process has the major drawback of needing an ion implantation step. Ion implantation is inherently a high energy process that creates significant damages to the material being implanted. Since the high temperature thermal anneal is not compatible with a-Si or flexible substrates, an excimer laser anneal must be used as an alternative. However, laser anneal comes with its own problems of non-uniformity and high cost [17].

Both the top-gate and bottom-gate self-alignment process for a-Si TFTs are less than ideal. The bottom-gate process requires specialized lithography and is not compatible with many flexible substrates. The top-gate process does not need specialized lithography tools and could be compatible with flexible substrates if an excimer laser anneal is used. However, excimer laser annealing is expensive and highly non-uniform. As such, both processes do not lend themselves to low-cost and high throughput manufacturing. Therefore, a new approach to self-alignment is needed to overcome these difficulties. Ideally, this approach should be low cost, uniform, fully compatible with flexible substrates and require no specialized equipment.

3.2. New device structure

One approach that can potentially meet the requirements outlined in the previous section is the Schottky contact transistor (Figure 3.4). As the name implies, the S/D contacts in this device structure is made of metallic silicide (silicon-metal alloy) and doping is avoided altogether. The self-alignment of the S/D contacts to the channel can be achieved by using a selective silicidation process at low temperature. As such, it avoids the use of implantation, need for high-temperature or laser anneal and specialized lithography tools.

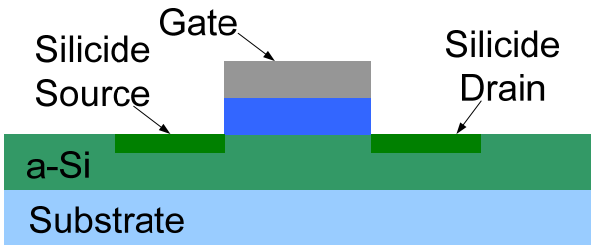


Figure 3.4. Proposed a-Si Schottky contact TFT with self-aligned S/D contacts.

3.2.1. Overview of Schottky contact transistors

The schottky contact transistor (SFET) was first proposed and demonstrated by Lepselter and Sze in 1968 as a single crystalline p-channel device with PtSi S/D regions to an n-type body region [18]. Unlike the conventional MOSFET, where the heavily doped S/D contact provides a gate-controlled thermal barrier, the silicide S/D provides a Schottky barrier to carriers injection into the channel. In the case of the PtSi S/D in [18], the inversion carrier (hole) Schottky barrier height was measured to be ~ 0.25 eV (determined from a current-voltage measurement of a Schottky diode using PtSi to p-type silicon), which implies an electron barrier height of ~ 0.85 eV. The smaller 0.25 eV barrier allows holes to flow into and out from the channel, whereas the larger 0.85 eV barrier suppresses electron flow.

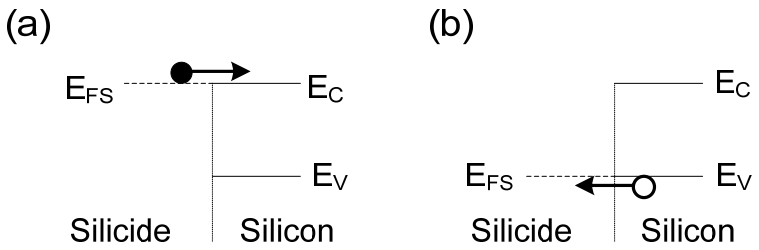


Figure 3.5. (a) Ideal n-type Schottky contact (b) Ideal p-type Schottky contact. E_{FS} refers the Fermi level in the silicide. The open and closed circles represent electrons and holes, respectively. The arrows indicate the direction of carrier injection from silicide into silicon.

Since Schottky barrier height, to first order, cannot be changed by the gate bias and is fixed by the silicide work function, it is crucial to choose the silicide that provides the smallest barrier height to achieve high drive current and high on current to off current ratio. Ideally, the n channel SFETs should use a silicide whose work function lines up with the silicon conduction

band and the p channel SFETs should use a silicide whose work function lines up with the silicon valence band (Figure 3.5). In practice, however, the best p-type contact is achieved with PtSi (~0.25 eV Schottky barrier to the valence band of silicon [19][20]) and the best n-type contact is achieved with Ytterbium Silicide (~0.27 eV Schottky barrier to the conduction band[21]). Novel techniques such the use of valence-mending absorbates [22] and fermi level depinning [23] have been proposed to achieve barrier as low as ~0.1 eV. However, these techniques are relatively complex and difficult to realize in large-scale production.

When compared to conventional single crystalline MOSFETs, single crystalline SFETs have significantly improved immunity to short channel effects, which include S/D charge sharing, drain-induced barrier lowering and subsurface punch through. S/D charge sharing refers to the reduction of transistor threshold voltage due to the effects of the depletion regions of the source and drain. As the channel gets shorter, the contribution to the bulk charge in the channel from these depletion regions becomes more significant. As a result, the amount of charge that must be induced by the gate voltage is diminished, reducing the threshold voltage (Figure 3.6). Drain-induced barrier lowering (DIBL) refers to the influence of the drain voltage on the source barrier to carrier injection into the channel. At short channel lengths, a large drain voltage can “pull down” the source barrier, causing the apparent threshold voltage of the transistor to decrease (Figure 3.7). Subsurface punch through also refers to the influence of the drain voltage on the source junction and barrier to carrier injection. Unlike DIBL, subsurface punch through happens beneath the channel in the bulk of the MOSFET body. However, the physics of the two processes are very similar (Figure 3.8). SFETs suffer less from the S/D charge sharing issue, because it is much easier to create very shallow and abrupt junctions with smaller depletion regions using silicide processes. SFETs are also less susceptible to DIBL and subsurface punch through, because, to first order, the Schottky barrier between the source and the channel is fixed by the difference between the Fermi level of the silicide and (conduction or valence) band edges of silicon. Therefore, the barrier height is fairly insensitive to the applied drain bias. SFETs also offer simplicity of fabrication and potentially lower series resistance by replacing highly doped silicon

with metallic silicide. These benefits make the SFET a very attractive candidate for aggressively scaled CMOS technology.

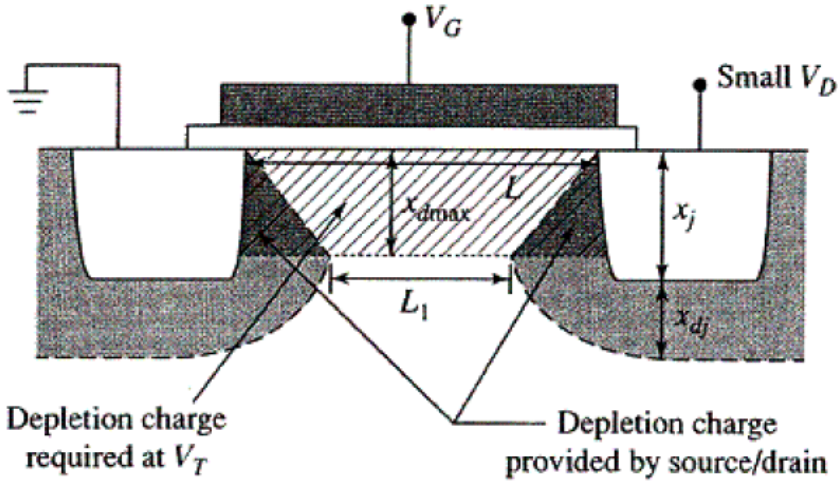


Figure 3.6. Part of the depletion charge at threshold is coupled to the source and drain, therefore less charge needs to be induced by the gate voltage, reducing the threshold voltage of the transistor [24].

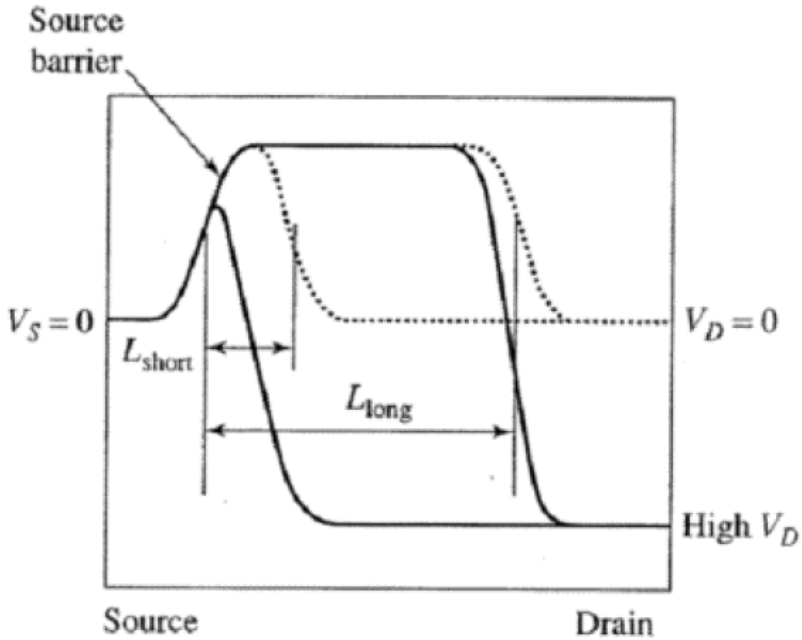


Figure 3.7. Conduction band of a long-channel and a short channel MOSFET at V_D = 0V (dotted line) and high V_D (solid line). The source barrier of the short-channel device is reduced by the drain voltage at high V_D [24].

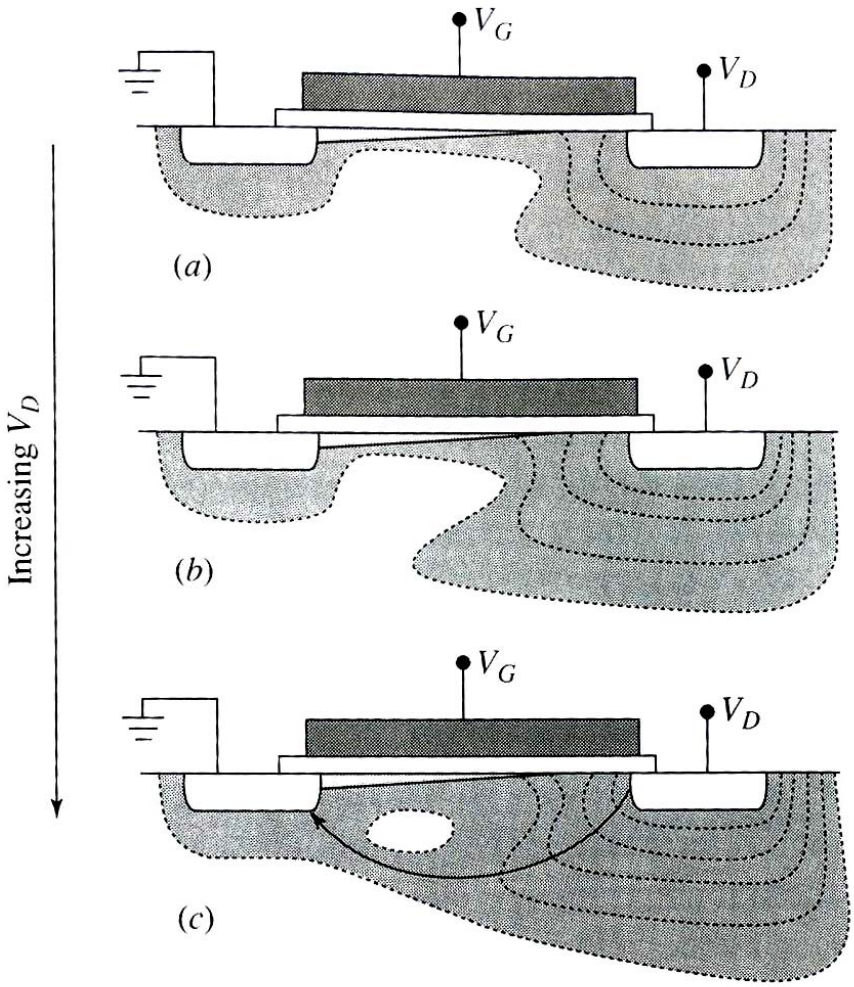


Figure 3.8. Cross section of a short-channel MOSFET with its source contact grounded, gate voltage (above V_T) held constant as the drain voltage V_D is increased from (a) to (c). The depletion region from the drain punches through to that of the source, underneath the channel, creating a path for the drain current as indicated by the arrow in (c) [24].

3.2.2.Silicides

While the SFET offers excellent short channel immunity, our interests in this structure lie primarily in its potential application as an easy-to-fabricate, low temperature self-aligned a-Si TFT process. By eliminating the need for doped contact layers, issues with implantation and thermal/laser anneals would be resolved. The key to realizing such a process is finding a silicide that can be formed at low temperatures (< 300°C) and has low barrier to electron injection.

3.2.2.1. Choice of silicide

Silicides are compounds formed by reaction between silicon and metal under elevated temperature. The temperature and rate at which the silicidation reaction occurs is determined by the difference in free energy between the separated components (metal and Si) and the compound phase (silicide) [25]. Metal-Si systems that have silicide phases with much lower free energy will have low silicidation temperature and fast silicidation rate. Examples of these metals include Ti, Co, Cr, Pd, Pt, and Ni.

Titanium silicide

Titanium disilicide ($TiSi_2$) is the most widely used silicide for making low-resistivity contacts to silicon in ultra large-scale integration devices. In the typical contact formation process, a thin film of Ti is deposited on a cleaned silicon surface, usually by sputtering. An annealing treatment at >500°C in nitrogen is applied to react the Ti with the Si to form the precursor phase C49 $TiSi_2$, which has a relatively high resistivity of 50 – 75 μΩ-cm [26]. The unreacted Ti is removed via a selective wet etch. This is followed by a second anneal at >700°C to transform the C49 $TiSi_2$ into the lower-resistivity C54 $TiSi_2$ phase (15 – 20 μΩ-cm) [26]. The barrier height for electron injection (φ_B) into silicon of $TiSi_2$ is ~0.6 eV [27]. The combination of the high temperature required for silicidation and large φ_B make $TiSi_2$ an unsuitable choice for an a-Si TFT process.

Cobalt silicide

Cobalt silicide is another material that has been widely investigated for applications to low-resistivity contact and high conductivity gate lines in integrated circuits. It has been shown that Cobalt reacts with silicon at temperatures above 350°C [28]. The first phase that appears at around 350°C is Co_2Si, which is replaced successively by CoSi and $CoSi_2$ upon annealing at higher temperatures. The growths of Co_2Si and CoSi have been shown to proceed via a diffusion limited process with activation energy of about 1.5eV and 1.9eV, respectively [28]. Electrical measurements at room temperature show that the bulk resistivities of Co_2Si, CoSi and $CoSi_2$ are 66, 86, 18 μΩ-cm, respectively [29]. The barrier height for electron injection is 0.68eV [27]. The silicide formation temperature of cobalt silicide is much lower than that of Titanium silicide, but it is still too high for an a-Si TFT process.

Chromium silicide

Chromium has been shown to form silicide with hydrogenated amorphous silicon at temperatures around 300°C [30]. The silicide layers typically have composition close to $CrSi_2$. The resistivity of the film is ~600 μΩ-cm and is relatively independent of the silicidation temperature [30]. The silicide growth proceeds via a diffusion limited process with a low activation energy of 0.55eV [30]. The barrier height to electron injection is 0.57eV. The silicidation temperature and barrier height of $CrSi_2$ are both more suitable than silicides of Titanium and Cobalt, but its resistivity is more than an order magnitude higher. This high resistivity makes it unattractive as a contact material.

Platinum, Palladium and Nickel silicides

These three transition metals are in the same column in the periodic table, and therefore have very similar silicide formation properties. They all have been shown to form low-resistivity silicides at temperatures around 300°C [31][32][33][35]. The initial phase of the silicides, at low temperatures (<300°C), are Pt_2Si, Pd_2Si, and Ni_2Si, with resistivities of approximately 50 μΩ-cm, 50 μΩ-cm and 30 μΩ-cm, respectively [36][32][35]. At higher silicidation temperatures (300°C - 600°C), the phases that appear are PiSi, PdSi and NiSi, with significantly lower resistivities of approximately 30 μΩ-cm, 30 μΩ-cm and 15 μΩ-cm, respectively [36][32][35]. Beyond 600°C, the resulting PdSi and PtSi properties are relatively independent of silicidation temperature. Ni, however, will form $NiSi_2$, a much more resistive phase of silicide, with resistivity > 50 μΩ-cm [35]. The barrier heights for electron injection of Pt_2Si, Pd_2Si, and Ni_2Si are 0.85eV, 0.71eV and 0.65eV, respectively [27]. All three silicides can be used in a-Si Schottky contact TFT process, but Ni silicide is the best candidate with the lowest resistivity and the lowest barrier to electron injection.

The different silicide material properties are summarized and compared in Table 3.1. Ni silicide emerges as the most promising candidate. However, despite having the lowest φ_B amongst the suitable low temperature silicides, Ni silicide still has barrier of 0.65eV, which is a large energy barrier for electrons to surmount to get in and out of the channel from the S/D

contacts. To determine whether Ni silicide can make a good S/D contact in a-Si TFT, numerical simulation was performed to better understand the electronic band structure and possible carrier injection mechanisms at the S/D contact-to-channel interface.

Metal	Lowest reported silicide formation temperature	Phase of silicide	Resistivity	Barrier Height
Ti	500°C	C49 $TiSi_2$	50-75 μΩ-cm	0.6eV
Co	350°C	Co_2Si	60-70 μΩ-cm	0.68eV
Cr	300°C	$CrSi_2$	600 μΩ-cm	0.57eV
Pt	300°C	Pt_2Si	40-50 μΩ-cm	0.85eV
Pd	300°C	Pd_2Si	40-50 μΩ-cm	0.71eV
Ni	250°C	Ni_2Si	20-30 μΩ-cm	0.65eV

Table 3.1. Properties of different silicide materials.

3.2.2.2. Simulation studies of the Ni silicide to a-Si contact

The Taurus Device simulation tool from Synopsys was used to numerically determine the behavior of the Ni silicide-to-channel junction during TFT operation. Specifically, we monitored the changes in the conduction band diagram along the Ni silicide to a-Si junction, close to the semiconductor-insulator interface (white dotted line in Figure 3.9), as the gate voltage was varied in the device. For the sake of simplicity, a-Si was treated as c-Si with a wider bandgap of 1.6eV and the band tails states are ignored. The omission of deep states in a-Si will lead to quantitative errors in the simulation, but it will provide a qualitative understanding of the device behavior. The a-Si, SiN_x and Cr layers are 150nm, 300nm and 80nm, respectively. Ni silicide is treated as a metal with a thickness of 30nm and barrier to electron injection of 0.65eV. All other material parameters are set to standard values. For more details on the simulation setup, refer to appendix B.

The simulation showed that under equilibrium conditions (V_{DS} = 0V), the applied gate voltage has a dramatic effect on the band profile along the Ni silicide – a-Si junction. Increasing V_G pushed the conduction band of a-Si towards the Fermi level, which rapidly reduced the Ni silicide source – a-Si channel Schottky barrier thickness (Figure 3.10). As the barrier thickness is reduced to sufficiently small value, electrons injection is no longer constrained to thermal emission over the Schottky barrier, and tunneling through the Schottky barrier becomes a viable pathway. Tunnel injection has been shown to be an important mechanism of electron transport in a-Si Schottky diodes under conditions of large internal electric fields, similar to the condition of the high applied gate field in our TFT simulation structure [34]. Therefore, Ni silicide can make good a-Si TFT S/D contacts if tunnel injection of electrons is possible under normal TFT operation conditions.

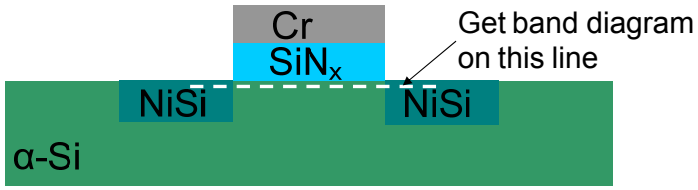


Figure 3.9. Taurus device simulation device structure.

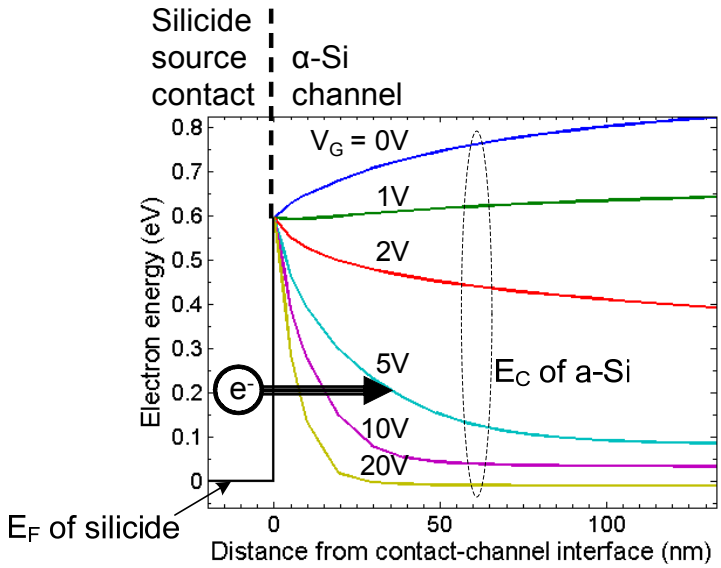


Figure 3.10. Simulated band diagrams of the Ni silicide source – a-Si channel junction. Black line represents E_F of the silicide and colored lines represent E_C of a-Si under various different gate bias conditions. At high positive gate voltage, electrons slight above EF in the silicide can tunnel into the conduction band of the silicon.

To assess whether tunnel injection of electrons from the Ni silicide source to the a-Si channel is possible under normal TFT operating conditions, the tunneling current through Schottky barrier was calculated using the approach outlined in [34]:

$$J_{TN} = \int_0^{q\phi_{bn}} J'_{TH}(u)|T|^2(u)du \qquad (3.1)$$

Where, J'_{TH} is a Boltzmann distribution of carriers assumed to be incident on the barrier and A* is the Richardson constant (Figure 3.11):

$$J'_{TH}(u)du = \frac{A^* T^2}{k_B T} e^{-\frac{u}{KT}} du \qquad (3.2)$$

and $|T|^2(u)$ is the tunnel probability calculated using the WKB method, A triangular barrier was used to approximate the barrier shape calculated via numerical simulation (for typical TFT operating conditions of V_{GS} = 10V and V_{DS} = 0.1V) (Figure 3.11)

$$|T|^2(u) = \exp\left[-\frac{4\pi}{h}(2m^*)^{\frac{1}{2}} \times \int_0^{x(u)} dx\sqrt{q\phi_{bn} - qE_s x - u}\right] \qquad (3.3)$$

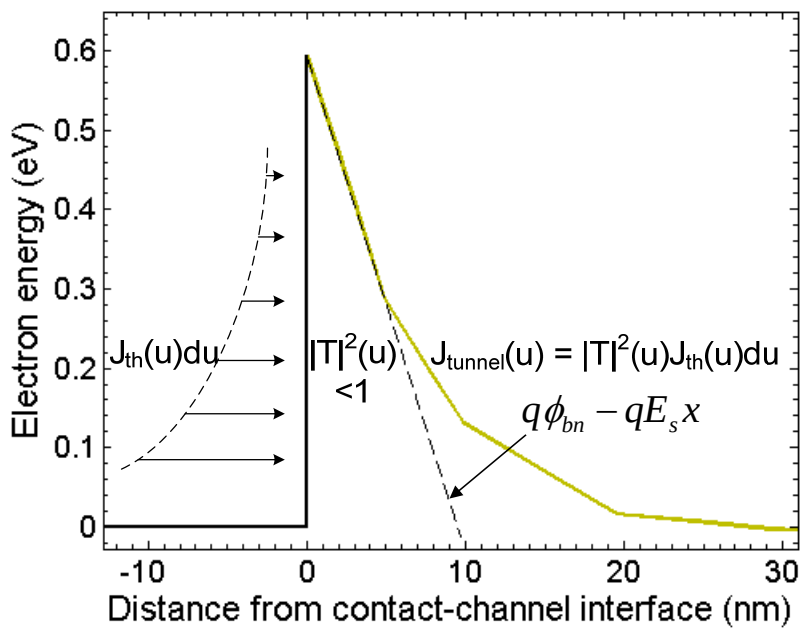


Figure 3.11. schematic illustration of the tunneling current calculation. The arrows on the left represent the thermally distributed incoming flux of electrons.

Under the above conditions, the tunnel current density was calculated to be about 4.3μA/μm^2. Assuming a TFT width of 80μm and the silicide contact thickness of 20nm, the cross sectional area of the silicide source – a-Si junction is about 1.6μm^2, which means the tunnel contact can support about 7μA of current. This value is much larger than the typical magnitudes of a-Si TFT current under the conditions specified. Despite being a very rough estimate of the tunnel current capacity, this suggests that tunneling through the Schottky barrier is a possible carrier injection mechanism for the a-Si TFT with Ni silicide source/drain.

3.2.2.3. Characterization of Nickel silicide on amorphous silicon

Ni silicide formation on a-Si grown in the Princeton PECVD tool was experimentally characterized. A blanket sheet of a-Si was grown on top of a glass slide using the standard amorphous silicon recipe (SiH_4 flow rate of 40sccm, chamber pressure of 500mT, deposition temperature ~250°C and plasma power density of 18mW/cm^2). A 30nm layer of Ni was deposited immediately after a-Si growth, using electron beam evaporation. The sample was annealed in N_2 ambient for 1 hour at temperatures ranging from 220°C – 300°C. The unreacted Ni was removed using a selective chemical etch (HNO_3:HCl:De-ionized water 1:5:3). The Ni silicide region appears yellowish under the microscope and is visually distinct from the brownish a-Si.

Sheet resistance of the Ni Silicide formed was measured using the four point probe method. The sheet resistance of Ni silicide decreased linearly with silicidation temperature starting from about 25 Ω/sq at 220°C to about 5Ω/sq at 300°C (Figure 3.12). This is in reasonable agreement previously observed values [35]. Although the lowest sheet resistance is obtained at 300°C, we have decided to use 280°C for the a-Si Schottky TFT process because a-Si deposited at 250°C degrades when subjected to temperatures >280°C. The sheet resistance of 10Ω/sq obtained at 280°C is sufficiently low for the purposes of source and drain contacts.

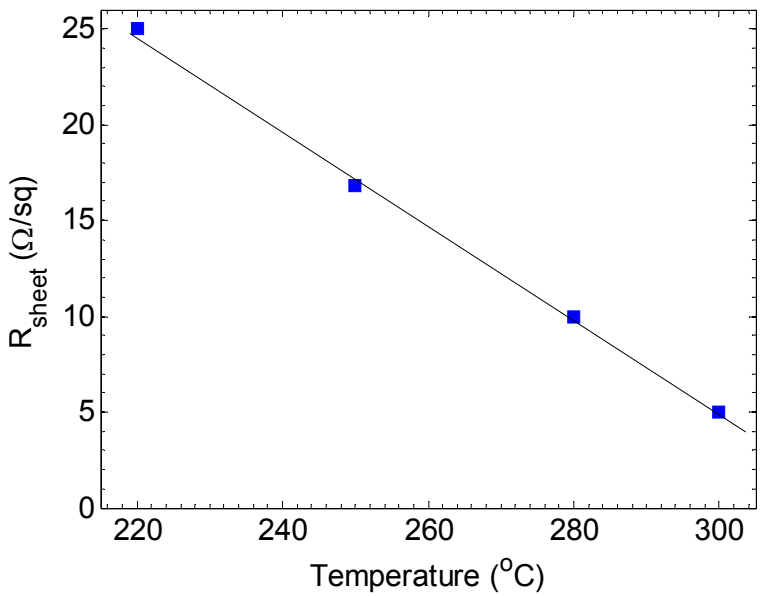


Figure 3.12. Sheet resistance of Ni silicide formed on PECVD amorphous silicon.

3.2.3. Fabrication process

With the ability to form a low-resistivity Ni_2Si on a-Si at 280°C, the a-Si TFT with self-aligned Schottky S/D can be realized (Figure 3.13). The process starts with the deposition of the TFT stack on 1.1-mm-thick Corning® 1737 glass slides using PECVD with an excitation RF frequency of 13.56MHz. The PECVD pressures and temperatures are 500mT and 250 °C unless otherwise noted. First, a 250nm layer of a-Si is deposited from a pure SiH_4 (50sccm) plasma with power density of 18 mW/cm^2. This is followed, without breaking vacuum, by the deposition of a 300nm SiN_x gate dielectric layer using a plasma with gas flow ratio of SiH_4:NH_3 = 14sccm : 130sccm and power density of 22mW/cm^2. A 80-nm layer of Cr is then thermally evaporated over the nitride as the gate metal (Figure 3.13(a)).

The gate is patterned by photolithography and wet etching (Figure 3.13(b)). The self-alignment begins with the reactive-ion etching of the gate insulator SiN_x in a fluorinated plasma, where the gate metal is used as the etch mask. The etch recipe (CF_4:H_2) is optimized for a high etch rate and a vertical sidewall. This anisotropy is extremely important for reasons to be discussed below. To form the self-aligned silicide S/D, photoresist is first patterned with openings that expose the regions that will become source and drain, as well as the intervening gate

electrode (Figure 3.13(c)). This step defines the width of the device and also electrically isolates one device from another.

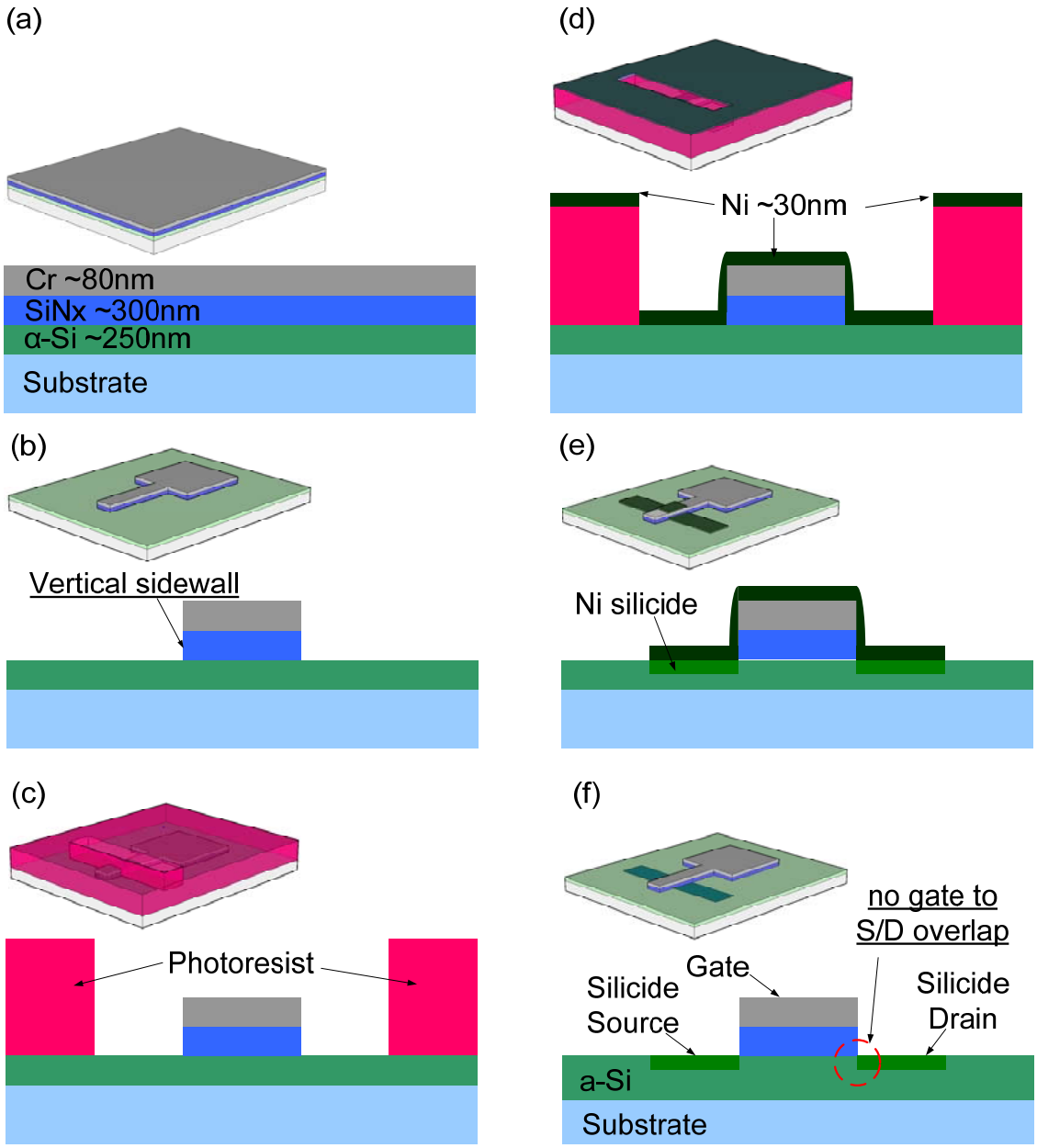


Figure 3.13. Fabrication process of the top-gate a-Si TFT with self-aligned silicide S/D: a) Deposition of TFT stack; b)definition of gate electrode; c) definition of the channel width and electrical isolation of devices; d) blanket deposition of Ni; e) lift off and silicidation; f) selective removal of unreacted Ni.

A blanket 30-nm nickel layer is deposited, and then removed outside the device region by lift-off (Figure 3.13(d)). The devices are then annealed at 280°C in N_2 ambient for 1 hour to convert the

nickel to nickel silicide by reaction with the underlying a-Si (Figure 3.13(e)). The unreacted nickel is removed in a selective wet etch consisting of HNO_3:HCl:H_2O (1:5:3) (Figure 3.13(f)). Since no silicide formed on the sidewall or on top of the metal gate, unreacted nickel can be selectively removed to ensure that there are no conducting paths between the gate contact and the S/D.

Anisotropic etch optimization

The conventional reactive ion etch recipe for SiN_x (CF_4/O_2 chemistry) is isotropic and as a result it creates an undercut profile in the SiN_x sidewall (Figure 3.14(a)). This is not acceptable because an undercut or tapered profile in the sidewall would result in a highly resistive un-gated a-Si region between the silicide S/D and the gated channel region. This leads to high contact resistance and potential device failure. Therefore it is important to develop an anisotropic etch that will create the desired vertical sidewall profile.

The species responsible for etching SiN_x in the CF_4 based reactive ion etch is the F radical, which comes from dissociation of CF_4 in the plasma. The addition of O_2 increases the F radical concentration. This increase in F radical is a result of reaction between O_2 and CF_x radicals forming stable compounds like CO_2 and COF_2, which releases more F radicals by suppressing recombination of F and CF_x radicals [37]. The overall effect of the increased F concentration is an increase in etch rate, and an increase in the isotropy of the etch.

To make the etch more anisotropic, CF_4/H_2 chemistry can be used. The addition of H_2 has two effects on the etch: (1) H_2 reduces the F radical concentration by forming the relatively inert HF gas, which reduces the overall etch rate (2) H_2 also reacts with the CF_x radicals to form CF, which are precursor to polymer deposition [37]. As a result, polymer chains, C_xF_y, are deposited on the surface of sample being etched. On areas of the sample, such as sidewall and trenches, where ion bombardment is relatively weak, etching is prevented by polymer, making the etch anisotropic [37].

By carefully controlling the CF_4/H_2 ratio in the reactive ion etch plasma, a vertical sidewall profile was achieved for the SiN_x gate dielectric (Figure 3.14(b)). This enabled the final structure of the top-gate a-Si TFT to have Ni_2Si on top of the a-Si directly adjacent to the gated channel

region, with no overlap between the gate electrode and the silicide S/D electrode. The optical image of the completed a-Si TFT with self-aligned silicide S/D is shown in Figure 3.15.

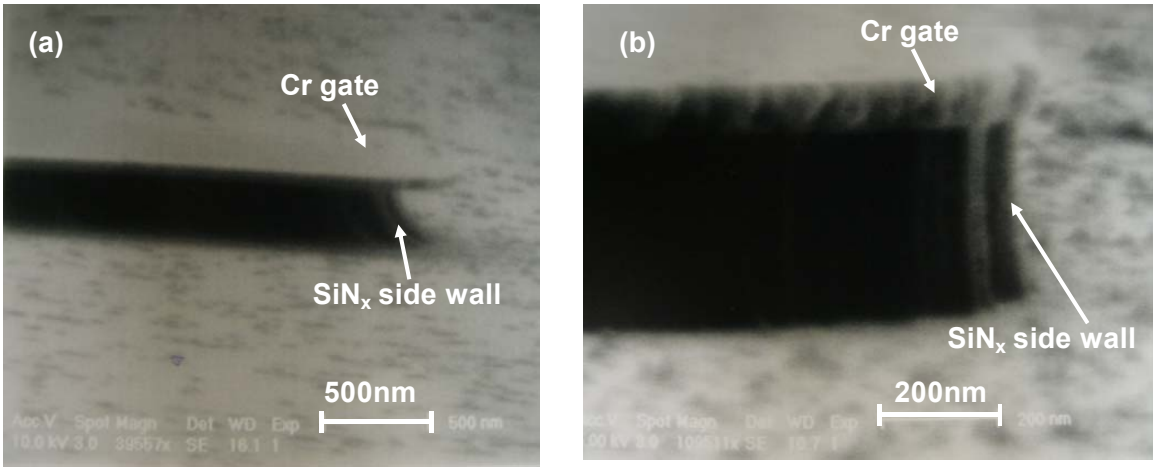


Figure 3.14. SEM images of SiNx gate dielectric side wall profiles (a) conventional etched with CF_4/O_2 chemistry (b) optimized CF_4/H_2 chemistry.

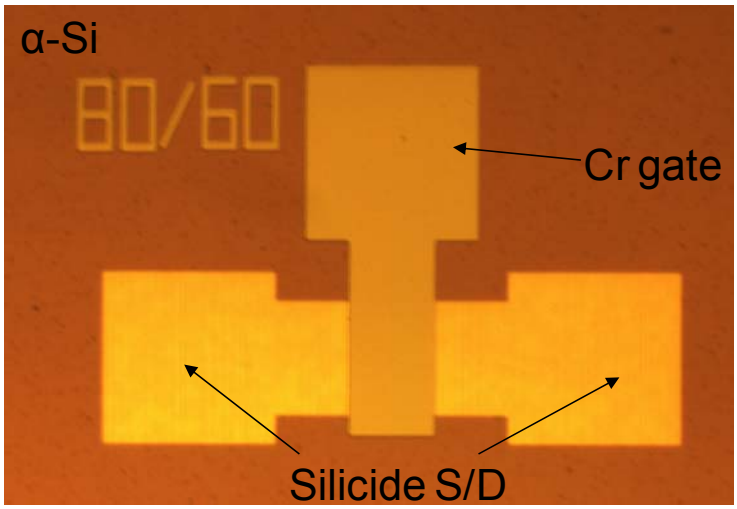


Figure 3.15 Optical image of the completed top-gate a-Si TFT with self-aligned silicide S/D

3.3. Device characteristics

The DC transfer characteristics of a typical a-Si top-gate TFT with self-aligned Ni silicide S/D (W/L=80μm/40μm) fabricated on glass at 280°C are plotted in Figure 3.16. The performance metrics were extracted from the saturation curve (V_D = 10V) using conventional MOS theory. The long-channel devices (L > 40μm) exhibited a threshold voltage of 2.7V, saturation field effect

mobility of 1.0cm^2/Vs (averaged over gate-source voltages of 3 to 12V), subthreshold slope of 600mV/dec and an ON/OFF ratio of ~2x10^6.

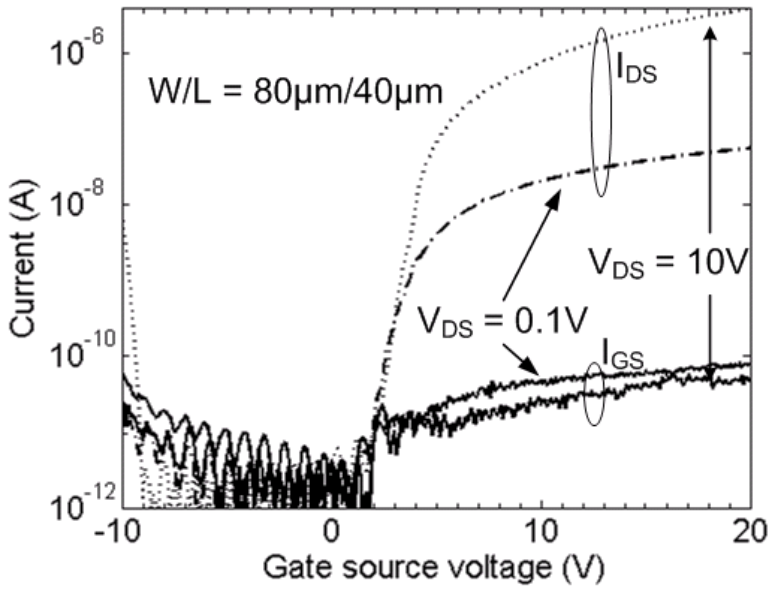


Figure 3.16. Room temperature transfer characteristics (drain current VS gate-source voltage for drain-source bias of 0.1V and 10V) for a top gate α-Si TFT with self-aligned nickel silicide source drain. W/L=80μm/40μm.

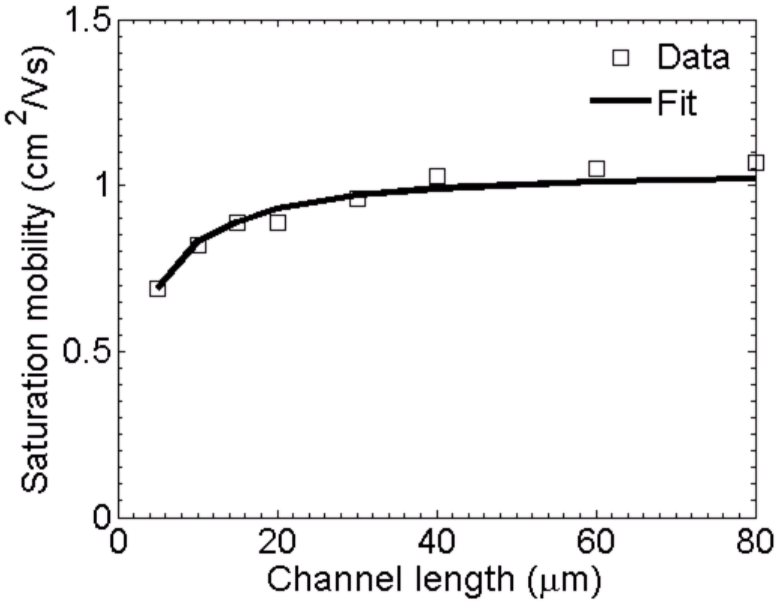


Figure 3.17. Channel length dependence of saturation field effect mobility.

The dependence of the saturation field effect mobility on channel length (in the range of 5μm to 80μm) is consistent with previous studies (Figure 3.17) [38]. As the channel resistance

drops with decreasing channel length, the contact resistance at the S/D-to-channel junction becomes increasingly significant, resulting in a decrease in apparent mobility at shorter channel lengths. For devices with a 5-μm channel, the apparent (uncorrected for contact resistance) saturation field effect mobility is still 0.7cm^2/Vs, which suggests that the contact resistance between the S/D and channel is low. This low series resistance is also supported by the TFT output characteristics shown in Figure 3.18, which shows a linear relationship between source-drain current and source-drain voltage at low source-drain biases. A poor contact to S/D typically leads to rectifying behavior and concave output curves at low source-drain biases, which is not observed in our device.

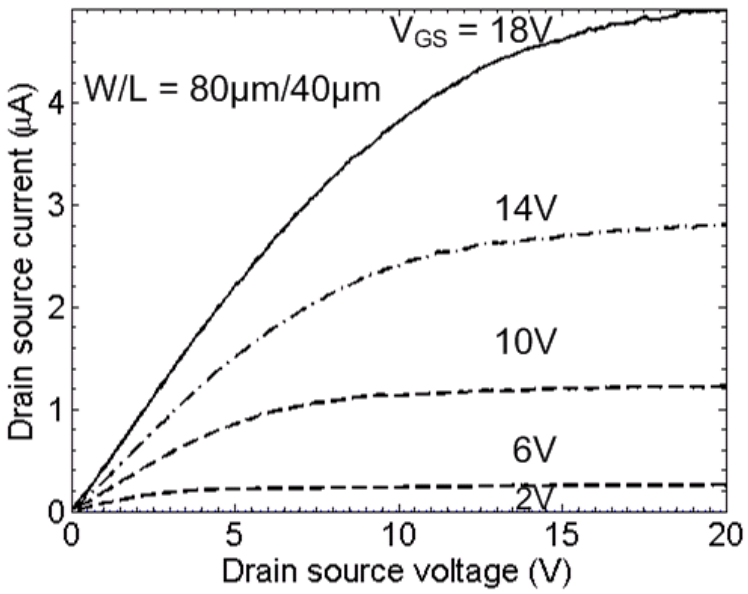


Figure 3.18. Room temperature output characteristics (drain current VS drain-source voltage for gate-source bias from 2V to 18V) of a top gate a-Si TFT with self-aligned silicide source drains. W/L=80μm/40μm.

The performance parameters of these TFTs are comparable with those of state-of-the-art conventional bottom gate TFT's. Previously published top-gate a-Si TFTs have mobilities in the range of 0.3cm^2/Vs to 0.9cm^2/Vs, and sub-threshold slopes from 0.75V/dec to 1.7V/dec [39][40][41][42]. The exception is an experiment using a process temperature as high as 625 °C that resulted in mobility of 1.2cm^2/Vs [43]. Therefore, the mobilities and subthreshold slopes we obtained are among the best ever measured in top-gate TFTs.

3.3.1. Schottky contact characterization

The electrical data showed that the Ni silicide source/drain make excellent contacts to the a-Si channel, with no observed non-linear or rectifying characteristics. Although our simulations had suggested that Ni silicide would be a viable contact, it is still surprising that they performed so well. In order to better understand the mechanism of electron injection across the Schottky barrier, we needed to more quantitatively characterize the contact during TFT operation. We performed two types of experiments, one based on transmission line theory [45] and the other based on four-point probe technique [46], to independently measure the contact behavior of the TFT apart from the channel characteristics.

Transmission line model

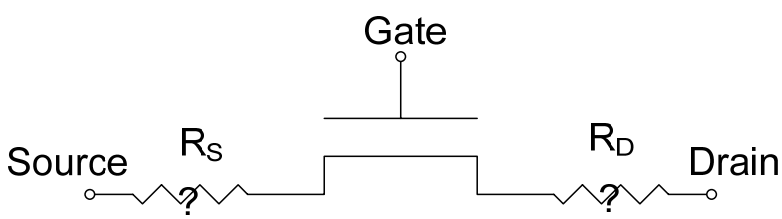


Figure 3.19. The transmission line model for the top-gate a-Si TFT with self-aligned silicide source/drain. The contact resistances are unknown parameters indicated by question marks.

The transmission line model treats the TFT as an ideal transistor in series with a source resistance and a drain resistance (Figure 3.19). During TFT operation, the total device resistance (R_{on}) is given by:

$$R_{on} = R_{ch} + R_C \qquad (3.4)$$

where R_{ch} is the resistance of the a-Si channel and R_C is the combined resistance of the source and drain contacts. R_C is the unknown parameter we are trying to determine and R_{ch} (at small drain-to-source biases) can be expressed using the ideal MOSFET theory as:

$$R_{ch} = \frac{L}{W\mu_n C_{SiNx}(V_G - I_{DS}R_C - V_T)} \approx \frac{L}{W\mu_n C_{SiNx}(V_G - V_T)} \qquad (3.5)$$

Combining equation 3.4 and 3.5, we get

$$R_{on} = \frac{L}{W\mu_n C_{SiNx}(V_G - V_T)} + R_C \qquad (3.6)$$

where L and W are the length and width of the TFT, μ_n is the effective electron mobility in the channel and C_{SiNx} is the capacitance of the SiN_x gate dielectric. In equation 3.6, R_{on} is the parameter that we can experimentally measure during TFT operation, and it is linearly proportional to the channel length L. By measuring R_{on} for an array of devices with different channel lengths, we can determine the unknown parameter R_C through a linear extrapolation of the measured data to L = 0. Furthermore, we can repeat the process for different gate bias values and find the gate-voltage dependence of the contact resistance.

The drain-source current vs drain-source voltage characteristics of devices with channel length ranging from 5μm to 100μm were measured at gate voltage bias ranging from 5V to 20V. A linear fit of the data at small drain-source voltage values provides the R_{on} for the different L and V_{GS} values (Figure 3.20). Then an extrapolation of the calculated R_{on} dependence on channel length, at a given V_{GS}, to zero channel length determined the contact resistance for that particular V_{GS} (Figure 3.21).

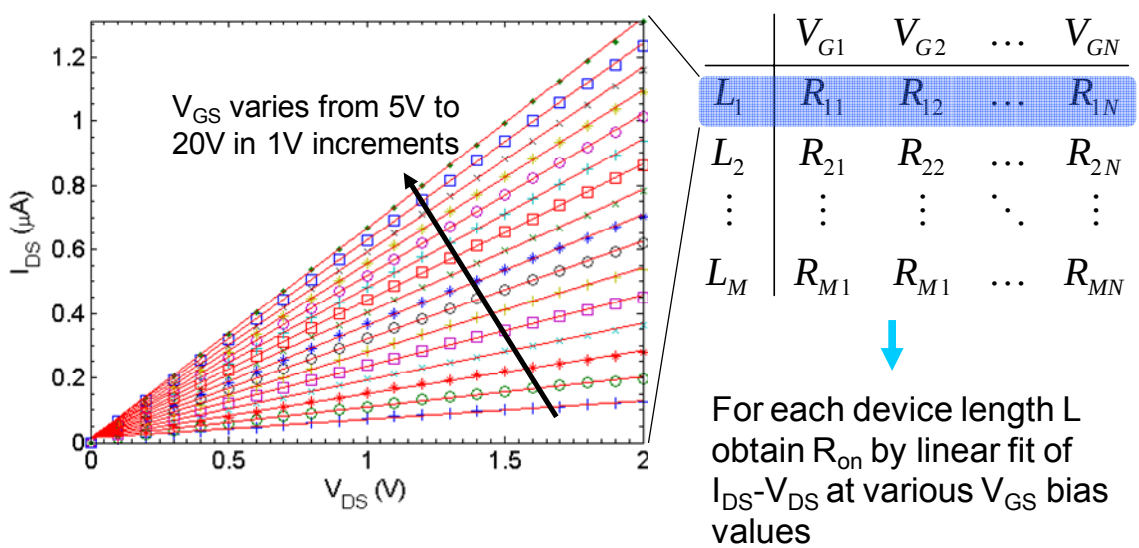


Figure 3.20. Linear fits (red lines) of the drain-source current vs drain-source voltage data (symbols) for different gate-source bias determine the total device resistance (R_{ON}) for a given channel length L. The values in the matrix represent R_{ON} for a given channel length and gate voltage.

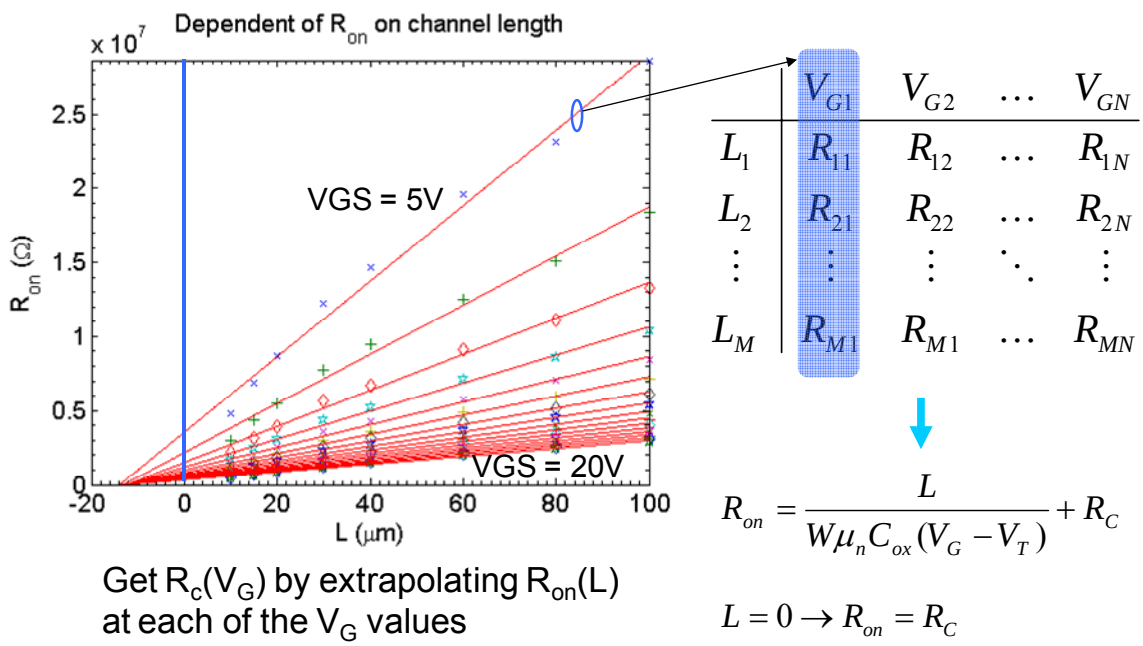


Figure 3.21. The total device resistance (R_{on}, symbols) plotted as a function of channel length L for different gate-source voltages. Extrapolation (red line) to zero channel length determines the contact resistance for that gate-source voltage.

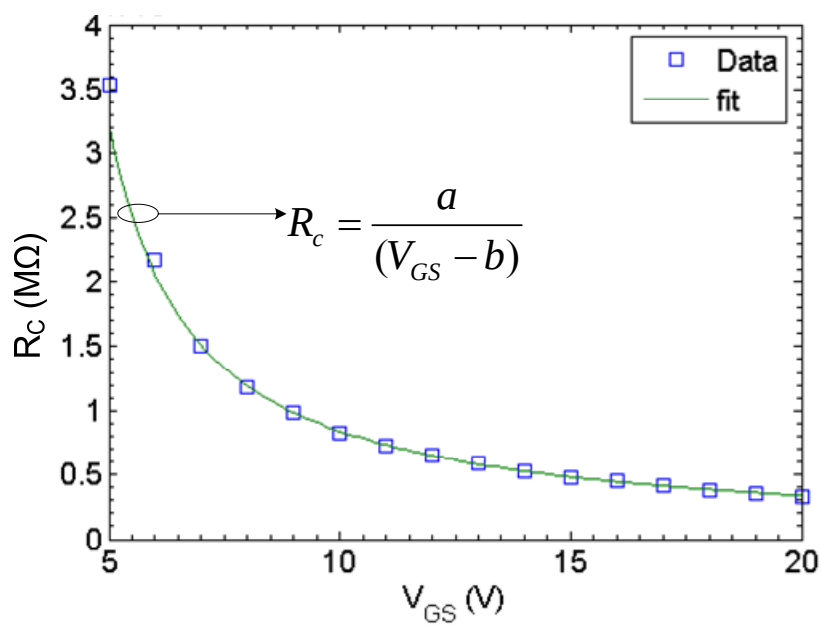


Figure 3.22. Contact resistance as a function gate-source voltage during TFT operation, as determined from the transmission line model.

The extracted R_C as function of V_{GS} is shown in Figure 3.22. The transmission line model analysis showed that the contact resistance (source and drain combined) is inversely proportional to the applied gate-source voltage during TFT operation. This is consistent with our model of tunnel injection of electrons, in which the gate voltage modulates the thickness of the Schottky barrier. Increasing gate voltage reduces tunnel barrier thickness, leading to reductions in contact resistance.

Four point probe method

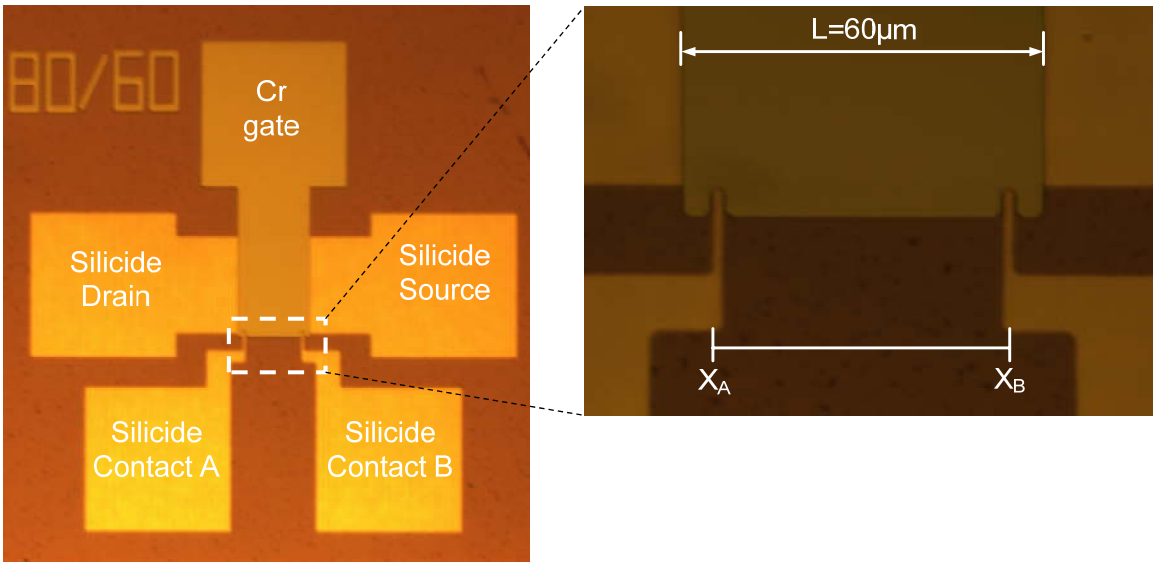


Figure 3.23. Optical image of a gated four terminal device. L = 60nm and X_A and X_B are referenced from the drain-channel junction at 0.

The contact resistance extracted from the transmission line model is the combined series resistance of the drain and the source. This method does not allow the contribution from each contact to be independently determined. The four point probe technique provides an alternative way to separately measure the source and drain contact resistances. The four-point measurement of the contact resistance was performed using a gate four terminal device, which had two additional silicide contacts that protruded into the channel (contact A and B in Figure 3.23). Contacts A and B are used to measure voltages insides the TFT channel during device operation. They are designed to be very small (2µm wide and extend into the channel by 1µm) so as to not disturb the normal operation of the TFT. Simulation using Taurus device show that, even

for a device with the short channel length of 10μm, the disturbance in the potential distribution within the channel due to voltage probes are minimal and localized at the edge of the channel (Figure 3.24) [46].

The channel voltage measurement was performed by sweeping the gate voltage applied to the four terminal TFT devices from -10V to 20V under constant applied drain source voltage of 0.5 V. The voltages on contact A and contact B were recorded along with the drain-source current through the TFT. It was observed that for gate voltages less than the threshold voltage of the TFT, contact A and contact B did not read sensible voltage values. This is because the carrier density in the channel was very low and the a-Si was highly resistive. As the gate voltage increased beyond the threshold voltage, raising the carrier density in the channel, the voltage readings became more consistent with what were expected for positions being probed in the channel (Figure 3.25).

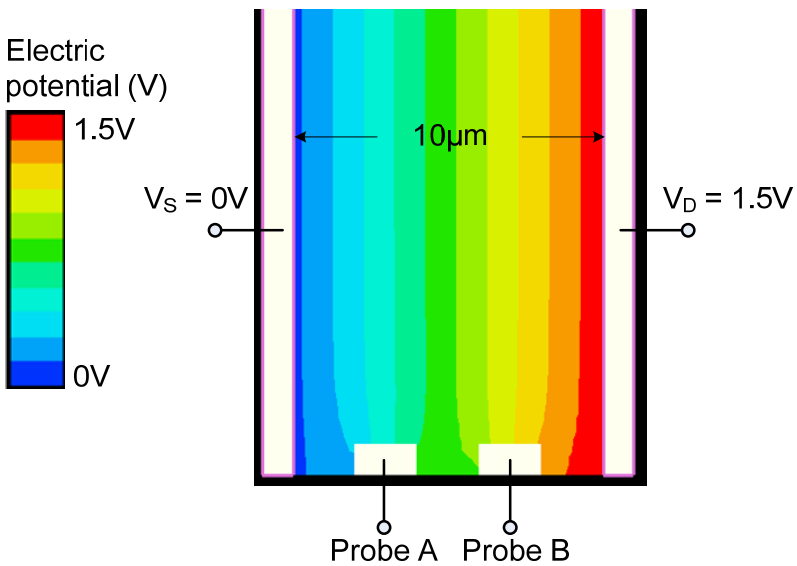


Figure 3.24. Simulated potential distribution within the channel of the TFT that has two silicide voltage probes protruding into the channel.

Using these data we can extract the contact resistance at the source-channel and channel-drain junctions by noting that the voltage difference between the drain and point A in the channel is the sum of the voltage drop across the drain-channel junction ($V_{D\text{-}A}$) and the voltage drop across the portion of the channel ranging from the drain to point A (V_{ch}(D,XA)):

$$V_{D-A} = V_{D-ch} + V_{ch}(D, XA) \tag{3.7}$$

We can express the voltage drops as products of resistances and the drain-source current:

$$V_{D-A} = I_{DS} R_D + I_{DS} \frac{XA}{W\mu_n C_{SiNx}(V_{GS} - V_T)} \tag{3.8}$$

Where R_D is the contact resistance associated with the drain-channel junction, XA is the distance between the drain and point A and V_T is the threshold voltage extracted from the drain-source current vs gate-source voltage characteristics of the four-terminal TFT device. Solving for R_D in equation 3.8 yields:

$$R_D = \frac{V_{D-A}}{I_{DS}} - \frac{XA}{W\mu_n C_{SiNx}(V_{GS} - V_T)} \tag{3.9}$$

Similarly the contact resistance associated with the source-channel junction may be expressed as:

$$R_S = \frac{V_{B-S}}{I_{DS}} - \frac{L - XB}{W\mu_n C_{SiNx}(V_{GS} - V_T)} \tag{3.10}$$

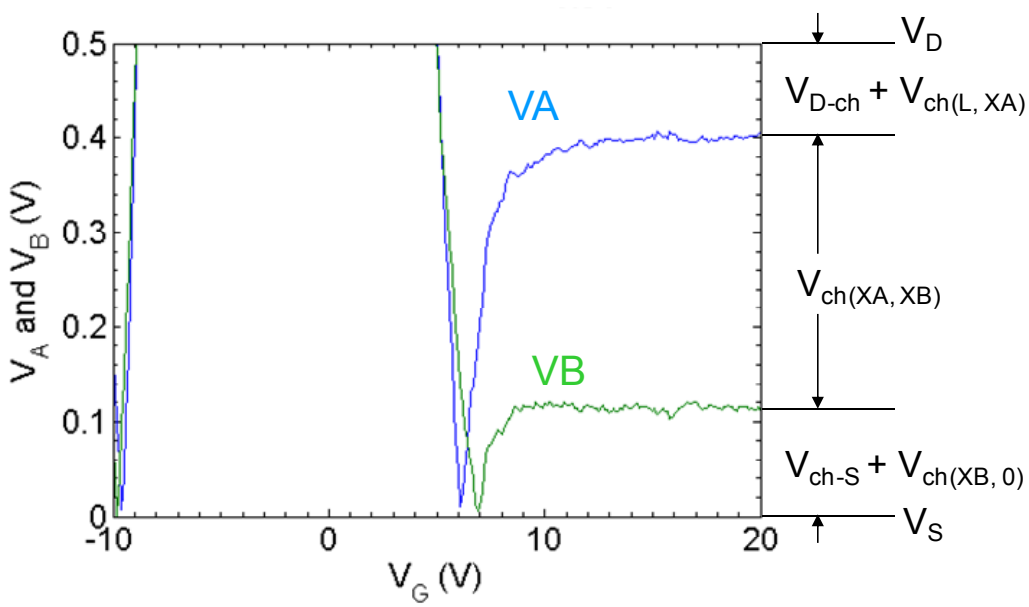


Figure 3.25. Voltages measured on contact A and B in the four-terminal device as a function of the applied gate voltage.

The value of the total contact resistance extracted from the four point probe method was in good agreement with the value obtained from the transmission line method (Figure 3.26). The fact that two independent methods of measuring the contact resistance yielded consistent values

suggests that the analysis and results are correct. The four point probe method also showed that the source and drain contact resistances both decrease with increasing applied gate bias, which is, again, consistent with our model of tunnel injection of electron through a Schottky barrier modulated by the applied gate voltage. However, it is also observed that the source contact resistance is slightly lower than the drain resistance (Figure 3.26). This observation is verified with additional measurements that interchanged the source and drain contacts, which indicated that it was a manifestation of the underlying device physics and not of non-uniformity in the contacts. The precise mechanism that caused this asymmetry in the source and drain contact is unclear, but it may be related to the fact that tunnel barrier at the channel-drain junction is the mirror image of barrier at the source-channel junction. The built-in electric field on the a-Si channel side of the channel-drain Schottky barrier may actually repel incoming electrons, resulting in higher resistance.

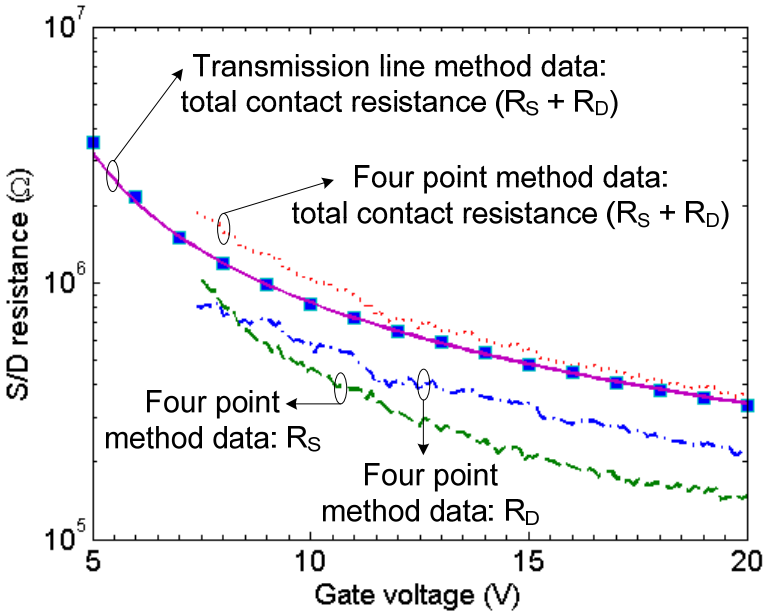


Figure 3.26. Contact resistance extracted from the four point probe method compared with the contact resistance extracted from the transmission line method.

3.4. Device fabrication on clear plastic substrate

The ability to fabricate the top-gate a-Si TFT with a self-aligned silicide source and drain on a flexible substrate which is transparent would enable a variety of application, such flexible

AMOLED displays, flexible sensor arrays and flexible medical image tools, to take advantage of the superior power and speed performance of this device. Plastic substrates are the most promising candidate for this purpose. However, as discussed in section 3.2.3, top-gate a-Si TFT with self-aligned silicide source and drain are fabricated on glass with the highest temperatures (silicidation reaction temperature) being 280°C. Replacing the glass substrates with plastic for the fabrication of this devices imposes strict requirements on the plastic substrates, including (i) high glass transition temperature (>300°C), (ii) low coefficient of thermal expansion (CTE) (<10ppm/°C), (iii) optical transparency, and (iv) vacuum and chemical process compatibility.

3.4.1. Overview of clear plastic substrate

Kapton® is a commercially available high temperature plastic substrate which has been used extensively for the fabrication of a-Si TFTs [47][48][49][50]. However, Kapton® is not optically clear and therefore not suitable for certain applications, such as AMOLED displays with standard bottom-emitting OLEDs. Other commercially available plastic substrates, such as Polyethylene Terephthalate (PET), Polyethylene Naphthalate (PEN) and Poly-Carbonate do not meet the requirements of high glass transition temperature and low coefficient of thermal expansion. Fortunately, our industrial collaborator (DuPont Company) has developed a novel clear plastic substrate that is optically transparent, has a glass transition temperature (>300°C) and low coefficient of thermal expansion. The properties of the novel clear plastic substrate are compared with that of the other commercially available plastic substrates in Table 3.2 [52]. More details regarding the various different properties of the novel clear plastic substrate and its application to high-temperature a-Si TFT processes can be found in Reference [52].

3.4.2. Device Fabrication

When fabricating devices on flexible substrates, it is crucial to carefully control the mechanical stress in the various device layers deposited onto the substrate using the PECVD. Mis-management of the mechanical stress can lead to cracks and even delamination of the films. Previous studies in our group have shown that the mechanical stress in the PECVD-grown layers

can be adjusted by changing the plasma power density [53][54]. Buffer nitride layers of differing thickness are deposited on the two sides of clear plastic at a plasma power density of 200mW/cm^2 resulting in tensile stress in the films, which balances out the compressive stress in the a-Si and gate nitride layers (deposited at plasma power densities of 22mW/cm^2 and 17mW/cm^2 respectively) and top Cr gate metal layer.

Substrate	Optical transmission (λ=700nm)@Thickness	Glass transition temperature (°C)	CTE (ppm/°C)	Max working temperature (°C)
Kapton®	<80% / 125μm	>300°C	20	300
PET	88% / 125μm	70 –110	15	< 120
PEN	82% / 125μm	120	13	130
Poly-Carbonate	90% / 125μm	130	60 –70	120
Clear Plastic	88% / 100 μm	> 300	< 10	300

Table 3.2. Properties of commercially available plastic substrates [52].

Before the actual device fabrication occurs, the clear plastic substrate is thoroughly cleaned by an ultrasonic bath in isopropyl alcohol. The substrate is then subjected to heat treatment at 300°C under vacuum of 10^{-6}Torr for 2 hours, to allow degassing and thermal-induced distortions to occur prior to PECVD deposition. Upon completion of the heat treatment, buffer SiN_x layers are deposited on both sides of the clear plastic substrate. The buffer SiN_x serves three different functions, which are (1) to protect the substrate from subsequent chemical processing, (2) to reduce the surface roughness of the substrate and (3) to provide stress balancing for device layers. The buffer SiN_x deposition is followed by the deposition of the a-Si, SiN_x and gate metal TFT stack. The fabrication process then proceeds the same way as it would on the glass substrate (Section 3.2.3).

It must be noted, however, the clear plastic substrates (and most other commercially available plastic substrates) are destroyed by organic solvents such as acetone. As such, photoresist, used for photo-lithographical definition of device layers, cannot be removed from the sample by conventional means, which involves acetone or a solvent-based stripper. To protect

the clear plastic substrate, the photoresist is removed by flood UV exposure and repeated rinising in the photoresist developer, which is typically a base.

Optical images of the completed sample and device are shown in Figure 3.27. It can be seen that the clear plastic substrate is significantly rougher than the glass substrate (pictured in Figure 3.15 right). This roughness can create problems for device uniformity and yield across the entire sample.

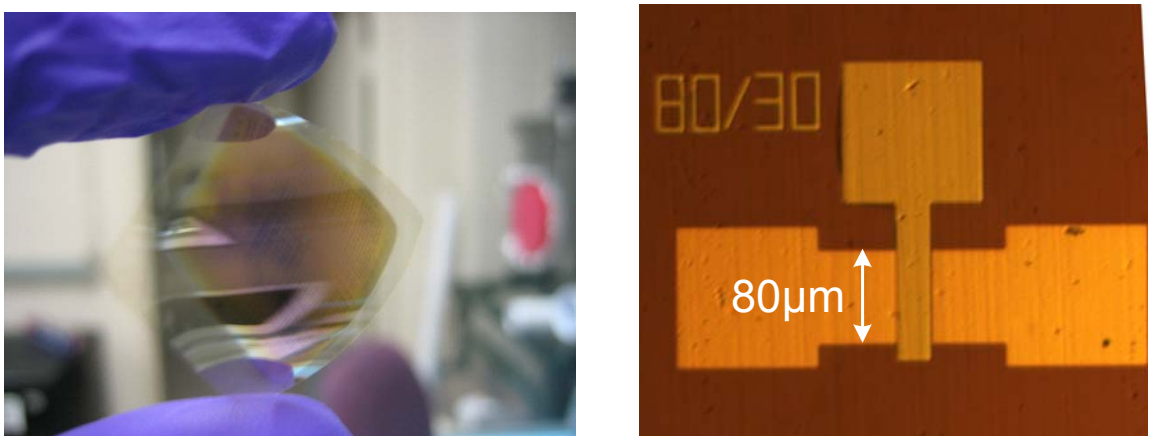


Figure 3.27. Left: photograph of the clear plastic substrate with an array of completed top-gate a-Si TFTs. Right: microscope image of a single top-gate a-Si TFT on the clear plastic substrate.

3.4.3. Device characteristics

The DC transfer characteristics of a typical a-Si top-gate TFT with self-aligned Ni silicide S/D (W/L=80µm/80µm) fabricated on clear plastic substrate at 280°C are plotted in Figure 3.28. The performance metrics were extracted from the saturation curve (V_D = 10V) using conventional MOS theory. The long-channel devices (L > 40µm) exhibited a threshold voltage of 5V, saturation field effect mobility of 0.8cm^2/Vs, subthreshold slope of 700mV/dec and an ON/OFF ratio of ~5x10^5.

The device characteristics of the TFTs fabricated on clear plastic substrate were inferior to that of TFTs fabricated on glass in several ways. The threshold voltage was significantly higher (5V instead of 2.7V). The drain-source leakage current at V_{DS} = 10V and V_{GS} = -10V was 100nA, much higher that of devices on glass. This ambipolar behavior could be a result of hole conduction through the device channel, with the onset of this conduction occurring at about -5V.

However, it is unclear as to why this behavior was observed only in the device fabricated on clear plastic substrate and not in devices fabricated on glass. Furthermore, the transfer curve at V_{DS} = 0.1V exhibited very poor subthreshold characteristics, which did not overlap with that of the transfer curve at V_{DS} = 10V, as it did in TFTs fabricated on glass.

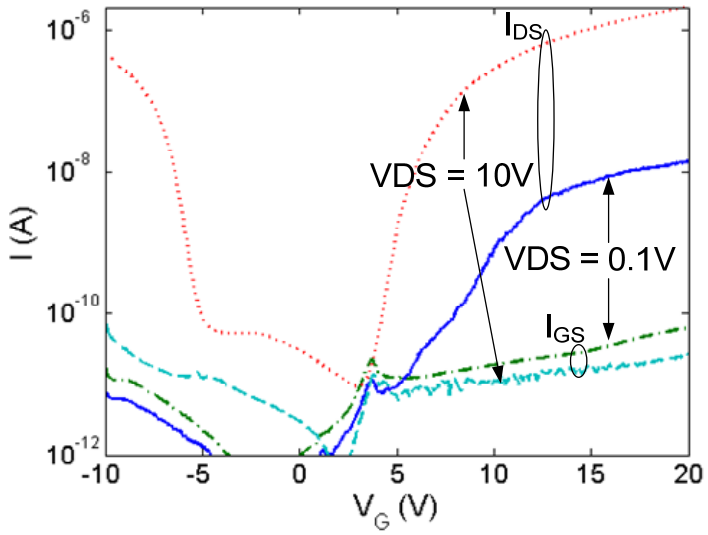


Figure 3.28. Room temperature transfer characteristics (drain current VS gate-source voltage for drain-source bias of 0.1V and 10V) for a top gate α-Si TFT with self-aligned nickel silicide source drain fabricated on clear plastic substrate. W/L=80μm/80μm.

The DC output characteristics (Figure 3.29) of the devices fabricated on clear plastic substrate showed slight concavity at small V_{DS} values, suggesting there is some non-linearity in the contact behavior. This is could explain the poor subthreshold behavior observed in the transfer curve at V_{DS} = 0.1V. The reason for the poorer contact performance in the devices fabricated on clear plastic substrate is unclear, but it may be attributed to roughness-induced changes to the S/D contact interface.

We have successfully demonstrated that the top-gate a-Si TFT with self-aligned silicide source/drain can be fabricated on clear plastic substrate. The devices have promising characteristics such as high saturation field effect mobility, but there are clearly many bugs in the process. Careful process optimization is required to eliminate these bugs and make the devices on plastic comparable to those fabricated on glass substrates.

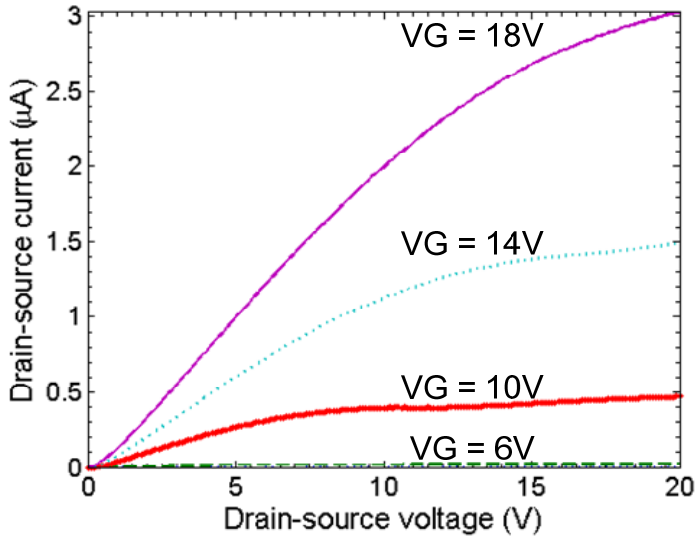


Figure 3.29 Room temperature output characteristics (drain current VS drain-source voltage for gate-source bias from 6V to 18V) of a top gate a-Si TFT with self-aligned silicide source drains fabricated on clear plastic substrate. W/L=80μm/80μm

3.5. Circuit application to ring oscillators

As discussed earlier, the top-gate a-Si TFT with self-aligned silicide source drain is expected to have better speed and power performances compared to conventional bottom-gate a-Si TFTs. A good way to demonstrate this improvement is through integration into ring oscillator circuits. With all other parameters being equal, the ring oscillator made with the top-gate a-Si TFTs with self-aligned silicide source drain should achieve higher oscillation frequency and lower power consumption than the one made with conventional a-Si TFTs.

3.5.1. Simulation

Simulations of the ring oscillator circuits are performed using SPICE. The simulated ring oscillator consisted of seven stages of inverters and one output buffer (Figure 3.30). Since p-channel devices made with a-Si have mobilities about two orders of magnitude lower than n-channel devices, the inverters are made with two n-channel a- Si TFTs in the enhancement load configuration. The pull up TFT has an aspect ratio of 20μm/10μm and the pull down TFT has an aspect ratio of 200μm/10μm (Figure 3.31).

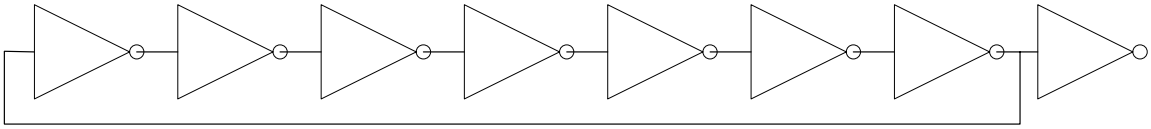
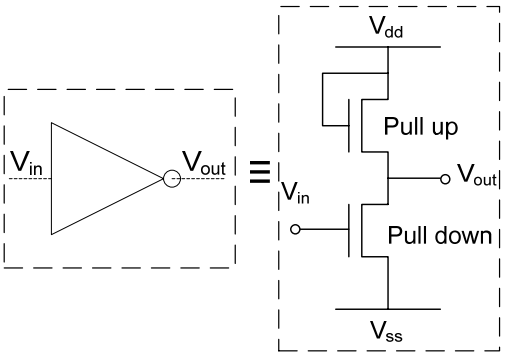


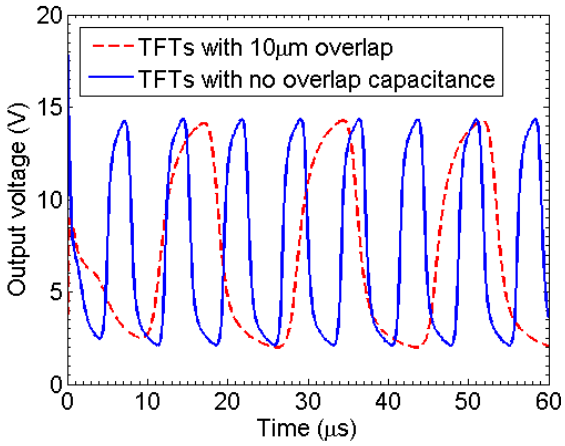
Figure 3.30 SPICE simulation model of a 7-stage ring oscillator



	Conventional TFT	Self-aligned TFT
Pull up size	20μm/10μm	20μm/10μm
Pull down size	200μm/10μm	200μm/10μm
overlap	10μm	0

Figure 3.31 Inverters are made of two n-channel TFTs in the enhancement load configuration. The only difference between the conventional bottom-gate TFT and self-aligned top-gate TFT is the 10μm overlap the gate electrode and the source/drain electrodes.

Our experimental data show that the top-gate a-Si TFT with self-aligned silicide source/drain achieves comparable performance metrics to the conventional bottom gate devices, therefore the only feature that distinguishes the two in the SPICE simulation model is the 10μm overlap between the gate electrode and the source/drain electrode of the conventional device.



	Conventional TFT	Self-aligned TFT
Stage delay	1.24μs	521ns
Average power consumption per stage	0.25mW	0.25mW

Figure 3.32 SPICE simulation output of the 7-stage ring oscillator made with conventional TFTs and self-aligned TFTs. V_{dd} = 20V.

Simulation results show that at a supply voltage (V_{dd}) of 20V, the ring oscillator made with self-aligned TFTs had a stage delay of 521ns, about 2.5X faster than the 1.24μs stage delay

observed in the ring oscillator made with conventional TFTs (Figure 3.32). Despite the dramatic increase in speed, power consumption in the ring oscillator with self-aligned TFT is the same as that of the ring oscillator with conventional TFTs. In ring oscillator circuits, speed is proportional to power consumption. Therefore, achieving faster speed without increasing power consumption implies that the ring oscillator with self-aligned TFT is more power efficient. The simulation results confirm that the self-aligned TFT provides both speed and power improvements over the conventional device.

3.5.2. Ring oscillator fabrication

Fabricating ring oscillator circuits using the top-gate a-Si TFT with self-aligned silicide source/drain involves adding an additional layer of metallization to make the necessary circuit interconnections. The individual transistors are first fabricated using the process described in section 3.2.3, then a blanket layer of insulator (typically PECVD SiNx) is deposited over the entire sample. Via holes are defined using photolithography and a wet etch. The interconnect metallization is deposited and patterned to make the necessary connections between individual transistors to form the ring oscillator circuit. Specifically, as shown in Figure 3.33, the gate of the pull-up transistor is connected with the drain of the pull-up transistor and the source of the pull-up transistor is interconnected with drain of the pull-down transistor. An optical image of the completed ring oscillator circuit is shown in Figure 3.34.

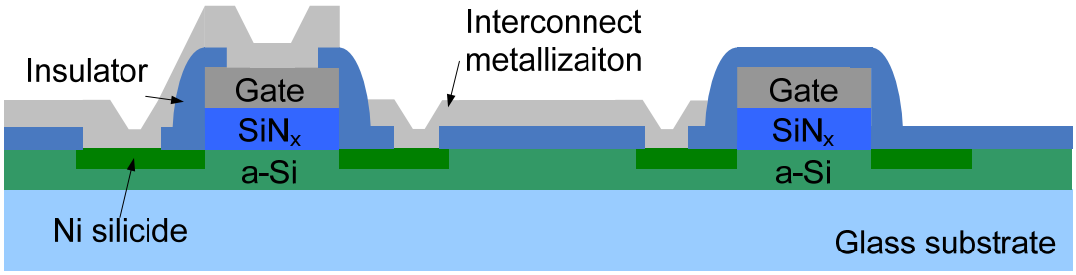


Figure 3.33. Cross section of a portion of the ring oscillator circuit (an inverter) fabricated using the top-gate a-Si TFT with self-aligned silicide source/drain. The gate of the pull-up transistor is connected with the drain of the pull-up transistor and the source of the pull-up transistor is connected with drain of the pull-down transistor.

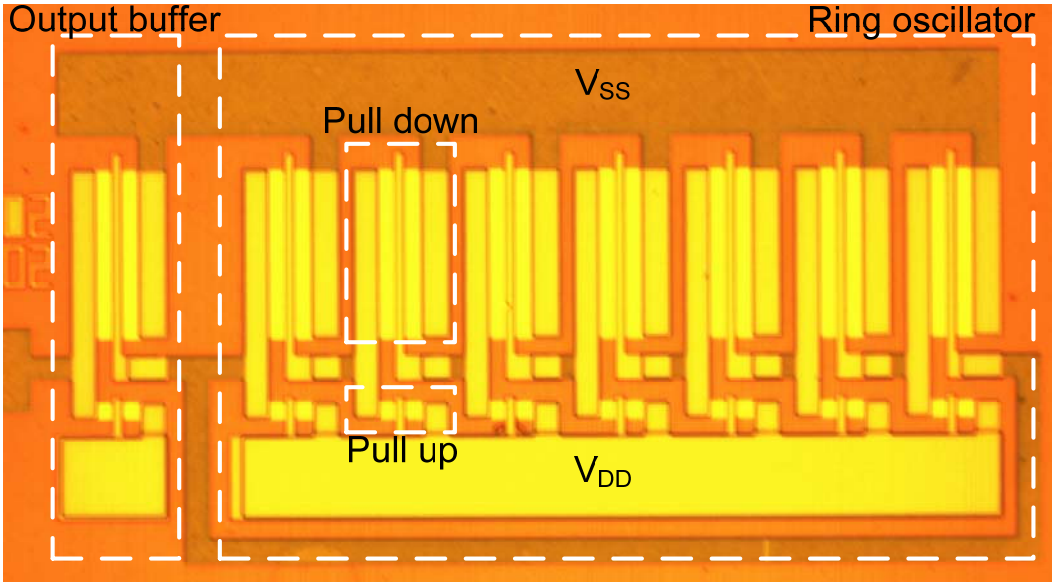


Figure 3.34. Microscope image of the completed ring oscillator circuit.

3.5.3. Electrical performance

The electrical performance of the ring oscillator was characterized at supply voltages (V_{dd}) ranging from 30V to 60V. A sample oscillating output waveform, as measured by the oscilloscope, at V_{dd} = 40V is shown in Figure 3.35. It is observed that peak-to-peak amplitude of the oscillation frequency is only about 0.4V, much smaller than the supply voltage and the value predicted by simulation. It is also observed that oscillation frequency is about 32.5 KHz implying a stage delay of approximately 2μs, which is much longer than the value predicated by simulation. In fact, the stage delay calculated from experimentally observed oscillation frequency is about one order of magnitude larger than the values predicated by simulation at all supply voltage values (Figure 3.36).

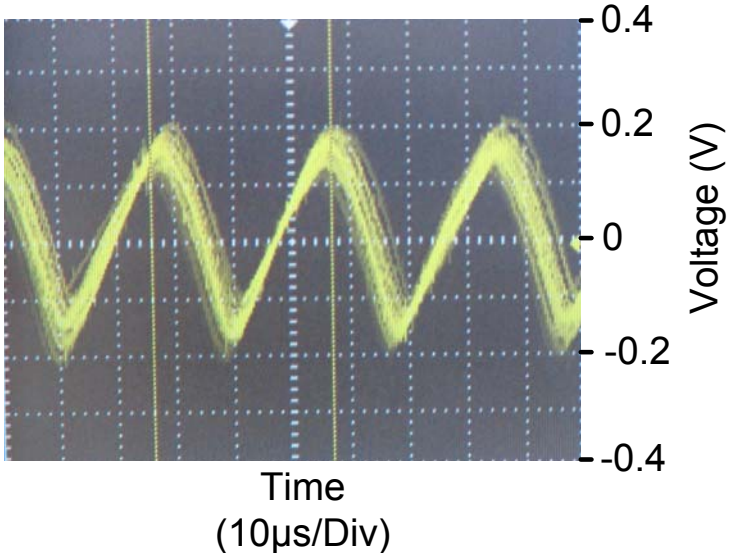


Figure 3.35. Oscilloscope image of the output from a 7-stage ring oscillator fabricated with the a-Si TFT with self-aligned silicide source/drain (V_{dd} = 40V).

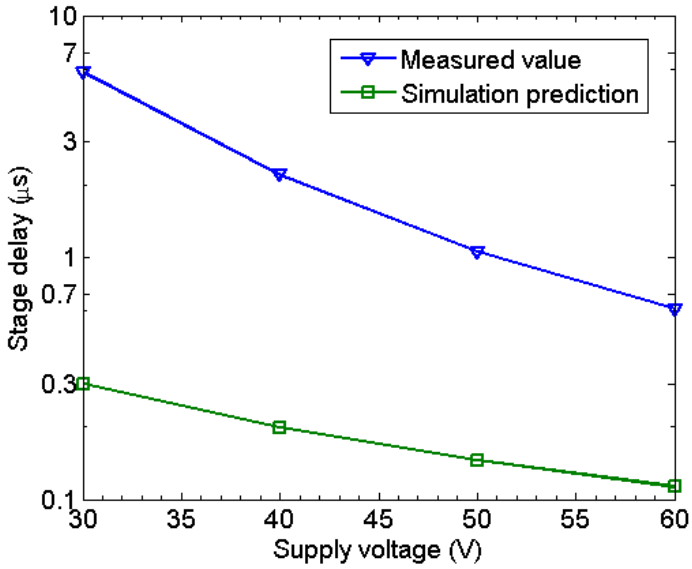


Figure 3.36. Experimentally determined and simulation predicted stage delay as a function of supply voltage (V_{dd}).

3.5.4. Understanding the discrepancy

To understand the reason behind this large discrepancy between the simulation results and experimental data, we look for clues in the characteristics of the individual TFTs. Specifically, we compared the difference in TFT performance before and after the additional processing

(deposition of the insulator, via definition, and deposition of the interconnect metallization) needed to complete the ring oscillator circuit.

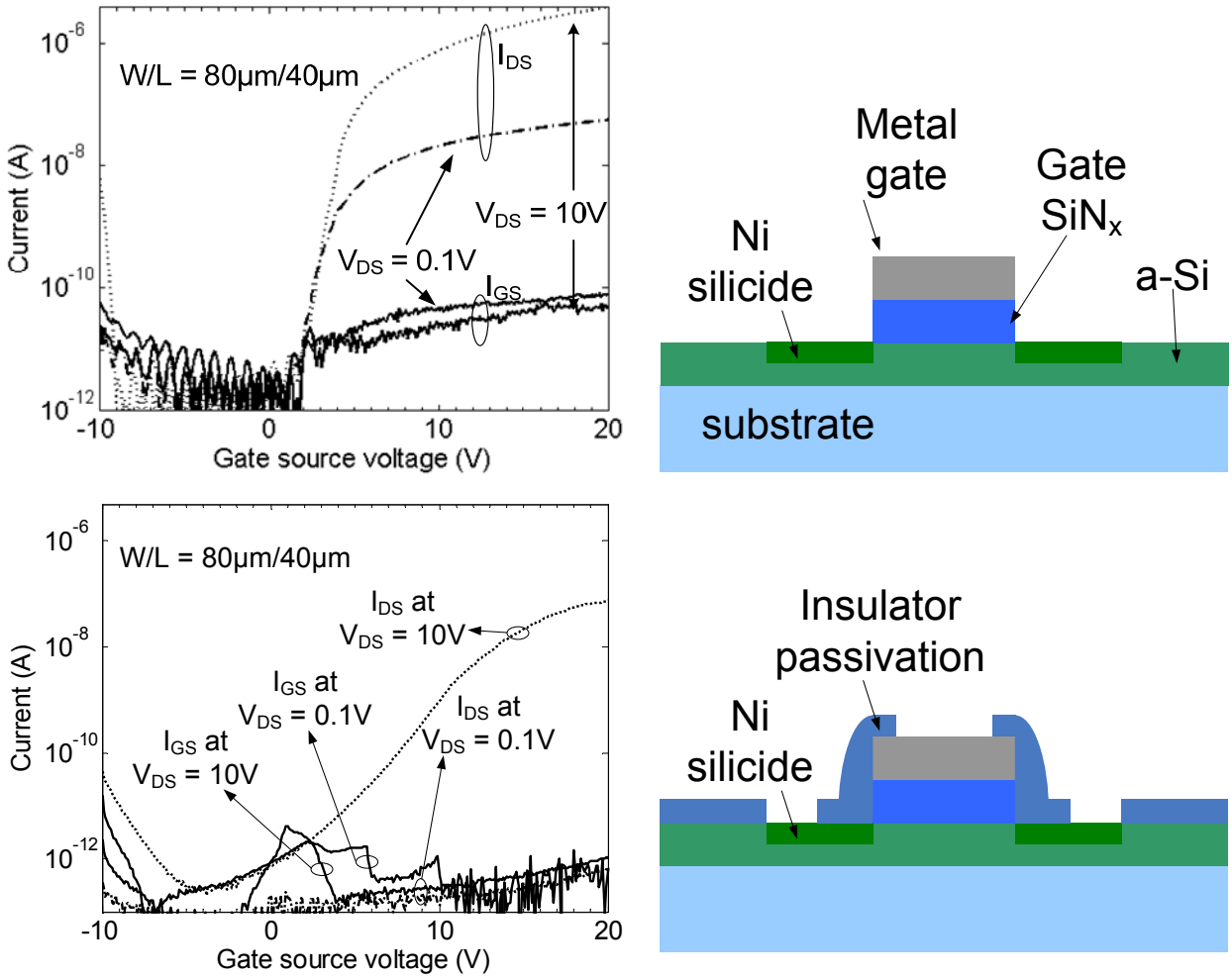


Figure 3.37. TFT characteristics before and after the additional processing necessary to complete the ring oscillator circuit.

It was observed that the a-Si TFT with self-aligned silicide source/drain exhibited excellent characteristics immediately after the completion of individual device fabrication. However, after the deposition of an insulating layer, via definition and deposition of the interconnect metallization, the characteristics degraded significantly. Specifically, as shown in Figure 3.37, the on current of the “after” device with a drain bias of 10V decreases by almost two

orders of magnitude compared to the "before" device; the "after" device does not seem to "turn on" with a drain bias of 0.1V and the subthreshold slope is also significantly higher.

Initial experiments used PECVD SiNx as the insulator layer on top of the TFTs. It was hypothesized that the degradation may be resulting from plasma damage to the devices during insulator deposition. However, similar degradations were observed when PECVD SIO_x, evaporated SiO_x, ALD Al_2O_3 and spin-coated photoresist were used as the insulator. Therefore, it cannot be attributed to plasma damage to the device during insulator deposition.

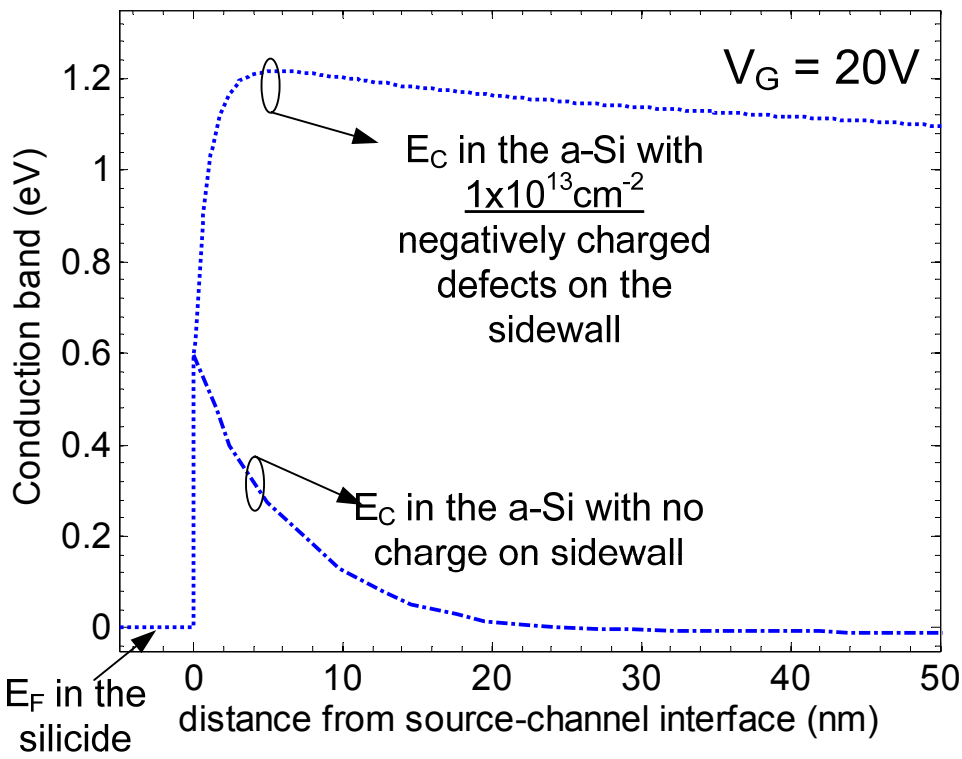


Figure 3.38. Simulated band diagrams of the silicide source-a-Si-channel interface with no charge and 1x10^{-13}cm^{-2} negatively charged defects on the sidewall of the gate dielectric SiN_x. V_{GS} = 20V and V_{DS} = 0V.

One speculative explanation for this phenomenon is that the insulator film on top of the TFTs immobilizes negative charges in the defects on the side wall of the gate dielectric. The negative fixed charges would screen the gate electric field and prevent it from reducing the tunnel barrier thickness at the source-to-channel junction between the silicide and a-Si. Simulation using the same framework as presented in section 3.2.2.2 showed that with 1x10^{13}cm^{-2} negatively

charged defects on the sidewall, the barrier to electron injection from the silicide source into the a-Si channel is significantly larger and thicker (Figure 3.38). As such, the tunnel injection mechanism is effectively “off” and electron would have to be thermally excited over the barrier to get into the channel. This would result in a very large contact resistance, which may lead to the observed device degradation. Without the top insulator, negative charge on the sidewall might migrate to the positive gate electrode when the gate voltage is turned on, removing the blocking effect.

Given that the sidewall of the gate dielectric is formed through a reactive ion etching process, it is very likely to have a high defect density on its surface, which can trap charge and lead to the observed degradation effect. If this is indeed the cause, then the key to mitigating this effect is to minimize the defect density on the sidewall or find an insulator material that can be deposited without immobilizing charge in the defects. Experimentally, whether this is the correct mechanism or not, various different gate dielectric etching methods and insulator materials have been tried, but so far no effective methods or materials have been discovered.

3.6. Summary

The conventional (bottom-gate) a-Si TFT processes require alignment tolerances to prevent device failure. These alignment tolerances lead to parasitic overlap capacitances between the gate and the source/drain electrodes of the device, which are detrimental to the speed and power performances of the circuits using these TFTs. Self-alignment techniques may be used to eliminate these parasitic capacitances. However, conventional approaches for a-Si TFT self-alignment are complex, expensive and incompatible with flexible substrates. We have successfully demonstrated a top-gate a-Si TFT with self-aligned silicide source/drain that is fully compatible with flexible substrates. This device can be fabricated with a simple two-photomask process and it does not require heavily doped source/drain contacts. It exhibits excellent DC electrical performance with the highest saturation field effective mobility ever reported for a top-gate a-Si TFT. It is also fully compatible with fabrication on the clear plastic substrate. Therefore, we believe the top-gate self-aligned silicide contact structure is an attractive path for high-speed

and low power a-Si TFT circuitry on flexible substrates. However, future is still necessary to resolve some of the engineering challenges associated with fabricating circuits using the a-Si TFT with self-aligned silicide source/drain.

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Self-aligned imprint lithography for fabrication of top-gate a-Si TFT with self-aligned silicide source/drain

One of the biggest challenges associated with fabricating large-area electronics circuits on flexible substrates is the deformation of the substrate as a result of thermal and chemical processing. This deformation has significant detrimental impacts on the yield of the process, because it prevents the proper alignment between various device layers. In this chapter, we present an overview of the concept of self-aligned imprint lithography (SAIL), which is a technique that can overcome the difficulties created by substrate deformation. We also demonstrate a SAIL process for the fabrication of the top-gate a-Si TFT with self-aligned silicide source/drain. This work was done in close collaboration with Elisabeth Lausecker from Johannes Kepler University in Linz, Austria and is described in reference [1].

4.1. Motivation

In Chapter 3, the fabrication of the top-gate a-Si TFTs with self-aligned silicide source/drain on a clear plastic substrate using conventional lithography techniques was described. It was noted during that discussion that the stresses in the deposited devices layers must be carefully balanced in order to avoid cracking of the entire stack. An additional effect of the stress, not mentioned in the previous discussion, is the expansion or contraction (depending on the nature of the stress) of the substrate dimensions. In our initial demonstration of device fabrication on a clear plastic substrate (Chapter 3), the active device region was approximately 4cm x 4cm. This area is relatively small and the substrate distortions did not result in severe misalignment that caused device failures. However, in practical large area electronics applications on flexible substrates, which can have dimensions up to ~10 m^2, substrate deformation would lead to significant yield reductions.

The potential device failure due to flexible substrate deformation is illustrated in Figure 4.1 for the two-photomask top-gate a-Si TFT process. To fabricate the top-gate a-Si TFT, the

gate metal layer is first defined and patterned using the photolithography. The chemical and thermal processing between the gate lithography and the source/drain lithography causes the clear plastic substrate to shrink. As a result, lithographic alignment between the gate electrodes and the source/drain photomask is not achievable across the entire substrate. Devices on the edge will not be functional due to severe misalignment.

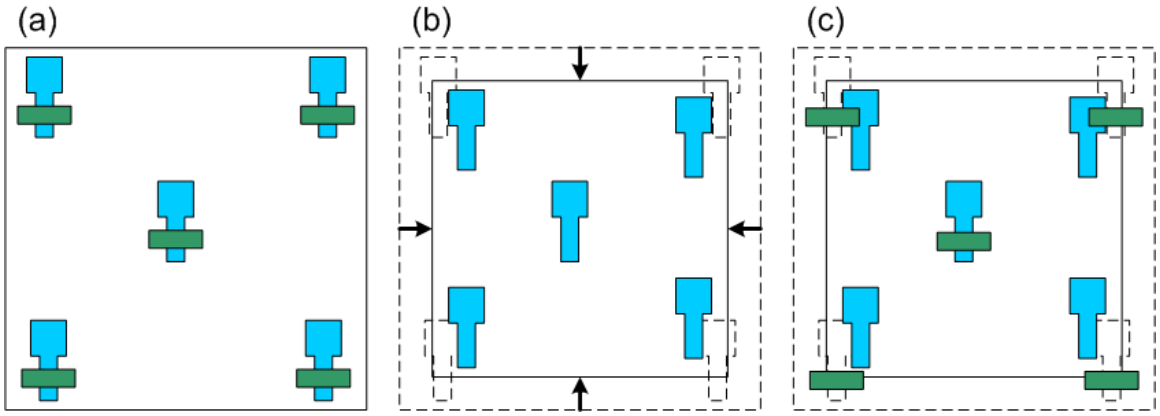

Figure 4.1. (a) proper alignment between gate photomask (blue) and source/drain photomask (green); (b) thermal and chemical processing after gate lithography step causes the substrate to shrink; (c) proper alignment between the patterned gate electrodes and source/drain photomask cannot be achieved across entire substrate leading to failure of the devices on the edge.

While even in a simple two-photomask process substrate deformation can lead to poor process yield, the impact on real-world large electronic circuits on flexible substrate such as x-ray sensor arrays [2] and electronic paper [3][4] will be far more severe. Therefore, precise control over alignment over many device layers is necessary for fabrication on dimensionally unstable substrates. This need has led to the development of many self-aligned photolithographic processes for the fabrication of a-Si TFTs [5][6]. However, to enable low-cost and high throughput fabrication of large-area electronics circuits on flexible substrates, roll-to-roll (R2R) processes based on imprint lithography must eventually be implemented [7][8]. These, however, require even more advanced approaches to self-alignment.

A particularly attractive technique called self-aligned imprint lithography (SAIL) was introduced by Hewlett Packard labs [9][10]. In SAIL, a multilevel mold encodes the geometric information of all device layers, including their alignment, in a three-dimensional imprinted mask.

Each elevation in the imprint mold is the functional equivalent of a photolithographic mask. Thus all mask levels are transferred in a single imprinting step, reducing both time and material costs associated with multiple conventional lithography steps. More importantly, SAIL has the advantage of being immune to substrate dimension changes. Any deformation or distortion of the substrate during processing will equally affect all levels of the imprinted mask, preserving layer-to-layer alignment of all the different device layers. As such, SAIL has the potential to eventually enable the fabrication of devices with submicrometer channel lengths on large, dimensionally unstable substrates, such as flexible plastic substrates.

It is important to note that the “self-aligned” in SAIL refers to the fact that all the device-layer alignment information is encoded in the imprinted multi-level resist structure, and no subsequent manual alignment is required to pattern the device layers. This is different from the “self-aligned” in the top-gate a-Si TFT with self-aligned silicide source/drain, which refers to the fact that the source and drain contacts in the TFT are perfectly adjacent to the edge of the gated channel and there is no overlap between the source/drain and the gate electrodes. SAIL, as proposed by HP labs, can only fabricate bottom-gate a-Si TFTs that have overlaps between the source/drain and gate electrodes. Therefore these TFTs do not have contacts that are “self-aligned” to the gate, and they suffer from the same parasitic overlap capacitances as conventional bottom-gate a-Si TFTs. As we have demonstrated in Chapter 3, the top-gate a-Si TFTs with self-aligned silicide source/drain eliminate the parasitic overlap capacitance, making them a more attractive option for high-speed and low-power large area electronics circuits. Therefore, we introduce a modified SAIL process for the fabrication of the top-gate a-Si TFT with self-aligned silicide source/drain, which achieves “self-alignment” in both senses of the term.

4.2. Mold design and fabrication

The HP SAIL process for bottom-gate a-Si TFTs uses a four-level imprinted mold to define the device layers. In our SAIL process for the top-gate TFT, a three-level imprinted resist topography is sufficient to define all the device layers, which is one level of complexity less than the HP process. The detailed structure and fabrication steps of the three-level mold are

summarized in Figure 4.2. The mold is fabricated by first depositing a 1.1µm-thick silicon dioxide (SiO_2) layer on a 1.1mm-thick Corning 1737 glass slide by plasma-enhanced chemical vapor deposition (PECVD). The SiO_2 is then coated with 60 nm of Chromium (Cr) via thermal evaporation. The three different levels of the mold are realized by multiple steps of partial removal of the protective Cr mask and subsequent reactive-ion etching (RIE) of the exposed SiO_2. The first photolithography step defines the gate structure (Figure 4.2(a)). The Cr in the gate region is removed with a wet etch and the exposed SiO_2 is etched with a CF_4:H_2 plasma, optimized for vertical sidewalls (Section 3.2.3). The depth of this first RIE is d1. The second photolithography defines the S/D areas (Figure 4.2(b)). The Cr in the S/D regions is removed with a wet etch and exposed SiO_2 is etched to a depth of d2. Note that during this second RIE of the SiO_2, the Cr-free gate region defined in the first lithographic step remain unprotected (Figure 4.2(c)). Thus, after the second RIE step, the gate structure defined by the first pattern transfer is etched to a total depth of d1+d2, while the S/D structures defined by the second pattern transfer are only etched to d2 (Figure 4.2(d)). d1 and d2 are approximately 350 nm each. The use of this Cr hard mask approach guarantees perfect “self-alignment” of the S/D to gate boundaries. Finally, the remaining Cr layer is completely removed from the mold surface by using a wet chemical etch (Figure 4.2(e)). The scanning electron microscope image in Figure 4.2(f) shows the three levels of the mold, demonstrating the cross-over of the gate and S/D structures with vertical sidewalls and gapless intersection. Prior to imprinting, the mold surface is made hydrophobic by spincoating the BGL-GZ-83 antisticking layer, which facilitates an easy, nondestructive release of the mold from the resist. The BGL-GZ-83 antisticking layer was developed at Profactor GmbH. During spin-coating of this fluorinated solution, the solvent evaporates and a thin, hydrophobic layer is formed on the mold surface [11]. The hydrophobic layer is fairly robust and can withstand up to 50 imprints without re-application.

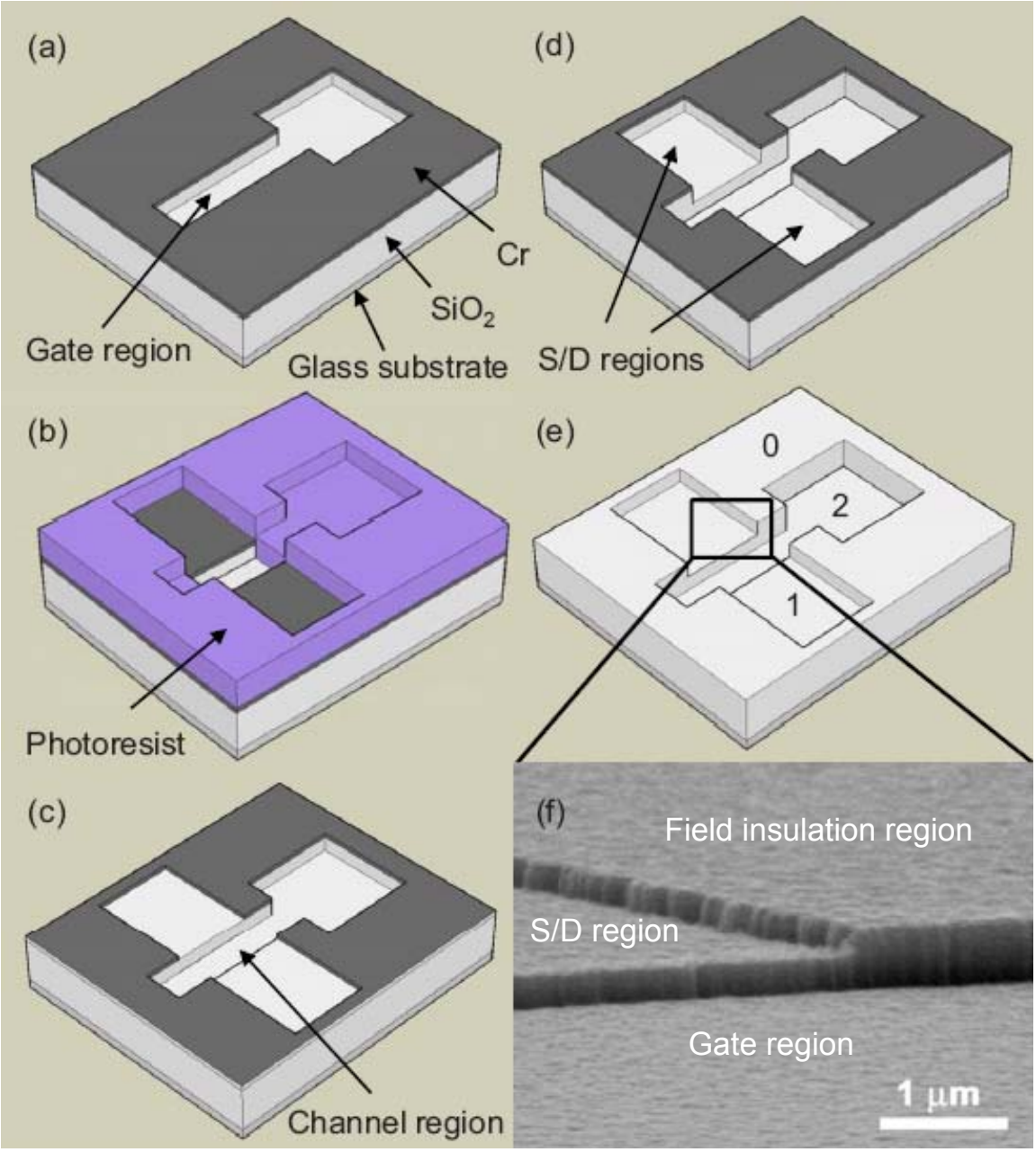

Figure 4.2. Three-level mold fabrication. Source (S) and drain (D) structure is self-aligned to the gate structure for the pattern definition of the top-gate a-Si TFT. The mold blank is a 1.1m-thick SiO2 layer on a glass substrate covered by 60 nm Cr. (a) First photolithography and RIE step defines the gate. (b) Second photolithography defines S and D. (c) Removal of photoresist, note that the Cr layer defines now both S/D and gate. (d) Second RIE step etches S/D and gate structures simultaneously. (e) Removal of Cr layer by wet-etching to expose final three-level mold. (f) Scanning electron microscopy image of the three levels on the mold at the S/D and gate cross-over, as indicated by the black rectangle in (e).

4.3. Device fabrication

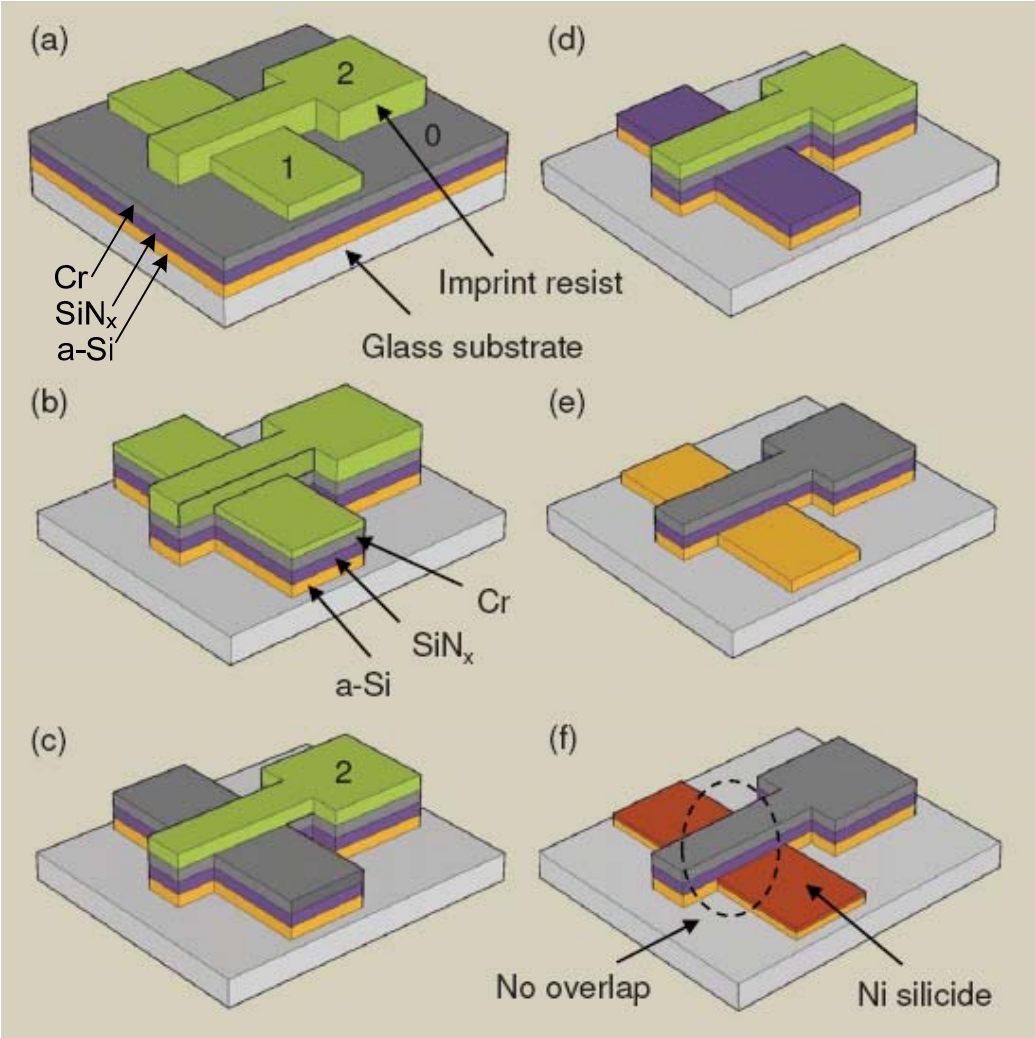

Figure 4.3. SAIL fabrication of the top-gate a-Si TFT with Ni silicide S/D self-aligned to the gate. (a) Three-dimensional imprinted mask on top of the TFT stack after residual resist layer etch at level 0. (b) Electrical separation of TFTs field insulation by RIE. (c) Thinning of the imprint resist to expose level 2. (d) Etching of Cr layer in S/D area. (e) Removal of imprint resist and anisotropic SiNx etch. (f) Blanket deposition of Ni, silicidation step and selective removal of unreacted Ni to expose the finished TFT.

We start SAIL device fabrication by depositing the TFT stack (a-Si, SiN_x and Cr) on a 1.1mm-thick Corning 1737 glass slide by PECVD. The device layers are deposited without breaking the vacuum in the four-chamber PECVD system at pressure and temperature of 500 mTorr and 250 °C, respectively. First, the 100-nm intrinsic a-Si channel layer is deposited using a pure SiH_4 plasma. Then the 180-nm SiN_x gate dielectric layer is deposited using a SiH_4:NH_3

plasma. Finally, 40 nm of Cr is thermally evaporated as the gate metal. The thickness of the layers are reduced from those used in Chapter 3, to ensure that the imprinted resist mask will stand up to the reactive ion etching of various device layers.

A photocurable imprint resist (Nanonex NXR-2010) was applied to the surface of the TFT stack via spin coating. Immediately after the application of the resist, the mold and the sample are brought into contact and placed in a NX-2000 nanoimprinter. The imprinter applies 200psi of pressure via a soft conformal membrane, which presses the mold into the photocurable resist. While maintaining pressure, UV exposure is performed to cure and harden the resist. Upon completion of the curing process, the mold and the sample are separated by injecting air in between them through a fine-tip nozzle. Homogeneous imprints, each containing 256 TFT structures, are achieved over the entire mold area of 1.5in x1.5in. The resulting three-level resist topography on top of the TFT stack defines the insolation, S/D, and gate regions of the TFTs.

Pattern transfer into the deposited TFT stack starts with the etching of the residual resist layer at level 0, exposing the isolation region (Figure 4.3(a)). The ability to anisotropically thin down the resist mask is of crucial importance to keep pattern fidelity during SAIL processing. Therefore we chose the silica-based Nanonex NXR-2010 resist and a CHF_3 plasma at low gas flow (10sccm), low pressure (10mT) and low power density (8mW/cm^2) to etch it (approximate etch rate is 1nm/s). The remaining resist at levels 1 and 2 serve as the etch mask for the reactive ion etching of the gate metal, gate SiN_x and a-Si in the exposed regions (Figure 4.3(b)). This step isolates the individual TFTs from its neighbors. The Cr layer is removed by a short O_2 descum and a subsequent Cl_2:O_2 plasma etch. The etch is followed by a 4 min de-ionized water rinse to reduce metal chloride content on the exposed SiN_x surface, which interferes subsequent processing steps [12]. Then the SiN_x layer is etched in a CF_4:O_2 plasma. Finally, the a-Si is etched in a SF_6 and CCl_2F_2 plasma.

In the next patterning step, the imprint resist is thinned down further to expose the Cr layer in the S/D area (Figure 4.3(c)). Now the resist on level 2, which contains the gate structure and alignment information, serves as the etch mask (Figure 4.3(d)). The Cr in the S/D region is again removed via reactive ion etching, followed by rinsing in de-ionized water. After Cr removal,

the imprinted resist is completely removed from the sample surface with a CHF_3 plasma (Figure 4.3(e)). The SiN_x that covers the a-Si in the S/D area is etched by using the remaining Cr, which is the gate electrode of the TFT, as the hard etch mask (Figure 4.3(e)). To prevent undercutting of the SiN_x gate dielectric, the optimized CF_4:H_2 plasma etch recipe is used to achieve vertical sidewalls (Section 3.2.3). Similar to the regular photolithography process, we want to avoid undercuts that break the electrical contact between S/D and the accumulation layer in the channel. Finally, a 30-nm blanket layer of nickel (Ni) is deposited via electron beam evaporation. Annealing in N_2 ambient at 280°C for 1 hour reacts the Ni with underlying a-Si to form the Ni silicide source/drain regions. The unreacted Ni is removed in a wet-etch of HNO_3:HCl:H_2O =1:5:3 (Figure 4.3(f)).

Because of the vertical sidewalls of the gate SiN_x, achieved by anisotropic etching, the Ni silicide source/drain contacts are perfectly lined with the edge of the gated channel. As such, our SAIL process is “self-aligned” in both senses of the term. It uses a three-dimensional imprinted mask structure that replaces all the manual alignment between device layers and it creates a top-gate a-Si TFT which has source/drain contacts perfectly lined up to the edge of the gated channel.

4.4. Device performance

Our SAIL-fabricated transistors have gate widths (W) ranging from 10μm to 160μm and lengths (L) ranging from 5μm to 80μm. The inset of Figure 4.4 shows an optical microscope image of a top-gate TFT fabricated using SAIL. The DC transfer characteristics of the a-Si top-gate TFT with W/L=80μm/40μm is shown in Figure 4.4. The drain-source and gate currents, I_{DS} and I_G, are plotted versus the gate-source voltage V_{GS} at drain-source voltages of V_{DS}=0.1V and 10 V. The device exhibits the characteristics typical of an enhancement mode MOS transistor with an I_{ON}/ I_{OFF} ratio of 5 x10^4. From the transfer characteristics measured at V_{DS} =10 V, an effective saturation field-effect mobility of 0.4cm^2/Vs is obtained. While this initial demonstration is done on a glass substrate, we have shown in Chapter 3 that this process is fully compatible with flexible substrates.

While we have demonstrated the feasibility of SAIL for top-gate a-Si TFT fabrication, the device electrical performance is much worse than that of the lithographically fabricated TFT. The current data are noisy and there seems to be some non-linearity that is causing the apparent threshold voltage of the linear and saturation curves to differ. However, we believe these are just bugs that can be eliminated by careful optimization of the SAIL fabrication process.

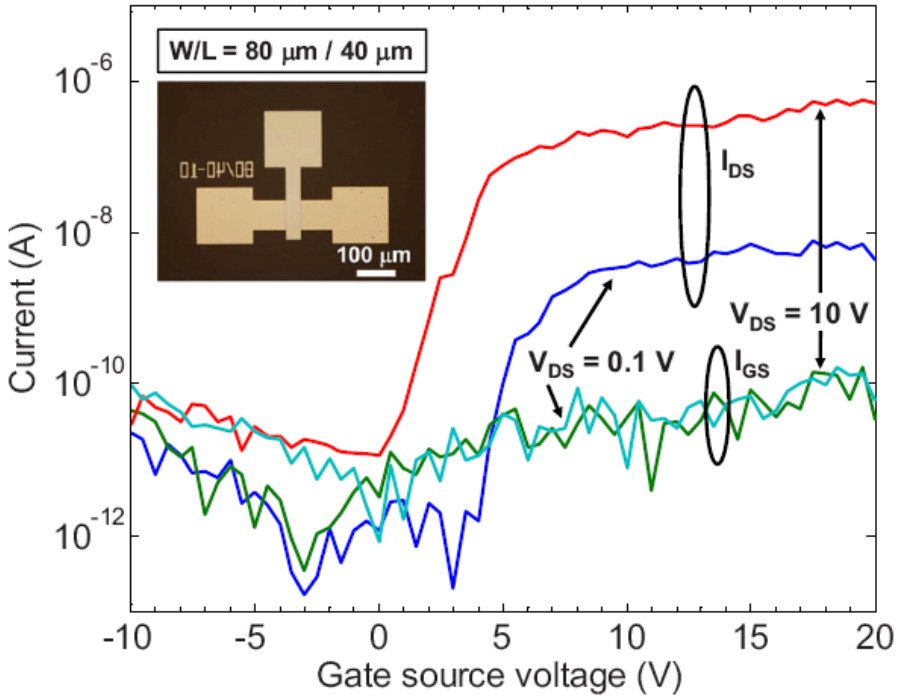

Figure 4.4. Room temperature transfer characteristics (drain current VS gate-source voltage for drain-source bias of 0.1V and 10V) for a top gate α-Si TFT with self-aligned nickel silicide source drain fabricated using the SAIL process. W/L=80μm/40μm Inset shows a microscope image of the completed TFT.

4.5. Summary

Dimensional instabilities of plastic flexible substrates can cause severe misalignment problems and poor yield for the circuits fabricated on these substrates. To combat the yield loss resulting from the dimensional instabilities, HP labs proposed a novel self-aligned imprint lithography technique, which uses a three-dimensional imprinted mask structure that replaces all the manual alignment of device layers. Since all the structural and alignment information needed to define the TFT is contained within the imprinted mask and transferred in one step, this process

is not susceptible alignment problems created by substrate deformation during subsequent processing.

SAIL, as proposed by HP, is limited to bottom-gate a-Si TFT fabrication. Furthermore, it is also designed to fabricate TFTs that have overlaps between the source/drain and gate electrodes, which lead to parasitic capacitances that are detrimental to speed and power performances. Therefore, we proposed and demonstrated a modified SAIL process, which enables the fabrication of top-gate a-Si TFTs with source/drain contacts that are perfectly aligned to the edge of the gated channel. While we successfully show that our SAIL process is feasible for the fabrication of top-gate a-Si TFTs, future work is necessary to improve process reliability and device performance.

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