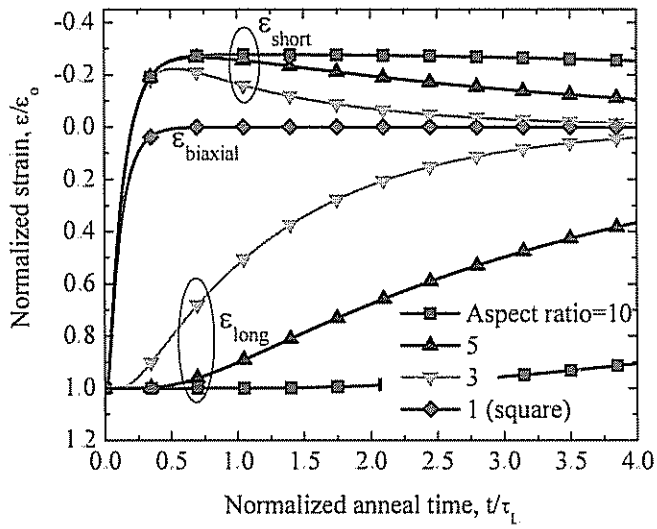


Figure 4.5: Normalized strain at the island center, $\varepsilon/\varepsilon_0$ at $x=y=0$, for a single SiGe layer vs normalized anneal time, t/τ_L, where τ_L is calculated from Eqn. 3.9 with $L=L_{short}=L_{square}$. Shown in the plot are strain in the short direction, ε_{short}, and strain in the long direction, ε_{long}, for rectangles with aspect ratios of 3, 5, and 10, and biaxial strain, $\varepsilon_{biaxial}$, for a square island. At long times, ε_{short} and ε_{long} converge at $\varepsilon_{biaxial}$. The data is from the model presented in Sec. 4.1; symbols are used to differentiate the lines.

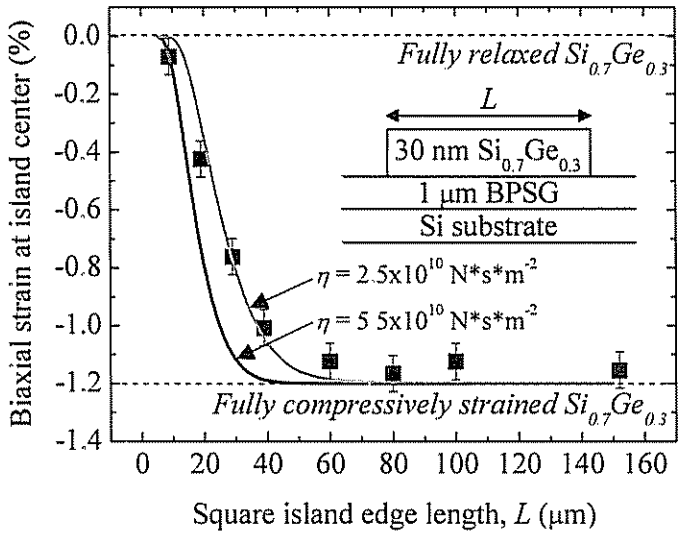


Figure 4.6: Comparison of measured and modeled biaxial strain in SiGe layer for squares of different sizes with edges aligned to <100>, after a 5-min anneal at 750 °C. The inset shows a schematic of the structure cross section. The thin (h_{Si}=1-2 nm) silicon layer between SiGe and BPSG has been omitted for simplicity. The symbols are measured biaxial strain at island center (identical to Fig. 3.23). The solid lines depicts predicted modeled strain at the island center for two viscosities, $\eta=2.5\cdot10^{10}$ and $5.5\cdot10^{10}$ N·s·m^{-2}, as labeled. The dashed lines indicate fully strained and fully relaxed $Si_{0.7}Ge_{0.3}$.

However in Fig. 4.6 the experimental data clearly are better matched to the model curve for η=2.5·10^{10} N·s·m^{-2}. This discrepancy between viscosity values fitted for the two different experiments is thought not to be due to experimental error in the second set of data.

The BPSG used in Ref. [111] was similarly prepared (by Northrop Grumman) to that used here but was much thinner, ~200 nm. Therefore is it possible that processing effects have changed the viscosity. Specifically, following the BPSG deposition by CVD the wafers were wet oxidized to densify the glass as part of Northrop Grumman's standard procedure. This densification step has been shown to drastically increase the effective viscosity of thin BPSG layers. For a 50-nm BPSG layer prepared using the same CVD process, no SiGe relaxation was observed at 750 or 800°C, unlike the thicker BPSG layers [153]. At 900°C partial SiGe relaxation was observed, and a viscosity value of η=3.3·10^{11} N·s·m^{-2} was obtained by curve-fitting assuming a model with a single, uniform BPSG layer as in Fig. 4.6. This value is ~400x greater than the value expected by extrapolating from previously measured viscosities for thicker BPSG (Fig. 3.4). It is believed that this increase in viscosity is due the creation of a thermal oxide layer under or inter-mixed with the BPSG because thermal oxide (without high boron or phosphorus concentrations) is known to have a very high viscosity [105-108], and because an increase in glass thickness (from 50 to 95 nm) was also observed after the wet oxidation step. The thinner the BPSG layer, the higher the linear (diffusion-based) thermal oxidation rate, and therefore a more pronounced viscosity increase is expected. In our case, thermal oxidation of a 1-μm BPSG layer is very slow, and thus its viscosity lower than that measured previously for thinner layers. By modifying the BPSG process (*e.g.*, switching the post-deposition step from wet oxidation to N_2 anneal), it should be possible to eliminate this viscosity dependence on BPSG layer thickness. In any case, it is clear that by a simple experiment of square island relaxation, it is possible to characterize the BPSG viscosity by comparison to the 2-D lateral relaxation model.

In Fig. 4.7 the modeled biaxial strain is shown on a semi-log plot (the data are identical to the linear plot of Fig. 4.5). From Fig. 4.7, it is clear that strain decreases exponentially with time, according to the time constant, τ_L. Curve-fitting the model between $0.035 \leq t/\tau_L \leq 1.1$, the following fitting result (with R^2=0.999999) is obtained:

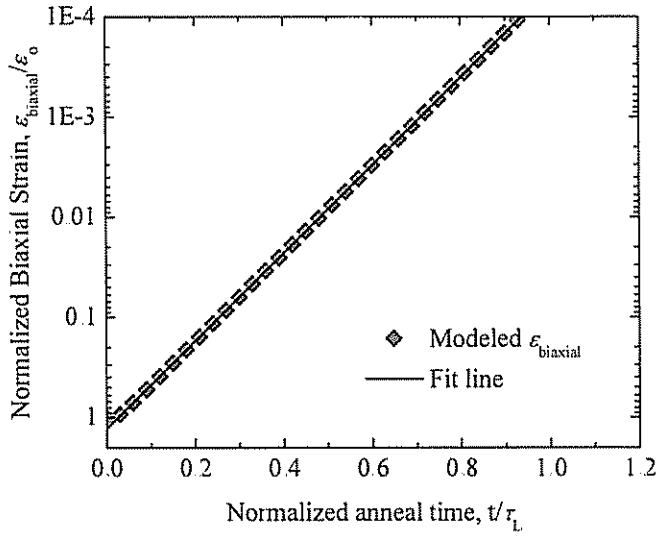


Figure 4.7: Normalized biaxial strain at the center of a square island, $\varepsilon_{biaxial}/\varepsilon_o$, vs. normalized anneal time, t/τ_L, plotted on a semi-log plot. The model results are plotted with symbols. For clarity, only one out of every 300 simulation points is plotted. The model curve is fitted between $0.035 \leq t/\tau_L \leq 1.1$ to the exponential function $\varepsilon_{biaxial}/\varepsilon_o(t) = 1.31 \cdot e^{-10.1\, t/\tau_L}$ with R^2=0.999999, as represented by the solid line. The two curves disagree only at the very beginning, for $t/\tau_L < 0.035$, which corresponds to $\varepsilon_{biaxial}/\varepsilon_o > 0.90$. The exponential nature of the relaxation process is evident.

$$\varepsilon_{biaxial}/\varepsilon_o(t) = 1.31 \cdot e^{-10.1\, t/\tau_L}. \quad (4.8)$$

Clearly, the value of τ_L is an exponential constant which governs the lateral relaxation process. The majority of the 10.1 factor dividing τ_L comes from the value of π^2, which was omitted in the original definition [142] of τ_L repeated in Eqn. 3.9, but should be included in the solution of any differential equation with the form of $\frac{\partial u}{\partial t} = \Omega \frac{\partial^2 u}{\partial x^2}$ (where Ω is a constant), which characterizes Eqn. 4.5 [152,154].

In summary, in this section the lateral relaxation of square islands has been modeled as described in Sec. 4.1. The model results show that biaxial strain decreases exponentially with time, according to the lateral relaxation time constant, τ_L. By comparing model and experimental data, the viscosity of the BPSG can be determined. In the next section, this model is applied to rectangular islands.

4.3 Lateral Expansion of Rectangular Islands

In Ch. 3, experiments showed that by using square and rectangular island geometries, the lateral relaxation process could be used to obtain biaxial and uniaxial SiGe stress. The previous two sections have described a 2-D model for the lateral relaxation process, and have shown that for square islands, the model results closely match experimental data, providing that the correct viscosity value is used. In this section, the models will be extended to rectangular islands of different aspect ratios in order to study the generation of uniaxial stress.

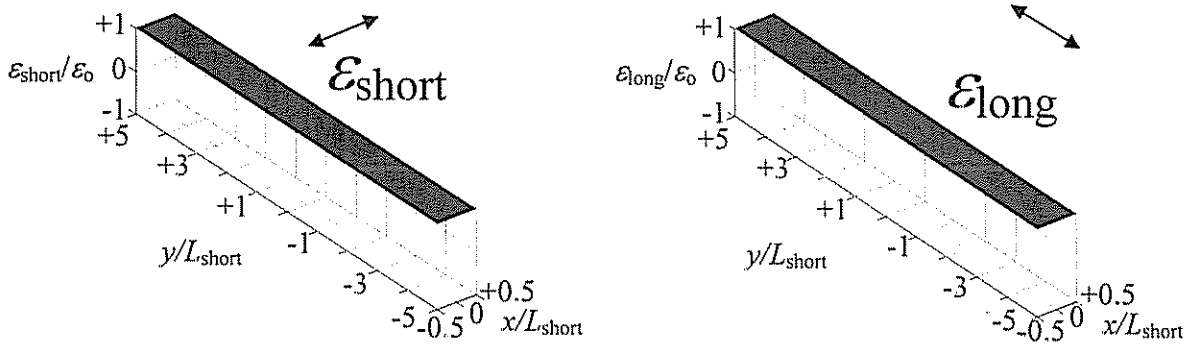
The 2-D numerical simulations of lateral relaxation for square islands were repeated using rectangular arrays of u, v, ε_{short} and ε_{long} (Eqns. 4.3 and 4.5), in order to represent rectangular islands. All other aspects of the simulation were unchanged from those presented in Sections 4.1 and 4.2, and the full *matlab* simulation script may be found in App. C.

In Fig. 4.3b, the normalized strain across the short dimension of a rectangle, $\varepsilon_{short}/\varepsilon_o$, is plotted for an island with $L_{long} = 10\ L_{short}$. For ease of comparison with the

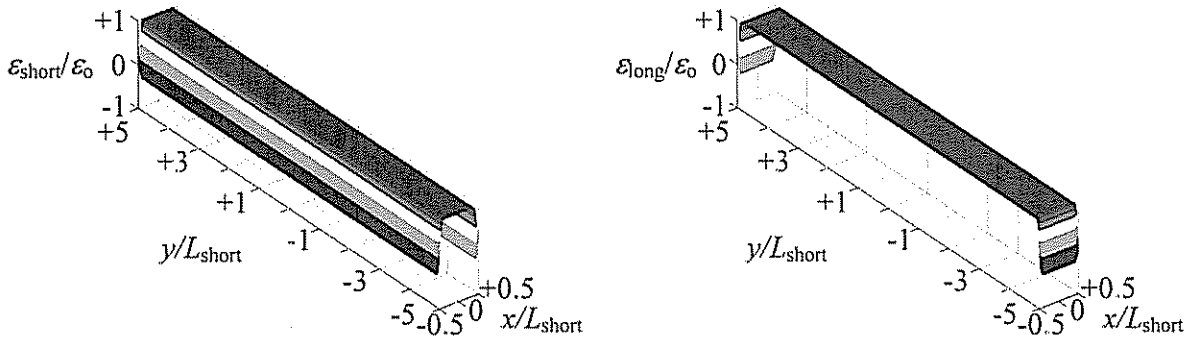
square simulation results plotted in Fig. 4.3a, τ_L is calculated with $L_{short} = L_{square}$. The curves look similar to those of the square, but this time the final simulation curve indicates uniform tension in the short direction. From Eqn. 3.10, the maximum normalized tension is equal to $-\nu$, and thus depends on the film material properties and island crystal direction. For $Si_{0.7}Ge_{0.3}$ aligned to <100>, $\nu = 0.28$ (Eqn. 3.12). At the final simulation time, when $t/\tau_L = 0.5$, $\varepsilon_{short}/\varepsilon_0 = -0.26 \pm 0.01$, that is, the maximum tensile strain has been achieved, and this strain is highly uniform across the island. The bottom plot, Fig. 4.3c, shows normalized strain across the long dimension of the same rectangle, $\varepsilon_{long}/\varepsilon_0$. Again, the strain gradually relaxes with time. However, for the longest anneal time simulated ($t/\tau_L = 0.5$), the majority of the island still remains fully compressively strained in the long direction: the center 70% of the island has normalized strain of greater than 90% in the long direction. Therefore, at $t/\tau_L = 0.5$, the strain is quite uniform across the rectangular island, *i.e.*, for the samples shown here, across an area of > 2,000 μm^2. Thus, our dynamic model yields a metastable solution for the uniaxial stress condition in precise agreement with the Poisson theory of Ch. 3 (which predicts only the end point): a biaxially strained SiGe layer, patterned into a rectangle and annealed, will have compression in the long direction and tension in the short direction.

Three-dimensional plots of ε_{short} and ε_{long} for a rectangle with an aspect ratio (AR) of 10 are shown for various anneal times in Fig. 4.8. The strain asymmetry is readily apparent: at the final simulation time the short direction is strongly tensile, while the long direction maintains its initial compressive strain, at least in the middle region, just as shown in Figs. 4.3b and 4.3c. This is in stark contrast to the similar plots for square islands in Fig. 4.4, where ε_{xx} and ε_{yy} were shown to be identical.

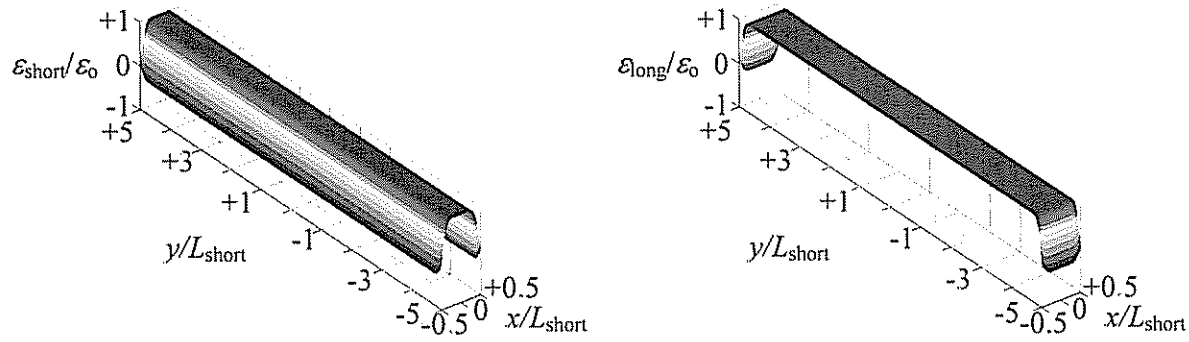
Also, the island edges in Figs. 4.3a and 4.3b, as well as Figs. 4.4 and 4.8, show the Poisson effect at work. The compression in the center of the island initially forces the edges to become tensile, regardless of the island geometry (Figs. 4.3a and 4.3b). For squares, the edges (Fig. 4.3a) and especially the corners (Fig. 4.4) quickly relax back to zero strain as the entire island relaxes. However for rectangles, the compressive strain in the long direction maintains the Poisson effect, forcing the edges perpendicular to the short direction to remain tensilely strained.



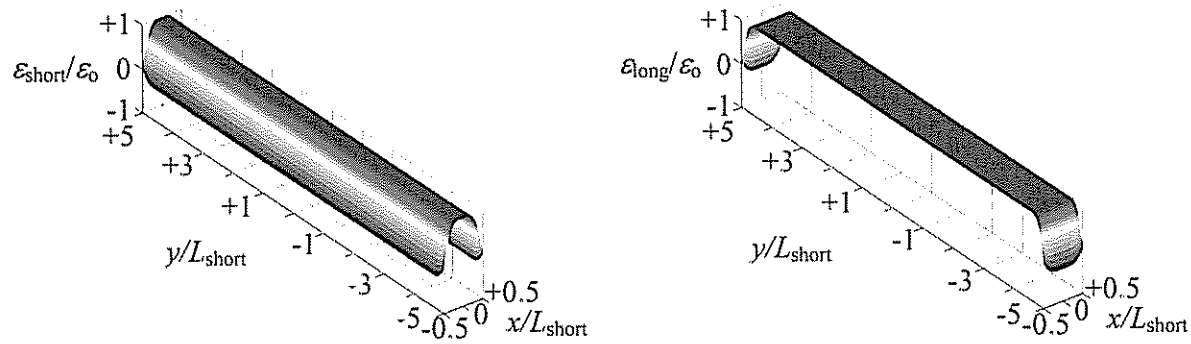
(a) $t/\tau_L = 0$ Film is initially in full biaxial compression.



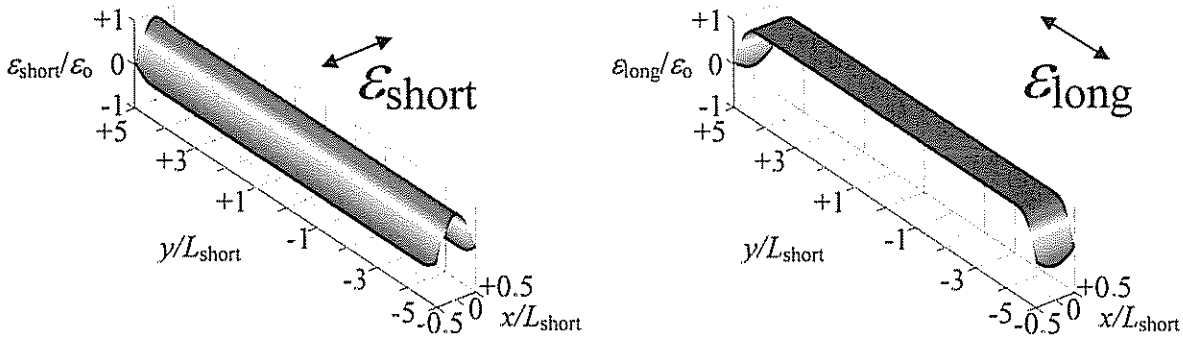
(b) $t/\tau_L = 0.001$ Edges immediately relax.



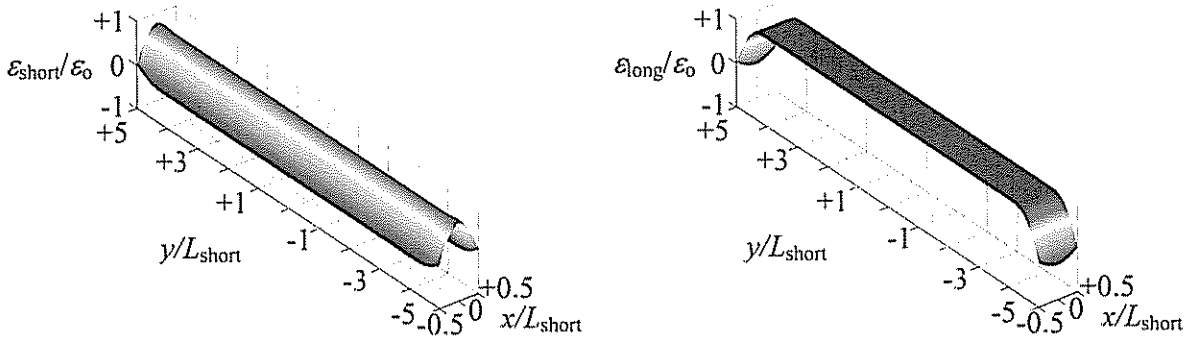
(c) $t/\tau_L = 0.005$



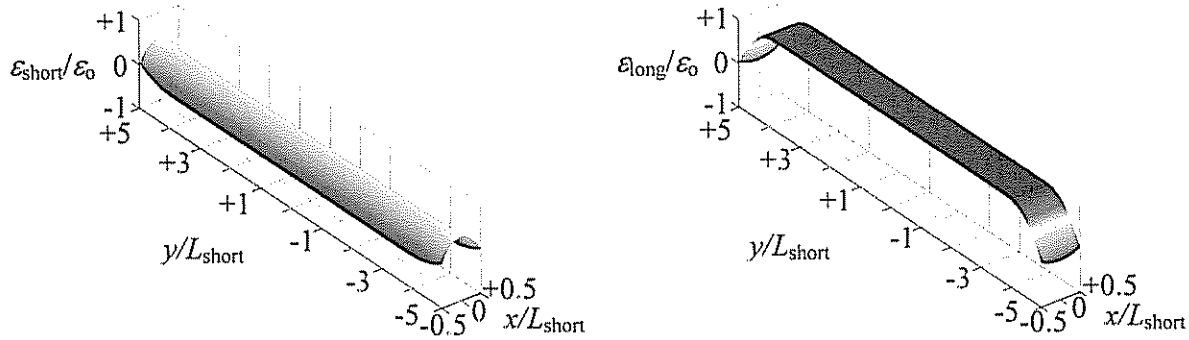
(d) $t/\tau_L = 0.01$ Relaxation moves to center.



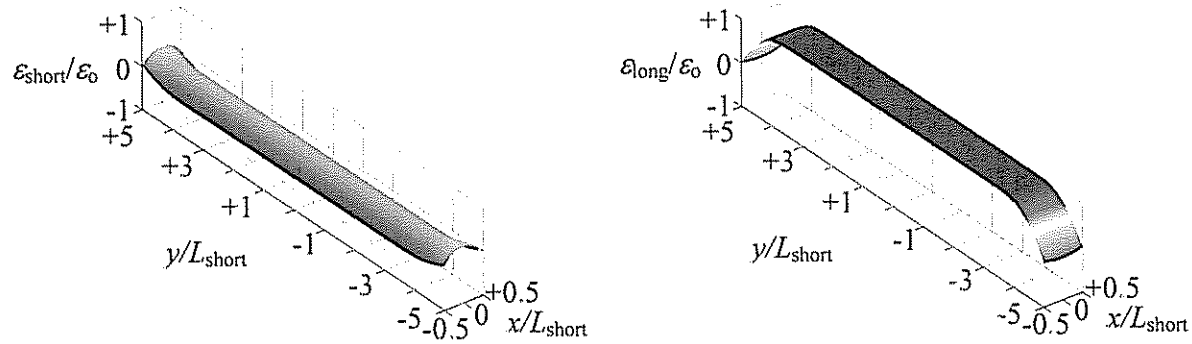
(e) $t/\tau_L = 0.03$



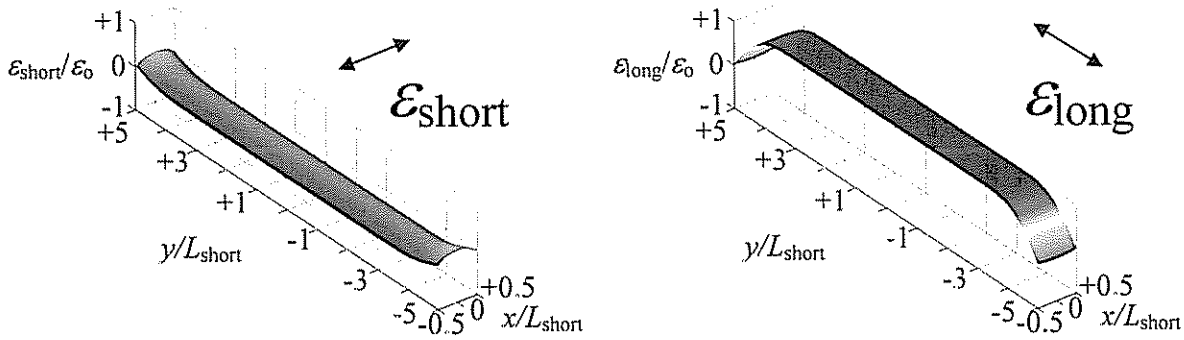
(f) $t/\tau_L = 0.05$ Center begins to relax in short direction creating asymmetric strain.



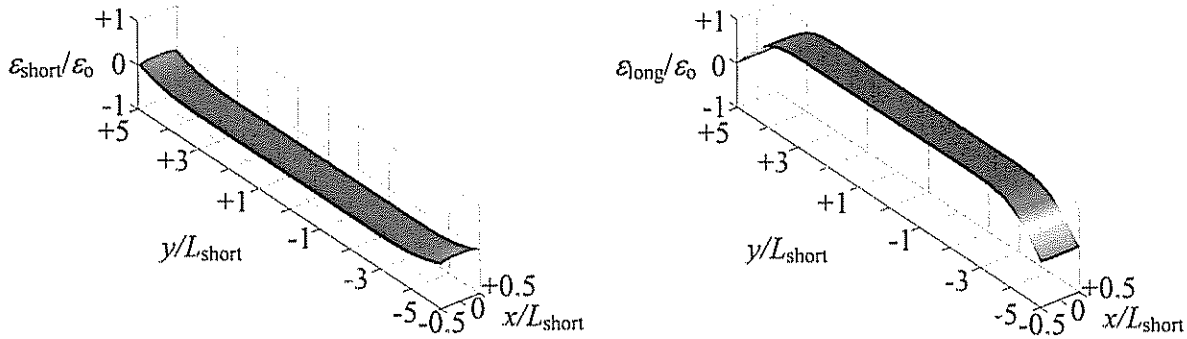
(g) $t/\tau_L = 0.10$



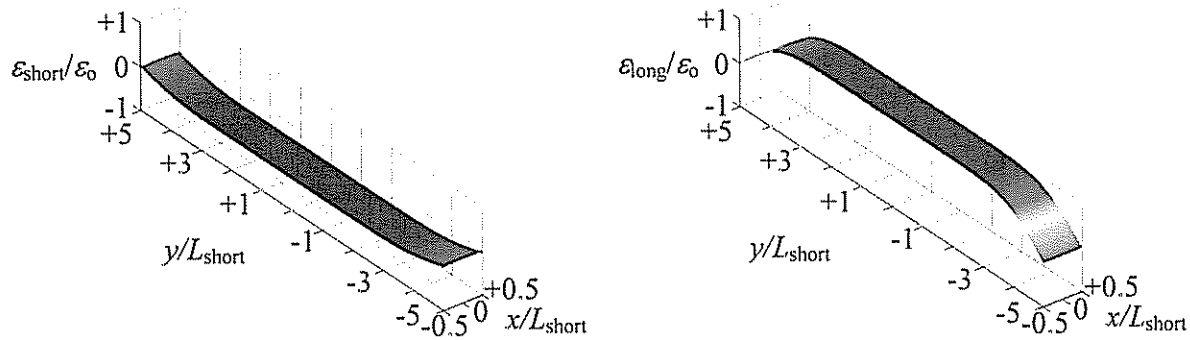
(h) $t/\tau_L = 0.15$



(i) $t/\tau_L = 0.20$ Tension in the short-direction can now be observed.



(j) $t/\tau_L = 0.30$



(k) $t/\tau_L = 0.50$ Tension in short direction and compression in long direction.

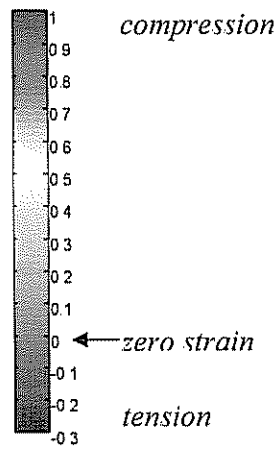


Figure 4.8: Numerical model of strain in a rectangular island vs relaxation anneal time. The island, with $L_{long} = 10$ L_{short}, consists of a single $Si_{0.7}Ge_{0.3}$ layer initially fully compressively strained, with island edges aligned to the <100> crystal directions. Strain in the short direction, plotted on the left, and strain in the long direction, plotted on the right, are normalized as in Fig. 4.3. Time is normalized by τ_L from Eqn. 3.9, with L replaced by L_{short}. At the final simulation time the island has highly anisotropic strain.

4.4 Process Windows for Maximum Strain Asymmetry

So far, only very narrow, long rectangular islands (AR=10) have been discussed. For such structures, the anisotropic strain state will persist for quite long anneals. However eventually the long island direction will also relax. This is because the final equilibrium state for all island shapes and sizes is the same: full relaxation in both in-plane directions. Clearly, the aspect ratio of the rectangle (defined as L_{long} / L_{short}) plays a critical role in determining the existence and length of a process window for maximum anisotropy of strain and, as discussed in Chapter 5, uniaxial silicon strain. To investigate, numerical simulations of lateral relaxation were performed using Eqns. 4.3 and 4.5 for rectangles with various aspect ratios. In Fig. 4.5, strain at the island center is plotted vs anneal time for rectangular islands with aspect ratios of 3, 5, and 10, and for square islands. Initially, the rectangular islands generate highly asymmetric strain, with the long direction maintaining initial compressive strain and the short direction becoming tensile. As the anneal progresses, the compressive strain in the long direction begins to relax to zero. As this occurs, the driving force for tension in the short direction is removed, and the tensile strain in the short direction also relaxes toward zero. Eventually, ε_{short} and ε_{long} for rectangles converge to the same value as $\varepsilon_{biaxial}$, for squares—both the long and short directions fully relax to zero strain (and zero stress). The higher the aspect ratio of the island rectangle, the longer the process window before such convergence occurs. As shown in Fig. 4.5, for rectangles with an aspect ratio of 10, the uniaxial strain is still fully present at the longest anneal time simulated, t/τ_L =4.0, whereas for this same time, islands with aspect ratios of 3 have completely lost their uniaxial strain and have nearly identical strain to the square island.

A desirable technological goal is to achieve maximum asymmetry of strain in the two in-plane directions. This asymmetry is defined as $\varepsilon_{short} - \varepsilon_{long}$ and plotted normalized by ε_o for various rectangular island aspect ratios in Fig. 4.9. For squares, there is never any asymmetry: $\varepsilon_{short} - \varepsilon_{long} \equiv 0$. For rectangles, the strain asymmetry increases as the short direction relaxes, and then as the long direction relaxes, the asymmetry decreases to zero. For rectangular islands with aspect ratios of 4 or more, the maximum possible asymmetry of $\varepsilon_{short} - \varepsilon_{long} = -(1+\nu)\varepsilon_o$ is achievable before the asymmetry falls to zero. A

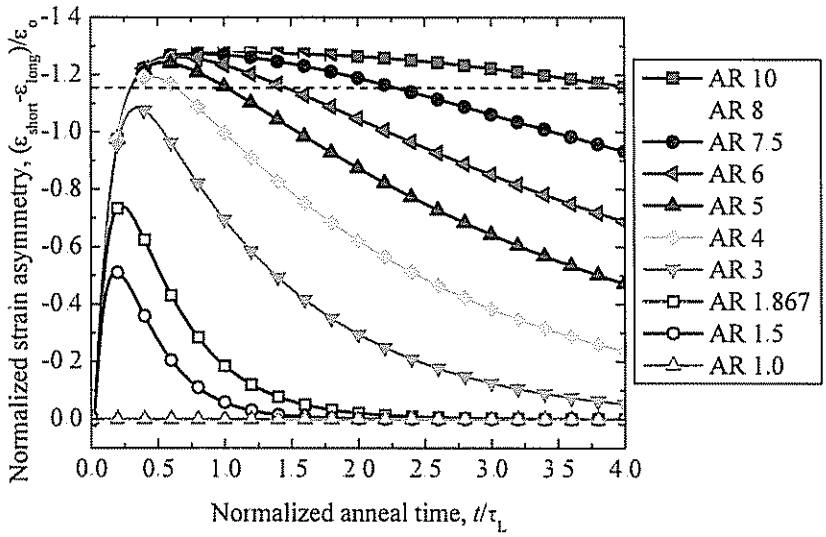


Figure 4.9: Normalized strain asymmetry, $(\varepsilon_{short} - \varepsilon_{long})/\varepsilon_o$, vs normalized anneal time. Strain asymmetry for a single SiGe layer is plotted for rectangular islands with different aspect ratios. The data are from the model of Sec. 4.1; symbols are used to differentiate the lines. Aspect ratios of 4 or more are needed to obtain maximum asymmetry of strain. Strain and time are normalized as in previous figures. The dashed line indicates the point at which 90% of the maximum possible strain asymmetry is achieved; these process windows for uniaxial strain are listed in Table 4.1.

Aspect Ratio	10	8	7.5	6	5	4	3
Maximum strain asymmetry	-1.276	-1.274	-1.273	-1.262	-1.242	-1.195	-1.084
t/τ_L start	0.302	0.302	0.302	0.302	0.303	0.314	–
t/τ_L end	~4	2.653	2.332	1.494	1.038	0.651	–
$\Delta t/\tau_L$ for maximum asymmetry	3.698	2.351	2.030	1.192	0.735	0.337	0

Table 4.1: Process windows for maximum strain asymmetry for rectangular islands of various aspect ratios, taken from the data plotted in Fig. 4.9. The maximum normalized strain asymmetry, $(\varepsilon_{short} - \varepsilon_{long})/\varepsilon_o$, is given; aspect ratios of 4 or greater are needed to obtain maximum asymmetry. The process windows, identified by starting and ending anneal times normalized by τ_L, are calculated when the strain asymmetry exceeds 90% of the maximum possible value: $(\varepsilon_{short} - \varepsilon_{long})/\varepsilon_o < -1.149$. The width of the process window for maximum strain asymmetry increases with the island aspect ratio.

process window for maximum strain asymmetry then exists: for an island with an aspect ratio of 5, the strain asymmetry is at least 90% of its maximum value from t/τ_L=0.30 to 1.04, as seen in Fig. 4.9. The process window widths for various aspect ratio islands are tabulated in Table 4.1, and plotted in Fig. 4.10. If an island has an aspect ratio of three or less, the long and short sides are too close in length, relaxing on similar time scales, so it is difficult to exploit the L^2 dependence of τ_L that drives strain asymmetry. In Fig. 4.9 this is shown by the curves for aspect ratios 3.0, 1.867 and 1.5, which never reach the maximum asymmetry value. For higher aspect ratio islands, a process window for maximum strain asymmetry exists. As the island aspect ratio increases, the process window widens signficantly as shown in Fig. 4.10. For an island with the cross section shown in the Fig. 4.6, with L_{long} = 150 μm and L_{short} = 30 μm, our model predicts a generous process window yielding greater than 90% of the maximum asymmetric strain for 750 °C anneals between 0.9 and 3.1 h in length.

4.5 Comparison of Model and Experimental Data for Rectangular Islands

Finally, in Fig. 4.11 these simulation results are compared to the measured asymmetric SiGe strain plotted in Figs. 3.27. Solid lines represent modeled strains at the island center for the two viscosity values discussed above in Sec. 4.2. The good agreement of the dynamic model (for η=2.5·10^{10} N·s·m^{-2}) and experimental data for both square and rectangular islands demonstrates the high level of control and predictability that our strain generation process affords.

The model also predicts that for the given anneal all islands are characterized by $\varepsilon_{long} = \varepsilon_0$ (at the island center), which justifies using this assumption in analyzing the Raman data to calculate ε_{short} as described in Ch. 3.

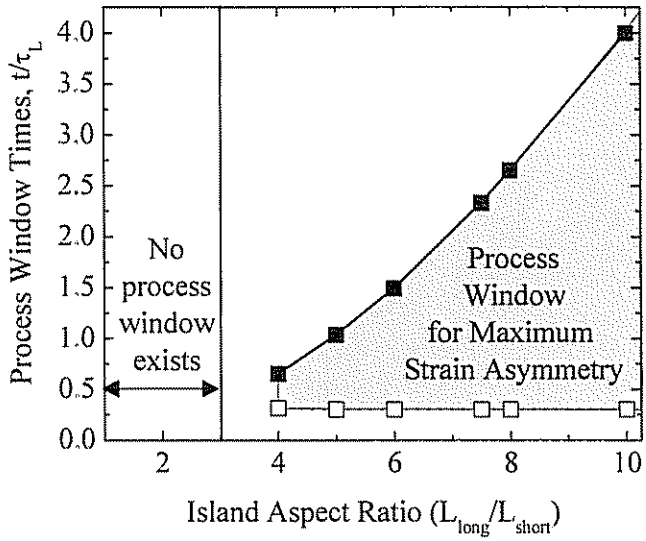


Figure 4.10: Graphical illustration of the process window for maximum asymmetry of strain (defined as $|(\varepsilon_{short} - \varepsilon_{long})/\varepsilon_0| > 90\%$ of maximum) in rectangular islands plotted as minimum and maximum normalized anneal times, t/τ_L, vs island aspect ratio. The data points are from Table 4.1. For islands with aspect ratios of three of less, the maximum strain asymmetry possible for a given structure cannot be obtained. When the aspect ratio is four or greater, the gray area indicates the process window for maximum strain asymmetry. As the island aspect ratio increases, the process window widens.

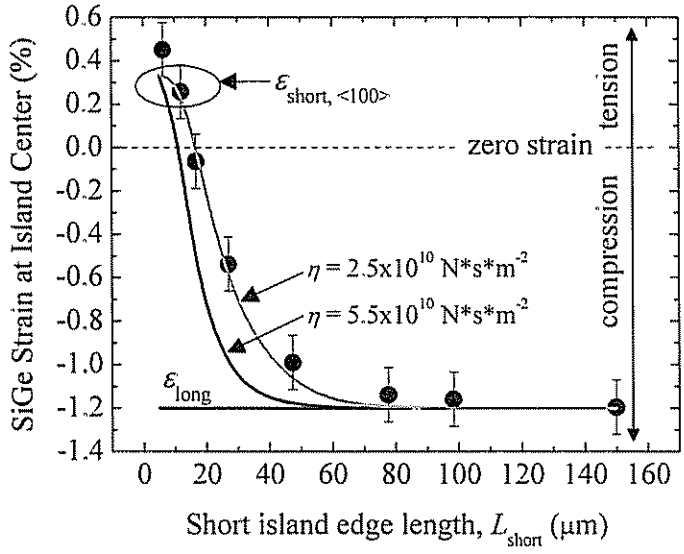


Figure 4.11: Comparison of Raman measurements and model predictions of SiGe strain at the island center of rectangles with various L_{short}, for a fixed L_{long} of 150 μm. Symbols indicate measured values of ε_{short} for rectangular islands aligned to <100> (the data is identical to Fig. 3.27 and the structure is shown in the Fig. 4.6 inset). The solid lines are predicted strains ε_{short} and ε_{long} for two different viscosities, η, as labeled.

4.6 Summary

This chapter has presented a 2-D model for the lateral expansion process, and used this model to predict the generation of biaxially-symmetric and asymmetric strain in square and rectangular islands, respectively, as experimentally observed and detailed in Ch. 3. The strain at the center of square islands decreases exponentially with time according to the lateral relaxation time constant, τ_L (Eqn. 3.9). The model and experimental results have been shown to agree well for both biaxial and asymmetric strain, once a correct value for BPSG viscosity has been measured. Finally, for the maximum strain asymmetry to be achieved, the rectangular island should have an aspect ratio (L_{long}/L_{short}) of at least four. A wide range of anneal times can be used to obtain this maximum strain asymmetry, according to the process window analysis. These models allow precise prediction and control of the strain generation process. In the next chapter, the tools of Chapters 3 and 4 will be adapted to obtain uniaxially-tensile strained silicon by relaxing bi-layers of silicon and SiGe.

Chapter 5

Generation of Uniaxial Strain in Silicon

As described in Ch. 2, strained silicon is of great technological interest to the integrated circuit community due to its ability to increase charge carrier mobility in MOSFETs. Biaxial tensile strain has been shown to exhibit significant electron mobility enhancement, and recently attention has shifted to uniaxial strain in order to similarly increase the hole mobility at high vertical electric fields.

The previous two chapters have described a wafer bonding and layer transfer technology for achieving biaxial and uniaxial stress in thin SiGe films. Numerical models of the lateral expansion process were used to determine process criteria for maximum uniaxial stress. In this chapter, this technology is modified by using a bi-layer of silicon and SiGe thin films with similar thickness instead of a single SiGe layer. When the bi-layer is annealed, the two films reach a stress balance in which the silicon layer is tensile strained. The film strain at stress balance, the minimum energy state, is predicted and compared to measured values. Both square and rectangular island geometries, which result in biaxial and uniaxial tensile strained silicon, respectively, are considered. The maximum uniaxial silicon strain observed is 1.0% tension along the <100> crystal direction.

5.1 Stress Balance of Si/SiGe bilayers

Previously, the relaxation of islands of a compressively strained SiGe film on BPSG has been discussed. As described in Chapter 3, the SiGe film was grown pseudomorphically on a silicon substrate and capped with a thin (1-2 nm) epitaxial silicon layer, then bonded and transferred by Smart-Cut^{TM} to a BPSG-coated wafer. The silicon cap layer was present in order to ensure a consistent bonding interface to the BPSG, but it was assumed to play no role in the SiGe relaxation process because it was so thin compared to the SiGe film. (Due to wafer cleaning before bonding, it is likely that

the silicon layer is even thinner than its epitaxially-specified thickness of 2 nm.) For the work in this chapter, the silicon layer is grown epitaxially, before the transfer process, to have a thickness on the order of that of the SiGe, so that the silicon strain can be readily controlled and measured. The silicon is initially unstrained and the SiGe is fully compressively strained (Fig. 5.1a). Upon annealing, the bi-layer structure will expand to reach a stress-balance state with the SiGe less compressively strained and the silicon layer in tension (Fig. 5.1.b). In this section, the stress-balance theory is detailed and compared to biaxially tensile strained-silicon results for square islands.

5.1.1 Introduction to Stress Balance

An unstrained silicon cap, of comparable thickness to the SiGe layer (*i.e.*, ten to thirty nanometers), is grown on top of the SiGe during initial epitaxy. The silicon and BPSG surfaces are then bonded and the SiGe/Si bilayer stack transferred to the BPSG handle wafer. After layer transfer the SiGe remains fully compressively strained, and the underlying silicon layer remains unstrained (see Fig. 5.1a cross-section). When annealed at high temperature, the BPSG softens and the SiGe expands to become less-compressively strained. As the SiGe layer relaxes it stretches the silicon layer to make it tensile, as shown in Fig. 5.1b. Cross-sections of the two samples used in this chapter are shown in Fig. 5.2.

The SiGe and silicon layers have a coherent interface and thus laterally expand together. The bi-layer structure acts like a perfect "virtual substrate" [155] and no misfit dislocations are required to generate the strain in the silicon layer. In Fig. 5.3, the strain in both layers is plotted versus position along a cross section of the short dimension of a rectangular island, showing that after a brief anneal the island layers maintain their initial strain at the center, while at the edges the layers are beginning to reach a state of force balance. The rectangular island has dimensions of 50 μm x 150 μm and the structure of Fig. 5.2a. (The SiGe-layer data were shown previously in Fig. 4.1 to demonstrate the lateral nature of the relaxation process.) Now comparing the strain of the two layers in Fig. 5.3, the coherence of the SiGe/Si film interface is demonstrated: at any given point along the cross-section, the change in film strain of the silicon layer (from its initial strain) is nearly identical to that of the SiGe layer.

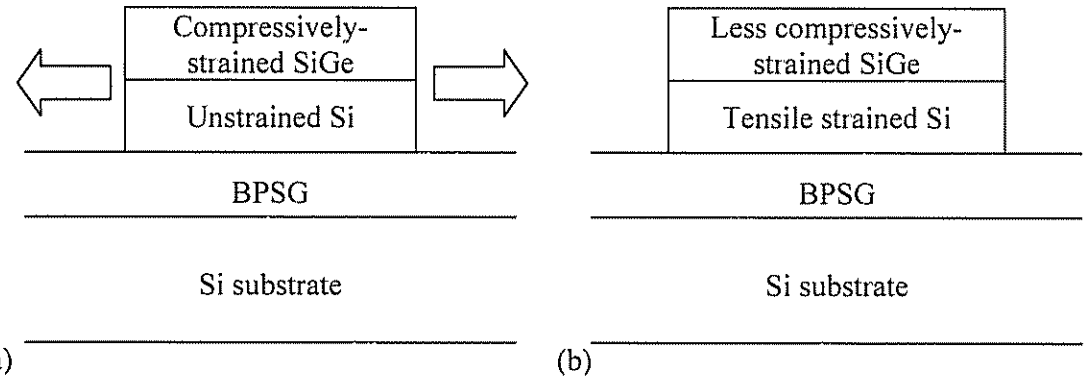


Figure 5.1: Cross-sections of a SiGe/Si bi-layer on BPSG (a) as bonded, before the relaxation anneal and (b) after annealing. Upon annealing, the BPSG flows and allows the two layers to expand, as shown by the arrows, to reach stress balance. The SiGe layer becomes less compressively strained, while the silicon becomes tensile. The lateral expansion process, shown by the arrows, is governed by the exponential time constant described by Eqn. 5.15 (after Eqn. 3.9), which is proportional to the square of the island dimension. Therefore this lateral expansion process will dominate for small square islands or the short dimension of narrow rectangles, as described in Ch. 3.

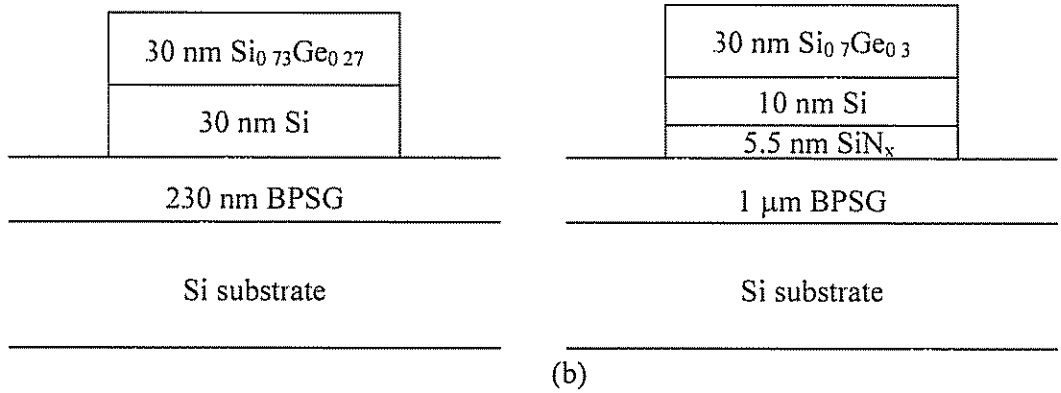


Figure 5.2: Cross-sectional schematics (not to scale) of the two SiGe/Si samples used in this chapter: (a) 30-nm $Si_{0.73}Ge_{0.27}$ on 30-nm Si (as measured by SIMS) on 230-nm BPSG and (b) 30-nm $Si_{0.7}Ge_{0.3}$ on 10-nm Si on 5.5-nm silicon nitride, on 1-μm BPSG.

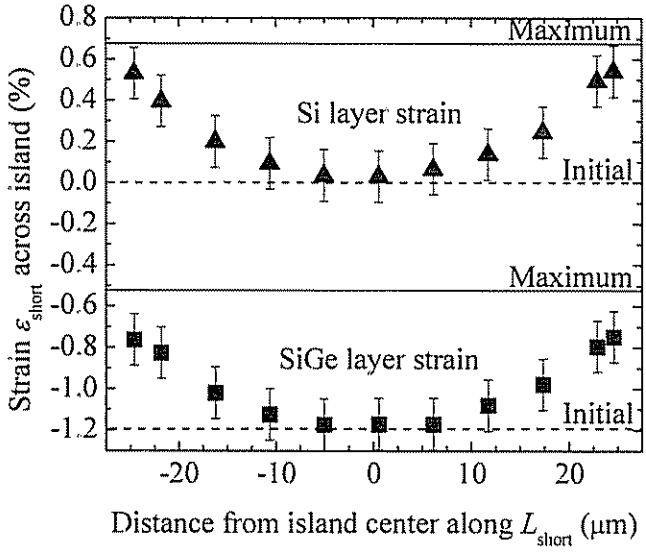


Figure 5.3: Strain in the short island direction, ε_{short}, across a 50-μm x 150-μm island aligned along <110> after a 15-min anneal at 750°C. The Fig. 5.2a shows the SiGe/Si bi-layer structure. The change in strain is nearly identical for the Si (triangles) and SiGe (squares) films, showing that the film interface is coherent and obeys Eqn. 5.11. The SiGe layer data were shown previously in Fig. 4.1 to illustrate the lateral relaxation process.

Upon a longer anneal, the two layers reach an equilibrium state of stress balance, which will be shown in the next section to occur when:

$$\sigma_{Si} h_{Si} + \sigma_{SiGe} h_{SiGe} = 0 \ , \tag{5.1}$$

where σ is the stress and h the thickness of each layer [148,155]. This equation assumes that the layers remain flat without curling. Note that for single layers, the equilibrium condition for square islands and the short dimension of rectangular islands was defined as the zero stress case, $\sigma = \varepsilon = 0$, whereas for a bi-layer the film stresses are non-zero and must be calculated from Eqn. 5.1. In both cases, the equilibrium state is simply the minimum energy state, at which there is no net force to drive further relaxation.

5.1.2 Derivation of the Stress Balance Equation

When an elastic thin film is subject to biaxial in-plane strain, the strain energy density (the energy per unit surface area) of the film, E, is given by [156,157]

$$E = \frac{1}{2} h \sum_{\alpha\beta} \sigma_{\alpha\beta} \varepsilon_{\alpha\beta} \tag{5.2}$$

where h is the film thickness, and $\sigma_{\alpha\beta}$ and $\varepsilon_{\alpha\beta}$ are the matrix elements of film stress and strain, respectively. For a (001) film with biaxial in-plane strain (σ_{zz}=0), by solving Hooke's law (see App. B) it is easily shown that Eqn. 5.2 reduces to

$$E = hB\varepsilon_{\text{biaxial}}^2 , \tag{5.3}$$

where $\varepsilon_{\text{biaxial}}$ is the film's biaxial strain, $B = c_{11} + c_{12} - 2c_{12}^2 / c_{11}$, and c_{11} and c_{12} are film elastic stiffness coefficients (see Table 3.1). Heteroepitaxially-generated biaxial film strain is defined (as in Eqn 2.28) as

$$\varepsilon \equiv \left(a_{\text{strained, in-plane}} - a_r \right) / a_r \ , \tag{5.4}$$

where a_r is the relaxed cubic lattice constant of the film.

For a bilayer of epitaxial SiGe and silicon, as in Refs. [107,155,158], the silicon and SiGe layers have a coherent interface between them. Fig. 5.4a depicts a SiGe/Si bi-layer as transferred; both the SiGe and silicon layers have lattice constants in the plane of the sample equal to $a_{r,Si}$. Thus the SiGe layer has an initial biaxial compressive strain of ε_o (for $Si_{0.7}Ge_{0.3}$, ε_o = -1.2%) and the silicon is unstrained (ε=0).

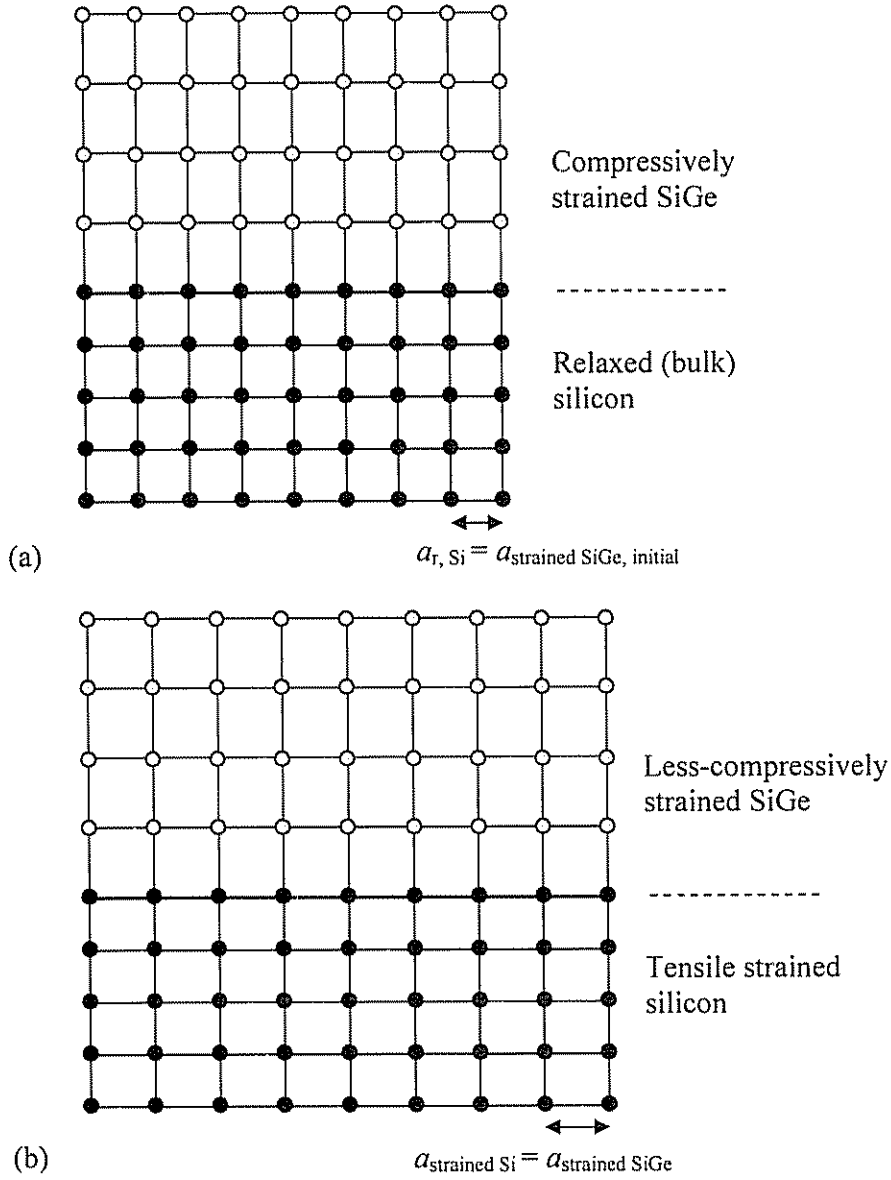


Figure 5.4: Schematic of a coherent bi-layer of silicon and SiGe (a) before and (b) after a high temperature anneal. Initially, as shown in (a), the silicon is unstrained and the SiGe pseudomorphically compressively strained. After annealing, the silicon is tensilely strained while the SiGe layer is less compressively strained than before, as shown in (b). The bulk (cubic) lattice constant, a_r, and the in-plane strained lattice constant, a_s, are indicated.

Upon high temperature annealing, the silicon/oxide interface becomes viscous, allowing the SiGe to partially relax and reduce its compressive strain, thereby stretching the underlying silicon so it becomes tensile. Fig. 5.4b depicts the bi-layer after it has been annealed. The in-plane lattice constant is still identical for both layers because they are coherently linked, $a_{\text{strained, in-plane, SiGe}} = a_{\text{strained, in-plane, Si}}$, and therefore

$$a_{\text{r, SiGe}} \cdot \Delta\varepsilon_{\text{SiGe}} = a_{\text{r, Si}} \cdot \Delta\varepsilon_{\text{Si}} . \tag{5.5}$$

During a lengthy anneal, the bi-layer can expand to reach a state of stress balance. Given the initial SiGe strain of ε_o and initially unstrained silicon, from Eqn. 5.5 the strains in the two coherent films (at any time) are related by

$$\varepsilon_{\text{SiGe}} = \varepsilon_{\text{o}} + \frac{a_{\text{r, Si}}}{a_{\text{r, SiGe}}}\varepsilon_{\text{Si}} . \tag{5.6}$$

Assuming that the bilayer films remain coherent and planar, Eqns. 5.3 and 5.6 can be combined to solve for the total energy of the strained bilayer:

$$E_{\text{TOTAL}} = \sum_{\textit{all films}} E_{\textit{film}} = h_{\text{Si}} B_{\text{Si}} \varepsilon_{\text{Si}}^2 + h_{\text{SiGe}} B_{\text{SiGe}} \left(\varepsilon_{\text{o}} + \frac{a_{\text{r, Si}}}{a_{\text{r, SiGe}}}\varepsilon_{\text{Si}} \right)^2 , \tag{5.7}$$

The equilibrium condition of the bilayer will be its minimum energy state, which can be determined by differentiating Eqn. 5.7 with respect to ε_{Si}:

$$\frac{dE_{\textit{TOTAL}}}{d\varepsilon} = 0 \tag{5.8}$$

(Since ε_{Si} and $\varepsilon_{\text{SiGe}}$ are linearly related via Eqn. 5.6, it does not matter which is the variable of differentiation.) What results is

$$\frac{h_{\text{Si}} B_{\text{Si}} \varepsilon_{\text{Si}}}{a_{\text{r, Si}}} + \frac{h_{\text{SiGe}} B_{\text{SiGe}} \varepsilon_{\text{SiGe}}}{a_{\text{r, SiGe}}} = 0 . \tag{5.9}$$

Since $a_{r,Si}/a_{r,SiGe} = 1 + \varepsilon_o$, to first order in ε one can drop the lattice constants in the denominator of Eqn. 5.9. Using the relation (Eqn. 3.14a) between stress and strain in biaxially strained films, $\sigma_{\text{biaxial}} = B\varepsilon_{\text{biaxial}}$, one arrives at the stress balance condition given in Eqn. 5.1 and repeated here:

$$\sigma_{\text{Si}} h_{\text{Si}} + \sigma_{\text{SiGe}} h_{\text{SiGe}} = 0 . \tag{5.10}$$

Simply put, Eqn. 5.10 states that a bi-layer reaches equilibrium when the total net force on the bi-layer in the plane is zero. A first-order strain approximation to Eqn. 5.5 states that the change in strain in the two layers must be identical,

$$\Delta\varepsilon_{SiGe} = \Delta\varepsilon_{Si}, \tag{5.11}$$

as observed in Fig. 5.3. Likewise, keeping only first order ε terms in Eqn. 5.6, the SiGe and silicon layer strains are related by

$$\varepsilon_{SiGe} = \varepsilon_o + \varepsilon_{Si}. \tag{5.12}$$

When Eqns. 5.10-5.12 are combined, the strain in the silicon film at stress balance can be expressed analytically as [159]

$$\varepsilon_{biaxial,Si} = -\frac{\varepsilon_O}{1+(h_{Si}/h_{SiGe})(B_{Si}/B_{SiGe})}. \tag{5.13}$$

The use of Eqns. 5.10-5.13, which include only the first-order strain terms, to solve for stress balance is justified because in all cases strain is approximately 1.0% (0.01) or less. Some authors [107,158] have further simplified Eqn. 5.13 by assuming B_{Si}=B_{SiGe}. This assumption introduces error of the order ~0.02% strain for the structures of Fig. 5.2. However, this error is much smaller than our Raman measurement error of 0.06% strain. For the remainder of this chapter the former approximation (but not the latter) will be utilized so that Eqns. 5.10-13 define stress balance.

Some authors [107,158] have quoted a bi-layer stress balance condition of

$$\varepsilon_{Si} = \varepsilon_o \frac{\left(h_{SiGe} - \sqrt{h_{Si}h_{SiGe}}\right)}{\left(h_{SiGe} - h_{Si}\right)} \tag{5.14}$$

and $\varepsilon_{SiGe} = \varepsilon_o - \varepsilon_{Si}$, based on $h_{Si}B\varepsilon_{Si}^2 = h_{SiGe}B\varepsilon_{SiGe}^2$. As shown above, this is incorrect, as we have recently pointed out [160].

The correct stress balance equations (Eqns. 5.10-5.13) state that the silicon strain always has the opposite sign to the SiGe layer strain. Moreover, the amount of silicon strain can be increased by either increasing the initial strain in the SiGe layer, ε_o, for instance by increasing its germanium content, or by decreasing the thickness of the silicon layer relative to the SiGe layer, *i.e.*, by decreasing the ratio h_{Si}/h_{SiGe}. Later in this chapter, the latter technique is used to obtain a maximum uniaxial silicon strain of 1.0% tension.

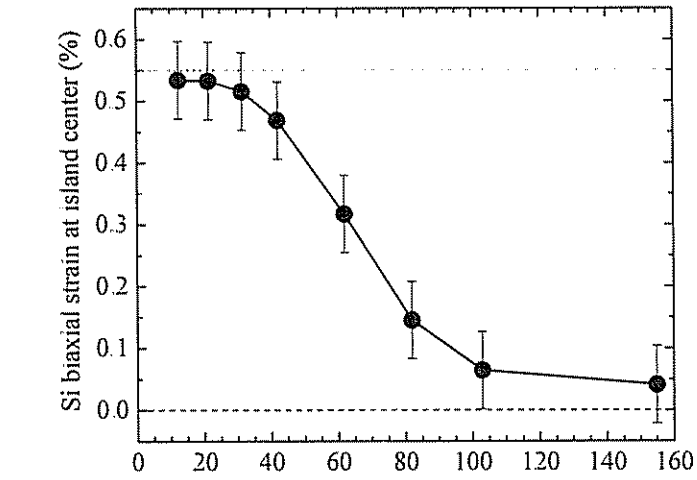
5.1.3 Observation of Biaxial Stress Balance in Square Islands

Square islands of a SiGe/Si bilayer, with the structure of Fig. 5.2a, were patterned with various island edge lengths. After annealing, the SiGe and silicon layer strains were measured by micro-Raman spectroscopy. The results are plotted in Fig. 5.5, where dashed lines indicate the initial film strain and dotted lines are the final film strains predicted by stress balance from Eqns. 5.12 and 5.13. Just as for the single SiGe layer islands in Chapter 3, the small SiGe/Si islands quickly expand to reach stress balance, while large islands maintain their initial strain. The changes in Si and SiGe strain from initial values are equal (within measurement error bars), as expected due to the coherency of the two films, in agreement with Eqn. 5.11.

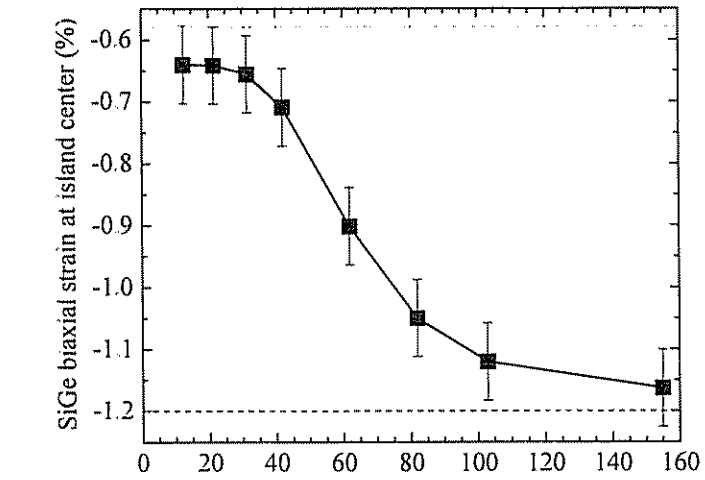
Compared to the single SiGe layer of Fig. 3.11, the bi-layer structure of Fig. 5.2a seems to require a longer and higher temperature anneal in order to laterally expand an identically sized island (compare 30 min at 800°C for Fig. 5.5 to 5 min at 750°C for Fig. 3.23). The lateral expansion time constant for a bi-layer can be expressed [155] as

$$\tau_L = \frac{\eta L^2}{h_g \sum_{films} \left(c_{11,film} h_{film} \right)} \tag{5.15}$$

It is clear that a thicker (bi-layer) stack should have a *smaller* value of τ_L (*i.e.*, *faster* expansion) than a thinner (single-layer) stack because a thicker structure results in a larger driving force for lateral expansion. However, the BPSG thickness also affects τ_L: the thinner the BPSG, the slower the expansion. For the samples used here, the large BPSG thickness difference (1 μm vs 230 nm) is dominant. For the bi-layer sample of Fig. 5.2a, $\tau_L \cdot L^{-2}$ at 750°C is calculated to be 24.2 sec·μm^{-2} compared to 11.1 sec·μm^{-2} for the single layer samples shown in Fig. 3.11. By increasing the anneal temperature to 800°C, $\tau_L \cdot L^{-2}$ for the bi-layer (Fig. 5.2a) is predicted to decrease to 5.3 sec·μm^{-2}. Thus the bi-layer samples on thin BPSG require a longer anneal and/or higher temperature to produce the same amount of lateral expansion as for a single SiGe layer on thick BPSG.



(a)



(b)

Figure 5.5: Biaxial strain in square islands of a SiGe/Si bilayer vs island edge length, L: (a) silicon layer strain and (b) SiGe layer strain. The islands, which have the structure of Fig. 5.2a, were annealed for 30 min at 800°C. Small islands relax to the calculated stress balance state (dotted lines from Eqn. 5.13) while large islands maintain their initial strain (dashed lines). The data are represented by symbols; the solid lines are solely a visual aid.

5.2 Uniaxially Strained Silicon

In Chapter 3, rectangular islands were used to create strain asymmetry in thin SiGe films, with tension in one direction and compression in the other in-plane direction. Now, using the same principle, rectangular islands of SiGe/Si bi-layers are used to generate uniaxially-strained silicon on insulator.

5.2.1 Stress Balance of Rectangular Islands

In Sec. 5.1 the stress balance of a biaxially-symmetric SiGe/Si bi-layer was predicted from thin film mechanics, and the measured results were shown to agree well with the theory. For a rectangular bi-layer island, the strain in the short direction, ε_{short}, has two contributions: (1) the stress balance of the bi-layer; and (2) the asymmetry of the rectangular island (the Poisson effect). To calculate the short-direction strain for bi-layers, Eqn. 3.10 ($\varepsilon_{short,\ single\ SiGe\ layer} = -\varepsilon_{long}\nu$), which is valid for single layers, is too simplistic. Instead, the stress balance model of Eqn. 5.10 is solved assuming that the long island directions maintain their initial strain. From App. B, for each layer the stress, σ', vs strain, ε', relationship in an arbitrary crystal direction is defined by

$$\begin{aligned}
\sigma'_{short} &= c'_{11}\varepsilon'_{short} + c'_{12}\varepsilon'_{long} + c'_{13}\varepsilon'_{zz} \\
\sigma'_{long} &= c'_{12}\varepsilon'_{short} + c'_{11}\varepsilon'_{long} + c'_{13}\varepsilon'_{zz} \\
\sigma'_{zz} &= c'_{13}\varepsilon'_{short} + c'_{13}\varepsilon'_{long} + c'_{33}\varepsilon'_{zz}
\end{aligned} \tag{5.16}$$

where c' are the crystal-direction dependent elastic stiffness coefficients (see App. B and Table 3.1). Eqn. 5.16 is written separately for the silicon and SiGe layers. The z-axis is normal to the film surface and unstrained, and thus $\sigma'_{zz,Si} = \sigma'_{zz,SiGe} = 0$. For squares, one assumes that $\varepsilon'_{long} = \varepsilon'_{short}$ (and therefore $\sigma'_{long} = \sigma'_{short}$) for each layer. For rectangles, one can assume that the island has a large aspect ratio and has been annealed within the maximum strain asymmetry process window so that in the long island dimension the initial strain is maintained: $\varepsilon'_{long,\ SiGe} = \varepsilon_o$ and $\varepsilon'_{long,\ Si} = 0$. Lastly, the Si/SiGe interface is assumed to be coherent as written in Eqn. 5.11, and the final state of the layers is

assumed to be determined by the force balance of Eqn. 5.10. Algebraically solving Eqns. 5.10, 5.12 and 5.16 under these conditions, the force balance state is determined to be:

$$\varepsilon'_{\text{short, Si}} = \frac{-\varepsilon_o}{A(\theta) + B(\theta) \cdot h_{\text{Si}} / h_{\text{SiGe}}}, \tag{5.17}$$

where A and B are given in Table 5.1, and are functions of the island geometry (square or rectangular), and the crystal direction alignment, θ, of the island (*e.g.*, θ=0° for <100> and θ=45° for <110>). From Table 5.1, it is clear that A and B for rectangular geometries are smaller, by factors of $(1+\nu)$, than A and B for square geometries. Physically, the silicon tension from the Poisson effect adds to the tension generated by stress balance, so the uniaxial silicon tensile strain for rectangular islands will always be greater than biaxial tensile strain generated in square islands. The crystal-direction dependence of Poisson's ratio (Eqn. 3.11 and Fig. 3.26) means that maximum uniaxial silicon tension occurs in the <100> direction:

$$\varepsilon_{\text{uniaxial, Si <100>}} > \varepsilon_{\text{uniaxial, Si <110>}} > \varepsilon_{\text{biaxial, Si}}. \tag{5.18}$$

Since the two layers are coherent, the SiGe strain is simply $\varepsilon_{\text{SiGe}} = \varepsilon_{\text{Si}} + \varepsilon_o$ as in Eqn. 5.12.

5.2.2 Experimental Measurements of Uniaxial Silicon Strain

The experiment described in Chapter 3 to obtain anisotropic strain in a single SiGe layer is repeated with a SiGe/Si bilayer to generate uniaxial silicon strain, after Ref. [148]. Rectangular bi-layer (Fig. 5.2a cross-section) islands with various L_{short} values (L_{long}=150 μm) are fabricated, and Si layer strain is measured by micro-Raman spectroscopy after a 30-min anneal at 800°C. The results are shown in Fig. 5.6. The silicon layer is uniaxially-strained in the surface plane: in the short direction there is a high level of tension (+0.6 to +0.8% strain, shown in Fig. 5.6), while in the long direction one can assume that the silicon remains unstrained. (The correctness of this assumption is verified in Sec. 5.3.) The narrowest islands show the strongest uniaxial strain while the center of the widest island (a 150-μm x 150-μm square) maintains its initial unstrained state. Clearly, the amount of strain asymmetry is dependent on rectangle aspect ratio as described in Chapter 4. As predicted from Eqns. 5.17 and 5.18, rectangular islands

Strain type	Condition on ε_{long}	A	B
Biaxially-symmetric	$\varepsilon_{long} = \varepsilon_{short}$	1	$\frac{s_{11,SiGe} + s_{12,SiGe}}{s_{11,Si} + s_{12,Si}}$
Asymmetric, edges aligned to θ	$\varepsilon_{long} = \varepsilon_{initial}$	$\frac{1}{1+\nu_{SiGe}(\theta)}$	$\left(\frac{s_{11,SiGe} + s_{12,SiGe}}{s_{11,Si} + s_{12,Si}}\right)\left(\frac{1}{1+\nu_{Si}(\theta)}\right)$

Table 5.1: Coefficients to calculate film strain in the short island direction from Eqn. 5.17. The values s_{11}, s_{12} and s_{44} refer to compliance coefficients (Table 3.1) and ν is Poisson's ratio (Eqns. 3.11 and 3.12). Theta, θ, is the angle the island edges make with the <100> direction in the (001) plane.

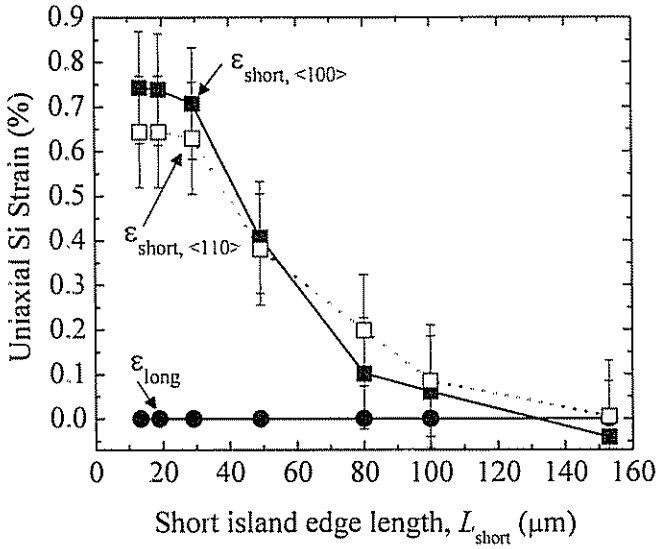


Figure 5.6: Measured uniaxial silicon strain in rectangular islands with L_{long} = 150 μm vs short island edge length after a 30-min anneal at 800 °C. The layer structure is shown in Fig. 5.2a. Symbols indicate ε_{short} for islands aligned along <100> (solid squares) and along <110> (open squares), with lines drawn from point to point. In both cases, ε_{long} (solid circles) is assumed fixed at zero by the large L_{long} that prevents relaxation.

aligned to <100> show the maximum amount of tension because for silicon the $\nu(0^o)$ for <100> island alignment of 0.279 is greater than the $\nu(45^o)$ for <110> alignment of 0.064. Likewise, for $Si_{0.7}Ge_{0.3}$, $\nu(0^o)$=0.276 and $\nu(45^o)$=0.052. Uniaxial strain in both <100> and <110> directions are greater than the measured maximum biaxial strain of +0.54%, measured in squares after the same anneal, because of the $(1+\nu)^{-1}$ factor in the *A* and *B* coefficients for rectangles in Table 5.1 and Eqn. 5.17.

In Fig. 5.7, the experimental data for several samples are compared to the stress balance model and excellent agreement is seen. Silicon and SiGe strain are plotted vs the ratio of silicon to SiGe layer thickness. The lines indicate the stress balance models of Eqn. 5.17 and Table 5.1, while points are measured data (see legend for details.) As the silicon to SiGe layer thickness ratio, h_{Si}/h_{SiGe}, decreases, the silicon strain increases. The left-most data points indicate the "single" SiGe layer data from Ch. 3. The right-most data points are from the bi-layer of Fig. 5.2a (data from the narrowest islands of Fig. 5.5 and 5.6). Using our strain generation process, the maximum uniaxial silicon tensile strain achieved to date is +1.0% in <100> crystal direction (circled data pts, in middle of Fig. 5.7). This strain is obtained on a structure (Fig. 5.2b) of 30-nm $Si_{0.7}Ge_{0.3}$ – 10-nm Si – 5.5-nm SiN_x – 1-μm BPSG, where the nitride layer is inserted to prevent outdiffusion [161] of boron and phosphorus from BPSG into the Si/SiGe (see discussion in Ch. 7). The presence of the nitride layer increases the effective silicon thickness and thus decreases the level of tensile silicon strain achieved by stress balance. For this structure, the effective silicon thickness has been set equal to the sum of the silicon and silicon nitride layer thicknesses, 15.5 nm, for a h_{Si}/h_{SiGe} ratio of 0.52. More sophisticated calculation methods are also available [8,161], which yield an effective silicon layer thickness of 20.8 nm. However the Young's modulus and deposited stress of the silicon nitride, which can vary widely, were not measured, and the Si and SiGe layer thicknesses have not been confirmed (*e.g.*, by SIMS) and thus both calculations are only estimates. The silicon and SiGe strains predicted for the h_{Si}/h_{SiGe} ratio of 0.52 used here show good agreement with the measured strains, as seen in Fig. 5.7.

After annealing a Si/SiGe bi-layer to generate silicon strain, the SiGe can be removed by selective etch to leave an ultra-thin (10-30 nm) uniaxially or biaxially-strained silicon-on-insulator structure, ideal for device fabrication [8,161].

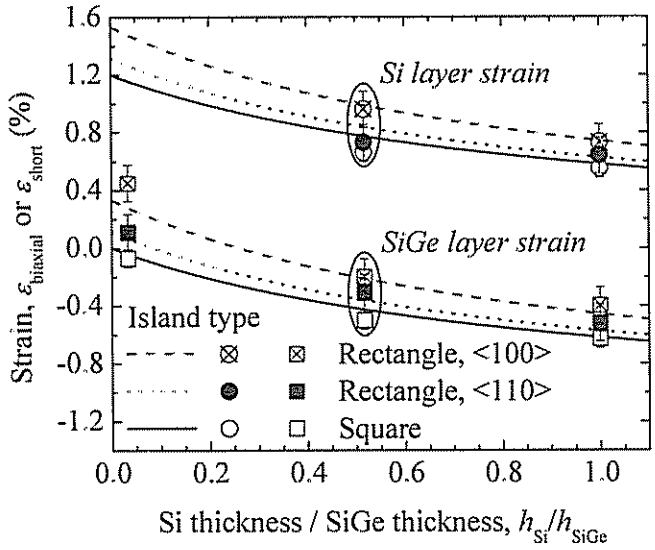


Figure 5.7: Silicon and SiGe strain vs film thickness ratio h_{Si}/h_{SiGe}. Biaxial strain is plotted for squares (open symbols and solid lines), and uniaxial strain in the short direction is plotted for rectangles (solid symbols and dotted lines for <110> alignment; crosshatched symbols and dashed lines for <100> alignment), after annealing to reach a state of stress balance in the squares and short rectangular dimensions. Lines are from the stress balance model of Eqn. 5.17 and Table 5.1; symbols are measured data. The left-most data points correspond to Fig. 3.11, the middle data to Fig. 5.2b and the right-most data to Fig. 5.2a.

5.3 Application of Lateral Expansion Model to Uniaxially-Strained Silicon

Finally, the numerical models described in Chapter 4 of strain evolution vs time can be used to predict process windows for uniaxially-strained silicon by using the known maximum strain asymmetry (Eqn. 5.17) and lateral expansion time constant (Eqn. 5.15) for the SiGe/Si bilayer to modify the normalized strain and time scales used in Chapter 4. The results are shown in Fig. 5.8. For islands with high aspect ratios, there exist processing windows for maximum uniaxial silicon strain. For a rectangle of dimensions 225 μm x 30 μm with the structure shown in the Fig. 5.2a inset, the predicted uniaxial silicon strain is at 90% or more of its maximum value of +0.81% for 800°C anneals from 31 min to greater than 110 min in length, as shown in Fig. 5.8. If the island has a small aspect ratio or is annealed beyond the uniaxial strain process window, ultimately both "long" and "short" strains would converge at the biaxial strain value determined by stress balance, indicated for a 30-μm x 30-μm square island in Fig. 5.8.

In Fig. 5.9 these numerical models are compared to the measured uniaxial silicon strain on the sample shown in Fig. 5.2a after a 30-min anneal at 800°C. A viscosity value of $\eta=1.2\text{x}10^{10}$ $\text{N}\cdot\text{s}\cdot\text{m}^{-2}$, obtained previously [8,111] by matching measured and model results for square islands of single SiGe layers on samples made using the same batch of BPSG, was used here. The model and measured data agree well, within the measurement error. As expected, the model predicts that for the measured island geometries, the silicon strain in the long direction always remains at zero. Thus, the lateral expansion model, which was initially developed to describe the relaxation of a single, compressively-strained (*e.g.*, SiGe) layer can easily be scaled to accurately predict the generation of uniaxial tensile strain in thin silicon layers.

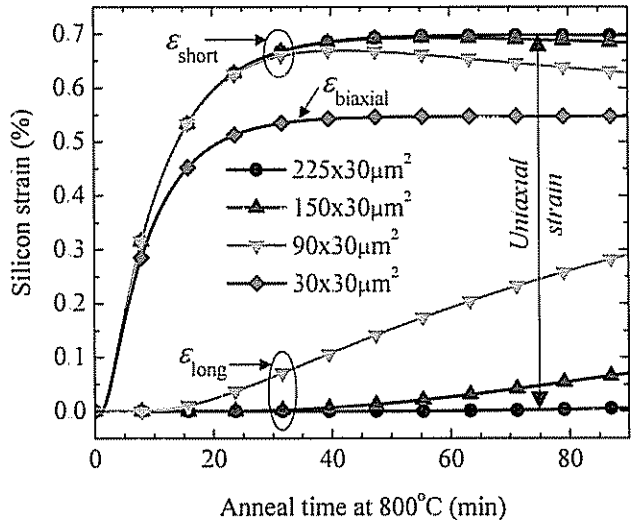


Figure 5.8: Model of uniaxial and biaxial silicon strain development as a function of anneal time at 800°C for rectangular islands with different aspect ratios, aligned to <100>, and for a square island. The island cross section is shown in Fig. 5.2a. Uniaxial in-plane silicon strain, for which ε_{short} is maximum while ε_{long} is close to zero, is indicated.

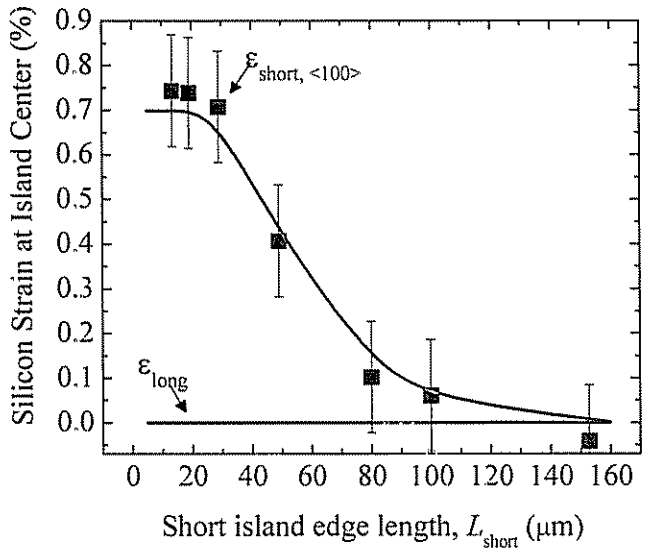


Figure 5.9: Comparison of lateral expansion model with $\eta=1.2\text{x}10^{10}$ N·s·m^{-2} (lines) and measured data (symbols, identical to Fig. 5.6) for uniaxially-strained silicon in SiGe/Si bi-layer islands aligned to the <100> crystal direction, after a 30-min anneal at 800°C. The SiGe/Si bi-layer has the structure shown in Fig. 5.2a.

5.4 Scalability of the Lateral Expansion Process to Smaller Islands

While the biaxial and uniaxial silicon strain generation process has been developed here for islands with large areas (~100-1000 μm^2), this process should be scalable for use in short-channel device technologies. There are two ways to scale the process for smaller islands: reduce the anneal temperature to increase viscosity, or reduce the BPSG thickness. Extrapolating from known viscosity values assuming exponential 1/T behavior (see Fig. 3.4), it is predicted that at 700°C, t/τ_L=0.6 (the earliest point at which biaxial and uniaxial strain are maximized) corresponds to 101 sec for a bilayer island of 30-nm $Si_{0.7}Ge_{0.3}$ on 25-nm silicon on 200-nm BPSG, with L_{square}=L_{short}=1 μm. Or, by keeping the anneal temperature at 750°C but reducing the BPSG thickness to 20 nm, for the same island the required anneal time is 189 sec. Such anneal times can be easily controlled using, for example, rapid thermal annealing. For very small islands (*i.e.*, L_{square}=L_{short}=100 nm), both methods can be used: for 10-nm BPSG a 130 sec anneal at 650°C corresponds to t/τ_L=0.6. Further experimental work is needed on small islands to verify the scalability of the uniaxial and biaxial strain process and models presented here.

5.5 Summary

In this chapter the work of Chapters 3 and 4 has been extended to generate uniaxial tensile strained silicon by lateral expansion of a SiGe/Si bilayer. Upon sufficient annealing, the bi-layer will reach a minimum energy state of stress balance where the SiGe has a reduced compressive strain and the silicon layer is in tension. Square islands result in biaxial silicon tension while rectangular islands generate uniaxial silicon strain. The Poisson effect increases the amount of silicon tension for rectangles compared to squares. By thinning the silicon layer, a maximum uniaxial tensile silicon strain of 1.0% was measured in the <100> direction. Analytical equations have been derived to accurately predict the stress balance end-point for uniaxial and biaxial strain, and the numerical models of Chapter 4 can readily be used to predict the dynamic process of uniaxial strain generation in silicon. This novel technique allows for the integration of

multiple types of silicon strain (biaxial, uniaxial, unstrained), with strain in various crystal directions, on the same sample.

Chapter 6

Studies of Buckling of Strained SiGe Films on BPSG

Compliant substrates are useful for manipulating the strain state of thin films. In Chapter 3 a process was described to bond a strained SiGe film to a compliant BPSG layer, and then relax SiGe islands through high temperature annealing. By varying the island geometry, SiGe films with biaxial stress, uniaxial stress and zero stress were obtained, in a process that does not require misfit dislocations. However the compliant BPSG layer may permit undesirable roughening (buckling) of the compressively strained SiGe film. Buckling, like the lateral expansion process described in Ch. 4, is driven by and relieves film stress. The two processes occur simultaneously, competing to determine the final strain and roughness states of the film. In order to achieve the lateral expansion described in Ch. 3-5, buckling must be minimized. This chapter will demonstrate two ways to minimize buckling.

The chapter begins with an initial introduction to the two-dimensional buckling of strained SiGe films. Then, two different methods to reduce the impact of buckling will be described. In the first method, the compliant BPSG layer is thinned, which helpfully slows the buckling process and reduces the buckling amplitude. In the second method, two-dimensional stress is reduced to one-dimensional stress. For the same strain level, films with one-dimensional stress and thus one-dimensional buckling exhibit slower buckling and lower final steady state buckling amplitude, which makes them technologically advantageous compared to biaxially-stressed films, which exhibit two-dimensional buckling. Furthermore, the crystalline orientation of the buckles is fully explained. Throughout, the experimental results will be explained through comparison with analytical models.

6.1 Two-Dimensional Buckling in Biaxially-Stressed Films

This section begins with a quantitative description of two-dimensional (2-D) buckling in biaxially-stressed SiGe films. Measurements of 2-D buckling are presented, followed by analytical models which explain the data.

6.1.1 Measurement of 2-D Buckling

In Chapter 3, a process was described to transfer a compressively strained SiGe film to a silicon wafer coated with borophosphorosilicate glass (BPSG), which functions as a compliant substrate. The SiGe layer is patterned into islands. When heated to about 750°C, the BPSG softens and allows the SiGe to laterally expand and relax. In addition to this desired lateral expansion mode there is an undesirable buckling mode [103,111,162,163] that competes with lateral expansion. Figure 6.1 shows a schematic representation of the lateral expansion (Fig. 6.1a) and buckling (Fig. 6.1b) processes.

Buckling is driven by stress; as a film buckles, it relieves its compressive stress through lengthening. From an elementary analysis of the lengthening of a line with fixed end points as it deforms from flat to sinusoidal, one can estimate the strain relieved by buckling (with no lateral expansion of the island) to be

$$\Delta\varepsilon = \left(\frac{\pi \cdot a}{\lambda}\right)^2, \tag{6.1}$$

where a is the buckling amplitude and λ the buckling wavelength, as shown in Fig. 6.2. In order to relieve the initial strain of a $Si_{0.7}Ge_{0.3}$ film, ε_o= –1.2%, with a buckling wavelength of λ = 1 μm the required buckling amplitude is a = 35 nm. While Eqn. 6.1 only provides a rough estimate (a more detailed theory will be developed in Sec. 6.1.3), it is nonetheless clear from this calculation that buckling is a non-trivial concern: here the buckling amplitude is greater than the typical SiGe film thickness of 30 nm.

If stress in the plane of the film is biaxially-symmetric (as at the center of large square islands), buckles can form in both in-plane dimensions before lateral relaxation occurs. A typical island, buckled after a 600-min anneal at 750°C, is shown in Fig. 6.3.

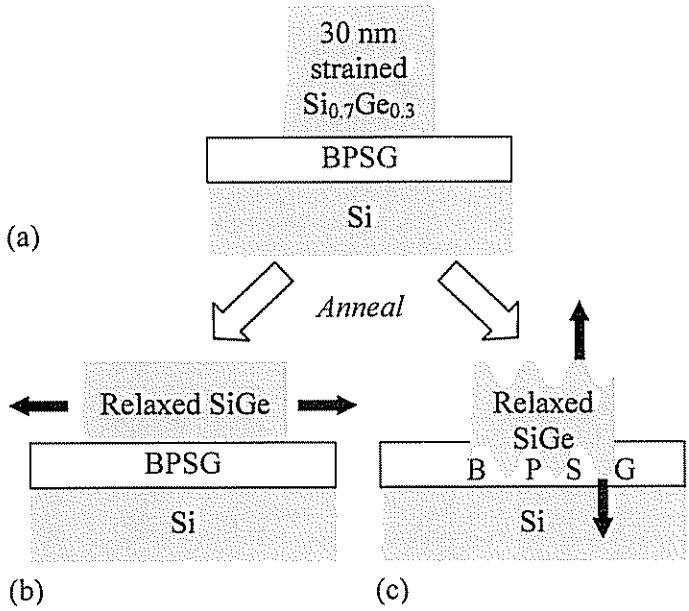


Figure 6.1: Schematic, after [8], of the two ways a compressively-strained SiGe film on a compliant BPSG layer can release its strain: (a) the strained film, as transferred and patterned; (b) lateral expansion generates a flat, relaxed film. The solid arrows show how the film expands to relieve stress; (c) buckling (vertical expansion) creates a rough surface. In practice, the buckling and lateral expansion modes occur simultaneously, in competition.

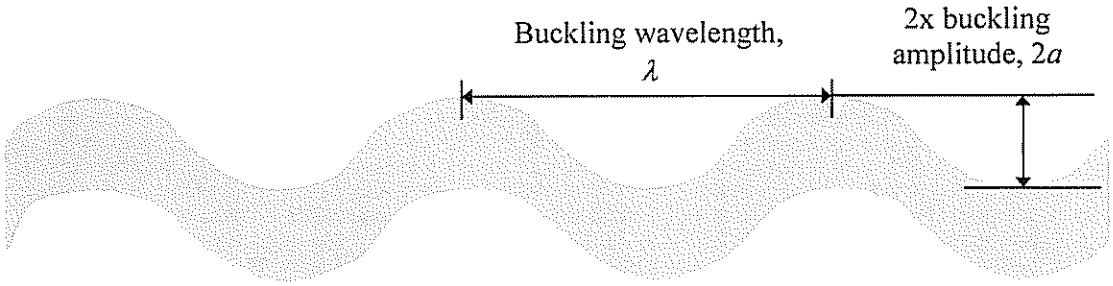


Figure 6.2: Schematic of a buckled film, characterized by its buckling amplitude, a, and buckling wavelength, λ. The amount of strain relieved by the lengthening of the line as it deforms from flat to sinusoidal is given as a function of a and λ in Eqn. 6.1.

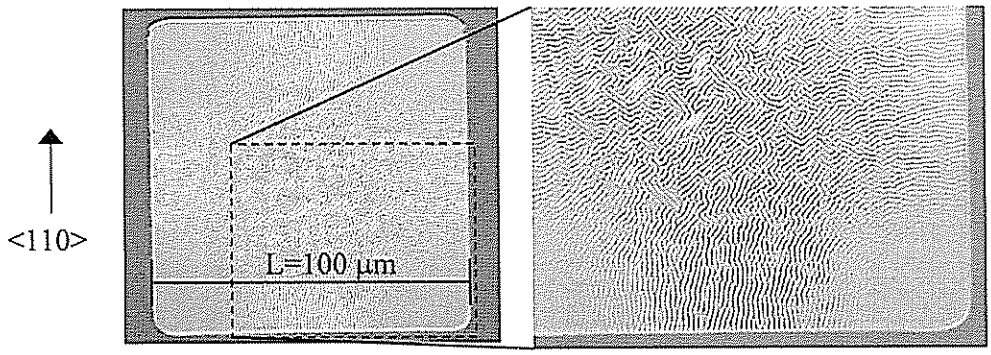


Figure 6.3: Optical micrograph of a 100-μm x 100-μm island of 30-nm 30% SiGe on 2-nm Si on 235-nm BPSG after a 600-min anneal at 750°C. On the left is shown the entire island; the expanded area shown at right is indicated by the dashed box. Note the different buckling morphologies in different regions (island center, corner and edge), caused by the simultaneously lateral expansion of the SiGe film. The buckling amplitude at center was measured by AFM to be 11 nm.

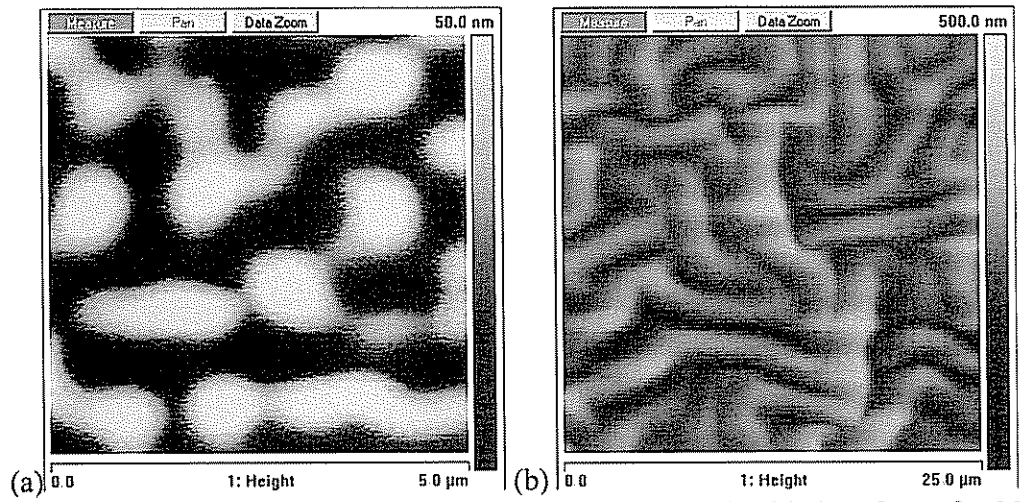


Figure 6.4: Atomic Force Microscopy (AFM) images of the buckled surface of a 30nm $Si_{0.7}Ge_{0.3}$ layer on 1-μm BPSG for (a) a 5-μm x 5-μm scan taken at the center of a 150-μm x 150-μm island after a 15-min anneal at 750°C, with RMS surface roughness of 15 nm; and (b) a 25-μm x 25-μm scan taken at the center of a 200-μm x 200-μm island after a 10-hour anneal at 750°C, with RMS surface roughness of 46 nm (note the different vertical scales).

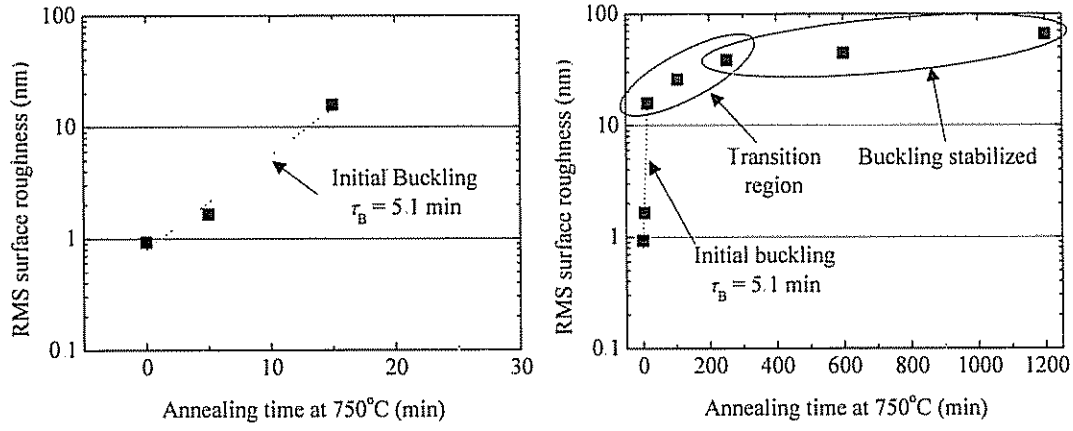
The 100-μm x 100-μm island consists of 30-nm 30% SiGe on 2-nm Si on 200-nm BPSG. At the center of the island, 2-D buckling occurs with buckles parallel to the <100> crystal directions in the (001) surface plane of the SiGe film. The crystal-direction-alignment of 2-D buckling will be explained in Sec. 6.1.2. The island corners, which can readily expand, are flat. Along the island edges, where the island can one-dimensionally expand, there are no buckle ridges parallel to the edge (*i.e.*, buckling occurs only in the direction of unrelieved stress). The different buckling morphologies in different regions of the islands clearly show that when lateral expansion is able relieve film strain, buckling does not occur. Clearly, the two processes are in competition.

Initially, when stress is about constant, the buckling amplitude, a, grows exponentially with time, t, according to

$$a(t) = a_0 \exp(t/\tau_B), \tag{6.2}$$

where τ_B is the buckling time constant [162]. Buckling is measured by Atomic Force Microscopy (AFM) as the RMS surface roughness of the film. For 2-D stress the roughness is measured at the center of large (>100-μm edge length) square islands. Typical AFM scans of buckling are shown in Fig. 6.4. For a 30-nm 30% SiGe layer on 1-μm BPSG, the initial exponential growth of buckling amplitude is seen in Fig. 6.5a. By fitting the experimental data, a buckling time constant of τ_B = 5.1 min is obtained. Upon further annealing, buckling effectively stabilizes, as shown in Fig. 6.5b, to a quasi-equilibrium state. The maximum buckling amplitude, a_{max}, observed after a 20-hour anneal at 750 °C is 66 nm. The buckling wavelength, λ, as observed visibly in Fig. 6.4b, is approximately 2.1 μm.

Buckling saturates because a majority of the initial film stress has been relieved by buckling, reducing the driving force for buckling. This explanation can be qualitatively justified: the amount of film strain relieved by buckling alone (assuming no lateral expansion) is calculated from Eqn. 6.2 for the observed buckling wavelength of Fig. 6.4b, and is plotted in Fig. 6.6. For the maximum measured buckling amplitude plotted in Fig. 6.5b, a_{max}=66 nm, approximately 90% of the film strain has been relieved. Thus, the buckled film can reach a stable state, with most of the film strain relieved, and further buckling proceeds slowly. A much more rigorous calculation of the saturated



(a) (b)

Figure 6.5: Buckling amplitude measured by AFM vs anneal time at 750°C for a 30nm $Si_{0.7}Ge_{0.3}$ layer on 1-μm BPSG for (a) short and (b) long anneal times. Initially in (a), the amplitude increases exponentially according to Eqn. 6.2. After a transition region, the buckling stabilizes as shown in (b). Experimental data (points) are shown along with an exponential fit line (dashed line), with the value of τ_B indicated. The initial buckling data and fit lines are identical in parts (a) and (b).

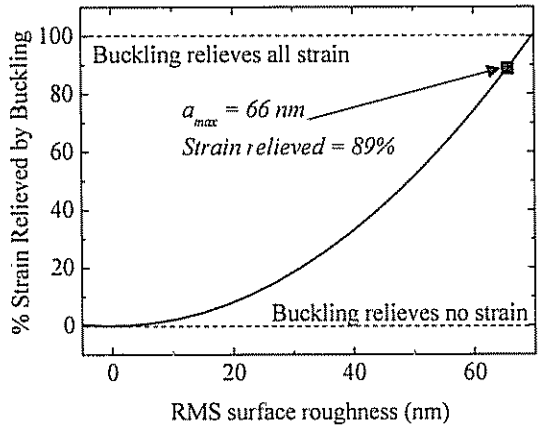


Figure 6.6: Percentage of initial SiGe strain, $\varepsilon_0 = -1.2\%$, relieved through buckling according to Eqn. 6.1 for $\lambda = 2.1\mu m$. The horizontal axis indicates surface roughness (*i.e.*, buckling amplitude), *a*. For the maximum measured roughness in Fig. 6.5b, $a_{max} = 66$ nm (indicated by the symbol), approximately 89% of the film strain has been relieved by buckling according to Eqn. 6.1.

buckling state will be developed in Sec. 6.1.3 based on energy minimization for a strained, buckled film.

In this section, two-dimensional buckling of biaxially-stressed SiGe thin films on BPSG has been experimentally measured. The buckling amplitude initially grows exponentially according to a buckling time constant, τ_B. Eventually, as the buckling amplitude gets large enough so that buckling relieves most of the initial film strain, the buckling amplitude saturates at a_{max}. The key parameters describing buckling are thus the initial τ_B, a_{max}, and the buckling wavelength, λ. In the following two sections, analytical models will be presented to calculate τ_B and λ from linear perturbation theory (Sec 6.1.2) and a_{max} from the minimum energy state of the buckled film (Sec 6.1.3), and the model predictions will be compared to measured data.

6.1.2 Modeling of 2-D Buckling: Exponential Growth Rate

In Ref. [162], Huang and Suo apply linear-perturbation analysis to model sinusoidal buckling of compressively-strained films on viscous substrates. The BPSG is modeled as an isotropic, incompressible viscous layer exhibiting "Stokes" or "creeping" flow, so that the layer is linearly viscous with zero flow velocity at bottom where the BPSG and substrate meet. Classical linear plate theory is used to model the elastic deformation of the SiGe film, and the tractions and displacements are assumed to be continuous across the BPSG/SiGe interface. Two-dimensional buckling is modeled in a cross-sectional slice of the SiGe/BPSG/Si substrate structure (Fig. 6.7), assuming that the SiGe film is infinite (no lateral relaxation), and the in-plane SiGe stress perpendicular to the slice (in the y-direction in Fig. 6.7) is equal to the initial film strain, ε_0. This model represents a refinement of earlier buckling theories [154,162,164-166], which are valid only under certain conditions. For example, the model of Ref. [164], is correct for very thick viscous layers, while Ref. [166] is correct for thin viscous layers. While a SiGe/BPSG structure is described here, the model results are entirely generic, and are valid for any elastic film on a viscous layer.

The model assumes that multiple buckling modes, characterized by different wavelengths, λ, grow simultaneously. The amplitude of each buckling mode grows (or decays) exponentially with time at its own rate, s_1. The fastest growing mode is assumed

to dominate buckling. Therefore the predicted buckling rate, τ_B^{-1} of Eqn. 6.2, is equal to the maximum value of s_1. The wavelength for this mode, λ_m, is the predicted buckling wavelength. The model thus calculates an exponential buckling growth rate, s_1, as a function of the buckling wavelength, λ:

$$s_1(\lambda)=\frac{1}{2}\left((\alpha-\beta)+\sqrt{(\alpha-\beta)^2+4\alpha\beta\left(1-\frac{\gamma_{12}^2}{\gamma_{11}\gamma_{22}}\right)}\right), \tag{6.3}$$

where α, β, γ_{11}, γ_{12} and γ_{22} are given by

$$\alpha(\lambda)=\frac{Ekh_{SiGe}}{24\eta(1-\nu^2)}\left[-12\varepsilon_o(1+\nu)-(kh_{SiGe})^2\right]\cdot\gamma_{11}, \tag{6.4}$$

$$\beta(\lambda)=\frac{Ekh_{SiGe}}{2\eta(1-\nu^2)}\cdot\gamma_{22}, \tag{6.5}$$

$$\gamma_{11}(\lambda)=\frac{1}{2}\cdot\frac{\sinh(2kh_{BPSG})-2kh_{BPSG}}{(kh_{BPSG})^2+\cosh^2(kh_{BPSG})}, \tag{6.6}$$

$$\gamma_{12}(\lambda)=\frac{(kh_{BPSG})^2}{(kh_{BPSG})^2+\cosh^2(kh_{BPSG})}, \text{ and} \tag{6.7}$$

$$\gamma_{22}(\lambda)=\frac{1}{2}\cdot\frac{\sinh(2kh_{BPSG})+2kh_{BPSG}}{(kh_{BPSG})^2+\cosh^2(kh_{BPSG})}. \tag{6.8}$$

The wavelength dependence comes through the buckling wavenumber, k, equal to $2\pi/\lambda$. The other variables include the SiGe film thickness, h_{SiGe}, and BPSG thickness, h_{BPSG}. The Young's modulus, E, and Poisson's ratio, ν, are functions of the material (SiGe) and crystal-direction; values and formulas have been given previously in Ch. 3 and App. B. The measurement of BPSG viscosity, η, was discussed in Ch. 3 and Ch. 4; values used here (calculated for room temperature despite experiments at 750-800°C; see discussion in Sec. 3.2.1) will be specified as needed.

The exponential growth rate for buckling, s_1, is calculated for a range of wavelengths. In Fig. 6.8, s_1 is plotted vs buckling wavenumber ($k=2\pi/\lambda$). When s_1 for a given wavelength is less than zero, the buckling component with that wavelength is predicted to exponentially decay. Positive values of s_1, conversely, indicate an expected exponential increase in buckling amplitude. For a given SiGe/BPSG structure and anneal temperature, the maximum value of s_1, denoted $s_{1,\,max}$, is determined numerically. The

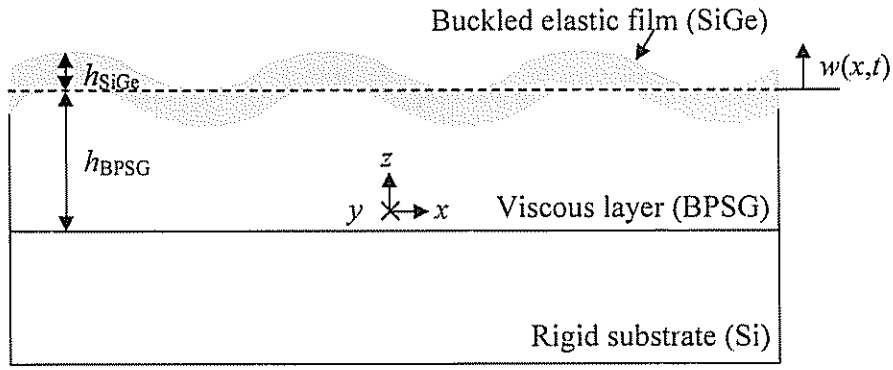


Figure 6.7: Schematic cross-section of a buckled elastic film on a viscous layer, with the *x, y, z* co-ordinates specified. Also shown are the viscous layer thickness, h_{BPSG}, the elastic film thickness, h_{SiGe}, and the *z*-direction elastic film displacement, $w(x,t)$.

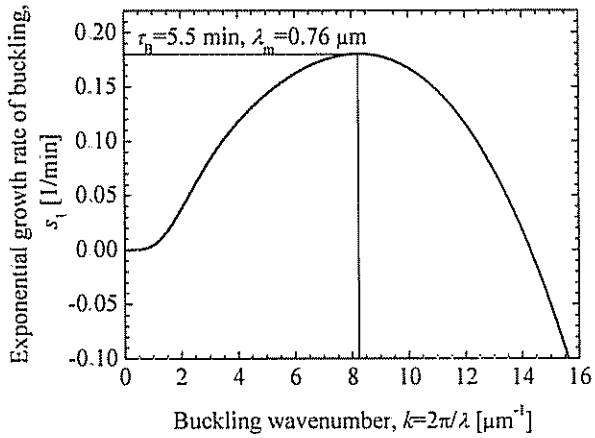


Figure 6.8: The exponential growth rate of buckling, s_1, vs the buckling wavenumber, k, plotted for a 30-nm $Si_{0.7}Ge_{0.3}$ layer on 1-μm BPSG, with viscosity of 5.5×10^{10} N·s·m^{-2} (as characterized previously [8,111] at 750 °C). The maximum growth rate is assumed to dominate buckling, and corresponds to the predicted τ_B and λ_m values of 5.5 min and 0.76 μm, respectively, as indicated.

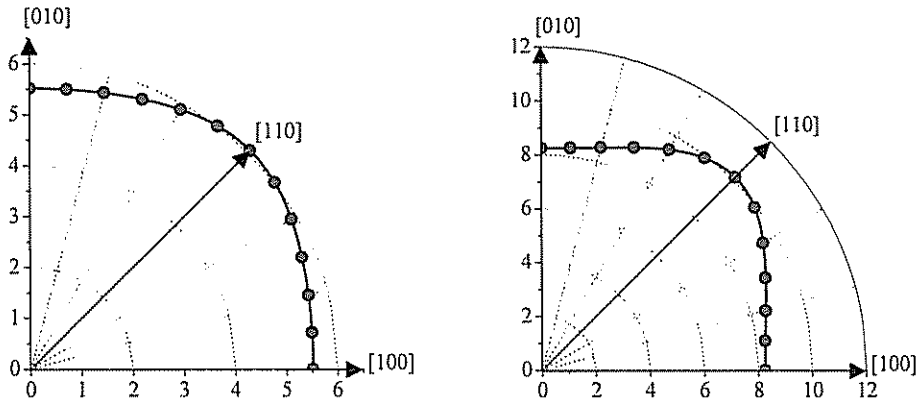
value of $s_{1,\,max}$ corresponds to the fastest possible buckling rate, which is assumed to dominate buckling. The predicted exponential buckling time constant of Eqn. 6.2, τ_B, is equal to $(s_{1,\,max})^{-1}$. Note from Eqn. 6.3-6.5 that s_1^{-1} and therefore τ_B are proportional to the BPSG viscosity, η. We will return to this point later in the chapter. The wavenumber, k_m, at which this maximum occurs, corresponds to the expected buckling wavelength, λ_m.

In Sec. 6.1.1, buckling on a 30-nm $Si_{0.7}Ge_{0.3}$ layer on 1-μm BPSG annealed at 750°C was measured. Fig. 6.8 shows the calculated s_1 vs k curve for this structure from Eqns. 6.3-6.8 with η=5.5x10^{10} N·s·m^{-2}. The predicted value of τ_B = 5.5 min indicated on the plot agrees well with the measured value of 5.1 min. However, the predicted wavelength of 0.76 μm is much shorter than the measured value of 2.1 μm. The predicted buckling time constant for a wavelength of 2.1 μm is τ_B = 12.1 min, much longer than the measured value of 5.1 min. The reason for this discrepancy is not known, but may be due to an effective thickness of the BPSG layer that is thinner than the deposited thickness of 1 μm, since the $k \cdot h_{BPSG}$ product is used in Eqns. 6.6-6.8.

As observed previously [163] and in Fig. 6.3, 2-D buckles at the center of large islands align to the <100> crystal directions. This alignment occurs because the buckling rate ($1/\tau_B$) is fastest in this direction. The buckling time constant, τ_B, varies with crystal direction through the Young's modulus, E, and Poisson's ratio, ν, as described in Ch. 3 and plotted in Figs. 3.29 and 3.26. Using Eqns. 6.3-6.8, one can calculate the dependence of τ_B on crystal direction in the (001) plane. The results are plotted in Fig. 6.9. For 1-μm BPSG, τ_B has a minimum value of 5.5 min in the <100> directions, and a maximum value of 6.1 min in the <110> directions. Thus, the film buckles most quickly in the <100> directions [167].

6.1.3 Modeling of 2-D Buckling: Saturated Buckling Amplitude

In the previous section, linear perturbation theory has been used to quantitatively explain the initial exponential increase in buckling amplitude and the crystal-direction dependence of 2-D buckling. In this section, the minimum energy state of a buckled, strained film is calculated to explain and quantitatively predict the saturated buckling amplitude. In Ref. [166], Huang and Suo, calculate the energy under certain conditions,



(a) (b)

Figure 6.9: Model of the 2-D buckling time constant, τ_B, vs crystal direction in the (001) surface plane, for 30-nm $Si_{0.7}Ge_{0.3}$ on (a) 1-μm BPSG and (b) 235-nm BPSG annealed at 750°C. The buckling time constants exhibit minima in the <100> directions of (a) 5.5 min and (b) 8.3 min, as calculated according to Eqns. 6.3-6.8, using the crystal-direction dependent values of E and ν as described in Ch. 3. Symbols are used every 50 pts in order to highlight the lines.

using the non-linear Von Karman plate theory. The non-linear plate theory is appropriate when the buckling amplitude is comparable to the film thickness, as is true for the highly buckled films measured in Sec. 6.1.1. Here, the film energy is calculated for arbitrary strain and buckling states. For a given buckling wavelength, λ, the minimum energy state corresponds to a unique (saturated) buckling amplitude, a_{max}.

The energy density (energy per unit surface area) of a strained and buckled film has two components: Φ_1, from film bending, and Φ_2, from in-plane deformation of the film, given by [156,166,168]

$$\Phi_1 = \frac{D}{2}\left[\left(\frac{\partial^2 w}{\partial x^2}+\frac{\partial^2 w}{\partial y^2}\right)^2 - 2(1-\nu)\cdot\left(\frac{\partial^2 w}{\partial x^2}\cdot\frac{\partial^2 w}{\partial y^2}-\left(\frac{\partial^2 w}{\partial x \partial y}\right)^2\right)\right] \tag{6.9}$$

$$\Phi_2 = \frac{1}{2}\sum_{\alpha=x,y}\sum_{\beta=x,y} N_{\alpha\beta}\varepsilon_{\alpha\beta}\,, \tag{6.10}$$

where w is the sinusoidal displacement of the elastic film in the z-direction with amplitude a, $w(x) = a\sin(kx)$, as indicated in Fig. 6.7, and D is the flexural rigidity of the elastic film:

$$D = \frac{Eh_{SiGe}^3}{12(1-\nu^2)}. \tag{6.11}$$

$\varepsilon_{\alpha\beta}$ is the component film strain, given by:

$$\varepsilon_{\alpha\beta} = \varepsilon_o\delta_{\alpha\beta} + \frac{1}{2}\left(\frac{\partial u_\alpha}{\partial\beta}+\frac{\partial u_\beta}{\partial\alpha}\right)+\frac{1}{2}\frac{\partial w}{\partial\alpha}\frac{\partial w}{\partial\beta}, \tag{6.12}$$

where the final term includes the non-linear plate theory. The displacements at the interface of the viscous and elastic layers in the x and y directions are u_x and u_y, and N is the membrane force in the film:

$$N_{\alpha\beta} = Eh_{SiGe}\left[\frac{1}{1+\nu}\varepsilon_{\alpha\beta}+\frac{\nu}{1-\nu^2}\delta_{\alpha\beta}\sum_{\gamma=x,y}\varepsilon_{\gamma\gamma}\right] \tag{6.13}$$

To simplify the analytical solution, it is assumed that buckling and relaxation only occur in the x-z plane and that the displacements in the z- and x- directions are sinusoidal with amplitudes of a and b:

$$w(x) = a\sin(kx)\,, \tag{6.14}$$

$$u_x(x) = b\cos(kx)\,, \tag{6.15}$$

$$u_y = 0 \tag{6.16}$$

Therefore from Eqns. 6.12 and 6.14-6.16, the strain in the y-direction remains constant at the initial strain value, $\varepsilon_{yy}=\varepsilon_o$ and $\varepsilon_{xy}=\varepsilon_{yx}=0$.

To solve for the total energy density of a buckled, strained film, the integral of Φ_1 and Φ_2 is taken over one wavelength:

$$\Phi_{total} = \frac{1}{\lambda}\int_0^{\lambda=2\pi/k}(\Phi_1 + \Phi_2)dx. \tag{6.17}$$

Using Eqns. 6.9-6.16 to solve Eqn. 6.17, the following result is obtained:

$$\Phi_{total} = \sigma_o h_{SiGe}\varepsilon_o + \frac{E}{(1-\nu^2)}\frac{h_{SiGe}^{\ 3}}{48}a^2k^4 + \frac{E}{(1-\nu^2)}\frac{3h_{SiGe}}{64}a^4k^4 + \frac{h_{SiGe}}{4}\sigma_o a^2k^2 + \frac{E}{(1-\nu^2)}\frac{h_{SiGe}}{4}b^2k^2 \tag{6.18}$$

where the first term is the equilibrium strain energy, equal to the value of Φ_2 when no buckling is present. The second term is from film-bending (Φ_1), and the remaining terms are the Φ_2 strain energy (from film stretching and compressing) for a buckled layer. The relationship between biaxial stress and strain from Eqn. 3.14a is:

$$\sigma_o = \frac{E\varepsilon_o}{1-\nu} \tag{6.19}$$

The total strain energy density and its components, Φ_1 and Φ_2, for a 30-nm $Si_{0.7}Ge_{0.3}$ layer with λ=2.1 μm (as measured in Sec. 6.1.1) is calculated assuming b=0, and is plotted in Fig. 6.10 vs buckling amplitude, a. For such a long wavelength, the bending energy is relatively small compared to the in-plane deformation energy, which dominates the total energy.

For a given buckling wavelength, λ, there exists a buckling amplitude, a_{max}, for which the system is in a minimum energy state. The predicted buckling amplitude at the minimum total energy, a_{max}, is 66 nm, which agrees exactly with the measured RMS surface roughness after a 20-hr anneal at 750°C (Fig. 6.5b). An analytical expression for a_{max} can be calculated from Eqn. 6.18 assuming b=0 (*i.e.*, once stabilized in a minimum energy state, there are no x- or y-direction displacements of the film):

$$a_{max} = \sqrt{-\frac{2}{9}\left[h_{SiGe}^{\ 2} + 3\sigma_o\left(\frac{1-\nu^2}{E}\right)\left(\frac{\lambda}{\pi}\right)^2\right]} \tag{6.20}$$

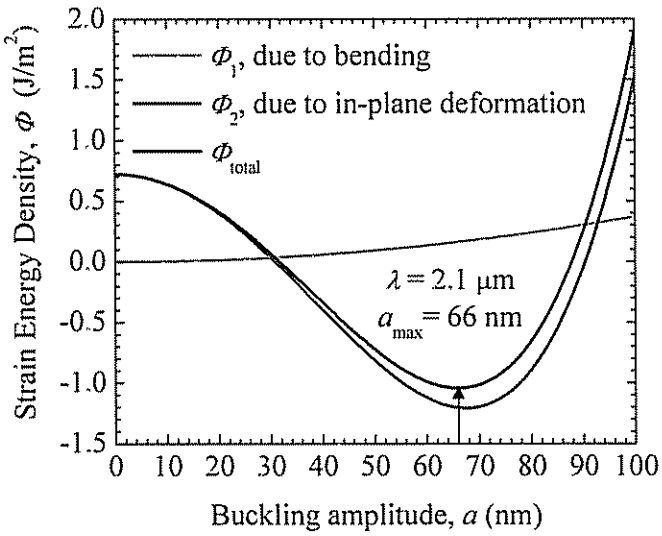


Figure 6.10: Energy density for a buckled, strained film of 30-nm $Si_{0.7}Ge_{0.3}$ as calculated from Eqn. 6.18 with b=0.

Buckling parameter	*2D*	*1D*	*Ratio 1D/2D*
Time constant, τ_B	5.1 min (5.5 min)	7.9 min (9.0 min)	1.55 (1.64)
Wavelength, λ	2.1 μm (0.76 μm)	2.2 μm (0.90 μm)	1.05 (1.18)
Amplitude, a_{max}	66 nm (66 nm)	43 nm (59 nm)	0.65 (0.89)

Table 6.1: Summary of measured and modeled buckling parameters for 30-nm $Si_{0.7}Ge_{0.3}$ on 1-μm BPSG annealed at 750°C. The model is calculated using BPSG viscosity $\eta = 5.5 \times 10^{10}$ Pa. Values predicted by modeling are in parentheses.

Note that the total strain energy density, Φ_{total}, given in Eqn. 6.18, and the buckling amplitude at minimum energy, a_{max}, given in Eqn. 6.20, are dependent solely on the elastic film characteristics (its Young's modulus, Poisson's ratio, thickness, and biaxial stress or strain) and on the buckling and stretching sinusoidal amplitudes, a and b, and the buckling wavelength, λ (via the wavenumber, k). The BPSG characteristics (*e.g.*, viscosity and thickness) thus only indirectly affect the energy density and a_{max} via their influence on λ, as will be explored in the next section.

Recall that earlier (Eqn. 6.1) a simple 1-D model of film elongation by buckling was used to calculate the amount of strain relieved by buckling. When the amount of strain relieved is equal to the initial strain, $\Delta\varepsilon=\varepsilon_o$, the buckling amplitude should be equal to a_{max}. Using Eqns. 6.1 and 3.14a, the 1-D model predicts that

$$a_{max} = \sqrt{-\sigma_o\left(\frac{1-\nu}{E}\right)\left(\frac{\lambda}{\pi}\right)^2}\ . \tag{6.21}$$

For the 30-nm $Si_{0.7}Ge_{0.3}$ layer with λ=2.1 μm described previously, Eqn. 6.21 predicts a value of a_{max} of 73 nm, which is about 10% greater than the measured value of 66 nm. The 2-D model of Eqn. 6.20 correctly includes the energy it takes to bend the film (Φ_l), while the 1-D model (Eqn. 6.21) only considers the film strain energy from local stretching and compression caused by buckling. Clearly the 2-D model is more complete, and gives a slightly better match to the measured data.

In this section, the 2-D buckling of biaxially stressed SiGe films on BPSG has been measured and explained through modeling. The buckling amplitude initially grows exponentially with a time constant, τ_B and buckling wavelength, λ. The values of τ_B and λ can be predicted by linear perturbation theory [162]; the results are compared to measured data in the second column of Table 6.1; the τ_B values agree particularly well. The previously observed [103,163] but poorly explained <100> crystal-alignment of 2-D buckling in films with (001) surface planes is explained here by calculating the predicted dependence of τ_B on crystal-direction. Buckling occurs most quickly along <100> directions, and thus this alignment will dominate buckled films. As buckling grows and relieves a significant portion of the film strain, the buckling amplitude saturates at a_{max}. To model buckling saturation, the total energy density of a strained, buckled film was

calculated. For a given buckling wavelength, the predicted buckling amplitude at minimum energy was shown to correspond to a_{max}, the measured saturated buckling amplitude. In the next section, these two models will be used to justify a new method to reduce buckling by thinning the compliant BPSG layer.

6.2 Compliant Layer Thinning to Reduce Buckling

As shown in the previous section, compressively strained films on viscous substrates, like SiGe on BPSG, can buckle when the viscous layer flows. The buckling occurs to release the compressive SiGe stress. In order to exploit the lateral relaxation techniques developed in Ch. 3-5 to engineer uniaxial and biaxial strain in thin silicon films, it is critical that the buckling of Si/SiGe thin films be well-controlled and minimized. In this section, a new technique for reducing buckling by thinning the viscous (BPSG) layer is demonstrated.

6.2.1 Benefits of Thin BPSG: Model Predictions

The sample described in Sec. 6.1, with a BPSG thickness of 1 μm, exhibited very large buckling amplitudes: the maximum measured buckling amplitude of 66 nm is more than twice the 30-nm SiGe film thickness. Clearly, the film is highly deformed from its initial uniform flat plane. In severe cases, the film can crack, as shown in the micrographs of Fig. 6.11a. For the same islands, the AFM-measured surface roughness data and predicted strain at island center (from the lateral expansion theory of Ch. 4) are plotted vs island size in Fig. 6.11b. Note that the lateral expansion theory ignores the strain relaxed due to buckling. For islands with edge lengths less than 60 μm, the islands relax to zero strain and remain smooth, with low surface roughness. Larger islands buckle and crack before lateral expansion can be completed. The buckles run along the <100> crystal directions, perpendicular to the island edges in the case, as described in Sec. 6.1.2. The cracks in the SiGe film occur along the <110> crystal directions, due to the low shear modulus in this direction. (For the same reason, (001) silicon cleaves along <110> directions.) When a crack occurs, the crack relieves the film strain and the neighboring

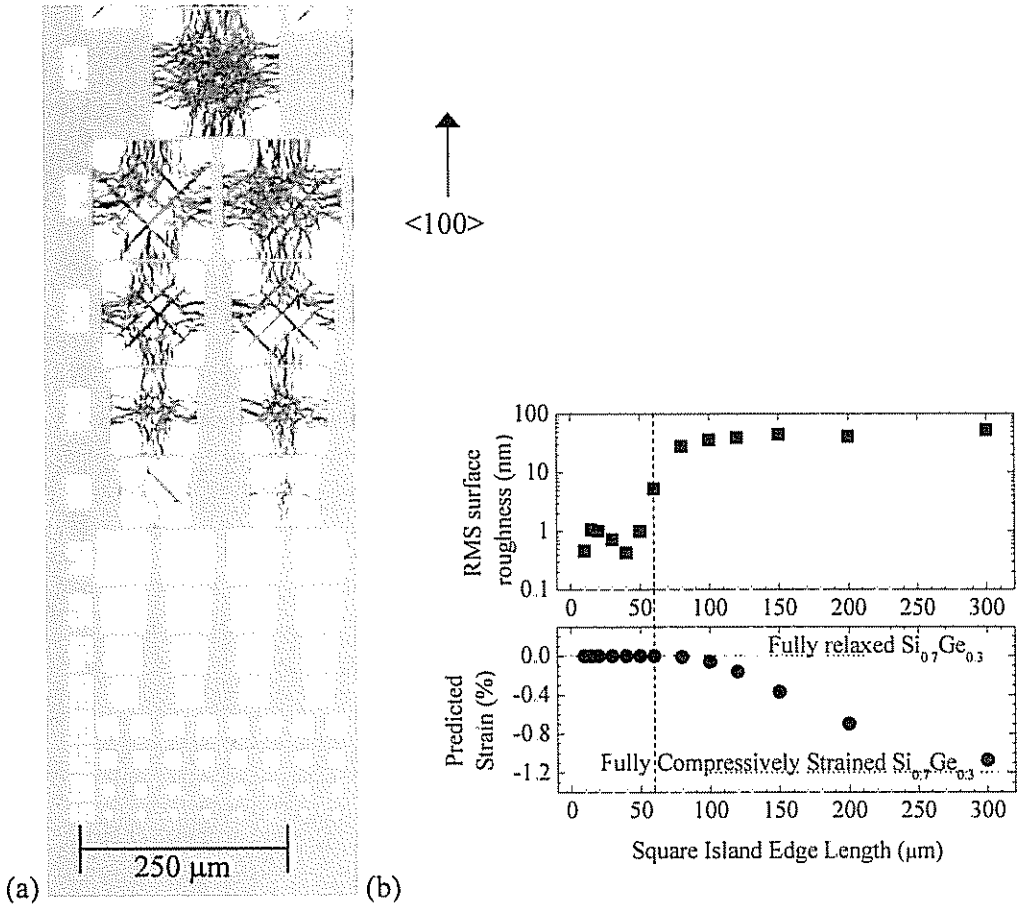


Figure 6.11: (a) Optical micrograph of buckled and cracked islands of 30-nm $Si_{0.7}Ge_{0.3}$ on 1-μm BPSG annealed for 10 hrs at 750°C. The island edge lengths in microns are given on the far left of the image. Small islands have relaxed by lateral expansion and remain smooth while large islands exhibit buckles and cracks. The buckles are the fine features running perpendicular to the island edges, along <100> crystal directions as described in Sec. 6.1.2. The cracks are the large features running diagonally across the islands, along the <110> crystal directions. (b) Measured RMS surface roughness and predicted strain (for the lateral expansion theory of Ch. 4) vs island edge length, for the islands pictured in (a).

area is relatively smooth and flat. (See, for instance, the 120-μm x 120-μm island on the right-hand side of Fig. 6.11a.) Clearly the buckling and cracking phenomena need to be avoided in order to obtain large, flat islands of strain-controlled films.

One way to reduce buckling is to thin the viscous BPSG layer. As the BPSG thickness is reduced it becomes more difficult to displace the BPSG and form buckles, and thus buckling slows and is characterized by smaller amplitudes *and* by shorter buckling wavelengths. Qualitatively, one expects that as the BPSG layer is thinned the buckling time constant, τ_B, will increase, while the buckling wavelength, λ, and buckling amplitude, a_{max}, will both decrease. As the BPSG becomes very thin (*i.e.*, of the order of the SiGe film thickness), τ_B, λ, and a_{max} should vary rapidly with small changes in h_{BPSG}. Conversely, if the BPSG thickness is much greater than the buckling wavelength, the buckling parameters will stabilize since the BPSG can be easily displaced. Thus, for BPSG layers thicker than the buckling wavelength, the buckling parameters are expected to be very weakly dependent on the BPSG thickness. Using the linear perturbation model of Sec. 6.1.2, these trends can be quantitatively examined.

In Fig. 6.12 the buckling parameters τ_B, λ, and a_{max} calculated from Eqns. 6.3-6.8 and 6.20 are plotted vs BPSG thickness, h_{BPSG}. Here, a_{max} is calculated from Eqn. 6.20 using the predicted buckling wavelength. All three expected trends are observed as the BPSG thins: the buckling time constant increases, and the wavelength and amplitude of buckling decrease. Note that τ_B is plotted on a semi-log plot and therefore the increase in τ_B is quite dramatic for small h_{BPSG}. If the BPSG thickness is reduced from 1 μm to 235 nm (the two points indicated by dotted lines on Fig. 6.12), the buckling time constant increases by about 60%, from 5.5 min to 8.3 min. At the same time, the predicted buckling wavelength decreases slightly from 0.76 μm to 0.62 μm. Note that the final buckling amplitude only changes due to the buckling wavelength according to Eqn. 6.20, since the SiGe film energy for a given λ and a does not depend on BPSG thickness. For the predicted wavelength change, the buckling amplitude is expected to decrease from 20 nm to 14 nm. In the next section, 2-D buckling on 235-nm BPSG will be measured and shown to be slower and of lower amplitude and wavelength, compared to the previous results on 1-μm BPSG, as predicted by the models.

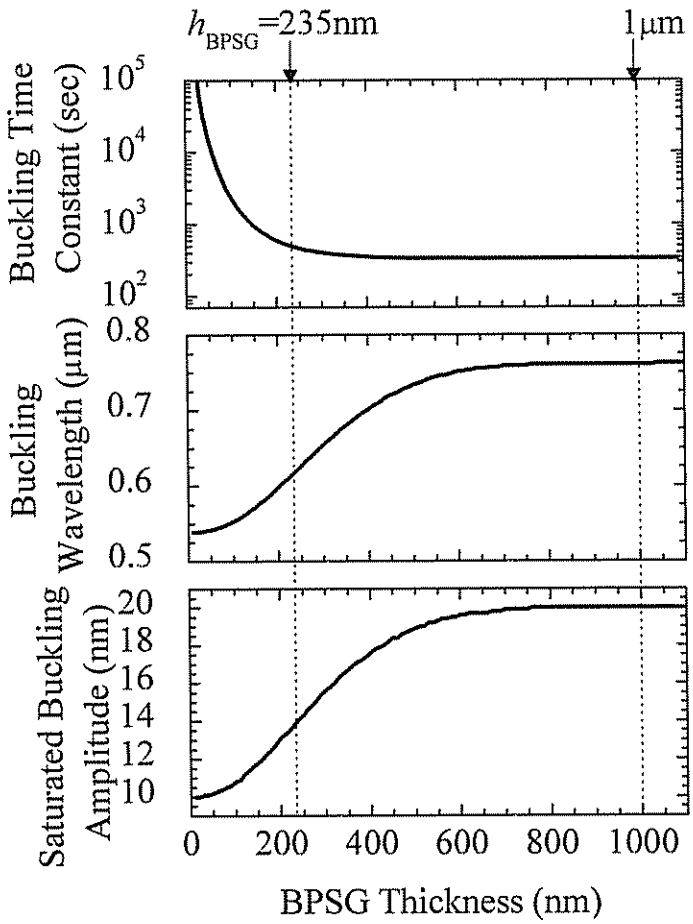


Figure 6.12: Predicted buckling time constant, τ_B, buckling wavelength, λ, and saturated buckling amplitude, a_{max}, vs BPSG thickness, according to the models of Sec. 6.1.2 and Sec. 6.1.3. Here, a_{max} is calculated using the predicted buckling wavelength. The modeled structure consists of a 30-nm $Si_{0.7}Ge_{0.3}$ layer on BPSG, annealed at 750°C.

6.2.2 Buckling Measurements on Thin BPSG

In the previous section, buckling models were used to predict how buckling parameters τ_B, λ, and a_{max} would vary with BPSG thickness. As the BPSG layer is thinned, it is expected that buckling will slow, and its amplitude and wavelength will be reduced. In this section, the experiments of Sec. 6.1.2 to measure 2-D buckling in thin SiGe films on 1-μm BPSG are repeated using 235-nm BPSG to test this hypothesis. The experiments confirm what the models predict: with thinner BPSG, buckling is slowed and the buckling amplitude and wavelength are shortened. In fact, the observed reduction in buckling due to BPSG thinning is even more dramatic than that predicted by the models.

AFM images of buckled 30-nm $Si_{0.7}Ge_{0.3}$ films on 235-nm BPSG at the center of 150-μm x 150-μm islands are shown for a variety of anneal times in Fig. 6.13. Cross-sections taken from these scans are plotted in Fig. 6.14. The initial SiGe surface is very flat (Fig. 6.13a). After a brief 25-min anneal at 750°C (Fig. 6.13b), the surface has slightly roughened, and as the anneal progresses (Fig. 6.13c) the surface is marked by bumps. Note qualitatively the drastic change in the time scale of buckling: in Fig. 6.4a after a 15-min anneal at 750°C, the SiGe on 1-μm BPSG is significantly buckled, while after a slightly longer (25-min) anneal at the same temperature, the SiGe on 235-nm BPSG is only very slightly roughened (Fig. 6.13b). As the anneal continues (Fig. 6.13c-f), these "bumps" aggregate into lines of buckles aligned along the <100> planes, as described earlier. The AFM image of Fig. 6.13f corresponds to the center of an island very similar to the one shown in the optical micrographs of Fig. 6.3.

The cross-sections of Fig. 6.14 show that the buckles are approximately sinusoidal, as assumed in the models of Sec. 6.1.2 and 6.1.3. (The AFM buckling progression and cross-sections of Figs. 6.13 and 6.14 are shown for the 235-nm BPSG case and not for 1-μm BPSG because the slower buckling time on 235-nm BPSG uniquely allows one to glimpse the buckling process in action.)

The buckling amplitude for SiGe on 235-nm BPSG is plotted vs anneal time in Fig. 6.15a. An initial exponential buckling time constant of τ_B = 88 min for 235-nm BPSG has been fit to the measured data. This is more than 15x greater than the measured τ_B = 5.1 min for 1-μm BPSG. (The data of Fig. 6.5 showing 2-D buckling on 1-μm BPSG

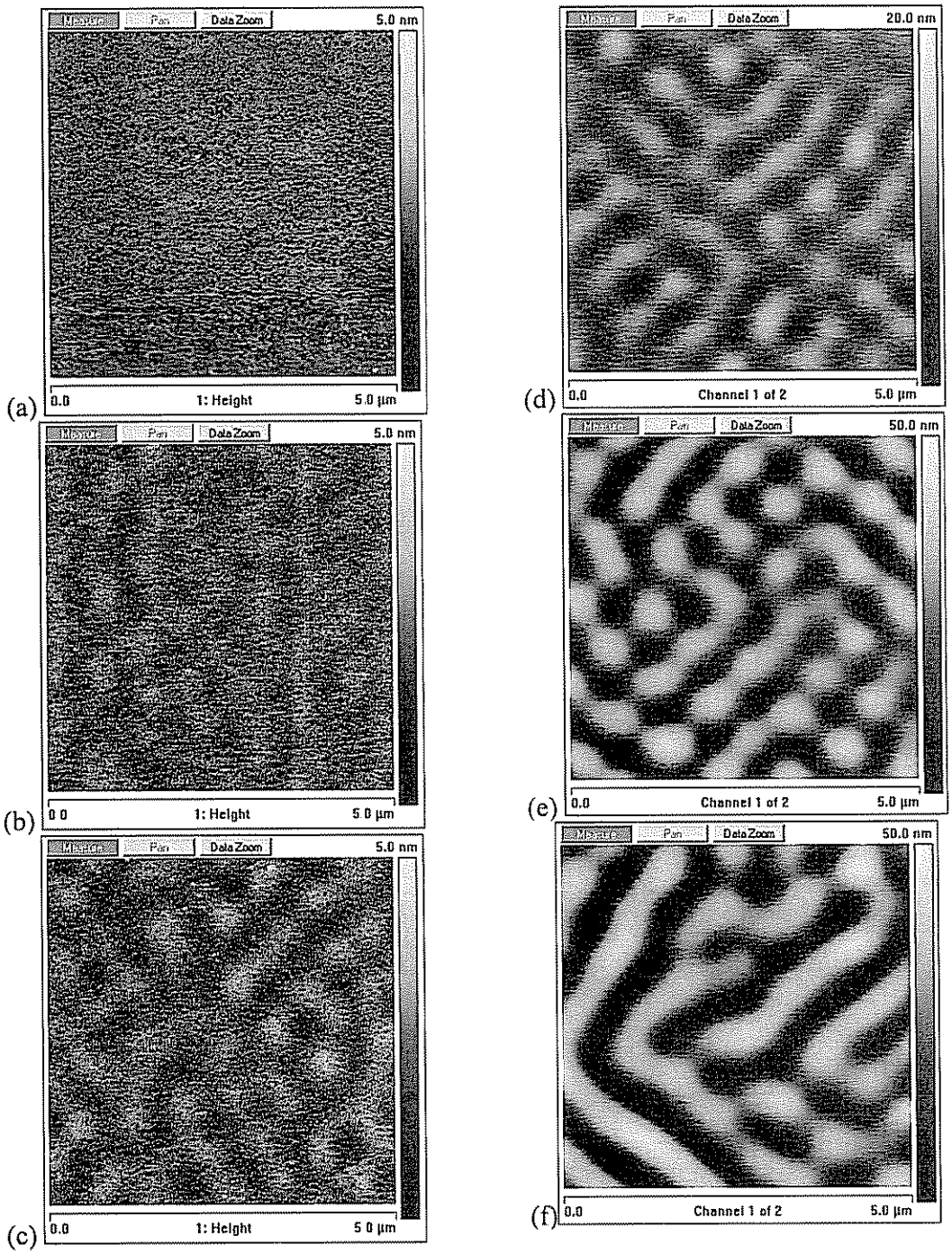


Figure 6.13: AFM images of buckled SiGe on 235-nm BPSG at the center of 150-µm x 150-µm islands after 750°C anneals of various lengths: (a) no anneal, (b) 25 min, (c) 50 min, (d) 105 min, (e) 253 min, and (f) 600 min. The AFM scan size is 5 µm x 5 µm, and the z-axis scale is indicated for each image. The scan edge is along a <110> crystal direction; buckles are along <100>, as before.

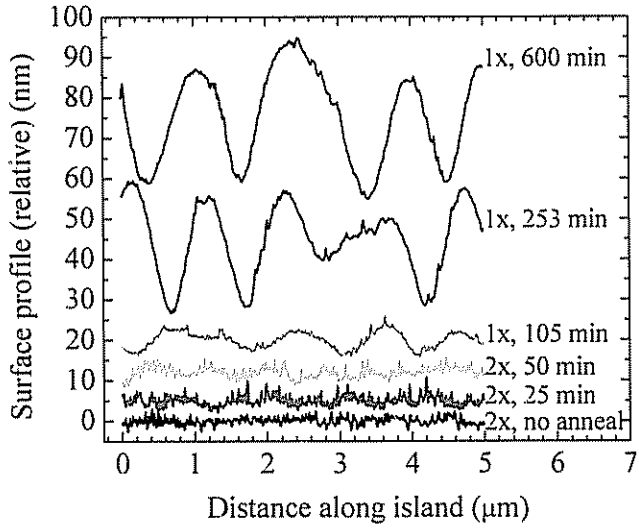
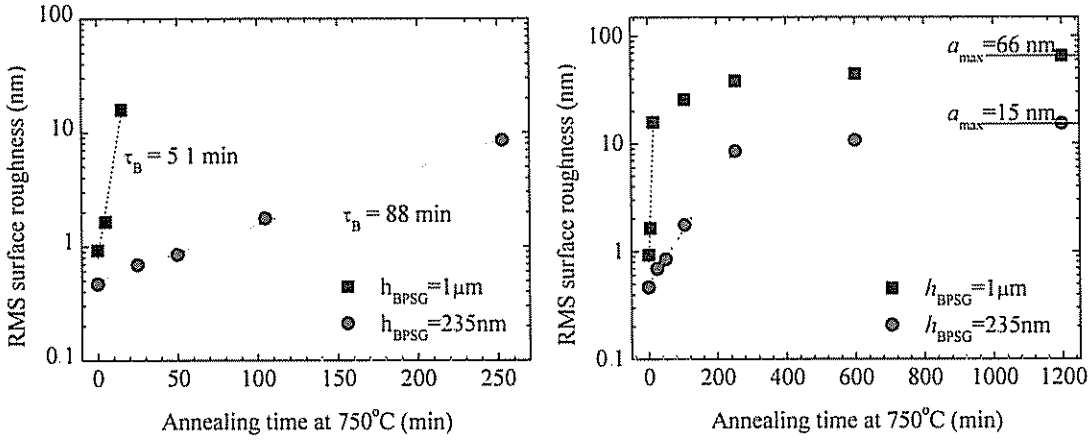


Figure 6.14: Representative cross-sections of the measured AFM scans shown in Fig. 6.13a-f. The surface roughness traces, which exhibit a sinusoidal shape, have been offset along the vertical axis to provide visual separation. Some of the small amplitude scans have been amplified by a factor of two, as indicated in the plot.



(a) (b)

Figure 6.15 Buckling amplitude vs anneal time at 750°C for 30-nm SiGe on 1-μm and 235-nm BPSG for (a) short and (b) (expanded x-axis) long anneal times. The points are measured data and the dotted lines are fitted exponentials to Eqn. 6.2, using the indicated values of τ_B. The initial SiGe film buckling shown in (a) is much slower on 235-nm BPSG than on 1-μm BPSG. In (b), the thinner BPSG exhibits a much smaller buckling amplitude, a_{max}, as shown. The data for 1-μm BPSG is identical to that of Fig. 6.5.

are repeated in Fig. 6.15 for comparison.) Thinning the BPSG from 1 μm to 235 nm has dramatically slowed the buckling process.

As seen previously for thick BPSG, buckling of SiGe on 235-nm BPSG gradually slows and reaches an equilibrium state (see Fig. 6.15b), where the buckling amplitude measured after a 20-hr anneal at 750°C is a_{max} = 15 nm. This is a dramatic improvement over the a_{max} = 66 nm measured for 1-μm BPSG. The analytical model for a_{max} (Eqn. 6.20) states that a_{max} is not a direct function of BPSG thickness. The strong reduction in a_{max} must thus be explained through a change in buckling wavelength. Compare the 25-μm x 25-μm AFM scan image for 235-nm BPSG shown in Fig. 6.16 to the image in Fig. 6.4b taken of a similarly prepared sample on 1-μm BPSG. The buckling wavelength has significantly decreased, from 2.1 μm for 1-μm BPSG to 0.91 μm for 235-nm BPSG. The buckling wavelength decreases with BPSG thickness because thinner BPSG is less readily displaced across long distances ($\sim\lambda$) in the plane of the film in order to form the buckles, *i.e.*, the buckling wavelength cannot be orders of magnitude greater than the BPSG thickness.

This reduction in buckling wavelength also changes the saturated buckling amplitude. As the buckling wavelength is reduced, the buckles are more densely packed and thus less buckling amplitude is needed to relieve the same amount of initial film strain. The relationship between buckling amplitude and wavelength required for minimum film energy is given by Eqn. 6.20. The impact of BPSG thickness on a_{max} is shown in Fig. 6.17, where the total strain energy density of Eqn. 6.18, Φ_{total}, is plotted vs buckling amplitude, a, for the two measured wavelengths. As the BPSG is thinned, the wavelength shrinks, causing the minimum energy point to shift and the value of a_{max} to decrease, as described analytically by Eqn. 6.20. For 235-nm BPSG with λ=0.91 μm, the predicted value of a_{max} = 26 nm is reasonably close to the measured value of 15 nm. The changes in buckling parameters with BPSG thickness predicted by the models have been experimentally observed: as the BPSG is thinned from 1 μm to 235 nm, τ_B strongly increases and a_{max} and λ both significantly decrease.

Note also that the observed increase in τ_B caused by BPSG thinning from 1 μm to 235 nm (τ_B goes from 5.1 min to 88 min) is much more than that predicted by theory

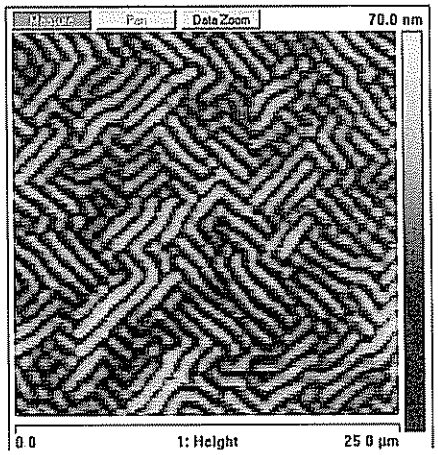


Figure 6.16 Atomic Force Microscopy (AFM) image of a buckled 30nm $Si_{0.7}Ge_{0.3}$ layer on 235-nm BPSG for a 25-µm x 25-µm scan taken at the center of a 120-µm x 120-µm island after a 10-hour anneal at 750°C, with RMS surface roughness of 12 nm. Note the greatly reduced buckling amplitude and wavelength compared to that for 1-µm BPSG in Fig. 6.4b.

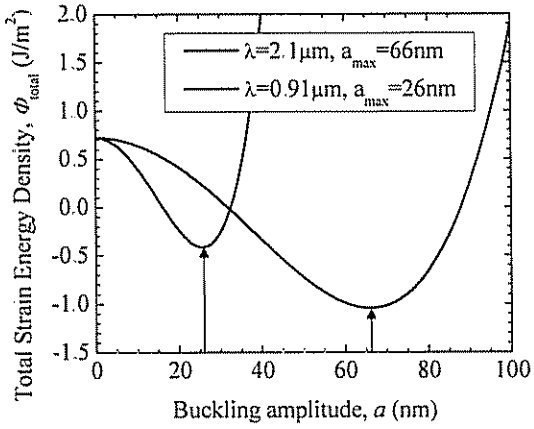


Figure 6.17 Total strain energy density from Eqn. 6.18 for 1-µm BPSG and 235-nm BPSG, using the measured buckling wavelengths of λ=2.1 µm and 0.91 µm, respectively. The expected values for a_{max} of 66 nm and 26 nm, respectively, which correspond to minimum film energy, are indicated. The Φ_{total} curve for λ=2.1 µm was shown previously in Fig. 6.10.

(5.5 min to 8.3 min). (The predicted time constants are calculated using the predicted buckling wavelengths of 0.76 μm and 0.62 μm. Using the observed buckling wavelengths of 2.1 μm and 0.91 μm in the model yields τ_B values of 12.1 min and 14.0 min for 1-μm and 235-nm BPSG, respectively – an even smaller increase.) Since in the buckling theory the buckling time constant is directly proportional to BPSG viscosity, $\tau_B \sim \eta$, this discrepancy between the model and measurement results indicates that the BPSG viscosity of the 235-nm sample is ~10x greater than expected. The viscosity value used in the model is 5.5×10^{10} Pa, which was obtained previously [8,111] by fitting the square island lateral relaxation model to Raman-measured strain data on other samples (see Sec. 4.2). To fit the 235nm BPSG buckling data, the value of η would need to increase to 5.8×10^{11} Pa. The discrepancy in viscosity values measured by lateral relaxation and buckling may be due to differences in the two theories, which use different BPSG layer models, or to inhomogeneity of the BPSG viscosity (as described in Sec. 4.2), or to a new effect with thin BPSG that is unaccounted for in the buckling models of Sec. 6.1.2.

In summary, by thinning the BPSG layer from 1-μm to 235-nm BPSG, the measured buckling parameters improve significantly: buckling is much slower, of much smaller maximum amplitude, and is characterized by a shorter buckling wavelength. The measured and predicted results for 2-D buckling on 1-μm and 235-nm BPSG are summarized in the second columns of Tables 6.1 and 6.2, respectively.

6.2.3 Buckling on Ultra-thin BPSG

In the previous section, it was shown that by thinning the BPSG layer, buckling becomes slower and of lower amplitude. But can thinning the BPSG help achieve the stated goal of large SiGe films that are flat and fully relaxed? In Fig. 6.18a, an image of buckled square islands on 235-nm BPSG is shown. Comparing with Fig 6.11a for 1-μm BPSG, on large islands (L > 80 μm) there are again clearly visible buckles aligned to <100> and cracks aligned to <110>. The measured buckling amplitude vs island edge length for these two BPSG thicknesses is plotted in Fig. 6.18b. While the thinner BPSG shows a greatly reduced buckling amplitude, as seen previously, the critical island size,

Buckling parameter	*2D*	*1D*	*Ratio: 1D/2D*
Time constant, τ_B	88 min (8.3 min)	217 min (16 min)	2.5 (1.9)
Wavelength, λ	0.91 μm (0.62 μm)	0.94 μm (0.70 μm)	1.0 (1.1)
Amplitude, a_{max}	15 nm (26 nm)	11 nm (22 nm)	0.73 (0.85)

Table 6.2: Summary of measured and modeled buckling parameters for 2D and 1D buckling for 30-nm $Si_{0.7}Ge_{0.3}$ on 235-nm BPSG annealed at 750°C. Values predicted by modeling (with BPSG viscosity $\eta = 5.5 \times 10^{10}$ Pa) are in parentheses.

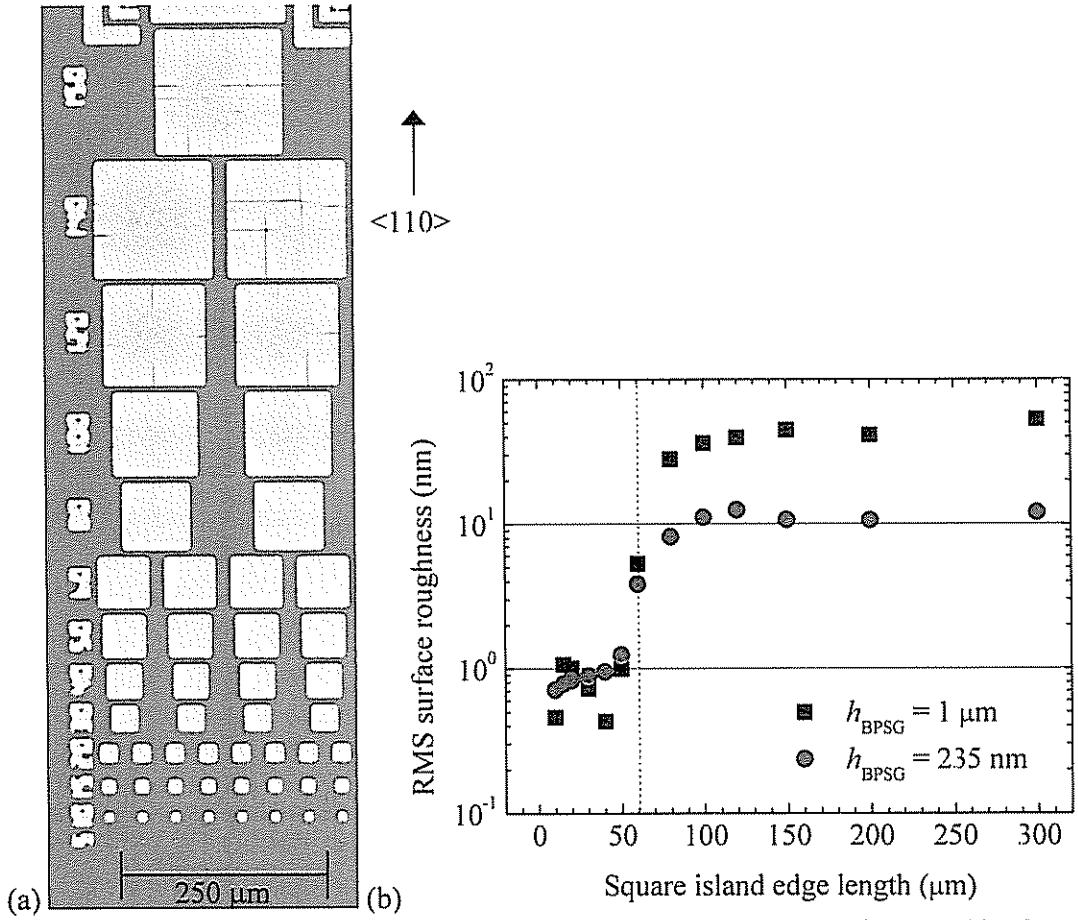


Figure 6.18: (a) Optical micrograph of buckled and cracked islands of 30-nm $Si_{0.7}Ge_{0.3}$ on 235-nm BPSG annealed for 10 hrs at 750°C. Compare to Fig. 6.11a for 1-μm BPSG. Here, the island edges are aligned to <110> crystal directions. Buckles aligned to <100> and cracks aligned to <110> are visible in the larger islands. (b) Comparison of measured RMS surface roughness vs island edge length, L, for BPSG thickness of 1 μm (data identical to Fig. 6.11b) and 235 nm (as pictures in (a)) after a 10-hr anneal at 750°C. In both cases flat islands are only possible when $L < 60$ μm.

above which buckling dominates over lateral expansion, is 60 μm, the same as for 1-μm BPSG. Despite slowing down buckling and limiting its amplitude, the maximum flat island size has *not* increased at all by thinning of BPSG from 1 μm to 235 nm.

Fundamentally, in order to allow lateral relaxation to dominate over buckling, τ_B must be much larger than τ_L. One might suspect that by annealing at a different temperature, some advantage might be gained from the temperature-dependent change in BPSG viscosity. Unfortunately, according to the models (Eqns. 3.9 and 6.3-6.5), both τ_L and τ_B are directly proportional to viscosity, so that changing the temperature is expected to yield no benefit. To confirm this, identical 235-nm BPSG samples were annealed at different temperatures for different anneal times (10 hrs at 750°C; 90 min at 800°C). The anneal conditions were chosen to effect the same amount of lateral relaxation in the two samples, as shown by the Raman measured data in lower half of Fig. 6.19. In the upper half of this figure, the AFM-measured buckling amplitude data is shown. For the same amount of relaxation, the buckling amplitude is identical for the two samples, regardless of the anneal temperature and time. So, temperature is not a useful parameter to manipulate the balance between buckling and lateral relaxation.

In order to understand the buckling results on 235-nm and 1-μm BPSG, the buckling models are examined again in more detail. In Fig. 6.20a, τ_L/π^2 and τ_B are plotted vs BPSG thickness. As the BPSG becomes very thin, *i.e.*, < 100 nm, the buckling time constant is predicted to increase dramatically compared to the lateral relaxation time constant. τ_L is calculated for L=10 μm so that $\tau_L/\pi^2 \approx \tau_B$ at h_{BPSG}=235 nm. Here it is the ratio between τ_B and τ_L that is important, not the absolute values. In Fig. 6.20b, the plotted τ_B/τ_L ratio reaches a minimum, at which buckling is expected to be most dominant, around h_{BPSG} = 200 nm. For thinner BPSG layers (< 200 nm), it becomes very hard to displace the BPSG to form the long-wavelength buckles and thus the buckling time constant increases rapidly. The increased τ_B/τ_L ratio for very thin BPSG should provide an advantage for lateral expansion over buckling, to achieve large, flat islands. For much thicker BPSG (> 400 nm), additional BPSG thickness does not increase the speed with which the film buckles and τ_B stabilizes, while the lateral expansion time constant, τ_L, decreases according to h_{BPSG}^{-1}. As h_{BPSG} increases from 235 nm to 1 μm the

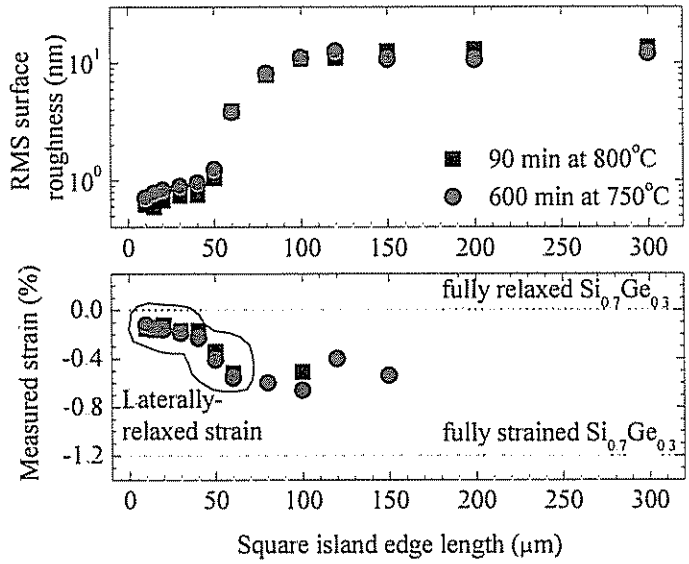
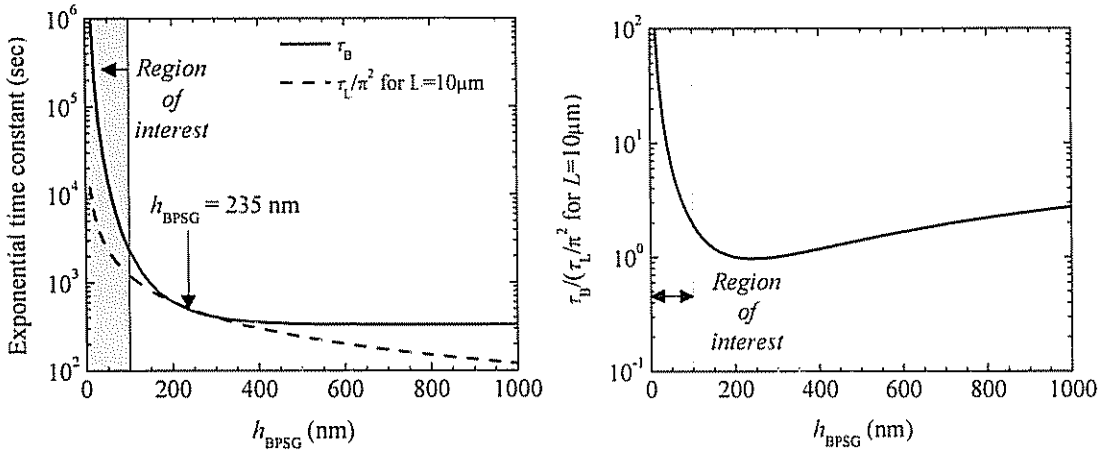


Figure 6.19: The upper plot shows RMS surface roughness vs square island edge length for two samples with h_{BPSG}=235 nm processed with different anneal temperatures and times. The critical island size to avoid buckling is 60 μm, regardless of anneal temperature. The lower plot shows Raman-measured strain at the center of the islands. As shown by the circled data in this plot, the anneal times were chosen so that the degree of strain relaxation is similar for the two samples. For islands larger than the 60 μm, the Raman peak is broad and thus does not give an accurate measure of the film strain.



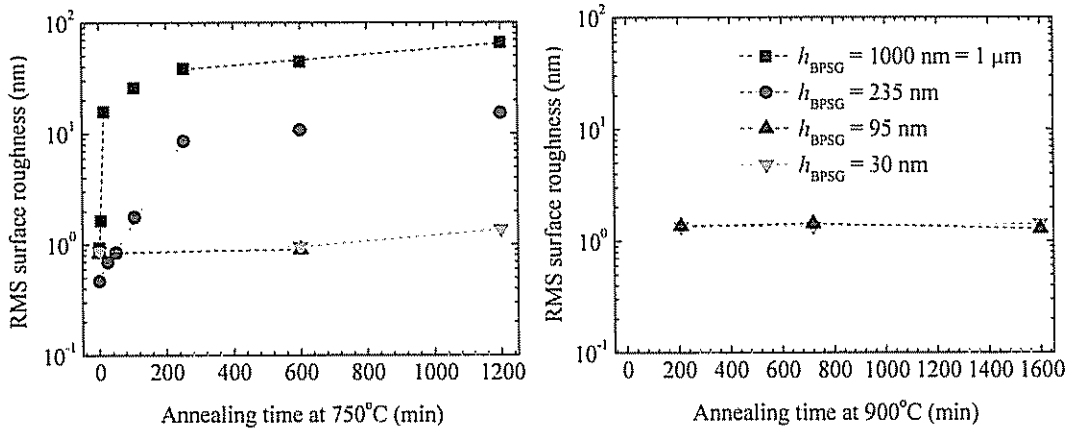
(a) (b)

Figure 6.20: (a) Exponential buckling and lateral relaxation time constants, and (b) the ratio of τ_B to τ_L, vs BPSG thickness. The lateral relaxation time constant, is divided by π^2 as described in Ch. 4, and is calculated for L = 10 μm. For thin BPSG (<100 nm), the large τ_B compared to τ_L offers the possibility of flat, relaxed SiGe films.

τ_B/τ_L ratio increases only slightly. At intermediate BPSG thicknesses around 200 nm, the distance the BPSG needs to travel to form buckles is approximately equal to its thickness: $\lambda/2 \approx h_{BPSG}\sqrt{2}$. Under this condition the BPSG can readily form buckles, and the relatively thin BPSG means that lateral expansion is slow. This explains the lack of improvement in flat island size for 235-nm BPSG compared 1-μm BPSG seen in Fig. 6.19b – the ratios between τ_B and τ_L are similarly small for these two BPSG thicknesses and thus buckling dominates for large islands. However, it is clear from Fig. 6.20b that for BPSG less than 100 nm thick, τ_B/τ_L is predicted to increase dramatically and thus the impact of buckling should be sharply reduced, allowing large, flat, relaxed SiGe films. It is to this parameter space that attention is now focused.

Additional samples with 30-nm $Si_{0.7}Ge_{0.3}$ (and 1-2 nm Si caps, hereafter neglected) were bonded to wafers with 95-nm and 30-nm BPSG, and the annealing experiments on large square islands were repeated. In Fig. 6.21, the measured buckling amplitudes are plotted vs anneal time for anneal temperatures of 750°C and 900°C. For even a very long (~ 27-hr) anneal at 900°C, the measured surface roughness is < 2 nm – the films are still flat. These results *seem* to indicate that the model predictions of Fig. 6.20 are indeed correct: thin BPSG will lead to very slow buckling. Unfortunately, the viscosity of these samples is much higher (~400x) than that of the thicker BPSG (235-nm and 1-μm) samples, and thus it is impossible to draw any substantial conclusions about the advantages of thin BPSG from this data.

The inconsistency in BPSG viscosity may be due to different preparation methods used for the BPSG films. The 95-nm BPSG sample was prepared by the standard BPSG process, with CVD deposition of 50-nm BPSG followed by wet oxidation at 800°C for 1 hr, after which a thickness of 95 nm was measured by reflectometry. The thickness increase after oxidation indicates that a large portion of SiO_2 has been incorporated into the BPSG matrix. At 900°C this sample exhibited partial SiGe relaxation, and a viscosity value of η=3.3·10^{11} N·s·m^{-2} was obtained by curve-fitting as described in Sec. 4.2. The 30-nm BPSG sample was prepared differently, using a dry instead of wet oxidation step, in an effort to minimize the viscosity change. Nonetheless, on this sample no SiGe relaxation was observable by Raman spectroscopy (it showed the full initial biaxial



(a) (b)

Figure 6.21: Buckling amplitude vs anneal time at (a) 750°C and (b) 900°C for various BPSG thickness. Symbols are measured data, dotted lines are to guide the eye. The thin BPSG layers show very low buckling amplitudes even after significant annealing. This may be due to the predicted thin BPSG effect illustrated in Fig 6.20, but more likely can be attributed to the very high measured viscosities of these films (see text).

strain, ε_0 for all anneal times and temperatures.). Clearly, the viscosity of these samples is much higher than that of the thicker BPSG and therefore the buckling data presented in Fig. 6.21 cannot be directly compared. Further experimental work is thus needed to establish the efficacy of thin BPSG for reducing buckling and enabling large, flat, SiGe islands, as predicted by the models.

6.3 One-dimensional Buckling in Uniaxially-Stressed SiGe Films

So far in this chapter the two-dimensional buckling that occurs in biaxially-stressed SiGe films has been quantitatively described, and it has been shown that by thinning the BPSG layer, buckling can be slowed and its amplitude reduced. Earlier, in Ch. 3, a new experimental method was used to obtain uniaxially-stressed SiGe, which is technologically of interest because the method can be readily extended to achieve uniaxially-strained silicon. These uniaxially-stressed/strained films can also buckle, and thus it is of critical importance to now examine buckling under the case of 1-D film stress, in order to minimize its technological impact. In this section, two-dimensional and one-dimensional buckling in thin silicon-germanium films under biaxial and uniaxial compressive stress, respectively, are quantitatively compared. For the same strain level, films with one-dimensional stress and thus one-dimensional buckling exhibit slower buckling and lower final steady state buckling amplitude, which makes them technological advantageous compared to biaxially-strained films, which exhibit two-dimensional buckling. The results are explained by modifying the previously-presented 2-D buckling models.

The same samples described above, with 30-nm $Si_{0.7}Ge_{0.3}$ on 235-nm or 1-μm BPSG, are used for these experiments. The SiGe layer is patterned into islands and annealed at 750°C. The type of stress that results is determined by island shape as described in Sec. 3.5.3. For square islands aligned to <100>, the initial in-plane stress is calculated using Eqn. 3.14a to be $\sigma_{\text{biaxial}} = E\varepsilon_{\text{biaxial}}/(1-\nu)$ = -2.0 GPa. At the center of large square islands, lateral expansion is negligible and the film stress changes slowly as it is relieved by buckling. In contrast, a rectangular island quickly relaxes in the short

direction to zero stress ($\sigma_{short} = 0$), while in the island long direction strain changes much more slowly and thus is effectively pinned to its initial value ($\varepsilon_{long} = \varepsilon_o$). From Hooke's law, one can calculate stress in the long direction from Eqn. 3.14c to be $\sigma_{uniaxial} = E\varepsilon_o$ = -1.5 GPa. The biaxial stress, $\sigma_{biaxial}$, is greater than uniaxial stress, $\sigma_{uniaxial}$, due to the Poisson effect of the non-zero compressive stress in the perpendicular in-plane direction. So after a brief relaxation anneal, a narrow rectangular island of SiGe film will have uniaxial in-plane stress driving the buckling process, while the center of a large square island will maintain its initial, larger biaxial stress.

The type of buckling is directly determined by the type of stress: 2-D stress yields 2-D buckling (as seen above in Sec. 6.1-6.2) while 1-D stress yields 1-D buckling. Fig. 6.22a-c shows AFM images of 2-D and 1-D buckling for square and rectangular islands, respectively, on the same sample. In Fig. 6.22b, the rectangular island edge is aligned to the <110> crystal direction while in Fig. 6.22c, it is aligned to <100>. In both cases, buckling occurs perpendicular to the long direction, *regardless of island orientation*, confirming that the rectangle orientation (and thus the direction of 1-D stress) determines the direction of 1-D buckling. Note that the 1D and 2D buckling directions are determined by different mechanisms: 1D buckling by the direction of 1D stress, and 2D buckling by the direction of the fastest buckling growth rate (*i.e.*, the <100> crystal direction) as shown in Fig. 6.9. In addition to controlling the direction of the buckles, 1-D stress causes slower buckling than 2-D stress, even for the same film strain perpendicular to the ridges of the buckles. This phenomenon will be examined in the next section.

6.3.1 Comparing 1-D and 2-D Buckling: τ_B and λ

One-dimensional (1-D) buckling is measured at the center of rectangular islands sized 20 μm x 150 μm. The island size is chosen such that in the short direction the island center relaxes to zero stress after annealing for less than two hours at 750°C, quickly creating a state of uniaxial stress in which 1-D buckling can occur. A plot of the evolution of 1-D stress in a narrow rectangular island, derived from the model of Ch. 4 and using Eqn. 3.14 to calculate film stress from strain, is shown in Fig. 6.23. The 1-D

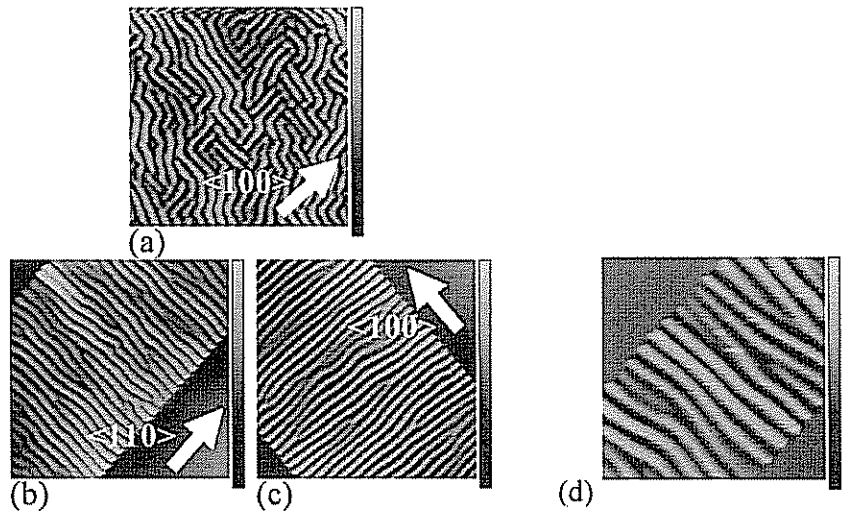


Figure 6.22: AFM images of SiGe on 235-nm BPSG islands: (a) 2-D buckling at the center of a square island, 150 μm x 150 μm; (b) and (c) 1-D buckling at the center of rectangular islands, 20 μm x 150 μm, aligned to the <110> and <100> crystal directions, as indicated, after a 20-hour anneal at 750 °C. The AFM scan size is 25x25 μm^2 and the z-axis scale is 70 nm. Image (d) shows 1-D buckling on 1-μm BPSG at the center of a 20-μm x 150-μm island aligned to the <100> crystal direction after a 10-hour anneal at 750°C, for comparison with 2-D buckling in Fig. 6.4. In (d) The AFM scan size is 25x25-μm^2, with a z-axis scale of 180 nm.

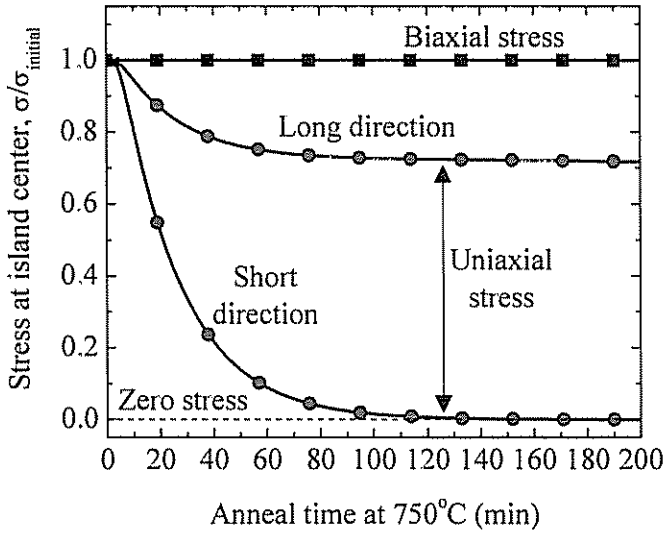


Figure 6.23: Predicted biaxial and uniaxial stress vs anneal time for a 30-nm SiGe layer on 235-nm BPSG patterned into square islands, 150 μm x 150 μm, and rectangular islands, 20 μm x 150 μm, respectively, aligned to the <100> crystal direction. The stress is calculated using Eqn. 3.14 from film strain modeled as described in Ch. 4. Symbols are indicated every 1000 points, in order to identify the different lines.

stress state is experimentally verified for selected samples by micro-Raman spectroscopy (see Fig. 3.31).

In Fig. 6.24, the 1-D buckling amplitude at the center of rectangular islands with edges aligned to the <100> crystal direction in the (001) surface plane of the film is plotted vs anneal time. The 1-D buckling amplitude initially grows exponentially and later stabilizes, as in the two-dimensional (2-D) buckling case. For both BPSG thicknesses, the 1-D buckling is significantly slower than 2-D buckling. On 235-nm BPSG, the extracted initial buckling time constant for 1-D buckling, 217 min, is about 2.5 times longer than τ_B for 2-D buckling (88 min). For 1-μm BPSG, there is a similarly large increase in τ_B from 5.1 min to 7.9 min going from 2-D to 1-D buckling.

The longer buckling time constant occurs because in the 1-D case the stress in the direction of buckling, $\sigma_{uniaxial}$, is much lower than that in the biaxial case, $\sigma_{biaxial}$, due to the Poisson effect described earlier. The stress perpendicular to the ridges determines buckling, not the strain (which is equal in the square and rectangular island cases). The lower magnitude of stress provides less of a driving force for buckling, and thus buckling occurs more slowly in the uniaxial case, despite the fact that in both cases the strain in the direction of buckling is equal to the original ε_0 of the SiGe. These measured 1-D vs 2-D buckling trends can be quantitatively understood by modifying the 2-D buckling model presented in Sec. 6.1.2. In Ref. [162], 2-D buckling is modeled as a one-dimensional process for analytical ease, but the stresses parallel and normal to the buckles are assumed to be identical and equal to $\sigma_{biaxial}$, as sketched schematically in Fig. 6.25. To model 1-D buckles, instead one must assume zero stress normal to the buckles. The only resulting change is to Eqn. 6.4, which becomes

$$\alpha = \frac{Ekh_{SiGe}}{24\eta\left(1-\nu^2\right)}\left[-12\sigma\left(\frac{1-\nu^2}{E}\right)-\left(kh_{SiGe}\right)^2\right]\gamma_{11}, \tag{6.22}$$

where σ represents the stress in the direction of buckling, $\sigma_{uniaxial}$ or $\sigma_{biaxial}$. The value of α is used to calculate s_1 and thus τ_B (see Eqns. 6.3-6.8). In general as α decreases, τ_B increases.

Because $|\sigma_{uniaxial}| < |\sigma_{biaxial}|$, these calculations predict that τ_B will approximately double for h_{BPSG}=235 nm, from 8.3 min for 2-D buckles to 16 min for 1-D buckles. For

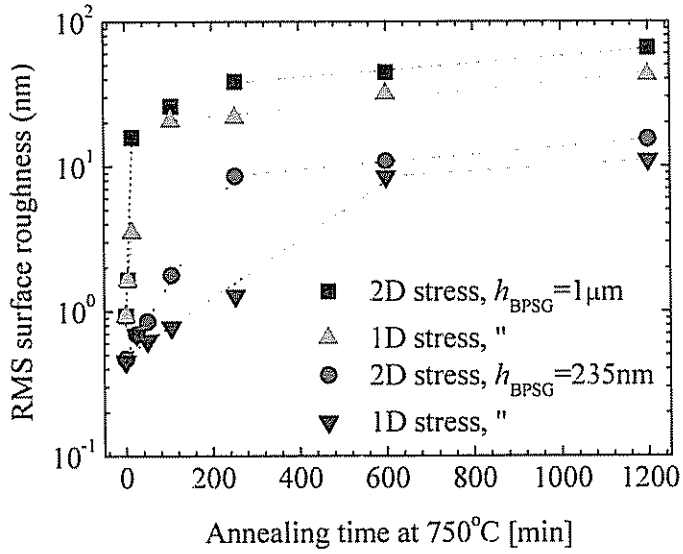


Figure 6.24: Measured buckling amplitude vs anneal time at 750°C, for 1-D and 2-D buckling on 1-μm and 235-nm BPSG, as indicated in the legend. Dotted lines show the exponential growth of buckling while symbols are measured data. Fitted values of τ_B are given in Tables 6.1 and 6.2. The 2-D buckling data is identical to that shown previously in Fig. 6.15.

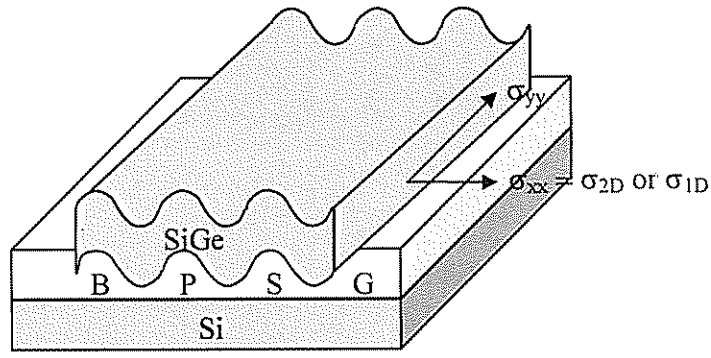


Figure 6.25: Schematic cross-section of buckled SiGe film on BPSG used in the model for τ_B and λ. In the 2-D buckling model, $\sigma_{yy} = \sigma_{2D}$, whereas for 1-D buckling, $\sigma_{yy} = 0$.

1-μm BPSG, τ_B is predicted to increase about 60% from 5.5 min to 9.0 min. The experimental results indicate similarly large increases of 2.5x and 1.6x, respectively. The larger buckling time constant of 1-D buckling compared to 2-D buckling can thus be attributed to the lower value of uniaxial stress compared to biaxial stress for the same film structure, and is technologically quite advantageous.

The measured buckling wavelengths increase very slightly from 2-D to 1-D buckling, as seen by comparing Fig. 6.22a-c for 235-nm BPSG to Fig. 6.4b and 6.22d for 1-μm BPSG. This observation is borne out by the models, which predict that λ will increase by 10-20% going from 2-D to 1-D buckling.

6.3.2 Comparing 1-D and 2-D Buckling: a_{max}

After the initial exponential growth of buckling amplitude, the film strain is partially relieved, and buckling slows for both 2-D and 1-D buckling, as shown in Fig. 6.24. The buckling amplitude saturates, and for 1-D buckling the saturation amplitude, a_{max}, is less than that for 2-D buckling. The value of a_{max} measured by AFM after a 20-hour anneal at 750 °C, is reduced from 15 nm for 2-D buckles to 11 nm for 1-D buckles on 235-nm BPSG, and from 66 nm to 43 nm for 1-μm BPSG.

To model the reduction of a_{max} with 1-D buckling, the strain energy model developed in Sec. 6.1.3 is used. Replacing Eqn. 6.16 by

$$u_y = -(1+\nu)\varepsilon_o y, \tag{6.23}$$

the result $\varepsilon_{yy}=-\nu\varepsilon_o$ is obtained as described in Ch. 4 for the case of uniaxial SiGe stress, and $\varepsilon_{xy}=\varepsilon_{yx}=0$. Solving Eqns. 6.9-6.15 and 6.17 with Eqn. 6.23, the strain energy of an arbitrarily buckled film is calculated to be:

$$\Phi_{total} = \frac{h_{SiGe}}{2}\sum_{x,y,z}(\sigma_i\varepsilon_i) + \frac{E}{(1-\nu^2)}\frac{h_{SiGe}^3}{48}a^2k^4 + \frac{E}{(1-\nu^2)}\frac{3h_{SiGe}}{64}a^4k^4 + \ldots$$
$$\ldots + \frac{h_{SiGe}}{4}\sigma a^2k^2 + \frac{E}{(1-\nu^2)}\frac{h_{SiGe}}{4}b^2k^2 \tag{6.24}$$

The changes from Eqn. 6.18, which is valid only for 2-D buckled films, to Eqn. 6.24, which is valid for any type of biaxial strain (symmetric or asymmetric), are in the first and fourth terms. The summation is over the two in-plane directions, *i.e.*, it is equal to

$2\sigma_{biaxial}\varepsilon_o$ or $\sigma_{uniaxial}\varepsilon_o$ for biaxial or uniaxial stress, respectively. In the fourth term, σ is defined as the stress in the buckling direction, just as for Eqn. 6.22.

In Fig. 6.26, the strain energy density of Eqn. 6.24 is plotted vs buckling amplitude, a, for the 1-D and 2-D buckling cases, using the observed buckling wavelengths, λ. The minima of the curves correspond to the equilibrium buckling amplitude, a_{max}, which can be written as

$$a_{max} = \sqrt{-\frac{2}{9}\left[h_{SiGe}{}^2 + 3\sigma\left(\frac{1-\nu^2}{E}\right)\left(\frac{\lambda}{\pi}\right)^2\right]}. \qquad (6.25)$$

The only change from Eqn. 6.20 to 6.25 is the value of σ, which now defined as the stress in the buckling direction, $\sigma_{uniaxial}$ or $\sigma_{biaxial}$. This model predicts smaller buckling amplitudes for 1-D vs 2-D: a_{max} = 26 nm for 2-D buckling with λ = 0.91 μm and a_{max} = 22 nm for 1-D buckling with λ = 0.94 μm for h_{BPSG} = 235 nm. Note that the slight change in buckling wavelength only accounts for a 1.0 nm shift in a_{max}; the majority of the change in a_{max} is due to the difference between $\sigma_{uniaxial}$ and $\sigma_{biaxial}$. Therefore, the reduction in buckling amplitude observed for 1-D buckling compared to 2-D buckling can also be attributed to the reduced uniaxial stress compared to biaxial stress.

6.3.3 Conclusions on 1-D vs 2-D Buckling

Tables 6.1 and 6.2 provide a summary of modeled and measured data. For compressively strained SiGe films on BPSG, the 1-D buckling process, generated by uniaxial stress, is significantly slower and the buckling amplitude is reduced compared to that for 2-D biaxially strained films. This is because buckling in any given direction depends on the film stress in that direction. For the same strain in the buckling direction (here, ε_o) the Poisson effect causes the uniaxial stress in that direction to be less than the biaxial stress, reducing the driving force for buckling. Notes that if $\sigma_{uniaxial}$=$\sigma_{biaxial}$, then τ_B as well as a_{max} will be identical for the uniaxial and biaxial stress cases, while Φ_{total} will differ by a constant. By comparing modeling and experimental data, it has been shown that the observed 1-D and 2-D buckling differences are attributable to the lower 1-D stress. Technologically, this means that buckling is less of a problem for the creation

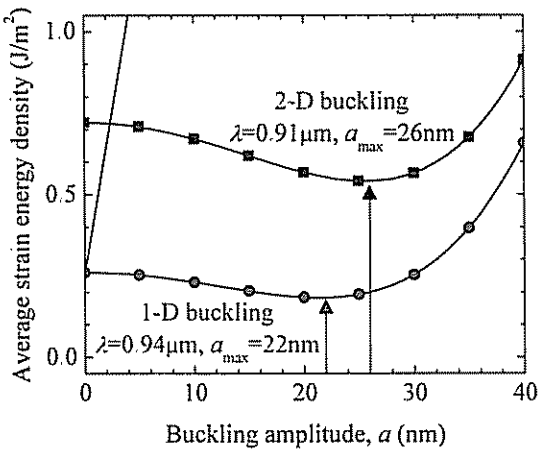


Figure 6.26: Average strain energy density of 1-D and 2-D buckled films vs buckling amplitude for h_{BPSG} = 235 nm, calculated from Eqn. 6.24. The energy curves are plotted for the measured buckling wavelengths, as indicated. Arrows indicate the buckling amplitude at the minimum energy equilibrium state of the film, a_{max}. Symbols are indicated every 50 points, in order to identify the different lines.

of uniaxially-stressed SiGe and uniaxially-strained silicon layers than would be inferred by existing 2-D buckling data and models.

6.4 Summary

In this chapter the buckling of a compressively stressed film on a viscous substrate has been described. Buckling competes with lateral expansion to release the compressive strain in SiGe films on BPSG. In order to achieve flat, relaxed SiGe films, buckling must be well-controlled. By thinning the compliant BPSG layer from 1 μm to 235 nm, it has been shown that the buckling process can be greatly slowed and the buckling amplitude and wavelength reduced. The results are in agreement with existing linear perturbation theory and minimum energy models for 2-D buckled elastic films. Based on these models, further improvement should be possible by continuing to thin the BPSG layer to less than 100 nm.

One-dimensional buckling of uniaxially-stressed SiGe films has also been measured and compared to 2-D buckling in biaxially-stressed layers. 1-D buckling is technologically advantageous in that it has a longer buckling time constant and lower buckling amplitude. By comparison with modeling, these changes can be attributed to the lower amount of 1-D stress compared to 2-D stress for the same level of original film strain, ε_0. While the results here are calculated for SiGe on BPSG, the models should be generally applicable for other compressively strained films on compliant substrates as well.

Chapter 7

FETs on Biaxially- and Uniaxially-Strained Silicon

In Ch. 5, a new technique was demonstrated to generate uniaxially-strained silicon in a thin silicon film on BPSG insulator. From the models presented in Ch. 2 described energy band splitting and warping, it is expected that uniaxially-strained silicon will enable hole and electron mobility enhancement, when the channel and strain alignment to the crystal are properly chosen.

In this chapter, the strain-engineering methods of Ch. 3-5 are used to fabricate uniaxially-strained, biaxially-strained, and unstrained silicon all on the same sample. In these silicon layers, n- and p-channel FETs are fabricated, with various channel alignments for the uniaxial strain case. The resulting silicon-on-insulator (SOI) transistors have low source/drain resistance and operate with a fully-depleted channel. By adding SiN_x/SiO_x barrier layers at the BPSG/Si interface during the initial wafer bonding step, the electronic quality of the back interface (as measured by sub-threshold slope) is improved to be equivalent to standard SOI wafers. Finally, the hole and electron mobility enhancement by biaxial and uniaxial strain is measured and compared to the model predictions of Ch. 2.

7.1 A Strained-Channel FET Process

In order to fabricate strained-channel FETs, first the silicon layer is strained using the lateral expansion process described in Ch. 3-5, and then a standard n- or p-MOS process is used to make field-effect transistors. A unique advantage of method is that biaxially-strained, uniaxially-strain and unstrained silicon islands can be formed on the same SOI sample, out of the same initial silicon film, so they are subject to *identical* device processing. This allows direct comparison of device performance under different strain conditions. Moreover, the direction of the strain relative to the crystal-direction and relative to the charge carrier movement in the channel can be easily manipulated through

layout geometry, allowing the exploration of mobility enhancement under a wide variety of strain conditions. No other known silicon strain technique offers this degree of flexibility (See Sec. 2.4 for a description of other methods). In this section, the two fabrication sequences, silicon strain generation and SOI FET processing, will be described in detail.

7.1.1 Preparing the Strained Silicon Channel Layer

As described in Ch. 3 and 5, a compressively-strained $Si_{0.7}Ge_{0.3}$ and unstrained silicon layer are heteroepitaxially grown on a bulk (001) Si wafer. The high quality of the epitaxial layers was confirmed by photoluminescence (PL) on an as-grown sample. The PL curves are shown in Fig. 7.1a for the sample cross-section of Fig. 7.1b. The PL spectrum exhibits peaks from the SiGe non-phonon (NP) transition as well as the SiGe and Si transverse optical (TO) phonon peaks [169]. No dislocation or defect peaks are visible and the ratio of SiGe/Si TO peak heights is ~30, indicating coherent growth and good epitaxial interface quality. The maximum oxygen content measured by Secondary Ion Mass Spectroscopy (SIMS) in the SiGe layer is ~1.8×10^{18} cm^{-3} (The oxygen concentration in the silicon layer was poorly resolved by SIMS since it lies at the surface of the sample.)

Sometimes, the top silicon layer is capped with a thermally-grown SiO_2 layer and/or a LPCVD SiN_x layer, in order to provide a dopant diffusion barrier between the BPSG (to which the epitaxial layer or capping layer will be bonded) and channel silicon. The SiO_2 growth and SiN_x deposition must be done at relatively low temperatures to prevent premature relaxation and thus defect formation in the SiGe/Si bi-layer and to prevent interdiffusion between the SiGe/Si layers. In Fig. 7.2 the thermal oxide thickness on bulk silicon is plotted vs oxidation time for two different anneal conditions: 750°C wet oxidation and 800°C dry oxidation. The lower temperature wet oxidation process is chosen to minimize the thermal budget for this process. For the samples used here, a wet oxidation at 750°C for 10 min was used, preceded by a 5-min dry oxidation and followed by a 5-min dry oxidation plus a 5-min nitrogen anneal, all at 750°C. This process yields an SiO_2 thickness of 5.1 nm as measured by ellipsometry. In Fig. 7.3 the silicon nitride thickness on bulk silicon is plotted vs low pressure chemical vapor deposition (LPCVD)

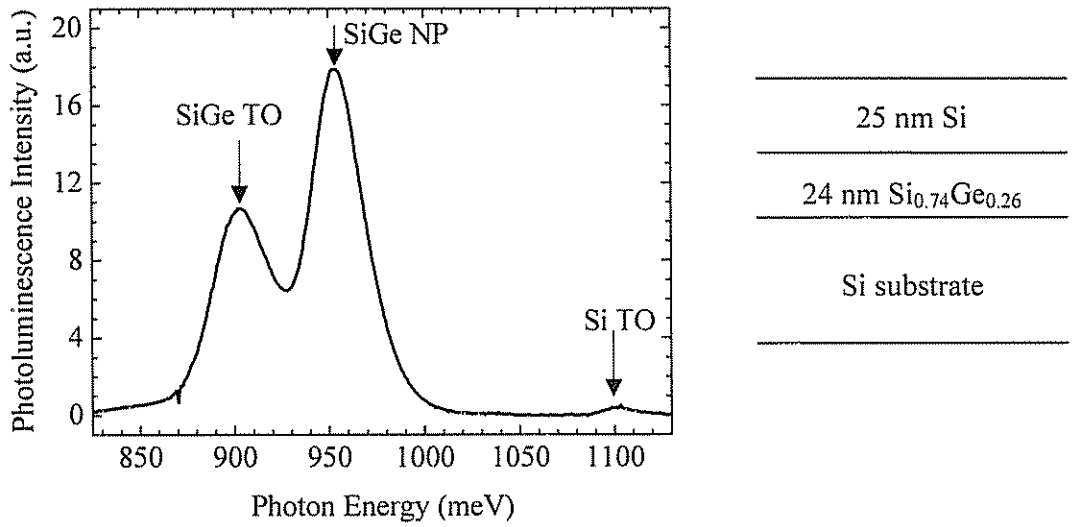


Figure 7.1: Si/SiGe epitaxy sample #51120A as-grown by Lawrence Semiconductor Research Laboratories, Inc. (Tempe, AZ) for wafer bonding: (a) photoluminescence spectrum measured using a 514-nm Argon ion laser at 77 K with typical pump power of 0.8 W and spot size of 2 mm and (b) cross-section determined by SIMS.

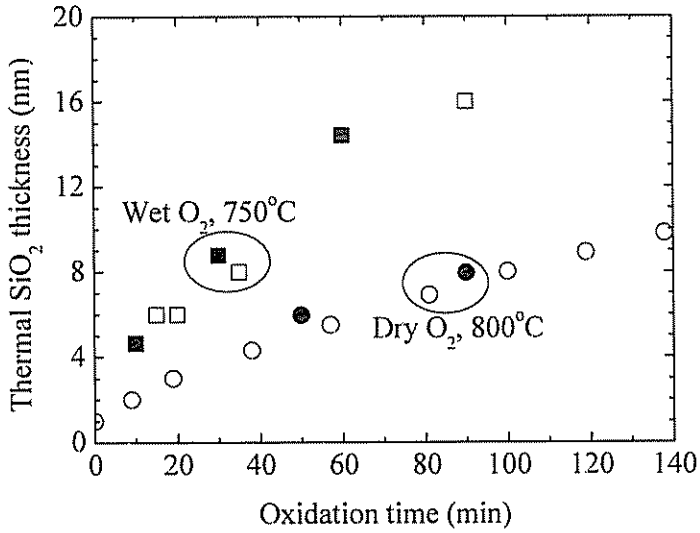


Figure 7.2: Thickness of SiO_2 thermally grown on a (001) silicon surface under two different conditions: wet oxidation at 750°C; and dry oxidation at 800°C. The open symbols indicate data from Refs. [28] (Wet O_2) and [170] (Dry O_2). The solid symbols indicate SiO_2 growths done for this work.

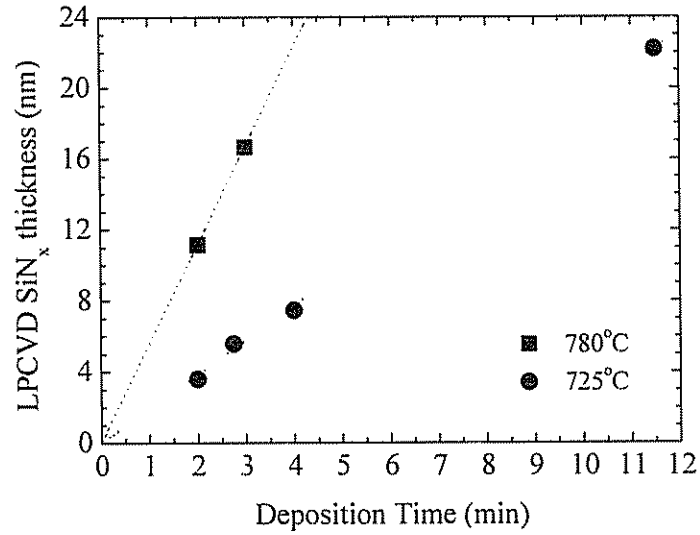


Figure 7.3: Thickness of silicon nitride vs low pressure chemical vapor deposition (LPCVD) time at 300mT for two different deposition temperatures. Note that the listed time is the total deposition time, including the one-minute "deposition-prep" step which is part of the standard recipe. The average refractive indices of the films measured by ellipsometry at 632.8nm are 2.06 for the 780°C depositions and 2.27 for the 725°C depositions. Stoichiometric Si_3N_4 has an index of 1.97 at this wavelength [22].

time for two different deposition temperatures at a pressure of 300mT. The 725°C process is much better controlled for thin layers. For selected FET samples used in this chapter, a SiN_x layer was deposited at 725°C, 300 mT for 2.75 min for a target thickness of 5.0 nm. Ellipsometry was used to measure a resulting SiN_x thickness of 5.6 nm and index of 2.36.

By wafer bonding and Smart-Cut™ the SiGe/Si layers (plus barrier layers, if present) are transferred to a silicon handle wafer covered with borophosphorosilicate glass (BPSG) and the residual silicon handle wafer layer is removed by a KOH wet etch as described in Ch. 3. The SiGe/Si bilayer is patterned into islands as shown in Fig. 7.4a. The four samples used in this chapter are shown in Fig. 7.5, and consist of: (a) a control SOI wafer from SOITEC (S.O.I.TEC Silicon On Insulator Technologies, Bernin, France), (b) a SiGe/Si/BPSG stack similar to that used in Ch. 5; (c) a SiGe/Si/SiO_2/BPSG stack; and (d) a SiGe/Si/SiO_2/SiN_x/BPSG stack. The latter two samples will be used in Sec. 7.2.3 to investigate the back Si/BPSG interface. The samples with SiO_2 and SiO_2/SiN_x caps require the bonding procedure to be adjusted slightly, because the bonding surface has changed from SiO_2(BPSG)-Si to SiO_2(BPSG)-SiO_2 or SiO_2(BPSG)-SiN_x, which exhibit a lower surface energy [119]. As described in Sec. 3.2.2, the length of the second plasma and wet etch steps are accordingly reduced to less than one minute each to create a stronger bond.

After layer transfer and island patterning, the samples are annealed at high temperature. The BPSG softens and the SiGe relaxes to become less compressively strained, stretching the silicon so it becomes tensile as depicted in Fig. 7.4b. As described in Ch. 3-5, if the island is square, expansion occurs symmetrically in both in-plane directions, resulting in biaxial strain. Lateral expansion occurs on a time-scale proportional to the square of island edge length, so small islands quickly reach stress balance, while large islands maintain initial strain. Thus, large and small square islands can be used to fabricate unstrained and biaxially-tensile strained silicon films, respectively, as shown in Fig. 7.6a and b. If a rectangular island is used, the long island direction has zero silicon strain while the short direction is tensile, with more tension than the biaxial case due to the Poisson effect, yielding uniaxially-tensile strained silicon. Using three different island geometries as shown in Fig. 7.6a-c, unstrained, biaxial-strained, and uniaxial-strained silicon are achieved side-by-side on the same sample. The

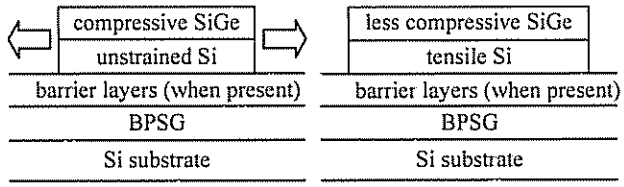


Figure 7.4: Schematic cross-sections of: (a) typical strained SiGe/relaxed Si bilayer after layer transfer and island patterning. Arrows indicate lateral expansion; (b) partially-relaxed SiGe/tensile Si bilayer after lateral expansion.

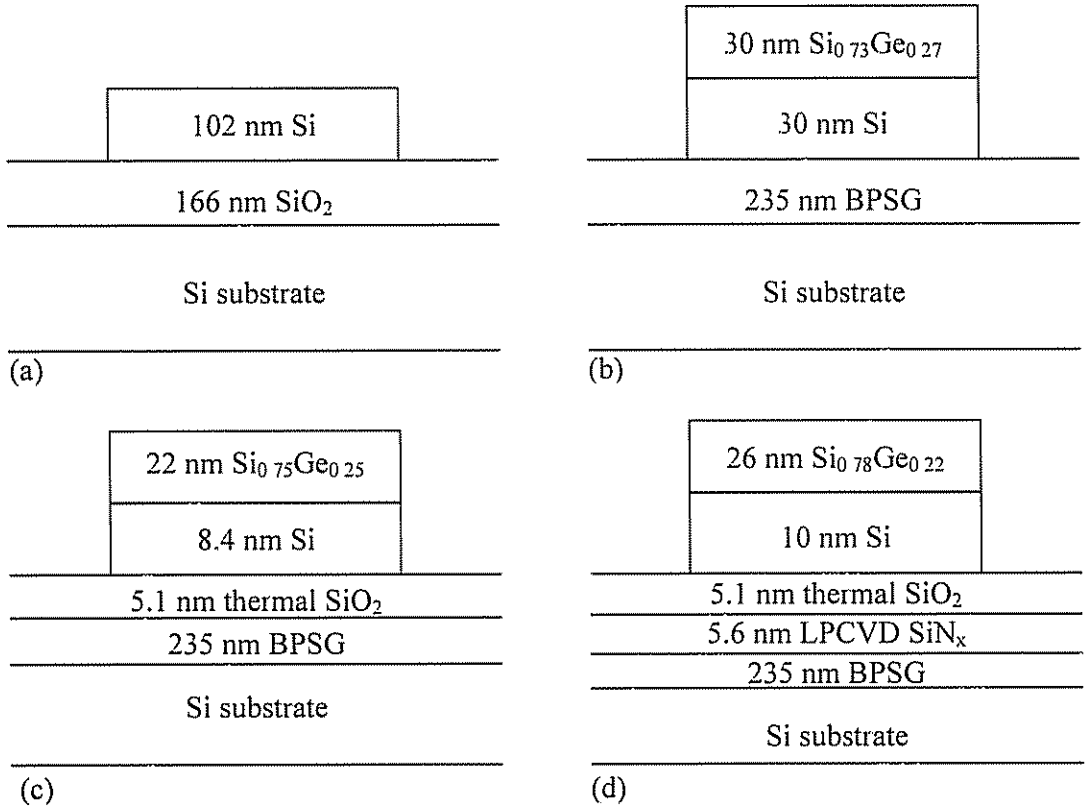


Figure 7.5: Cross-sectional schematics (not to scale) of the four samples used in this chapter to make devices: (a) an SOI wafer from SOITEC; (b) a SiGe/Si/BPSG bonded sample; (c) a SiGe/Si/SiO_2/BPSG bonded sample; and (d) a SiGe/Si/SiO_2/SiN_x/BPSG bonded sample. For (a) the layer thicknesses are taken from the manufacturer's specifications. For (b)-(d), the SiGe and Si epi layer thicknesses and Ge contents were determined by SIMS, while the SiO_2, SiN_x, and BPSG thicknesses were determined by ellipsometry or reflectometry.

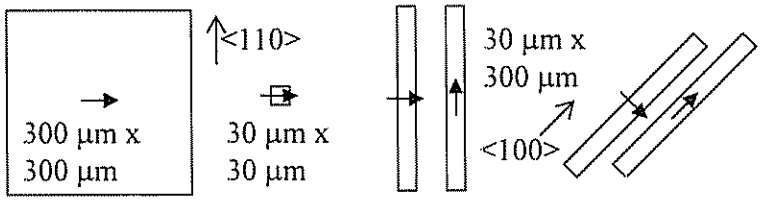


Figure 7.6: Schematic of islands used to generate strain in silicon: (a) zero strain; (b) biaxial strain; and uniaxial strain (c, d), aligned to <110>. Similar islands can be patterned rotated by 45° so strain is aligned to <100> as shown in (e) and (f). Solid arrows indicate carrier transport parallel (c, e) or perpendicular (d, f) to the uniaxial strain. As shown in Sec. 4.3, the strain is uniform over the majority of the island area, here 100's of μm^2.

channel and strain orientation relative to the crystal-direction can be varied by rotating patterns on the transistor and island masks. Namely, strain in the <100> and <110> crystal directions are examined with uniaxial strain either parallel or perpendicular to the charge carrier transport in the channel, as drawn schematically in Fig. 7.6c-f.

The island sizes shown in Fig. 7.6 are chosen to achieve the desired strains. For rectangular islands with aspect ratios greater than four, there exists an annealing process window for uniaxial Si strain (see Figs. 4.5 and 4.9, and the accompanying discussion). Here, an aspect ratio of 10 is chosen to ensure fully-uniaxial silicon strain. The predicted strain vs anneal time is shown in Fig. 7.7 for the three island geometries. After a moderate anneal of 45 min at 800°C in N_2, the large square islands (300 μm x 300 μm) should have zero strain, while the small square islands (30 μm x 30 μm) are predicted to have biaxial tensile strain and rectangular islands (30 μm x 300 μm) will be in uniaxial silicon tension. These predicted strain levels are confirmed by micro-Raman spectroscopy on all samples; typical data are shown in Fig. 7.8.

After the lateral expansion anneal to generate silicon tension, the SiGe layer is removed by a selective wet etch in 1:2:3 HF (6% buffered): H_2O_2 30%: CH_3COOH (99.8% Acetic Acid). This etchant has a selectivity of ~35 for SiGe vs Si [161]. The solution was allowed to sit for at least one week before use in order to stabilize the etch rate at > 1nm / sec [161]. The resulting strained-silicon layers are very thin, < 10 nm, for the samples shown in Fig. 7.5c and d. Such a thin channel layer could cause quantum confinement effects to dominate the transistor action, as well as causing difficulties doping the source/drain by ion implantation and making source/drain electrical contacts. Thus the strained-silicon layers need to be thickened before transistors are made.

A rapid thermal chemical vapor deposition (RTCVD) tool is used to epitaxially grow more strained silicon on samples 7.5c and d to achieve a more reasonable silicon thickness for FETs (the other samples are not subjected to silicon regrowth). First, the samples are cleaned in Pirahna etchant (~1:1 H_2SO_4: H_2O_2) for 5 minutes to getter organic contaminants, then etched in 1:100 HF (49%): D.I. H_2O to make the silicon surface hydrophobic and immediately loaded into the RTCVD chamber. The silicon regrowth process is run on multiple 1-cm x 1-cm samples at once to expedite the work, using a specially designed sample holder pictured in Fig. 7.9. The samples are subjected

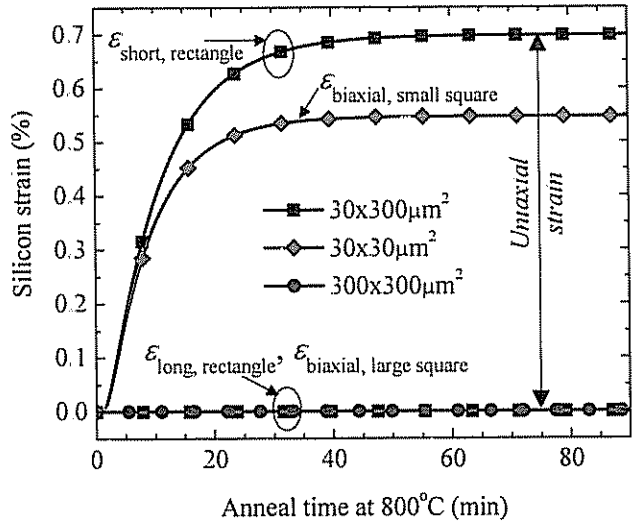


Figure 7.7: Predicted silicon strain vs anneal time at 800°C for 25-nm silicon on 30-nm $Si_{0.7}Ge_{0.3}$ on 235-nm BPSG, for various island sizes aligned to <100>. Strain is calculated from the lateral expansion model of Ch. 5, as in Fig. 5.8. The small square island quickly relaxes to biaxial strain, while the rectangular island reaches a state of uniaxial strain, and the large square island maintains its initial unstrained state. Symbols are placed every 1000 points to distinguish the different traces.

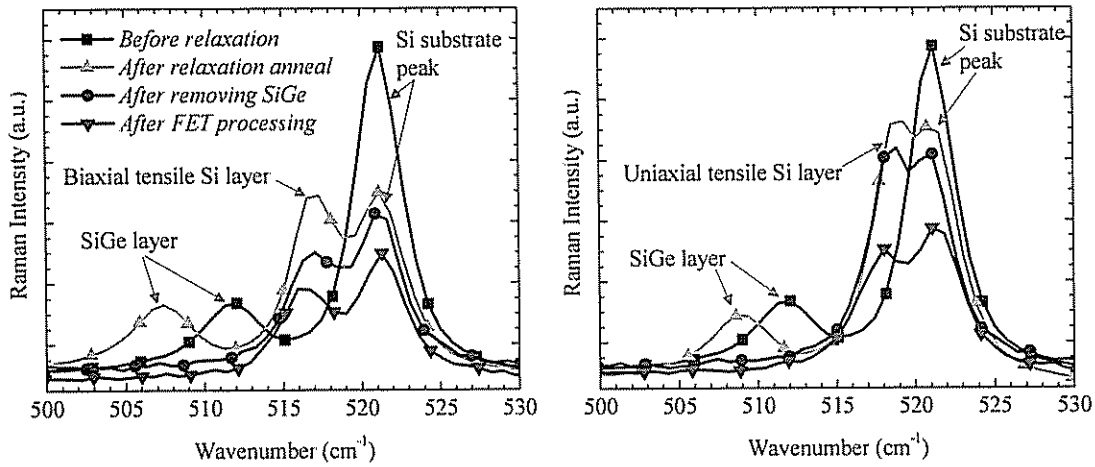


Figure 7.8: Raman spectrum of (a) biaxially- and (b) uniaxially-strained islands at various stages of FET processing, for the structure of Fig. 7.5b with no barrier layer. Measured by micro-Raman spectroscopy at 514 nm with ~3-μm laser spot size. Measurement error is $\pm 0.5 cm^{-1}$. Note that the absolute value of intensity is arbitrary. Symbols are used to distinguish the data traces.

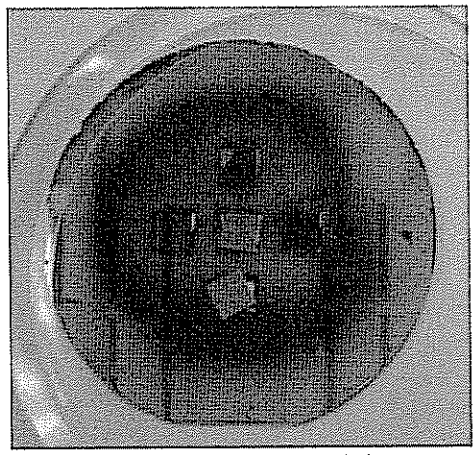


Figure 7.9: Picture of the sample holder for epitaxial regrowth of strained silicon and polysilicon deposition by rapid thermal chemical vapor deposition (RTCVD). The sample holder is made from a 100-mm diameter Si wafer with five square holes of ~1 cm x 1cm etched by TMAH in a two-step process to create ledges for the samples. The five small square samples rest on the ledges over the holes, so they are exposed directly to the lamps used for heating, which are positioned under the sample holder when it is loaded in the growth chamber. The vibrant colors on the sample holder are due to poly-silicon regrowth on an underlying oxide layer (which used as an etch mask to make the sample holes) during multiple deposition runs.

to a cleaning step at 25% lamp power (~800°C) for 2 min with H_2 flowing at 3 slpm (standard liters per minute) at a pressure of 10 Torr. This cleaning process has been shown to effectively remove contaminants and give a clean interface, indistinguishable from a continuously grown layer [171]. The strained-silicon layer is then thickened using 26 sccm (standard cm^3 per minute) dichlorosilane (DCS) in 3 slpm H_2 at 700°C at 6 Torr. The temperature is monitored by measuring the optical transmission at 1.3 and 1.55 μm through the center small sample (see Refs. [172-174] and App. E). A typical run sequence is provided in App. D, and a plot of temperature vs time for one run is shown in Fig. 7.10. The silicon growth rate for this process on 100-mm silicon wafers is 2-2.5 nm/min, so 42-53 nm of regrown silicon is expected. However, for small samples the sample temperature is generally lower than that measured due to laser beam scattering around the edges of the small samples as they sit in the sample holder. Some of the scattered light reaches the detector and falsely raises the measured transmission, causing the control software to believe the wafer is warmer than it actually is. (See App. E for details on the temperature control system.) For the four FET samples (Fig. 7.5d type) processed in the run shown in Fig. 7.10, the average silicon thickness measured by reflectometry increased from 10.0 to 36.8 nm, a change of 26.8 nm. For the samples shown in Fig. 7.5c, the average thickness after regrowth was 44.1 nm. The samples of Fig. 7.5b, which did not require regrowth, had an average silicon thickness of 27.3 nm. For all samples, the strained-silicon channel layers are now thick enough to avoid quantum confinement effects and yet thin enough to enable full depletion, as will be shown below.

During the regrowth process, it is possible that the silicon strain may relax, since the SiGe layer which provided the stress balance has been removed. In particular, the ~800°C cleaning step is of concern. To examine the effects of the regrowth process on strained-silicon films, two test samples with the cross-section shown in Fig. 7.11b were patterned with square islands of various sizes. The samples were annealed to achieve SiGe/Si stress balance. On one sample, the SiGe layer was removed by wet-etch and the silicon layer was regrown using the RTCVD process described above. The silicon strain was then measured on both samples, and is plotted in Fig. 7.11a. For islands with edge lengths < 30 μm, the regrowth process allows at least part of the silicon tensile strain to relax toward the zero strain state. The smallest islands, with L=5 μm, are nearly fully

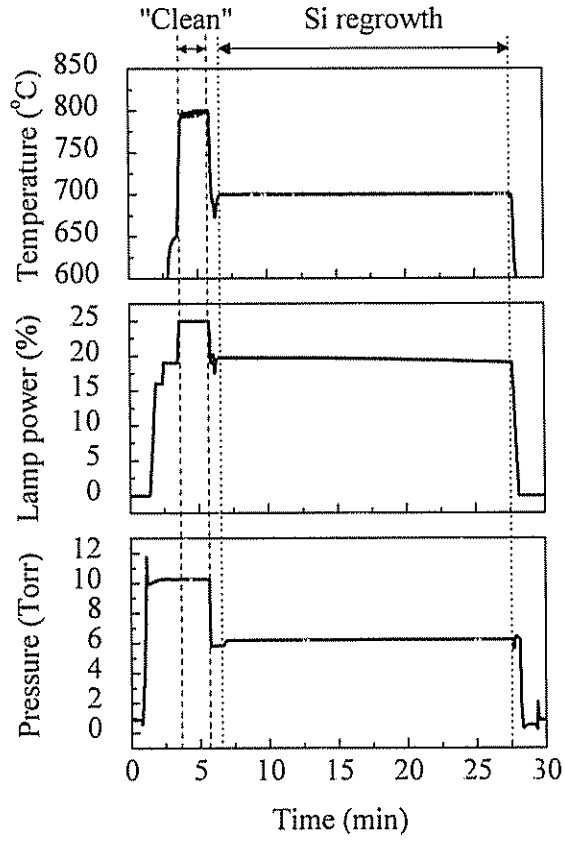
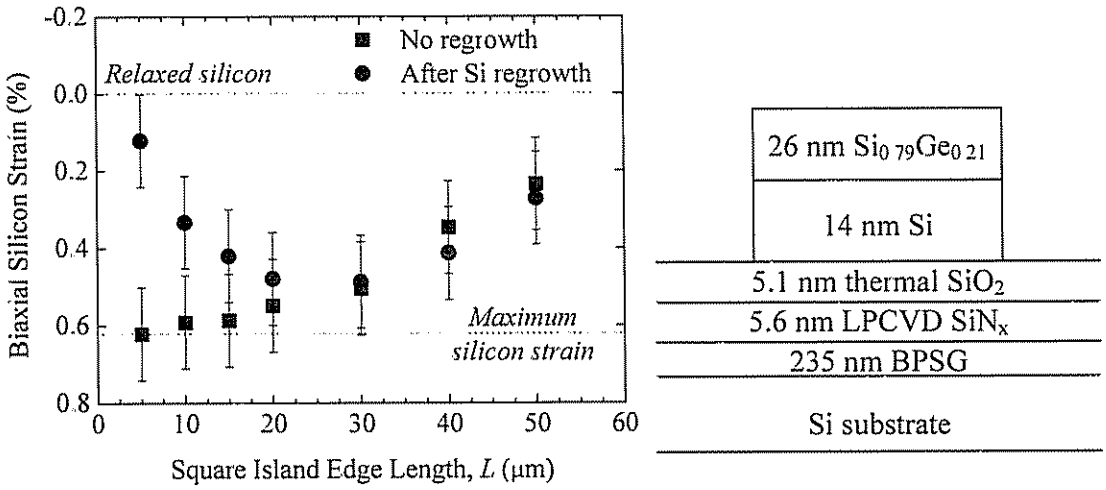


Figure 7.10: RTCVD process variables vs process time for run #3844. The process temperature measured by 1.55-μm laser transmission, lamp power, and pressure are plotted. The 21-min silicon regrowth step is indicated at the top, as is the 2-min high-temperature, high-pressure cleaning step. This run was for silicon regrowth on the samples shown in Fig. 7.5d.



(a) (b)

Figure 7.11: (a) Silicon strain before and after silicon regrowth vs square island edge length, as measured by Raman spectroscopy at the island center. The sample, shown in (b), was first annealed for 45 min at 800°C to achieve stress balance. The SiGe layer was then removed before the regrowth process, which was identical to that portrayed in Fig. 7.10. Islands < 30 μm wide relax toward a zero strain state during regrowth while islands 30 μm and larger maintain their stress-balance strain levels.

relaxed after regrowth. However, for islands 30 μm or larger (the size used for the FETs), the full stress-balance strain is maintained after regrowth. So, the regrowth process is an effective method for increasing the thickness of the strained-silicon layer without changing its strain, for islands with dimensions 30 μm or larger.

At this point, on the three SiGe/Si samples (Fig. 7.5b-d) the silicon islands were patterned with a second mask to trim off the island edge, in order to avoid any edge states (*i.e.*, defects that act as electron or hole traps) which may have been introduced by the stress balance or regrowth processes. On the SOI control sample (Fig. 7.5a) the same mask was used to pattern silicon islands for FETs. Islands are used for all four FET samples in order to isolate different devices on the same sample, and to ensure consistency of the device structure across the various samples. Both this step and the prior SiGe/Si dry etch are performed in a Plasmatherm 720 SLR using a 40-sec (or less) etch with 20 sccm O_2 and 60 sccm SF_6 at 100mT and 100W, preceded by a brief (1-minute) oxygen plasma ash with 40 sccm O_2 at 200mT and 35W power.

7.1.2 FET Process Flow

The fabrication flow for FETs is shown in Fig. 7.12. Above the dotted line are the strained silicon preparation steps described above in Sec. 7.1.1, which vary depending on the sample. Below the dotted line are the common steps for n-channel and p-channel MOSFET fabrication. This section describes the FET processes in detail.

First, the gate stack must be formed. In order to limit the thermal budget, the SiO_2 gate dielectric is deposited by low pressure chemical vapor deposition (LPCVD) using TEOS (tetraethyl-orthosilicate, $Si(OC_2H_5)_4$). TEOS can be used at temperatures of ~550-750°C to deposit high-quality silicon dioxide layers that exhibit good conformality [16]. Three different deposition temperature/pressure conditions were investigated for use in these devices. The results are shown in Table 7.1 and Fig. 7.13. All three deposition conditions exhibit low leakage currents, good indices of refraction, and reasonable deposition rates. Examining the capacitance-voltage curves in Fig. 7.13a, of the three conditions tested, the SiO_2 layer deposited at 575°C at 300mT exhibits the smallest flat-band voltage and best C-V shape. Thus, for the FET devices, after cleaning in Pirahna etchant (~1:1 H_2SO_4: H_2O_2) for 15 minutes, followed by a 1:100 HF (49%): D.I. H_2O

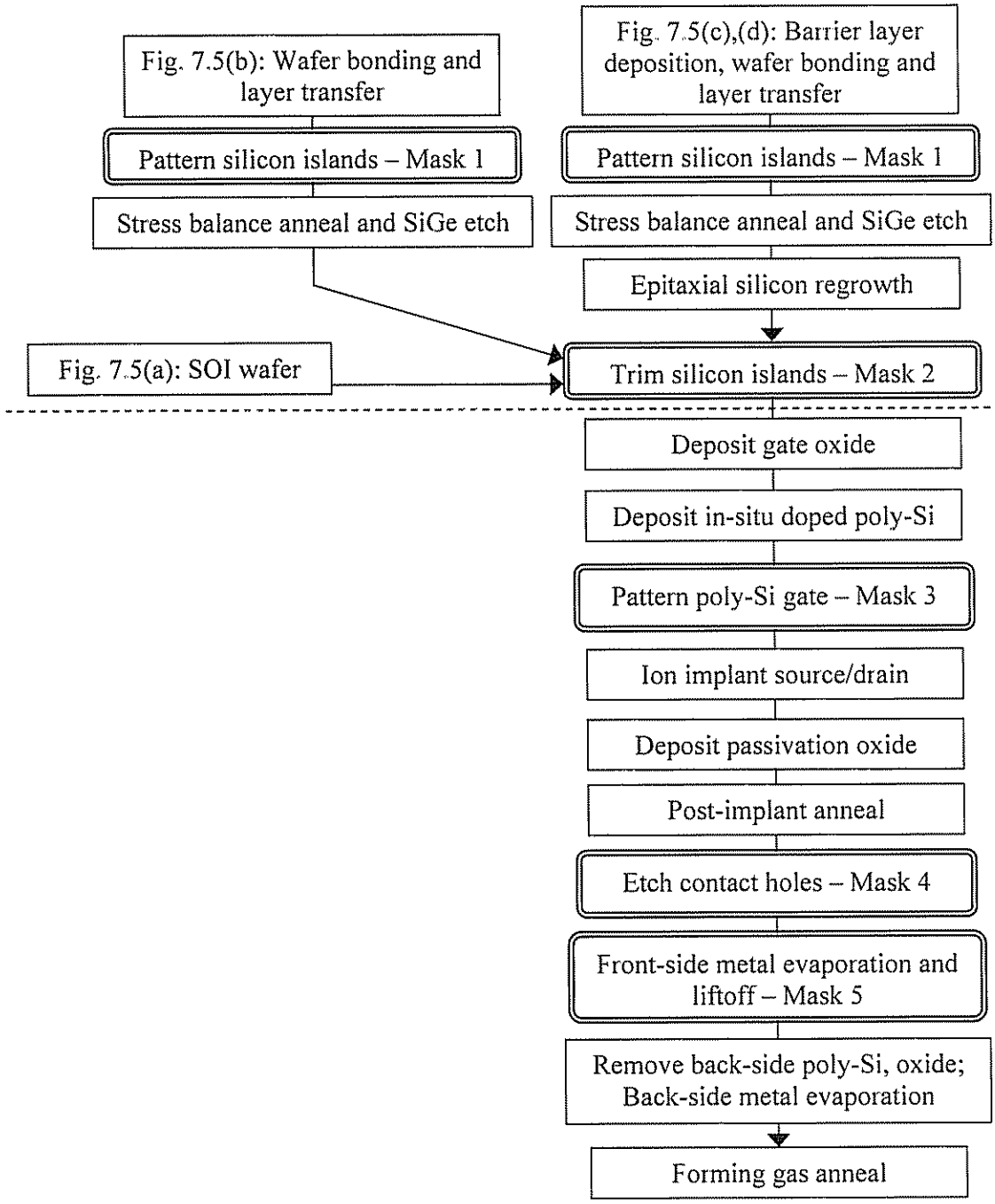
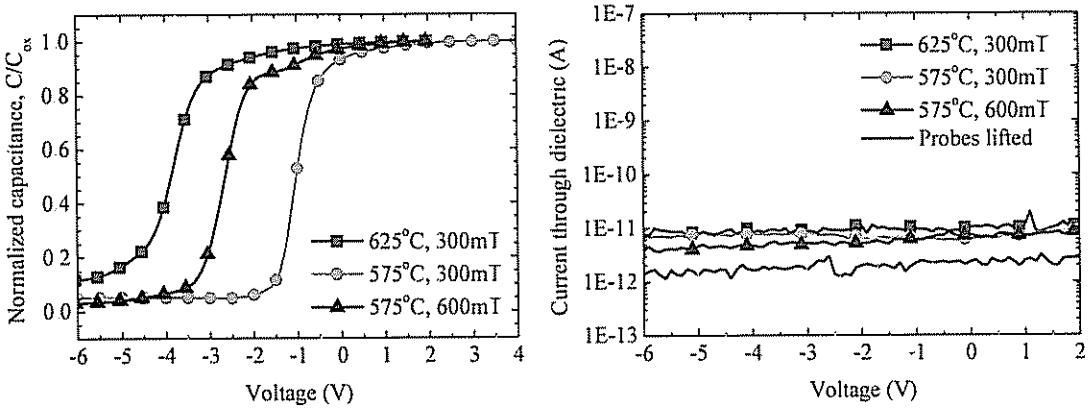


Figure 7.12: FET process flow for the four FET samples shown in Fig. 7.5. The blanket processes are shown in square boxes while the mask processes are shown in rounded boxes with double line borders. The dashed line separates the strained silicon preparation described in Sec. 7.1.1, which vary depending on the sample, and the common FET fabrication processes described in Sec. 7.1.2.

Temperature	625°C	575°C	575°C
Pressure	300 mTorr	300 mTorr	600 mTorr
Oxide thickness (1-hr dep.)	73.2 nm	25.8 nm	31.8 nm
Deposition Rate	1.22 nm/min	0.43 nm/min	0.53 nm/min
Index of refraction	1.44	1.52	1.47

Table 7.1: Characterization of TEOS oxide deposition under different conditions. The deposition time was one hour. The layer thickness and index were measured by ellipsometry at 632.8 nm. The index of refraction for stoichiometric SiO_2 at this wavelength is 1.48 [22].



(a) (b)

Figure 7.13: (a) High frequency (1 MHz) capacitance-voltage and (b) DC current-voltage characteristics for the three TEOS oxide deposition conditions as detailed in Table 7.1. The capacitors are made on n-type Si with an Al top contact. Because of the different oxide thicknesses (see Table 7.1), the capacitance for each device is normalized to its maximum accumulation capacitance, C_{ox}. The SiO_2 layer deposited at 575°C at 300mT gives the smallest flat-band voltage and best C-V shape. The leakage currents are very low in all three cases. Symbols are placed every 10 data points to distinguish the data traces.

etch, the gate oxide is deposited at 575°C at 300mT for 72 min, yielding a 33-nm gate oxide layer.

For a typical long-channel NMOS or PMOS process, the gate electrode is a poly-silicon layer. Undoped poly-silicon is usually deposited by CVD, and the source/drain ion implant and post-implant anneal are designed to provide sufficiently high and uniform poly-silicon doping to ensure low gate resistance. In order to obtain a small work-function difference across the gate stack, ϕ_{ms}, to ensure enhancement-mode devices, the poly-silicon gate is doped with the same dopant type as the source/drain during the same ion implantation step [22,175]. Since the poly-silicon layer is thick (~100nm), a high temperature (900-1000°C) and/or lengthy anneal are necessary. For our strained-silicon FET process, the thermal budget must be kept to a minimum in order to maintain the silicon strain introduced at the beginning of the process. Therefore, the poly-silicon gates are doped *in situ*, during deposition by RTCVD.

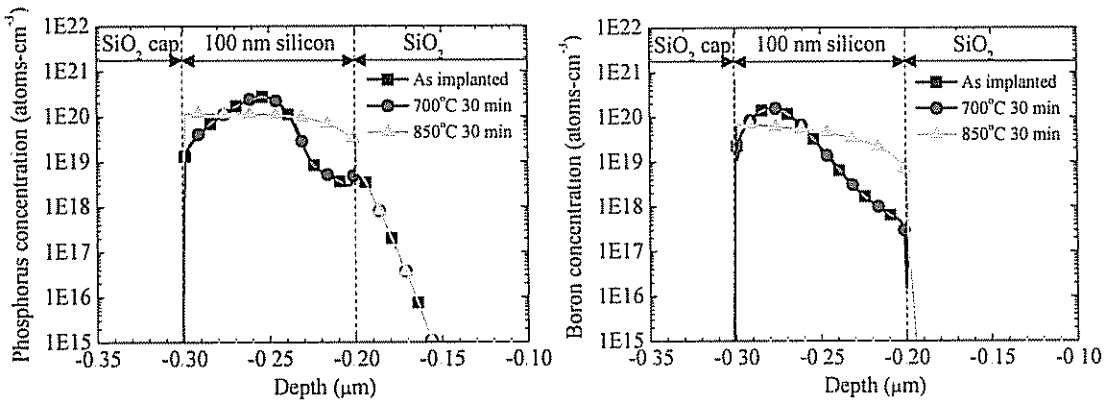
The poly-silicon is deposited using silane (SiH_4) deposition processes that have been developed previously [28,176]. The samples are first cleaned in ~1:1 H_2SO_4: H_2O_2 for 15 minutes, and then loaded into the RTCVD reactor. The samples are cleaned by a 2-min *in situ* bake at 18% lamp power (~675°C) with 3 slpm H_2 flowing with a chamber pressure of 6 Torr. After the temperature is stabilized at 700°C (~1 min), the poly-silicon deposition is begun. For n+ poly-silicon, the deposition takes place at 700°C and 6 Torr for 44 minutes using 100 sccm silane (10% SiH_4 in argon) and 450 sccm phosphine (100 ppm PH_3 in H_2) in 3 slpm H_2. For these deposition conditions, the expected phosphorus concentration is ~$2x10^{19}$ cm^{-3} [28], and the measured n+ poly-silicon thickness is ~80 nm, corresponding to ~400 Ω/□. For p+ poly-silicon, the 25-min deposition at 700°C uses 100 sccm silane (SiH_4) and 250 sccm diborane (30 ppm B_2H_6 in H_2) in 3 slpm H_2 at a chamber pressure of 6 Torr. The resulting p+ poly-silicon is expected to have a boron concentration of ~$5x10^{20}$ cm^{-3} [176], with a thickness of ~200 nm, corresponding to ~10 Ω/□. The same sample holder shown in Fig. 7.9 is used again to expedite the depositions, and a typical run command sequence is given in App. D.

The poly-silicon layers are then patterned using a reactive ion etch (RIE) using a Plasmatherm 720 SLR. The etch consists of two steps, the first of which is a 1-min oxygen plasma ash with 40 sccm O_2 at 200 mT and 35W power. The poly-Si is then

etched using 60 sccm SF_6 and 20 sccm CCl_2F_2 at 100 mT and 100 W. The etch rate is approximately 100 nm/min. An initial etch of 40 sec is performed, followed by subsequent 20 sec etches until the poly-Si pattern is fully etched, as determined by microscope inspection and reflectometry measurements.

The samples are then ion implanted with $5x10^{14}$ cm^{-2} BF_2 at 25 keV (for p-channel devices) or $1x10^{15}$ cm^{-2} $^{31}P^+$ at 25 keV (for n-channel devices) by Implant Sciences Corp. (Wakefield, MA). After the ion implant the samples are cleaned and a passivation layer of SiO_2 is deposited by plasma enhanced chemical vapor deposition (PECVD). The deposition process uses 35 sccm of SiH_4 in N_2 and 160 sccm N_2O at 800 mT and 100 W. At 250°C the SiO_2 deposition rate is ~26 nm/min. For a 13-minute deposition, a silicon dioxide thickness of 340 nm is measured by reflectometry. The samples are then annealed to activate the implanted dopants and smooth the dopant profile. The p-channel devices implanted with BF_2 are annealed at 850°C for 30 min, while the n-channel devices implanted with phosphorus are annealed at 700°C for 30 min. The temperatures and lengths of these anneals were determined to be the minimum possible to ensure low series resistance in the transistor source/drains. This point will be discussed below in Sec. 7.2.1 in greater detail. At this stage in the processing, the channel strain is maintained by the thick gate stack on top of the channel, so the relatively high temperature of the PMOS anneal is not a concern.

Simulations of the as-implanted and post-anneal boron and phosphorus concentrations vs depth are plotted in Fig. 7.14, and typical simulation code is supplied in Table 7.2. As implanted, the peak concentrations of phosphorus and boron are predicted to be $2.7x10^{20}$ and $1.6x10^{20}$ cm^{-3}, respectively. After annealing at 850°C for 30 min, the profiles have significantly flattened, and the concentrations of phosphorus and boron near the top of the simulated 100-nm silicon layer are $1.2x10^{20}$ and $6.8x10^{19}$ cm^{-3}, respectively. Such doping levels should allow sufficiently low resistance source / drains. For the thinnest silicon layers used here (27 nm, as in Fig. 7.5b), the sheet resistance for PMOS and NMOS source/drains should be approximately 550 and 220 Ω/□, respectively. The validity of these simulations was ascertained by measuring the Boron concentration in a finished FET sample by Secondary Ion Mass Spectroscopy (SIMS). The results are shown in Fig. 7.15. The measured boron level in the implanted silicon



(a) (b)

Figure 7.14: (a) Phosphorus and (b) boron concentrations vs sample depth as implanted and after two different post-implant anneals. TSUPREM4 is used to model BF_2 ($5x10^{14}$ cm^{-2}, 25 keV) and ^{31}P ($1x10^{15}$ cm^{-2}, 25 keV) ion implantation (from the left in these profiles) into a 100-nm silicon layer on 200-nm oxide (not BPSG) on a silicon support wafer. After implantation, the simulation models deposition of a 350-nm SiO_2 cap layer, followed by a 30-min anneal at various temperatures. The symbols are used to distinguish overlapping simulation traces. A typical simulation script is given in Table 7.2.

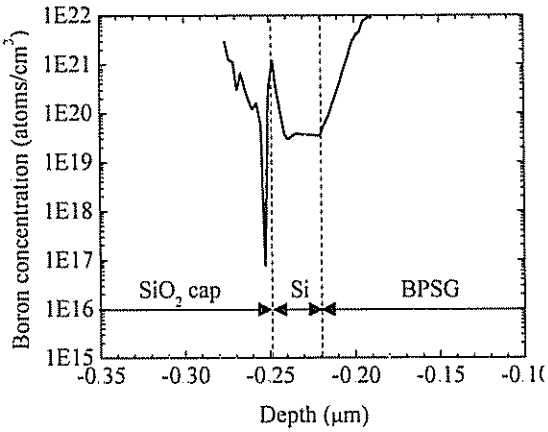


Figure 7.15: Boron concentration vs depth measured by Secondary Ion Mass Spectroscopy (SIMS). The sample originally had the structure of Fig. 7.5b, and was processed to make pFETs as described in Sec. 7.1. The region probed by SIMS was subject to a BF_2 ion implant of 25 keV, $5x10^{14}$ cm^{-2}, followed by anneals 800°C for 45 min and 850°C for 30 min during FET processing. Boron enters the ~27-nm silicon channel both from the front-side ion implant and from out-diffusion from the BPSG. The boron level in the majority of the channel is ~$4x10^{19}$ cm^{-3}, in close agreement with the simulation results shown in Fig. 7.14b.

Table 7.2 TSUPREM4 file for simulation of ion implantation and post-implant anneal

```
INITIALIZE BORON=1E15

DEPOSITION MAT=OXIDE THICKNESS=0.200 SPACES=200
DEPOSITION MAT=SILICON THICKNESS=0.100 SPACES=200

IMPLANT BF2 DOSE=5E14 ENERGY=25 TILT=7 IMPL.TAB=tr.bf2
## OR
## IMPLANT P DOSE=1E15 ENERGY=25 TILT=7

OPTION DEVICE=POSTSCRIPT PLOT.OUT=bf2_5e14_impl.ps
SELECT Z=LOG10(BORON) TITLE="Doping Profile" LABEL=LOG(CON)
PLOT.1D BOTTOM=14 TOP=22 RIGHT=0.5 LEFT=-0.5 LINE.TYP=5
SELECT Z=LOG10(PHOSPHOR)
PLOT.1D ^AXES ^CLEAR LINE.TYP=2

SELECT Z=BORON
EXTRACT OUT.FILE="bf2_5e14_imp_B.data" PREFIX="Depth vs. Boron doping"
FOREACH DEPTH (-0.31 TO 0.5 STEP 0.001)
EXTRACT X=0.0 DISTANCE=@{DEPTH} Y.EXT VAL.EXT
END
EXTRACT CLOSE

SELECT Z=PHOSPHORUS
EXTRACT OUT.FILE="bf2_5e14_imp_P.data" PREFIX="Depth vs. P doping"
FOREACH DEPTH (-0.31 TO 0.5 STEP 0.001)
EXTRACT X=0.0 DISTANCE=@{DEPTH} Y.EXT VAL.EXT
END
EXTRACT CLOSE

DEPOSITION MAT=OXIDE THICKNESS=0.350 SPACES=350
DIFFUSION TEMP=850 TIME=30 INERT
## ADJUST DIFFUSION TEMPERATURE ABOVE

OPTION DEVICE=POSTSCRIPT PLOT.OUT=bf2_5e14_ann.ps
SELECT Z=LOG10(BORON) TITLE="Doping Profile" LABEL=LOG(CON)
PLOT.1D BOTTOM=14 TOP=22 RIGHT=0.5 LEFT=-0.5 LINE.TYP=5
SELECT Z=LOG10(PHOSPHOR)
PLOT.1D ^AXES ^CLEAR LINE.TYP=2

SELECT Z=BORON
EXTRACT OUT.FILE="bf2_5e14_ann_B.data" PREFIX="Depth vs. Boron doping"
FOREACH DEPTH (-0.66 TO 0.5 STEP 0.001)
EXTRACT X=0.0 DISTANCE=@{DEPTH} Y.EXT VAL.EXT
END
EXTRACT CLOSE

SELECT Z=PHOSPHORUS
EXTRACT OUT.FILE="bf2_5e14_ann_P.data" PREFIX="Depth vs. P doping"
FOREACH DEPTH (-0.66 TO 0.5 STEP 0.001)
EXTRACT X=0.0 DISTANCE=@{DEPTH} Y.EXT VAL.EXT
END
EXTRACT CLOSE
```

source/drain region is ~$4x10^{19}$ cm^{-3}, in good agreement with the value of $6.8x10^{19}$ cm^{-3} predicted by simulation.

Next, the contact holes are etched using a two step etch process. The first step is an RIE in a Plasmatherm 790. A dry etch is used for the majority of the SiO_2 removal in order to avoid undercutting the narrow (2.5 μm) contact-to-gate spacing by wet etching, which was a problem during early processing runs, causing device shorts. The samples are briefly subjected to oxygen plasma (40 sccm O_2, 150 mT, 100W, 1 minute) and then the SiO_2 layer is etched using 25 sccm CF_4 and 6 sccm H_2 at 150 mT and 200W for 4 minutes and 35 seconds. The etch rate is approximately 65 nm/min, so that ~300nm of SiO_2 is etched, leaving about 75 nm of SiO_2, consisting of the remaining PECVD passivation layer plus the underlying TEOS gate oxide. Wet chemistry is used to complete the SiO_2 etching to avoid damaging the silicon source/drain by the dry (RIE) etch. The remaining silicon dioxide is then removed in the contact holes using Buffered Oxide Etch (BOE) with surfactant mixed 1:10 with D.I. H_2O for 2.5 min. The etch rate of this solution at room temperature is ~53 nm/min. The etch time is deliberately longer than required in order to ensure complete removal of the dielectric in the contact hole areas. The hydrophobicity of the silicon surface is clearly visible during the D.I. H_2O rinse, and reflectometry is used to establish that the SiO_2 layer has been fully removed in contact hole regions too small to be visible with the naked eye.

Note that the passivation oxide was intentionally deposited before the post-implant anneal. This was done in order to densify the PECVD oxide and reduce its etch rate, so as to better control the contact hole etching process. In Fig. 7.16 the etch rate of SiO_2 in 1:10 BOE: H_2O is shown for three different anneal conditions. When the oxide is not annealed, the SiO_2 etches at a rate of 107 nm/min. Films that have been annealed 30 min at 700°C etch at a slower rate of 66 nm/min. Further anneals (*i.e.*, another 30 min at 700°C) do not affect the etch rate. The exact etch rates are slightly different from those used for the FETs (53 nm/min) because the PECVD film used for the process characterization shown in Fig. 7.16 was deposited at a different temperature (335°C compared to 250°C used for the FET process).

Finally, the front-side metallization is done by thermal evaporation and liftoff. The metallization consists of 27-nm Cr topped with 230-nm Al. Because the SOI device

architecture contains, in effect, a dual-gate FET structure with the substrate acting as a back gate, it is necessary to obtain an ohmic contact to the substrate. Thus, earlier, after the post-implant anneal, the backside poly-Si was removed using the poly-Si RIE etch recipe described above while protecting the front-side of the transistors using a blanket photoresist layer. Then, the back-side TEOS oxide was removed during the contact hole etch in BOE. Now, the back-side must be metallized. Again, photoresist is spun on the front-side to protect the devices and a diamond scribe is used to roughen the back substrate surface to improve the electrical contact. Aluminum (~100nm) is then evaporated onto the back-side of the sample substrates. The protective front-side photoresist is removed by a solvent clean, and the samples are annealed in forming gas (H_2:N_2=5:95) at ~350°C for 10 min. The impact of the forming gas anneal will be discussed below. A completed NMOSFET transistor is shown in Fig. 7.17a, and the corresponding device layout shown in Fig. 7.17b.

After device fabrication, one of the samples is deconstructed in order to measure the final silicon strain in the channels of actual transistors by etching off the Al/Cr metallization (two wet-etches), the PECVD SiO_2 layer (using photoresist masking to expose only the gate areas, then wet etch), and the gate poly-silicon (dry etch, using the photoresist mask above) in order to probe the channel areas of previously working devices by Raman spectroscopy. In order to examine the worst-case scenario, a sample with the thinnest silicon layer (Fig. 7.5b) and the highest thermal budget (p-channel devices) is chosen. The results are shown in Fig. 7.8. The strained silicon peak positions have not shifted as a result of the FET fabrication. Clearly, the biaxial and uniaxial silicon strains introduced by stress balance are still fully present at the end of the FET processing.

7.2 Bonded SOI Transistor Characteristics

Transistors on thin silicon layers such as silicon-on-insulator (SOI) substrates differ in several significant ways from MOSFETs fabricated on bulk silicon wafers. In this work, the SOI substrates are fabricated using a wafer bonding procedure, which adds further complications. In this section, three particular issues that affect bonded SOI

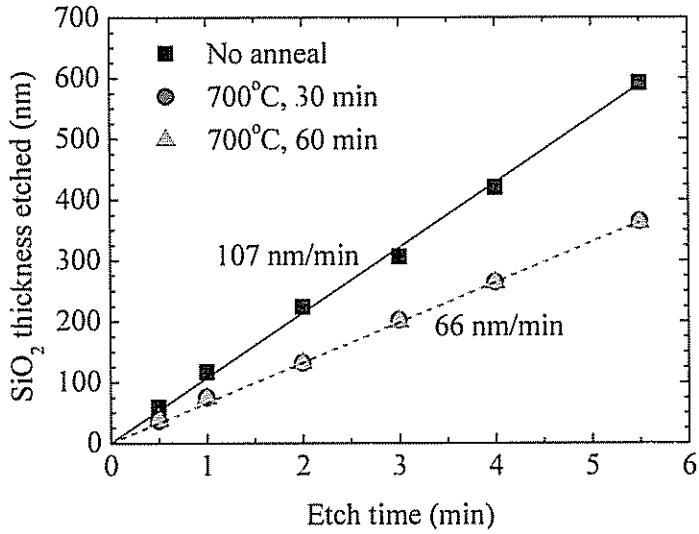
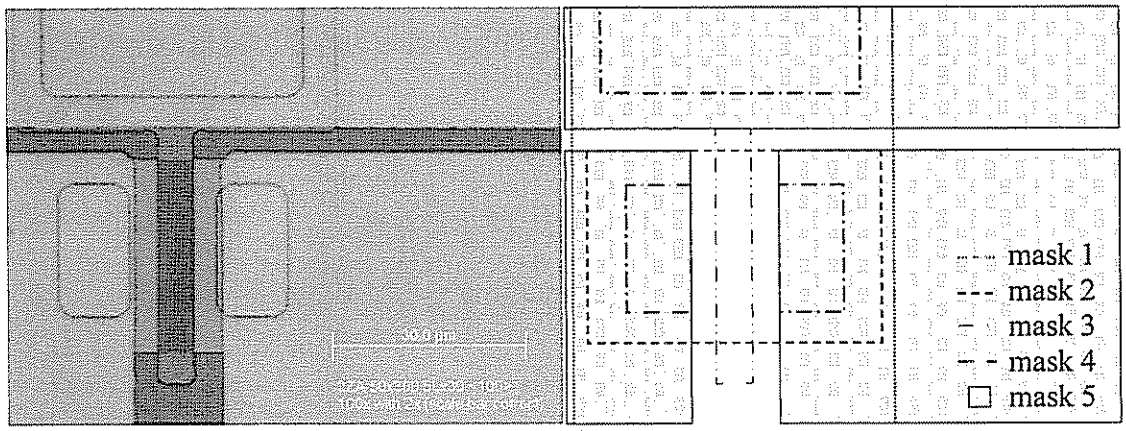


Figure 7.16: Thickness of SiO_2 etched vs etch time after three different anneals. The SiO_2 was deposited by PECVD at 335°C. The etchant is 1:10 BOE (buffered oxide etch) with surfactant: D.I. H_2O. Symbols indicate oxide thicknesses measured by reflectometry and lines indicate linear fits to extract etch rates, as listed.



(a) (b)

Figure 7.17: (a) Optical micrograph of a typical completed NMOSFET transistor and (b) corresponding mask layout. (See Fig. 7.12 for mask and process details.) The initial island size on mask 1 is 300 μm x 50 μm. Mask 2 then trims the island to 30 μm x 45 μm. The finished transistor has W / L=30 μm / 5 μm.

transistors will be examined: (1) obtaining ohmic, low resistance contacts to the thin silicon layer (*i.e.*, the transistor source and drain); (2) ensuring full channel depletion using the substrate as a back gate; and (3) optimizing the back silicon/BPSG interface through use of barrier layers.

7.2.1 Minimizing Source/Drain Resistance

The thin silicon layer used in these devices poses particular challenges in obtaining ohmic and low resistance contacts to the transistor source and drain. In any conductive thin film with uniform doping, the sheet resistance, R_{sheet}, of the layer is inversely proportional to the layer thickness, t, and directly proportional to its resistivity, ρ:

$$R_{sheet} = \frac{\rho}{t}. \tag{7.1}$$

The resistivity is determined by the substitutional (activated) dopant concentration, *i.e.*, by the ion implant parameters and the post-implant anneal conditions. In a bulk silicon device, the layer thickness can be considered equal to the depth of the PN junction between the source/drain and substrate. In the SOI devices presented here, the source/drain thickness is simply the silicon layer thickness – a much smaller value. Thus, the sheet resistance of these devices is much higher than desired. This can be overcome by selectively increasing the source/drain thickness, *i.e.*, by creating a raised source/drain [177]. However this requires that an extra epitaxial growth step be added to the process flow. Therefore, in this work the source/drain resistance will be reduced as much as possible within the given process flow.

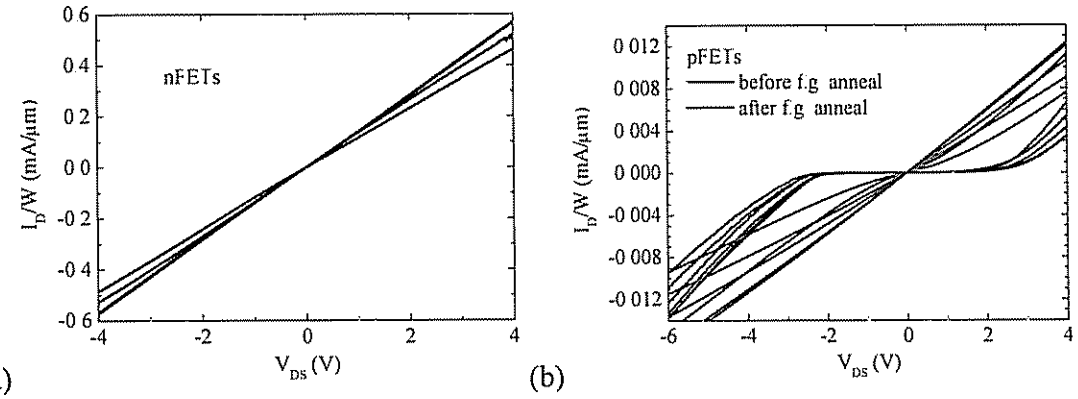
Initial devices were fabricated with top-side metallization of aluminum only. The source/drain silicon layer resistance was measured on NMOS and PMOS samples, which were both subject to a post-implant anneal of 700°C for 30 min. The test structures consist of FET devices with no gate stack (so that the entire channel layer is ion implanted), having W=15, 30 or 45 μm, and a source/drain spacing of 15 μm. The resulting current-voltage curves are shown in Fig. 7.18. The nFET test devices, which were not annealed in forming gas, show an average resistivity of 1.4×10^{-3} Ω-cm, which corresponds to a P doping level of ~5×10^{19}. This agrees quite well with the ion implant

simulation result shown in Fig. 7.14. For a 27-nm film, the corresponding sheet resistance is 520 Ω/□.

The BF_2 implanted devices tell a different story. As shown in Fig. 7.18b, before the forming gas anneal the test structure resistance is non-linear. The aluminum contact to the p-type layer is non-ohmic. After a forming gas anneal of 10 min at 400°C, the contact has become ohmic – the I-V curves are linear. The resistivity of the film before and after the forming gas anneal is 4.8×10^{-2} and 7.0×10^{-2} Ω-cm, respectively, where the resistivity value is extracted from the portion of the curve past breakdown for unannealed traces. The p-type epitaxial layer resistance is more than an order of magnitude higher than the n-type resistance, yielding an unacceptably high sheet resistance of 17,800 and 25,900 Ω/□ before and after the anneal, respectively. This must be reduced in order to ensure that the channel resistance of PMOSFETs can be effectively measured. Moreover, the current-voltage traces taken after the forming gas anneal, shown in Fig. 7.18b, have a wide degree of scatter, which is undesirable.

In Fig 7.19, pictures of the resistance test structures measured above are shown. The nFET sample devices which have not been annealed in forming gas, shown in Fig. 7.19a, look as expected. However the pFET devices, which were annealed in forming gas, shown in Fig. 7.19b, show a problem: the aluminum has merged with the thin (~27nm) silicon layer on the rightmost structure, entering the region in between the two contacts (where the channel would be in an FET device.) This occurs because when silicon and aluminum are in contact during a forming gas anneal, the silicon will dissolve in the aluminum to a concentration of about 0.3% at 400°C [16]. In bulk silicon this effect can cause metal spiking through the source/drain-to-substrate PN junction, as the dissolved silicon quickly diffuses along the Al grain boundaries away from the contact, allowing Al to flow into the voids left behind. In SOI devices, we hypothesize that the aluminum supply is effectively limitless compared to the silicon film (much thicker layer and larger area), and the aluminum can consume the thin silicon layer.

The effect of this aluminum diffusion on a pFET transistor on the same substrate can be seen in Fig. 7.20b, where the drain current – gate voltage characteristic of a transistor is shown. The image in Fig. 7.20a of the transistor shows aluminum diffusion under the gate region, but a small amount of the channel still seems to be silicon. The I-V



(a) (b)

Figure 7.18: Current-voltage characteristics for resistance test structures on n-channel and p-channel FET samples of the type shown in Fig. 7.5b. The traces represent measurement of different devices on the same sample. The samples were subjected to a post-implant anneal of 700°C for 30 min, and have Al top-side metallization. The nFET samples shown in (a) were not annealed in forming gas. In (b) pFET sample data is shown both before and after a 10-min forming gas anneal at 400°C.

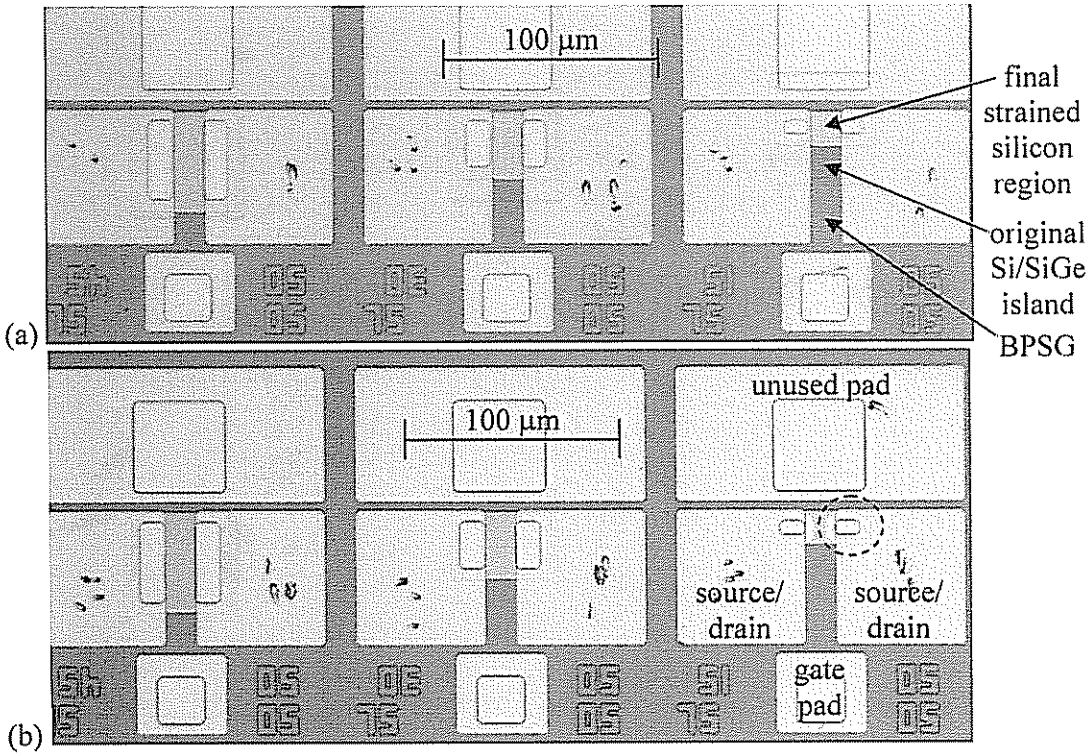


Figure 7.19: Optical micrographs of (a) NMOS and (b) PMOS resistance test structures on samples with the starting structure of Fig. 7.5b, with top-side metallization of aluminum only. The test structures consist of FETs with no poly-Si gates, so that the entire channel region is subject to ion implantation. In (a), the original Si/SiGe island and final, trimmed strained-silicon region are indicated by arrows. The PMOS sample (b) has been subjected to a forming gas anneal for 10 min at 400°C, while the NMOS sample (a) has not. The migration of Al into the thin silicon source/drain during the forming gas anneal can clearly be seen in the right-most structure in image (b) in the dotted circle.

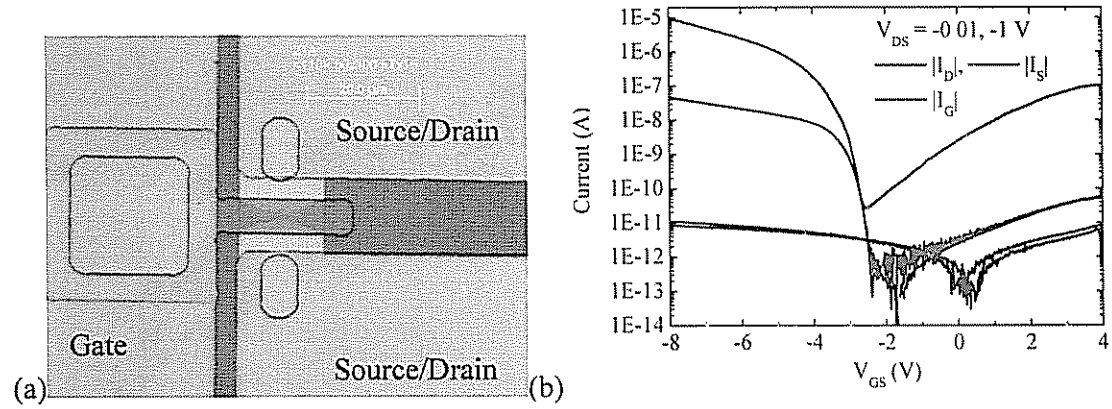


Figure 7.20: (a) Optical micrograph of a PMOS transistor made on a sample with the starting structure of Fig. 7.5b, with top-side metallization of aluminum and annealed in forming gas for 10 min at 400°C. As in Fig. 7.19b, the Al has diffused into the thin silicon channel under the gate. (b) I-V characteristics for this transistor. The Al diffusion under the gate makes it difficult to turn off the transistor.

characteristic shows that indeed, the gate can still induce channel modulation, but it is difficult to turn the channel off. At positive gate voltages, when the drain current should be minimal, instead it is observed that a current is drain-voltage dependent. The aluminum diffusion under the gate is allowing the device to act as a (poor) resistor. This aluminum diffusion problem is the cause of the scatter in the pFET sample data in Fig. 7.18b, and it must be solved.

So, there are two challenges: first, to reduce the resistivity of the p-type thin silicon source/drains; and second is to obtain an ohmic source/drain contact to p-type silicon without causing diffusion of the metal under the gate.

To increase the conductance of the source / drain regions, the post-implant anneal conditions of the p-channel MOSFET devices must be optimized. In Fig. 7.21 the sheet resistance of BF_2 doped n-Si silicon is plotted as a function of the post-implant anneal temperature. In order to avoid the aluminum diffusion problems outlined above, a bulk n-Si wafer implanted with BF_2 was used for this experiment. After the implant, islands were patterned into wafer surface to isolate the test structures from one another. The samples were coated with a passivation oxide, annealed for 30 min at the given temperature, and contacted using aluminum. As shown in Fig. 7.21, for a post-implant anneal temperature of 700°C, the sheet resistance of the p-type silicon is quite high, but as the anneal temperature increases the sheet resistance falls. When the anneal temperature is 850°C or higher, the implanted boron is fully activated and the sheet resistance reaches a minimum value of 550 Ω/□.

Now that the optimal anneal conditions have been determined, the problem of ohmic contacts can be addressed. In order to avoid diffusion of aluminum into the thin silicon epi layer, a thin layer of 30-nm chromium is thermally evaporated first, followed by a thicker 230-nm aluminum film. Both evaporations were done in the same vacuum chamber, with no break in vacuum between the two metal evaporations. The chromium acts as a diffusion barrier for short forming gas anneals, while the aluminum provides a low resistance metal film.

The resistance of test structure on pFET samples using an 850°C, 30-min post-implant anneal and Cr/Al top-side metallization is shown in Fig. 7.22. The resistance is initially non-linear, but after a 10-min forming gas anneal at 400°C, the contacts become

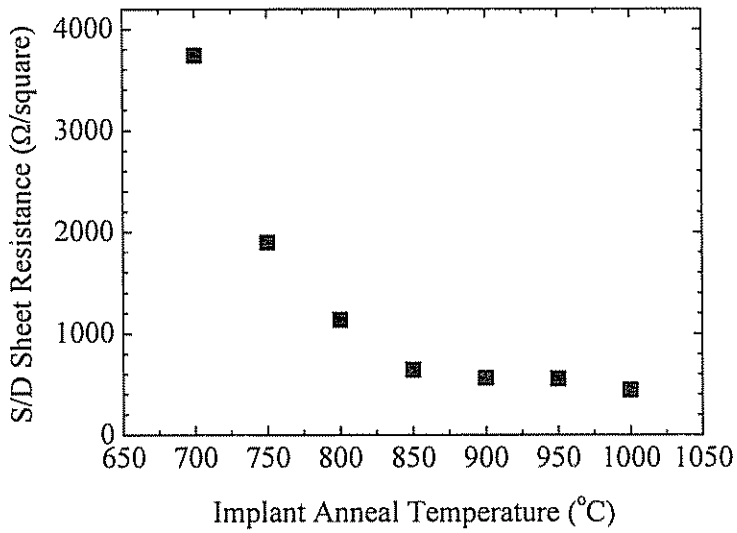


Figure 7.21: Sheet resistance of the BF_2 doped silicon source/drain vs. 30-min post-implant anneal temperature. The resistance was measured using two-terminal test structures identical to those shown Fig. 7.19b, but the starting material was a bulk n-type silicon wafer instead of a bonded thin silicon layer, to eliminate the Al diffusion problems shown in Fig 7.19b and 7.20a. Regression analysis was performed on samples with different lengths and widths. In all cases this analysis confirmed that the probe/metal contact resistance could be neglected; the measured resistance is dominated by the silicon layer resistance. For anneals at 850°C or greater, the sheet resistance reaches a minimum of 550 Ω/□.

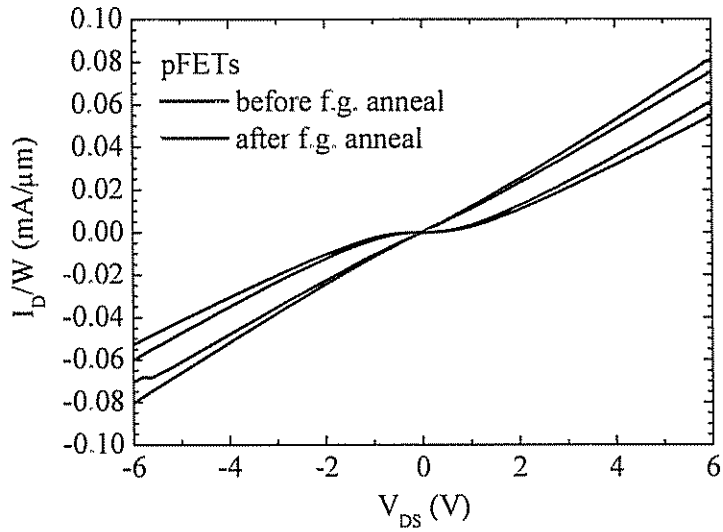


Figure 7.22: Current-voltage characteristics for resistance test structures on pFET samples of the type shown in Fig. 7.5b before and after a 10-min forming gas anneal at 400°C. The samples have Cr/Al top-side metallization and were subjected to a post-implant anneal of 850°C for 30 min.

ohmic. The average resistivity before and after the forming gas anneal (taken from the linear region of the curves) are $1.6x10^{-2}$ and $1.4x10^{-2}$ Ω-cm, respectively. The 850°C anneal temperature has significantly reduced the resistivity (to 25% of its previous value), compared to the 700°C anneal condition shown in Fig. 7.18. Note that while the forming gas anneal is still required to make the contact ohmic, it does not significantly change the epitaxial silicon layer resistance. Moreover, with the Cr/Al metallization the diffusion problem seen earlier has been eliminated, as shown in the image of a completed p-channel MOSFET transistor in Fig. 7.23.

The source / drain resistance results are summarized in Fig. 7.24 for both nFET and pFET devices, in which sheet resistance is plotted vs silicon layer thickness. From Eqn. 7.1, it is expected that the sheet resistance will scale inversely with silicon thickness. Indeed, this is true for the pFET samples, where the average resistivity for all four samples (shown by the dashed fitted curve) is $1.5x10^{-2}$ Ω-cm, in agreement with the data shown for one of the samples in Fig. 7.22. The nFET samples, in contrast, show an average sheet resistance of 410Ω/□ independent of silicon thickness. It is not clear why the sheet resistance for nFETs is independent of silicon layer thickness. This may be due to the low temperature of the post-implant anneal, which prevents phosphorus diffusion as shown by the simulation of Fig. 7.14b, or to the lack of phosphorus segregation in SiO_2 during annealing, unlike boron. In future work it might be fruitful to increase the nFET post-implant anneal temperature to allow greater phosphorus diffusion, since even 850°C was seen to cause no strain degradation in pFETs (Fig. 7.8).

While the nFET samples with Cr/Al metallization show linear resistance without a forming gas anneal, a forming gas anneal is still needed in order to reduce the electronic state density at the gate oxide/channel interface [16]. The effect of a forming gas anneal on NMOSFET drain current – gate voltage I-V characteristics is shown in Fig. 7.25 for two different samples. Before the forming gas anneal, the transistors function, but show a very high sub-threshold slope of 881 mV/dec and 1129 mV/dec for control SOI and bonded SiO_2/SiN_x barrier devices, respectively. After the forming gas anneal, the turn-on voltages remain unchanged, but the devices reach threshold much more quickly: the sub-threshold slopes are now 123 and 162 mV/dec, respectively. Clearly, the forming gas

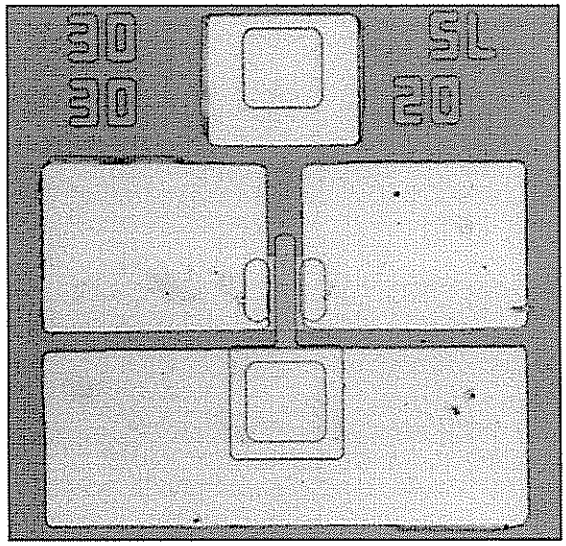


Figure 7.23: Completed PMOSFET device started on sample from Fig. 7.5b with Cr/Al metallization and a forming gas anneal. Note the contrast with Fig. 7.20, where the Al had diffused under the gate. The Cr/Al devices were subject to no such problems because the Cr acted as a diffusion barrier for the Al.

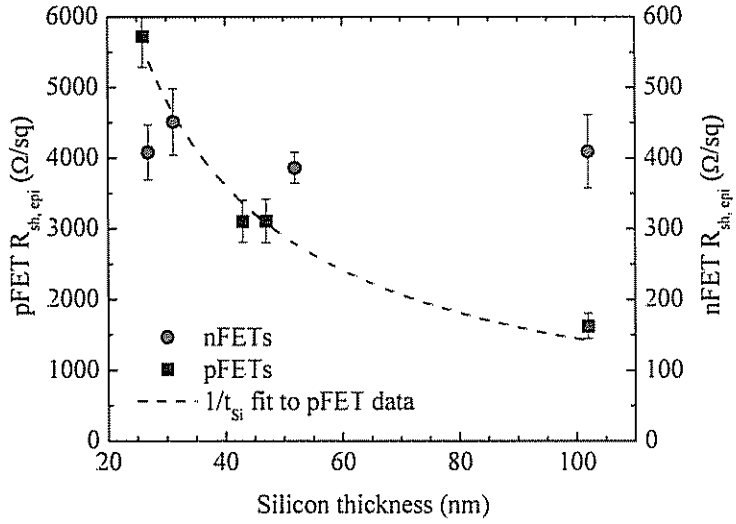


Figure 7.24: Sheet resistance of resistance test structures on n-channel and p-channel FET samples with Cr/Al top-side metallization vs silicon layer thickness. All measured I-V resistance curves were linear. The nFET samples were annealed at 700°C for 30 min after the implant, but were not annealed in forming gas after metallization. The pFET samples were annealed at 850°C for 30 min after the implant, and were annealed in forming gas 10 min at 400°C after metallization.