$$k_S = S_{eff} \cdot v_{th} \qquad [4.7]$$

where v_{th} is the thermal velocity of the oxygen molecules and S_{eff} is the effective sticking coefficient of oxygen on the growing surface. S_{eff} is bounded by zero and one ($0 \leq S_{eff} \leq 1$). For each temperature in our experiment, we can approximate the effective sticking coefficient. To do so, we assume that below 750 °C, desorption of oxygen from the wafer surface is negligible and that the thermal velocity of the oxygen is determined by the substrate temperature and follows a Mawellian distribution of velocity given by [4]:

$$v_{th} = \left(\frac{k_B T_S}{2\pi \cdot M(O)}\right)^{1/2} \qquad [4.8]$$

where M(O) is the mass of oxygen and T_S is the substrate temperature. Combining Eqns. 4.6 through 4.8, we arrive at an estimate of S_{eff}. The values for S_{eff} are listed in Table 4.1 for each growth temperature. All values for S_{eff} are on the order of 10^{-4}. This is two orders of magnitude lower than the sticking coefficient of oxygen on a clean silicon surface as determined by Hagstrum, Lander *et al.* and Ghidini *et al.* (Refs. 15,10-12 of Ch. 2)

4.6 Discussion of the Reduction of Oxygen Incorporation in CVD

We associate the reduction of the oxygen incorporation to (1) the hydrogen passivation of the silicon surface (reduced S_{eff}) and to (2) the formation of the boundary layer leading to a reduced oxygen concentration at the wafer surface. The reduction in k_S is due to the reduction of the effective sticking coefficient, which is a property of the surface reaction. We associate this decrease in surface reactivity to oxygen with the hydrogen passivation of the surface. An equally effective way to reduce the oxygen contamination at the surface of the growing film is to create a large boundary layer to reduce the mass-transfer coefficient and hence the number of oxygen molecules which can interact with the surface. We have determined that the mass transfer coefficient (h_g) and the surface reaction coefficient (k_S) are related by the ratio, B, of Eqn. 4.6 and that they are of the same order of magnitude. This implies that they are both important to our

experiments. Since their effects on the sticking are additive in nature and not multiplicative, they both have the effect of reducing the effective sticking coefficient by a factor of the order of 100. For instance, if the surface reaction were to occur infinitely fast ($k_s = \infty$) and h_g is fixed at the measured value, the incorporated oxygen concentration would increase by only a factor of approximately two. The same result occurs if the mass transfer were infinitely fast ($h_g = \infty$, which means the an infinite surface velocity and S_{eff} –> 1) and the surface reaction rate retains its measured value.

We have neglected the desorption of oxygen from the silicon surface in our model for oxygen incorporation under the assumption that we are well below the desorption temperature for SiO. The line in Figure 2.1 (the Lander and Morrison data) corresponds to the situation where the desorption rate of SiO equals the sticking rate of oxygen. Under UHV conditions, the hit rate of oxygen is governed by the kinetic theory of gases. Therefore, we can estimate the desorption rate of oxygen from the silicon surface using the data of Lander and Morrison. The oxygen flux incorporating in the layers of our experiment is approximately 5×10^{13} $cm^{-2}s^{-1}$. According to the Lander experiment, the desorption temperature to accommodate this incoming flux is approximately 850 °C. At 750 °C, the desorption flux (from the Lander experiment) is approximately 7×10^{11} $cm^{-2}s^{-1}$. Thus, we see that our assumption of negligible desorption below 750 °C is valid.

The reduction of the sticking coefficient with surface coverage is not entirely unexpected. Hydrogen passivation is expected to tie up surface bonds. Therefore, the likelihood that an impinging O_2 molecule will be chemisorbed is greatly reduced. Assuming one open site is needed for adsorption according to first order Langmuir adsorption, as shown in Fig. 4.2, the predicted reduction in S_{eff} is a factor of 200. This is because the simple thermodynamic model of Chapter 2 predicts a surface coverage of hydrogen of 99.5% at 750 °C and a background hydrogen pressure of 6 Torr. It should be noted that if oxygen can physisorb and migrate on the surface to find a site, then the improvement will not be noticed except at a very high surface coverage, as qualitatively

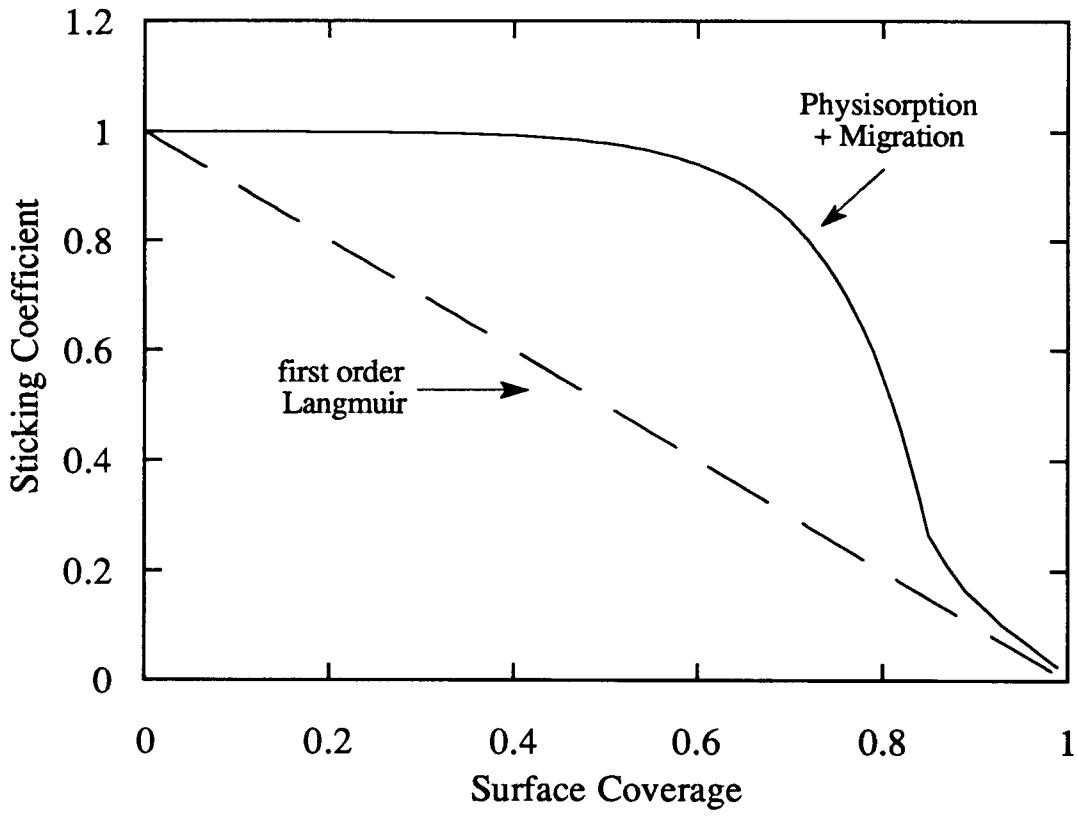


Figure 4.2. Schematic plot of the sticking coefficient of oxygen on the surface of silicon. The ideal case is that of first order Langmuir adsorption where the sticking probability drops linearly with the number of open sites. Not many molecules follow this model. Most molecules are allowed to physisorb to the surface and migrate until a site is found to chemisorb. In this situation, the sticking probability is relatively insensitive to surface coverage until most of the sites are covered. This plot is only a schematic representation for oxygen on silicon; the actual critical points are not known.

shown in Figure 4.2. The value of the oxygen sticking coefficient in the UHV clean surface case is ~ 10^{-2} and in the CVD case it is ~ 10^{-4}, a difference of a factor of ~100. This is close to the first order Langmuir prediction.

4.7 High Purity CVD Growth

Since the incorporation of oxygen in the growing silicon film is reduced by 100 due to hydrogen passivation and boundary layer effects, we can tolerate 100 times more oxygen in the gas flow than expected from the experiments performed on a clean silicon surface in UHV. This in turn means that in order to grow a silicon or silicon-germanium film below 750 °C (at a growth rate of 500 Å/min at 10 Torr with an oxygen concentration in the film of less than 10^{18} cm^{-3} (the peak solid solubility of oxygen in silicon), we can tolerate 100 ppb oxygen in the total gas stream (100 times more than calculated from the classical Lander and Morrison curve in Fig. 2.1). This is a level well within the specifications of semiconductor gas purifiers available on the market today. At 10 ppb (approximate limit of purifiers), we can grow down to rates of 50 Å/min. Although our experiments are for O_2, similar reduction in oxygen incorporation due to residual water vapor would be expected. To confirm this, we have grown many low-temperature silicon and silicon-germanium epitaxial layers in our reactor without oxygen introduction and with a load-lock to prevent contamination. Figure 4.3 shows a SIMS plot of a silicon-germanium layer grown at 625 °C (100 Å/min.) with a structure similar to that of Fig. 3.6. However, in this case, the oxygen concentration in the silicon-germanium layer has been reduced to the background resolution of SIMS. Similar levels of oxygen in silicon grown at 700 °C (30 Å/min.) with DCS have been obtained. This is the first time that such low-oxygen concentrations have been obtained in non-UHV silicon CVD epitaxial layers. This is of tremendous technical importance for manufacturing.

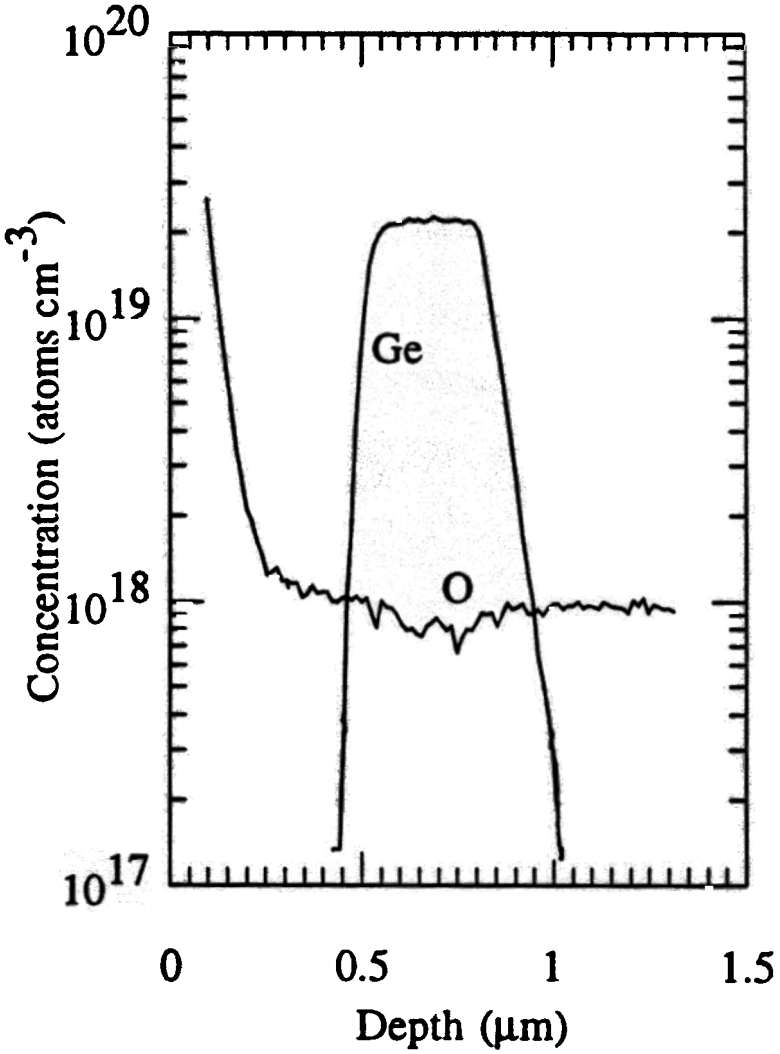


Figure 4.3. SIMS plot of silicon-germanium grown at 625 °C with little oxygen contamination. The oxygen concentration is below the detection limit of SIMS. This sample was grown after the load-lock was installed on the system. The load-locks prevents oxygen and water vapor from contaminating the chamber between depositions.

The central experimental results of this thesis on oxygen incorporation in silicon and silicon-germanium have made improvements in new devices possible. The improved properties for devices will be discussed in the next chapter.

4.6 References

1. A.S. Grove, Physics and Technology of Semiconductor Devices, Wiley, New York (1967).

2. S.W. Wolf, R.N. Tauber, Silicon Processing for the VLSI Era: Volume I - Process Technology, Lattice, Sunset Beach, CA (1986): from H. Schlichting, Boundary Layer Theory, 4th Ed., McGraw Hill, NY, (1960).

3. Perry and Chilton, Ed.,Chemical Engineers' Handbook, 5th Ed., McGraw-Hill, New York, (1973).

4 M.A. Morris, M. Bowker and D.A. King, "Kinetics of Adsorption, Desorption and Diffusion at Metal Surfaces," Comprehensive Chemical Kinetics **19**, Elsevier, Amsterdam (1984).

Chapter 5

Electronic Properties

Introduction

All semiconductor devices rely on recombination-generation processes whether the lifetimes are long, as needed in p-n diodes, or short, as required in high speed photoconductive switches. The electronic properties of the silicon and silicon-germanium strained layers were determined by studying the minority carrier lifetimes of the films. We studied both the generation and recombination lifetimes of the films by fabricating several device structures with oxygen concentrations of various levels. For quantitative measurements we studied heterojunction bipolar transistors and MOS capacitors, and for qualitative measurements of recombination lifetimes we studied a basic optoelectronic property of the silicon-germanium.

Recombination-Generation

Here we briefly discuss recombination and generation and review some of the important characteristics of semiconductors and the effects they have on carrier lifetimes. A

semiconductor in a non-equilibrium state of carrier depletion will attempt to return to equilibrium by the generation of carriers. Mechanisms for carrier generation are depicted in Figure 5.1(a). Carriers can be generated by band-to-band generation where an electron in the valence band absorbs energy (an amount $\geq E_g$) and jumps into the conduction band leaving behind a valence band hole. This process can also take place by utilizing mid-gap states. The electron in the valence band absorbs a small amount of energy and jumps to an energy level in the forbidden gap; by absorption of another small amount of energy, it is excited into the conduction band. The final product of these two mechanisms is the same: an electron in the conduction band and a hole in the valence band.

Recombination, on the other hand, is the reverse process. In a non-equilibrium situation where a surplus of carriers resides in the semiconductor, recombination occurs to drive the material back into equilibrium. Recombination methods are depicted in Figure 5.1b. Carriers can be annihilated by band-to-band recombination or through mid-gap states.

Band-to-band optical recombination and generation processes are extremely slow in silicon and germanium because of their indirect band gaps. Phonons are required in order to conserve momentum. However, these processes can be mediated by localized states in the band gap. As the number of mid-gap states in the material increases, the rate of carrier generation and recombination increases, allowing the recombination and generation processes to occur quite rapidly. These states can be formed in silicon by the incorporation of transition metals such as Fe, Au, and Cu but also by defects. We will show that the addition of large amounts of oxygen which can incorporate in silicon when grown at low temperature can form these states.

5.3 Generation Lifetime Measurements

5.3.1 Pulsed MOS capacitor / Background

A pulsed metal-oxide-semiconductor (MOS) capacitor technique was used to determine the generation lifetimes of the films by employing a Zerbst analysis [1] to extract

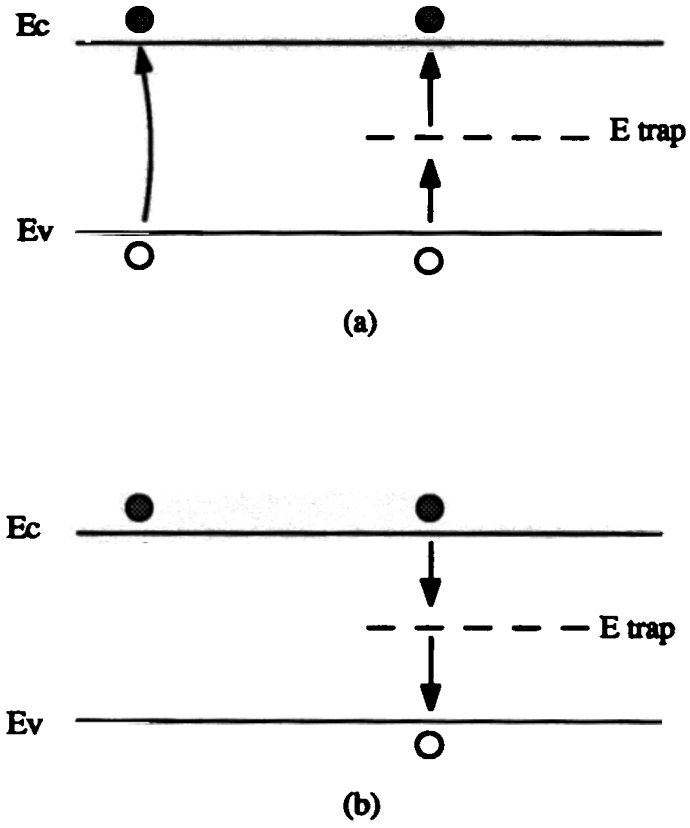


Figure 5.1. Schematic diagrams of carrier (a) generation and (b) recombination. Both processes can occur directly across the band gap or indirectly through mid-gap traps. In indirect band gap materials such as silicon and silicon-germanium, direct recombination and generation are slow and mid-gap states are needed to speed the recovery.

numerical values for generation times We probed the minority-carrier generation properties of $Si_{1-x}Ge_x$ by driving an MOS capacitor into deep depletion and monitoring the recovery of the device from the deep depleted state to the inverted state. This is seen as an increase in capacitance due to the shrinking of the depletion region in the semiconductor by the creation of minority carriers. There is a direct relationship between the rate of recovery of a capacitor from deep depletion and the minority carrier generation time. Long generation lifetimes are important for devices such as p-i-n photodiodes [2] and heterojunction bipolar transistors [3] (HBT) which require low leakage junctions under reverse bias. A more complete description of the technique follows.

The layers under study in this experiment were grown in the susceptor-free, rapid thermal chemical vapor deposition system described in Chapter 3. The substrates were four inch, p-type, <100> Cz silicon with resistivities of 1-10 Ω-cm. The chemical clean and the *in situ* hydrogen clean are also the same as described in Chapter 3.

Each structure was initiated with a 1.5 μm buffer layer followed by the active area of the device. The active region consisted of a 30 nm $Si_{0.82}Ge_{0.18}$ strained layer grown at 625 °C and a silicon cap layer of 30 nm grown at 850 °C for 30 seconds to simulate our standard heterojunction bipolar transistor growth process. All layers were doped p-type to a level of ~3 x 10^{17} cm^{-3} with boron. The oxygen concentrations in the some of films were kept below the detection limit of SIMS (~ 2 x 10^{18} cm^{-3}) while in other samples the oxygen concentrations were > 5 x 10^{19} cm^{-3}. A cross section of the device is shown in Figure 5.2. Control samples of all-silicon layers were also grown at 700 °C (similar doping and oxygen levels) for parallel fabrication and testing. Although not specifically measured in this study, transmission electron microscopy (TEM) measurements on similar structures fabricated in our laboratory have shown that the $Si_{1-x}Ge_x$ layers are fully strained with a negligible number of misfit dislocations (≥ 10 μm spacing).

The gate dielectric of the capacitors were formed by both plasma deposition of SiO_2 and thermal oxidation of silicon Strain relaxation, and hence the formation of interface

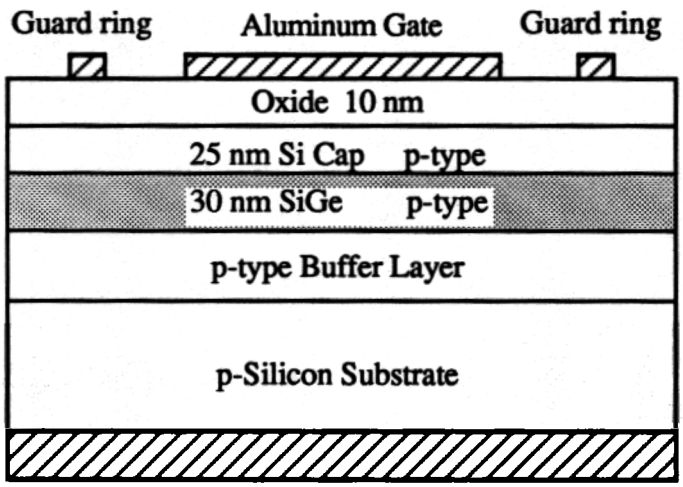


Figure 5.2. Capacitance structure used for testing the generation lifetimes of the $Si_{0.82}Ge_{0.18}$ strained layer. The capacitor is pulsed into deep depletion and monitored during recovery to inversion.

defects, in the $Si_{0.82}Ge_{0.18}$ film was avoided by using a low-temperature (400 °C) plasma deposition of silicon dioxide (10 nm) followed by a 600 °C anneal in nitrogen The nitrogen anneal served to increase the dielectric strength of the material. A thermal oxide, grown at 800 °C in dry O_2, was also used as the gate insulator on some devices.

In all devices, the oxide/semiconductor interface was formed with silicon instead of silicon-germanium. (The SiO_2/Ge interface has been observed to have poor electrical properties [4].) Since the thermal oxide consumes silicon, the cap layer of silicon in the final thermal oxide structures is estimated to be 25 nm thick as shown in Figure 5.2. The aluminum gate and guard ring were formed by thermal evaporation, followed by photolithography and etching. The guard ring surrounding the gate provides a means of limiting the active area of the device.

High frequency (1 MHz) capacitance-voltage curves of the capacitors showed well defined regions of accumulation, depletion and inversion for both the silicon and silicon-germanium buried layer capacitors. The dopings and the oxide thicknesses extracted from the curves were consistent with the values discussed earlier. Straightforward calculations show that the depletion layer in inversion contains the buried layers of silicon-germanium. Generation lifetimes were measured by applying a voltage pulse to the gate of the capacitor and monitoring the recovery of capacitance from deep depletion (Figure 5.3) as in the Zerbst [1] technique.

5.3.1.1 Theory

The Zerbst analysis consists effectively of plotting the generation rate vs. generation volume of the capacitor with the slope of the plot being related to the generation lifetime. By analyzing the change in depletion layer width with time and relating it to the device capacitance, the following (Zerbst) relationship for bulk semiconductors is found: [1]

$$\frac{d}{dt}\left(\frac{C_o}{C}\right)^2 = \frac{2n_i C_o}{\tau_g N_A C_i}\left(\frac{C_i}{C} - 1\right) \qquad [5.1]$$

where C_o, C_i, and C are the oxide capacitance, inversion capacitance, and the instantaneous

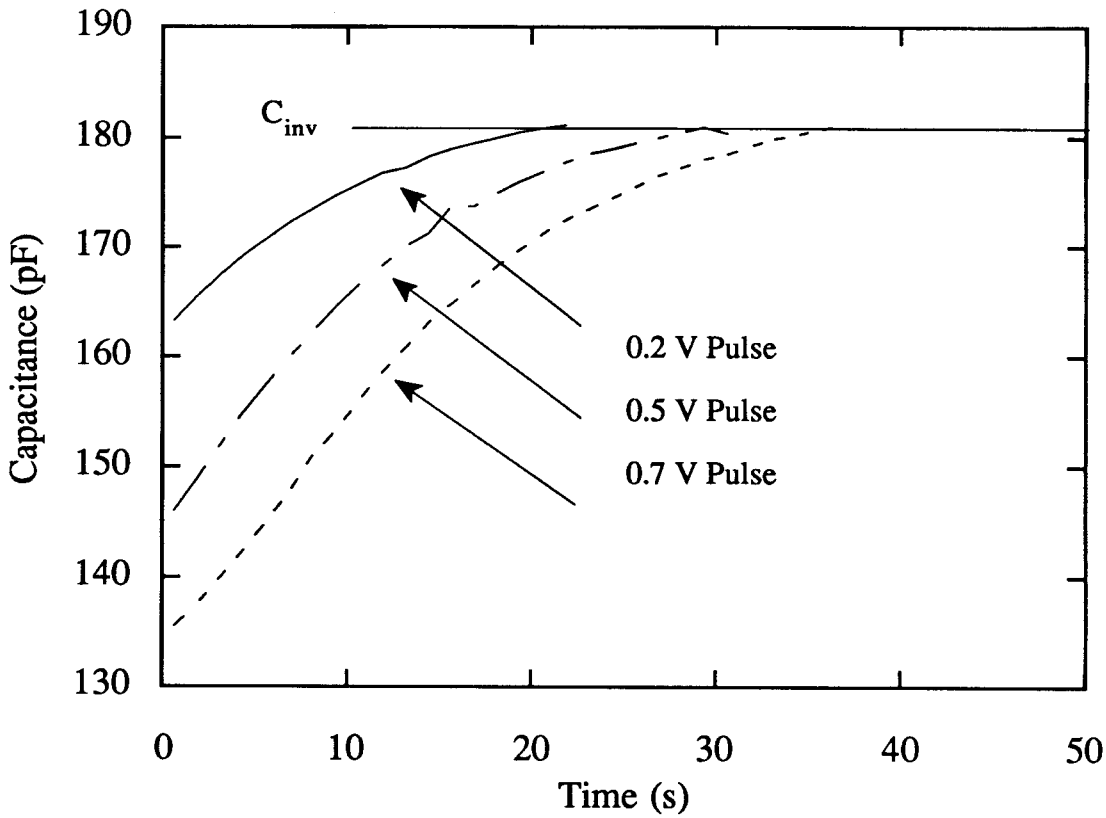


Figure 5.3. Capacitance recovery *vs.* time. Three different voltage pulses were applied to this capacitor, 0- 0.2 V, 0 - 0.5 V, 0 - 0.7 V, and the capacitance was recorded with time. The capacitors recover from deep-depletion to inversion (C_{inv} is shown on the plot). Notice that the recovery times increase with increased voltage pulse.

capacitance, n_i is the intrinsic carrier concentration, N_A is the doping concentration and τ_g is the generation lifetime. However, because of the multilayer heterostructure, the details of generation must be examined before the above equation can be used and lifetimes extracted.

Generation processes in bulk semiconductors can be modeled by the Shockley-Hall-Read equation:

$$U = \frac{v_{th} N_T (n_i^2 - np)}{1/\sigma_n (n + n_1) + 1/\sigma_p (p + p_1)} \qquad [5.2]$$

where n and p are the concentrations of electrons and holes, respectively, v_{th} is the thermal velocity of the carriers, N_T is the trap density and σ_n and σ_p are the capture cross sections of the traps for electrons and holes, respectively, and

$$n_1 = n_i \, e^{(E_T - E_i)/kT} \qquad [5.3]$$

and

$$p_1 = n_i \, e^{(E_i - E_T)/kT} \qquad [5.4]$$

where E_T is the energy level of the trap and E_i the intrinsic Fermi level.

The generation process dominates only if the np product is less than n_i^2. If we assume $\sigma_n = \sigma_p = \sigma$ and that $E_T = E_i$ for simplicity, we find:

$$G = \frac{n_i^2}{\tau_o (n + p + 2n_i)} \qquad [5.5]$$

where $\tau_o = (\sigma N_T v_{th})^{-1}$. From this expression it is clear that the generation rate is maximized when n and p are both less than n_i. In this case, G is commonly written as n_i/τ_g, where $\tau_g = 2\tau_o$ is called the generation lifetime. This expression cannot be applied to the entire depletion region because the carrier concentrations decrease with a finite slope when moving from neutral (high carrier concentration) regions to depletion regions. The situation is further complicated in our multilayer structures since the band gap of the $Si_{0.82}Ge_{0.18}$ layers is less than that of the silicon layers, resulting in a larger intrinsic carrier concentration. Under conditions where n or p is greater than n_i, G can be much less

than n_i/τ_g resulting in an over-estimate of the generation lifetime. This subtlety is often overlooked in many experiments resulting in reports of an incorrectly high τ.

Assuming a band gap reduction of 150 meV in the $Si_{0.82}Ge_{0.18}$ compared to silicon [5], n_i in the $Si_{0.82}Ge_{0.18}$ is approximately $n_i(Si)\cdot\exp(150meV/2kT) = 2.6 \times 10^{11}$ cm^{-3} at room temperature. To illustrate this point, Fig. 5.4 shows the logarithm of the calculated carrier profiles as a function of depth into the capacitor at two different times during the recovery from deep depletion to inversion for a gate-substrate voltage pulse from 0 to 0.7 V. This voltage range operates the capacitor in the inversion regime for the total range of its recovery. This diagram can be constructed in a straightforward manner from the capacitance assuming an electron quasi-Fermi level calculated from the inversion layer density and a flat hole quasi-Fermi level in equilibrium with the substrate. The discontinuity in the hole concentration reflects the discontinuity in the valence band between the silicon and the silicon-germanium layers. As was stated previously, maximum generation will occur in regions where both the electron and hole concentrations are less than the local intrinsic carrier concentration, n_i (n_i is shown as the dashed line in Figure 5.4). During the recovery, this region is seen to sample the $Si_{0.82}Ge_{0.18}$ layer, meaning that the generation in the $Si_{0.82}Ge_{0.18}$ layer is not artificially suppressed because of high carrier concentrations. This understanding of the generation-recombination processes in semiconductors is needed when interpreting the experimental data.

A standard Zerbst plot is shown in Fig. 5.5 for a $Si_{0.82}Ge_{0.18}$ buried layer structure with a thermal oxide. However, before relating the slope of the Zerbst plot to the lifetime as is generally done, two points must be made. If we assume as a worst case that all of the generation occurs in the silicon-germanium films, the actual generation volume ($Si_{1-x}Ge_x$ only) is less than the total generation volume (includes $Si_{1-x}Ge_x$ and Si). Examination of Fig. 5.4 shows this correction, which reduces the extracted $Si_{1-x}Ge_x$ lifetime, by approximately 50%. Also, the generation rate and hence the recovery time are related by $G = n_i/\tau_g$. Since the intrinsic carrier concentration (n_i) depends upon the band gap, one must

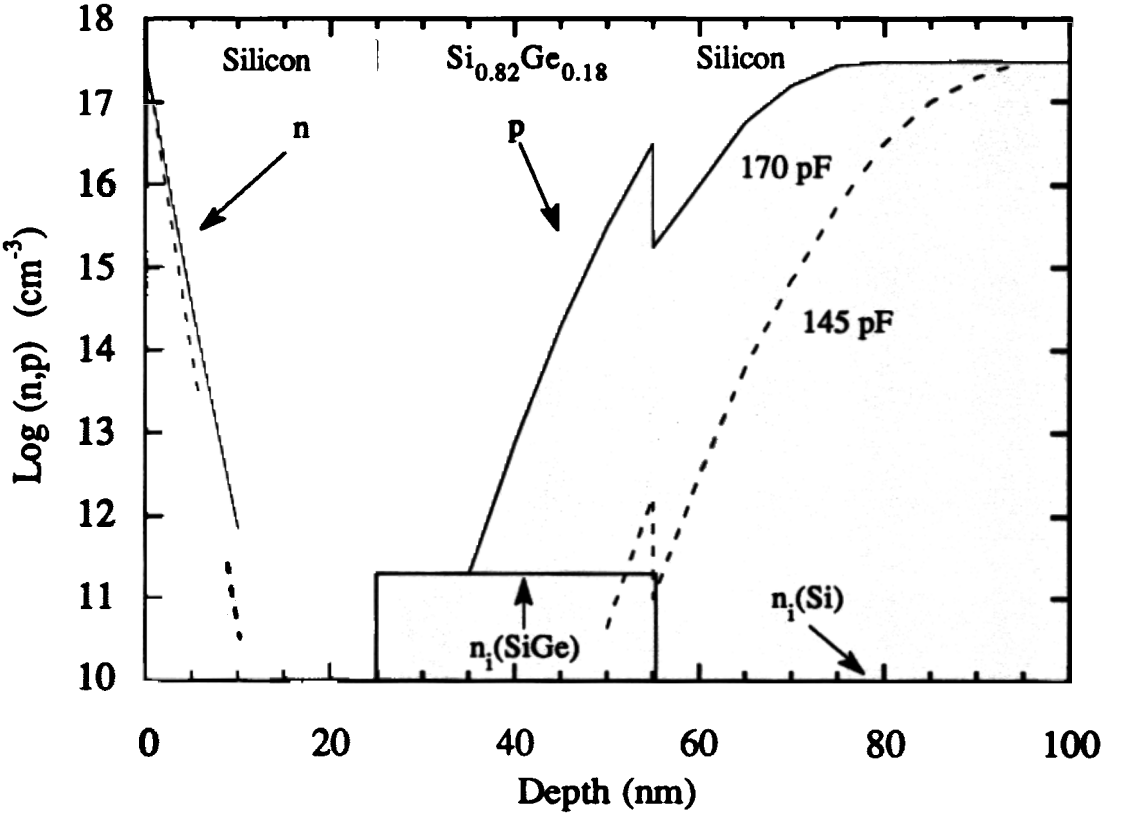


Figure 5.4. Logarithm of the carrier profiles as a function of depth into the semiconductor at two points in the recovery from deep-depletion to inversion. The dashed line represents the carrier concentrations when the capacitance is 145 pF while the solid line represents the carrier concentrations when the capacitance is 170 pF. The discontinuity in the hole concentration corresponds to the valence band discontinuity at the silicon/silicon-germanium interface. The effective generation region is seen to sample the $Si_{0.82}Ge_{0.18}$ layer.

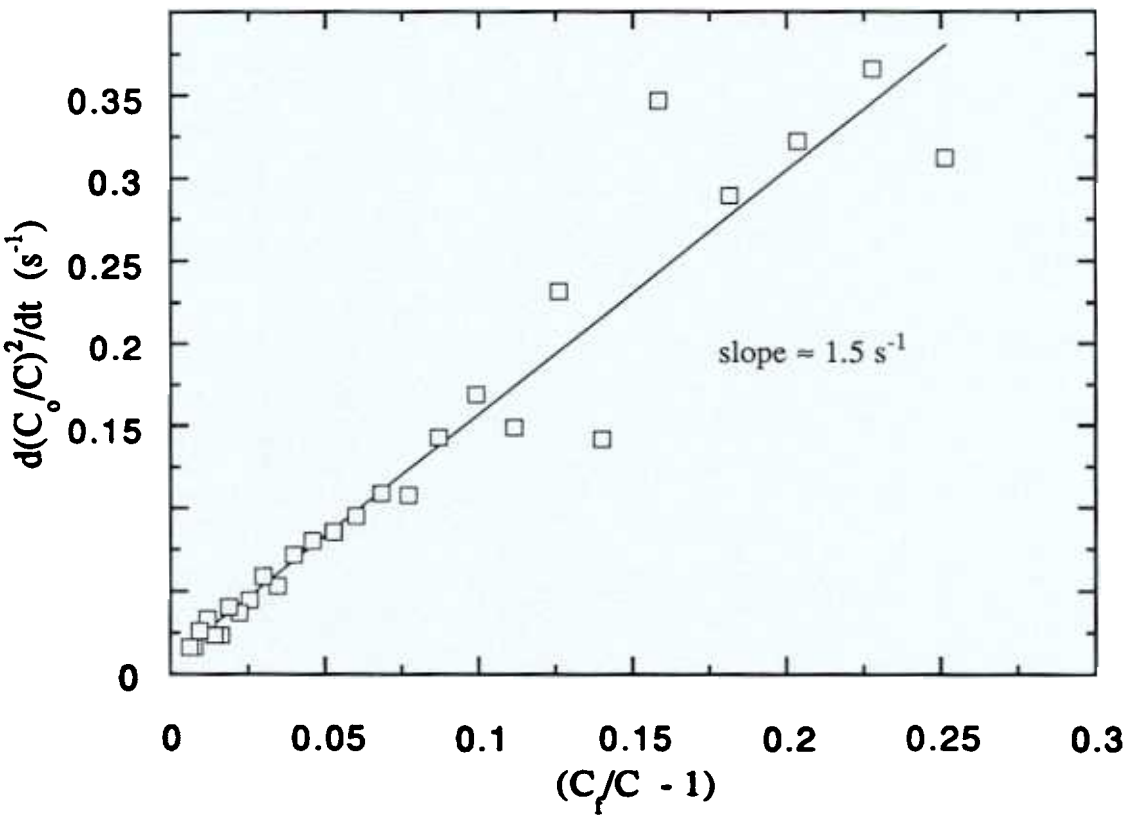


Figure 5.5. Zerbst plot of a recovering capacitor. The Zerbst analysis is effectively plotting the generation volume *vs*. the generation rate and extracting a lifetime from the slope. The lifetime is directly proportional to n_i and inversely proportional to the slope of the Zerbst plot. The lifetime of this capacitor is ~ 2 μs.

use n_i for $Si_{0.82}Ge_{0.18}$ when calculating τ_g from the recovery time (slope of the Zerbst plot). Since generation is a thermally-activated process of emission from traps to band edges, we expect faster generation in a narrower gap material for identical trap densities and cross sections. (Lifetime, by definition, depends only on trap density and capture cross-section). A consequence of this is that the generation rate (G) in the silicon-germanium is much greater than that in silicon for the same generation lifetimes.

5.3.1.2 Data and Interpretation

The generation lifetime (extracted with the Zerbst technique using the proper corrections) of the low-oxygen content ($<10^{18}$ cm^{-3}) $Si_{0.82}Ge_{0.18}$ buried layers is approximately 1.45 μs for the capacitor with a thermal oxide. The lifetimes of the high oxygen content films ($> 10^{19}$ cm^{-3}) were much lower and were limited by the measurement set-up (~ 1ns). This lower lifetime suggests that a deep level trap resides in the oxygen doped layers. Several capacitors on each wafer were tested for lifetimes and typical values are seen in Table 5.1. These lifetimes were found using an approximation to the Zerbst analysis described by Schroder and Guldberg [1]. The generation lifetime found above using the Zerbst analysis and that found using the approximate method differ only by a factor of approximately 1.5

The recovery times (τ_r), shown in Table 5.1, are defined as the time required for the capacitor to reach 90% of its final capacitance value after application of the voltage pulse. This parameter illustrates the difference between the buried silicon-germanium capacitors and the all silicon devices due to the difference in the intrinsic carrier concentrations. The low-temperature all-silicon capacitors (grown at 700 °C) have total recovery times approximately 20 times longer than their silicon-germanium counterparts which were fabricated in parallel.

The larger recovery times in the silicon devices demonstrate that the generation in the buried $Si_{1-x}Ge_x$ devices is most likely in the $Si_{1-x}Ge_x$ layer and not at the Si/SiO_2 interface. (Both samples had Si at the SiO_2 interface.) If the generation were surface-

Sample	Doping ($\times 10^{17}$ cm^{-3})	Oxide type	τ_g (μsec)	Recovery time (sec)	Oxygen Conc. (cm^{-3})
<100> Cz Si	0.005	thermal	9	325	$< 10^{18}$
<100> Cz Si	0.005	deposited	8	275	$< 10^{18}$
700 °C Si	2	thermal	2	400	$< 10^{18}$
$Si_{0.82}Ge_{0.18}$	3	thermal	1	26	$< 10^{18}$
$Si_{0.82}Ge_{0.18}$	2	deposited	1	19	$< 10^{18}$
750 °C Si	~ 2	deposited	$< 10^{-3}$	$<10^{-3}$	~ 10^{20}

Table 5.1. Recovery times and generation times of capacitors with different oxides and one with a large concentration of oxygen. The silicon heavily-doped with oxygen has a generation lifetime shorter than the resolution of the measurement. The lifetimes of the silicon-germanium layers were calculated using the increased intrinsic carrier concentration for $Si_{0.82}Ge_{0.18}$. The silicon devices were pulsed from 0 V to 3 V while the silicon-germanium devices were pulsed from 0 V to 0.7 V.

dominated, one would expect the total recovery time of the $Si_{1-x}Ge_x$ and the silicon capacitors to be similar for large voltage pulses. Further evidence that the generation is not surface related comes from comparing the lifetimes of the capacitors with thermal oxides and those with plasma deposited oxides. We see that the deposited oxides have lifetimes of the same order of magnitude. Although the silicon capacitors had recovery times ~ 20 times longer than that of the $Si_{1-x}Ge_x$ capacitors, one finds similar lifetimes in the two materials because of the difference in their intrinsic carrier concentrations. This implies that the silicon and silicon-germanium layers have similar trap densities and properties.

We also performed temperature dependent measurements of the total recovery time on some of the capacitors. Since the generation of carriers is a thermally activated process from traps to the band edges, this gives us a measure of the trap level within the band gap. An Arrhenius plot of the recovery time is shown in Figure 5.6. From the slope we find an activation energy of 0.6 eV which corresponds to the energy difference between either the trap level and the conduction band or the trap level and the valence band. Our assumption of the midgap trap level in Eqn.'s 5.3 and 5.4 proves to be reasonable since the band gap of silicon is 1.12 eV at room temperature.

Since we know the trap level and a maximum carrier lifetime, we can estimate a capture cross section of the oxygen contaminant. If we assume, as a worst case, we have one trap per oxygen (10^{-20} cm^{-3} for < 1ns lifetime), the minimum capture cross section is 10^{-18} cm^{-2}. This is a lower limit since τ was the upper limit due to the measurement resolution for short lifetimes.

By pulsing an MOS capacitor we have probed the minority carrier lifetimes in oxygen-doped and oxygen-free epitaxial layers. The effect of oxygen on the lifetimes of the films is dramatic, reducing the lifetimes by at least three orders of magnitude, clearly demonstrating the detrimental effects of oxygen on the minority carrier lifetimes. The lifetimes of the low-oxygen concentration films are the longest lifetimes reported for silicon-germanium strained layers grown by any technique. The long lifetimes demonstrate

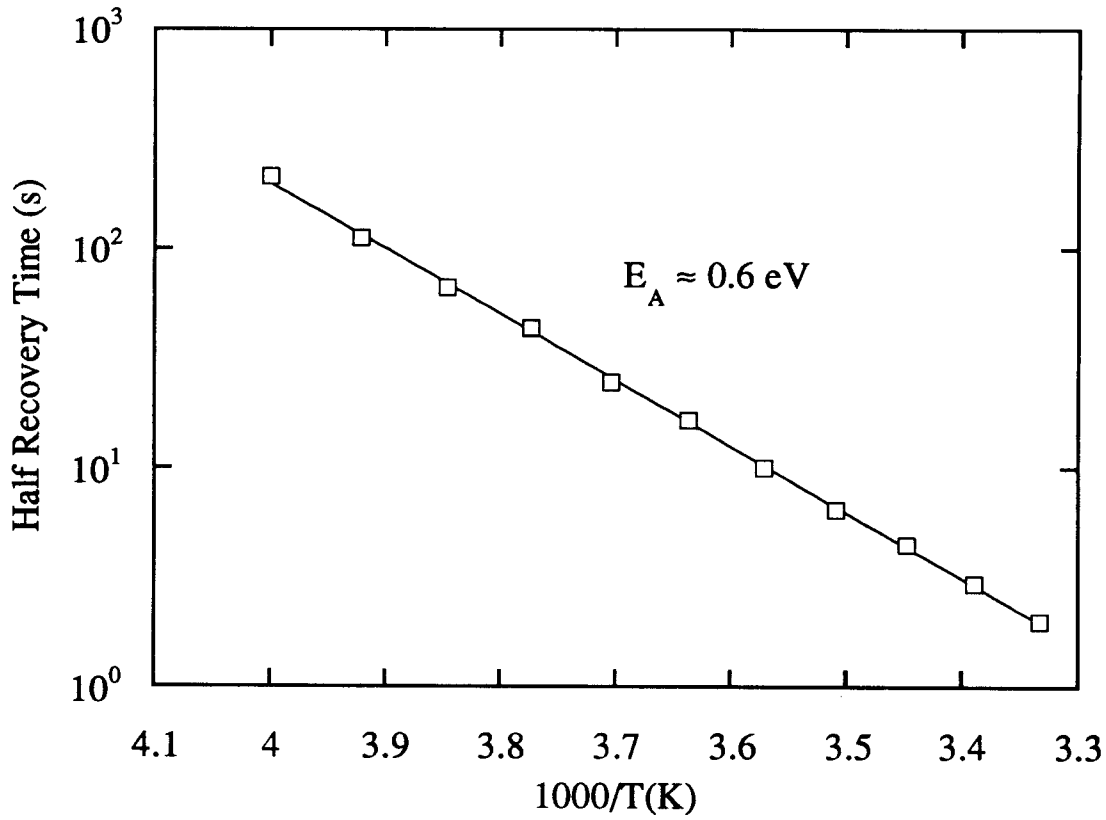


Figure 5.6. Temperature dependence of recovery time for an all-silicon device. The activation energy of this plot is 0.6 eV.

that one can make low leakage junctions with this material as needed for heterojunction bipolar transistors and p-i-n photodiodes.

5.4 Recombination Lifetime Measurements

The recombination lifetimes were studied by analyzing the base current characteristics of HBT's. There is an intimate relationship between the gain of a bipolar transistor and the minority carrier lifetime in the base. The gain of the transistor increases with the minority carrier lifetime in the base region. Long carrier lifetimes are required to minimize base currents, thus maximizing current gain. We also used the photoluminescence properties of the silicon-germanium strained layers to qualitatively measure the recombination lifetimes of the films. Long recombination lifetimes are required in indirect band gap materials (such as silicon, germanium and silicon-germanium) in order to see band-edge luminescence. By studying the properties of the films with and without oxygen contamination, we have determined the limiting effects on carrier lifetime due to oxygen in the epitaxial layers.

5.4.1 Heterojunction Bipolar Transistor Characteristics

We studied the base current characteristics of $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors (HBT's) to determine the lifetime limiting effects of oxygen on minority carrier recombination lifetimes. HBT's are important electronic devices for high speed circuit applications because they allow heavy base doping while maintaining a high injection efficiency because of the band gap offset between the silicon emitter and the $Si_{1-x}Ge_x$ base. Most HBT work has been reserved for compound semiconductor systems such as $GaAs/Al_{1-x}Ga_xAs$ [6] and $InP/In_{1-x}Ga_xP$ [7] but the potential compatibility of $Si_{1-x}Ge_x$ with silicon VLSI manufacturing technology is especially attractive. It is also possible to study the effects of oxygen on homojunction devices, but for historical reasons we chose to study $Si_{1-x}Ge_x$-based HBT base currents.

In the first $Si/Si_{1-x}Ge_x/Si$ HBT's grown by low temperature CVD, by C.A. King *et al.* [3] at Stanford University, oxygen concentrations reached levels of 10^{20} cm^{-3} in the

base regions. These were the first HBT's in silicon-germanium to exhibit an ideal collector current increase with the addition of germanium to the base. At the time, it was wondered if the oxygen was actually necessary for ideal I_C transistor characteristics. In these devices, however, the base currents were not ideal and the high oxygen content in the base region was blamed for the degradation. By removing the oxygen from the films, we were able to study the effect of oxygen contamination on the base current characteristics and also report the first ideal base currents in $Si/Si_{1-x}Ge_x$ HBT's grown in a non-UHV environment [8]. The following discussion assumes a knowledge of bipolar transistors - an excellent reference for the physics of HBT's can be found in the doctoral thesis of E.J. Prinz [9] and also a review article by Iyer [10].

5.4.1.1 Theory

Figure 5.7 shows the band diagrams for a silicon homojunction bipolar transistor (BJT) and a $Si_{1-x}Ge_x$ HBT (both npn structures). The layers of the HBT are similar to the semiconductor layers used in the capacitor of Figure 5.2 with the appropriate doping types. The collector and emitter regions of both devices are formed in silicon but the base region of the HBT is formed by strained $Si_{1-x}Ge_x$ and hence has a narrower band gap. The collector current in the device is determined by the number of electrons which can surmount the potential barrier between the emitter and base and traverse the base region to be collected at the opposite side of the device (collector). Because of the band alignment of the $Si_{1-x}Ge_x$, the barrier seen by the electrons at the emitter-base junction is lower in the HBT than in the BJT by an amount ΔE_g. This lowering of the barrier in the HBT leads to an exponential increase in the collector current over the BJT ($I_{C\ HBT} \approx I_{C\ BJT} \exp(\Delta E_g/kT)$[11]). Since the transistor gain (ß) is proportional to I_C, ß increases by the same exponential factor.

The base current, on the other hand, is ideally independent on the band gap difference of the $Si_{1-x}Ge_x$. In general, there are four main sources of base current in heterojunction bipolar transistors. The primary source of base current in injection-

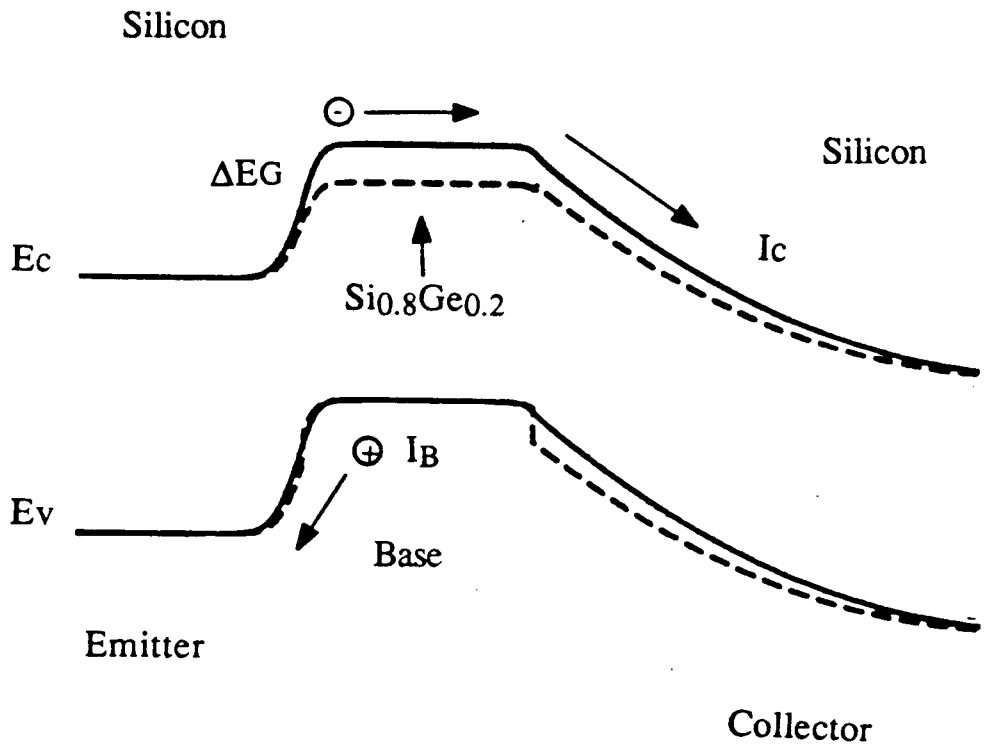


Figure 5.7. Band diagram for a heterojunction bipolar transistor and a silicon homojunction device. The the base region of the HBT has a narrower band gap which leads to a lowering of the conduction band in the HBT compared to the BJT. This lowering of the conduction band increases the gain of the device. Also shown are the collector current and the base current.

efficiency limited devices is due to the back injection of holes from the base to the emitter (or holes in the base region which surmount the potential barrier to be injected into the emitter) (I_{b1} in Fig. 5.8(a)). As can be seen in Fig. 5.7, the barriers experienced by the holes in the HBT and the BJT are identical, and consequently the base currents of the two devices should be equal, to first order. The base currents are, however, greatly increased if the minority carrier lifetimes in the silicon-germanium are very low.

The three other sources of base current are neutral base recombination (I_{b2}), recombination in the narrow band gap material of the emitter-base depletion region (I_{b3}), and recombination on the emitter side (lightly doped side) of the emitter-base metallurgical junction (I_{b4}) (see Figure 5.8). The total base current density in a narrow band gap base HBT with uniform base doping and germanium profiles, where the minority carrier diffusion length is much greater than the base width, can be expressed as: [12]

$$J_B = q\left(\frac{D_E\, n_{Ei}^2}{N_E\, W_E} + \frac{1}{2}\frac{W_B\, n_{Bi}^2}{\tau_B\, N_B} + \frac{1.7\, n_{Bi}^2\, x_B}{N_B\, \tau_{BB}}\right)\exp\left(\frac{qV_{EB}}{kT}\right)$$

$$+ \frac{1}{2}\frac{q\, n_{Ei}\, W_{EB}}{\tau_{BE}}\exp\left(\frac{qV_{EB}}{2kT}\right) \qquad [5.6]$$

where D_E is the minority carrier diffusion length in the emitter, W_B and W_E are the metallurgical widths of the base and emitter, respectively, τ_B is the minority carrier lifetime in the neutral base, τ_{BB} is the lifetime in the base-emitter space charge region on the base side of the metallurgical p-n junction (narrow gap) and τ_{BE} is the lifetime on the emitter side of the base-emitter metallurgical junction (wide gap). N_B is the base doping, N_E the emitter doping, and x_B the depletion width extending into the base region from the metallurgical junction. We distinguish the difference between the intrinsic carrier concentrations in the base (n_{Bi}) and emitter (n_{Ei}) regions. However, they are related, to first order, by $n_{Bi} = n_{Ei}\exp(\Delta E_g/kT)$. The first term in Eqn. 5.6 is due to back injection of holes into the emitter (I_{b1}), the second term is due to neutral base recombination (I_{b2}), and the third term is due to recombination in the emitter-base space-charge region extending from the heterojunction

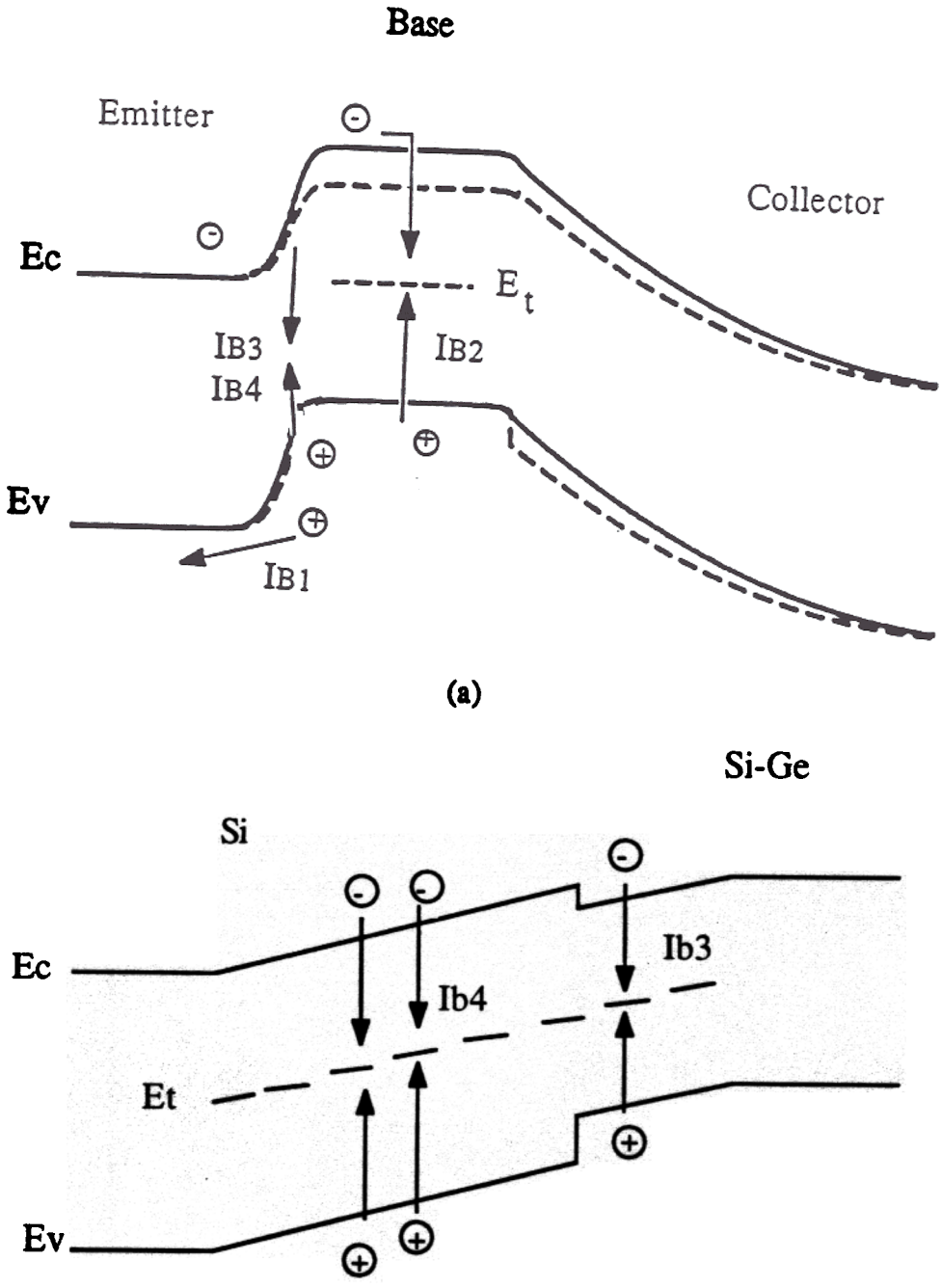


Figure 5.8. Base current components in bipolar transistors. (a) the four primary base currents of a bipolar transistor are: I_{b1} due to back injection, I_{b2} due to neutral base recombination, I_{b3} and I_{b4} due to recombination in the depletion region between the emitter and the base. (b) is an expanded view of recombination in the space-charge region. I_{b4} is the recombination on the lightly doped emitter side of the junction while I_{b3} is due to recombination in the depletion region on the heavily-doped, narrow-gap side of the junction. For I_{b3} to dominate, the lifetime in the heavily doped material must be much shorter than the lifetime in the lightly doped material.

to the neutral base and the fourth term is recombination in the space charge region on the emitter side of the p-n junction.

The first two terms and the fourth term of Eqn. 5.6 are standard base current components associated with bipolar transistors and are described in detail in Ref. [23] of Ch. 1. Current components I_{b1} and I_{b2} have an $\exp(qV_{EB}/kT)$ dependence and are termed 'n=1' currents referring to the ideality factor associated with p-n junction diodes. The slope of an 'n=1' current on a semi-log plot of current and voltage is ~ 60 mV/dec. The fourth current (I_{b4}) component has an $\exp(qV_{EB}/2kT)$ dependence and is termed an 'n=2' current, which on a semi-log plot has a slope > 60 mV/dec. The third term is different, however, from typical recombination current designations and is also an 'n=1' current component. Appendix I contains the derivation of the two space charge recombination currents (I_{b3}, I_{b4}) and shows the subtle differences in the assumptions that enter into the their determination. The characteristics of 'n=1' and n=2' currents will be important for data interpretation.

The gain of the heterojunction bipolar transistors can be related to the minority carrier lifetime by dividing Eqn. 5.6 by the collector current of an HBT [11]:

$$J_C \approx \frac{q\, n_{Bi}^2\, D_N}{N_B\, W_B} \exp\left(\frac{qV_{EB}}{kT}\right) \qquad [5.7]$$

assuming a flat germanium and doping profile in the base. Since $\beta = I_C/I_B = J_C/J_B$ we find the reciprocal of the HBT gain to be:

$$\frac{1}{\beta} \approx \left(\frac{N_B W_B}{D_B} \quad \frac{D_E}{N_E W_E}\right) + \frac{1}{2}\left(\frac{W_B^2}{D_B\, \tau_B}\right) + \left(\frac{1.7\, x_B\, W_B}{D_B\, \tau_{BEB}}\right)$$

$$+ \frac{1}{2}\left(\frac{n_{Ei}\, N_B\, W_{EB}\, W_B}{\tau_{BEE}\, n_{Bi}^2\, D_N}\right) \exp\left(\frac{-qV_{EB}}{2kT}\right) \qquad [5.8]$$

The first term, again, dominates when hole injection into the emitter is the largest form of base current, and the second term dominates if the minority carrier lifetime in the neutral base region is short. The third term is predominant if there is a short lifetime in the emitter-

base depletion region and the fourth term is dominant if the lifetime is short on the emitter side of the p-n junction. We will use these relationships in a later discussion.

5.4.1.2 Data and Interpretation

Figure 5.9 is a Gummel plot (logarithm of I_C and I_B vs. base emitter bias) for an HBT fabricated at Stanford University by C.A. King [3]. Also shown on the same plot is a homojunction control device made of all silicon layers (BJT). This was the first report of a heterojunction bipolar transistor in $Si/Si_{1-x}Ge_x$ grown in a non-UHV reactor very similar to the one used in our experiments but without a load-lock. At first glance, the device performance looks quite good - ideal base and collector current slopes ('n=1' and 60 mV/dec) down to 10^{-12} Amps and a current gain of 400. The HBT shows the enhanced collector current as expected due to the heterojunction (the base region was formed with $Si_{0.70}Ge_{0.30}$), but the base current has increased by a factor of almost 50 over the BJT. This increased base current was not expected as discussed earlier in this section and is characteristic of a short carrier lifetime in the base region of the device. It was reported for this HBT that the oxygen concentration in the silicon-germanium reached 10^{20} cm^{-3}.

From the arguments on n=1 current given above, even From the arguments on n=1 current given above, even though the base currents have ideal slopes down to 10^{-12} A, it is possible that the base current of this HBT has been increased by recombination in the base region of the device. From Eqn. 5.8 there are two different lifetimes to consider as the gain limiting mechanism and we can estimate a range for the minority carrier lifetime in this device. If $\tau_B \ll \tau_{BB}$ neutral base recombination will dominate the gain. In this case the estimated lifetime in the device is approximately 100 ps ($D_B = 6$ $cm^2/V/s$ and $W_B = 20$ nm - given in King's report). If, however, $\tau_{BB} \ll \tau_B$ (which may be caused by increased defect concentration near the hetero-interface), the third term of Eqn. 5.8 dominates the gain and (from the doping data given) the lifetime in the silicon-germanium in the emitter-base depletion region is ~ 2 ps. The third condition, where $\tau_B \approx \tau_{BEB}$ (which is reasonable since

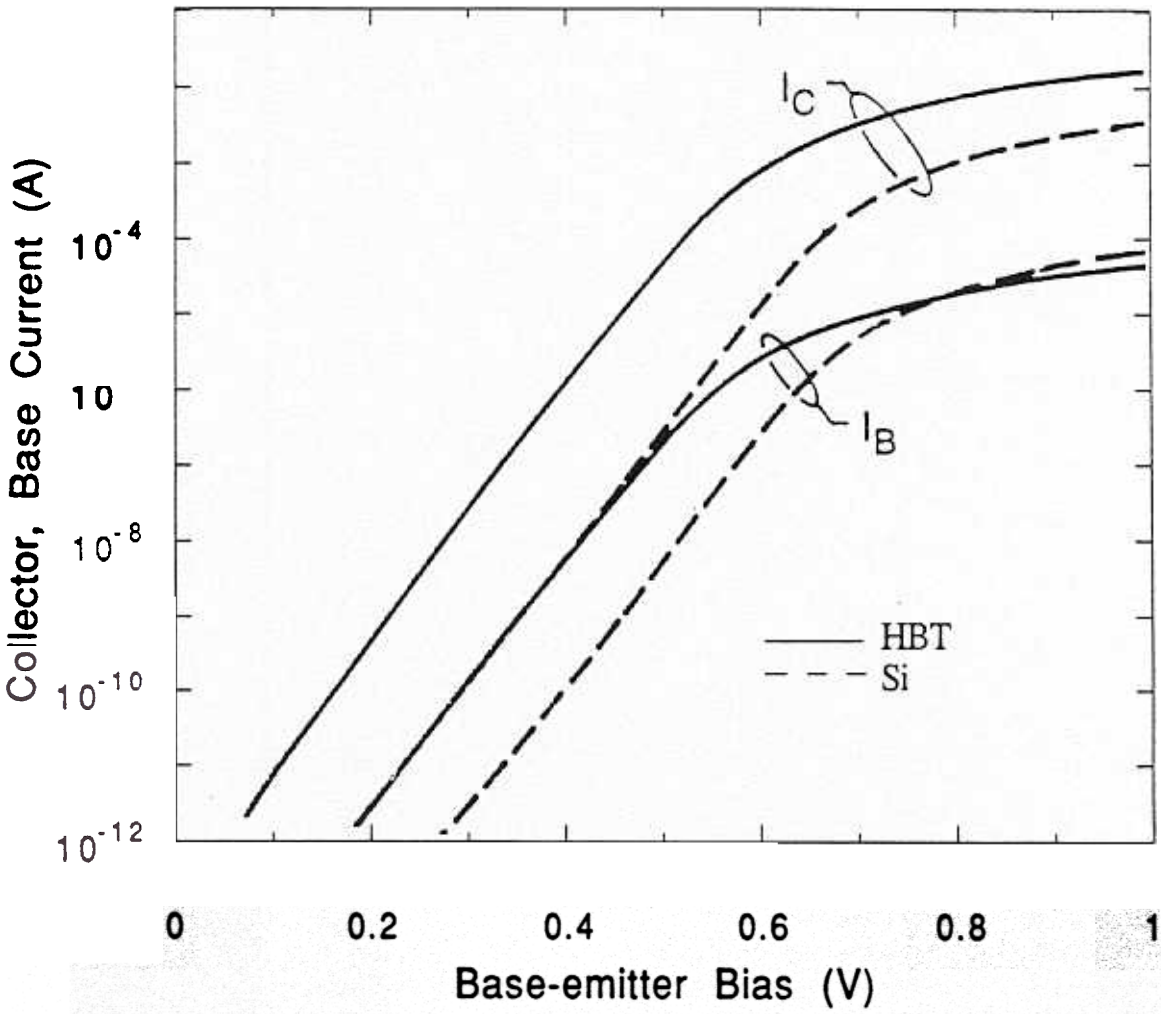


Figure 5.9. Gummel plot of a Stanford HBT (King). The plot of the logarithm of the base and collector currents as a function of base-emitter bias. The HBT exhibits the expected increase in collector current as expected, but the base current of the HBT has also increased which was not expected. The ideal slopes of the base current coupled with the increased base current suggest that the device is limited by recombination of carriers in the base region.

both are material characteristics of the base) is the same condition as the first since $W_B \gg x_B$. In any case, the gain of the gain of the device is determined by a carrier lifetime.

Figure 5.10 is a Gummel plot of an HBT and a BJT grown in our reactor and processed by E. J. Prinz. The germanium concentration in the base region is 20%. The oxygen content in this base region is below the detection limit of SIMS ($<10^{18}$ cm^{-3}). This HBT exhibits the increased collector current as expected, but also exhibits no increase in base current over the BJT. This implies the HBT is an injection-limited device, and the base current is not limited by neutral base recombination or space-charge region recombination but rather by back injection of carriers into the emitter. Since we are not limited by neutral base recombination, we can extract a lower limit to the minority carrier lifetime in the base from Eqn. 5.8, and we find it to be $\geq$ 10,000 ps compared to 100 ps in the silicon-germanium with an oxygen concentration level of 10^{20} cm^{-3} of King. This high recombination lifetime in the silicon-germanium without oxygen is consistent with the high generation lifetime in silicon without oxygen.

The high concentration of oxygen in the base region of the Stanford heterojunction bipolar transistor decreased the lifetime of the carriers by at least two orders of magnitude from the ideal case. By eliminating the oxygen from the silicon-germanium, we have increased the carrier lifetime in the base and demonstrated the first near-ideal base currents in $Si/Si_{1-x}Ge_x$ HBT's (no increase over a standard BJT) grown in a non-UHV environment. The ability to grow high lifetime films at low temperature in a non-UHV reactor is very important for industry since it avoids unneeded complexity of the manufacturing equipment.

5.4.2 Photoluminescence

Photoluminescence provides a qualitative means by which we can determine the relative magnitude carrier lifetimes in the silicon-germanium layers. Photoluminescence (PL) is a basic optoelectronic property of a material. Electrons and holes are generated by

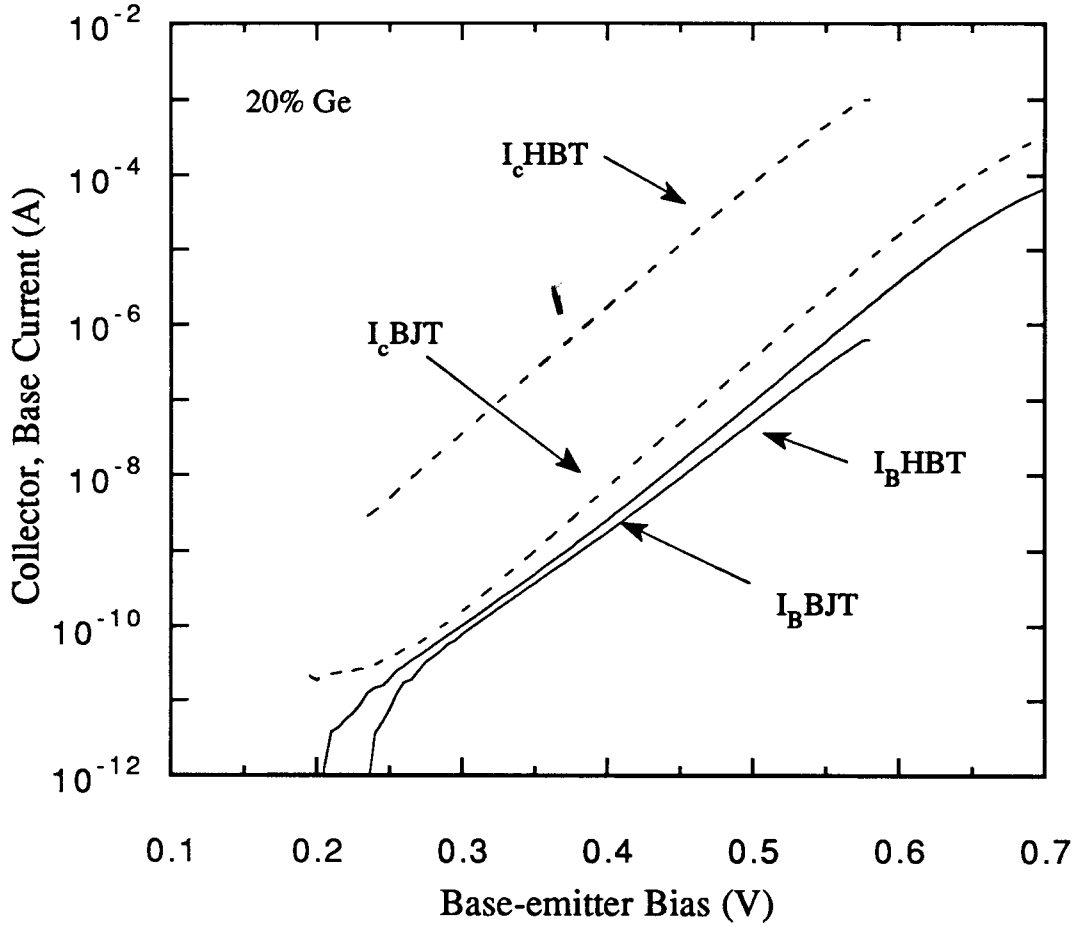


Figure 5.10. Gummel plot of a Princeton University HBT. The oxygen concentration in the base region of these devices was below the detection limit of SIMS ($<10^{18}$ cm^{-3}). The HBT has the enhanced collector current over the homojunction device as expected and has no increase in base current as expected. This HBT is an injection limited device, neutral base recombination is not the dominant source of base current.

laser illumination and light emitted during the subsequent radiative recombination of the carriers is detected. A schematic of PL in an indirect band gap is shown in Figure 5.11.

Conduction-band to valence-band recombination is an extremely slow process in indirect band gap materials such as silicon and germanium since phonons are required to conserve momentum (**k**). Since both radiative and non-radiative processes in semiconductors occur simultaneously, the fastest recombination process will tend to dominate the carrier recombination process. Relaxation processes are analogous to current distribution in an electronic circuit containing resistors of different values in parallel; if one resistor is significantly less than the other(s), most of the current passes through this resistor. In order to see conduction-valence band PL in silicon-germanium, the non-radiative (low resistance) paths must not shunt the radiative paths (*i.e.* we must increase the non-radiative recombination lifetime relative to the radiative recombination lifetime).

The first reports of band-edge luminescence in a strained layer of $Si_{1-x}Ge_x$ were by Terashima *et al.* [13] in thick epitaxial layers of 4% germanium content grown by molecular beam epitaxy (MBE) on silicon. If more germanium was added to the layers, the layers relaxed and were not strained. Band-edge photoluminescence of silicon-germanium strained layer quantum wells, however, has proven elusive. Noël *et al.* [14] at the National Research Council of Canada have reported strong PL (at 4K) in MBE grown $Si_{1-x}Ge_x$ at an energy level ~150 meV below the band-edge. Since this is significantly below the band gap energy, this luminescence is believed to be due to impurities or defects which incorporate during growth and give rise to levels within the band gap. Noël also recently explain the phenomena by luminescence from germanium clusters formed during epitaxial growth. Other work on strained SiGe layer superlattices [15, 16] has yielded luminescence which is almost certainly due to dislocations rather than the superlattices themselves. In our epitaxial layers grown by CVD at low temperatures and containing low concentrations of oxygen, we have observed the first band-edge photoluminescence of the silicon-germanium strained layer quantum wells.

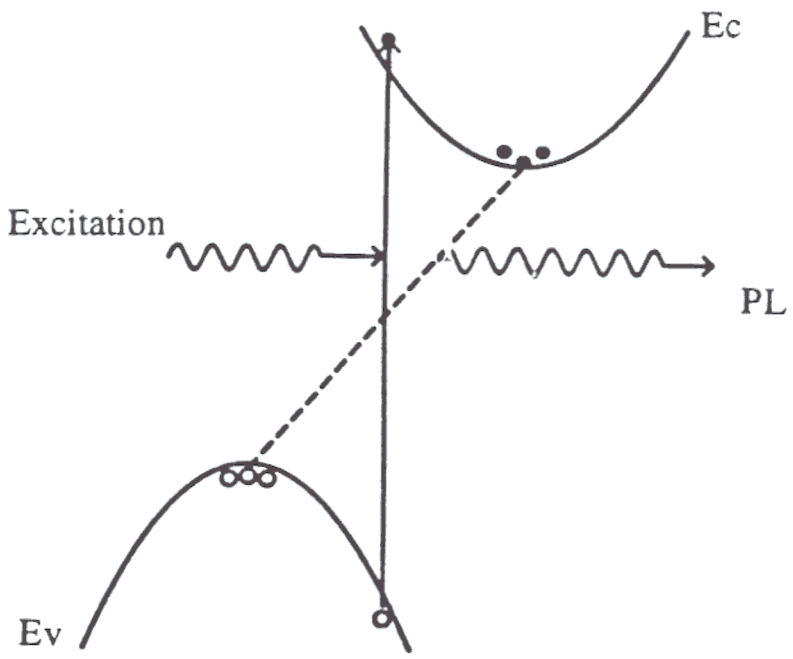


Figure 5.11. Schematic of photoluminescence in an indirect band gap semiconductor. Carriers are excited fom the valence band to the conduction band by laser illumination creating an electron-hole pair. The carriers relax to the lowest energy state of the band until they recombine. Phonons or alloy scattering are required to conserve momentum in these materials. Long carrier lifetimes are needed or carriers will non-radiatively recombine at traps.

The light detected from our samples is due to exciton recombination and phonon assisted transitions as opposed to defect related recombination. An exciton is an electron-hole pair which behaves much like a hydrogen atom and in some cases is free to move throughout the material.[17]. The energy of the emitted light from the free exciton (FE) recombination path is the band gap energy of the material reduced by the small binding energy of the exciton (~15 meV). Excitons can also be bound (bound exciton, BE) to impurity atoms which lowers the binding energy even further from the free exciton case. The phonon assisted transitions occur at energies reduced from the exciton energy by the characteristic energy of the phonons.

Figure 5.12 is a PL spectrum taken at 4 K, in an FTIR PL spectrometer, of a $Si_{0.80}Ge_{0.20}$ strained layer quantum well of width 3 nm grown in our laboratory and measured by Thewalt and Lenchyshyn at Simon Fraser University. By reducing the sample temperature to 4 K, many more features can be resolved demonstrating the long lifetimes of our oxygen-free silicon germanium layers. Figure 5.12 is a feature-rich spectrum. The peak labeled NP (at 1015 meV) corresponds to the no-phonon transition of a bound exciton in the silicon germanium alloy and occurs ~ 20 meV below the band edge of the $Si_{1-x}Ge_x$ strained layer (after correction for quantum confinement and the temperature dependence of the band gap). This transition is allowed due to the randomness of the alloy (localized alloy scattering) which satisfies conditions on **k** conservation [18]. Also visible are the phonon-assisted replicas (transverse optical - TO) corresponding to the different chemical bonds in the silicon-germanium alloy (the Si-Si, Ge-Ge and the Si-Ge bonds) and the transverse acoustic (TA) phonon replica. These were the first such features observed in strained $Si_{1-x}Ge_x$ quantum wells [19]. At 77 K, the individual phonon replicas are not resolvable and a broad peak encompassing the different chemical bonds results. Figure 5.13 is a PL spectrum taken at 77K showing the broad phonon-assisted peak, note this PL is due to a free exciton and not the bound exciton

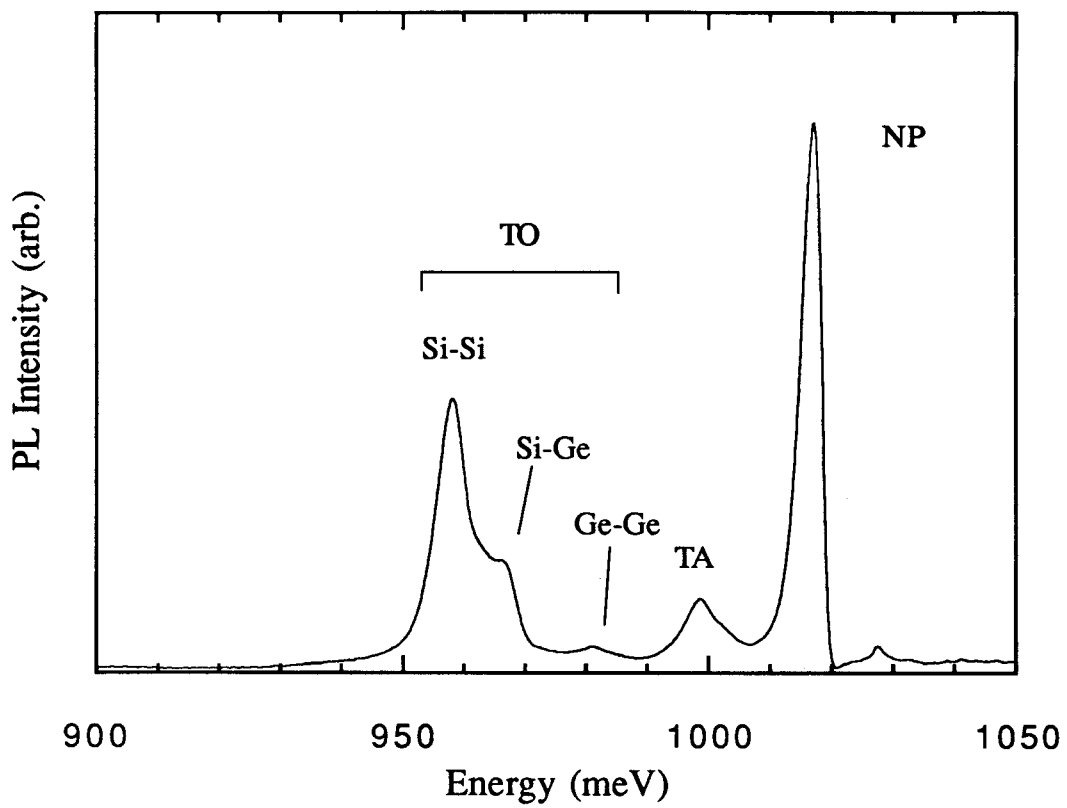


Figure 5.12. 4K Photoluminescence spectrum of a 30 Å thick $Si_{0.80}Ge_{0.20}$ strained layer. The no-phonon (NP) line is due to the randomness of the silicon-germanium alloy and occurs just below the band-edge of the silicon-germanium. The phonon replicas are clearly visible and correspond to the different chemical bonds in the material, Si-Si, Ge-Ge, and Si-Ge. The luminescence is due to bound excitons.

The photoluminescence properties of our films are strongly dependent upon the oxygen concentration in the $Si_{1-x}Ge_x$ layer. Figure 5.13 shows the photoluminescence spectra of two different samples containing $Si_{0.80}Ge_{0.20}$ strained layers taken at 77 K. The two spectra illustrate the difference in the non-radiative recombination lifetimes of the two films; notice the factor of 100 difference between the two intensity scales. The upper spectrum corresponds to a $Si_{0.80}Ge_{0.20}$ layer of high quality. The lower spectrum of Fig. 5.13 is from the second sample grown after venting the CVD chamber to atmosphere. The oxygen concentration of this sample reached approximately 3×10^{18} cm^{-3} in the silicon-germanium layer as determined by SIMS. From the argument presented above, this means that the non-radiative recombination lifetimes differ by at least two orders of magnitude. (We cannot assign an absolute number since we do not know the exact ratio of non-radiative to radiative lifetime in either sample.)

Increasing the oxygen concentration in the silicon-germanium layers to levels $\geq 5 \times 10^{19}$ cm^{-3} removes all signs of band-edge PL at 77 K. The elimination of the PL peaks is due to an introduction of band gap states in the alloy. As discussed in the introduction of this chapter, the presence of a set of localized traps within the energy gap of an indirect band gap material provides an efficient path for non-radiative carrier recombination. Whether the disappearance of the PL is due to an oxygen complex or the formation of defects in the material is still unclear. TEM was not performed on the structures to determine a defect density and defect etching could not be performed because the layer were too thin.

We have demonstrated the ability to grow low oxygen content, high lifetime epitaxial layers at low temperature under non-UHV conditions. By avoiding oxygen contamination in our epitaxial films, we have succeeded in demonstrating the first band-edge photoluminescence from strained $Si_{1-x}Ge_x$ quantum wells qualitatively demonstrating long carrier lifetimes. MBE samples also have low oxygen concentration, but the best PL is still from CVD grown material. MBE has a problem with metal contamination or some

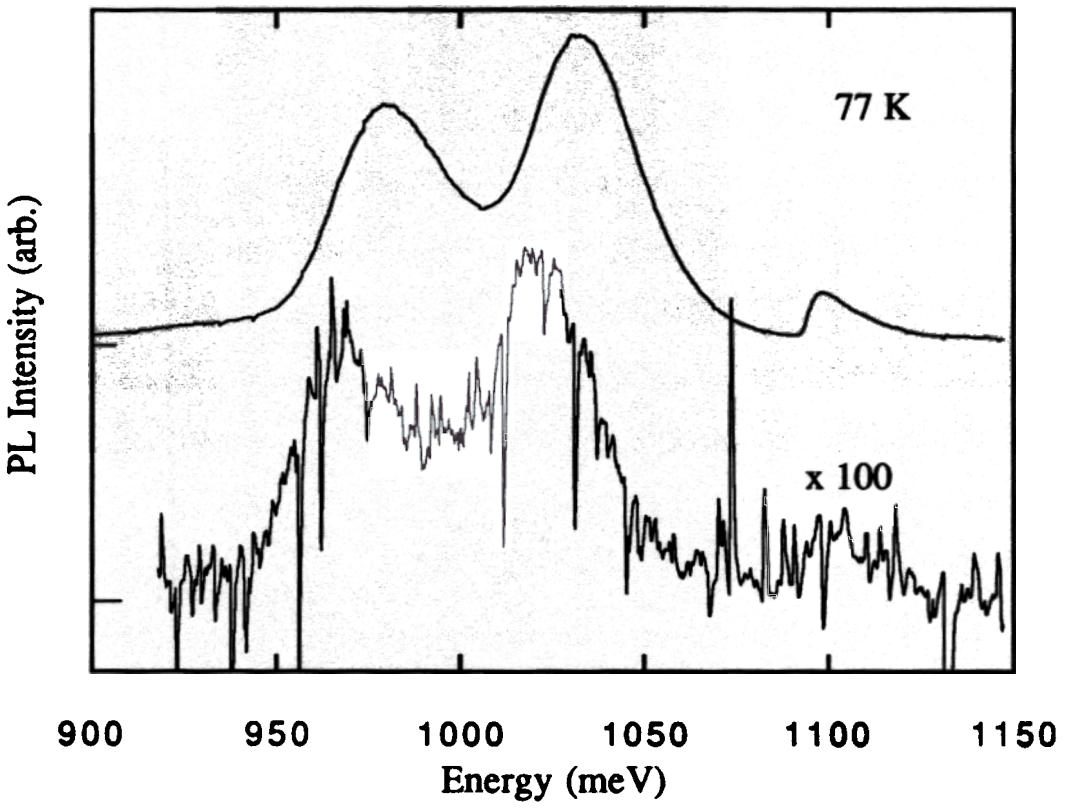


Figure 5.13. PL spectra of silicon-germanium layers grown in a well baked system and a newly vented system. The top spectrum corresponds to a silicon-germanium sample grown in a baked-out system and the bottom spectrum corresponds to a silicon-germanium layer grown as the second sample after the system was vented. Notice the factor of 100 difference between the two scales. The luminescence is due to free excitons.

other lifetime killing defect incorporating in the film. We have also demonstrated the first $Si/Si_{1-x}Ge_x/Si$ HBT's with ideal base current characteristics and reported the longest generation lifetimes measured in silicon-germanium strained layers to date.

5.5 Discussion of lifetime measurements

We have quantitatively investigated lifetimes in low-temperature CVD silicon and silicon germanium with and without oxygen. Ghani *et al.* [20] compared experimental data of silicon-germanium p-i-n diodes with SEDAN simulations of diodes to extract recombination lifetimes. By adjusting the minority carrier lifetimes in the diode simulations, they estimated the minority carrier lifetimes of devices containing different amounts of oxygen. The trend of lifetime with oxygen concentration is consistent with qualitative measurements of lifetimes by PL. At high concentrations of oxygen, the predicted lifetimes are comparable to the HBT data given above (2 ps for [O] ~ 2×10^{20} cm^{-3} and 100 ps for [O] ~ 8×10^{19} cm^{-3}). From the Stanford transistors and diodes and our generation lifetime measurements, we can estimate a capture cross section for the carriers in the silicon and the silicon-germanium. Again, we assume one trap per oxygen atom. The results are displayed in Table 5.2. The cross sections are in the regime of 10^{-17} cm^{-2} for the different devices fabricated. The cross section measured by the generation lifetime is limited by the measurement set-up as mentioned before.

The microstructure of the oxygen in the epitaxial films or metal impurities gettered at the oxygen sites may be the cause the short lifetimes associated with the heavily doped samples. Given similar numbers for lifetime *vs.* oxygen concentration between us and Ghani, metal impurities are unlikely since we would expect a larger variation in lifetime and cross section. Therefore, the low lifetimes are probably an intrinsic property of the high oxygen concentration. Oxygen coordinates as an electronically inactive interstitial atom in bulk Cz-silicon and therefore does not become a recombination center. In silicon films grown by low temperature CVD, however, the oxygen coordinates differently as is evident from the FTIR data of the high oxygen content films shown previously (Sec. 3.5). This

[O] cm^{-3}	Material	Measurement	τ (sec)	E_{trap} (eV)	σ (cm^{-2})
$<10^{18}$	Princeton $Si_{0.80}Ge_{0.20}$	Rec. HBT	$> 10^{-8}$	?	$> 10^{-17}$
10^{20}	Princeton Si	Gen. Cap.	$< 10^{-9}$	$E_v + 0.6$, or $E_c - 0.6$	$< 3 \times 10^{-18}$
10^{20}	Stanford $Si_{0.31}Ge_{0.79}$	Rec. HBT	100×10^{-12}	?	10^{-17}
2×10^{20}	Stanford $Si_{0.78}Ge_{0.22}$	Rec. Diode	2×10^{-12}	?	2.5×10^{-16}
10^{18}	Stanford $Si_{0.78}Ge_{0.22}$	Rec. Diode	2×10^{-8}	?	5×10^{-17}

Table 5.2. Capture cross section data determined by recombination and generation lifetime measurements on different devices.

different configuration may be due to the high concentrations of oxygen in excess of solid solubility. These possible configurations include substitutional oxygen and small SiO_2, platelets but the exact configuration is not known at this time. However, the configuration of oxygen in low temperature CVD films is clearly electronically active.

5.6 References

1. D.K. Schroder and J. Guldberg, "Interpretation of Suface and Bulk Effects Using the Pulsed MIS Capacitor," *Solid State Electr.* **14**, 1285 (1971);
M. Zerbst, " Relaxation Effects at Semiconductor Insulator interfaces," *Z. Angew. Phys.* **22**, 30 (1966) *in german.*

2. H. Tempkin, T.P Pearsall, J.C. Bean, R.A. Logan and S. Luryi, "Ge_xSi_{1-x} Strained-Layer Superlattice Waveguide Photodetectors Operating near 1.3 μm," *Appl. Phys. Lett.* **48**(15), 963 (1986).

3. C.A. King, J.L. Hoyt, C.M. Gronet, J.F. Gibbons, M.P. Scott and J. Turner, "$Si/Si_{1-x}Ge_x$ Heterojunction Bipolar Transistors Produced by Limited Reaction Processing," *IEEE Elect. Dev. Lett.* **EDL-10**(2), 52 (1989).

4. T.O. Sedgwick, "Dominant Surface Electronic Properties of SiO_2-Passivated Ge Surfaces as a Function of Various Annealing Temperatures," *J. Appl. Phys.* **39**(11), 5066 (1968).

5. R. People, "Indirect Band Gap of Coherently Strained Ge_xSi_{1-x} Bulk Alloys on <100> Silicon Substrates, " *Phys. Rev. B* **32**(2), 1405 (1985).

6. P.M. Asbeck, M.-C. F. Chang, J.A. Higgins, N.H. Sheng, G.J. Sullivan and K.-C. Wang, "GaAlAs/GaAs Heterojunction Bipolar Transistors: Issues and Prospects for Application," *IEEE Trans. Elec. Dev.* **TED-36**(10), 2032 (1989).

7. Y.-K. Chen, R.N. Nottenburg, M.B. Panish, R.A. Hamm and D.A. Humphrey, "Subpicosecond InP/InGaAs Heterostructure Bipolar Transistors," *IEEE Elect. Dev. Lett.* **EDL-10**(6), 267.

8. E.J. Prinz and J.C. Sturm, "Base Transport in Near-ideal Graded-base $Si/Si_{1-x}Ge_x/Si$ Heterojunction Bipolar Transistors form 150 K to 370 K," *IEDM Tech. Dig.* **IEDM 90**, 975 (1990).

9 E.J. Prinz, "," *Doctoral Thesis*, Princeton University (1992).

10 S.S. Iyer, G.L. Patton, J.M.C. Stork, B.S. Meyerson and D.L. Harame, "Heterojunction Bipolar Transistors Using Si-Ge Alloys," *IEEE Trans. Elec. Dev.* **TED-36**(10), 2043 (1989).

11. H. Kroemer, "Heterostructure Bipolar Transistors and Integrated Circuits," *Proc.IEEE* **70**(1), 13 (1982).

12. C.A. King, J.L Hoyt, J.F. Gibbons, "Bandgap and Transport Properties of $Si_{1-x}Ge_x$ by Analysis of Nearly Ideal $Si/Si_{1-x}Ge_x/Si$ Heterojunction Bipolar Transistors, " *IEEE Trans. Elect. Dev.* **36**(10), 2093 (1989).

13. K. Terashima, M. Tajima amd T. Tatsumi, "Near-band-gap Photoluminescence of $Si_{1-x}Ge_x$Alloys Grown on Silicon by Molecular Beam Epitaxy," *Appl. Phys. Lett.* **57**(18), 1925 (1990).

14 J.-P. Noël, N.L. Rowell, D.C. Houghton, and D.D. Perovic, "Intense Photoluminescence between 1.3 and 1.8 μm from Strained $Si_{1-x}Ge_x$ Alloys," *Appl. Phys. Lett.* **57**(10), 1037 (1990).

15. H. Okumura, K. Miki, S. Misawa, K. Sakamoto, T. Sakamoto and S. Yoshida, "Observation of Direct Gap Properties in Ge_nSi_m Strained-layer Superlattices," *J. Jour. Appl. Phys.* **28**(11), L1893 (1989).

16. R. Zachai, K. Eberl, G. Abstreiter, E Kaspar and H. Kibbel, "Photoluminescence in Short-period Si/Ge Strained-layer Superlattices," *Phys. Rev. Lett.* **64**(9), 1055 (1990).

17. J.I. Pankove, Optical Processes in Semiconductors, Dover, New York (1975).

18. J. Weber and M.I. Alonso, "Near-band-gap Photoluminescence of Si-Ge Alloys," *Phys. Rev. B* **40**(8), 5683 (1989).

19 X. Xiao, C.W. Liu, J.C. Sturm, L.C. Lenchyshyn, M.L.W. Thewalt, R.B. Gregory and P. Fejes, "Quantum Confinement Effects in Strained Silicon-germanium Alloy Quantum Wells," *Appl. Phys. Lett.* **60**(17), 2135 (1992).

20. T. Ghani, J.L. Hoyt, D.B. Noble, J.F. Gibbons, J.E. Turner and T.I. Kamins, " The Extraction of Minority Carrier Lifetime from the Current-voltage Chararteristics of $Si/Si_{1-x}Ge_x$ Devices," *Proc. Mat. Res. Soc.* **220**, 385 (1991).

Chapter 6

Semi-insulating Silicon by O-Doping

6.1 Introduction

We have shown that high concentrations of oxygen in silicon degrade the minority carrier lifetimes in the epitaxial layers. Short carrier lifetimes reduce gain in bipolar transistors, increase recombination currents in diodes, and shunt the radiative recombination processes required for photoluminescence. However, there are some properties of the oxygen-doped silicon layers which can be exploited to improve circuit and device performance. By intentionally introducing oxygen into the silicon layers, we can pin the Fermi level of the material near the center of the band gap. Since these films are crystalline (as was determined in Sec 3.4), we are able to grow crystalline silicon with low oxygen concentrations layers on top of the semi-insulating oxygen-doped material. In this chapter we display the semi-insulating characteristics of the oxygen-doped films and discuss their potential uses in the silicon material system. We then demonstrate a MOSFET fabricated in crystalline silicon grown on top of the oxygen-doped silicon (Si:O).

6.2 Semi-insulating Materials

Semi-insulating layers are important to high speed electronics because they provide circuits and devices with intrinsically small capacitances. Device interconnects fabricated on semi-insulating substrates have lower intrinsic capacitances and hence smaller RC time constants than those fabricated on semi-conducting substrates [1]. Low source-to-substrate and drain-to-substrate capacitances are also gained by fabricating MOS transistors on semi-insulating substrates [1].

Semi-insulating layers require minimal electron and hole concentrations in a material, which means the Fermi level is near mid-gap This requires the formation of an intrinsic material. This is difficult to achieve in silicon because even small concentrations of impurity atoms (10^{13} cm^{-3} impurity atoms out of 5 x 10^{22} cm^{-3} host atoms) yield a resistivity on the order of 1000 Ω-cm. Semi-insulating layers can be achieved, however, by introducing deep-level traps within the band gap to pin the Fermi level.

A considerable advantage of GaAs over silicon for high speed circuits (other than higher carrier mobilities) is the availability of semi-insulating substrates. Before ultra-pure GaAs was available, these substrates were formed by introducing a deep-level impurity to the substrate lattice. Chromium was the metal of choice not only because of its position in the GaAs band gap (E_V + 0.74 eV) [2] but also because of its low solid-state diffusion constant (2 x10^{-13} $cm^{-2}s^{-1}$ at 600 °C) compared to other deep-level impurities in GaAs [3]. Since GaAs requires low-temperature processing techniques (<700 °C), the chromium does not diffuse out of the substrate into the active device areas.

Most deep-level metal impurities in silicon (Fe, Au, Cr...) are efficient trapping centers but diffuse quickly even at moderate temperatures. For example, Fe will diffuse 440 μm in 20 min at 900 °C [3] (a standard processing condition for an implant anneal) [3]. This makes metal impurities impractical as mid-gap impurities in substrates for minority carrier devices. We propose using oxygen-doped silicon films, Si:O, to function as a semi-insulating material on which device quality silicon can be grown.

6.3 Si:O Electronic Characteristics

We grew oxygen-doped layers by the process described in Chapter 3. We grew several different layered structures for the various devices which we would use to test the electronic characteristics of the Si:O material. The electronic characteristics which we measured were: material resistivity, Fermi level position and carrier mobilities. The device structures used to measure the electronic characteristics are shown in Figure 6.1. We chose to measure vertical transport properties of the films to avoid parallel conduction channels in the conducting substrates in horizontal experiments.

6.3.1 Resistivity Measurements

We started by measuring the resistivity of the oxygen-doped layers using metal-(Si:O)-(n-Si) and metal-(Si:O)-(p-Si) Schottky diodes. Figure 6.2 is a typical current-voltage relationship for the n-type Schottky device. This device has an oxygen concentration of 2×10^{20} cm^{-3} and a film thickness of 10 μm. Notice that the voltage scale is –1 V to 5 V and the full-scale forward-bias current is less than 10 μA. This demonstrates the highly resistive nature of the oxygen-doped films. Similar results were obtained for p-type devices. We then measured the resistivity of the films as a function of temperature using the same device structure.

The electron concentration (n) in silicon is related to the Fermi level (E_f) position in a material by:

$$n = N_c \exp\left(\frac{E_f - E_c}{kT}\right) \qquad [6.1]$$

where N_c is the effective density of states for electrons in silicon and E_c is the conduction band energy, k is the Boltzmann constant and T the absolute temperature. Since resistivity (ρ) is inversely proportional to the carrier concentration ($\rho^{-1} = q\mu_n n$), we obtain the position of the Fermi level in the material with respect to the conduction band edge from the slope of a plot of resistivity *vs.* T^{-1} We assume that the dependence of μ_n and E_f on temperature is small over the range of the measurement. Figure 6.3 is a temperature-dependent plot of the resistivity of two Si:O layers (with the device structure of Fig. 6.1(a)

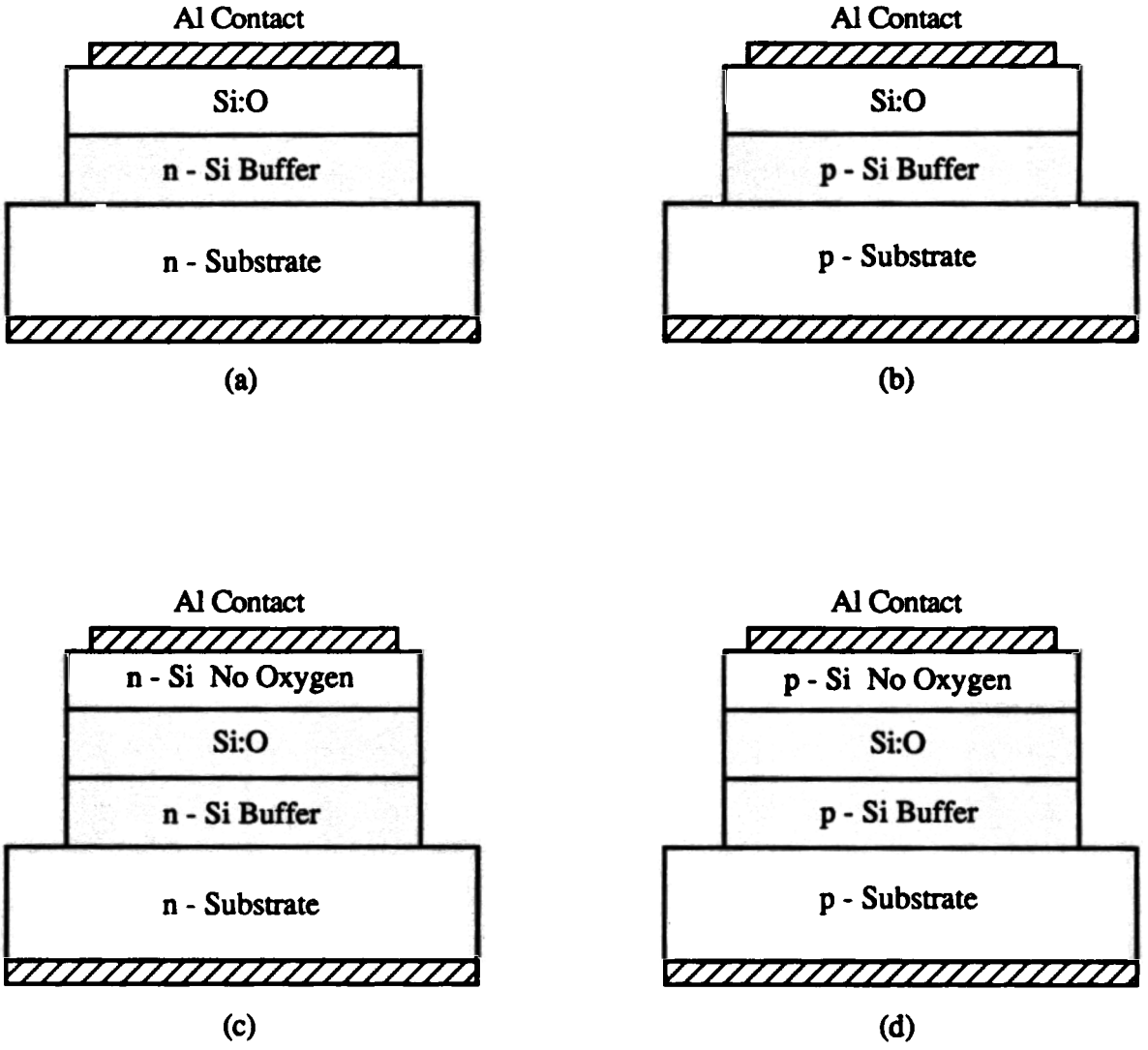


Figure 6.1. Device structures used for testing the electronic characteristics of the oxygen doped silicon layers. (a) Metal - Si:O - n and (b) Metal - Si:O - p were the devices used to measure the resistivity of the Si:O. (c) n - Si:O -n and (d) p - Si:O - p were used to determine the carrier mobilities.

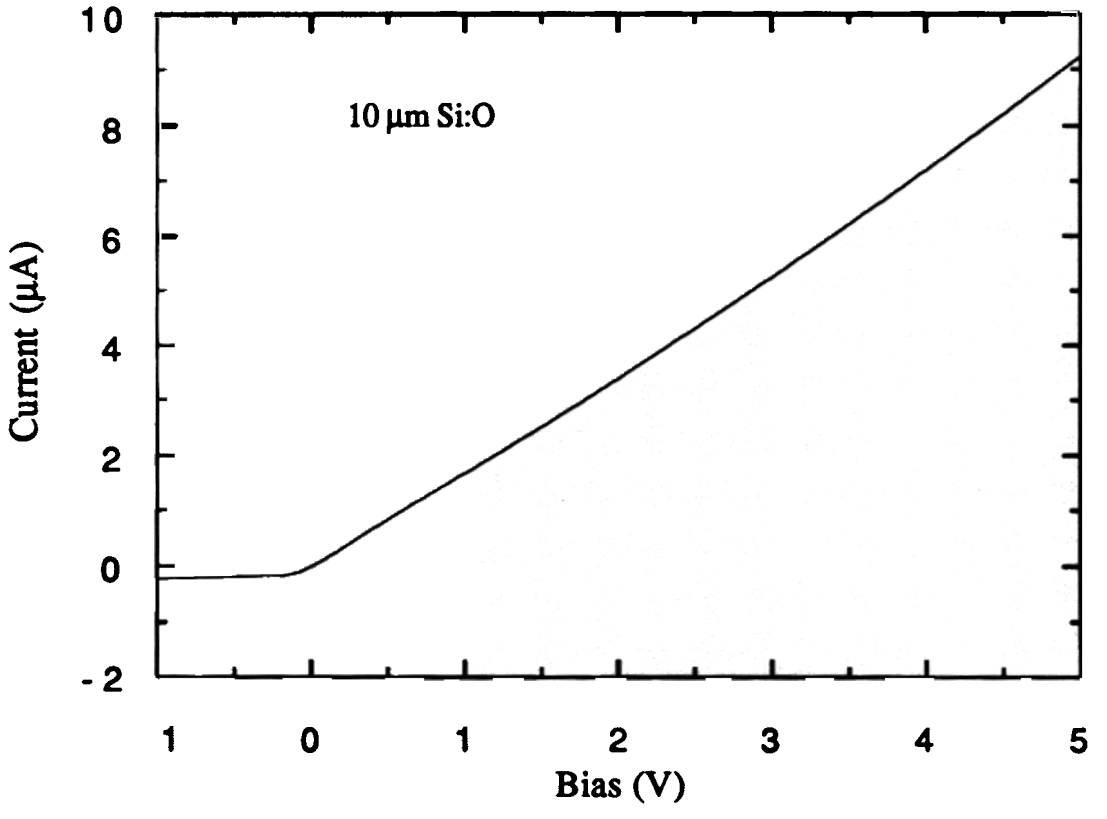


Figure 6.2. Room-temperature Current-Voltage characteristics of the metal - (Si:O) - (n-Si) device. Note that the full-scale current is only 10 μA for a 50 V bias. This demonstrates the high resistivity of the oxygen-doped silicon. The device area is 1.8×10^{-3} cm^{-3}.

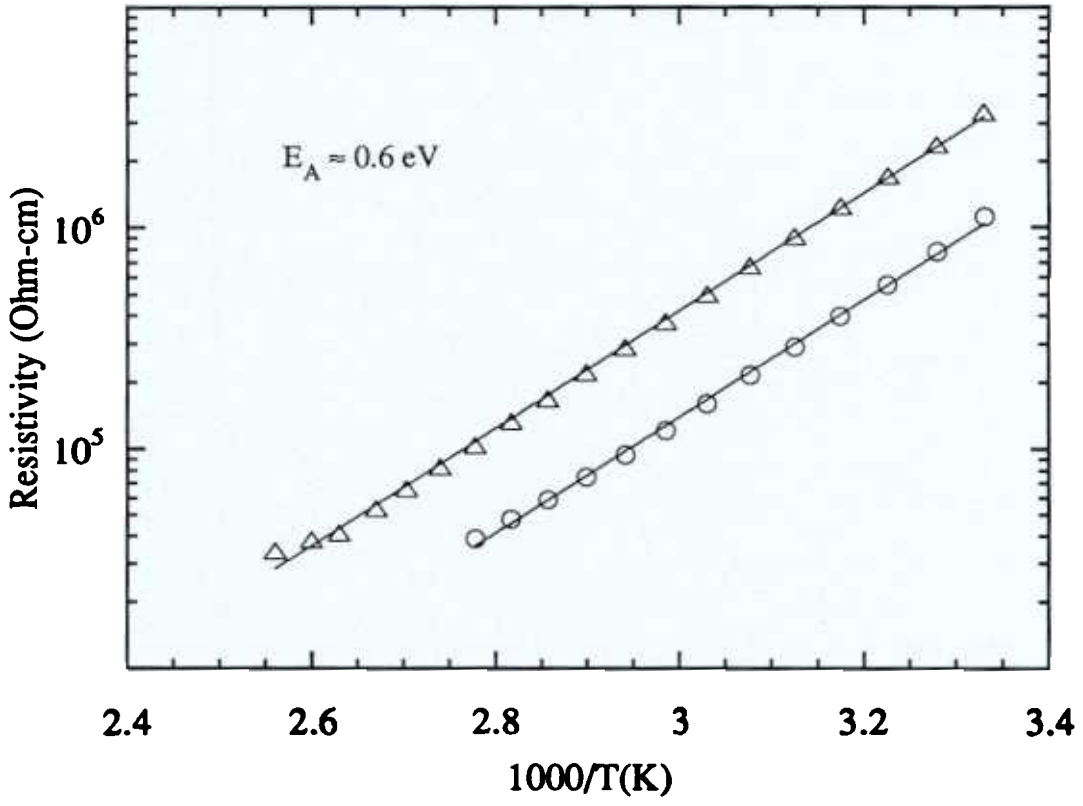


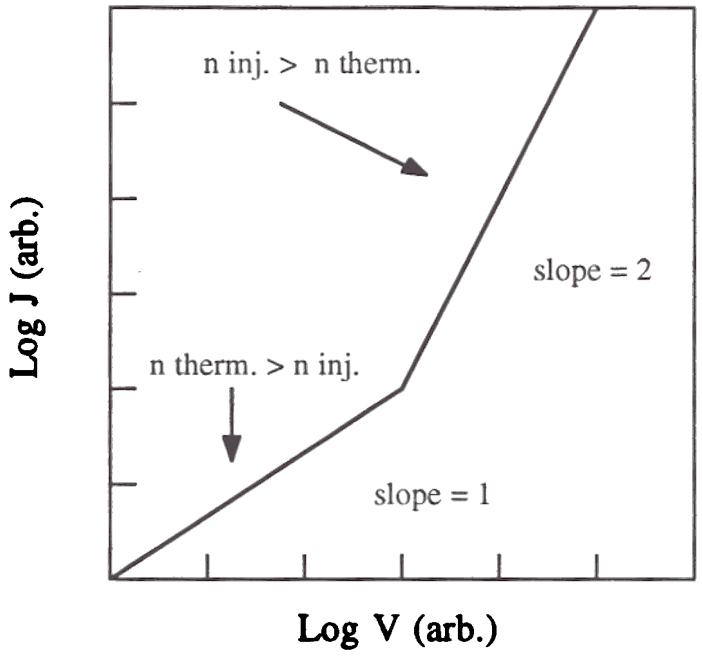
Figure 6.3. Resistivity of Si:O as a function of temperature. The slope of the curves (activation energy) gives us a position of the Fermi level in the material. The lighter-doped sample has an activation energy suggesting that the Fermi level is pinned at E_v + 0.4 eV or E_v + 0.6 eV. The data was taken at +4 Volts. The triangles are data taken on a sample doped to 2 x 10^{20} cm^{-3} with oxygen, and the circles are data taken on a sample doped to 5 x 10^{19} cm^{-3} with oxygen.

doped to levels of 2 x 10^{20} cm^{-3} and 5 x 10^{19} cm^{-3}. We measured the resistivities at 4 V forward bias to insure that any voltage drop across the Schottky contact is negligible. The slopes of Figure 6.3 (~ 0.6 eV) show that the Fermi level is indeed pinned near mid-gap. We have succeeded in pinning the Fermi level near E_v + 0.6 eV or E_c - 0.6 eV, which implies that the carrier concentration is within a factor of four of its intrinsic value.

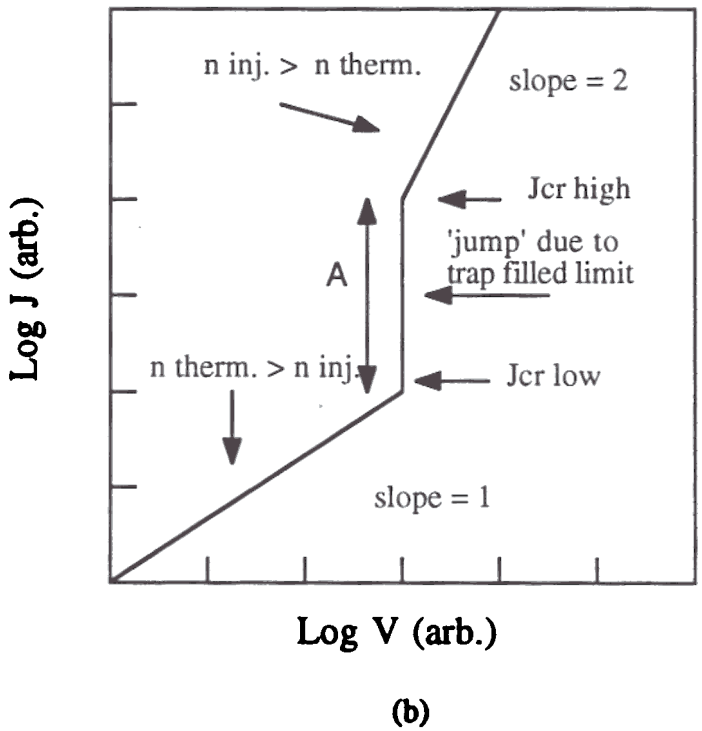
6.3.2 Mobility Measurements

We measured the carrier mobility properties using the n-Si:O-n and p-Si:O-p structures of Figure 6.1. Using the theory of Lampert and Mark [4] to describe the current-voltage characteristics of insulators exhibiting space-charge-limited current, we extracted the carrier mobilities for oxygen-doped films. We mention that we did not perform horizontal transport measurement (such as Hall mobility measurements), thereby avoiding parallel conduction in the silicon substrate. The theory of space-charge-limited current in insulators with traps is quite involved, and we refer the interested reader to the work of Lampert and Mark [4] for a full description. Here we give a physical picture of space-charge-limited current in insulators which contain a background of thermal carriers and trap levels within the band gap, and we discuss the current-voltage relationship in such materials.

First we describe the current-voltage characteristics of an insulating material with a background of thermal carriers in the absence of traps within the band gap. As a bias is applied to such a material, carriers are injected into the insulator and contribute to space-charge. Until the injected carrier concentration surpasses the background space-charge concentration, the charge of the carriers has little effect on the electric field and Ohm's Law is obeyed. This corresponds to a slope of one on a logarithmic plot of current and voltage (Figure 6.4(a)). The data Figs. 6.2 and 6.3 are taken from the linear regime. When the injected carrier concentration exceeds the background concentration, the space-charge set up by the injected carriers dominates the electric field and hence the voltage drop. Current flow in a space-charge-limited regime is proportional to the square of the voltage (J



(a)



(b)

Figure 6.4. Current transport in an insulator with a background of thermal carriers (a) without traps and (b) with a single trap level within the band gap. For both cases, Ohms Law is followed at low bias (n=1), but for high bias the square law prevails due to the build up of space-charge. In (b), however, a sudden jump in current occurs due to the filling of the trap level. A and $J_{cr\ low}$ are defined in Eqn. 6.2.

$\propto V^2$), which corresponds to a slope of two on a logarithmic plot of current and voltage (see Figure 6.4(a)).

Insulators with traps have a slightly different current-voltage relationship than the ideal insulator. We assume in the following that there is a single trap level within the band gap and that the Fermi level is at the trap level in equilibrium. Figure 6.4(b) will help to illustrate the conditions of current transport in the semi-insulating material with traps. At low bias and high bias the characteristics look very similar to the ideal insulator of Fig. 6.4(a). As a bias is applied across the device of Figure 6.1 (c), carriers are injected from the n region into the semi-insulating region. Until the injected carrier concentration exceeds the background concentration, the current will be due to the background of thermal carriers in the material and Ohms Law is obeyed, much like the trap-free case. On the schematic plot of logarithm of current *vs.* the logarithm of voltage of Figure 6.4(b), this corresponds to a slope of one (n=1).

As we continue to increase the bias across the device, the carriers injected into the Si:O initially serve to fill the traps within the material since the Fermi level is pinned at the trap level energy. When all of the trap sites are filled, the current increases sharply with voltage because the quasi-Fermi level is able to move above the trap level. This corresponds to a sudden increase in the current with a small increase in voltage. (A factor of two change in carrier concentration corresponds to raising the Fermi level approximately 0.7 eV). In Figure 6.4(b), this correspond to the region labeled "jump".

Once the traps are filled, all of the injected carriers contribute to space-charge and the current characteristics are similar to the trap-free condition. In Figure 6.4(b), this corresponds to the region where the slope is two. The theoretical expression for the current at the point where the current jumps from the low current level to the high current level ($J_{cr\ low}$) is [4]:

$$J_{cr\ low} = \frac{A\, q^2\, n_o^2\, \mu\, L}{\varepsilon} \qquad [6.2]$$

where A is the size of the current jump at the critical point, q the electron charge, n_o the thermal carrier background concentration, μ the mobility, L the length of the insulator and ϵ the dielectric constant.

Figure 6.5 is a logarithmic plot of the current and voltage for a p-Si:O-p device with a 3 μm semi-insulating region. By changing the length of the semi-insulating region, we can shift the critical voltage to different values ($V_{cr} \propto L^2$). The diode of Fig. 6.2 (L = 10 μm) does not show the jump in current until 100 V is applied. The features of Fig. 6.5 are similar to those depicted in Fig. 6.4(b) demonstrating the trapping properties of the film. The mobility we extract from the p-Si:O-p device is approximately 100 $cm^2V^{-1}s^{-1}$ (for holes) and for an n-Si:O-n device it is about 400 $cm^2V^{-1}s^{-1}$ (for electrons). We calculated n_o from the position of the Fermi level determined from the temperature dependent measurements. These high mobilities may find application in high speed photoconductive switches where short lifetimes and high mobility materials are required.

6.4 Silicon on Semi-insulating Layers

Semi-insulating silicon layers can be used for many purposes, as discussed in the opening section of this chapter. We now propose using Si:O as a semi-insulating substrate on which to fabricate MOS devices. Figure 6.6 is a device structure which we have fabricated to utilize the insulating nature of the oxygen-doped silicon.

Crystalline silicon on top of an insulating layer is advantageous for MOS circuits. The insulating layer provides device isolation without the risk of bipolar latch-up found in CMOS circuits [1]. The insulating layer is also useful for reducing the parasitic capacitances of interconnects and source-substrate and drain-substrate capacitances. Devices with ideal sub-threshold slopes of 60 mV/dec, which is important for switching devices on and off, can also be fabricated by using thin layers, which can be fully depleted, on top of the insulator. Most insulators, however, are amorphous (*e.g.* SiO_2) and make it impossible to grow crystalline silicon directly on top of the insulator. Silicon-on-insulator

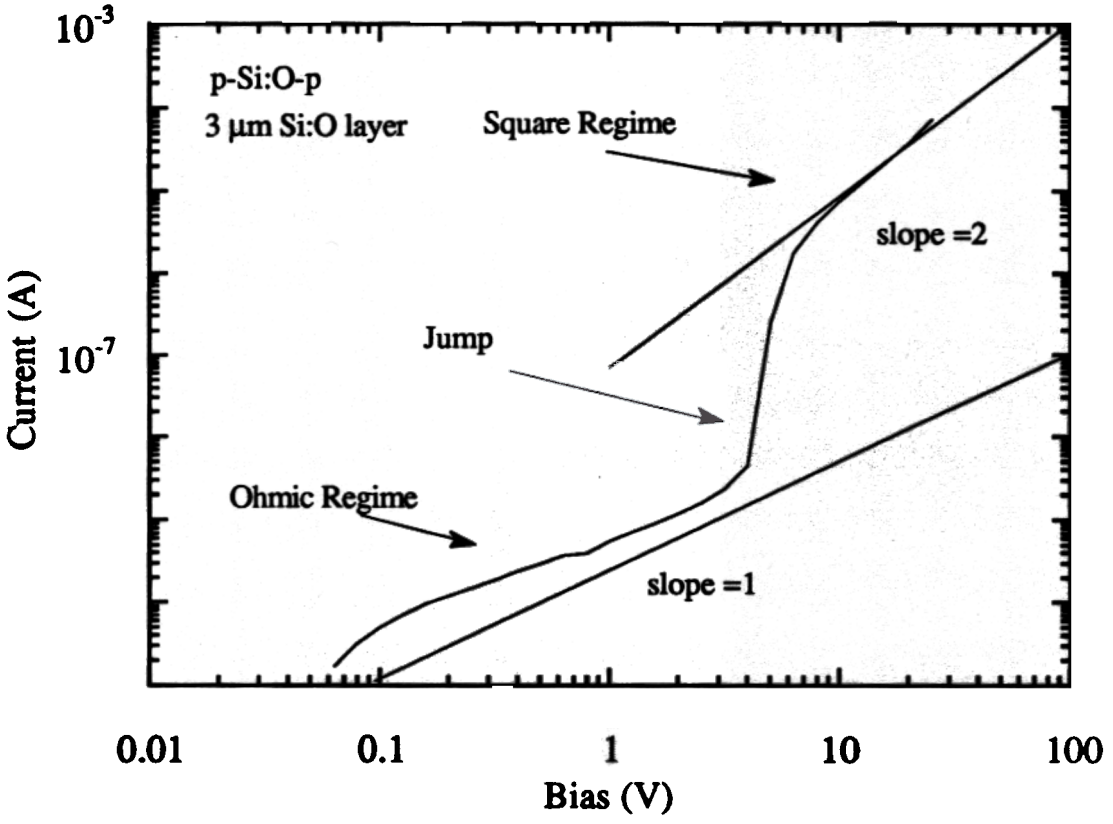


Figure 6.5. Current *vs.* Voltage for a p-i-p structure with a silicon layer doped to 2 x 10^{20} cm^{-3}, with oxygen doped layer forming the intrinsic region. Notice the three regimes; Ohm's Law, "jump" corresponding to trap filling, and square law due to space-charge. The jump indicates a single trap level within the band gap.

devices are now formed by SIMOX (separation by implanted oxygen) [5] or by growing silicon on expensive sapphire substrates

6.4.1 Silicon-on-Si:O Growth

To demonstrate the feasibility of this device structure using Si:O as the insulating layer, we fabricated the device shown in Figure 6.6 using standard MOS processing techniques. We started the growth process with the cleaning sequence and buffer layer sequence discussed in Sec 3.4. For n-channel devices, the buffer layers were doped to about 10^{17} cm^{-3} p-type, and for p-channel devices, the layers were doped 10^{16} cm^{-3} n-type. The DCS and H_2 flow rates were 26 standard cubic centimeters per minute (sccm) and 3 standard liters per minute (slpm), respectively. The temperature of the substrate was then lowered to 750 °C for one minute of growth of silicon (~100 Å). The hydrogen flow was then reduced and stabilized (~10 sec) before the DCS was switched off and the silane switched on. The oxygen-doped layers were grown using 4% SiH_4 in H_2 as the source gas such that the total silane flow was 10 sccm and the total hydrogen flow was 2 slpm.

The oxygen was introduced to the reactor in an Argon carrier (280 ppm O_2 in Ar) gas through a calibrated mass flow controller. The flow of argon was adjusted to give the proper oxygen level. The oxygen was introduced into the reactor 30 sec. after the SiH_4 was injected and was left flowing for the duration of the layer. Typically, a 1.5 μm Si:O layer was used for device isolation (30 min. growth). The oxygen-doped layer was not intentionally doped with phosphorous or boron.

The cap (active) layer was grown at 1000 °C with silane as the source gas. Following the oxygen-doped layer, a 30 sec. silicon layer at 750 °C (using silane) was grown (~ 240 Å) before the temperature was raised to 1000 °C. The active region was grown to a thickness of approximately 0.5 μm (with silane) and doped *in situ* n-type or p-type depending upon the channel required

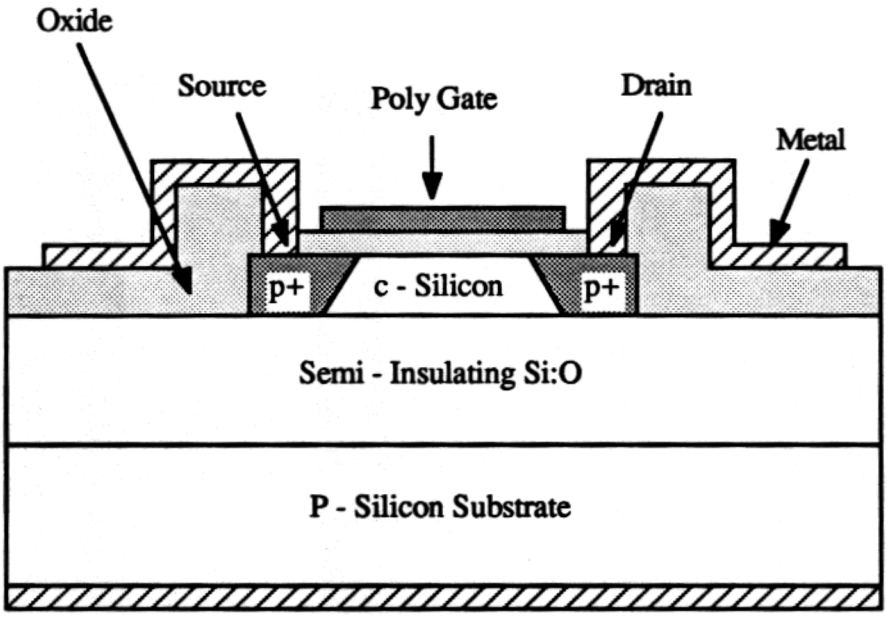


Figure 6.6. Proposed device structure to demonstrate Si:O as a semi-insulating substrate. The oxygen-doped silicon remains crystalline during growth, allowing high quality crystalline silicon (without oxygen) to be grown as the active layer. We fabricated several p-channel and n-channel devices using this structure with gate lengths ranging from 2 μm to 50 μm.

6.4.2 FET Processing

We processed the devices using standard self-aligned SOI-MOS processing techniques. We started by isolating the active areas with a reactive ion etch so that the mesa walls reached the Si:O layer. We then grew the 300 Å gate oxide at 1000 °C in dry O_2 and delivered the wafers to David Sarnoff Laboratories for the poly-crystalline silicon deposition.

Because the Si:O is not a perfect insulator, it conducts when heavily doped. We changed the standard self-aligned gate process slightly to accommodate this situation. We implanted the entire poly-silicon layer for the gate doping before the poly-crystalline silicon etch. The implant conditions were 4×10^{15} cm^{-2} at 100 keV, using boron for the p-channel devices and As for the n-channel devices. We then patterned the gate by reactive ion etching and opened the source and drain contact holes. Another implant was performed under the same conditions as above to define the source and drain regions. To avoid implanting the Si:O in the field regions, the photoresist used to pattern the gate was also used as the implant mask.

The devices were then cleaned thoroughly and the implant damage and gate drive-in anneals were performed simultaneously. The n-channel devices had a 35 min., O_2 anneal at 950 °C while the p-channel devices underwent only a 20 min. anneal in O_2. Oxide was then deposited on the surface at 350 °C and annealed at 600 °C for 30 min. in N_2 The contact holes were then opened and Al evaporated and patterned to finish the devices. Forming gas anneals were needed on some devices to improve the device performance.

Although the structures were not optimized for state-of-the-art performance, the devices fabricated do operate as FET's. Figures 6.7(a) and (b) are families of I-V curves for p-channel FET's with 2 μm gates. Figure 6.7(a) is the Si:O isolated device and 6.7(b) is the bulk silicon wafer (~ 10 ohm-cm resistivity) processed in parallel with the Si:O device. The semi-insulating layer of Fig. 6.7(a) was doped 5×10^{19} cm^{-3} with oxygen. The higher threshold voltage in the Si:O device is due to the doping level in the active

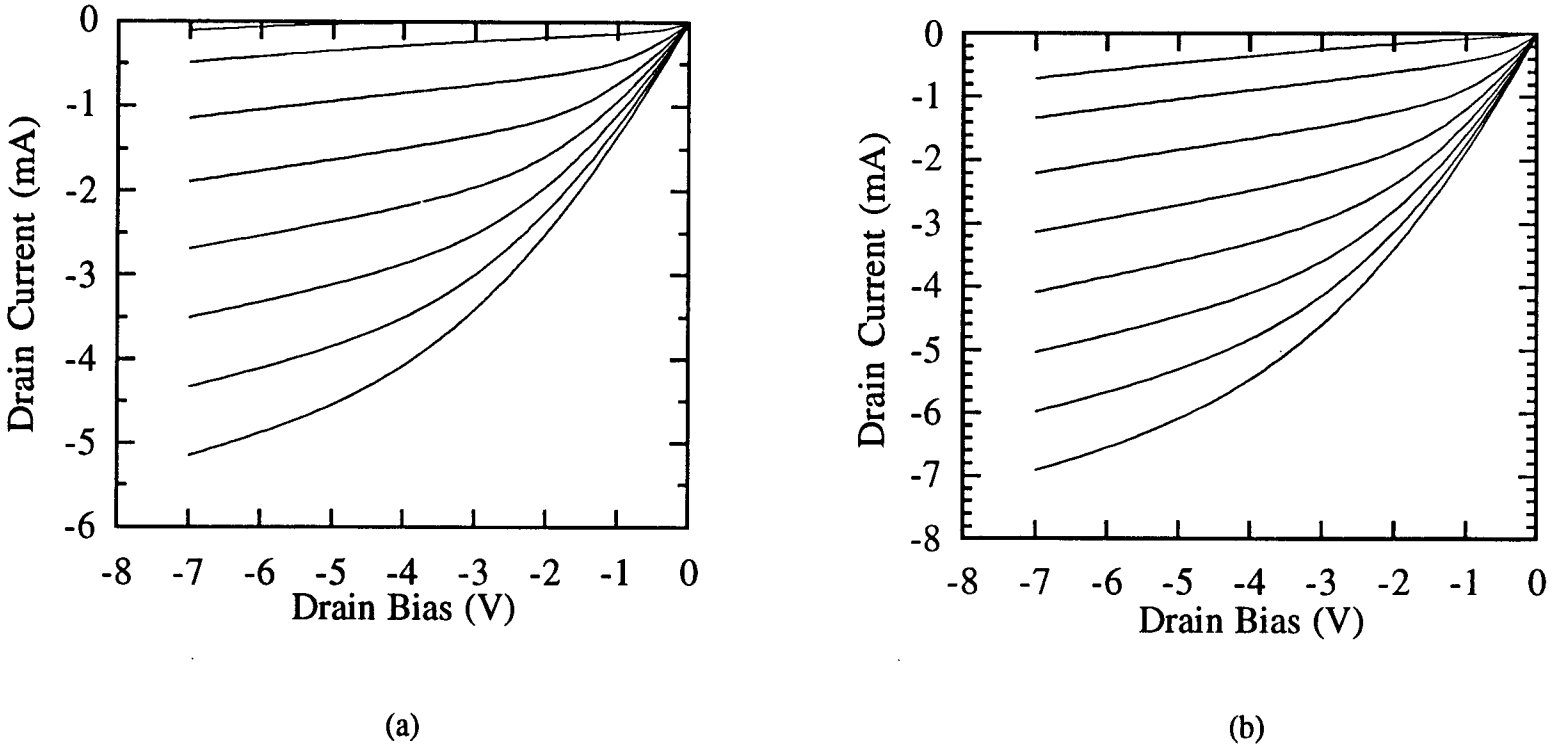


Figure 6.7. MOSFET curves for (a) a 2 μm gate FET in Si on Si:O and (b) a 2 μm gate FET processed on a bulk n-type wafer in parallel with the Si on Si:O. The device widths are 50 μm in both cases. The difference in the threshold voltage is due to the difference in the doping of the active region.

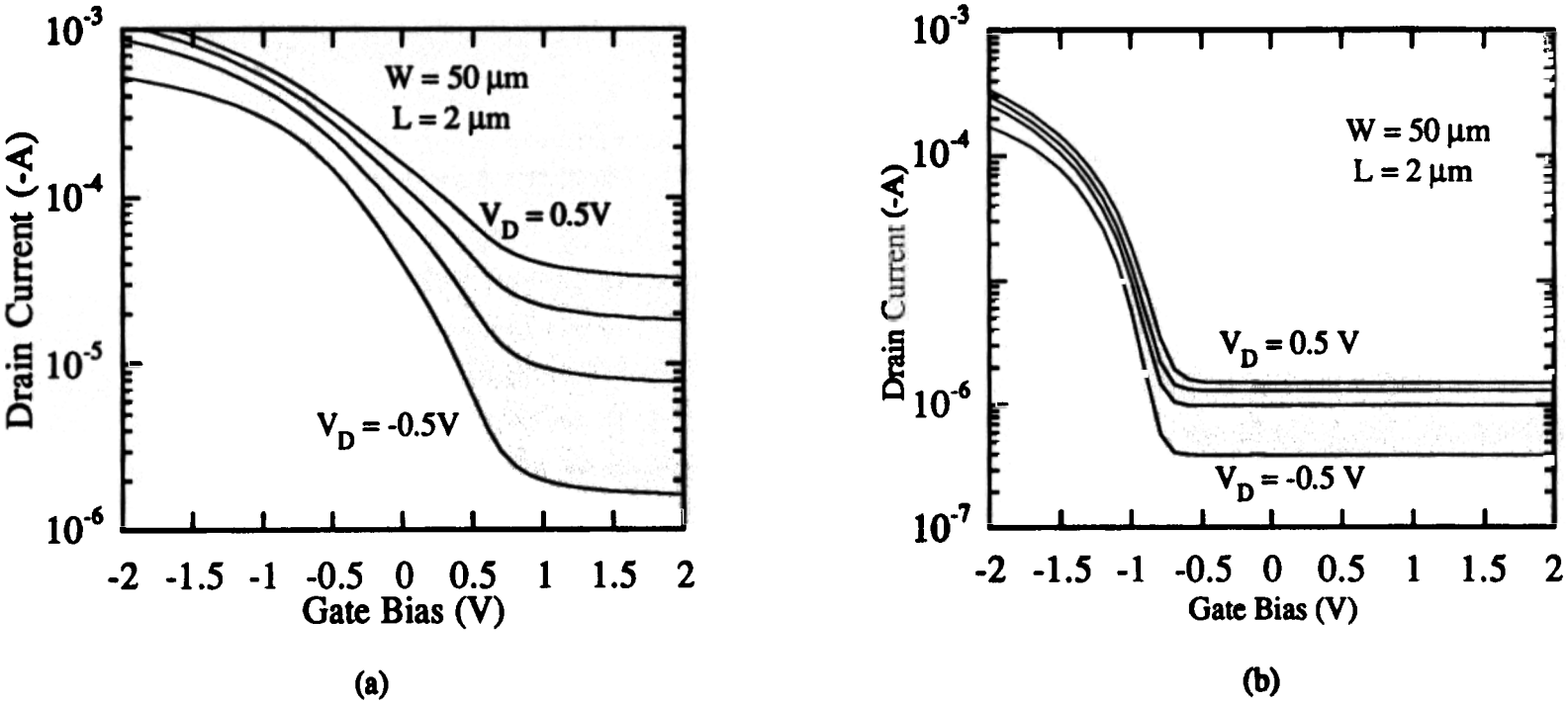


Figure 6.8. Subthreshold characteristics of (a) a MOSFET in Si on Si:O and (b) a MOSFET in bulk silicon. The subthreshold slope of the devices fabricated on Si:O approximately 1000 mV/Dec while the control device is 250 mV/dec.

region. The sub-threshold characteristics are shown in Figures 6.8(a) and (b). We did not design the Si:O structures with optimum parameters, but the devices are comparable (in the active region) to MOSFET's fabricated in parallel on bulk silicon wafers. Both devices have high leakage currents in the off state which means the source is most likely a function of device the processing, not the silicon quality of the SOI. The n-channel devices also had large leakage currents for both the control devices and the test devices.

6.5 Future of Si:O

The possibility of using Si:O as an insulating layer is a potentially exciting field of study. We have already demonstrated the semi-insulating and crystalline features of the material. Now other characteristics must be studied. Some of the characteristics which need to be investigated deal mostly with the advantages inherent to the silicon-on-insulator (SOI) material system.

SOI devices are inherently radiation-hard. Carriers generated deep within the semiconductor by alpha particles are blocked by the insulator and thereby kept from diffusing into the active device areas. Since the Si:O layers contain mid-gap trap levels, these traps may prevent carriers from reaching the active areas as well. SOI also reduces short channel effects in MOSFET's such as preventing punch-through of the source and drain regions. Since the device structure which we fabricated was not optimized to study these effects in the Si:O devices, these effects can remain an area open to study.

There are some characteristics of Si:O which may make it more advantageous than SiO_2 as the under-lying insulator for SOI. Since SiO_2 is an insulator, making contact to the active area substrate is difficult and a self-biasing effect [6] causes a change in the threshold voltage of SOI MOSFET's. Since Si:O is not a perfect insulator, making contact to the active area substrate may be easier. SiO_2 also has poor thermal conductivity (0.014 W/cm/°C) as compared to silicon (0.6 W/cm/°C) [7]. Therefore, heat is not dissipated easily from the active device areas, particularly in bipolar devices in SOI. Since Si:O is

more than 99% silicon, the thermal conductivity should be much larger than amorphous SiO_2 and the power dissipation better than in SOI.

Another potential use for Si:O is as the substrate for high speed metal semiconductor-metal (MSM) photodetectors. In silicon MSM devices, the initial photo-response of the device can be as short as 10 ps, but carriers generated deep within the substrate lead to a long (>100 ps) tail in the recovery time of the devices [8]. By using Si:O as a substrate layer, the carriers generated deep within the substrate may be removed quickly because of the dense populations of traps thereby eliminating the long carrier tail. Preliminary studies of carrier lifetimes by a pump and probe reflection technique [9] show the lifetimes in the Si:O layers doped to 5×10^{19} cm^{-3} with oxygen to be on the order of 10 ps.

6.7 Conclusions

Much work is needed to determine if the Si:O layers truly improve device performance to the same extent as other silicon-on-insulator structures. We have demonstrated the semi-insulating nature of the oxygen-doped silicon films by studying the carrier transport properties in the material. We have shown that the Fermi level is pinned near mid-gap in the silicon and that the films are highly resistive at room temperature. We have also demonstrated electronic devices fabricated in crystalline silicon grown on top of Si:O.

6.8 References

1. K.E. Bean and W.R. Runyan, "Dielectric Isolation: Comprehensive, Current, Future," *J. Electrochem. Soc.* **124**(1), 5C (1977).

2 S.M. Sze, Physics of Semiconductor Devices, 2nd Ed., Wiley, New York (1981).

3 CRC Handbook of Chemistry and Physics, 72nd Ed., (1991 1992).

4 M.A. Lampert and P. Mark, Current Injection in Solids, Academic Press, New York (1970).

5. P.L.F. Hemment, "Silicon on Insulator Formed by O^+ or N^+ Implantation," *Proc Mat. Res. Soc.* **53**, 207 (1986).

6. J. Tihanyi and H. Schlotterer, "Influence of the Floating Substrate Potential on the Characteristics of EFSI MOS Transistors," *Solid State Electr.* **18**, 309 (1975).

7 A.S. Grove, Physics and Technology of Semiconductor Devices, Wiley, New York (1967).

8. Y. Liu, W. Khalil, P.B. Fischer, S.Y. Chou, T.Y. Hsiang, S. Alexandrou and R. Sobolewski, "Nanaoscale Ultrafast Metal-semiconductor-metal Photodetectors," *Dev. Res. Conf.*, Boston (1992).

9 F.E. Doany, D. Grischkowski and C.-C. Chi, "Carrier Lifetime Versus Ion-implantation Dose in Silicon on Sapphire," *Appl. Phys. Lett.* **50**(8), 460 (1987).

Chapter 7

Summary

In the previous six chapters we have described the status of oxygen in epitaxial silicon and silicon-germanium layers grown by low-temperature chemical vapor deposition. The motivation for this study stems from the drive to increase device and circuit performance by improving the electronic material in which the devices are fabricated. Low temperature epitaxy provides a method for growing thin epitaxial layers with abrupt interfaces. It can be used with silicon technology to grow $Si/Si_{1-x}Ge_x$ heterojunctions to improve device performance.

The obstacles associated with low-temperature CVD epitaxial growth techniques are rooted in the stability of oxygen on the silicon surface. We demonstrated that oxygen concentrations far above the peak solid solubility can incorporate into epitaxial silicon and silicon-germanium layers grown at low-temperatures. These high concentrations of oxygen were shown to reduce minority carrier lifetimes in heterojunction bipolar transistors, p-n junction diodes, and MOS capacitors. The short carrier lifetimes associated

with oxygen contamination of silicon-germanium alloys also reduces the non-radiative recombination lifetimes of the carriers in the $Si_{1-x}Ge_x$ layers so that photoluminescence processes are masked.

We also showed that hydrogen passivation of the silicon surface can reduce the probability that oxygen will stick to the growing interface and that the boundary layer can reduce the transport of oxygen to the growth interface, therefore reducing the amount of oxygen incorporating into the growing film. This is a critical advantage of CVD over MBE, and makes CVD possible with oxygen and water partial pressures far in excess of what is predicted by classical surface science studies. We proceeded to show that high-lifetime, low oxygen concentration epitaxial films could, indeed, be grown at low temperature in a non-UHV environment, and that improved device performance resulted.

In Chapter 6, we exploited the electronic properties of oxygen doped silicon films for use as semi-insulating epitaxial layers. We demonstrated the crystalline and semi-insulating nature of these films and showed that we could grow high-quality silicon films with low oxygen concentrations on top of the oxygen doped layers. This structure provides many opportunities for improved device performance such as MOS transistors and high speed photoconductors.

Appendix I

Recombination Currents in P-N Junctions

Here we discuss the different currents associated with recombination in the space-charge region of p-n junctions. As seen in Chapter 5, an extra term, due to recombination in depletion region extending into the narrow band gap base, has been added to the conventional recombination currents. This extra current component has a slope of one ("n = 1") on a semi-logarithmic plot of current *vs.* voltage and is a dominant term if the lifetime in the narrow band gap region is short. The discussion of recombination current is found in detail in Grove (Ref. 1 of Chapter 4).

Recombination within the space-charge region of a p-n junction gives rise to a current component described by:

$$J_{rec} = \int_0^W U\,dx = \int_{-x_n}^0 U\,dx + \int_0^{x_p} U\,dx \qquad [A1.1]$$

where W is the width of the space-charge region, x_n and x_p are the depletion widths on the n- and p-sides of the junction, U the Shockley-Hall-Read (SHR) (see Eqn. 5.2)

recombination equation and J_{rec} the recombination current-density. With the simplifying assumptions of mid-gap traps ($E_t = E_i$) and equal electron and hole capture cross sections ($\sigma_n = \sigma_p = \sigma$) the recombination rate, U, is given by:

$$U = \sigma v_{th} N_t \frac{pn - n_i^2}{n + p + 2n_i} \qquad \text{[A1.2].}$$

Under the assumption of quasi-equilibrium (quasi-Fermi levels constant), the electron hole product is constant throughout the space charge region and is given by:

$$pn = n_i^2 \exp\left(\frac{q|V_F|}{kT}\right) \qquad \text{[A1.3]}$$

where V_F is the forward bias voltage.

For a given forward bias, U will have a maximum value at the location in the space-charge region where n = p since np is a constant. This condition is satisfied where the intrinsic Fermi level (E_i) is halfway between the quasi-Fermi levels for the holes and the electrons, therefore, the carrier concentrations are given by:

$$n = p = n_i \exp\left(\frac{q|V_F|}{2kT}\right) \qquad \text{[A1.4]}$$

and hence, U_{max} is given by:

$$U_{max} = \sigma v_{th} N_t \frac{n_i^2\left(\exp\left(\frac{q|V_F|}{kT}\right) - 1\right)}{2n_i\left(\exp\left(\frac{q|V_F|}{2kT}\right) + 1\right)} \qquad \text{[A1.5]}$$

or for $V_F \gg kT$:

$$U_{max} = \frac{1}{2}\frac{n_i}{\tau_o}\exp\left(\frac{q|V_F|}{2kT}\right) \qquad \text{[A1.6]}$$

where $\tau_o = \sigma v_{th} N_t$ and is the carrier lifetime. Assuming that the lifetime is the same on both sides of the junction, the approximation to the integral in Eqn. A1.1 gives the standard current associated with recombination within the space charge region of a p-n junction, and is written:

$$J_{rec} \approx \frac{1}{2}\frac{qn_i}{\tau_o} W \exp\left(\frac{q|V_F|}{2kT}\right) \qquad \text{[A1.7]}$$

which is an "n=2" current as discussed in Chapter 5.

In the case where the lifetime is different on the two sides of the p-n junction, the integral of Eqn. A1 must be evaluated separately on either side of the junction. In the case of a bipolar transistor we separate the integral of Eqn. A1.1 into two integrals, one over the depletion region extending into the emitter, and the other integral over the depletion region extending into the base. See Figure A1.1

In the case of the npn heterojunction bipolar transistor with a narrow band gap base, the base region is more heavily doped than the emitter ($N_B \approx 100\, N_E$) and most of the depletion region extends into the n-type emitter ($W \approx x_n \gg x_p$). Therefore, the condition where n = p occurs in the emitter region and the integral over the n-depletion region can be approximated by Eqn. A1.7. This term is denoted I_{b4} in Eqn. 5.6.

The integral over the depletion region extending into the p-type base yields a separate recombination term. In the narrow band gap material of the base, the hole concentration is much greater than the electron and intrinsic carrier concentrations ($p \gg n, n_i$). Therefore the simplification to the SHR equation becomes:

$$U \approx \frac{1}{2}\frac{n}{\tau_{BE}} \qquad \text{[A1.8]}$$

where τ_{BE} is the lifetime in the narrow band gap base region and is different than the lifetime in the wider band gap emitter. This simplification leads to the "n=1" current component of Eqn. 5.6. The carriers are accounted for by the potential which is assumed to vary linearly across the depletion region extending into the base. The integration over the depletion region extending into the heavily doped base region then leads to the following expression for the recombination current:

$$J_{rec} \approx \frac{1.7\, x_p\, n_i^2{}_{base}}{\tau_{BE}\, N_B} \exp\left(\frac{q|V_F|}{kT}\right) \qquad \text{[A1.9]}$$

We have assumed that the base doping is 70 times larger than the emitter doping which leads to the constant 1.7 term in the numerator. (The base to emitter doping-ratio was taken from King in Ref. 3 in Chapter 5 whereby giving the same expression described by King). This expression is the "n=1" term designated I_{b3} in Eqn. 5.6 and is a dominant

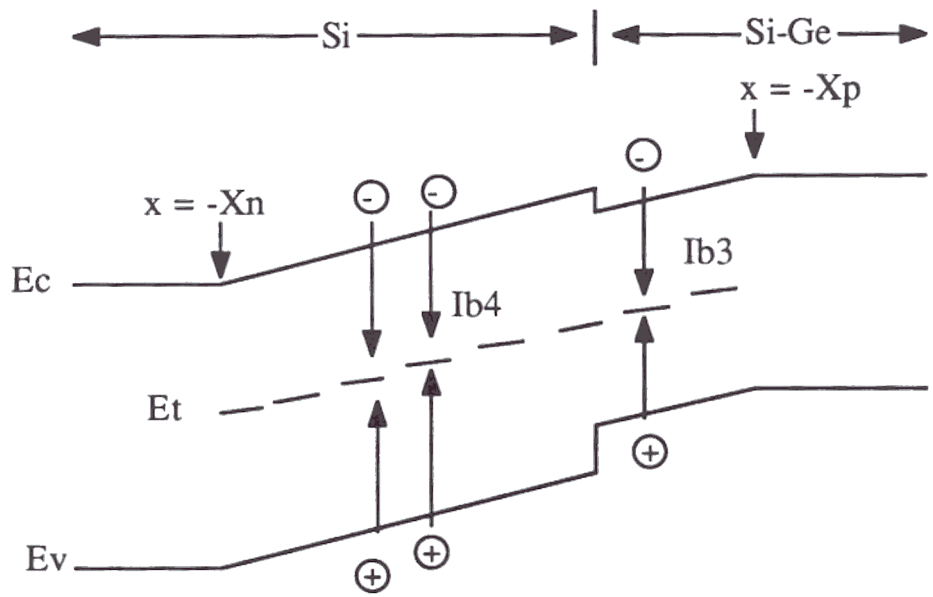


Figure AI.1. Expanded view of recombination in the space charge region. I_{b4} is the recombination in the lightly doped emitter side of the junction while I_{b3} is due to recombination in the depletion region on the heavily-doped, narrow-gap side of the junction. For I_{b3} to dominate, the lifetime in the heavily doped material must be much shorter than the lifetime in the lightly doped material. This condition yield an "n=1" base current.

term for recombination current if τ_{BE} is much shorter than the other lifetimes in the device. This "n=1" current is characteristic of a short lifetime on the heavily doped side of the p-n junction and is not limited to heterojunctions or heterojunction bipolar transistors.

Appendix II

Publications and Presentations Related to this Work

Journals

1. J.C. Sturm, X. Xiao, P.V. Schwartz, C.W. Liu, L.C. Lenchyshyn, and M.L.W. Thewalt, *to be published in J. Vac. Sci. and Tech.* **B10** (4), July/Aug (1992).

2 L.C. Lenchyshyn, M.L.W. Thewalt, J.C. Sturm, P.V. Schwartz, E.J. Prinz, N.L. Rowell, J.-P. Noël, and D.C. Houghton, "High Quantum Efficiency Photoluminescence from Localized Excitons in $Si_{1-x}Ge_x$," *Applied Physics Letters* **60**(25), 3174 (1992).

3. V. Venkataraman, P.V.Schwartz and J.C. Sturm, "Symmetric $Si/Si_{1-x}Ge_x$ Two-dimensional Hole Gases Grown by Rapid Thermal Chemical Vapor Deposition," *Applied Physics Letters* **59**(22), 2871 (1991).

4. J.C. Sturm, P.V. Schwartz and E.J. Prinz, "Growth of $Si_{1-x}Ge_x$ by Rapid Thermal Chemical Vapor Deposition and Applications to Heterojunction Bipolar Transistors," *J. Vac. Sci. and Tech.* **B9**, 2011 (1991).

5. Z. Matutinovic-Krstelj, E.J. Prinz, P.V. Schwartz and J.C. Sturm, "Reduction of the p^+-n^+ Junction Tunneling Current for Base Current Improvement in Si/SiGe/Si Heterojunction Bipolar Transistors," *IEEE Electron Device Letters* **EDL-12**(4), 163 (1991).

6. X. Xiao, J.C. Sturm, K.K. Goel and P.V. Schwartz, "Fabry-Perot Optical Light Modulator at 1.3 μm in Silicon," *IEEE Photonics Technology Letters* 3(3), 230 (1991).

7. J.C. Sturm, P.M. Garone and P.V. Schwartz, "Temperature Control of Silicon-germanium Alloy Epitaxial Growth on Silicon Substrates by Infrared Transmission," *Journal of Applied Physics* 69(1) (1991).

8 E.J. Prinz, P.M.Garone, P.V. Schwartz, X. Xiao and J.C. Sturm, "The Effects of Base Dopant Outdiffusion and Undoped $Si_{1-x}Ge_x$ Junction Spacer Layers in $Si/Si_{1-x}Ge_x/Si$ Heterojunction Bipolar Transistors," *IEEE Electron Device Letters* **ED12-2**, 42(1991).

9. J.C. Sturm, P.V. Schwartz and P.M. Garone, "*In-situ* Temperature Measurement by Infrared Absorption for Low-temperature Epitaxial Growth of Homo- and Hetero-epitaxial Layers on Silicon," *Journal of Electronic Materials* 19(10), 1051-1054 (1990).

10. P.V. Schwartz and J.C. Sturm, "Microsecond Carrier Lifetimes in Strained Silicon-germanium Alloys Grown by Rapid Thermal Chemical Vapor Deposition," *Applied Physics Letters* 57(19), 2004-2006 (1990).

11. P.M. Garone, J.C. Sturm, P.V. Schwartz, S.A. Schwarz and B. Wilkens, "Silicon Vapor-phase Epitaxial Growth Catalysis by the Presence of Germane," *Applied Physics Letters* 56, 1275 (1990).

12. J.C. Sturm, P.V. Schwartz and P.M. Garone, "Silicon Temperature Measurement by Infrared Transmission for Rapid Thermal Processing Applications," *Applied Physics Letters* 56, 961 (1990).

3. J.C. Sturm, E.J. Prinz, P.M. Garone and P.V. Schwartz, "Bandgap Shifts in Silicon-germanium Heterojunction Bipolar Transistors," *Applied Physics Letters* 54, 2707-2709 (1989).

Conferences

1. P.V. Schwartz, C.W. Liu, J.C. Sturm, T. Gong and P.M. Fauchet, "Current Transport Properties of Semi-Insulating Oxygen-Doped Silicon Films for Use in High Speed Photoconductive Switches," *Electronic Materials Conference,* Boston, MA (1992).

2. E.J. Prinz, X. Xiao, P.V. Schwartz and J.C. Sturm, "A Novel Double Base Heterojunction Bipolar Transistor for Low Temperature Bipolar Logic,"*Device Research Conference,* Boston, MA (1992)

3. L.C. Lenchyshyn, M.L.W. Thewalt, J.C. Sturm, P.V. Schwartz, E.J. Prinz, N.L. Rowell, J.-P. Noël, and D.C. Houghton, "Photoluminescence Spectroscopy of Localized Excitons in $Si_{1-x}Ge_x$," *Electronic Material Conference,* Boston, MA (1992).

4. C.W. Liu, J.C. Sturm, P.V. Schwartz and E.A. Fitzgerald, "Misfit Dislocation Nucleation Mechanisms and Metastability Enhancement of Selective $Si_{1-x}Ge_x/Si$ Grown by Rapid Thermal Chemical Vapor Deposition," *Proc. Symp. Mat. Res. Soc.* 238 (1992).

5. J.C. Sturm, Q. Mi, X. Xiao and P.V. Schwartz, " Well Resolved Band-edge Photo- and Electro-luminescence in Strained $Si_{1-x}Ge_x$ Quantum Wells and Superlattices," *Proc. Int. Conf. on Solid State Devices and Materials*, in press (1991).

6. J.C. Sturm, P.V. Schwartz, H. Manoharan, X. Xiao and Q. Mi, " High Lifetime Strained $Si_{1-x}Ge_x$ Films Grown by Rapid Thermal Chemical Vapor Deposition," *Proc. Symp. European Material Research Society* (1991).

7. J.C. Sturm, P. Prucnal, Y-M. Liu, H. Manoharan, Q. Mi, P.V. Schwartz and X. Xiao, "Applications of $Si_{1-x}Ge_x$ Strained Layer Alloys for Silicon-based Optical Interconnects," *Proc. IEEE Sarnoff Symp.* (1991).

8. J.C. Sturm, P.V. Schwartz and P.M.Garone, "Non-invasive Silicon Temperature Measurement by Infrared Transmission for Rapid Thermal Processing Applications," *Proc. Symp. on VLSI Tech.* **10**, 107-119 (1991).

9. J.C. Sturm, Q. Mi, P.V. Schwartz and H. Manoharan, "Band-Edge Exciton Photoluminescence in Strained Silicon-Germanium Alloy Films Grown by Rapid Thermal Chemical Vapor Deposition" *Presented Electronic Materials Conference* Boulder, CO (1991).

10 Z. Matutinovic-Krstelj, E.J. Prinz, P.V. Schwartz and J.C. Sturm, "Reduction of the p^+-n^+ Junction Tunneling Current for Base Current Improvement in Si/SiGe/Si Heterojunction Bipolar Transistors," *Proc. Mat. Res. Soc.* **220**, (1991).

11. J.C. Sturm, P.V. Schwartz, H. Manoharan, Q. Mi, L.C. Lenchyshyn, M.L.W. Thewalt, N.L. Rowell, J.-P. Noël, and D.C. Houghton, "Well-Resolved Band-Edge Photoluminescence from Strained $Si_{1-x}Ge_x$Layers Grown by Rapid Thermal Chemical Vapor Deposition," *Proc. Symp. Mat. Res. Soc.* **220**, (1991).

12. X. Xiao, K.K. Goel, J.C. Sturm and P. V. Schwartz, "Data Transmission at 1.3μm using Silicon Spatial Light Modulator", *Proc. SPIE Symp.* **1476** in press (1991).

13. J.C. Sturm, P. V. Schwartz, E.J. Prinz and C.W. Magee, "Control of Oxygen Incorporation and Lifetime Measurements in $Si_{1-x}Ge_x$ Epitaxial Films Grown by Rapid Thermal Chemical Vapor Deposition," *Proc. SPIE Conf. on Rapid Thermal Processing*, **1393**, 252-259 (1990).

14. X. Xiao, J.C. Sturm, P.V. Schwartz and K.K. Goel, "Vertical 1.3μm Optical Modulator in Silicon-On-Insulator," *Proc. 1990 IEEE SOS/SOI Technology Conference*, 192, Key West, FL, October (1990).

15 J.C. Sturm, H. Manoharan, V. Venkataraman, P.V. Schwartz and P.M. Garone, "Control of Individual Layer Growth Temperatures by Rapid Temperature Switching in $Si_{1-x}Ge_x$ Multilayer Structures Grown by Rapid Thermal Chemical Vapor Deposition," *Proc. Inter. Conf.on Elec. Mat.*,(1990).

16. J.C. Sturm, P.M. Garone, E.J. Prinz, P.V. Schwartz and V. Venkataraman, "Interface Abruptness in Epitaxial Silicon and Silicon-Germanium Structures Grown by Rapid Thermal Chemical Vapor Deposition," *Proc. Int. Conf. on CVD XI* **90-12**, 295 (1990).

17. J.C. Sturm, E.J. Prinz, P.V. Schwartz, P.M. Garone and Z. Matutinovic, "Growth and Transistor Applications of $Si_{1-x}Ge_x$ Structures by Rapid Thermal Chemical Vapor Deposition," *Proc. Topical Symposium on Silicon Based Heterostructures*, Toronto, Canada (1990).

18 P.V. Schwartz, J.C. Sturm and C.W. Magee, "Reduction of Oxygen Incorporation and Lifetime Measurements in Epitaxial $Si_{1-x}Ge_x$ Films Grown by Low Temperature Rapid Thermal CVD," *Electr. Mater. Conf.*, Santa Barbara, CA (1990).

19. J.C. Sturm, P.V. Schwartz and P.M. Garone, "Temperature Measurement by Infrared Transmission for Rapid Thermal Processing Applications," *Proc. Symp. Mat. Res. Soc.* **157**, (1990).

20. P.V. Schwartz, J.C. Sturm and P.M. Garone, "Extreme Supersaturation of Oxygen in Low Temperature Epitaxial Silicon and Silicon-germanium Alloys," *Proc. Symp. Mat. Res. Soc.* **163**, (1990).

21 E.J. Prinz, P.M. Garone, P.V. Schwartz, X. Xiao and J.C. Sturm, "The Effect of Base-emitter Spacers and Strain-dependent densities of States in $Si/Si_{1-x}Ge_x/Si$ Heterojunction Bipolar Transistors," *IEDM Technical Digest*, 639 (1989).

22. J.C. Sturm, P.V. Schwartz and P.M. Garone,"Oxygen Incorporation in Low Temperature (625 - 800 °C) Silicon and Silicon-Germanium Epitaxial Layers Grown By Vapor Phase Techniques in a Non-UHV System," *Elect. Mater. Conf.*, Cambridge, MA (1989).

23. P.M. Garone, P.V. Schwartz and J.C. Sturm, "Growth Rate and Doping Kinetics in Silicon-germanium Films Grown by Limited Reaction Processing," *Proc. Symp. Mat. Res. Soc.* **146**, 41 (1989).

24. J.C. Sturm, X. Xiao, P.M. Garone and P.V. Schwartz, "Electron-Beam-Induced-Current (EBIC) Imaging of Defects in $Si_{1-x}Ge_x$ Multilayer Structures," *Proc. Symp. Mat. Res. Soc.* **148**, 341 (1989).

25 J.C. Sturm, E.J. Prinz, P.M. Garone and P.V. Schwartz, "Electron Transport in Silicon-Germanium Strained-layer Heterojunction Bipolar Transistors," *American Physical Society Meeting*, St. Louis, MO (March 1989).