STABILITY OF AMORPHOUS SILICON THIN FILM TRANSISTORS AND CIRCUITS

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Abstract

Hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) have been widely used for the active-matrix addressing of flat panel displays, optical scanners and sensors. Extending the application of the a-Si TFTs from switches to current sources, which requires continuous operation such as for active-matrix organic light-emitting-diode (AMOLED) pixels, makes stability a critical issue.

This thesis first presents a two-stage model for the stability characterization and reliable lifetime prediction for highly stable a-Si TFTs under low gate-field stress. Two stages of the threshold voltage shift are identified from the decrease of the drain saturation current under low-gate field. The first initial stage dominates up to hours or days near room temperature. It can be characterized with a stretched-exponential model, with the underlying physical mechanism of charge trapping in the gate dielectric. The second stage dominates in the long term and then saturates. It corresponds to the breaking of weak bonds in the amorphous silicon. It can be modeled with a "unified stretched exponential fit," in which a thermalization energy is used to unify experimental measurements of drain current decay at different temperatures into a single curve.

Two groups of experiments were conducted to reduce the drain current instability of a-Si TFTs under prolonged gate bias. Deposition conditions for the silicon nitride (SiN_x) gate insulator and the a-Si channel layer were varied, and TFTs were fabricated with all reactive ion etching steps, or with all wet etching steps, the latter in a new process. The two-stage model that unites charge trapping in the SiN_x gate dielectric and defect generation in the a-Si channel was used to interpret the experimental results. We identified the optimal substrate temperature, gas flow ratios, and RF deposition power densities. The stability of the a-Si channel depends also on the deposition conditions for the underlying SiN_x gate insulator. TFTs made with wet etching are more stable than TFTs made with reactive ion etching. Combining the various improvements raised the extrapolated 50% decay time of the drain current of back channel passivated dry-etched TFTs under continuous operation at 20°C from 3.3×10^4 sec (9.2 hours) to 4.4×10^7 sec (1.4 years). The 50% lifetime can be further improved by ~2 times through wet etching process.

Two assumptions in the two-stage model were revisited. First, the distribution of the gap state density in a-Si was obtained with the field-effect technique. The redistribution of the gap state density after low-gate field stress supports the idea that defect creation in a-Si dominates in the

long term. Second, the drain-bias dependence of drain current degradation was measured and modeled. The unified stretched exponential was validated for a-Si TFTs operating in saturation.

Finally, a new 3-TFT voltage-programmed pixel circuit with an in-pixel current source is presented. This circuit is largely insensitive to the TFT threshold voltage shift. The fabricated pixel circuit provides organic light-emitting diode (OLED) currents ranging from 25 nA to 2.9 μA, an on/off ratio of 116 at typical quarter graphics display resolution (QVGA) display timing. The overall conclusion of this thesis research is that the operating life of a-Si TFTs can be quite long, and that these transistors can expect to find yet more applications in large area electronics.

Acknowledgement

My PhD study at Princeton is one of the most rewarding experiences that I have had in my life and will always be in my memory. There are many people I would like to thank who have given me incredible help and support throughout half a decade in Princeton. I will start off by first thanking my advisor Prof. James C. Sturm for his invaluable guidance, enlightening insight, unwavering support and perpetual encouragement. He is an advocate to cultivate independent researchers and encourages students to realize their dreams. His liberal style of mentoring allows me to study at my own pace and explore the fields of my interest. It is my lifetime fortune to have him as my advisor.

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Table of Contents

Abstract i

Acknowledgement iii

Chapter 1 Introduction 1

1.1 Thin-film transistors for large-area electronics 1

1.2 Stability issue in TFT technologies 3

1.3 Thesis outline 5

Chapter 2 Amorphous-Silicon Thin-Film Transistors 8

2.1 Basic properties of a-Si 8

2.1.1 Atomic structure 8

2.1.2 Density of states 10

2.1.3 Electronic transport 13

2.1.4 Metastability 14

2.2 Structures and operation principle of a-Si TFTs 17

2.2.1 Bottom-gate structure 17

2.2.2 Operation of a-Si TFTs 19

2.2.3 Characterization of a-Si TFTs 21

Chapter 3 Fabrication of Amorphous-Silicon Thin-Film Transistors 27

3.1 PECVD growth of thin films in a-Si TFTs 27

3.1.2 Parameters in PECVD growth 27

3.1.3 a-Si growth 28

3.1.4 SiN_x growth 32

3.2 Dry-etch and wet-etch fabrication process flows 35

3.3 Comparison of dry-etch and wet-etch processes 42

Chapter 4 Two-Stage Model for Lifetime Prediction of Highly Stable a-Si TFTs 45
4.1. Instability mechanisms in a-Si TFTs 45
4.1.1 Modeling defect creation in a-Si 45
4.1.2 Modeling charge trapping in the gate SiNx 52
4.1.3 Summary of instability models for a-Si TFTs 53
4.2. Sample preparation and bias-temperature-stress measurement 54
4.3. Two-stage model for lifetime prediction 55
4.3.1 Single stretched-exponential fit 56
4.3.2 Unification of time and temperature 57
4.3.3 Unified stretched exponential fit (Stage II model) 58
4.3.4 Two-stage model 60
4.4. Discussion 62
4.5. Summary and conclusion 65
Chapter 5 Optimization of Fabrication Conditions for Highly Stable a-Si TFTs 69
5.1. Introduction 69
5.2. Effects of deposition conditions on a-Si TFT stability 70
5.2.1 SiN_x gate insulator deposition 73
5.2.2 a-Si channel layer deposition 74
5.2.3 Discussion 76
5.3. The stability of wet and dry-etched TFTs 77
5.3.1 DC characteristics comparison 77
5.3.2 Comparison of dry and wet-etched a-Si TFTs 78
5.3.3 Discussion 81
5.4. Summary and conclusion 81

Chapter 6 Redistribution of Gap State Density after Low Gate-Field Stress 86

6.1. Theory of field-effect technique to determine gap state density 86

6.1.1 Assumptions and approximations 86

6.1.2 Determination of gap state density.. 88

6.1.3 Relation between gate voltage and surface potential [9].............................. 89

6.1.4 Sheet conductance calculation 89

6.2. Sample preparation and measurement 90

6.3. Experiment results and gap state density determination 90

6.4. Discussion.. 93

6.5. Summary and conclusion.. 95

Chapter 7 Drain-Bias Dependence of Drain Current Degradation 99

7.1. Modeling of threshold voltage shift with drain-bias 100

7.2. Numerical simulation of drain current degradation.. 101

7.3. Analytical solution of drain current degradation.. 103

7.4. Experimental and modeling results 104

7.5. Discussion.. 107

7.6. Summary and conclusion.. 112

Chapter 8 3-TFT Highly Stable OLED Pixel Circuit with In-pixel Current Source 114

8.1. Pixel circuit operation... 114

8.2. Pixel circuit fabrication and characterization 117

8.3. Stability analysis and preliminary experimental results 120

8.4. Summary and conclusion.. 122

Chapter 9 Summary and Future Work 125
9.1. Summary 125
9.2. Future work 126
Appendix A Publications and Presentations from Thesis Research 128
A.1. Journal and conference publications 128
A.2. Conference presentations 129
Appendix B Substrate temperature Calibration 131

Introduction

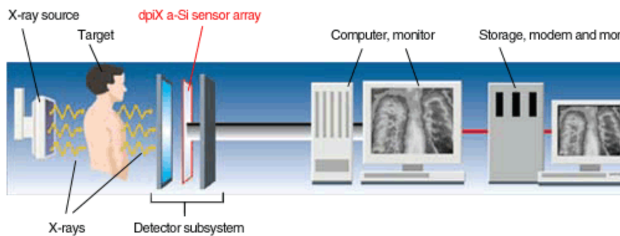
This chapter introduces the motivation behind the work presented in this thesis and the organization of the thesis chapters. Thin-film transistors (TFTs) for large-area electronics and in particular the stability requirement will be briefly reviewed. The stability issue is a common challenge that all new TFT technologies are facing.

1.1 *Thin-film transistors for large-area electronics*

Large-area electronics is a rapid growing field expected to impact all aspects of human life such as energy, health and the environment. Large area applications include but are not limited to: switching and driving devices for active matrix flat panel displays (AMFPDs) based on liquid crystal pixels (AMLCDs) and organic light emitting diodes (AMOLEDs), medical imagers, pressure sensors, low-power communication and energy harvesting [1] (Fig. 1.1). The flat-panel display industry is currently the largest industry in the field of large-area electronics – a market worth in excess of $90Bn (source: DisplaySearch Inc). Thin-film transistors (TFTs) have in the past 20 years become the “rice” of the electronic flat panel industry, just as silicon chips were earlier the “rice” of the electronic computer revolution [2]. At present, the entrenched technology in large area electronics applications, especially the backplanes of AMLCDs, is based on TFTs comprising hydrogenated amorphous silicon (a-Si:H) active layers [3]. However, as the applications for large-area electronics expand, other TFT technologies, like polycrystalline silicon (poly-Si), microcrystalline silicon (μc-Si), organic semiconductors and metal oxides draw growing attention from researchers. Comparion of different TFT technologies is summerized in Table 1-I. Although different large area applications require different performance standards, the general guidelines for the requirements of TFTs in large area electronics are: low processing temperature (~300°C for glass substrates, ~350°C for metal foil substrates and ~150°C for plastic substrates), low leakage current, high on/off ratio, low voltage operation, small area, high uniformity and high stability [4]. Among all these requirements, stability is always important for a new TFT technology to get commercialized.

Sharp 108” AMLCD TV [5]

Samsung flexible AMOLED display [6]



dpiX amorphous silicon (a-Si) X-ray image sensor [7]

E-skin with pressure sensors [1]

Prototype for low-power communication [8]

Nellis Air Force Solar Power Plant, Nevada, USA [9]

Fig. 1.1. Large area applications including AMLCDs, AMOLEDs, medical imagers, pressure sensors, low-power communication and energy harvesting.

Table 1-I. Comparison of different TFT technologies [4, 10, 11]

Attribute	**a-Si**	**μc-Si**	**Poly-Si**	**organic**	**Metal oxides**
Circuit type	NMOS	NMOS / PMOS	NMOS / PMOS	PMOS	NMOS
Mobility	low	higher than a-Si	high	low	high
Stability	issue	stable	stable	issue	under investigation
Uniformity	high	potentially high	improving	improving	high
Manufacturability	mature	RF PECVD?	new	has potential	has potential
Cost	low	low	high	potentially low	Low
Flexible substrate	promising	promising	uncertain	promising	promising

1.2 *Stability issue in TFT technologies*

While the a-Si TFT has long been the workhorse in the AMLCD industry, its stability issue becomes the bottleneck that hinders its further application in large-area electronics. Under positive gate bias, the threshold voltage of a-Si TFTs increases with time due to charge trapping in the gate nitride and defect creation in the a-Si channel [12]. This problem is not critial in AMLCDs since LCDs are non-conducting and switching TFTs in LCD pixels are working in operation with only ~0.1% duty cycle. However, the threshold voltage instability becomes serious when the TFTs are needed for accurate current supply or measurements, such as in the pixels of AMOLED displays and x-ray image sensors. In particular, the AMOLED pixels operate in DC and the OLED current depends directly and continuously on the TFT threshold voltage. Therefore as the threshold voltage increases, the OLED current supplied by the TFTs and thus the pixel brightness drops. This leads to various issues including the distortion of color balance in pixels, which is a serious problem [13] because human eyes are sensitive to the brightness drop and can detect a degradation of only 5% (Fig. 1.2).

From Table 1-I, a-Si is not the only TFT technology that is confronted with the stability issue. The emerging and fast growing organic and metal oxide TFTs also need to be proven stable to survive in the field of large area electronics.

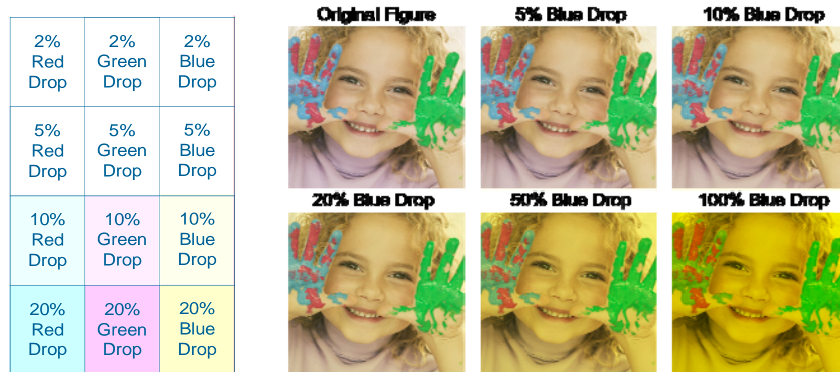


Fig. 1.2. The degradation of white color as a result of the drop of one of the blue, red and green components with respect to the others; (b) The figure discoloration [13]

This thesis focuses on the stability of a-Si TFTs for the following reasons:

- Resolving the stability issue of a-Si enables the mainstream a-Si TFT production infrastructure to be used for the emerging applications instead of requiring a new infrastructure employing new materials [13];
- Highly stable a-Si TFTs with extrapolated DC saturation current half-life of 100 to 1000 years from room temperature measurements outperforms organic and metal oxide TFTs (Fig. 1.3) [14] and make a-Si TFTs promising to stay in the play ground of large area electronics;
- The stability analyzing and optimizing method of a-Si can be applied to other TFT technologies, because the instability mechanisms can be common.

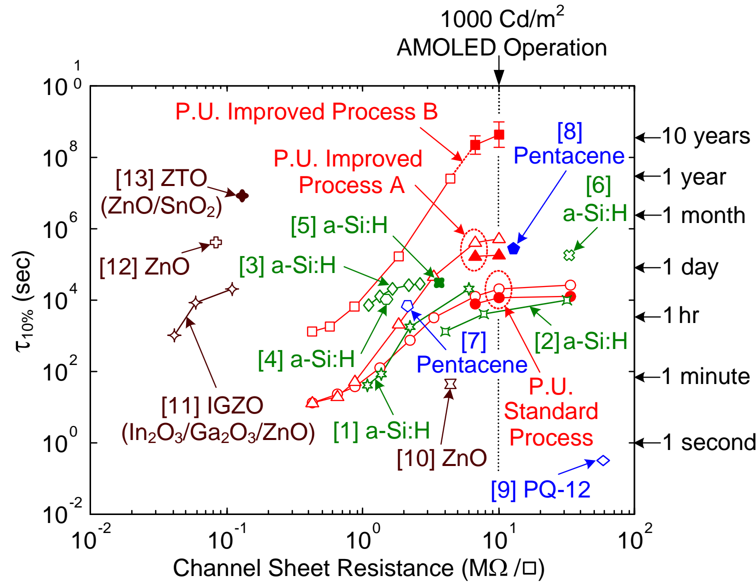


Fig. 1.3. The 10% color decay lifetime vs channel sheet resistance for a-Si, organic and metal oxide TFT technologies (P.U. refers to "Princeton University") [14]

1.3 *Thesis outline*

The topic of this thesis is stability characterization, optimization and circuit compensation for a-Si TFTs.

Chapter 2 introduces a basic knowledge of a-Si and a-Si TFTs, with focuses on the stability related properties of a-Si and the bottom-gate back-channel passivated (BCP) structured a-Si TFTs and their operation principles.

Chapter 3 emphasizes on the fabrication of the a-Si TFTs. It presents the PECVD growth of silicon nitride (SiN_x) and a-Si layers. Then a new full wet-etch fabrication process that has the same deposition steps as the dry-etch process is introduced along with the dry-etch process.

Chapter 4 develops a two-stage model for lifetime prediction of highly stable a-Si TFTs under low-gate field stress. This model is based on the physical mechanisms in a-Si and SiN_x instability and can be used as a relible tool to quantify the stability of a-Si TFTs.

Chapter 5 applies the two-stage model to characterize the stability of a-Si TFTs fabricated with different deposition conditions and etching methods. It provides guidance to optimize fabrication conditions for highly stable a-Si TFTs.

Chapter 6 and Chapter 7 discuss two important assumptions for the two-stage model. In Chapter 6, the gap state density in a-Si before and after low gate-field stress is determined from the field-effect technique. The redistribution of the gap state density after the gate-field stress proves that defect creation occurs in a-Si TFTs under low gate-field stress. Chapter 7 calculates the drain current degradation under both drain and gate bias, without assuming the channel is uniform as in Chapter 4 when the two-stage model is developed.

Chapter 8 presents a new 3-TFT voltage-programmed pixel circuit with an in-pixel current source. This circuit is largely insensitive to the TFT threshold voltage shift and can be used to further promote the application of a-Si TFTs in AMOLED displays.

Chapter 9 summarizes the thesis and makes suggestions for future work in this area.

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Amorphous-Silicon Thin-Film Transistors

Amorphous silicon thin-film transistors (a-Si TFTs) have been widely used in the active-matrix addressing circuits in flat panel displays, optical scanners and x-ray image sensors [1, 2] since their first demonstration in 1976 by Madan, LeComber and Spear [3]. This chapter briefly reviews the fundamental knowledge and concepts that will be further discussed in the thesis, starting first with an overview of the basic properties of a-Si, with emphasis on the stability-related properties. Subsequently, the typical structures of a-Si TFTs are introduced, with focus on the bottom-gate back-channel-passivated (BCP) structure which is used throughout our work. Finally, the operation principles of a-Si TFTs and the relevant characterization methods are presented.

2.1 *Basic properties of a-Si*

The amorphous silicon (a-Si) discussed in this thesis is actually hydrogenated amorphous silicon, denoted by the abbreviation symbol a-Si:H. Amorphous silicon without hydrogen has a very high defect density and is thus not suitable for making semiconductor devices.

2.1.1 *Atomic structure*

The atomic structural disorder is the main feature of amorphous materials that differs from crystalline materials. A schematic atomic structure for a-Si is illustrated in Fig. 2.1.

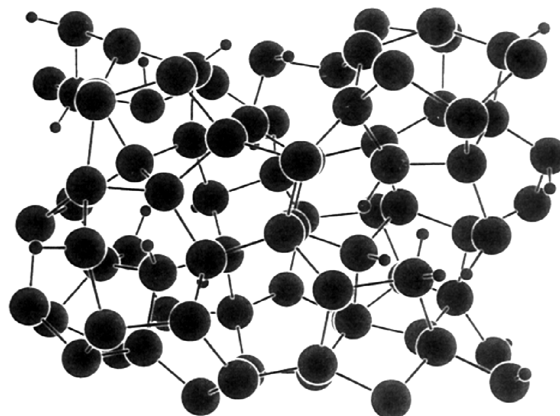


Fig. 2.1. Schematic representing the atomic structure of a-Si [4]

Fig 2.1 illustrates that a-Si is a disordered form of silicon consisting of a backbone of silicon atoms (big spheres in Fig. 2.1) with hydrogen atoms (small spheres in Fig. 2.1). Experimentally, the information of the atomic structure can be obtained by x-ray diffraction [5], electron diffraction [6], neutron diffraction [7] and EXAFS (extended x-ray absorption fine structure) [8]. An example of a typical radial distribution function (also known as pair distribution function, this shows the average atomic density at distance r from any atom) obtained from x-ray diffraction is shown in Fig. 2.2..

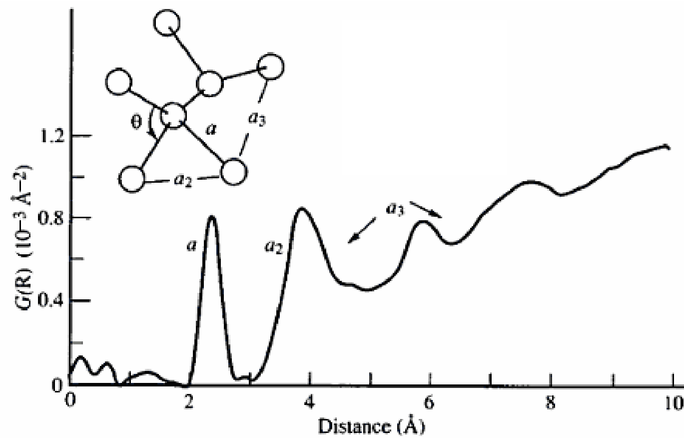


Fig. 2.2. Example of the radial distribution function of a-Si obtained from x-ray scattering [4, 5]

The radial distribution function of a-Si suggests that a-Si is not completely disordered and has a degree of short range order. Similar to crystalline Si, Si atoms in a-Si are generally bonded to four neighbors at tetrahedral angles ($\theta = 109°$) with a Si-Si bond length of $a = 0.23$ nm. However, unlike crystalline Si with determined bond angle and bond length, a-Si has a ~10% spread in bond angle and a ~1% spread in bond length [4]. These strained bonds are weak bonds. About 10% Si atoms with missing bonds and they are mostly passivated with hydrogen. The remaining 10^{15} to 10^{16} cm^{-3} so-called “broken” bonds are not passivated with hydrogen and become structural defects [9]. The short range order in the a-Si atomic structure allows the material to retain some useful semiconductor properties of crystalline Si. However, the lack of long range order provides a-Si with unique electronic and optical properties.

2.1.2 *Density of states*

The electronic properties of amorphous solids depend critically on the density of states distribution. The atomic structure of a-Si discussed earlier determines the density of states distribution, a model of which can be represented by Fig. 2.3.

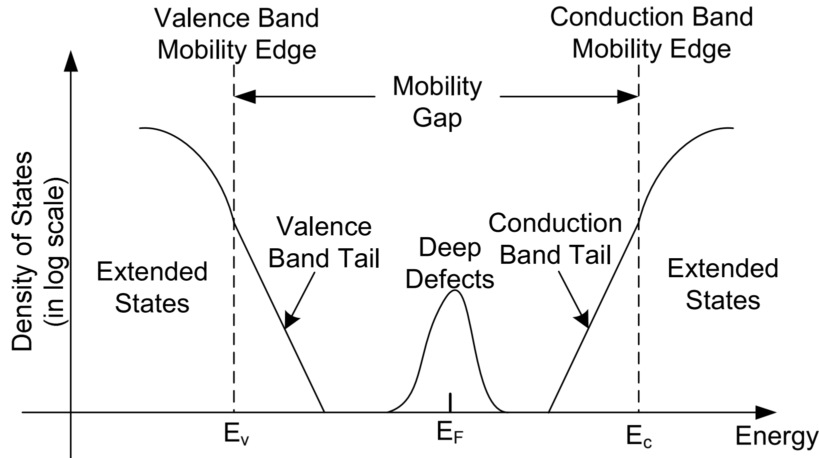


Fig. 2.3. Schematic a-Si density of states distribution

The short range order in a-Si results in a pseudo band gap [10], thereby enabling semiconducting properties. This pseudo band gap can be understood as a mobility gap. Within the mobility gap, the states are the result of disorder in the atomic structure; these are localized states. The weak bonds which result from the spreads in bond length and bond angle are the cause for the band tails. The structural defects from dangling bonds result in electronic states close to the mid gap. Beyond the mobility edges, the states are termed "extended states" and are similar to the states in crystalline Si.

The density of states can be determined with spectroscopy techniques, which generally can be divided into three categories [10]:

- Electron-spin resonance (ESR): by detecting singly occupied states (D^0), the equilibrium spin density can only correctly measure the defect density in undoped a-Si [4];
- Optical defect spectroscopy: including photocurrent spectroscopy (PCS), photothermal deflection spectroscopy (PDS) and photoacoustic spectroscopy (PCS);

– Space charge spectroscopy: including field-effect (FE) measurements, deep-level transient spectroscopy (DLTS) and space charge limited current (SCLC) measurements.

Among all the above techniques, field-effect measurement was the first technique to obtain density of states distribution in a-Si [3, 4] and it will be discussed in detail in Chapter 6.

As shown in Fig. 2.3, the density of states distribution contains the following major parts:

– **Band tails**

It has been proven by a variety of measurements [11-13] that both the valence band tail and the conduction band tail have an exponential distribution extending 0.1 eV to 0.5 eV below the corresponding mobility edge [4]. The slope of the band tails are often described by characteristic temperatures T_V for the valence band tail and T_C for the conduction band tail.

The valence band tail states density can be expressed as [4]

$$N_V(E) = N_{V0}\exp(-E/kT_V) \qquad (2.\ 1)$$

The logarithmic slope is about 50 meV / dec, with $T_V \approx 500$ K [12, 13].

The conduction band tail states density can be expressed with

$$N_C(E) = N_{C0}\exp(-E/kT_C) \qquad (2.\ 2)$$

The logarithmic slope is about 30 meV / dec, with $T_C \approx 300$ K [12-14].

The Urbach energy [15] obtained from optical absorption measurements gives a good measure of valence band slope, because the valence band tail is broader than the conduction band tail [13]. The density of states density at the mobility edges (N_{V0} and N_{C0}) is about 3 $\times 10^{21}$ cm^{-3} eV^{-1} [4].

– **Deep defects**

A dangling bond defect can exist in three charge states D^+, D^0 and D^- depending on the position of the Fermi level [4]. The defect is neutral (D^0) when singly occupied, can have an electron excited out of (or equivalently have a hole trapped into) the neutral bond, leaving a positively charged center D^+. Alternatively, the dangling bond defect can be occupied by a second electron and become a negatively charged state D^- [3]. According to the widely accepted concept of the

"defect-pool model" [11, 16-20], the dangling bonds form at the sites which minimize their formation energy, so the characteristic energy and density of deep defects depend on the Fermi energy during equilibration [16]. Thus, the distribution of deep defects can be greatly varied for a-Si prepared under different conditions (as shown in Fig. 2.4). The most common models describe the deep defect density as either following a Gaussian distribution [18, 21, 22] or an exponential distribution [14]. The exponential distribution of deep defect density is similar to the band tail distribution but with a large characteristic temperature, and it can be viewed as the tail part of the Gaussian distribution. In reality, the deep defect density distribution can be considered as a superposition of the Gaussian distributions for D^+, D^0 and D^- [23].

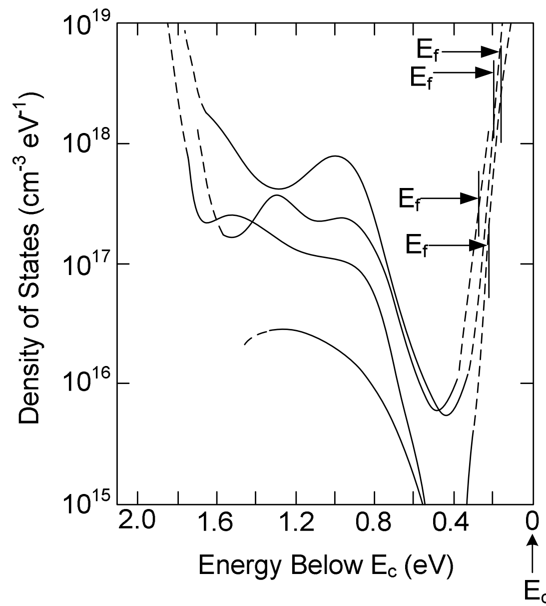


Fig. 2.4. Density of states distribution of n-type a-Si with different phosphorus doping levels measured by DLTS [24]; the distribution of deep defects varies with doping level.

– Extended states

Electrons in the extended states have higher mobility than in the localized states, and the mobility is known as free carrier mobility or band mobility μ_0. The distribution of extended states in a-Si can deviate from the parabolic distribution as in crystalline Si, and a linear density of states near and above the valence band edge has been reported [20].

– Mobility gap

The mobility gap separates extended and localized states, and can be reliably measured with the internal photoemission measurement [25]. Mobility gap was roughly estimated with the optical gap, which is derived by Tauc model from an extrapolation of parabolic band edge with the optical absorption coefficient [22]. However, optical determinations of the band gap for a-Si tend to underestimate the mobility gap [26].

2.1.3 *Electronic transport*

There are three main conduction mechanisms in a-Si [4] as illustrated in Fig. 2.5.

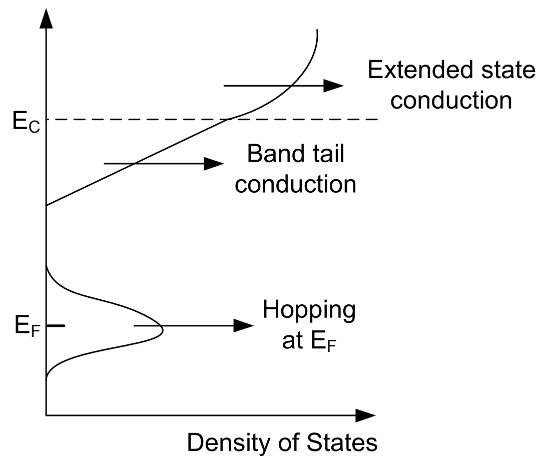


Fig. 2.5. Illustration of the three main conduction mechanisms in a-Si [4]

- Extended state conduction: the conduction through thermally activated carriers from the Fermi energy to above the mobility edge;
- Band tail conduction: a thermally activated tunneling process [10] of hopping from site to site. At very low temperatures approaching 0K, this type of conduction does not take place;
- Hopping conduction at the Fermi energy: this occurs when the density of states is large enough at the Fermi energy for significant tunneling of electrons. The conduction can be neglected in a-Si:H with low deep defect density.

The carrier mobility is an alternative measure of the conductivity and they can related with the following relation [4]

$$\sigma = nq\mu = \int N(E)f(E,T)q\mu(E)dE \qquad (2.\ 3)$$

Where n is the carrier density, $N(E)$ is the density of states, $f(E,T)$ is the Fermi function, $\mu(E)$ is the mobility at a specific energy level.

In n-type a-Si and a-Si TFTs under positive gate voltage, the Fermi energy E_F is in the conduction band tail. In p-type a-Si, E_F is in the valence band tail. Thus, the mobility of carriers in band tails is of great interest. The mobility will be limited by frequent trapping in the tail states and is known as the effective carrier mobility or drift mobility μ_D. The simplest model for explanation is the multiple trapping model, in which carriers move at the mobility edges and interact with tail states by trapping and thermal release [10]. The drift mobility can be related to the band mobility with the following relation [4]

$$\mu_D = \mu_0/(1 + f_{trap}) \qquad (2.4)$$

Where f_{trap} is the ratio of the time that the carrier spends in localized traps to that spent in mobile states. The band mobility is 1 – 10 cm^2 / V·s for both electrons and holes [27, 28]. The reported drift mobility is ≤ 4 cm^2 / V·s for electrons [29] and ≤ 0.01 cm^2 / V·s for holes [30].

2.1.4 *Metastability*

In a-Si, the disorder in structure results in the afore-mentioned weak bonds and dangling bonds. These two states are alternatives to each other, leading to the metastable configurational coordinate diagram as shown in Fig. 2.6 with two energy wells. The energy barrier E_b arises from the bonding energy of weak bonds, which is higher for stronger bonds and smaller for weaker bonds. The energy difference is the defect formation energy U_d and determines the dangling bond density in thermal-equilibrium [4].

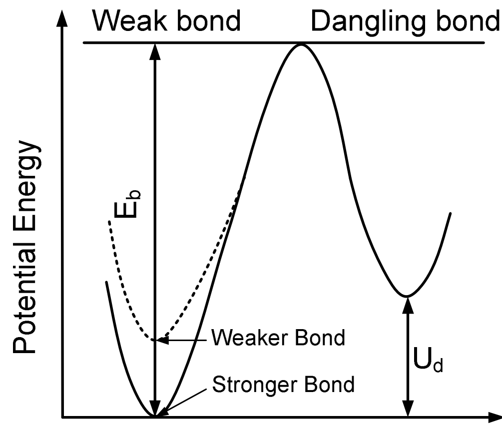


Fig. 2.6. Configurational coordinate diagram of a weak bond state and a dangling bond state separated by a potential energy barrier E_b

The conversion of weak bonds into dangling bonds is known as defect creation and the reverse process is defect annealing. The defect creation process can be illustrated with the density of states redistribution in Fig. 2.7.

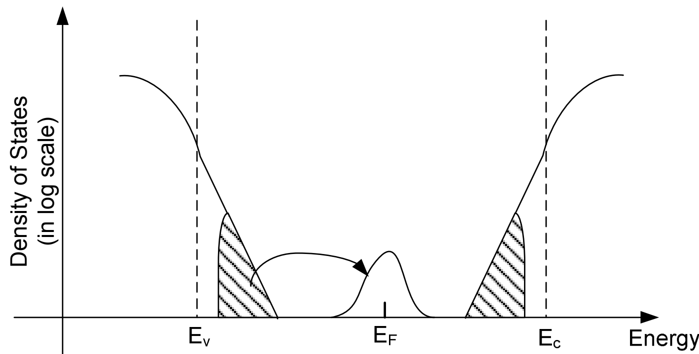


Fig. 2.7. Schematic density of states redistribution as a result of defect creation

As shown in Fig. 2.7, the created dangling bonds from weak bonds result in additional defect states. Defect creation is an important mechanism responsible for the instability issues in a-Si. The most widely-study defect creation phenomena include light-induced degradation in a-Si, particularly for a-Si solar cells [31-33] and the threshold voltage instability of a-Si TFTs [34, 35]. The latter will be further discussed in Chapter 4.

Two classes of models are widely used to explain the metastability in a-Si: thermal-equilibrium models and bond-breaking models [10].

– **Thermal-equilibrium models**

In thermal-equilibrium, the concentration $C(Q)$ of a certain structural configuration Q is determined by the Gibbs free energy $F(Q) = H(Q) - TS(Q)$ of this configuration through the relation

$$C(Q) \propto \exp\left(-\frac{F(Q)}{kT}\right) = \exp\left(\frac{S(Q)}{T}\right)\exp\left(-\frac{H(Q)}{kT}\right) \quad (2.\ 5)$$

The enthalpy $H(Q) = U(Q) - PV$, $U(Q)$ is the formation energy and $S(Q)$ is the entropy. In a solid, the changes in the pressure P and the volume V are negligible. Thus, the enthalpy $H(Q)$ can be equated with the formation energy $U(Q)$ without significant error [4].

Equation (2. 5) can be used to explain the field-effect bias induced defect creation in a-Si TFTs, because the formation energy is dependent on the Fermi level by

$$U(Q) = U_0(Q) - |E_F - E(Q)| \quad (2.\ 6)$$

Where $U_0(Q)$ is the formation energy of defect configuration without field-effect bias, E_F is the Fermi energy position, and $E(Q)$ is the electronic level of the created defect under field-effect bias. The term $|E_F - E(Q)|$ describes the gain in total energy for a defect that can exchange charge with the Fermi level [10].

Combining (2. 5) and (2. 6), it can be obtained that

$$C(Q) \propto \exp\left(\frac{|E_F - E(Q)|}{kT}\right) \quad (2.\ 7)$$

This means that the concentration of defects is dependent on the Fermi-level. Under field-effect bias, the increase in Fermi-level leads to the increase in the defects. The main disadvantage of the thermal-equilibrium models is that although it can explain the macroscopic changes in metastable states, it gives little microscopic information.

– **Bond-breaking models**

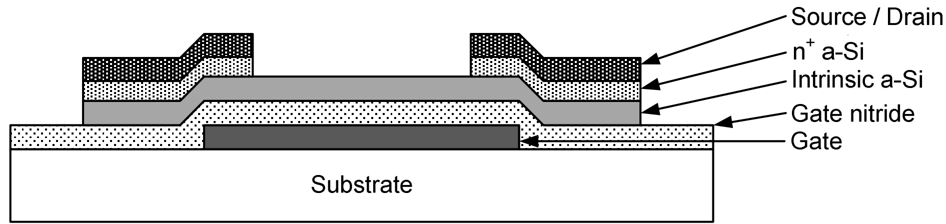
The bond-breaking models depict the microscopic defect creation process from the rupture of weak bonds. The thermal-equilibrium between the weak bonds and the dangling bonds is broken, such as in a-Si solar cells under light illumination or in a-Si TFTs under gate-field bias. In a-Si solar cells, the energy released by the nonradioactive recombination of photo excited electron-hole pairs lowers the energy barrier E_b in Fig. 2.6, so the defect creation rate is much higher than the defect annealing rate. In a-Si TFTs, electron in the channel induce weak bonds to break into dangling bonds, this process is immediately reversible unless the dangling bonds relax into stable configuration. The stabilization step actually created the barrier energy for the defect annealing process. Generally, there are two microscopic models for the stabilization step - hydrogen-diffusion-controlled defect-relaxation (HCR) model [33, 36, 37] and defect-controlled defect-relaxation (DCR) model [38]. These two models will be elaborated in Chapter 4.

2.2 *Structures and operation principle of a-Si TFTs*

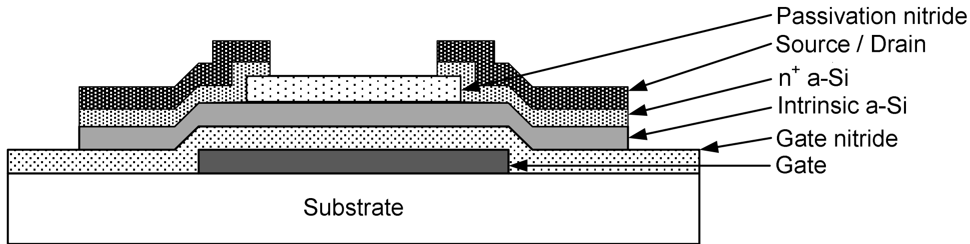
As a special kind of field-effect transistor, a thin-film transistor (TFT) is composed of a stack of thin films including a semiconducting active layer, a gate dielectric layer and metallic contacts over a supporting substrate [39]. In a-Si TFTs, the active layer is intrinsic a-Si and the gate dielectric typically is silicon nitride (SiN_x). Because the hole mobility of a-Si is very low, only n-type a-Si TFTs are available in practical applications. For n-type a-Si TFTs, between the intrinsic a-Si layer and the source / drain metal, a layer of phosphorous doped n^+ a-Si is usually used to ensure low resistance ohmic source/drain contacts.

2.2.1 *Bottom-gate structure*

The most commonly used a-Si TFT structure is the inverted-staggered structure. This is because this structure has easy fabrication processes and gives good electrical performance. The term “inverted” means that the position of the gate is on the bottom. The term “staggered” in contrast to “coplanar” refers to the fact that the source / drain electrodes and the gate electrode are located on different sides of the active layer. The inverted structures are also called bottom-gate structures. The TFTs with the inverted-staggered structure can be subdivided into two types – bi-layer (back-channel etched / cut) and tri-layer (back-channel passivated) [40] (Fig. 2.8).



(a) Back-channel etched (BCE) structure



(b) Back-channel passivated (BCP) structure

Fig. 2.8. Schematic cross-section of (a) back-channel etched (BCE) and back-channel passivated (BCP) standard a-Si TFT structures.

The inverted (bottom-gate) a-Si TFT structures have the active a-Si layer on top of the gate SiN_x dielectric layer. It has been reported that the interface with a-Si on top of SiN_x as in the bottom-gate structure is better than interfaces with SiN_x on top of a-Si as in a top-gate structure, with a lower interface charge density and lower hydrogen concentration [41-43]. As a result, bottom-gate a-Si TFTs have a higher field-effect mobility, lower threshold voltages and lower subthreshold slopes than top-gate a-Si TFTs.

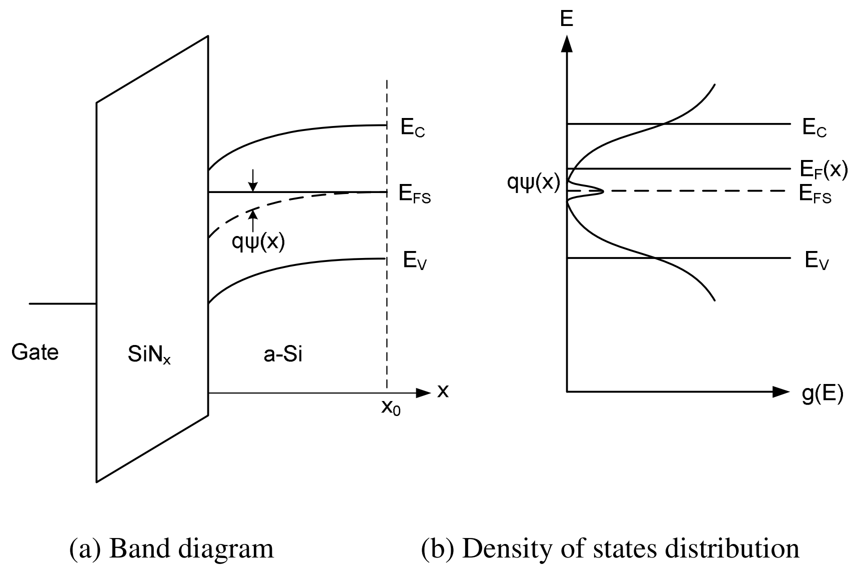
In the bi-layer (BCE) structure, the gate SiN_x, intrinsic and doped n+ a-Si are consecutively deposited without breaking vacuum. Since the etchant of n^+ a-Si also etches the active a-Si layer, a slight over-etch of the back channel cannot be avoided. Compared with the bi-layer (BCE) structure, the tri-layer (BCP) structure has one extra layer of SiN_x on top of the active a-Si layer. The gate SiN_x, intrinsic a-Si and passivation SiN_x are consecutively deposited in one-pump down. The passivation SiN_x layer serves as an etch-stop during the n^+ a-Si etching, and thus the BCP structure is also called an etch-stop structure.

The advantages of the BCP structure come from the protection granted by the passivation SiN_x layer. TFTs with BCP structure can have very thin active layers (as thin as ~50 nm), because the

passivation SiN_x layer prevents the under-cut of the a-Si back channel. This shortens the a-Si deposition time, decreases the leakage current through the a-Si layer and reduces the S/D - channel parasitic resistance [44]. By preventing the back channel from the exposure to the reagents during the n^+ a-Si film etching (the strong alkaline solution in wet-etching process or plasma damage in dry-etching process) and the ambient during operation, back-channel passivated TFTs can have higher field-effect mobility [44] and better threshold voltage stability [45]. However, the BCP structure needs an extra deposition step and an extra photolithography step, so it is more complicated in fabrication than the BCE structure. Another drawback of the BCP structure is that the length of the passivation SiN_x determines the channel length, so the channel length is more difficult to scale down than the BCE structure. For this thesis, the BCP structure is used because the threshold stability is the key concern.

2.2.2 *Operation of a-Si TFTs*

Because of the negligible hole mobility and the hole blocking at the source / drain contact by n^+ a-Si, the contribution of holes will be ignored in the following analysis. The operation of a-Si TFTs can be interpreted with the band diagram of an a-Si TFT as shown in Fig. 2.9.



(a) Band diagram (b) Density of states distribution

Fig. 2.9. Band diagram of an a-Si TFT under positive gate bias and density of states distribution.

Under positive gate bias, the band bends with the Fermi level near the SiN_x / a-Si interface deep into band tails. The band bending profile can be calculated by solving the Poisson's equation

$$\frac{d^2\psi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_{si}} \qquad (2.\ 8)$$

Where x is the distance away from the SiN_x / a-Si interface in the a-Si layer. At the interface,

$$\psi(x = 0) = \psi_s = V_G - \frac{|Q_n|}{C_{ins}} \qquad (2.\ 9)$$

C_{ins} is the capacitance of the gate SiN_x per unit area, and Q_n is the charge per unit area induced in the channel by the gate voltage V_G with

$$Q_n = \int_0^{x_0} \rho(x)dx \qquad (2.\ 10)$$

The charge density distribution $\rho(x)$ in a-Si layer can be related to the band bending $\psi(x)$ with

$$\rho(\psi) = -q\int_{E_{FS}}^{\infty} g(E)f(E - q\psi)dE \qquad (2.\ 11)$$

Where $f(E) = \frac{1}{1+\exp\left(\frac{E-E_{FS}}{kT}\right)}$ is the Fermi-Dirac distribution function.

From Fig. 2.3, the density of states distribution $g(E)$ is composed of deep defect states $g_d(E)$, band tail states $g_b(E)$ and extended states $g_e(E)$. They result in three corresponding components in $\rho(\psi)$ denoted as $\rho_d(\psi)$, $\rho_b(\psi)$ and $\rho_e(\psi)$ respectively. The schematic charge distribution is illustrated in Fig. 2.10. Deep defect states and band tail states are localized states and the channel conduction can be viewed mainly from electrons in the extended states, i.e. $\rho_e(\psi)$ and it keeps increasing with the increasing band bending ψ.

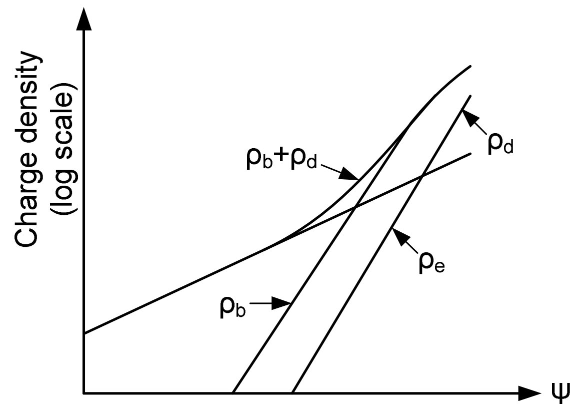


Fig. 2.10. Charge distribution as a function of band bending.

Fig. 2.10 shows that only a small portion of induced charge is from free electrons in extended states. Thus, the effective field-effect mobility μ_{FET} can be related to the band mobility μ_0 with

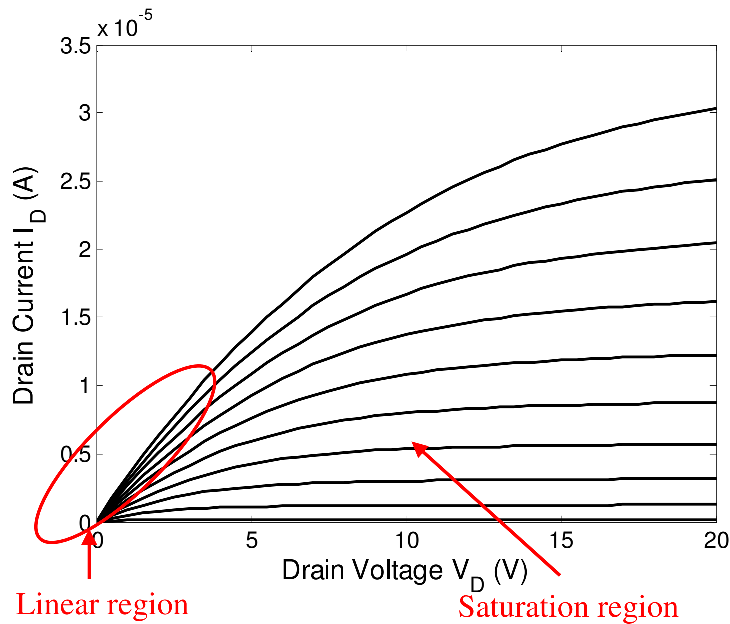
$$\mu_{FET} = \mu_0 \frac{Q_e}{Q_n} = \mu_0 \frac{\int_0^{x_0} \rho_e(x)dx}{\int_0^{x_0} \rho(x)dx} \quad (2.\ 12)$$

Typically, the effective field-effect mobility μ_{FET} a-Si TFTs is 1.2 – 1.4 cm^2/V·s in laboratory [46] and 0.3 – 0.6 cm^2/V·s in production [47]. A record high $\mu_{FET} \approx 2$ cm^2/V·s has been achieved using a SiO2–silicone hybrid dielectric [48].

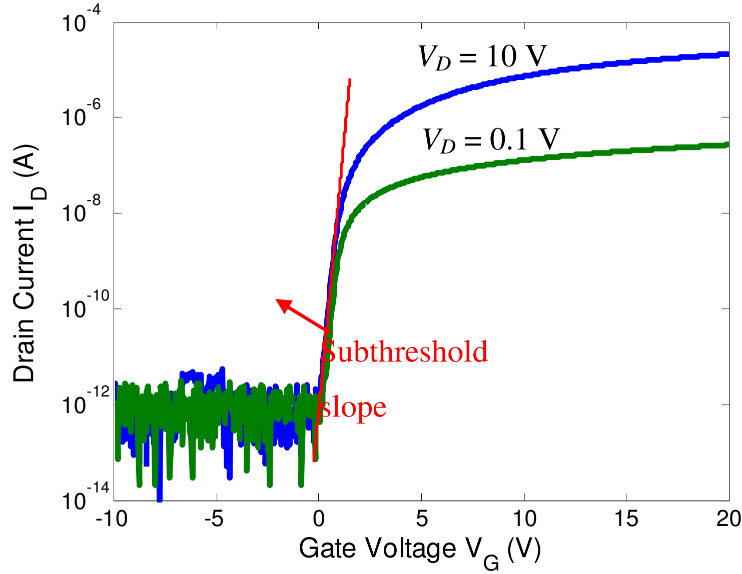
The theoretical analysis of I-V characteristics can be found in Chapter 6.

2.2.3 *Characterization of a-Si TFTs*

Experimentally, the typical I-V characteristics of a good-performance a-Si TFT with 150 μm channel width and 15 μm channel length are shown in Fig. 2.11.



(a) Output characteristics with $V_G = 2$ V – 20 V in steps of 2 V



(b) Transfer characteristics with $V_D = 0.1$ V and 10 V

Fig. 2.11. I-V characteristics of a typical a-Si TFT with W/L = 150 / 15 μm.

The off-current I_{off} is at the sub-pA level, and the on / off current ratio is about 10^7. The subthreshold slope (red line in Fig. 2.11(b)) is about 300 mV / dec.

The I-V characteristics of a-Si TFTs are similar to those obtained from conventional MOSFETs. Thus the gradual channel model for conventional MOSFET can be used to characterize the a-Si TFTs operating in linear regime and saturation regime [10].

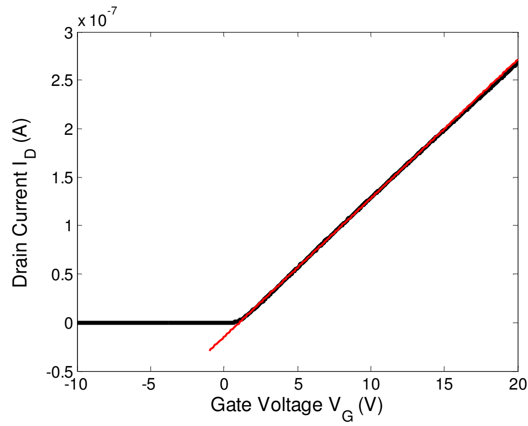
In the linear region with $V_D < V_G - V_T$, the drain current is given by

$$I_D = \mu_{FET,lin} C_{ins} \frac{W}{L}\left[\left(V_G - V_{T,lin} - \frac{1}{2}V_D\right)V_D\right] \quad (2.\ 13)$$

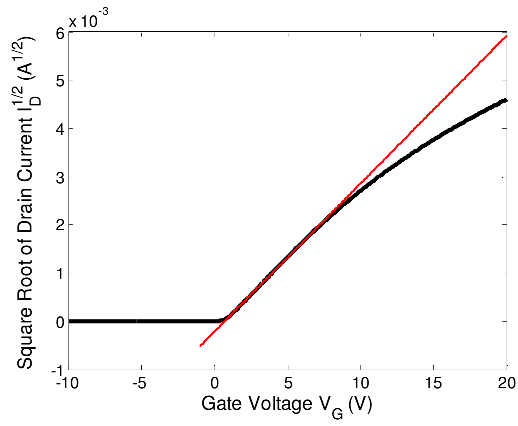
In the saturation region with $V_D \geq V_G - V_T$, the drain current is given by

$$I_D = \mu_{FET,sat} C_{ins} \frac{W}{2L}\left[\left(V_G - V_{T,sat}\right)^2\right] \quad (2.\ 14)$$

Where $\mu_{FET,lin}$ and $\mu_{FET,sat}$ are the effective field-effect mobility in linear and saturation regime; $V_{T,lin}$ and $V_{T,sat}$ are the threshold voltage in linear and saturation regime. They can be extrapolated from the least-square fits to transfer characteristics as in Fig. 2.12.



(a) Linear region



(b) Saturation region

Fig. 2.12. Least-square fits to transfer characteristics of the a-Si TFT.

In the linear region, $\mu_{FET,lin} = 0.83$ cm^2/V·s and $V_{T,lin} = 1.0$ V.

In the saturation region, $\mu_{FET,sat} = 1.1$ cm^2/V·s and $V_{T,sat} = 0.69$ V.

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Fabrication of Amorphous-Silicon Thin-Film Transistors

Amorphous-silicon thin-film transistors (a-Si TFTs) in this thesis were fabricated with bottom-gate non-self-aligned processes in the back-channel passivated (BCP) structure. The silicon nitride (SiN_x) and amorphous silicon (a-Si) layers were deposited in a plasma-enhanced chemical vapor deposition (PECVD) system at 13.56 MHz. This chapter first presents the PECVD growth of thin films of SiN_x and a-Si. Then a new full wet-etch fabrication process that has the same deposition steps as the dry-etch process is introduced along with the dry-etch process. The stability of dry-etched and wet-etched a-Si TFTs will be compared in Chapter 5.

3.1 *PECVD growth of thin films in a-Si TFTs*

Plasma enhanced chemical vapor deposition (PECVD) is widely used to grow thin film materials for a-Si TFTs. The most common PECVD reactors are in a diode configuration with the plasma confined between two parallel electrodes. The PECVD reactor in Princeton is in a triode configuration, using a metal grid in the reactor to separate the plasma from the growing surface, thereby reducing ion bombardment [1]. The triode configuration PECVD reactor with radio frequency (RF) radiation at 13.56 MHz is used to deposit a-Si TFTs for this thesis. The substrate temperature calibration of the PECVD system is displayed in Appendix B.

3.1.2 *Parameters in PECVD growth*

There are several parameters that control the PECVD growth of thin films.

– **Gas pressure**

The gas pressure during deposition is maintained by a throttle valve which controls the amount of gases that are pumped out. The gas pressure determines the mean free path for collisions of the gas molecules and influences whether the reactions happen at the growing surface or in the gas [1]. Deposition of hydrogenated amorphous materials usually takes place at a gas pressure of 0.01 – 1 Torr with a film of material coating most of the exposed surfaces in the neighborhood of the plasma [2].

– **Gas flow rate**

Mass flow controllers (MFC) regulate the gas flow rates of the precursor gases before they enter the PECVD chamber. For a given pressure, the gas flow rate controls the length of time that a given gas molecule resides inside the chamber, known as the residence time [3]. The convenient unit for gas flow rate is sccm (standard cubic centimeters per minute at $T = 273$ K, 1 atm), i.e. 4.5×10^{17} molecules/second.

– **RF power**

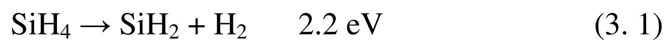
The RF power determines the energy in the plasma [3] which helps the dissociation of the gas species and therefore controls the film growth rate [1]. However, increasing the power also increases the plasma potential and hence the ion bombardment energy [3].

– **Substrate temperature**

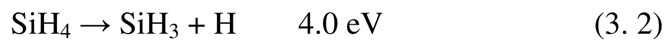
The temperature of the substrate temperature controls the chemical reactions on the growing surface. Diffusion is a thermally activated process responsible for the transport of gas species both on the deposition surface and in the film bulk. Thus, increasing substrate temperature increases diffusivity [3, 4].

3.1.3 *a-Si growth*

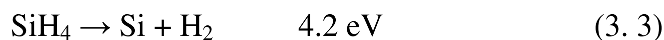
The usual deposition method of intrinsic a-Si is by PECVD using silane gas (SiH_4). a-Si films can be grown between 450°C and 550°C in the absence of plasma. The plasma provides energy to the dissociation of silane and enables the deposition of a-Si films at lower temperatures [1]. The main growth species are neutral radicals. Some silane dissociation reactions related to a-Si growth with low energy requirement are [1]



$SiH_4 \rightarrow SiH_2 + H_2$ 2.2 eV (3. 1)



$SiH_4 \rightarrow SiH_3 + H$ 4.0 eV (3. 2)



$SiH_4 \rightarrow Si + H_2$ 4.2 eV (3. 3)

The dominant radical responsible for the a-Si deposition is SiH_3, which has a reactive dangling bond and can be transported to the H-saturated growing surface [3] as in Fig. 3.1.

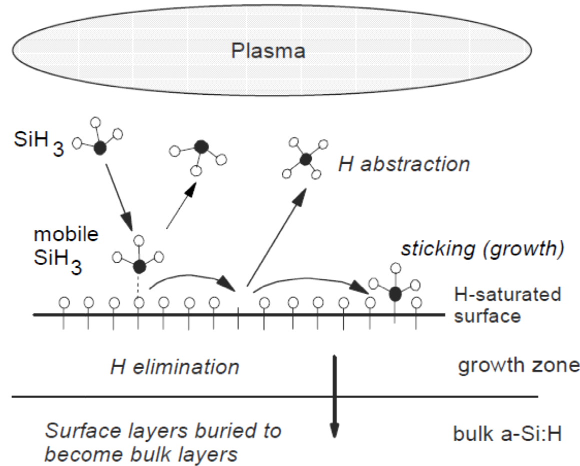


Fig. 3.1. Surface reactions on a-Si [4].

SiH_3 can add to an existing surface dangling bond leading to film growth, it can diffuse to the neighbouring Si-H sites without reaction or desorbing and it can also abstract a hydrogen from a surface Si-H bond to leave a surface dangling bond [4-6].

The PECVD parameters are critical for high quality a-Si growth as well the hydrogen dilution in silane:

– **Substrate temperature and RF power**

Increasing the substrate temperature increases the diffusivity of species such as SiH_3 and H. It means that more hydrogen on the surface can be abstracted. Therefore, hydrogen content of the material reduces with the increasing substrate temperature (Fig. 3.2). The removal of hydrogen from the surface results dangling bonds and will be attached by SiH_3 radicals. As a result, the equilibrium of weak bonds and dangling bonds distribution also depends on the substrate temperature. As explained in the last chapter, the Urbach energy reflects the distribution of the weak bond density and a higher Urbach energy represents a more disordered a-Si structure. Fig. 3.2 shows that the Urbach energy strongly depends on the substrate temperature and reaches the minimum around 250°C [4]. The defect density is lowest when the substrate temperature is about 300°C, and this temperature is also known to have the most stable a-Si TFTs [7]. The growth rate is proportional to the RF power [1]. However, the hydrogen content, Urbach energy and defect density all increases with the rising RF power (Fig. 3.2).

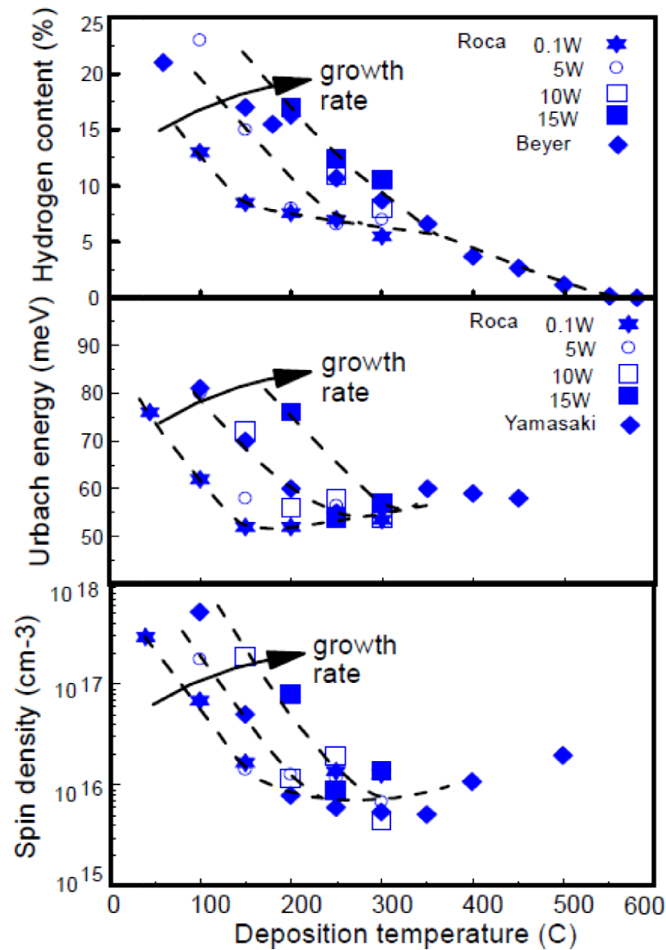


Fig. 3.2. Dependence of hydrogen content, Urbach energy and spin density on substrate temperature and RF power [4]. Notes: Roca [8], Beyer [9], and Yamasaki [10].

– **Gas pressure and hydrogen dilution**

Two distinct regimes have been identified for PECVD growth of a-Si - α regime and γ regime [4, 7, 11, 12]. The α regime dominates in the low pressure regime. The RF energy is weakly coupled to the plasma by sheath oscillations, producing fast electrons which collide with silane molecules to generate highly reactive silicon based radicals. In the α regime, the deposition rate is low (Fig. 3.3). However, the ion-flux component is high, leading to high ion bombardment. The mobility of a-Si TFTs with a-Si grown in the α regime is high, but the threshold voltage stability is low (Fig. 3.4).

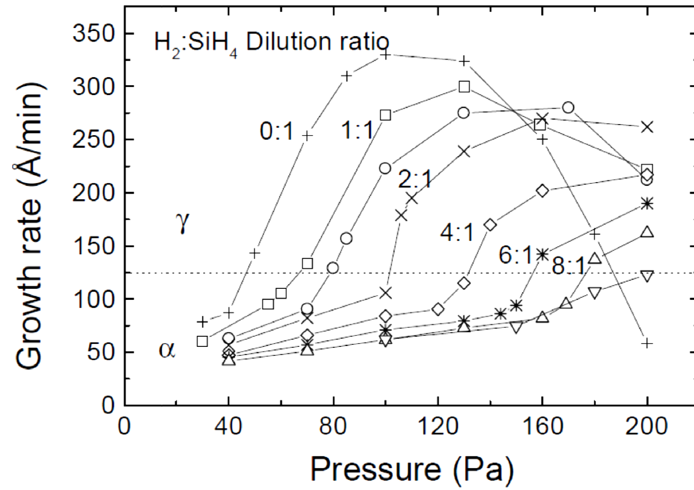


Fig. 3.3. a-Si growth rate vs. gas pressure for different ratios of hydrogen dilution [4].

The γ regime dominates in the higher pressure regime and the plasma is excited by Joule heating. This means more efficient power coupling into the plasma, more dissociation of silane molecules and thereby higher deposition rates [12] (Fig. 3.3).

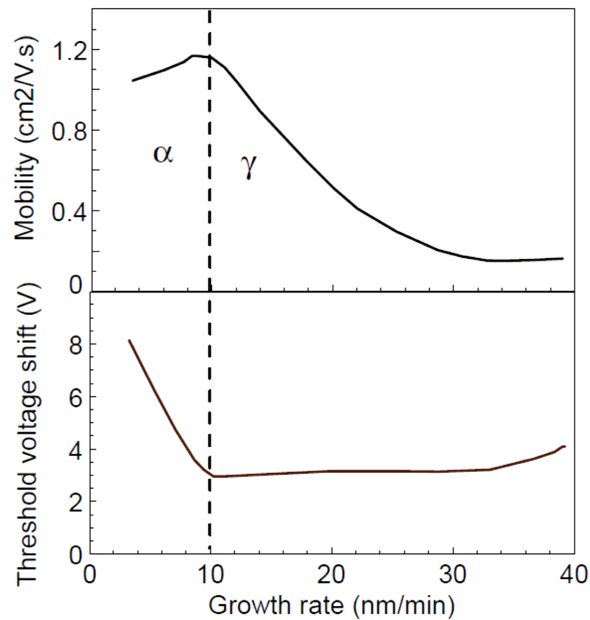


Fig. 3.4. Schematic dependence of mobility and threshold voltage stability in the α regime and γ regime [4].

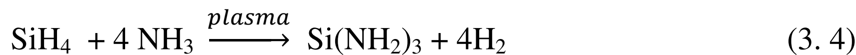
The mobility of a-Si TFTs with a-Si grown in the γ regime is low, but the threshold voltage stability is high (Fig. 3.4). Fig. 3.4 shows that the most stable a-Si TFTs have the a-Si deposited

at the boundary of the α regime and the γ regime, where the plasma condition is unstable. In hydrogen diluted silane, the transition from the α regime to the γ regime depends mainly on the silane partial pressure. From Fig. 3.3, for higher hydrogen dilution, the distinction between α and γ regimes is less clear, and there is no sharp fall in growth rate. Hydrogen dilution increases the role of atomic hydrogen and ions, which helps dehydrogenation of the a-Si, reducing the formation of polyhydride phases and thereby decreasing the Urbach energy [4, 12].

3.1.4 *SiN_x growth*

Amorphous silicon nitride can be deposited in PECVD with silane and ammonia mixtures (SiH_4 + NH_3). The PECVD film is not generally stoichiometric Si_3N_4 and is actually hydrogenated, so it can be more properly denoted as SiN_x:H or SiN_x for simplicity. When $x > 1.33$, the film is nitrogen-rich. When $x < 1.33$, the film is silicon-rich. For the nitrogen-rich SiN_x, silicon atoms are almost all bonded to nitrogen atoms and the excess nitrogen atoms are bonded to hydrogen atoms, resulting in a very low content of Si-H bonds [13]. The nitrogen-rich film is better than the silicon-rich film for the gate dielectric in a-Si TFTs, in terms of less interface charging, higher mobility and better threshold voltage stability [14, 15].

The SiN_x growth mechanisms can be schematically illustrated in Fig. 3.5. The reactions for the PECVD deposition of nitrogen-rich SiN_x are first the precursor – forming reaction



$$SiH_4 + 4\,NH_3 \xrightarrow{plasma} Si(NH_2)_3 + 4H_2 \qquad (3.\,4)$$

And the following surface condensation reaction

$$Si(NH_2)_3 \xrightarrow{heat} Si_3N_4 + 8\,NH_3 \qquad (3.\,5)$$

The key parameters are the SiH_4 / NH_3 ratio, RF power, substrate temperature and hydrogen dilution, which all affect the quality of the deposited SiN_x.

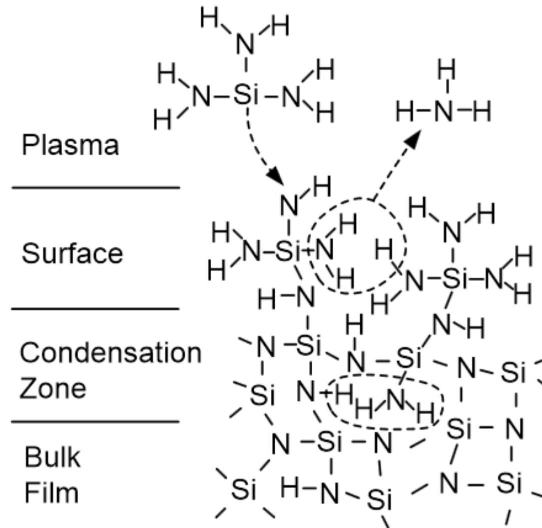


Fig. 3.5. Schematic growth mechanism of PECVD SiN_x [13].

– **SiH_4 / NH_3 flow ratio and RF power**

The N / Si ratio x can vary widely by tuning SiH_4 / NH_3 flow ratio and RF power. x increases by increasing NH_3 / SiH_4 flow ratio (Fig. 3.6) or increasing RF power (Fig. 3.7).

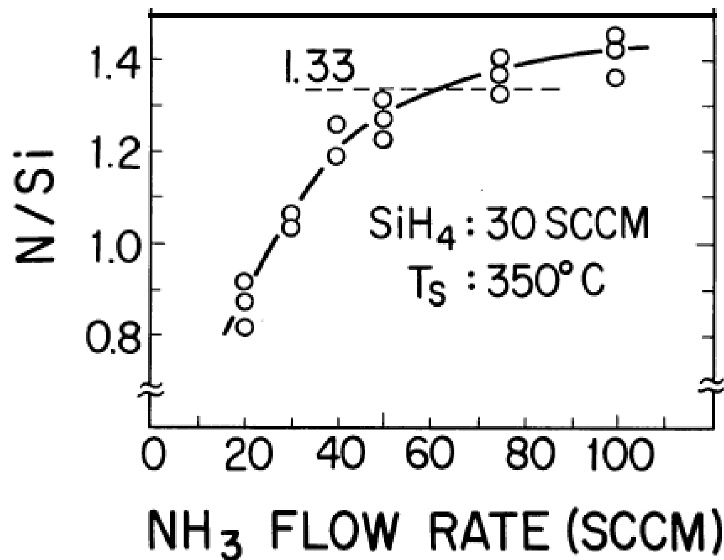


Fig. 3.6. N / Si ratio as a function of NH_3 flow rate. During deposition, SiH_4 flow rate was 30 sccm, the substrate temperature is 350°C, the gas pressure was 1.2 Torr and the power density was 1.04 W/cm^2 [16].

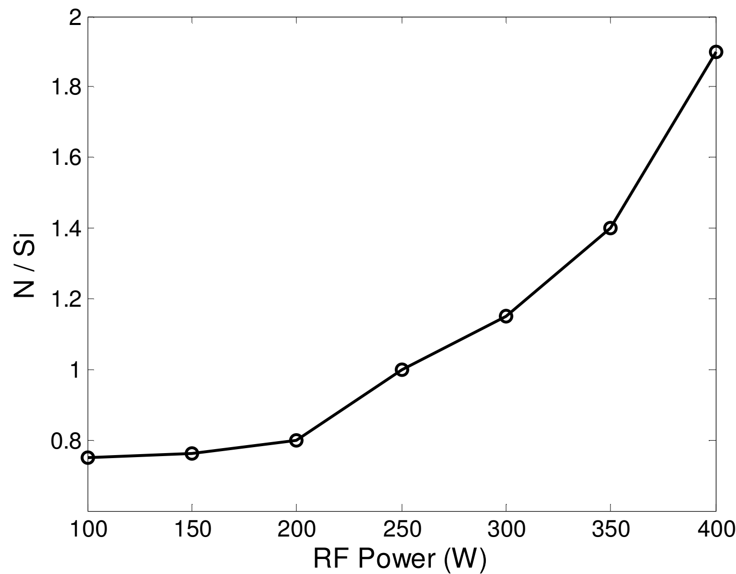


Fig. 3.7. N / Si ratio as a function of RF power. The reacting gases were SiN_4 (1.70%) and NH_3 (2.39%) in Ar carrier gas, with the total flow rate 2320 sccm, the gas pressure is 0.95 Torr, and the substrate temperature was 275°C [17].

The nitrogen-rich SiN_x with low Si-H content and good electrical properties can be grown at high NH_3 / SiH_4 flow ratio and high RF power [13]. The results in Fig. 3.6 and Fig. 3.7 were from the earliest research about PECVD SiN_x with SiH_4 and NH_3. Lowering the gas residence time through control of gas flow rate and pressure enables high quality nitrogen-rich SiN_x at lower NH_3 / SiH_4 ratios and RF powers [18, 19].

- **Substrate temperature and hydrogen dilution**

For the nitrogen-rich SiN_x deposition, the N / Si ratio decreases x with increasing substrate temperature [13] and hydrogen dilution [18]. Increasing the substrate temperature helps to remove amino (NH_2) content and leads to a denser nitride film structure, driving the film to be tensile. Hydrogen dilution also reduces amino (NH_2) content and makes the nitride film more compact, but drives the film to be compressive. Thus, the stress of film can be controlled by tuning the substrate temperature and the hydrogen dilution level [18].

3.2 *Dry-etch and wet-etch fabrication process flows*

In our dry-etching process, reactive ion etching (RIE) was performed to pattern the silicon nitride and a-Si. There are four plasma etching steps, which were replaced with wet-etching methods for wet-etched a-Si TFTs. The full-wet-etch process uses the same plasma enhanced chemical vapor deposition steps for the TFT stack growth as the dry-etch process, unlike an earlier wet-etch a-Si TFT process that required an additional SiN_x layer [20, 21]. The equipment used for intrinsic a-Si, n^+ a-Si and SiN_x deposition is a Solarex / Innovative S900 four-chamber PECVD system. The RIE for the dry-etch process is performed in a Plasma-Therm 720 RIE system.

The dry-etch and wet-etch fabrication process flows are presented step by step and contrasted:

- **Step 1: Gate metal deposition and patterning**

After cleaning the glass substrate, the gate metal layer of ~70nm Chromium (Cr) is thermally evaporated and patterned (mask #1-dry and mask #1-wet). Cr is etched with etchant Cr 7. This step is identical for dry-etch and wet-etch processes. The top view of the sample after this step is schematically shown in Fig. 3.8.

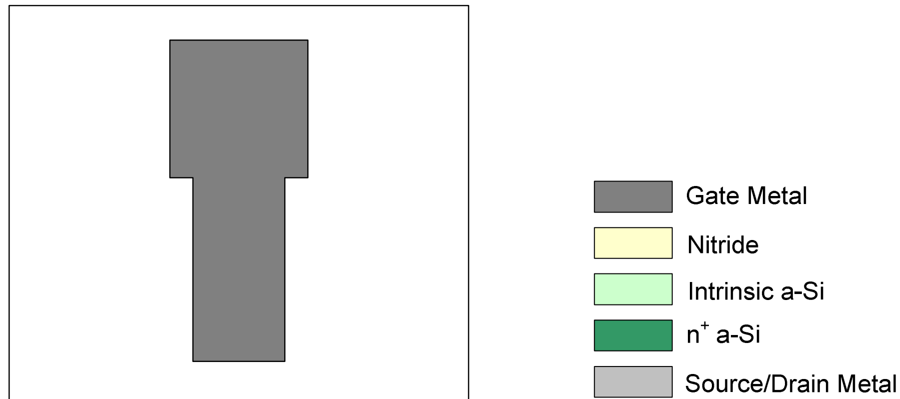


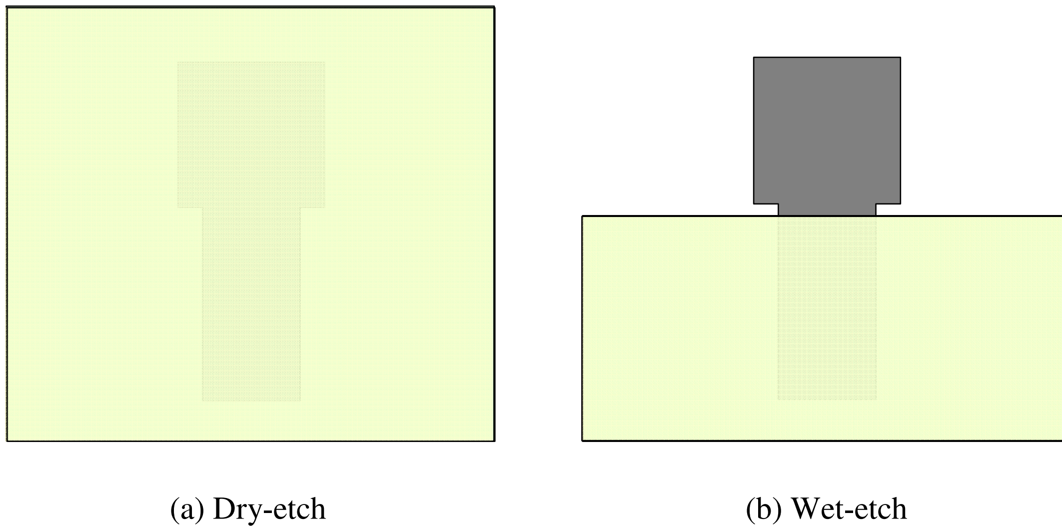
Fig. 3.8. Schematic top view of dry-etched and wet-etched TFTs after Step 1.

- **Step 2: Gate SiN_x / a-Si / Passivation SiN_x deposition**

A stack of ~300-nm gate SiN_x, ~200-nm intrinsic hydrogenated a-Si and ~300-nm passivation SiN_x is deposited in this step. The deposition conditions for the gate SiN_x and the a-Si layer will be varied and compared to find the best recipe for most stable a-Si TFTs in Chapter 5. During the

deposition of the passivation SiN_x, SiH_4 = 6 sccm, NH_3 = 150 sccm, pressure = 500 mTorr, RF power = 5 W, substrate temperature is 220°C, and the growth rate is ~0.2 nm / sec.

The gate SiN_x deposited with hydrogen diluted SiH_4 and NH_3 gases at high temperature is very dense. For the wet-etch process, only very strong etchant, e.g. heated phosphoric acid can etch the dense gate SiN_x to open the via contact to the gate metal. The strong etchant etches photoresist, a-Si and gate metal as well. To avoid using the strong etchant for the gate SiN_x etch, a shadow mask (mask #2-wet) is used during the three layer stack deposition in order to cover part of the gate metal and leave the area to make the gate contact. The top view of the dry-etch and wet-etch samples after this step is schematically shown in Fig. 3.9.



(a) Dry-etch (b) Wet-etch

Fig. 3.9. Schematic top view of dry-etched and wet-etched TFTs after Step 2.

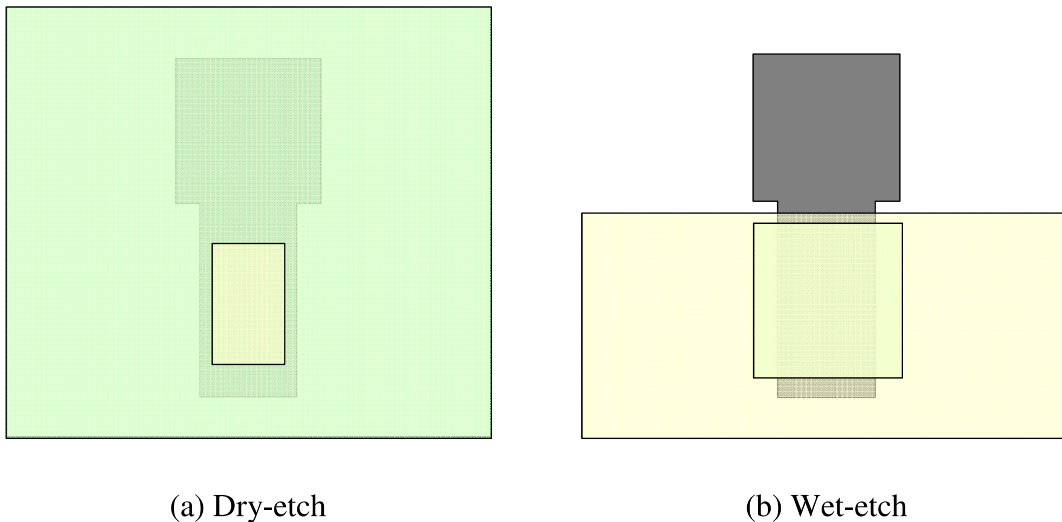
– **Step 3: Passivation etching for dry-etch and island etching for wet-etch**

To avoid the extra deposition of a masking SiN_x layer as in Ref [20] and [21], the passivation SiN_x layer is used as the mask for island etching of the a-Si layer. Thus, from Step 3, the fabrication flow processes are different between dry-etch and wet-etch. However, the differences only exist in the etching steps, while the deposition conditions and steps are kept the same for a valid comparison in Chapter 5.

For dry etching, the passivation SiN_x layer is etched to define the gate length (mask #2-dry). The dry etching is conducted using a CF_4 / O_2 mixture, with CF_4 = 70 sccm, O_2 = 10 sccm, gas pressure = 50 mTorr and RF power = 100 W. The etching rate is about 6 nm / sec for the passivation SiN_x.

For wet etching, the passivation SiN_x layer is first patterned (mask #2-dry), and then the patterned passivation SiN_x is used as the mask to etch the underneath a-Si layer for the isolation of TFTs. The passivation SiN_x is etched with diluted HF (1% in H_2O), and the etching rate is about 5nm / sec. The a-Si is etched with KOH solution (10% weight percentage in H_2O), and the etching rate is about 0.7 nm / sec.

The top view of the samples after this step is schematically shown in Fig. 3.10.



(a) Dry-etch (b) Wet-etch

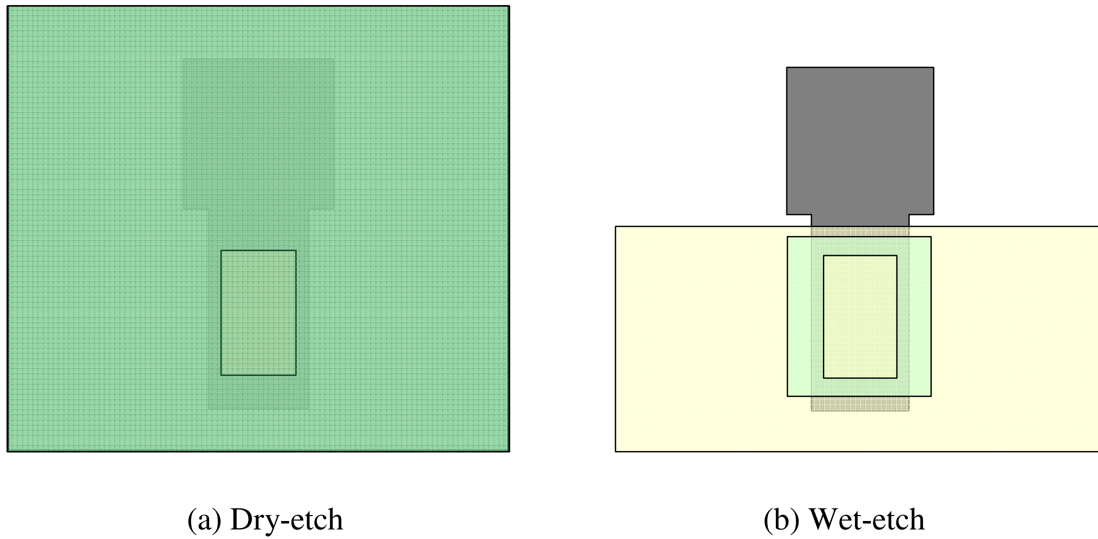
Fig. 3.10. Schematic top view of dry-etched and wet-etched TFTs after Step 3.

– **Step 4: n^+ a-Si deposition for dry-etch and passivation etching for wet-etch**

For dry-etching, ~20 nm n+ a-Si is deposited in PECVD system with a mixture of SiH4 and PH_3. During deposition, SiH_4 = 44 sccm, PH_3 = 8 sccm, pressure = 500 mTorr, RF power = 4 W, substrate temperature is ~200°C, and the growth rate is ~0.1nm / sec.

For wet-etching, the passivation SiN_x layer is etched again with the diluted HF (1% in H_2O), and mask #4-wet is used to define the gate length.

The top view of the samples after this step is schematically shown in Fig. 3.11.



(a) Dry-etch (b) Wet-etch

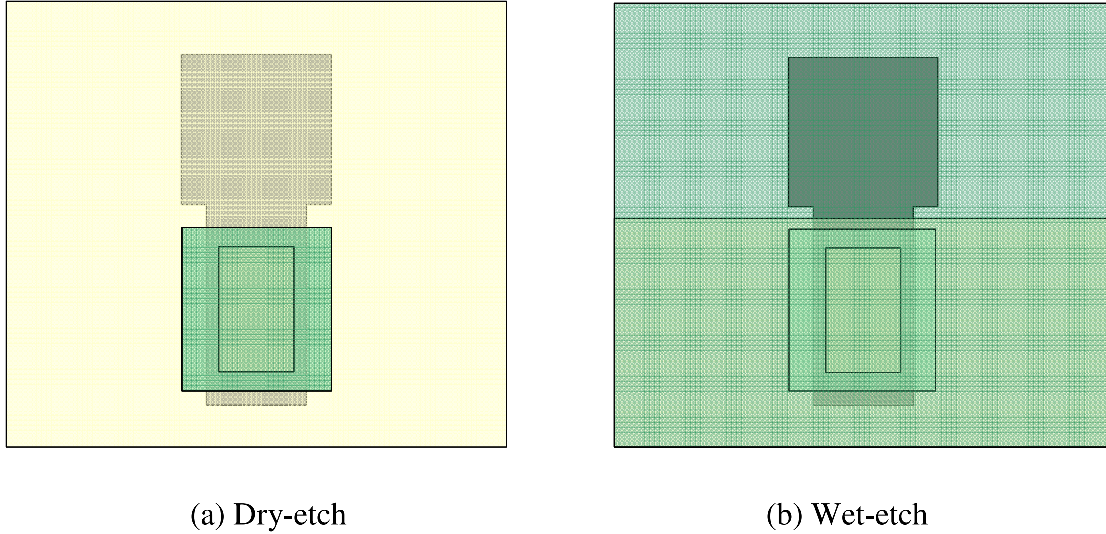
Fig. 3.11. Schematic top view of dry-etched and wet-etched TFTs after Step 4.

- **Step 5: Island etching for dry-etch and n^+ a-Si deposition for wet-etch**

For dry-etching, the n^+ a-Si and intrinsic a-Si layer are etched to isolate TFTs (mask #3-dry). The dry etching is conducted using a CCl_2F_2 / SF_6 mixture, with CCl_2F_2 = 60 sccm, SF_6 = 20 sccm, gas pressure = 100 mTorr and RF power = 100W. The etching rate is about 2 nm / sec.

For wet-etching, ~20 nm n+ a-Si is deposited in PECVD system with a mixture of SiH_4 and PH_3.

The top view of the samples after this step is schematically shown in Fig. 3.12.



(a) Dry-etch (b) Wet-etch

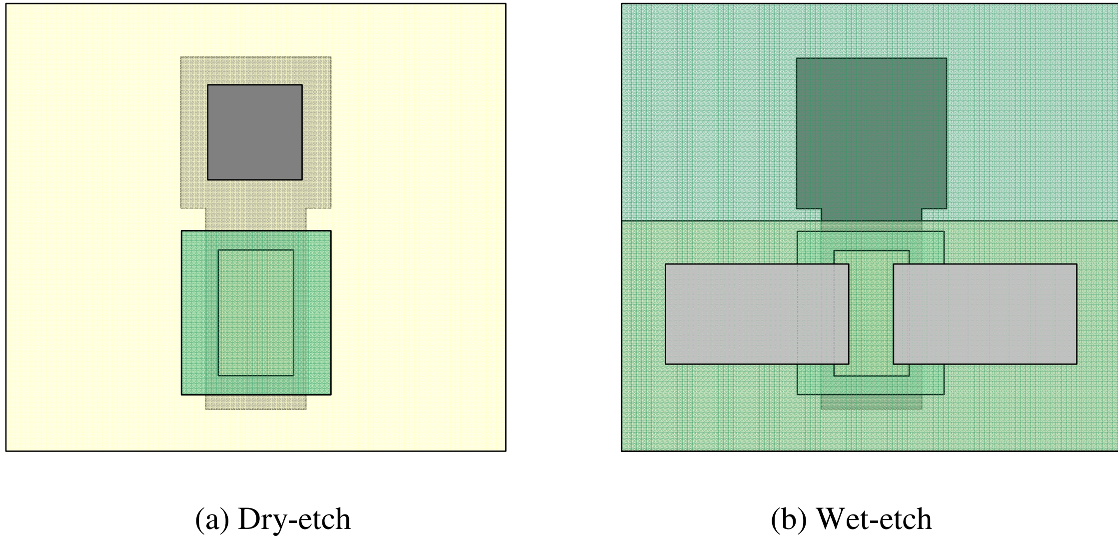
Fig. 3.12. Schematic top view of dry-etched and wet-etched TFTs after Step 5.

– **Step 6: Contact via opening for dry-etch and source / drain metallization for wet-etch**

For dry etching, the gate SiN_x layer is etched to open the contact via to gate metal (mask #4-dry). The dry etching is conducted using a CF_4 / O_2 mixture, with CF_4 = 70 sccm, O_2 = 10 sccm, gas pressure = 50 mTorr and RF power = 100W. Depending on the deposition condition for the gate SiN_x, the etching rate varies from 3 to 6 nm / sec.

For wet etching, source / drain (S/D) metal is patterned with a lift-off process. If the S/D metal is etched away instead of lifted off, the metal residual in the channel region will prevent the etchant from etching the n^+ a-Si in the next step for wet etching. In the lift-off process, photoresist is spun on and patterned with mask #5-wet. Then the S/D metal (Chromium / Aluminum / Chromium = 15 nm / 250 nm / 15 nm) is thermally evaporated. Last, the sample is placed in acetone and an ultrasound bath is used to lift off the S/D metal.

The top view of the samples after this step is schematically shown in Fig. 3.13.



(a) Dry-etch (b) Wet-etch

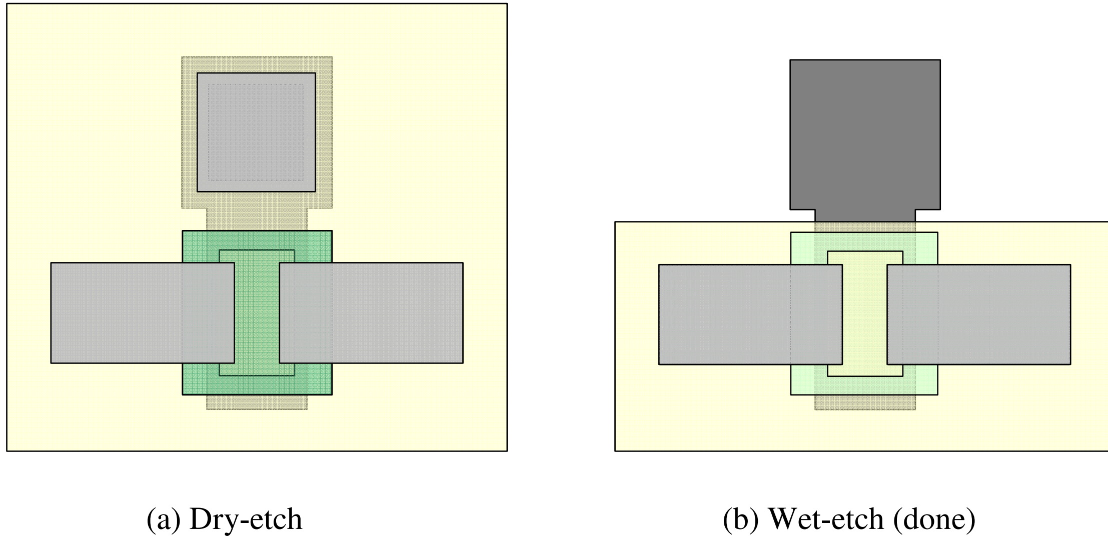
Fig. 3.13. Schematic top view of dry-etched and wet-etched TFTs after Step 6.

– **Step 7: Source / drain metallization for dry-etch and n^+ a-Si etching for wet-etch**

For dry etching, the S/D metal (Chromium / Aluminum / Chromium = 15 nm / 250 nm / 15 nm) is thermally evaporated and patterned with mask #5-dry. The S/D metal is etched with Chromium etchant Cr 7 and Aluminum etchant Al 11.

For wet etching, the n^+ a-Si is etched with Potassium hydroxide (KOH) solution (10% weight percentage in H_2O), and the etching rate is about 0.7 nm / sec. The S/D metal serves as the mask. The deposition and etching steps for the wet-etch process are completed, with one etching step less than the dry-etch process due to the use of the shadow mask.

The top view of the samples after this step is schematically shown in Fig. 3.14.

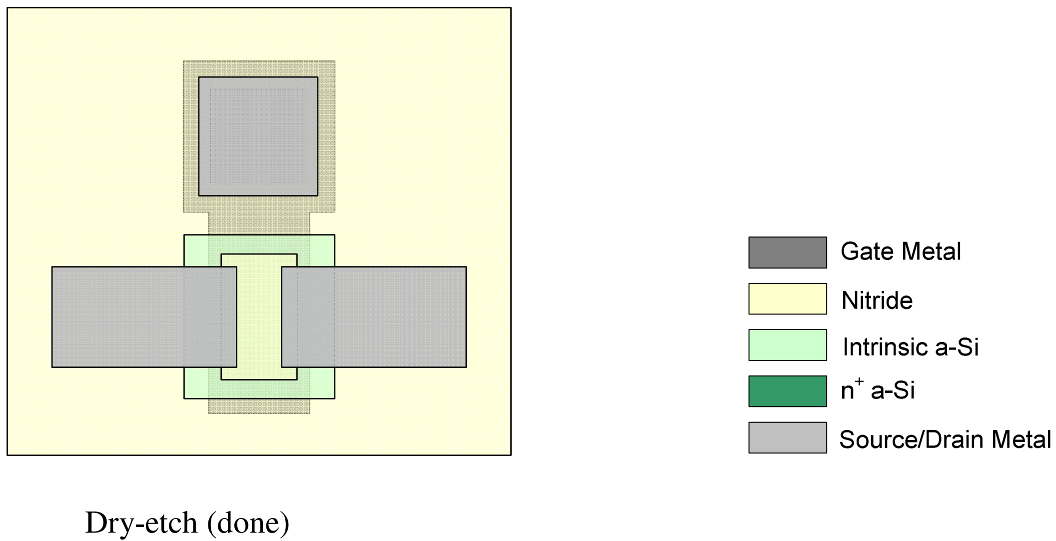


(a) Dry-etch (b) Wet-etch (done)

Fig. 3.14. Schematic top view of dry-etched and wet-etched TFTs after Step 7.

– **Step 8: n^+ a-Si etching for dry-etch**

For wet etching, the n^+ a-Si is etched with CCl_2F_2 / O_2 plasma. The S/D metal serves as the mask. During RIE, CCl_2F_2 = 70 sccm, O_2 = 10 sccm, gas pressure = 100 mTorr and RF power = 100W. The etching rate is ~0.05 nm / sec. The deposition and etching steps for the dry-etch process are now completed.



Dry-etch (done)

Fig. 3.15. Schematic top view of dry-etched TFTs after Step 8.

3.3 *Comparison of dry-etch and wet-etch processes*

Dry-etch and wet-etch fabrication processes have the same deposition steps. There are four plasma etching steps in dry-etch fabrication process, which were replaced with wet-etching methods for wet-etched a-Si TFTs (Table 3-I). The wet-etch process has one etching step less than the dry-etch process due to the use of the shadow mask.

Table 3-I. Comparison of dry-etching and wet-etching steps

	Plasma etching Step in dry-etching	**Dry-etching**		**Wet-etching**	
		Mask	**Etchant**	**Mask**	**Etchant**
1	Passivation SiN_x etch	Photoresist	Plasma	Photoresist	HF
2	Channel a-Si etch	Photoresist	Plasma	Passivation SiN_x	KOH
3	n+ a-Si etch	Photoresist	Plasma	S/D Cr	KOH
4	Gate SiN_x via etch	Photoresist	Plasma	Shadow mask	N/A

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Two-Stage Model for Lifetime Prediction of Highly Stable a-Si TFTs

In n-channel amorphous-silicon thin-film transistors (a-Si TFTs), the threshold voltage increases under positive gate bias, leading to the decreased drain current. As pointed out in Chapter 1, this instability issue in the a-Si TFT hinders its further application in large area electronics. This chapter first discusses the modeling for two instability mechanisms in a-Si TFTs – defect creation in a-Si and charge trapping in the gate silicon nitride (SiN_x). Then a two-stage model is presented for the reliability characterization and lifetime prediction of highly stable a-Si TFTs under low gate-field stress.

Two stages of the threshold voltage shift are identified from the decrease of the drain saturation current under low gate-field stress. The first initial stage dominates up to hours or days near room temperature and it can be characterized with a stretched-exponential model. The second stage dominates in the long term and then saturates, corresponding to the breaking of weak bonds in a-Si. It can be modeled with a "unified stretched exponential fit," in which a thermalization energy is used to unify experimental measurements of drain current decay at different temperatures into a single curve.

4.1. *Instability mechanisms in a-Si TFTs*

It is well established that two mechanisms can be responsible for the instability corresponding to the threshold voltage rise: (i) defect creation in a-Si [1-3], and (ii) charge trapping in the gate SiN_x [4-8]. In mechanism (i) [1], channel electrons induce the weak Si-Si bonds to break and form dangling bonds, which then trap electrons and become negatively charged. In mechanism (ii) [8], channel electrons which leak into the gate silicon-nitride (SiN_x) are captured by traps in the SiN_x. As we review below, the threshold shift vs. time caused by these two mechanisms can both be characterized by a "stretched exponential expression" [1, 8].

4.1.1 *Modeling defect creation in a-Si*

Electrons in the channel induce weak Si-Si bonds to break into dangling bonds (Fig. 4.1). This process is reversible unless the dangling bonds relax into stable configurations. Two alternative models explain this defect relaxation kinetics – hydrogen-diffusion-controlled defect-relaxation (HCR) and defect-controlled defect-relaxation (DCR). In the HCR model, a hydrogen atom

diffuses to the site, attaches itself to one of the dangling bonds, and thereby separates the two dangling bonds [9-11]. In the DCR model, the two dangling bonds relax locally without the aid of a diffusing atom [12].

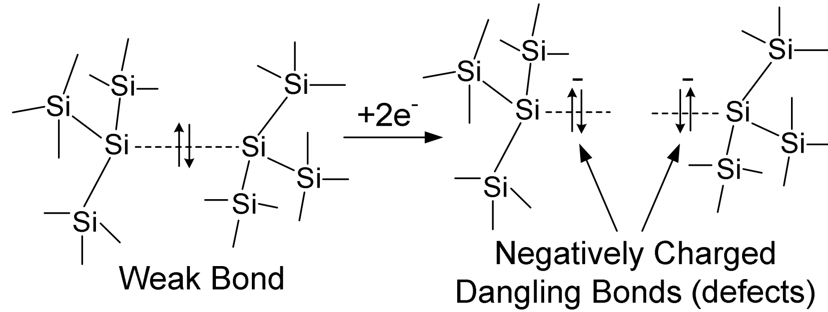


Fig. 4.1. Defect creation in a-Si [13].

– **Modeling threshold voltage shift**

In the DCR model, defect creation in a-Si is modeled as a transition in energy from an initial weak bond state to stabilized but metastable dangling bond states [12]. In the two-level configuration coordinate diagram (Fig. 4.2), state A is the weak bond state and state B is the dangling bond state.

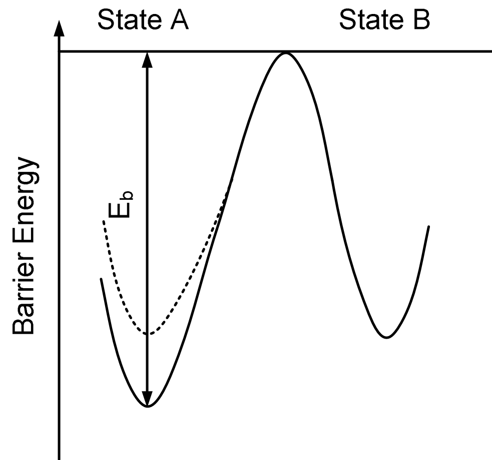
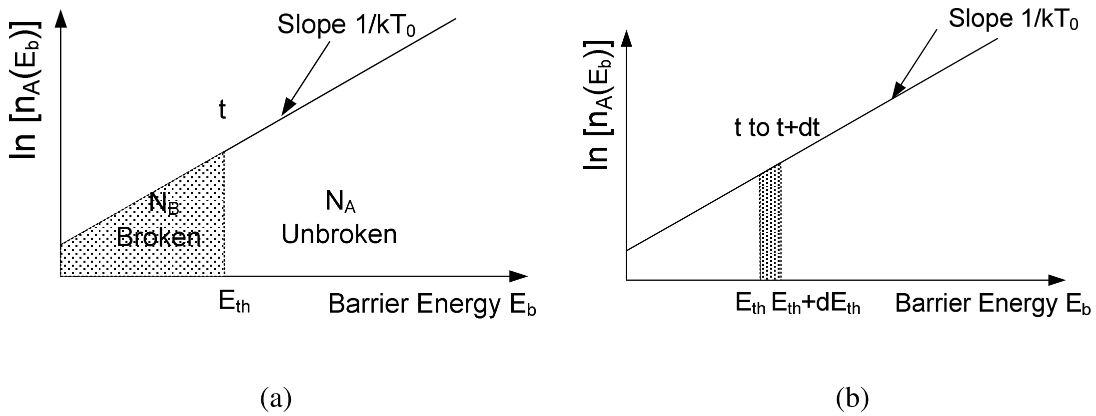


Fig. 4.2. Two-level configuration coordinate diagram for metastability in a-Si. State A represents the weak bond state, and state B represents the dangling bond state. E_b is the barrier-breaking energy.

Because of variations of bond lengths and bond angles in a-Si, the number of weak bonds per unit energy per unit volume n_A with breaking-barrier energy E_b has an exponential distribution in fresh a-Si TFTs before stress (Fig. 4.3) [12, 14]

$$n_A(E_b) = C_0 e^{E_b/kT_0} \quad (4.1)$$



(a) (b)

Fig. 4.3. Logarithm of the number of weak bonds per unit energy per unit volume n_A. (a) Schematic distribution of the volume density of weak bonds N_A and broken bonds N_B in the valence band tail of a-Si; and (b) illustration of the progress of bond breaking with increasing duration t of gate-bias stress, expressed as $E_{th} = kTln(\nu t)$.

This distribution means that few very weak bonds are easily broken (dotted curve in Fig. 4.2) and an increasing number of stronger bonds are harder to break. The characteristic temperature T_0 reflects the degree of disorder. A low value of T_0 implies a steep tail in the energy distribution of weak bonds [15].

The transition from the weak bond state to the dangling bond state is thermally activated (Fig. 4.2), with a characteristic time $\tau(E_b)$

$$\tau(E_b) = \nu^{-1}\exp\left(E_b/kT\right) \quad (4.2)$$

ν is the attempt-to-escape frequency. Transitions over low energy barriers are frequent, while those over high energy barriers are rare.

To a first-order approximation, at time t, weak bonds with a characteristic time $\tau(E_b)$ less than the time t will all have been broken, and those with a characteristic time $\tau(E_b)$ larger than t will

not yet have been broken. This statement can also be expressed in terms of a "thermalization energy" E_{th} [16], which is defined as $E_{th} \equiv kT\ln(\nu t)$ (4. 3)

At time *t*, we can approximate that weak bonds with a barrier energy E_b less than E_{th} will have been broken and the stronger bonds above E_{th} will be intact (Fig. 4.3 (a)). It follows that between time t and $t + dt$ bonds with barrier energies between E_{th} and $E_{th} + dE_{th}$ will break (the shaded region in Fig. 4.3(b)).

Defining $N_B(t)$ as the number of broken bonds per unit volume, the defect creation rate is then $\frac{\mathrm{d}N_B(t)}{\mathrm{d}t} = \frac{\mathrm{d}N_B}{\mathrm{d}E_{th}}\frac{\mathrm{d}E_{th}}{\mathrm{d}t}$ (4. 4)

The area of the shaded region in Fig. 4.3(b) is

$$\mathrm{d}N_A(E_{th}) = n_A(E_{th})\mathrm{d}E_{th} \quad (4.\ 5)$$

Because one weak bond breaks into two dangling bonds, we have $\mathrm{d}N_B(E_{th}) = 2\mathrm{d}N_A(E_{th})$. Here we relate the weak bond states to the created dangling bond states with a ratio of 1 : 2.

Thus the defect creation rate with thermalization energy is

$$\frac{\mathrm{d}N_B}{\mathrm{d}E_{th}} = 2n_A(E_{th}) = 2C_0e^{E_{th}/kT_0} \quad (4.\ 6)$$

Combined with (4. 2), the defect creation rate is

$$\frac{\mathrm{d}N_B(t)}{\mathrm{d}t} = \frac{\mathrm{d}N_B}{\mathrm{d}E_{th}}\frac{\mathrm{d}E_{th}}{\mathrm{d}t} = 2C_0kT\nu(\nu t)^{T/T_0-1} \quad (4.\ 7)$$

Experiments show that the defect creation rate increases with the applied gate voltage V_{GS} [17, 18]. Often the defect creation rate is assumed to be proportional to the number of channel electrons per unit volume n_{ch} [12, 18], because electrons induce the weak bond to break [12, 16, 18, 19]. After factoring the electron volume density n_{ch} into (4. 7), the defect creation rate as a function of time becomes

$$\frac{\mathrm{d}N_B(t)}{\mathrm{d}t} = C_1n_{ch}(t)kT\nu(\nu t)^{T/T_0-1} \quad (4.\ 8)$$

C_1 is a new constant.

Because channel electrons are captured by the dangling bonds and raise the threshold voltage, the threshold voltage is related to the number of dangling bonds per unit volume by

$$V_T(t) = q\int N_B(t)\mathrm{d}x\,/C_{ins} \qquad (4.\ 9)$$

C_{ins} is the capacitance of the gate SiN_x and the integration is along the channel thinkness x. Here we assume that the defects in the a-Si are created very close to the SiN_x / a-Si interface. At constant gate-source bias V_{GS}, we have

$$\int n_{ch}(t)\mathrm{d}x = C_{ins}[V_{GS} - V_T(t)]/q \qquad (4.\ 10)$$

Substituting (4. 9) and (4. 10) into (4. 8) leads to a stretched exponential expression for the threshold voltage shift vs. time

$$\Delta V_T(t) = V_T(t) - V_{T0} = (V_{GS} - V_{T0})\left\{1 - \exp\left[-\left(\frac{t}{\nu^{-1}\exp\left(E_{act}/kT\right)}\right)^{T/T_0}\right]\right\} \qquad (4.\ 11)$$

V_{T0} is the initial threshold voltage before the application of gate bias, and the activation energy $E_{act} = -kT_0\ln(C_1kT_0)$.

To simplify the formulation of (4. 11), we define

$$\Delta V_{Tmax} \equiv V_{GS} - V_{T0} \qquad (4.\ 12)$$

because in a given experiment ΔV_T cannot exceed $V_{GS} - V_{T0}$,

$$t_0 \equiv \nu^{-1}\exp\left(E_{act}/kT\right) \qquad (4.\ 13)$$

and

$$\beta \equiv T/T_0 \qquad (4.\ 14)$$

Which leads to (4. 15)

$$\Delta V_T(t) = \Delta V_{Tmax}\left\{1 - \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right]\right\} \qquad (4.\ 15)$$

β is the ratio of kT to the characteristic energy of the distribution of the weak bonds and β decreases as the distribution broadens.

Initially, the threshold voltage shift ΔV_T is zero and then it rises because the exponential term in (4. 15) becomes smaller. For $t > t_0$, the exponential term is so insignificant that ΔV_T saturates. When $t = t_0$, $\Delta V_T(\,t_0) = \Delta V_{Tmax}(1 - \exp(-1)) \approx 0.63\Delta V_{T,max}$ and $E_{th} = E_{act}$. The term "activation energy" E_{act} , as it is known in literatures on stretched exponential processes, does not imply a single energy barrier as in a conventional Arrhenius relation. Rather, E_{act} is closely related to the maximum energy barrier surmountable on the time scale of the experiment [2].

The hydrogen-diffusion-controlled defect-relaxation (HCR) model [9-11] also leads to (4. 15), if we assume the diffusion of hydrogen is a thermally activated process with a barrier energy E_b and the density of hydrogen atoms with diffusion energy barrier E_b has an exponential function $n_A(E_b) = C_0 e^{E_b/kT_0}$. Thus, for the purpose of fitting experimental results, defect-controlled defect-relaxation (DCR) model and the hydrogen-diffusion-controlled defect-relaxation (HCR) model are equivalent. For the rest of this thesis, we will use the terminology associated with the DCR model.

– **Modeling drain current degradation in saturation**

One important application of stable a-Si TFT's is to drive OLEDs in flat panel displays [13, 20]. In this case the a-Si TFT is usually biased in saturation to operate as a current source. When the threshold voltage shifts, the drain current $I_D(t)$ responds as:

$$I_D(t) = \frac{1}{2}\mu_n C_{ins}\frac{W}{L}[V_{GS} - (V_{T0} + \ \Delta V_T(t))]^2 \qquad (4.\ 16)$$

Since changes of mobility reduces the drain current much less than changes of threshold voltage [15], we neglect mobility change in our analysis.

We define the "normalized drain current" $I_{D,nor}(t)$ as the ratio of drain current at time t to that at the beginning of the stressing period,

$$I_{D,nor}(t) \equiv I_D(t)/I_D(t = 0) \qquad (4.\ 17)$$

Combining this with (4. 15) and (4. 16), the normalized drain current as a function of time then analytically becomes [21]

$$I_{D,nor}(t) = \exp\left[-2\left(\frac{t}{t_0}\right)^{\beta}\right] \qquad (4.\ 18)$$

Strictly speaking, in saturation the electron density in the channel and therefore the rate of threshold voltage shift will vary along the channel, whereas (4. 15) assumes a uniform electron density and a uniform rate of threshold voltage shift along the channel. Thus, (4. 15) cannot rigorously be applied to TFTs operating in saturation. To clarify this issue, we experimentally measured the threshold voltage shift in a-Si TFTs in the linear region at small drain voltage, and the threshold voltage shift in saturation under the same gate voltage (Fig. 4.4).

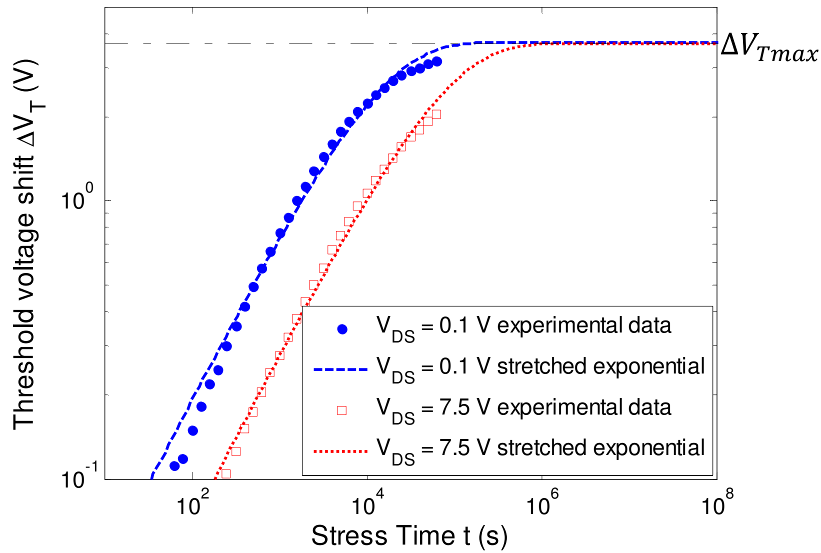


Fig. 4.4. Threshold voltage shift vs. time in linear and saturation mode of the same V_{GS} =5 V at 120°C. In the linear mode at V_{DS} = 7.5 V (solid dots and dashed curve): ΔV_{Tmax} = 3.8 V, β = 0.6, and $t_0 = 1.2 \times 10^4$ s. In the saturation mode at V_{DS} = 7.5 V (open squares and dotted curve): ΔV_{Tmax} = 3.8 V, β = 0.6, and $t_0 = 6.6 \times 10^5$ s.

By "threshold voltage" in saturation, we assumed that the TFT during degradation could still be modeled by the usual "square law" relation (4. 16), with a single effective threshold voltage for the entire device, and attributed all the decrease in the drain current in saturation to an increase in this effective threshold voltage. Under the same V_{GS}, the two threshold shifts vs. time in Fig. 4.4 both exhibit the stretched exponential dependence as in (4. 15) with the same β and $\Delta V_{T,max}$, but with a different t_0 [1]. t_0 is larger for TFT in saturation. In this Chapter we use (4. 18) as a closed form for the degradation of the normalized drain current in saturation, and fits it to

experimental measurements in Section 4.3. In Chapter 7, the dependence of drain current degradation and threshold voltage shift on the drain-bias will be addressed in detail.

4.1.2 *Modeling charge trapping in the gate SiNx*

When channel electrons enter the gate insulator and then are captured by traps there, the threshold voltage shifts (Fig. 4.5).

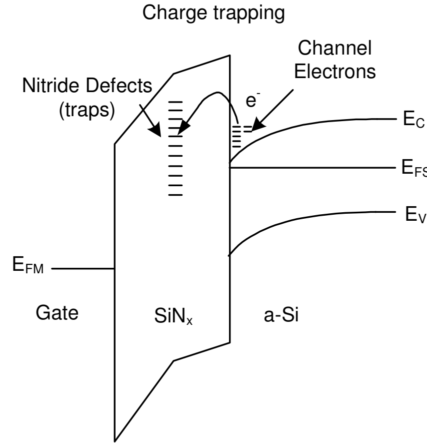


Fig. 4.5. Charge trapping in gate SiN_x [13].

If one assumes that all electrons that enter the insulator are trapped, the threshold voltage shift depends strictly on the process of electron tunneling into the gate insulator, and has a logarithmic time dependence [5].

$$\Delta V_T(t) = r_d \log(1 + t/t_0) \quad (4.\ 19)$$

The constant r_d contains the density of traps N_T [cm^{-3}] and a tunneling constant λ [cm] [5]. This tunneling mechanism typically dominates at high-gate field (> 10^6 V/cm) [13, 20] and produces a weak temperature dependence [5].

On the other hand, if most electrons that enter the gate insulator are not trapped and continue to the gate electrode, the threshold voltage shift can be shown to follow the stretched exponential expression as (4. 15) [5, 6, 8, 22]. This expression can be derived by assuming a continuous distribution in the capture cross section of the trapping sites [8]. The parameters ΔV_{Tmax} , β and t_0 in (4. 15), which characterize charge trapping in the gate SiN_x, have physical origins that are different from those to characterize defect creation in a-Si. When all traps in the SiN_x are filled,

the threshold voltage shift saturates and reaches ΔV_{Tmax} . Thus, the parameter $\Delta V_{Tmax} = qN_{tot} < d > /\varepsilon \cdot area$, where N_{tot} is the total density of traps, $< d >$ is the centroid of trapped charge measured from the gate metal, and ε is the permittivity of the gate SiN_x. β is a measure of the distribution width of capture cross section, with a value between 0 and 1. β decreases as the distribution broadens, and $\beta = 1$ implies a single trap cross section. In principle, the characteristic time t_0 can be determined from the gate leakage current and characteristic capture cross section for the ensemble of traps [8]. In practice, t_0 is determined from (4. 15) as the time when $\Delta V_T = 0.63\ \Delta V_{Tmax}$. Because gate leakage current and capture cross section may depend on temperature [8], the threshold voltage shift also may depend on temperature.

The above charge-trapping model, based on continuous distribution in trapping capture cross section, was first derived to explain the threshold voltage shift in single crystalline Si field-effect transistors with high permittivity dielectric gate insulator, such as Al_2O_3 and H_fO_2. When applied to a-Si TFTs with SiN_x gate insulator, the stretched exponential form of (4. 15) has also results in good fits to experimental data, although without connecting to an explicit physical model.

4.1.3 *Summary of instability models for a-Si TFTs*

A conclusion from the previous two sections is that the stretched exponential expression (4. 15) can be used to model the threshold voltage shift caused by either defect creation in a-Si or charge trapping in the gate SiN_x. The model requires three parameters ΔV_{Tmax}, β and t_0, which are listed in Table 4-I. They are used to describe the threshold voltage shift vs. time at a given temperature. It is difficult to determine which instability mechanism is operating in a-Si TFTs from simply observing the threshold voltage shift [22]. However as noted in Section 4.1.1, for defect creation in a-Si, we expect $\Delta V_{Tmax} = V_{GS} - V_{T0}$, while for charge trapping in SiN_x, ΔV_{Tmax} could be less than $V_{GS} - V_{T0}$ if the number of traps in the gate insulator is small. Such an observation in practice would allow one to differentiate between the two instability mechanisms. Furthermore, defect spectroscopy techniques [23] would allow one to observe the newly created defect states in a-Si. In Chapter 6, field-effect technique proves that defect creation occurs in a-Si TFTs under low gate-field.

Table 4-I. Stretched exponential expression for instability mechanisms in a-Si TFTs

$\Delta V_T(t) = \Delta V_{Tmax}\left\{1 - \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right]\right\}$		
Parameter	**Defect creation in a-Si (Stage II)**	**Charge trapping in gate SiN_x (Stage I)**
ΔV_{Tmax}	$V_{GS} - V_{T0}$	$qN_{tot} < d >/\varepsilon \cdot area$
β	A measure of the distribution of barrier energy E_b with $\beta = T/T_0$	A measure of width of the distribution of the capture cross section $0 \leq \beta \leq 1$
t_0	Time scale to reach $\Delta V_{T,max}$. Depends on the attempt-to-escape frequency ν, activation energy E_{act}, and temperature T, with $t_0 = \nu^{-1}\exp(E_{act}/kT)$	Time scale to reach $\Delta V_{T,max}$. Depends on the gate leakage current and characteristic capture cross section

4.2. *Sample preparation and bias-temperature-stress measurement*

Highly stable a-Si TFTs were fabricated with a standard bottom-gate non-self-aligned process in the back-channel passivated (BCP) structure. The silicon nitride and amorphous silicon were deposited in a plasma-enhanced chemical vapor deposition (PECVD) system. 300-nm gate nitride, 200-nm intrinsic hydrogenated a-Si and 300-nm passivation nitride were deposited sequentially at 320°C, 320°C and 220°C, respectively. A dry-etching process as described in Chapter 3 was performed to pattern the silicon nitride and a-Si. All the samples were annealed at 180°C for an hour to remove the plasma-induced damage from the dry-etching process [15]. After annealing, the initial threshold voltage V_{T0} was 1.0 V and electron mobility μ_n was 0.9 $cm^2/V \cdot s$.

The TFTs were biased in the saturation mode with a constant gate voltage of 5 V (a gate field of ~1.5×10^5 V/cm) and a constant drain voltage of 7.5 V. Saturation, as opposed to linear mode, was used because this mode of operation is used for driving OLEDs, an application which demands very high stability [13]. We raised the substrate temperature from 20°C to 140°C in steps of 20°C. At each temperature we biased a fresh TFT on the same substrate without any prior stress and again measured the drain current as a function of time. At the end of the continuous bias stress period, a gate-bias voltage sweep and fixed drain voltage were applied to

measure the I_D - V_G characteristics of the TFTs [15]. This allowed us to measure the mobility of the TFT at the end of the stress period. The experimental data of normalized drain current $I_{D,nor}(t) \equiv I_D(t)/I_D(t=0)$ as a function of time at different temperatures are shown with open squares in Fig. 4.6.

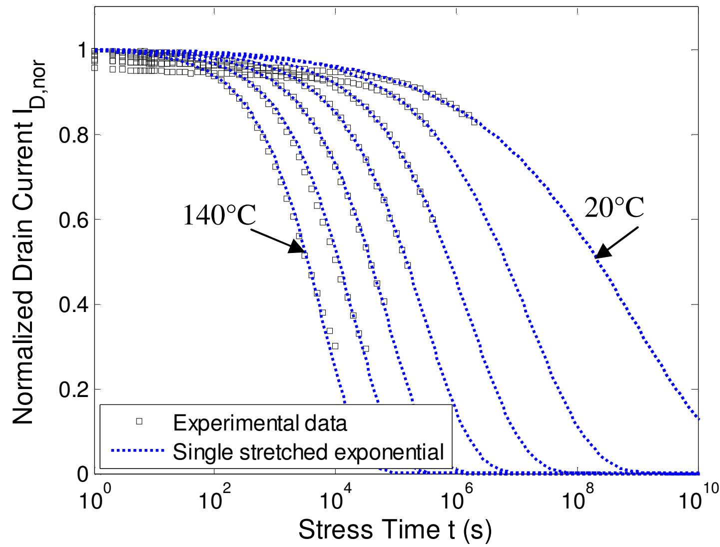


Fig. 4.6. Single stretched exponential fits to normalized drain current data at temperatures from 20°C to 140°C in steps of 20°C.

4.3. *Two-stage model for lifetime prediction*

It has been shown that defect creation in a-Si and charge trapping in the gate SiN_x can both be modeled with a stretched exponential expression with a stretched exponential expression. In this section, single stretched-exponential fit is tried to model the drain current degradation first. Next, a "unified stretched exponential fit" to the drain current degradation caused by defect creation in a-Si is proposed. The unified stretched exponential fit agrees well with the experimental data in the temperature range from 80°C to 140°C. At lower temperatures (20°C to 60°C), the drain current degradation approaches the model only at long times. A different instability mechanism contributes in the beginning (Stage I), in addition to the unified stretched exponential model (Stage II). By subtracting the threshold voltage shift of the unified stretched exponential fit from the total threshold voltage shift data, we identify and characterize the Stage I.

4.3.1 *Single stretched-exponential fit*

Fig. 4.6 shows that at 5 V gate bias, the drain current approaches zero at long times and depends strongly on temperature. We fit the stretched exponential expression of (4. 15) for defect creation in a-Si to the experimental data for each temperature (dotted curves in Fig. 4.6). Each temperature requires separate fitting parameters $T_0 \equiv T/\beta$ and t_0, which are plotted in Fig. 4.7 and Fig. 4.8, respectively.

Fig. 4.7 shows that the characteristic temperature T_0 of the defect energy distribution changes from 1032 K at 20°C to 616 K at 140°C, and that it decreases rapidly in low temperature range. Similar results were reported in [6, 21]. From the slope of the Arrhenius plot of $\log t_0$ (straight line in Fig. 4.8), the activation energy $E_{act} = 0.89$ eV and the attempt-to-escape frequency $\nu = 4 \times 10^6$ Hz are extracted from (4. 13) $t_0 \equiv \nu^{-1}\exp\left(E_{act}/kT\right)$. However, the experimental t_0 at low temperatures does not fall on the straight line.

From the discussion of instability in a-Si of Section 4.1.1, the anomalously large T_0 and t_0 near room temperature result from either changes in material properties with temperature, or a single stretched exponential fit not being appropriate for the entire temperature range. In Section 4.3.4, we will show that material properties do not change. Another instability mechanism relevant near room temperature for short time makes the single stretched exponential fit inadequate.

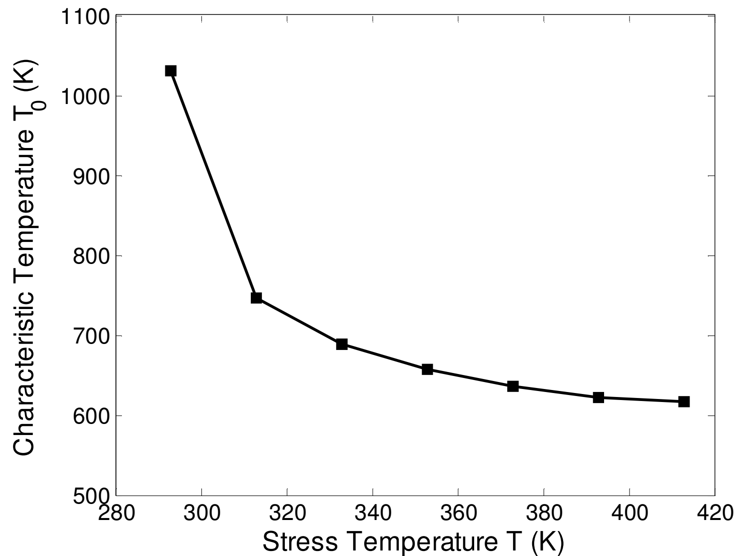


Fig. 4.7. Fitting parameter characteristic temperature T_0 as a function of bias stressing temperature.

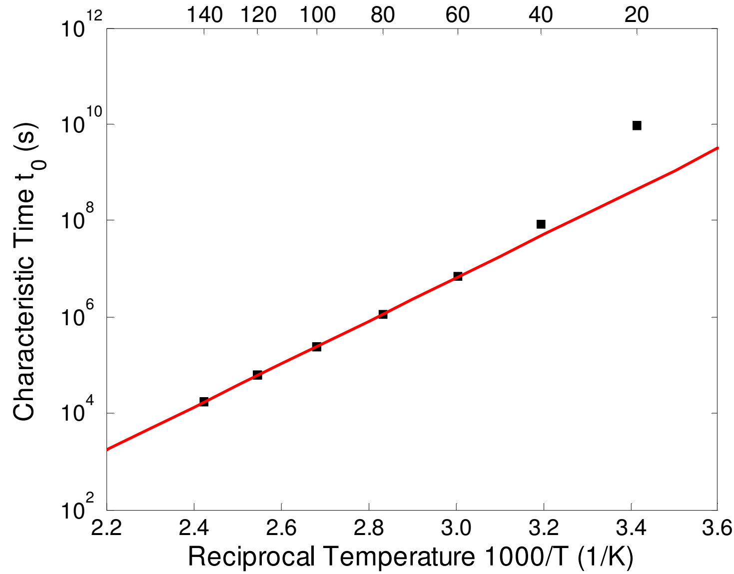


Fig. 4.8. Fitting parameter characteristic time t_0 as a function of reciprocal temperature in an Arrhenius plot. $E_{act} = 0.89$ eV and $\nu = 4 \times 10^6$ Hz.

4.3.2 *Unification of time and temperature*

If the instability is caused by defect creation in a-Si and the material properties do not change with temperature, it can be captured with a formulation that unifies time and temperature dependence. The definition of the thermalization energy E_{th} of (4. 3) implies that the time scale can be converted to the E_{th} scale. Doing that enables reducing all sets of current vs. time data for different temperatures to a single curve [16]. As discussed in Section 4.1.1, for a given thermalization energy a given number of bonds has been broken, leading to a specified change in threshold voltage and drain current. As time t advances and weak bonds with higher barrier energy E_b are broken, the thermalization energy E_{th} increases. Schematically, this is represented by an increase to the area of the shaded region in Fig. 4.3(a). Temperature affects only how long it takes to reach a given thermalization energy.

When ν is set to be 5×10^6 Hz, all experimental data on drain current degradation from 20°C to 140°C cluster as shown by the open squares in Fig. 4.9.

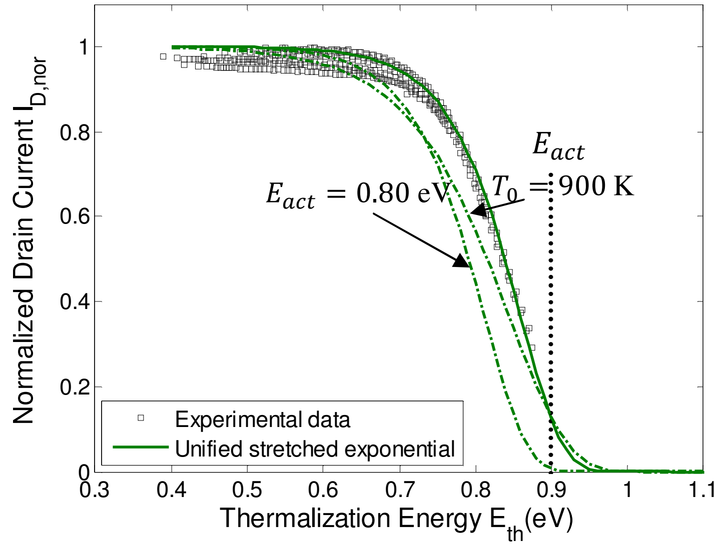


Fig. 4.9. Normalized drain current $I_{D,nor}$ unified in terms of the thermalization energy $E_{th} = kTln(\nu t)$, with $\nu = 5 \times 10^6$ Hz, and unified stretched exponential fit with parameters $E_{act} = 0.90$ eV and $T_0 = 643$ K (solid curve). Dash dotted curves are unified stretched exponential models at different E_{act} or T_0, to show the effect on $I_{D,nor}$.

The fitting parameter ν is close to that obtained from Fig. 4.8 of 4 × 10^6 Hz. This agreement suggests that the material properties remain essentially unchanged between 20°C and 140°C in our experiment. This observation gives us confidence for applying the unified stretched exponential fit to drain current degradation that follows.

4.3.3 *Unified stretched exponential fit (Stage II model)*

By substituting (4. 3) $E_{th} = kT\ln(\nu t)$, (4. 13) $t_0 = \exp(E_{act}/kT)$, and (4. 14) $\beta = T/T_0$ into (4. 18), we obtain the unified stretched exponential expression for $I_{D,nor}$ as a function of thermalization energy E_{th}

$$I_{D,nor}(E_{th}) = \exp\left\{-2\exp\left[\frac{E_{th}-E_{act}}{kT_0}\right]\right\} \quad (4.\ 20)$$

The activation energy E_{act} is the barrier energy for defect creation when the normalized drain current has droped to $e^{-2} \approx 0.135$. As discussed in Section 4.1.1, E_{act} is related to the maximum energy barrier surmountable on the time scale of the experiment [2]. Note that this unified stretched exponential expression is independent of temperature.

The solid curve in Fig. 4.9 shows that (4. 20) provides an excellent fit to the clustered data. The fitting parameters are $E_{act} = 0.90$ eV and $T_0 = 643$ K, which are typical values for a-Si [19]. The dash-dotted curves in Fig. 4.9 are plotted for $E_{act} = 0.80$ eV and $T_0 = 900$ K to show the effect of varying E_{act} and T_0 on the curve fit. Varying the activation energy E_{act} is seen to shift the current degradation, while varying the characteristic temperature T_0 affects the slope.

The relation of $E_{th} = kT\ln(\nu t)$ between thermalization energy and time enables plotting stretched exponential fits in a direct function of time as shown by dotted curves in Fig. 4.10. The experimental data fit well at high temperatures from 80°C to 140°C. At low temperatures, the experimental drain currents degradation lie below the unified stretched exponential fit at short times, but trend toward the unified stretched exponential fit at long times. These observations suggest that an additional instability mechanism causes the drain current to drop at the beginning of the tests. This initial instability mechanism, which is manifest at low temperatures and short times, requires an additional physical model.

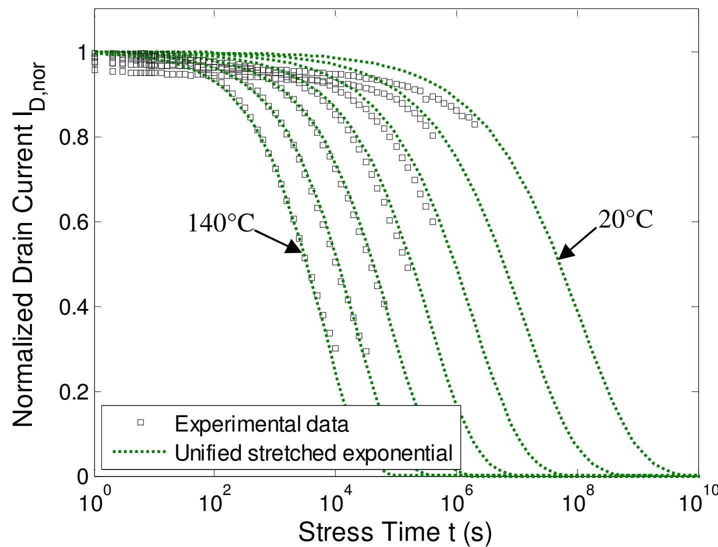


Fig. 4.10. Unified stretched exponential fits (Stage II) vs. stress times to experimental data from 20°C to 140°C in steps of 20°C, with fitting parameters $\nu = 5 \times 10^6$ Hz, $E_{act} = 0.9$ eV and $T_0 =$ 643 K.

4.3.4 *Two-stage model*

In order to model the initial additional instability at low temperatures, we define the threshold voltage shift caused by the initial instability mechanism as $\Delta V_{T,I}(t)$ (Stage I), and add it to the long-term threshold voltage shift characterized by the unified stretched exponential model $\Delta V_{T,II}(t)$ (Stage II), to obtain the total threshold voltage shift $\Delta V_{T,total}(t)$

$$\Delta V_{T,total}(t) = \Delta V_{T,I}(t) + \Delta V_{T,II}(t) \qquad (4.\ 21)$$

We first analyze the threshold voltage shift at 20°C, where the initial instability is most pronounced. Fig. 4.11 shows the experimental data points and model fits at 20°C. Open squares are the experimental data for $\Delta V_{T,total}(t)$ extracted from the measured drain current data using (4. 16). The dotted curve in Fig. 4.11 is from the unified stretched exponential fit in Section 4.3.3., that is now referred as the Stage II model. At long times, the Stage II model approaches the experimental data. However, at short times (< 10^3 seconds), a fast initial mechanism makes the threshold voltage shift rise above the unified stretched exponential fit. Stage I degradation saturates at the maximum threshold voltage shift $\Delta V_{Tmax,I}$, which is marked in Fig. 4.11. $\Delta V_{T,II}(t)$ for Stage II is obtained from (4. 15) with $\Delta V_{Tmax,II} = V_{GS} - V_{T0} - \Delta V_{Tmax,I}$. By subtracting $\Delta V_{T,II}(t)$ from the total threshold voltage shift vs. time data, $\Delta V_{T,I}(t)$ is obtained. While the mechanism of Stage I is not known, we fit the $\Delta V_{T,I}(t)$ data also with the stretched exponential expression (4. 15).

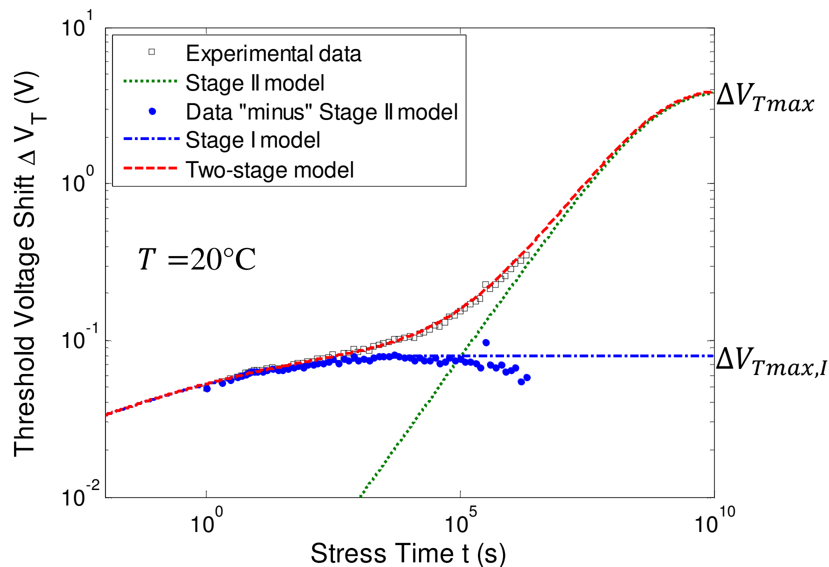


Fig. 4.11. Two-stage model fits to threshold voltage shift vs. time at 20°C (dashed curve, overlaps with Stage I curve at lower left and overlaps with Stage II curve at upper right). The dots for Stage I "data" result from subtracting the Stage II model (determined by high temperature experiments) from the experimental data. The fitting parameters for Stage I are $\Delta V_{Tmax,I} = 0.08$ V, $t_{0,I} = 0.7$ sec and $\beta_I = 0.15$; and for Stage II are $t_{0,II} = 5.2 \times 10^8$ sec and $\beta_{II} = 0.46$.

From Section 4.3.3, the fitting parameters are $\nu = 5 \times 10^6$ Hz, $E_{act} = 0.9$ eV and $T_0 = 643$ K, corresponding to $t_{0,II} = 5.2 \times 10^8$ sec and $\beta_{II} = 0.46$ at 20°C for Stage II. In Fig. 4.11, we choose $\Delta V_{Tmax,I} = 0.08$ V. $\Delta V_{T,I}(t)$ is plotted with solid dots and saturates at 0.08 V. It means the choice of $\Delta V_{Tmax,I} = 0.08$ V is proper. Taking the empirical approach, we find that $\Delta V_{T,I}(t)$ can be fitted with the stretched exponential model (4. 15) with the parameters $\Delta V_{Tmax,I} = 0.08$ V, $t_{0,I} = 0.7$ sec and $\beta_I = 0.15$, shown with the dash-dotted curve in Fig. 4.11. The two-stage fit of the dashed curve then is obtained by adding Stage I fit and Stage II fit. The result agrees well with the experimental data taken at 20°C over the entire measurement time.

We also applied the two-stage model to the experimental data taken at temperatures from 40°C to 140°C. The maximum threshold voltage shift in Stage I $\Delta V_{Tmax,I}$ varies with temperature as illustrated in Fig. 4.12.

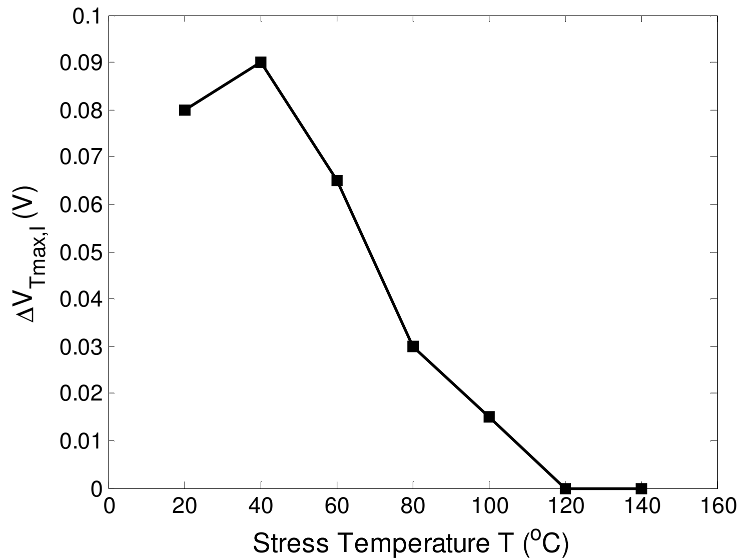


Fig. 4.12. Maximum threshold voltage shift in Stage I $\Delta V_{Tmax,I}$ at temperatures from 20°C to 140°C.

At high temperatures, it decreases to zero. After converting the threshold voltage back to drain current via (4. 16), the two-stage fits to the normalized drain current degradation from 20°C to 140°C are shown in Fig. 4.13. The fits agree well with the experimental data at all temperatures and times, clearly better than the single stretched exponential fits of the dotted curves in Fig. 4.6 or the unified stretched exponential fits (Stage II only) of the dotted curves in Fig. 4.10.

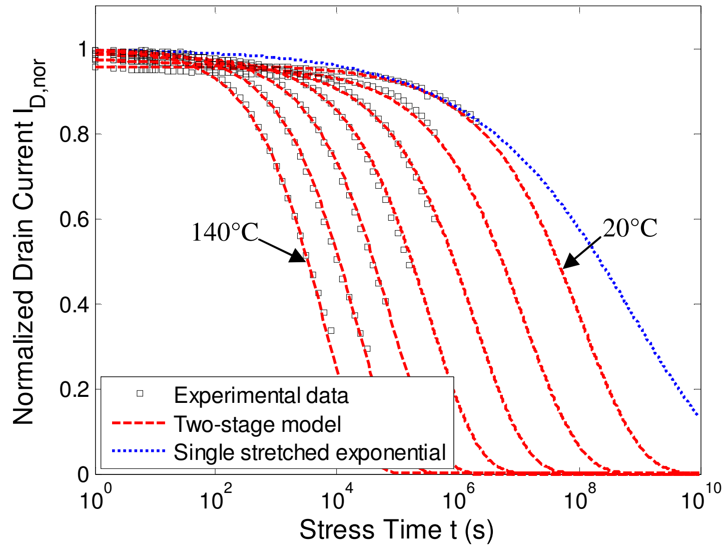


Fig. 4.13. Two-stage model fit to experimental data from 20°C to 140°C in steps of 20°C (dashed curves), and the single stretched exponential fit at 20°C (dotted curve at right).

4.4. *Discussion*

– Two-stage model

From Section 4.3, we know that the unified stretched exponential fits Stage II from 80°C to 140°C, but does not agree well with the experimental data at low temperatures from 20°C to 60°C. Fig. 4.12 tells us that the maximum threshold voltage shift in Stage I $\Delta V_{max,I}$ is negligible at high temperatures. The reason is that the threshold voltage shift in Stage I occurs so fast that above 60°C the Stage I mechanism has already saturated by the time we took our initial drain current data point, about 0.1 sec after the gate and drain bias were applied to get the first data point. Therefore, at elevated temperatures Stage II can be modeled reliable with the unified stretched exponential, because the effect of Stage I can be neglected. In summary, the unified

stretched exponential fit of (4. 19) can be used to model Stage II, and Stage I can be modeled with the stretched exponential expression of (4. 15). Because Stage I saturates at $\Delta V_{Tmax,I}$ noticeable below $V_{GS} - V_{T0}$, we attribute the instability mechanism of Stage I to charge trapping in the gate SiN_x , where the trap density is grown-in and independent of the density of electrons in the channel. The threshold voltage shift in Stage II is attributed to defect creation in a-Si, which is induced by the density of electrons in the channel and therefore rises with rising gate bias.

The backward process is charge de-trapping for charge trapping and defect annealing for defect creation. In the presence of the channel electrons, rates of the backward processes are much lower than the rate of the corresponding forward processes [12, 24]. When the gate voltage is turned off, the threshold voltage recovers through the backward process. The two-stage model does not take into account of the backward processes in two stages.

– **Prediction of drain current lifetime**

At room temperature, the drain current degradation in Stage I is still fast and measured at short times. The current degradation in Stage II can be predicted from the unified stretched exponential fit to the experimental data at elevated temperatures. We define the time for the TFT drain current to drop to x% of its initial value under constant gate voltage bias as x% drain current lifetime ($\tau_{x\%}$). The lifetime at room temperature can be predicted from the two-stage model. Fig. 4.14 demonstrates the 90%, 70% and 50% lifetimes ($\tau_{90\%}, \tau_{70\%}, \tau_{50\%}$) measured in our experiment (open squares).

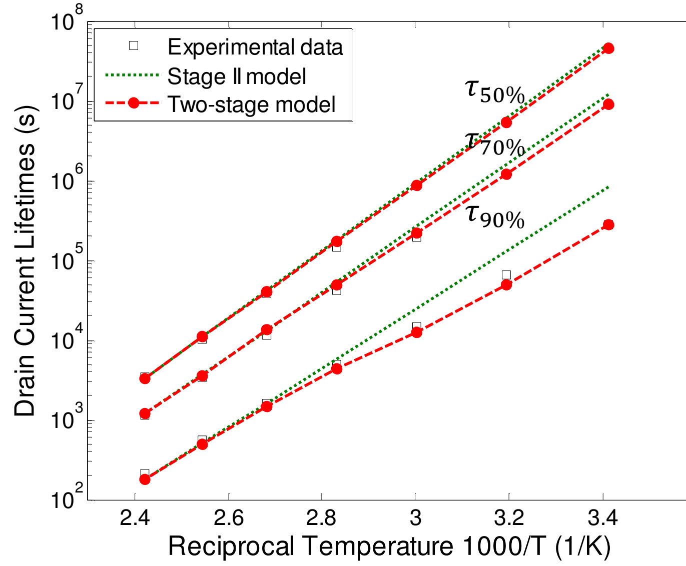


Fig. 4.14. Time at which the drain current drops to 50%, 70% and 90% of its initial value, in function of temperature. Open squares: experimental data; dotted lines: Stage II model with unified stretched exponential fit; solid dots and dashed lines: two-stage model.

The lifetimes extrapolated from only the Stage II model (unified stretched exponential fits, dotted lines) and the full two-stage model (solid dots and dashed lines). Since the threshold voltage shift in Stage I of our highly stable a-Si TFTs saturates at no more than 0.1 V, at long times the threshold voltage shift will be dominated by Stage II. The fitting parameters and the predicted 50% lifetimes are listed in Table 4-II.

Table 4-II. Fitting parameters and predicted 50% lifetime

Stage I			**Stage II**						**Two-stage**
$\Delta V_{Tmax,I}$ (V)	$t_{0,I}$ (s)	β_I	ν (Hz)	T_0 (K)	E_{act} (eV)	$t_{0,II}$ (s)	β_{II}	50% lifetime (s)	50% lifetime (s)
0.08	1.1	0.2	5×10^6	643	0.90	5.2×10^8	0.46	5.1×10^7	4.5×10^7

One conclusion of our work is that gate-bias stress test conducted at 20°C for times shorter than 10^6 seconds do not accurately predict the long term (Stage II) performance [13, 20, 25]. This conclusion is illustrated by the discrepancy between the dotted curve and the dashed curve in Fig. 4.13, both of which fit 20°C data.

In Fig. 4.14, note that the slopes of the Stage II model fit to the 90%, 70% and 50% lifetimes are different. The differences reflect that no single activation energy applies to the degradation of a-Si TFTs, in contrast to the conventional Arrhenius model that is applied to the thermal aging of many other electronic devices.

– **Extension to constant current stress**

In AMOLED pixel circuits with threshold voltage compensation, the gate voltage increases with the increasing threshold voltage, so the driver transistors are subject to constant current stressing [26, 27]. Since $V_{GS}(t) - V_T(t)$ is kept constant, from (4. 8) - (4. 10) threshold voltage shift in Stage II from defect creation follows a power law relationship [28]

$$\Delta V_T(t) = [V_{GS}(t) - V_T(t)]\left(\frac{t}{t_0}\right)^{\beta} \qquad (4.\ 22)$$

As in Section 4.3.2, the time scale can be converted to the thermalization energy E_{th} scale using (4. 3) $E_{th} = kT\ln(\nu t)$ to give

$$\Delta V_T(E_{th}) = [V_{GS}(E_{th}) - V_T(E_{th})]\exp\left[\frac{E_{th} - E_{act}}{kT_0}\right] \qquad (4.\ 23)$$

Thus, the room temperature threshold voltage shift in Stage II can be predicted from the threshold voltage shift at elevated temperatures. Note the electron density and the rate of threshold voltage shift are assumed to be uniform along the channel. The rigorous non-uniform channel analysis for TFTs biased in saturation should follow a similar analysis as in Chapter 7.

4.5. *Summary and conclusion*

We measured and modeled the drain current degradation and threshold voltage shift of a-Si TFTs under low gate-field stress between 20ºC and 140ºC. Over most of the time-temperature range, the unified stretched exponential model that reflects defect creation in the a-Si channel (Stage II) applies. Near room temperature, a separate mechanism contributes to TFT degradation. An empirical fit, with a stretched exponential, suggests that the underling mechanism is the charge trapping in the SiN_x gate insulator (Stage I). While this mechanism makes only a minor contribution to the overall threshold voltage shift and drain current degradation, it can considerably falsify TFT lifetimes extrapolated from tests done at room temperature. Because for

reasonable test duration (~1 month) at room temperature, it is not yet possible to accurately estimate the parameters which dominate the long term degradation.

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Optimization of Fabrication Conditions for Highly Stable a-Si TFTs

Chapter 4 presented the two-stage model for stability characterization and lifetime prediction of highly stable a-Si TFTs under low gate-field stress (~1.5×10^5 V/cm). In this chapter, two groups of experiments are presented to reduce the drain current instability of a-Si TFTs under prolonged gate bias. Deposition conditions for the silicon nitride (SiN_x) gate insulator and the a-Si channel layer were varied, and TFTs were fabricated with all reactive ion etch steps, or with all wet etch steps, the latter in a new process. The two stage model that unites charge trapping in the SiN_x gate dielectric and defect generation in the a-Si channel was used to interpret the experimental results. The optimal substrate temperature, gas flow ratios, and RF deposition power densities are identified. The stability of the a-Si channel depends also on the deposition conditions for the underlying SiN_x gate insulator, and TFTs made with wet etching are more stable than TFTs made with reactive ion etching.

5.1. *Introduction*

The a-Si TFT stability depends on their fabrication processes, in particular a-Si deposition conditions and etching methods. Among the deposition conditions, hydrogen dilution [1, 2] and ammonia to silane flow ratio for SiN_x gate insulator growth [2, 3], SiN_x deposition temperature [1-3], a-Si deposition temperature [4, 5] and hydrogen dilution [4, 6, 7] for a-Si growth have been shown to affect the stability of a-Si TFTs. Wet-etched a-Si TFTs [8] have been reported to be more stable than dry-etched TFTs. We present an extensive and systematic study of the relation between a-Si TFT stability and its fabrication processes. We varied both deposition conditions and etching methods, and linked their effects with the physical mechanisms that change the threshold voltage of a-Si TFTs during low gate bias. No comparable study exists in the a-Si literature.

In Chapter 4, we presented a two-stage model for characterizing stability and predicting lifetime of highly stable a-Si TFTs under low gate-field stress (~1.5×10^5 V/cm). We defined the time for the TFT drain current to drop to x% of its initial value under constant gate voltage bias as x% drain current lifetime ($\tau_{x\%}$). The drain current degradation is the result of the threshold voltage shift. The overall threshold voltage shift $\Delta V_{T,total}(t)$ of a-Si TFTs develops in two stages, which

are the fast initial threshold voltage shift $\Delta V_{T,I}(t)$ (Stage I) and the dominant long-term threshold voltage shift $\Delta V_{T,I}(t)$ (Stage II).

$$\Delta V_{T,total}(t) = \Delta V_{T,I}(t) + \Delta V_{T,II}(t) \quad (5.\ 1)$$

The threshold voltage shift in Stage I is most likely caused by charge trapping in SiN_x. It can be modeled with a stretched exponential model,

$$\Delta V_{T,I}(t) = \Delta V_{Tmax,I}\left\{1 - \exp\left[-\left(\frac{t}{t_{0,I}}\right)^{\beta_I}\right]\right\} \quad (5.\ 2)$$

The threshold voltage shift in Stage II $\Delta V_{T,2}(t)$ is caused by defect creation in a-Si also fits a stretched exponential expression

$$\Delta V_{T,II}(t) = (V_{GS} - V_{T0} - \Delta V_{Tmax,I})\left\{1 - \exp\left[-\left(\frac{t}{t_{0,II}}\right)^{\beta_{II}}\right]\right\} \quad (5.\ 3)$$

Here

$$t_{0,II} = \nu^{-1}\exp\left(E_{act}/kT\right) \quad (5.\ 4)$$

and

$$\beta_{II} = T/T_0 \quad (5.\ 5)$$

In this chapter, we use the two-stage model to characterize the stability of a-Si TFTs fabricated under various processes conditions. We first study the deposition conditions of dry-etched a-Si TFTs on stability. Then we investigate the dependence of stability on dry or wet etching.

5.2. *Effects of deposition conditions on a-Si TFT stability*

We studied the effect of plasma-enhanced chemical vapor deposition conditions on the stability of a-Si TFTs under low gate-field stress. All TFTs have gate nitride dielectric layers grown at 320°C and use the dry-etching process. In the gate SiN_x growth, we varied the hydrogen dilution and ammonia (NH_3) to silane (SiH_4) ratio. In the channel a-Si growth, we varied a-Si substrate temperature and hydrogen dilution. We also varied the deposition power for SiN_x and a-Si near the SiN_x / a-Si interface. The TFTs were biased in saturation with a constant gate-source voltage

of 5 V (a gate field of ~1.5×10^5 V/cm) and a constant drain-source voltage of 7.5 V. The drain current was measured at temperatures from 20°C to 140°C in steps of 20°C. The deposition conditions and the corresponding stability parameters extracted from the two-stage model at 20°C are listed in Table 5-I.

The stability in Stage I can be characterized by the maximum threshold voltage shift $\Delta V_{Tmax,I}$ and the characteristic time $t_{0,I}$. The a-Si TFTs with a good Stage I stability should have a small $\Delta V_{Tmax,I}$ and a big $t_{0,I}$. The stability in Stage II can be characterized by parameters $t_{0,II}$ and β_{II} obtained from the stretched exponential fit in (5. 3) from accelerated tests at high temperatures. $t_{0,II}$ and β_{II} are related to the attempt-to-escape frequency ν, the activation energy E_{act} and the characteristic temperature T_0. These three parameters reflect the a-Si properties. The a-Si TFTs with a good Stage II stability should have a big $t_{0,II}$ and a big β_{II}. Two-stage 50% lifetime $\tau_{50\%}$ is the time when the drain current has dropped to 50% of its initial value predicted with the two-stage model combining Stage I and Stage II together, and it is the most comprehensive index to evaluate the stability of a-Si TFTs.

The initial threshold voltage, before gate bias stress applied to a-Si TFTs, is $V_{T0} = 0.83 \pm 0.45$ V. It is not obviously correlated with their TFT stability. In describing the process conditions and stability results, we refer to the numbered entries in Table 5-I.

Table 5-I. Deposition conditions and corresponding stability parameters

	Etch	Gate SiN_x		a-Si			Stage I		Stage II					Two-stage
No.	Wet / Dry	Hydrogen diluted?	[NH3] / $[SiH_4]$	Temp. (°C)	$[H_2]$ / $[SiH_4]$	Power density (mW/cm^2)	$\Delta V_{max,1}$ (V)	$t_{0,1}$ (s)	ν (kHz)	T_0 (K)	E_{act} (eV)	$t_{0,2}$ (in 10^6 s)	β_2	$\tau_{50\%}$ (in 10^4 s)
1	Dry	No	10	220	10	17	0.3	<<1	5	1165	0.60	4.5	0.25	3.2
2	Dry	No	15	220	10	17	0.1	<<1	50	1035	0.69	13.3	0.28	25.0
3	Dry	No	25	220	10	17	0.1	<<1	100	967	0.69	8.3	0.30	20.7
4	Dry	Yes	10	200	10	17	0.1	1.0	500	830	0.78	53.9	0.35	218.7
5	Dry	Yes	10	220	10	17	0.08	8.7	500	730	0.79	77.9	0.40	454.8
6	Wet	Yes	10	220	10	17	0.31	69.5	500	565	0.79	67.8	0.52	542.7
7	Dry	Yes	15	220	10	17	0.15	42.7	500	797	0.78	49.1	0.37	201.3
8	Dry	Yes	20	220	10	17	0.14	10.1	500	964	0.78	49.1	0.30	111.2
9	Wet	Yes	20	220	10	17	0.23	29.8	500	793	0.78	55.0	0.37	192.4
10	Dry	Yes	10	220	2	8.6	0.16	22.4	1000	781	0.82	124.6	0.38	517.7
11	Dry	Yes	10	220	5	8.6	0.12	55.0	1000	772	0.82	118.9	0.38	562.0
12	Dry	Yes	10	220	10	8.6	0.23	1224	1000	766	0.82	120.8	0.38	449.5
13	Dry	Yes	10	300	10	8.6	0.08	206	5000	685	0.88	215.2	0.43	1802.2
14	Dry	Yes	10	320	10	17	0.06	1.2	5000	709	0.88	312.1	0.41	2099.9
15	Dry	Yes	10	320	2	8.6	0.19	0.3	5000	698	0.90	521.9	0.42	3040.1
16	Dry	Yes	10	320	5	8.6	0.08	0.2	5000	643	0.90	524.0	0.46	4490.8
17	Dry	Yes	10	320	7.5	8.6	0.15	0.5	5000	831	0.90	666.9	0.35	2252.2
18	Dry	Yes	10	330	2	8.6	0.2	0.3	5000	744	0.90	215.2	0.43	1325.7

5.2.1 *SiN_x gate insulator deposition*

Except for the SiN_x gate insulator deposition conditions, samples #1, #2, #3, #5, #7 and #8 have the same fabrication conditions. We plotted the two-stage 50% lifetimes $\tau_{50\%}$ of these six samples in Fig. 5.1.

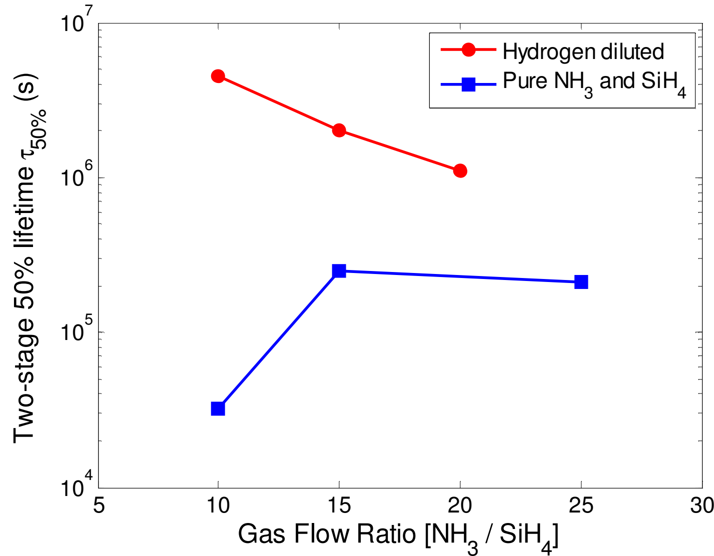

Fig. 5.1. Dependence of 50% lifetime from the two-stage model fit on the gate SiN_x deposition conditions.

– **Effect of hydrogen dilution**

In the gate SiN_x depositions for samples #5, #7 and #8, the H_2 to SiH_4 ratio is about 50. Fig. 5.1 shows that the two-stage 50% lifetime $\tau_{50\%}$ can be raised 10 to 100 times by this hydrogen dilution during nitride growth. Hydrogen dilution makes the SiN_x film more compact, and drives the film to be compressive [9]. The longer Stage I characteristic time $t_{0,I}$ for samples #5, #7 and #8 than for samples #1, #2 and #3 (Table 5-I), shows that hydrogen dilution during the gate SiN_x growth raises the stage I stability by improving SiN_x film itself. More important is that hydrogen dilution during SiN_x growth also greatly improves the stability in Stage II, where it decreases the characteristic temperature T_0 and increases the activation energy E_{act} (Table 5-I). These two parameters characterize the a-Si properties. This means hydrogen dilution improves the a-Si quality by influencing the growth of a-Si above the SiN_x.

– **Effect of ammonia to silane ratio**

The NH_3 to SiH_4 gas flow ratio [NH_3 / SiH_4] also affects the TFT stability. Fig. 5.1 shows that in the absence of the hydrogen dilution, the best [NH_3 / SiH_4] = 15. For the hydrogen-diluted samples, the best [NH_3 / SiH_4] = 10. Note that for no-hydrogen diluted and hydrogen-diluted cases, the samples with best [NH_3 / SiH_4] have both the best stage I stability (smallest $\Delta V_{Tmax,I}$) and the best stage II stability (longest $t_{0,II}$). A high but proper[NH_3 / SiH_4] flow ratio produces nitrogen-rich SiN_x , which has a low content of Si-H bonds and good electrical properties, including high resistivity, high breakdown voltage and low charge trapping rate [10]. The dependence of the stage II stability on the gate SiN_x deposition conditions shows that the gate SiN_x depositions conditions do not only affect the quality of the SiN_x but also affect the quality of the a-Si channel materials.

5.2.2 *a*-Si channel layer deposition

As shown above, when the a-Si deposition conditions are fixed, the best gate SiN_x is deposited using hydrogen dilution and [NH_3 / SiH_4] = 10. Given this SiN_x, we varied the a-Si deposition conditions. The resulting two-stage 50% lifetimes $\tau_{50\%}$ are shown in Fig. 5.2. The open squares represent samples #4, #5 and #14 with a-Si deposition power at 17mW/cm^2, and the solid dots represent samples #10 - #13 and #15 - #18 with a-Si deposition power at 8.6mW/cm^2.

– **Effect of a-Si deposition temperature**

Fig. 5.2 shows that by increasing the substrate temperature from 200°C (process #4) to 320°C (process #14) during a-Si deposition, with all other deposition conditions staying the same, the two-stage 50% lifetime $\tau_{50\%}$ can be raised 10 times for the samples deposited at 17mW/cm^2. For the samples deposited at 8.6mW/cm^2, the two-stage 50% lifetime $\tau_{50\%}$ can be raised about 8 times by increasing the a-Si deposition temperature from 220°C (process #10 - #12) to 320°C (process # 15 - #17). However, if the deposition temperature for the a-Si exceeds that for the gate SiN_x (process #18), the stability deteriorates. Thus, we find that the best a-Si deposition temperature is the same as the gate SiN_x deposition temperature.

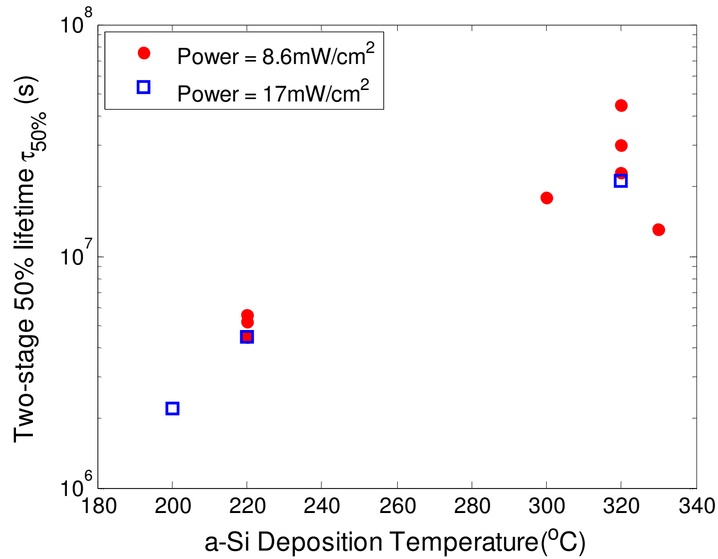

Fig. 5.2. Dependence of two-stage 50% lifetime on the a-Si deposition temperature and power using two-stage model.

– **Effect of hydrogen dilution**

The a-Si layers of samples #10, #11 and #12 are deposited at 220°C with three different H_2 to SiH_4 gas flow ratios [H_2 / SiH_4]. Samples #15, #16 and #17 are deposited at 320°C, also with three different [H_2 / SiH_4] ratios. The squares in Fig. 5.3 shows that for a-Si deposited at 220°C the effect of hydrogen dilution has no effect on the two-stage 50% lifetime $\tau_{50\%}$. At the a-Si deposition temperature of 320°C (solid dots in Fig. 5.3), the most stable a-Si TFTs are made with [H_2 / SiH_4] = 5 (process #16).

– **Effect of deposition power at both sides of the SiN_x / a-Si interface**

The deposition power for the a-Si and the gate SiN_x near the SiN_x / a-Si interface also affects the stability of the TFTs. In processes #4, #5 and #14, the gate SiN_x is deposited at 21.5 mW/cm^2 and the a-Si is deposited at 17 mW/cm^2. In processes #10 - #13 and #15 - #18, the a-Si and the gate SiN_x near the SiN_x / a-Si interface are deposited at 8.6 mW/cm^2. Because the growth of SiN_x at 8.6 mW/cm^2 is slow, the SiN_x more than 50nm away from the interface is still deposited at 21.5 mW/cm^2. Fig. 5.2 and Table 5-I suggest that the stability may be slightly improved through decreasing deposition power near the SiN_x / a-Si interface (process # 10 - #12 vs. process #5 at

220°C, and process #15 - #17 vs. process #14 at 320°C). The stability improvement is reflected in the rise of E_{act}. A lower plasma power leads to reduced number of weak bonds in the a-Si, because the plasma may damage the a-Si.

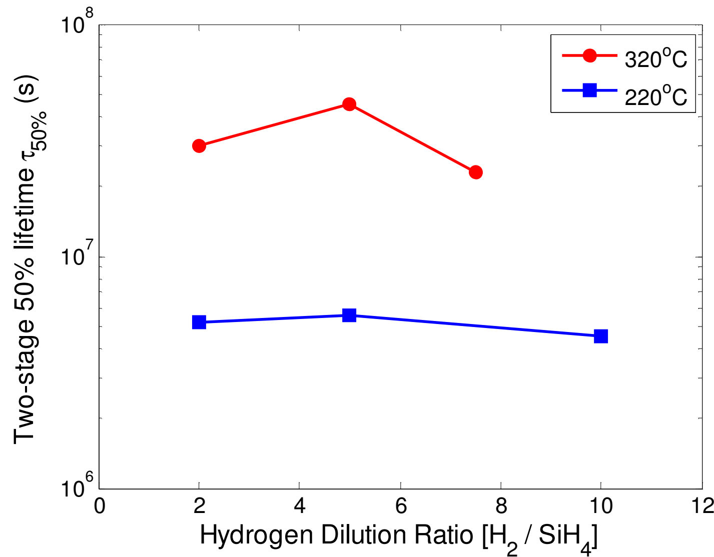

Fig. 5.3. Dependence of 50% lifetime on the hydrogen dilution during a-Si deposition using two-stage model (Squares: a-Si deposited at 220°C; Dots: a-Si deposited at 320°C).

5.2.3 *Discussion*

We observed that deposition conditions of the gate SiN_x and a-Si affects the stability of a-Si TFTs. Since the a-Si is deposited after the gate SiN_x for the bottom gate TFT structure, the quality and microstructure of the a-Si can be affected by that of the underlying SiN_x. The dependence of Stage II stability on the gate SiN_x deposition conditions indicates that the SiN_x quality affects the quality of a-Si in the channel region close to the SiN_x / a-Si interface where defect creation in a-Si occurs [11-13]. Hydrogen dilution and a proper [NH_3 / SiH_4] flow ratio for SiN_x growth can slow down both instability mechanisms in two stages – charge trapping in SiN_x and defect creation in a-Si. Thus, hydrogen dilution and a proper [NH_3 / SiH_4] ratio improve the quality of the SiN_x and the quality of a-Si near the a-Si / SiN_x interface as well. By optimizing the gate SiN_x deposition conditions, further stability improvement can be achieved by matching the a-Si properties to those of the gate SiN_x. The a-Si layer of the most stable a-Si TFTs in our

work was deposited at the same temperature as that of the gate SiN_x, at low deposition power near the interface and with hydrogen dilution during deposition.

5.3. *The stability of wet and dry-etched TFTs*

We also investigated the effects of dry or wet etching on the TFT stability under low gate-field stress. The fabrication processes of wet and dry-etched TFTs are described in Chapter 3. The wet-etched TFTs were fabricated with the same recipe as the dry-etched TFTs, except for the etching steps.

5.3.1 *DC characteristics comparison*

The DC transfer characteristics of dry-etched and wet-etched TFTs are similar and uniform across the 3-inch × 3-inch substrates. Fig. 5.4 shows typical transfer characteristics of dry and wet-etched a-Si TFTs with 150 μm channel width and 15 μm channel length. The dry-etched a-Si TFTs had initial threshold voltages V_{T0} = 0.71±0.28 V and field-effect mobilities μ_{FET0} = 1.14±0.04 cm^2/V·s. The wet-etched a-Si TFTs had V_{T0} = 0.80±0.15 V and μ_{FET0} = 1.08±0.03 cm^2/V·s.

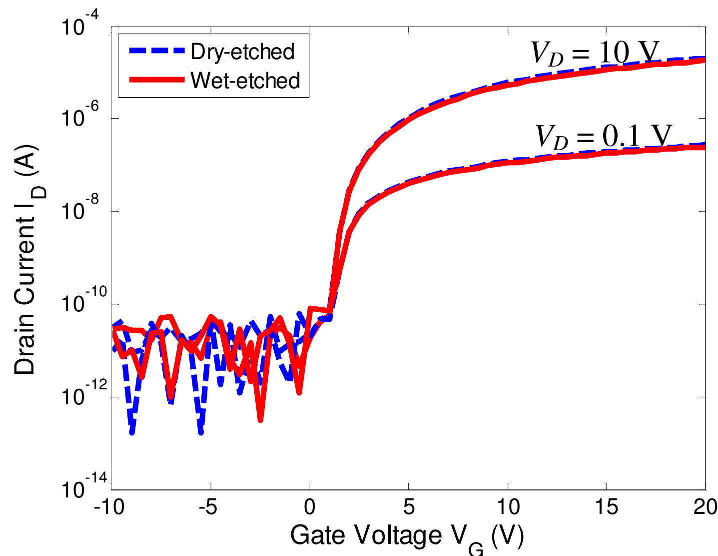

Fig. 5.4. Transfer characteristics of dry and wet-etched a-Si TFTs (samples #8 and #9 in Table 5-I).

5.3.2 *Comparison of dry and wet-etched a-Si TFTs*

Across the 3-inch × 3-inch substrates, we randomly picked three dry-etched and three wet-etched a-Si TFTs (samples #8 and #9 in Table 5-I). At 20°C, we stressed them in saturation with a constant gate-source voltage of 5V and a constant drain-source voltage of 7.5V for about 24 hours. $\Delta V_{T,total}(t)$ was extracted from measured drain current data vs. time. These are the squares in Fig. 5.5 for dry etching and Fig. 5.6 for wet etching. To study the stability in Stage II, we then stressed a-Si TFTs at temperatures from 40°C to 140°C in steps of 20°C, using one fresh wet-etched and one fresh dry-etched a-Si TFT at each bias-stressing temperature (Series A in Fig. 5.7). The Stage I parameters obtained for the three dry-etched and wet-etched a-Si TFT pairs are listed in Table 5-II and show that in Stage I wet-etched a-Si TFTs are more uniform than dry-etched TFTs. This point is also evident from Fig. 5.5 with its wide spread between the early threshold voltage shifts of dry-etched a-Si TFTs. Two-stage model fittings to the threshold voltage shifts of these dry-etched and wet-etched pairs are shown in Fig. 5.6. For clarity, we fit the data of only one TFT. 20°C two-stage 50% lifetimes are $\tau_{50\%} = 1.1 \times 10^6 \pm 31\%$ seconds for the dry-etched samples, and $\tau_{50\%} = 1.9 \times 10^6 \pm 1\%$ seconds for the wet-etched samples.

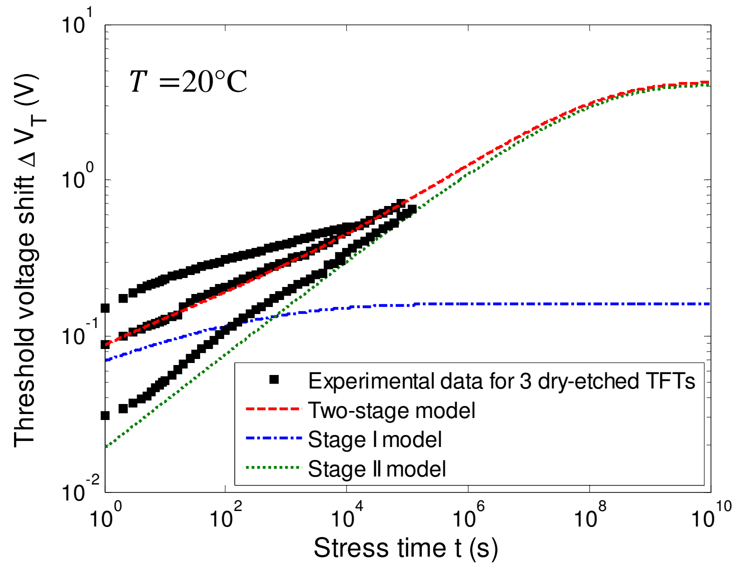

Fig. 5.5. Threshold voltage shift of three randomly picked dry-etched a-Si TFTs at 20°C and two-stage model fitting to the threshold voltage shift of one TFT.

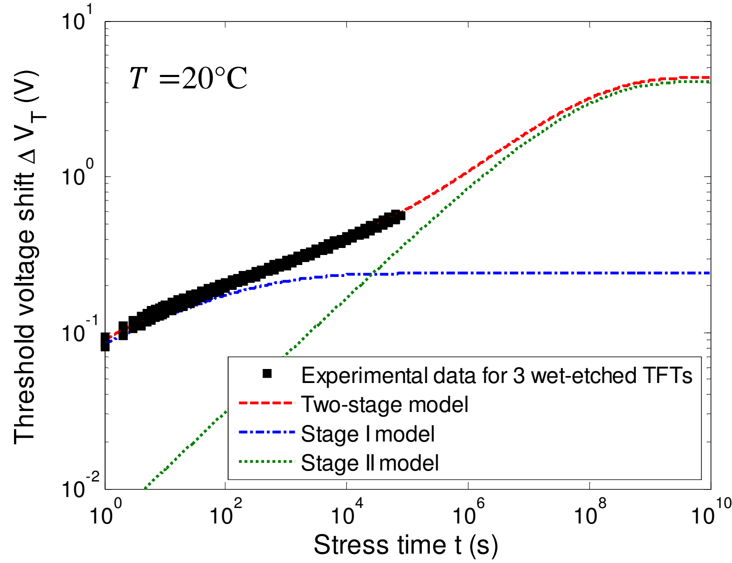

Fig. 5.6. Threshold voltage shift of three randomly picked wet-etched a-Si TFTs at 20°C and two-stage model fitting to the threshold voltage shift of one TFT.

Table 5-II. Stage I fitting parameters for dry and wet-etched a-Si TFTs

	Dry-etched a-Si TFTs			Wet-etched a-Si TFTs		
Sample	$\Delta V_{Tmax,I}$ (V)	$t_{0,I}$ (s)	β_I	$\Delta V_{Tmax,I}$ (V)	$t_{0,I}$ (s)	β_I
1	0	0	NA	0.24	35	0.24
2	0.16	28.8	0.18	0.23	15	0.25
3	0.25	1.4	0.36	0.23	39	0.24
Average	0.14±93%	10.1±160%	0.27±48 %	0.23±2.5%	30±43%	0.24±2.3%

We studied the stability of the dry-etched and wet-etched TFTs in Stage II by bias-stressing at elevated temperatures. The fitting parameters for Series A in Fig. 5.7 obtained from the Stage II model (5. 3) are listed in Table 5-III. The times when the drain current has dropped to its initial value (50% lifetimes $\tau_{50\%}$) are shown in the Arrhenius plot for Series A in Fig. 5.7. The squares are the experimentally measured 50% lifetimes at high temperatures, and the straight lines are 50% lifetime $\tau_{50\%,II}$ extracted from the Stage II model fits (5. 3), which enables us to extrapolate

from the elevated bias-stress temperatures to room temperature. It can be seen that the wet-etched a-Si TFTs have a better long-term stability. The Stage II model produces this result because the wet-etched a-Si TFTs have a lower T_0 than dry-etched a-Si TFTs, while the parameters ν and E_{act} are similar (see Table 5-III). A lower T_0 means that the energy distribution of weak Si-Si bonds in wet-etched a-Si TFTs is steeper than that in dry-etched TFTs. To confirm this conclusion about dry-etching and wet-etching effects on Stage II stability, we measured another series of dry and wet-etched a-Si TFTs (Series B in Fig. 5.7) fabricated under different deposition conditions (#5 and #6 in Table 5-I). Again, wet-etched a-Si TFTs have a better stability in Stage II.

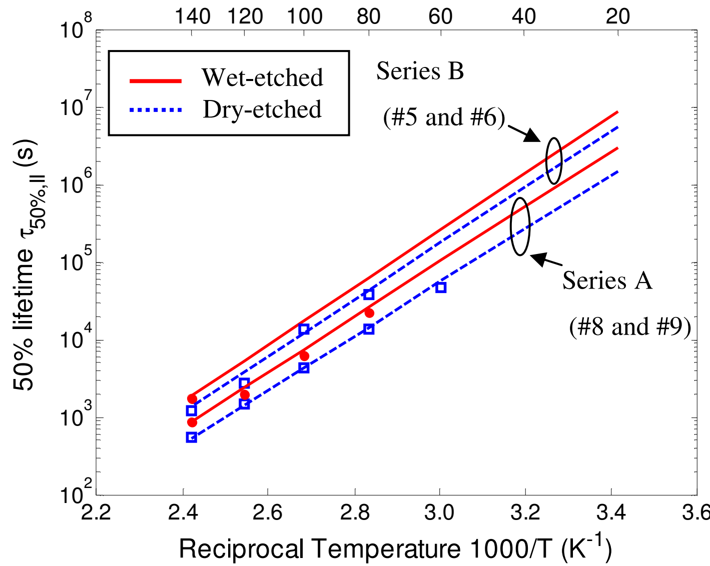

Fig. 5.7. Stage II 50% lifetime at different temperatures for two series of dry and wet-etched a-Si TFTs (solid squares: experimental data; straight lines: stage II model).

Table 5-III. Stage II fitting parameters for dry and wet-etched a-Si TFTs

	ν (Hz)	T_0 (K)	E_{act} (eV)
Dry-etched a-Si TFTs	5×10^5	964	0.78
Wet-etched a-Si TFTs	5×10^5	793	0.78

5.3.3 *Discussion*

Three sources in a reactive ion etching (RIE) that can cause damage TFTs [14]: ion bombardment, plasma radiation and surface charge buildup. Ion bombardment causes the surface damage. Because our a-Si TFTs have the back-channel passivated structure, surface damage from ion bombardment should not affect the channel region. In Fig. 5.5, we observed that dry-etching induced widely distributed threshold voltage shifts in Stage I. As discussed in Chapter 4, the instability in Stage I is most likely caused by the charge trapping in the gate SiN_x. Therefore, we attribute the non-uniform threshold voltage shifts of the dry-etched a-Si TFTs in Stage I to spatially non-uniform surface charge buildup during plasma etching, which can induce surface states at the SiN_x / a-Si interface and eventually trap charge in SiN_x [15]. The long-term instability of Stage II is caused by defect creation in a-Si. The deterioration of long-term stability in Stage II (Fig. 5.7) caused by RIE probably is the result of the high photon energy plasma radiation, which could cause the Staebler-Wronski type defects in the a-Si layer that are not fully reversible by thermal annealing [14, 16]. Comparing the stability between dry and wet-etched a-Si TFTs suggests that some damage caused by RIE remains after a one-hour long annealing at 180°C [8].

5.4. *Summary and conclusion*

Using results from low gate-field stress over a range of temperatures, and their fit to a two-stage model for threshold voltage shift, we evaluated the effect of a-Si TFT fabrication steps on the stability of the drain current. The main measure of stability is the time over which the drain current drops to 50% of its initial value. That time is either measured, or extrapolated from shorter-time measurements using the two-stage model. The stability of a-Si TFTs are determined by deposition conditions and etching methods, which are summarized in Table 5-I. The instability in Stage I leads to a maximum threshold voltage shift $\Delta V_{Tmax,1} \leq 0.3$ V. As a result, the two-stage 50% lifetime is mainly determined by Stage II. Instability in Stage II is caused by defect creation in a-Si and can be characterized by three parameters the attempt-to-escape frequency ν, activation energy E_{act} and characteristic temperature T_0 in (5. 4) and (5. 5). The statistical dependence of two-stage 50% lifetimes on these three parameters for a-Si TFTs in Table 5-I are illustrated in Fig. 5.8, Fig. 5.9 and Fig. 5.10. The a-Si TFTs with large ν, high E_{act} and low T_0 have better stability and long lifetime. As pointed out in Chapter 4, a-Si with high

E_{act} and low T_0 has high barrier energies for defect creation and small disorder in structure. Note that the attempt-to-escape frequency ν is the effective attempt-to-escape frequency [17], which measures combined effect of both defect creation and defect annealing. Thus, a-Si TFTs with large ν do not necessarily tend to be unstable. In contrast, as shown in Fig. 5.8, the most stable a-Si TFTs have a large ν.

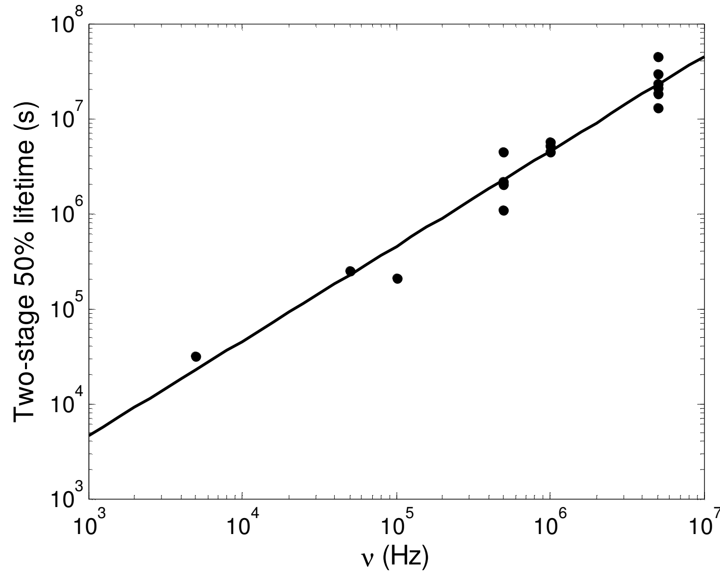

Fig. 5.8. Dependence of two-stage 50% lifetimes on the attempt-to-escape frequency ν.

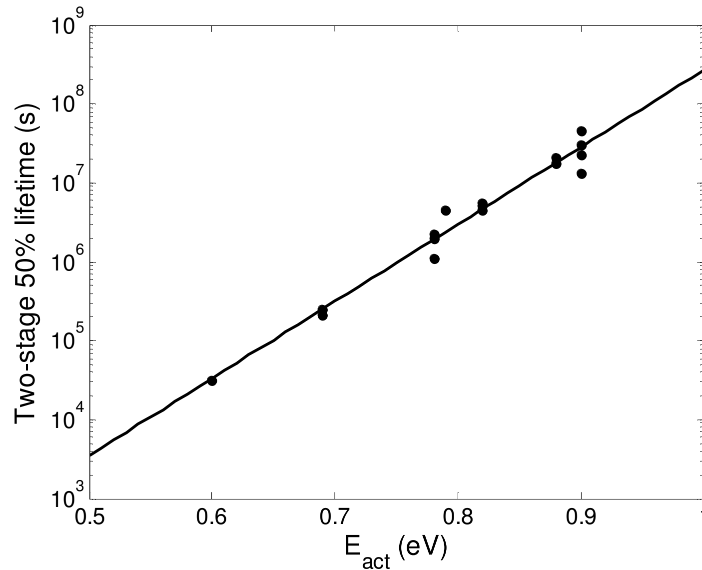

Fig. 5.9. Dependence of two-stage 50% lifetimes on the activation energy E_{act}.

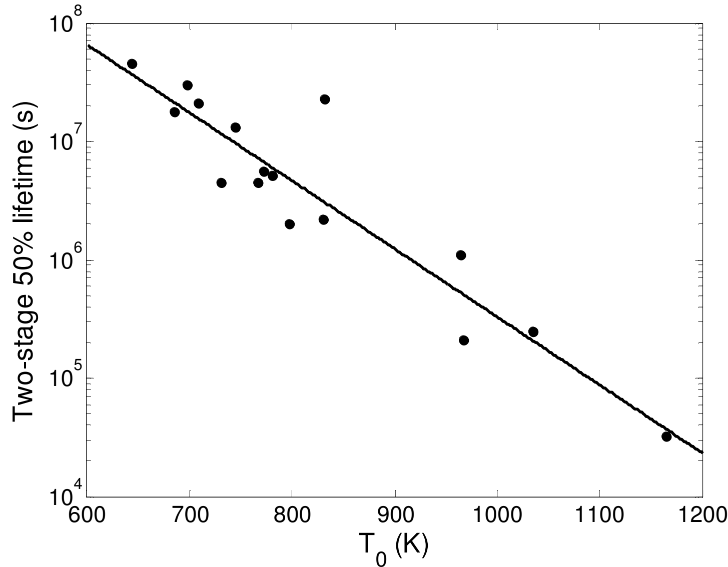

Fig. 5.10. Dependence of two-stage 50% lifetimes on the characteristic temperature T_0

Another important result is that reaching high stability requires the coupling of several parameters for processing the SiN_x gate insulator and the a-Si channel layer. The optimum NH_3 / SiH_4 gas flow ratio is 10, and hydrogen dilution makes the SiN_x more stable. The most stable a-Si is deposited at high temperature, but not exceeding the temperature of SiN_x deposition. An H_2 / SiH_4 flow ratio of 5 produces the most stable a-Si. One important result is that reaching high stability requires the coupling of several parameters for processing the SiN_x gate insulator and the a-Si channel layer. When the SiN_x gate dielectric is deposited with H_2 dilution, the a-Si deposited on top of it becomes more stable than when the gate SiN_x is deposited without H_2 dilution. We also find that the highest TFT stability is achieved when both the SiN_x and a-Si layers near the SiN_x /a-Si interface are grown at low plasma power. By combining these deposition techniques we raised the extrapolated 50% lifetime of the drain current under continuous operation from 3.3×10^4 sec (9.2 hours) to 4.4×10^7 sec (1.4 years). Etching is the most important post-deposition process that affects stability. We developed a TFT fabrication process with four wet etch steps, which produces TFTs that are more uniform in Stage I and more stable in Stage II than those processed with plasma etching.

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Redistribution of Gap State Density after Low Gate-Field Stress

In Chapter 4, two stages of the threshold voltage shift were identified and modeled with the two-stage model. The threshold voltage shifts in the two stages were both modeled with the stretched exponential expression. Stage I initially dominates up to hours or days near room temperature and is attributed to charge trapping in the gate SiN_x. Stage II dominates in the long term and is attributed to defect creation in a-Si. Although most reports suggest that defect creation is the dominant mechanism for the threshold voltage shift under low gate-field as assumed in Chapter 4 [1-6], a consensus has yet to be reached [7].

In this Chapter, the gap state density in a-Si is determined from the analysis of the field-effect characteristics [8, 9] in the a-Si TFT before and after low-gate field stress. Although this technique to measure the density of states (DOS) has limitations, such as in distinguishing between bulk and interface states [10], it provides adequate information to show that the gap state density is redistributed after a constant low gate field stress [11]. The redistribution of gap state density suggests that the low gate-field leads to increased mid gap states and decreased tail states. This provides evidence to show that defect creation occurs in a-Si TFTs under low-gate field.

6.1. *Theory of field-effect technique to determine gap state density*

We consider a metal/insulator/amorphous silicon (MIS) structure as illustrated in Fig. 6.1. With several assumptions and approximations in Section 6.1.1, the gap state density can be obtained from the surface potential, which can be determined from the field-induced conductance.

6.1.1 *Assumptions and approximations*

To develop the field-effect technique, assumptions and approximations are made to simplify the procedure to obtain the relationship between gap state density and field-effect conductance.

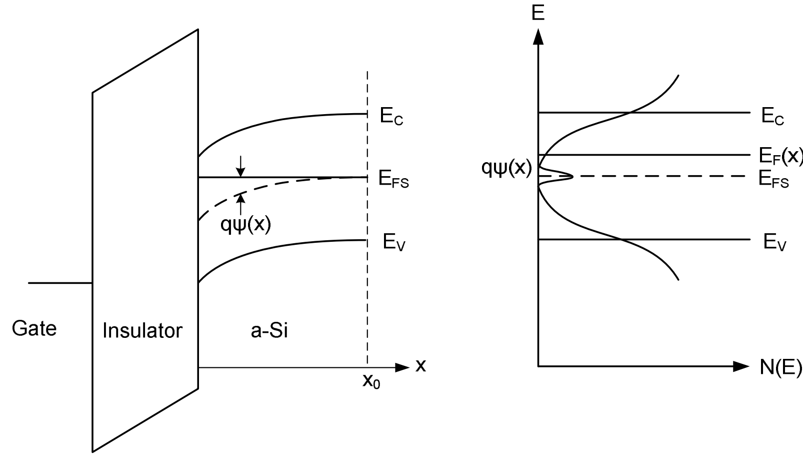

Fig. 6.1. Energy band diagram of the metal / insulator / amorphous silicon (MIS) structure with a positive gate bias and schematic density of states distribution.

– **Spatially uniform distribution of gap states [10]**

We assume that the distribution of gap states $N(E)$ is uniform in the a-Si from the surface region near the gate insulator into the a-Si bulk region. It is natural to make this assumption for fresh a-Si TFTs with uniformly deposited a-Si. However, for a-Si TFTs after low-field stress, $N(E)$ in the surface region is different from that in the bulk region, because the heavier free-carrier concentration in the surface region induces more defects there. The validity of this assumption will be discussed in Section 6.4.

– **Zero-temperature statistics [9, 10]**

For sufficiently low temperatures, it can be assumed that all induced charges are in localized states, thus neglecting the space charge of the free carriers.

– **Unmodulated bulk [10]**

For a-Si TFTs with a ~200 nm thick a-Si layer, it makes sense to assume that the bulk region far away from the a-Si / insulator interface is unmodulated, i.e.

$$\left.\frac{d\psi}{dx}\right|_{x=x_0} = 0 \qquad (6.\ 1)$$

where x_0 is the thickness of the a-Si layer, and $x = 0$ is the position at the a-Si / insulator interface (Fig. 6.1).

– **Negligible effect of the interface states [10]**

For our good quality a-Si TFTs with interface state density below 10^{11} $cm^{-2}eV^{-1}$, the effect of interface states can be neglected without leading to serious errors [12].

6.1.2 *Determination of gap state density*

We represent the field-effect technique as described in Ref. 14 and Ref. 15. The band bending in the a-Si layer, $\psi(x)$ (Fig. 6.1), follows Poisson's equation:

$$\frac{d^2\psi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_{si}} \quad (6.\ 2)$$

where ϵ_{si} is the a-Si dielectric constant and $\rho(x)$ is the local space-charge density at x due to the local Fermi-level shift of $q\psi(x)$. With the assumption of zero-temperature statistics, $\rho(x)$ is related to the gap state density distribution $N(E)$ by

$$\rho(x) = -q\int_{E_{FS}}^{E_{FS}+q\psi(x)} N(E)dE \quad (6.\ 3)$$

After multiplying by $2d\psi(x)/dx$ and integrating from the insulator / a-Si interface at $x = 0$ to the unmodulated neutral bulk at $x = x_0$, we obtain

$$\left[\frac{d\psi}{dx}\bigg|_{x=0}\right]^2 = \frac{2q}{\epsilon_{si}}\int_0^{\psi_s} d\psi_s \int_{E_{FS}}^{E_{FS}+q\psi} N(E)dE \quad (6.\ 4)$$

where ψ_s is the band bending at $x = 0$. Then, the gap state density is expressed by

$$N(E_{FS} + q\psi_s) = \frac{\epsilon_{si}}{2q}\frac{\partial^2}{\partial\psi_s{}^2}\left[\frac{d\psi}{dx}\bigg|_{x=0}\right]^2 \quad (6.\ 5)$$

Assuming negligible interface states, the electric field at the insulator / a-Si interface is given by

$$\frac{d\psi}{dx}\bigg|_{x=0} = -\frac{\epsilon_{ins}}{\epsilon_{si}}\frac{V_{ins}}{d_{ins}} = -\frac{\epsilon_{ins}}{\epsilon_{si}}\frac{V_G - V_{FB} - \psi_s}{d_{ins}} \quad (6.\ 6)$$

where ϵ_{ins} is the gate insulator dielectric constant and d_{ins} is the thickness of the insulator layer, V_{FB} is the flat band voltage, V_G is the gate voltage, and V_{ins} is the voltage drop across the

insulator. Combining (6. 5) and (6. 6), the density of the gap states can be calculated, if the relation between V_G and ψ_s is known.

6.1.3 *Relation between gate voltage and surface potential [9]*

The surface potential ψ_s can be determined from the measured field-induced conductance as a function of gate voltage. The sheet conductance σ is written as

$$\sigma = \sigma_{FB} + \sigma_{FB}\frac{1}{x_0}\int_0^{x_0}\{\exp[q\psi(x)/kT] - 1\}dx$$

$$= \sigma_{FB} - \sigma_{FB}\frac{1}{qx_0}\int_0^{q\psi(x=0)}\frac{\exp(q\psi/kT)-1}{d\psi/dx}d(q\psi) \quad (6.7)$$

where σ_{FB} refers to the conductance for the flat band condition, i.e. $\psi_s = 0$. The increment in the gate voltage δV_G causes a corresponding change in the surface potential $\delta\psi_s$. As a consequence, the sheet conductance modulation $\delta\sigma$ is given by

$$\delta\sigma = -\sigma_{FB}\frac{1}{qx_0}\frac{\exp(q\psi_s/kT)-1}{d\psi/dx|_{x=0}}\delta(q\psi_s) \quad (6.8)$$

From this and (6. 6), we have

$$\delta\psi_s = \frac{\delta\sigma}{\sigma_{FB}}\frac{\epsilon_{ins}}{\epsilon_{si}}\frac{x_0}{d_{ins}}\frac{V_G - V_{FB} - \psi_s}{[\exp(q\psi_s/kT)-1]} \quad (6.9)$$

Starting from $V_G = V_{FB}$, the surface potential ψ_s as a function of gate voltage V_G can be successively obtained using (6. 9).

6.1.4 *Sheet conductance calculation*

Because the a-Si active layer is intrinsic and a high field exists everywhere in the a-Si TFT, the current is a drift current in both the subthreshold region and above threshold region [13]. Thus, the field-induced sheet conductance σ is the inverse of sheet resistance and can be calculated from the TFT transfer characteristics of drain current I_D vs. gate voltage V_G for very low drain bias with

$$\sigma(V_G) = \frac{1}{R_s} = \frac{1}{V_D/I_D(V_G)\cdot W/L} = \frac{I_D(V_G)L}{V_D W} \quad (6.10)$$

Thus, sheet conductance as a function of gate voltage V_G can be obtained.

Substituting (6. 10) into (6. 9) enables us to obtain the relation between the surface potential ψ_s and the gate voltage V_G. Then with (6. 5) and (6. 6), the gap state density can be determined.

6.2. *Sample preparation and measurement*

The sample was fabricated with the dry-etching process described in Chapter 3. 300-nm gate nitride, 200-nm intrinsic hydrogenated a-Si and 300-nm passivation nitride were deposited sequentially at 320°C, 220°C and 220°C, respectively. At the end of the process, the sample was annealed at 180°C for an hour. After annealing, a gate-bias voltage sweep at a fixed drain voltage 0.1 V was applied to measure the I_D - V_G transfer characteristics of a fresh a-Si TFT at room temperature. Then the a-Si TFT was biased with a constant gate voltage $V_G = 5$ V (a low-gate field of ~1.5×10^5 V/cm) at 120°C for 5 minutes. The high temperature stress at 120°C was used to accelerate the threshold voltage shift under low-gate field stress. The drain voltage was set at zero, so the threshold voltage shift along the channel was uniform. After the 5-miniute bias-temperature stress, another gate-bias voltage sweep at a fixed drain voltage 0.1 V was applied to measure the I_D - V_G transfer characteristics at room temperature. During the two I_D - V_G sweeps, a small drain voltage $V_D = 0.1$ V (<<$V_G = 5$ V to make the channel generally uniform) was applied to obtain the field-effect conductance.

6.3. *Experiment results and gap state density determination*

The a-Si TFT we measured has a channel width of $W = 150$ μm and a channel length of $L = 15$ μm. I_D - V_G transfer characteristics before and after the low-gate field stress are shown in Fig. 6.2. Before stress, the threshold voltage was $V_{T0} = 1.54$ V, the field-effect mobility was $\mu_{FET0} =$ 0.83 cm^2/V·s, and the subthreshold slope was $SS_0 = 235$ mV/dec. After stress, the threshold voltage was $V_T = 2.38$ V, the field-effect mobility was $\mu_{FET} = 0.83$ cm^2/V·s, and the subthreshold slope was $SS = 240$ mV/dec. After the gate-bias stress at 120°C, the threshold voltage shifts, the subthreshold slope slightly increases (Fig. 6.2(a)) and the field-effect mobility stays almost unchanged (Fig. 6.2(b)).