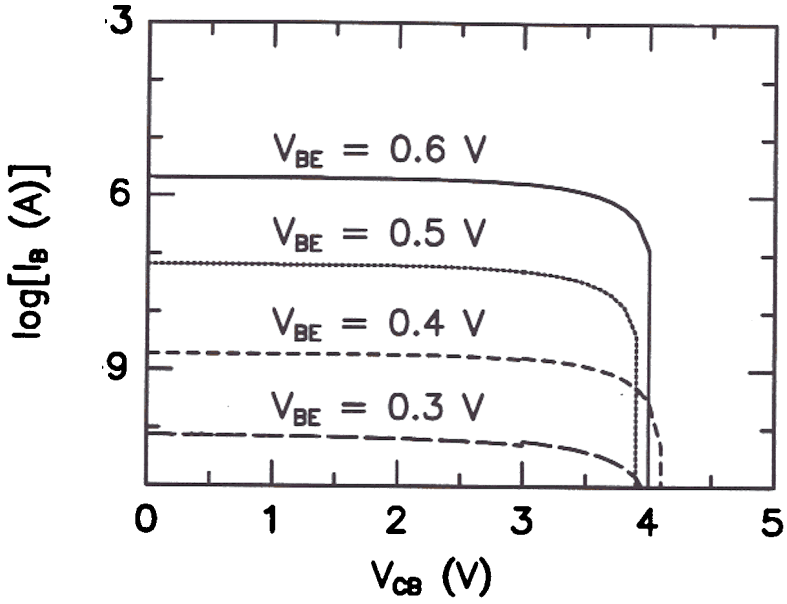


Figure 6.14: Measured base current of device #636 at room temperature for a constant base-emitter bias V_{BE}. At $V_{CB} > 3.8$ V, the base current component due to holes generated by avalanche multiplication in the base-collector junction dominated and caused the current gain to increase to ∞ ("bipolar snapback").

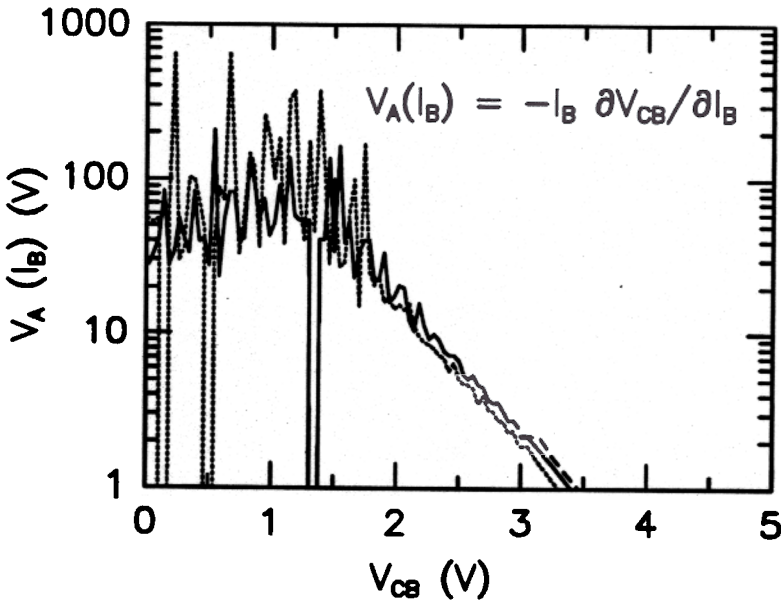


Figure 6.15: Contribution of the relative change in the *base* current to the Early voltage measured in the common-emitter configuration. Note the onset of weak avalanche multiplication at values of V_{CB} as low as 1.6 V.

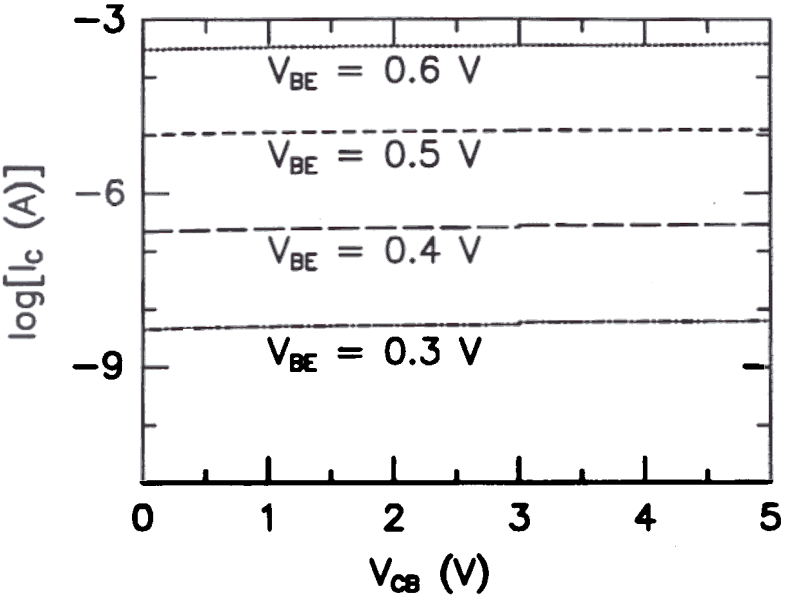


Figure 6.16: Measured collector current of device #636 at room temperature for a constant base-emitter bias V_{BE}. The increase in the collector current with reverse bias V_{CB} was due to the Early effect.

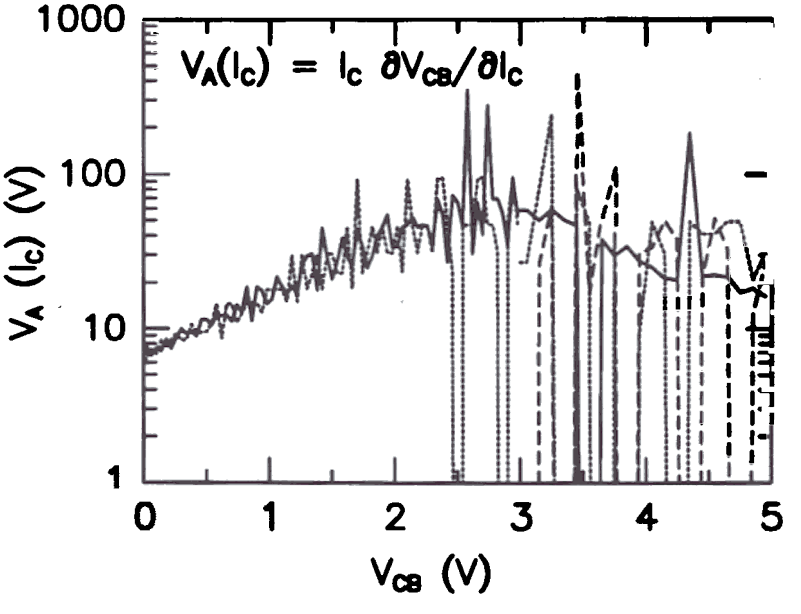


Figure 6.17: Contribution of the relative change in the *collector* current to the Early voltage measured in the common-emitter configuration. Note the degradation of $V_A(I_C)$ at values of V_{CB} below 2.5 V, caused by small amounts of dopant outdiffusion and the resulting parasitic barriers at the base-collector junction.

Chapter 7

The Double-Base Heterojunction Bipolar Transistor

7.1 Introduction

In Chapters 4 and 6 it was shown how epitaxy can be used to shape the potential barrier seen by electrons in a heterojunction bipolar transistor, thereby affecting the electrical properties of the device. Using epitaxy to incorporate the $Si/Si_{1-x}Ge_x$ heterojunction into silicon technology also allows one to employ "bandgap engineering" to increase the functionality of bipolar devices. Ideally, a circuit function can then be performed with fewer devices reducing the power consumption of the chip.

Examples of devices with increased functionality are charge-coupled devices and resonant-tunneling transistors [126]. Here we describe a Double-Base Heterojunction Transistor jointly developed with Xiaodong Xiao. First the principle of operation is explained. Then the layer growth and device processing are outlined, followed by electrical measurements. Finally, simple models for collector and base currents are presented.

7.2 Principle of Operation of Double-Base-HBT

Consider the band diagrams of Fig. 7.1. In a flat-base $Si/Si_{1-x}Ge_x/Si$ HBT (solid

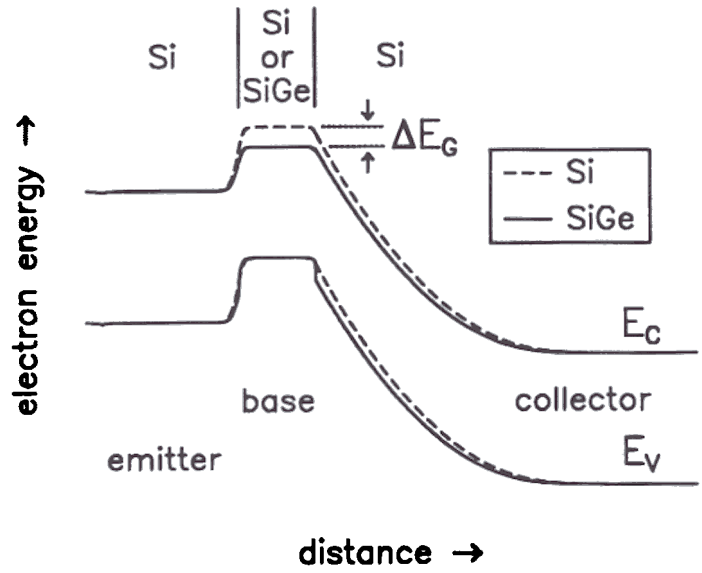


Figure 7.1: Band diagram of Si homojunction transistor (dashed line) and flat-base $Si/Si_{1-x}Ge_x/Si$ HBT (solid line). Plotted is electron energy vs. vertical distance perpendicular to the epitaxially grown layers. Note that the barrier seen by electrons in the $Si/Si_{1-x}Ge_x/Si$ HBT is lowered by the constant energy gap difference ΔE_G between the $Si_{1-x}Ge_x$ alloy and silicon.

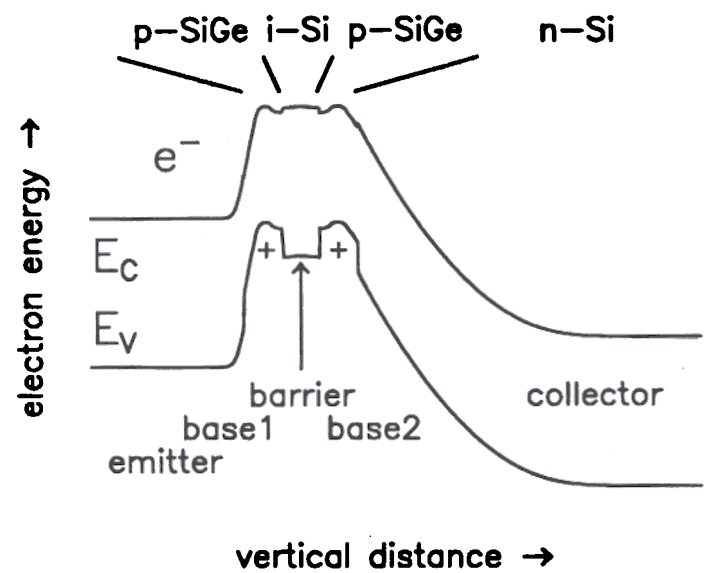


Figure 7.2: Band Diagram of Double-Base Heterojunction Bipolar Transistor, obtained by inserting an intrinsic silicon layer into the p-$Si_{1-x}Ge_x$ base of a flat-base HBT. Note that the conduction band in the base is still approximately flat because $\Delta E_C \ll \Delta E_V$ at the $Si/Si_{1-x}Ge_x$ heterojunction.

lines) the energy gap difference ΔE_G in the base compared to a homojunction device is constant. If an intrinsic silicon layer is inserted into the $Si_{1-x}Ge_x$ base, the band diagram of Fig. 7.2 is obtained. The hole quasi-Fermi level Φ_p is constant in the p-$Si_{1-x}Ge_x$ layers. There is essentially no band bending in the silicon layer because it is undoped. Since the band lineup at the $Si/Si_{1-x}Ge_x$ heterojunction is such that $\Delta E_C \ll \Delta E_V$ and the Si layer is fully depleted, the conduction band in the base is approximately constant if both $Si_{1-x}Ge_x$ layers are at the same potential, like that in a flat base $Si/Si_{1-x}Ge_x/Si$ HBT. The intrinsic silicon layer in the base, however, causes a barrier for holes of height $E_V(Si) - E_V(SiGe)$ in the valence band between the two p-$Si_{1-x}Ge_x$ layers at the emitter and the collector side of the base. This valence band potential barrier can isolate the two $Si_{1-x}Ge_x$ layers in the base from each other. If separate contacts are made to these two $Si_{1-x}Ge_x$ layers, they will be electrically independent of each other. The resulting device, which we call Double-Base Heterojunction Bipolar Transistor (DB-HBT), has four terminals; emitter, base 1, base 2, and collector.

The modes of operation of this DB-HBT are illustrated in Fig. 7.3. The basic principle is that the shape of the barrier seen by electrons in the *conduction band* is determined by the voltages applied to both of the base contacts, as opposed to a single base in a normal bipolar transistor. We assume for the moment that the base 2-collector junction is always reverse biased resulting in negligible electron injection into the base from the collector side. If both bases are shorted to the emitter, no electrons are injected into the base from the emitter, resulting in no collector current (Fig. 7.3 (a)). If only one of the bases is forward biased with respect to the emitter, the base which is not forward biased still presents a barrier for electrons in the conduction band, and no collector current flows (Fig. 7.3 (b, c)). Only if *both* bases are forward biased with respect to the emitter vanishes the barrier for electron flow in the conduction band, resulting in collector current (Fig. 7.3 (d)). In series with a load

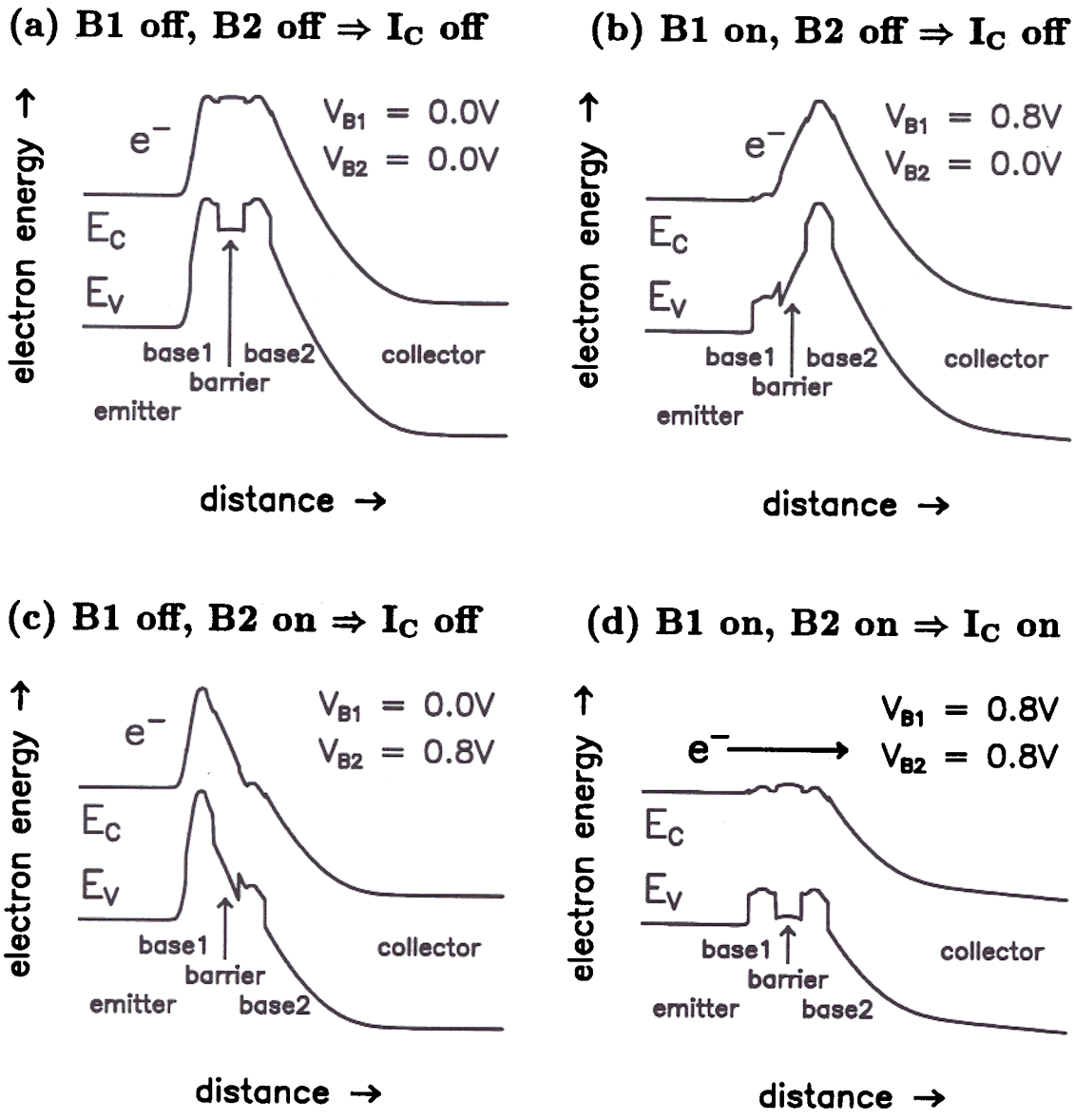


Figure 7.3: Band diagrams showing modes of operation of DB-HBT ("two-input switch"). Only if *both* base inputs are forward biased with respect to the emitter are electrons injected into the *p*-base region. They can then diffuse to the collector side of the base like in a normal bipolar transistor resulting in collector current.

Table 7.1: Device structures for DB-HBT's grown by RTCVD

device	1075	1076	1077	1078
nominal Ge concentration (%)	20	25	25	38
GeH_4 flow (sccm)	105	300	300	450
nominal p-$Si_{1-x}Ge_x$ thickness (Å)	160	30	60	40
nominal i-$Si_{1-x}Ge_x$ thickness (Å)	50	60	45	30
barrier thickness W_{Si} from C-V (Å)	299	427	288	310
E_A from T-dependent I_C (meV)	158	215	215	239
$E_V(Si) - \Phi_p(SiGe)$ from T-dependent $I_{B1,B2}$ (meV)	178	215	275	255

resistor this device can therefore be used in a single-transistor NAND gate, as will be demonstrated below. This increases the functionality of the DB-HBT compared to a $Si/Si_{1-x}Ge_x/Si$ HBT.

Growth of Epitaxial Layers and Device Processing

The layer sequence grown by RTCVD is shown in Fig. 7.4. First the collector layers were grown at 1000°C without intentional doping on a n^+ buffer layer as described in Chap. 3. Then the temperature was lowered to grow the base layers, first the second p-doped $Si_{1-x}Ge_x$ base with intrinsic $Si_{1-x}Ge_x$ spacers on both sides, then the nominally 200 Å thick intrinsic Si barrier, and finally the first p-$Si_{1-x}Ge_x$ base, again with i-$Si_{1-x}Ge_x$ spacers. The i-$Si_{1-x}Ge_x$ spacers were inserted to prevent the base dopant from diffusing into the i-Si barrier. In the four wafers grown, the germanium concentration in the two bases and the i-$Si_{1-x}Ge_x$ spacer thicknesses were varied as shown in Table 7.1. The emitter was grown at 700°C using silane because of its higher growth rate compared to $SiCl_2H_2$ to minimize the thermal budget experienced by the

Si	n^+-emitter	10^{19} cm^{-3}	1000 Å	700°C
Si	n-spacer	10^{17} cm^{-3}	200 Å	700°C
$Si_{1-x}Ge_x$	i-spacer	undoped	30–60 Å	625°C
$Si_{1-x}Ge_x$	p-base 1	10^{19} cm^{-3}	30–160 Å	625°C
$Si_{1-x}Ge_x$	i-spacer	undoped	30–60 Å	625°C
Si	i-barrier	undoped	200 Å	700°C
$Si_{1-x}Ge_x$	i-spacer	undoped	30–60 Å	625°C
$Si_{1-x}Ge_x$	p-base 2	10^{19} cm^{-3}	30–160 Å	625°C
$Si_{1-x}Ge_x$	i-spacer	undoped	30–60 Å	625°C
Si	n-collector	10^{17} cm^{-3}	3000 Å	1000°C
Si	n^+ -buffer	10^{19} cm^{-3}	1 μm	1000°C
<100> silicon substrate				

Figure 7.4: Layer sequence of Double-Base HBT. The base of a Si/$Si_{1-x}Ge_x$/Si HBT is replaced by a p-$Si_{1-x}Ge_x$/i-Si/p-$Si_{1-x}Ge_x$ sequence which results in a valence band barrier formed in the i-Si layer.

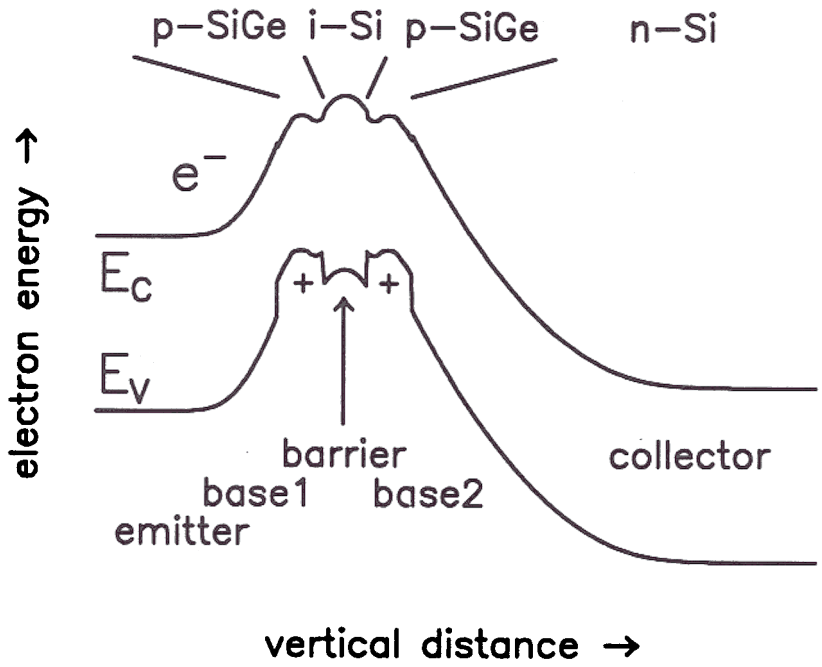


Figure 7.5: Calculated band diagram for DB-HBT in which boron from the two bases diffused into the i-Si barrier. Dopant diffusion reduces the collector current (higher conduction band barrier for electrons) and increases the base-to-base leakage current (tunneling through triangular part of valence band barrier in base).

base layers [127].

The band diagram of Fig. 7.5 suggests that even small amounts of boron diffusion from the two bases into the intrinsic silicon barrier will severely degrade device performance. The parasitic barrier in the conduction band reduces the collector current as discussed in Chap. 5. In the valence band, the trapezoidal barrier seen in an intrinsic silicon layer is replaced by two triangular barriers whose height is effectively reduced by tunneling of holes (Fowler-Nordheim tunneling through the triangular barriers) leading to reduced isolation between the two bases.

Table 7.1 shows that the $Si_{1-x}Ge_x$ layers were thicker than the equilibrium critical thickness. On wafers #1076 and #1078 misfit dislocations could be observed by phase contrast (Nomarski) microscopy, because they caused increased chemical

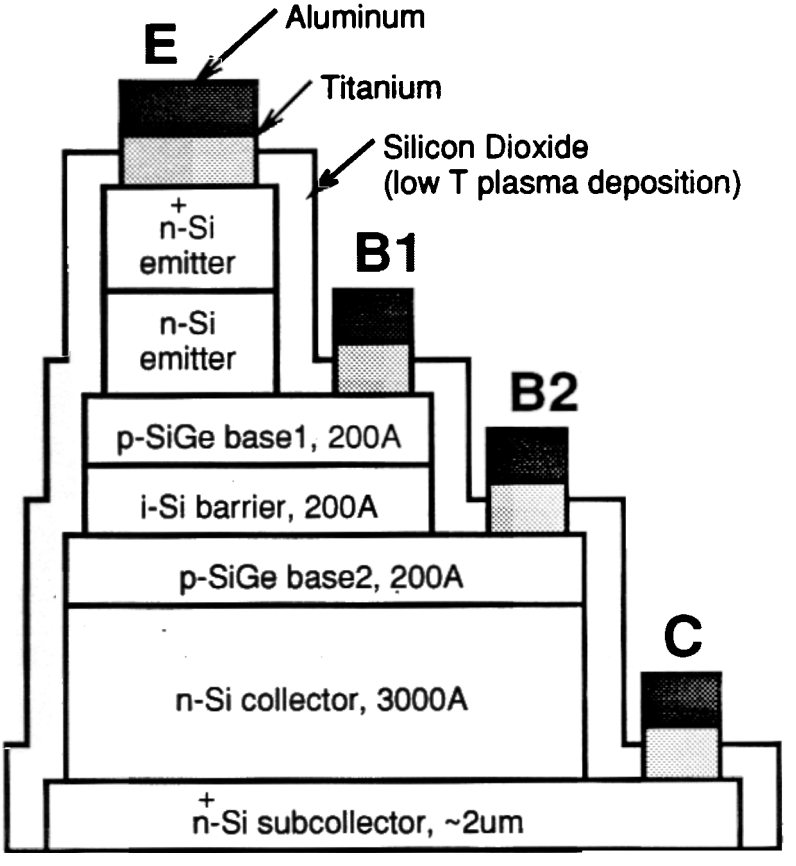


Figure 7.6: Triple mesa device structure of DB-HBT

etching during device processing.

From these layers devices were then fabricated in a triple-mesa process with low thermal budget similar to the one employed by Narozny *et al.* (see Fig. 7.6) [65]. First low-temperature silicon dioxide (p-SiO_2) was deposited with plasma-deposition and patterned with the emitter mesa mask. Then the silicon emitter was etched in a room-temperature solution of 150 g KOH, 6 g $K_2Cr_2O_7$, 150 ml n-propanol, and 600 ml deionized water, which was vigorously agitated because n-propanol is insoluble in the remaining solution. This solution etches silicon at about 75 Å/min, while the etch rate for strained $Si_{1-x}Ge_x$ is much smaller (it also removes AZ-1350J positive

photoresist). The p-SiO_2 mask was then removed in 1:6 HF:NH_4F (BOE), followed by the base 1 mesa photolithography. The $Si_{1-x}Ge_x$ base layer was next etched in a solution of 200 ml HNO_3, 100 ml H_2O, and 25 ml 1:100 HF:H_2O which etches the $Si_{1-x}Ge_x$ alloy with a high selectivity compared to silicon at an etch rate of about 200 Å/min [128]. Next, new oxide was deposited and patterned with the base 1-mesa mask, and the base 2 $Si_{1-x}Ge_x$ etched as described for base 1. Finally, the base 2 mesa was plasma-etched down to the n^+-buffer layer. The oxide was then removed, and new oxide deposited over the whole structure, followed by the metallization process described in Chap. 3 (5000 Å Ti; 5000 Å Al; 400°C anneal in forming gas for 20 min).

The yield on all four wafers was fairly low, because in most devices the two base layers where internally shorted to each other, even at low temperature. This is thought to be due to defect-enhanced diffusion during the metallization step, especially the forming gas anneal, and could be alleviated by (a) growing the $Si_{1-x}Ge_x$ films below the critical thickness to prevent dislocation formation, and (b) reducing the thermal budget of the metallization process (both e-beam evaporation and anneal). The device on wafer #1077 whose electrical characteristics are presented in Section 7.4 had an emitter area of about $70 \times 70\ \mu m^2$ and a base-1 area of about $215 \times 215\ \mu m^2$. The smallest working devices had an emitter area of $30 \times 30\ \mu m^2$.

Electrical Measurements on Double-Base-HBT's

The devices were then evaluated with temperature-dependent current-voltage and capacitance-voltage measurements. Working devices were obtained on all four wafers. We now present measurements taken on wafer #1077. Corresponding measurements on the other wafers yielded similar results.

Fig. 7.7 shows a typical room-temperature Gummel plot. With both bases externally shorted together, the devices worked like $Si/Si_{1-x}Ge_x/Si$ HBT's. The base

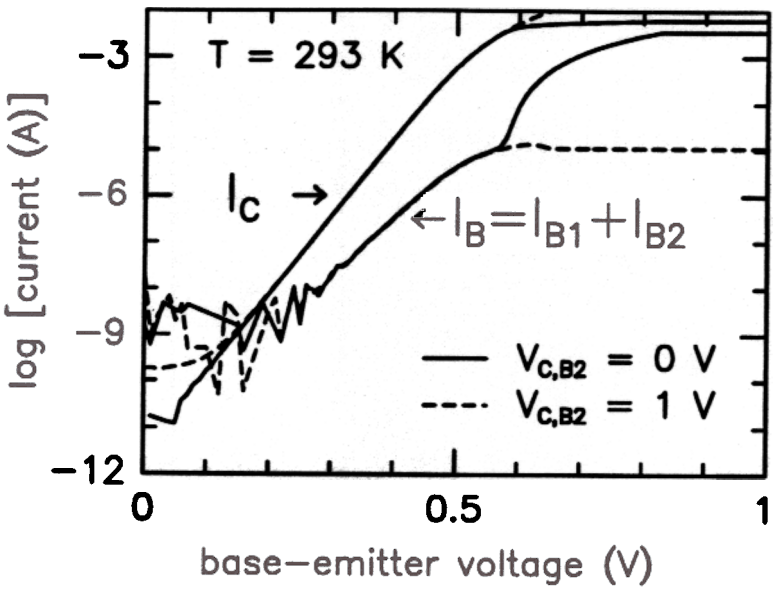


Figure 7.7: Room temperature Gummel plot showing normal transistor operation of DB-HBT #1077 at room temperature, with both bases externally shorted together.

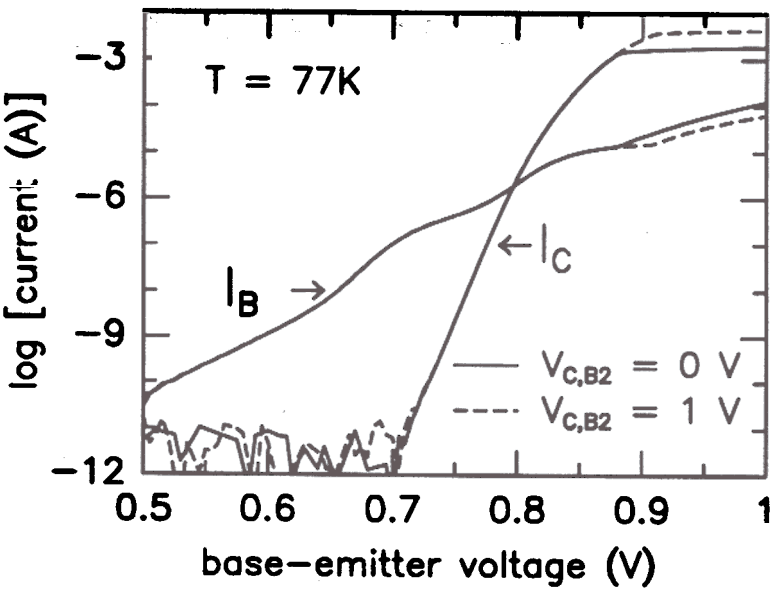


Figure 7.8: Gummel plot of DB-HBT #1077 at a temperature of 77 K with both bases externally shorted together. The base current was non-ideal because of a recombination current component originating from the mesa periphery.

currents were non-ideal with ideality factors of $n \approx 1.3$ because the base-emitter junctions were mesa-isolated, resulting in recombination current from the periphery of the devices due to surface states. This has also been observed by other groups using a similar process for fabricating conventional $Si/Si_{1-x}Ge_x/Si$ HBT's [72]. The collector currents were ideal with slopes of 60 mV/decade. At zero base-collector reverse bias the parasitic collector resistance forced the transistor into saturation, limiting the collector current to less than 10 mA (solid lines in Fig. 7.7). Saturation could be prevented by applying a reverse-bias $V_{C,B2}$ (dashed lines in Fig. 7.7).

At reduced temperature the devices still worked like $Si/Si_{1-x}Ge_x/Si$ HBT's, with ideal collector and non-ideal base currents. At 77 K the maximum current gain with both bases externally shorted together was above 100, as shown in Fig. 7.8.

The key point for the operation of the DB-HBT is the p-$Si_{1-x}Ge_x$/i-Si/p-$Si_{1-x}Ge_x$ barrier in the valence band. Fig. 7.9 shows its room and low temperature current-voltage characteristics. If a bias is applied between the two p-$Si_{1-x}Ge_x$ layers, holes are injected by thermionic emission over the valence band discontinuity at the $Si/Si_{1-x}Ge_x$ heterojunction. The magnitude of this current precluded independent base operation of the DB-HBT at room temperature. At 77 K, however, thermionic emission was sufficiently suppressed to provide isolation between the two base layers, and the two bases were independent with leakage currents below 5 μA for relative base voltages of less than 0.5 V in a device with a base mesa area of 184×184 μm^2.

That the two bases were independent at a temperature of 85 K is shown in Fig. 7.10. Emitter, base 1, and collector terminal were connected like in a bipolar transistor common-emitter $I_C(V_{CE};\ I_B = const.)$ measurement, i.e. the collector current I_C was measured as a function of V_{CE} with constant current into base 1. The voltage at base 2 was first set to 1 V, resulting in a current gain I_C/I_{B1} of about 100 (see Fig. 7.10 (a)). If the voltage at base 2 was lowered to 0.8 V, the current gain dropped to zero (see Fig. 7.10 (b)).

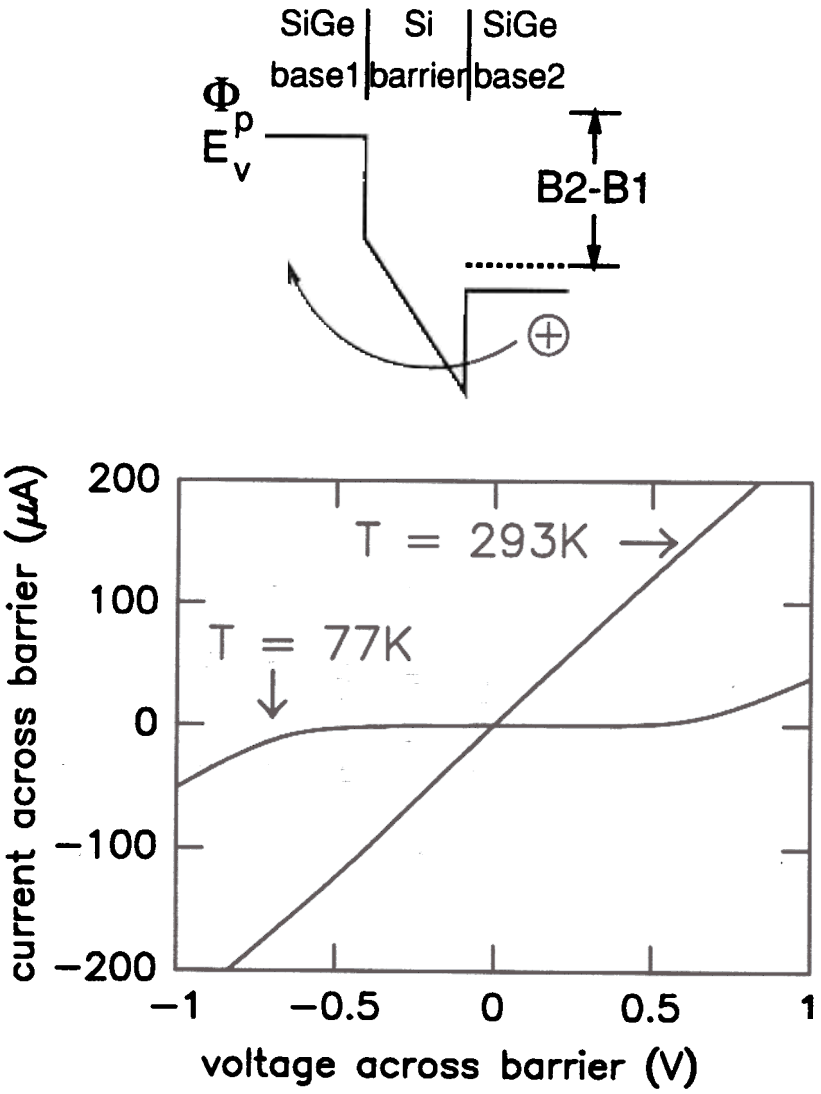


Figure 7.9: Current-voltage characteristics of the p-$Si_{1-x}Ge_x$/i-Si/p-$Si_{1-x}Ge_x$ barrier of device #1077 at room temperature and at 77 K. At 77 K thermionic emission was effectively suppressed, and the barrier blocked holes for $-0.5\text{V} \leq V \leq 0.5\text{V}$.

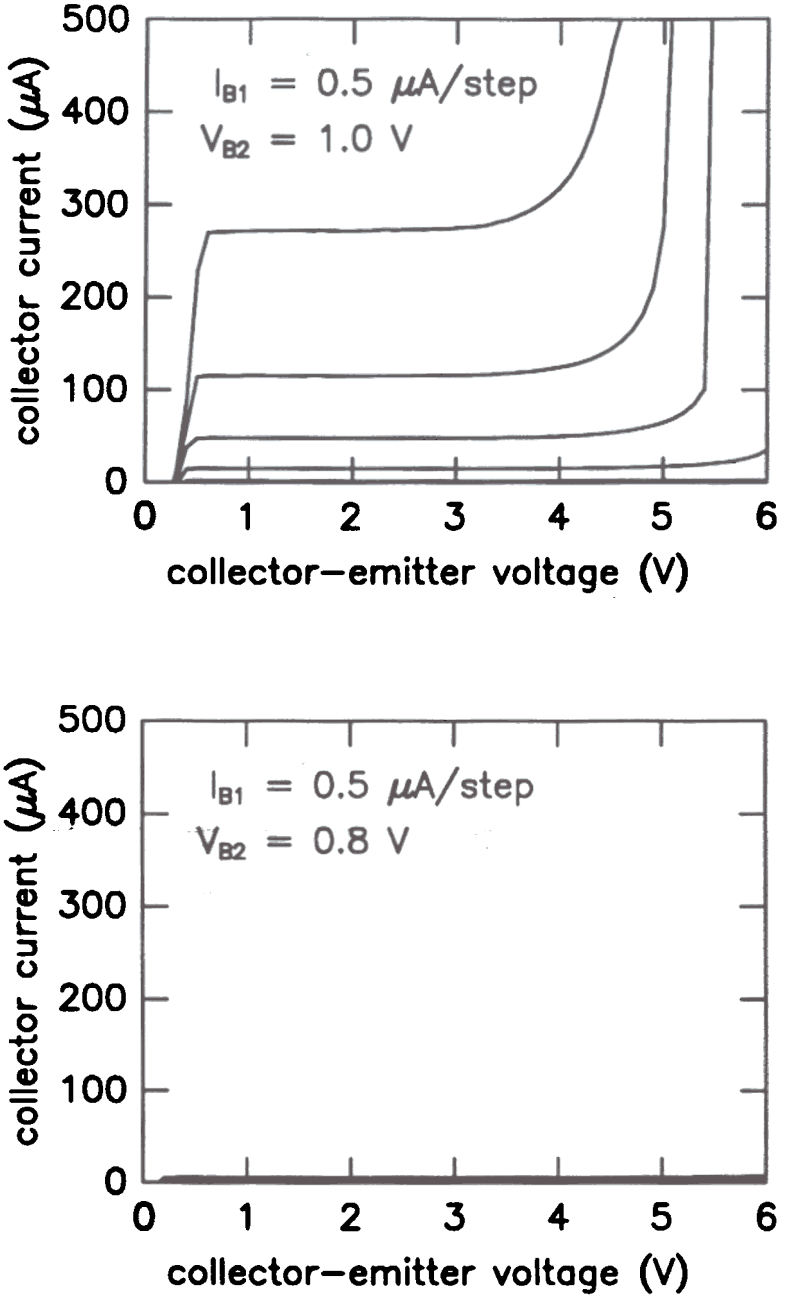


Figure 7.10: Collector current characteristics of DB-HBT at 85 K for a V_{B2} of (a) 1.0 V, and (b) 0.8 V. The current gain I_C/I_{B1} corresponding to the first base could be controlled by the voltage on the second base.

Since the voltages applied at *both* bases shaped the conduction band the collector current consisting of electrons injected from the emitter could be controlled independently with either base contact as shown in the three-dimensional Gummel plot of Fig. 7.11, taken at 77 K. Only if *both* bases were forward-biased with respect to the emitter was the collector current turned on. It increased with an inverse slope of less than 17 mV/decade, close to the ideal value of 15.3 mV/decade at 77 K. This confirmed the basic operating principle of the device, which has here been demonstrated for the first time

The collector current observed in all working devices can be modeled using charge-control theory. Since it is determined by the shape of the conduction band barrier seen by the electrons which depends on both base input voltages, it should be accurately described by Eqn. 4.12, which can be simplified because the highest barrier seen by the electrons is in a charge-neutral p-layer connected to one of the base terminals:

$$I_C(V_{B1}, V_{B2}) = \frac{qA_E}{\int_{base1} \frac{N_A(x)}{n_i^2(x)D_n(x)}dx \; e^{-qV_{B1,B}/k_BT} + \int_{base2} \frac{N_A(x)}{n_i^2(x)D_n(x)}dx \; e^{-qV_{B2,B}/k_BT}} \tag{7.1}$$

This equation expresses that the collector current is limited by the highest barrier in the conduction band, as outlined in Fig. 7.3

The currents into bases 1 and 2 are shown in Figs. 7.12 and 7.13. There can be two components of I_{B1}: due to holes injected into the emitter (or the base-emitter space charge region), whose number will depend only on $[V_{B1} - V_E]$; and due to holes moving over the barrier to or from base 2, whose number will depend on $[V_{B1} - V_{B2}]$. The current into base 1 was not symmetric with respect to the difference of the base inputs. It depended strongly on the voltage applied at base 1 suggesting that it was due to holes injected from base 1 into the base-emitter depletion region, or into the neutral emitter for large $V_{B1,E}$. Neutral base recombination could also contribute to this current For low base 1-emitter voltages, the current reversed its direction, and it was dominated by holes leaking through the valence band barrier into the

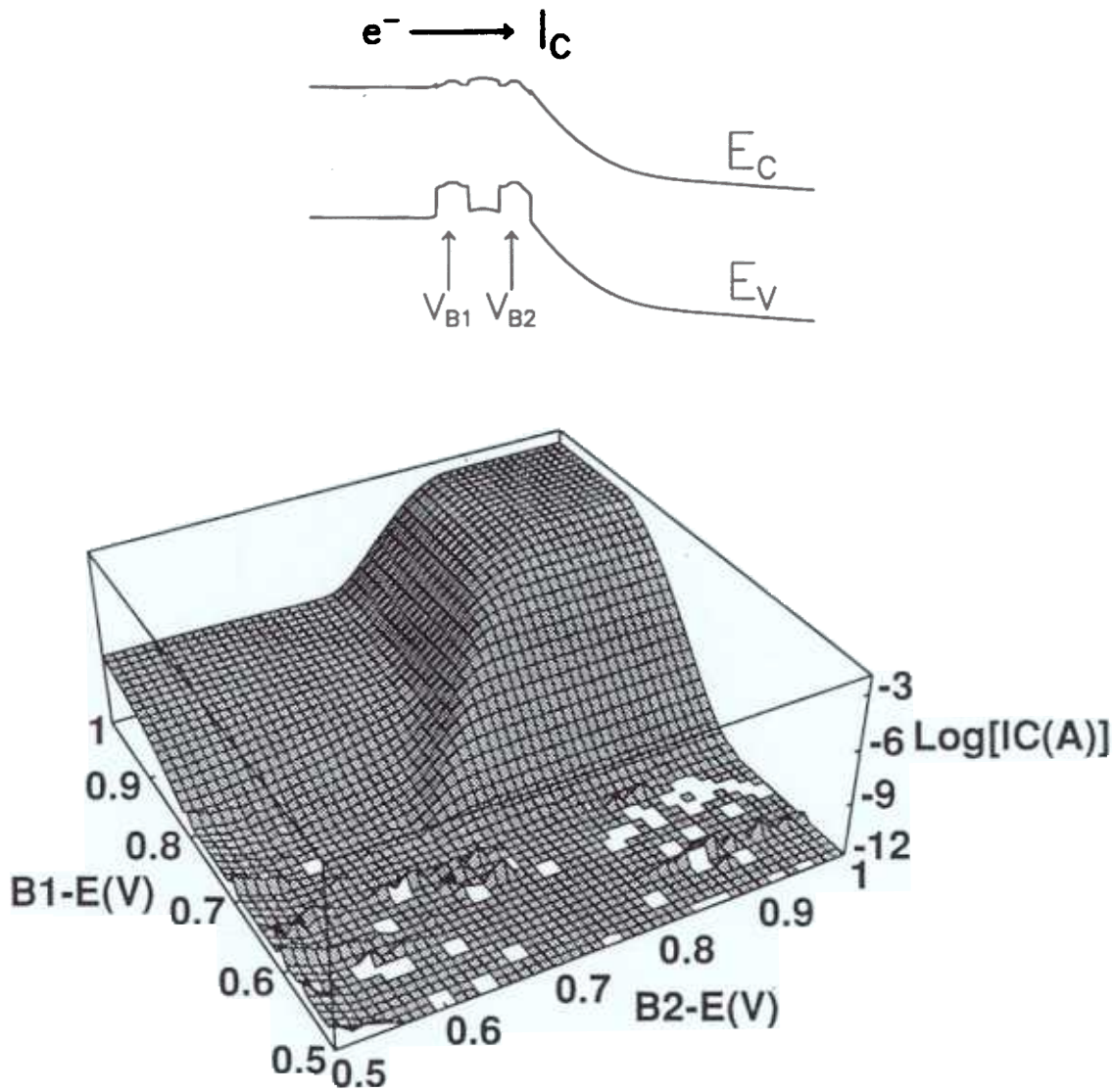


Figure 7.11: Measured collector current of DB-HBT #1077 at 77 K. Only if the voltages on both bases exceeded 0.8 V, were electrons injected into the base resulting in increased collector current.

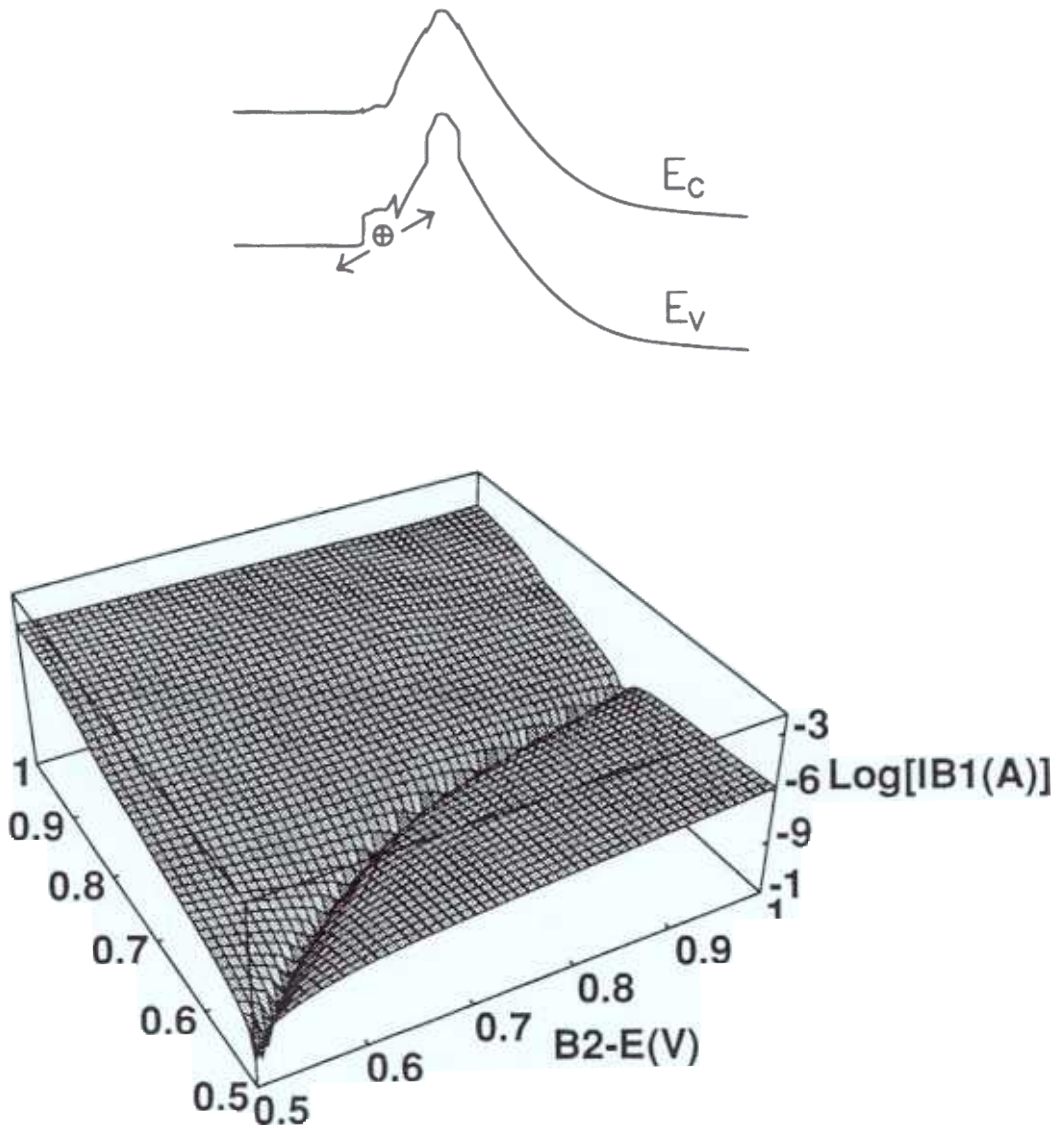


Figure 7.12: Measured magnitude of the current into base 1 vs. base input voltages of device #1077 at 77 K. It has two components due to (i) recombination of holes in the base-emitter junction, and (ii) due to leakage through the valence band barrier between base 1 and base 2.

base 2-layer.

The current into base 2 consists of holes traveling over the barrier to or from base 1, of holes recombining with injected electrons in the neutral base 2, and of holes generated by avalanche multiplication or thermal generation in the reverse-biased base-collector junction. The current into base 2 was symmetric with respect to the difference of the base input voltages, i.e. the voltage across the valence band barrier between base 1 and base 2, for values of V_{B1} and V_{B2} below the turn-on voltage of about 0.8 V, suggesting that it was dominated by holes leaking through this barrier. Above turn-on, however, there was a non-ideal component of base 2 current, probably due to neutral base recombination in base 2.

Since the collector current in a Double-Base HBT was controllable with either base input, a one-transistor NAND-gate could be built together with a 1 kΩ load resistor, as shown in Fig. 7.14, and operated at temperatures up to 150 K. Only if both base inputs were *HIGH* did collector current flow thereby driving the output *LOW*. This shows the increased functionality of the Double-Base HBT.

7.5 Electrical Evaluation of Band Diagram Parameters

Some parameters of the band diagram of Fig. 7.2 could be determined from electrical measurements. They are listed in Table 7.1, and schematically shown in Fig. 7.15. The thickness of the Si barrier, W_{Si} was measured with a capacitance-voltage measurement at 85 K, where the leakage current through the barrier was suppressed. Base 1 was shorted to the emitter and base 2 to the collector. From the measured value of the capacitance between the two bases, which acted as the plates of a capacitor with the Si barrier and the partly depleted i-$Si_{1-x}Ge_x$ spacers being the dielectric, the thickness of the isolating barrier was determined. The measured values of about 300 Å are consistent with the growth rates assumed for the Si and $Si_{1-x}Ge_x$ layers.

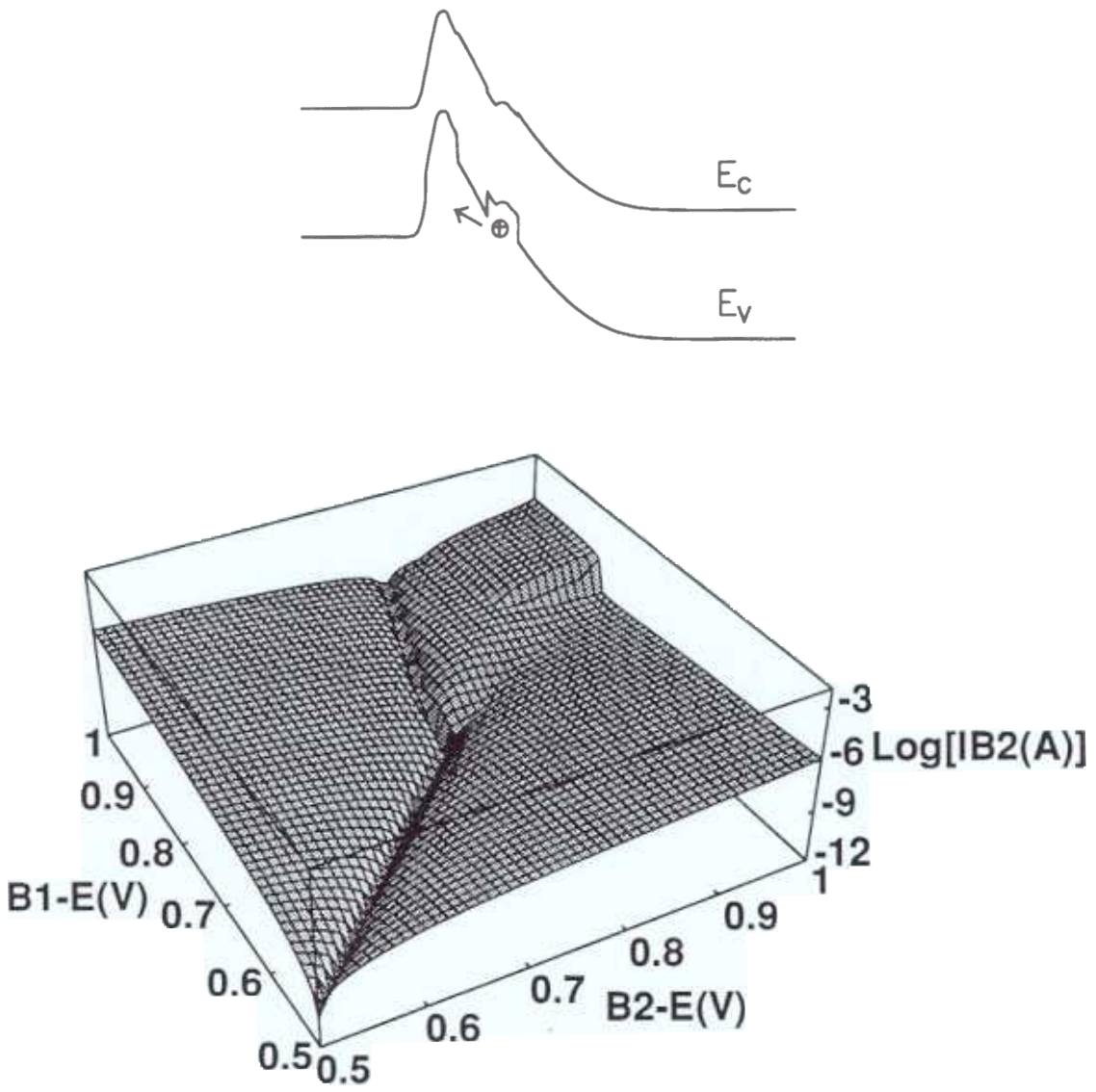
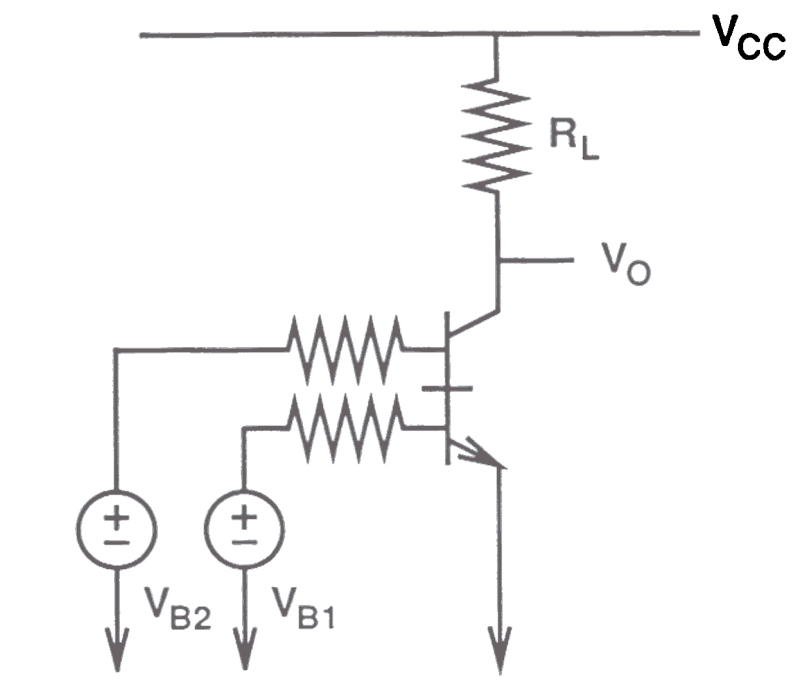


Figure 7.13: Measured magnitude of the current into base 2 vs. base input voltages of device #1077 at 77 K. Note that it was more symmetric in the base-voltage difference (i.e. the voltage across the valence band barrier), except for a non-ideal component at high values of both V_{B1} and V_{B2}.



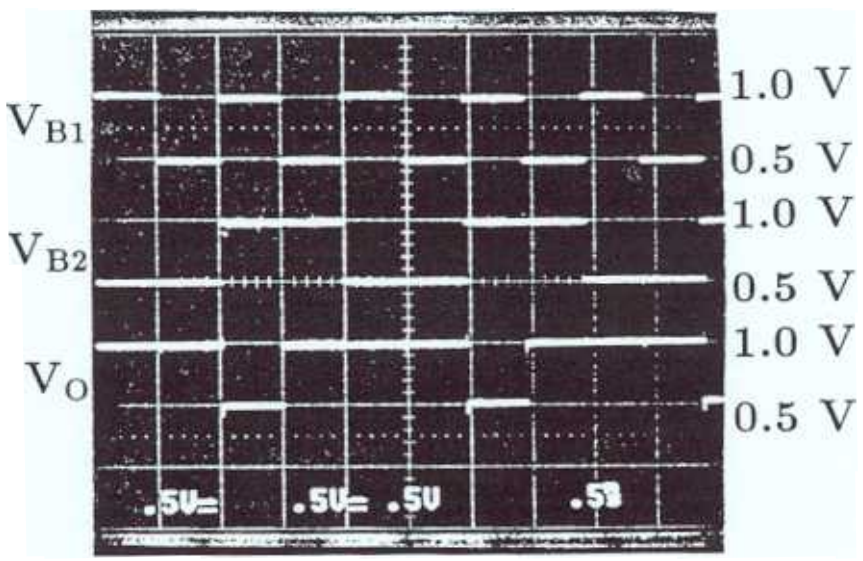


Figure 7.14: (a) Circuit diagram of single-transistor NAND gate which operated at temperatures up to 150 K; and (b) output from oscilloscope showing the base input voltages V_{B1} and V_{B2} and the output voltage V_O, and demonstrating the successful implementation of low-temperature single-transistor logic (time scale: 0.5 msec/div).

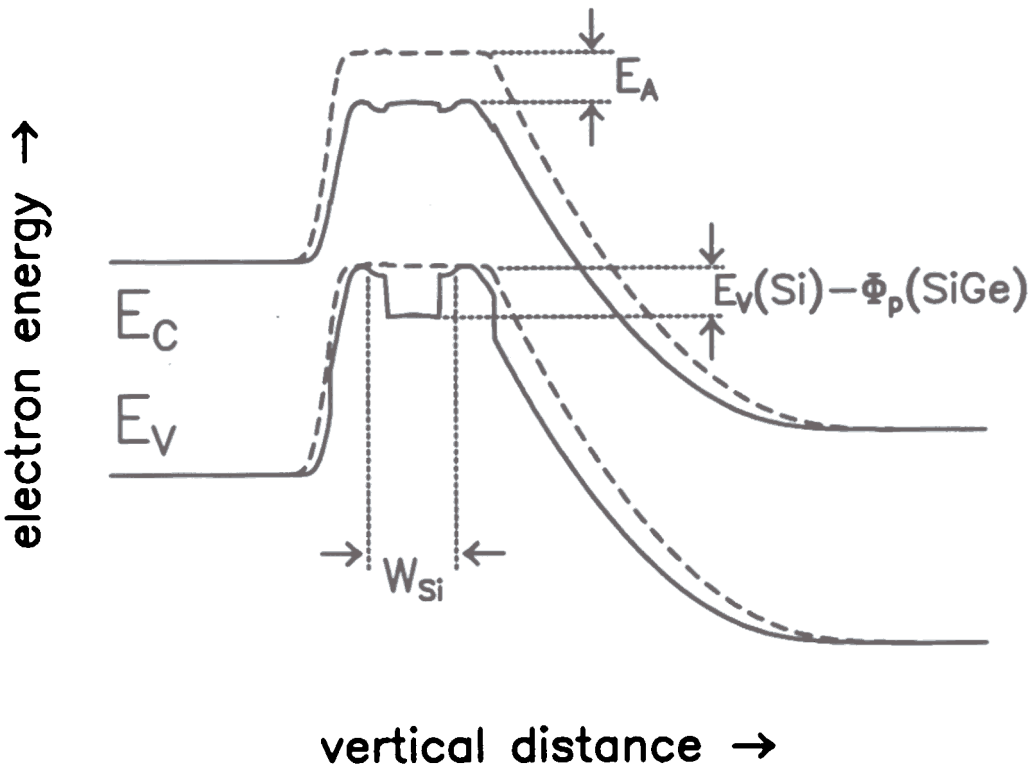


Figure 7.15: Band diagram of DB-HBT (solid lines) and Si homojunction transistor (dashed lines) showing the parameters determined from electrical measurements: barrier thickness W_{Si}; effective bandgap reduction E_A; and barrier height for holes, $\{E_V(Si) - \Phi_p(SiGe)\}$.

In wafer #1076 thicker i-$Si_{1-x}Ge_x$ spacer layers were inserted on both sides of the p-$Si_{1-x}Ge_x$ bases. This was reflected in a thicker barrier (427 Å).

The effective bandgap reduction E_A between the DB-HBT doped about 10^{18} cm^{-3} and a Si homojunction device doped 10^{19} cm^{-3} was determined from a temperature-dependent collector current measurement, with both bases externally shorted together. If there are no i-$Si_{1-x}Ge_x$ spacers and the Si barrier is fully depleted, E_A would be expected to be equal to the valence band discontinuity of the p-$Si_{1-x}Ge_x$ layer, because the conduction band in the Si barrier is higher by an amount ΔE_C than the one in the p-$Si_{1-x}Ge_x$ bases. The calculated band diagram of a structure with i-spacers shows, however, that in this case the bandgap reduction is closer to ΔE_G, the bandgap difference between the base layers of the DB-HBT and the Si control. The activation energies E_A of the Arrhenius plots, listed in Table 7.1, were between the expected values of ΔE_V and ΔE_G for the Ge concentrations used, except for device #1078. This proved that dopant diffusion or segregation into the Si barrier did not occur in our devices, since it would have degraded the measured E_A, as shown in the calculated band diagram of Fig. 7.5.

The current-voltage characteristics of the p-$Si_{1-x}Ge_x$/i-Si/p-$Si_{1-x}Ge_x$ barrier was also measured as a function of temperature. For this measurement, base 1 was externally shorted to the emitter, and base 2 was externally shorted to the collector. For temperatures below about 120 K, the leakage current through the barrier was a weak function of temperature, indicating that in this temperature range thermionic emission was suppressed. In the temperature range between about 120 K and 200 K, thermionic emission of holes over the valence band barrier caused a strong increase in current corresponding to the Richardson-law of thermionic emission [129]:

$$I_{B1,B2} = A_{B1}\, A^*\, T^2\, e^{-(E_V(Si)-\Phi_p(SiGe))/k_BT}$$

$$A^* = \frac{4\pi q m^* {k_B}^2}{h^3} \tag{7.2}$$

where A_{B1} is the area of the base 1 mesa, and A^* the effective Richardson constant. From these measurements the activation energy could be extracted which corresponds to the energy difference between the valence band in the Si barrier and the hole quasi-Fermi level Φ_p in the $Si_{1-x}Ge_x$ degenerately doped bases. The measured activation energy decreased with applied bias across the barrier, indicating that holes tunneled through the triangular part of the barrier (Fowler-Nordheim tunneling). The maximum values of $E_V(Si) - \Phi_p(SiGe)$ which were obtained at small biases of ≤ 0.02 V across the barrier are shown in Table 7.1. They are less accurate than the values of the effective bandgap reduction described above, because the exponential increase in $I_{B1,B2}$ was limited for temperatures above about 200 K by the parasitic resistance between the base 2 contact and the region of the base 2 layer vertically below base 1, and we estimate the error bars to be about 30 meV. Within this accuracy, the experimentally obtained hole barrier heights agreed with the expected values.

The close agreement between the three measured parameters of the band diagram shown in Table 7.1 and the expected values from theory proved again that the Double Base HBT's worked as described in Section 7.2.

Chapter 8

Conclusions and Suggestions for Further Research

The research leading to this thesis focussed on the vertical profile engineering in $Si/Si_{1-x}Ge_x/Si$ HBT's using a non-UHV growth technique, Rapid Thermal Chemical Vapor Deposition. The major achievements were:

- Near-ideal base currents in $Si/Si_{1-x}Ge_x/Si$ HBT's were achieved using a non-UHV technique for the first time. This was possible, because first, the growth procedures developed by Peter V. Schwartz (including installation of the load lock) resulted in oxygen-free $Si_{1-x}Ge_x$ alloy layers with a high minority carrier lifetime; and second, a HBT process was developed, similar to the one described by King *et al.* [22], which minimized parasitic components of base current. This achievement proved that high-lifetime $Si_{1-x}Ge_x$ material can be fabricated using processes compatible with standard silicon technology, i.e. chemical vapor deposition at reduced pressure (LP-CVD), and that UHV techniques are not required.

- Graded-base $Si/Si_{1-x}Ge_x/Si$ HBT's were fabricated in a non-UHV epitaxial technology for the first time, and their electrical characteristics were modeled analytically using charge-control theory. It was found necessary to incorporate into the model the strain-induced reduction of the effective densities of states

product $N_C N_V$ in the $Si_{1-x}Ge_x$ layer to accurately model the collector currents. No parameters were adjusted.

- The formation of parasitic conduction band barriers for electrons in the base of $Si/Si_{1-x}Ge_x/Si$ HBT's resulting from base dopant outdiffusion or non-abrupt interfaces was studied for the first time. It was found that the parasitic barriers degrade the current gain improvement possible in the HBT's. This effect is especially important in devices with narrow, heavily doped bases fabricated using processes with high thermal budget. To alleviate the performance degradation induced by base dopant outdiffusion into the adjacent silicon layers, intrinsic $Si_{1-x}Ge_x$ spacer layers were inserted on both sides of the base, resulting in an improved collector current, or, alternatively, in an increased thermal budget *without* collector current degradation, compared to HBT's without intrinsic $Si_{1-x}Ge_x$ spacers. A theory for the collector current in the presence of parasitic barriers was formulated for the first time.

- The tradeoff between the common-emitter current gain β and the Early voltage V_A (output resistance) in heterojunction bipolar transistors with graded bandgap bases was investigated for the first time. This tradeoff is important for analog applications of HBT's, and it has been shown that inserting a thin, narrow-bandgap layer in the base close to the base-collector junction reduces the Early effect dramatically leading to a high Early voltage. For optimum performance, base dopant outdiffusion into the silicon collector has to be prevented, for example by using the intrinsic $Si_{1-x}Ge_x$ spacer layers introduced above.

- A novel Double-Base HBT has been developed jointly with Xiaodong Xiao and Peter V. Schwartz which increases the functionality of HBT's. Temperature-dependent measurements proved that the DC characteristics of the DB-HBT can be modeled using a version of charge-control theory. Switching was demon-

strated in a single-transistor NAND gate at temperatures up to 150 K.

This thesis focussed on DC measurements on $Si/Si_{1-x}Ge_x/Si$ HBT's not optimized for lateral scaling of the device structure. Limitations by base dopant diffusion were studied, and opportunities for analog applications and increased functionality explored. This research could be extended in various ways:

- Phosphorus doping in the collector and subsequent temperature reduction for the growth of the $Si_{1-x}Ge_x$ strained layers resulted in phosphorus spikes incorporated at the $Si/Si_{1-x}Ge_x$ interface. This has not been observed in atmospheric pressure CVD (APCVD). We propose to study phosphorus incorporation and associated memory effects vs. pressure and temperature, with the goal of obtaining controlled phosphorus profiles in both emitter and collector of HBT's.

- All $Si/Si_{1-x}Ge_x/Si$ HBT structures presented in this work were grown non-selectively on <100> silicon wafers with a high temperature clean in hydrogen. For process integration of these devices selective epitaxy or non-selective epitaxy on a patterned substrate might be advantageous. Important issues to be studied are the dependence of selectivity on the chlorine content of the gas mixture, on the quality of the oxide (grown; implanted; plasma-deposited), on the cleaning method, and on the patterning method (plasma vs. chemical etching) used.

- Recently the epitaxial growth of singe-crystalline silicon carbide at temperatures below 800°C was reported using a CVD method. Rapid Thermal Chemical Vapor Deposition could be used to grow SiC and dope it *in-situ* with phosphorus (using PH_3) or arsenic (using AsH_3). The obvious application would be a wide-gap emitter/silicon spacer/$Si_{1-x}Ge_x$ graded base/silicon collector HBT combining the improved emitter efficiency of the wide-gap emitter HBT and the built-in drift field of the graded $Si_{1-x}Ge_x$ base HBT. In this device the Ge layer

could be grown below the equilibrium critical thickness, e.g. 0–20% Ge, while still maintaining a high current gain and low base sheet resistance. Devices could be fabricated in a low thermal budget process using chemical etching, or in an integrated circuit compatible process with self-aligned emitter and base contacts.

- In the Double-Base HBT, the material responsible for the barrier in the valence band should have a wider bandgap than silicon to achieve room-temperature operation of the device. SiC or the $Si_xGe_yC_{1-x-y}$ alloy could be employed as barrier material. Doping the intrinsic barrier layer n-type could help to achieve a higher barrier for holes in the valence band, and to prevent barrier lowering by the bias sustained between the two base contacts. Furthermore, since no doping diffusion induced degradation was observed in our first four wafers which were fairly lightly doped, the $Si_{1-x}Ge_x$ layer thickness could be decreased to prevent misfit dislocation formation.

- Boron diffusion in the strained $Si_{1-x}Ge_x$ alloy and boron segregation at the $Si/Si_{1-x}Ge_x$ interface have to be studied in more detail to estimate the thickness of intrinsic spacer layers for a given thermal budget of a process.

- The electrical activation of indium in silicon could be studied to obtain a dopant with lower diffusion constant.

Appendix A

Publications and Presentations Resulting from this Thesis

1. E. J. Prinz, X. Xiao, P. V. Schwartz, and J. C. Sturm, "A novel double base heterojunction bipolar transistor for low temperature bipolar logic," *Device Research Conf. Tech. Dig.*, p. IIA–2, 1992.

2. L. C. Lenchyshyn, M. L. W. Thewalt, J. C. Sturm, P. V. Schwartz, E. J. Prinz, N. L. Rowell, J.-P. Noël, and D. C. Houghton, "Photoluminescence spectroscopy of localized excitons in $Si_{1-x}Ge_x$," *Elec. Mater. Conf. Tech. Dig.*, 1992.

3. L. C. Lenchyshyn, M. L. W. Thewalt, J. C. Sturm, P. V. Schwartz, E. J. Prinz, N. L. Rowell, J.-P. Noël, and D. C. Houghton, "High quantum efficiency photoluminescence from localized excitons in $Si_{1-x}Ge_x$," *Appl. Phys. Lett.*, vol. 60, pp. 3174–3176, 1992.

4. E. J. Prinz and J. C. Sturm, "Current gain – Early voltage products in heterojunction bipolar transistors with nonuniform base bandgaps," *IEEE Electron Device Lett.*, vol. 12, pp. 661–663, 1991.

5. E. J. Prinz and J. C. Sturm, "Analytical modeling of current gain – Early voltage products in $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors," *International Electron Devices Meeting Tech. Dig.*, pp. 853–856, 1991.

6. J. C. Sturm, P. V. Schwartz, E. J. Prinz, and H. Manoharan, "Growth of $Si_{1-x}Ge_x$ by rapid thermal chemical vapor deposition and application to heterojunction bipolar transistors," *J. Vac. Sci. Technol. B*, vol. 9, pp. 2011–2016, 1991.

7. E. J. Prinz and J. C. Sturm, "Current gain – Early voltage products in graded base $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors," *Device Research Conf. Tech. Dig.*, p. IIB–5, 1991.

8. J. C. Sturm and E. J. Prinz, "Graded base $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors grown by rapid thermal chemical vapor deposition with near-ideal electrical characteristics," *IEEE Electron Device Lett.*, vol. 12, pp. 303–305, 1991.

9. E. J. Prinz, P. M. Garone, P. V. Schwartz, X. Xiao, and J. C. Sturm, "The effects of base dopant outdiffusion and undoped $Si_{1-x}Ge_x$ junction spacer layers in $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 12, pp. 42–44, 1991.

10. Ž. Matutinović-Krstelj, E. J. Prinz, P. V. Schwartz, and J. C. Sturm, "Reduction of the p^+-n^+ junction tunneling current for base current improvement in Si/SiGe/Si heterojunction bipolar transistors," *Proc. Mater. Res. Soc.*, vol. 220, pp. 445–450, 1991.

11. Ž. Matutinović-Krstelj, E. J. Prinz, P. V. Schwartz, and J. C. Sturm, "Reduction of the p^+-n^+ junction tunneling current for base current improvement in Si/SiGe/Si heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 12, pp. 163–165, 1991.

12. J. C. Sturm, P. V. Schwartz, E. J. Prinz, and C. W. Magee, "Control of oxygen incorporation and lifetime measurements in $Si_{1-x}Ge_x$ epitaxial films grown by

rapid thermal chemical vapor deposition," *Proc. SPIE Conf. on Rapid Thermal Processing*, vol. 1393, pp. 252–259, 1990.

13. J. C. Sturm, P. M. Garone, E. J. Prinz, P. V. Schwartz, and V. Venkataraman, "Interface abruptness in epitaxial silicon and silicon-germanium structures grown by rapid thermal chemical vapor deposition," *Proc. Int. Conf. on CVD XI*, vol. 90-12, p. 295, 1990.

14. J. C. Sturm, E. J. Prinz, P. V. Schwartz, P. M. Garone, and Ž. Matutinović-Krstelj, "Growth and transistor applications of $Si_{1-x}Ge_x$ structures by rapid thermal chemical vapor deposition," *Proc. Topical Symposium on Silicon Based Heterostructures, Toronto, Canada*, 1990.

15. E. J. Prinz and J. C. Sturm, "Base transport in near-ideal graded-base $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors from 150 K to 370 K," *International Electron Devices Meeting Tech. Dig.*, pp. 975–978, 1990.

16. E. J. Prinz, P. M. Garone, P. V. Schwartz, X. Xiao, and J. C. Sturm, "The effect of base emitter spacers and strain-dependent densities of states in $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors," *International Electron Devices Meeting Tech. Dig.*, pp. 639–642, 1989.

17. J. C. Sturm, E. J. Prinz, P. M. Garone, and P. V. Schwartz, "Band-gap shifts in silicon-germanium heterojunction bipolar transistors," *Appl. Phys. Lett.*, vol. 54, pp. 2707–2709, 1989.

18. J. C. Sturm, E. J. Prinz, P. M. Garone, and P. V. Schwartz, "Electron transport in silicon-germanium strained-layer heterojunction bipolar transistors," 1989 March Meeting of the American Physical Society, Saint Louis, MO, 1989.

Appendix B

Growth and Processing Details

Schematic Mask Layout for HBT Process

The mask set supplied by Dr. Cliff King consists of seven masks; base implant (dark field), emitter implant (dark field), base mesa (bright field), contact hole (dark field), metal (bright field), and (not shown) a big mesa surrounding base and collector. The key feature is that the base implant surrounds the emitter, forming a junction isolation between the base and the emitter contact. This is important because it is much easier to obtain emitter-injection limited transistors with near-ideal base currents using a junction-isolated base-emitter junction, compared to mesa isolation. For the Double-Base HBT, several other masks were fabricated from this mask set, by adding or subtracting existing masks using photolithographic techniques. Figs. B.1 and B.2 show a schematic top view of the masks described above. Unfortunately there were no test structures on the mask set for base sheet resistance measurements Hall bars were therefore processed simultaneously with the transistors

Growth Parameters for Graded-Base Devices #448–450

Here we tabulate the base Ge and doping profiles of the graded-base devices of Chap. 4 The nominally 500 Å thick bases were divided into ten 50 Å segments

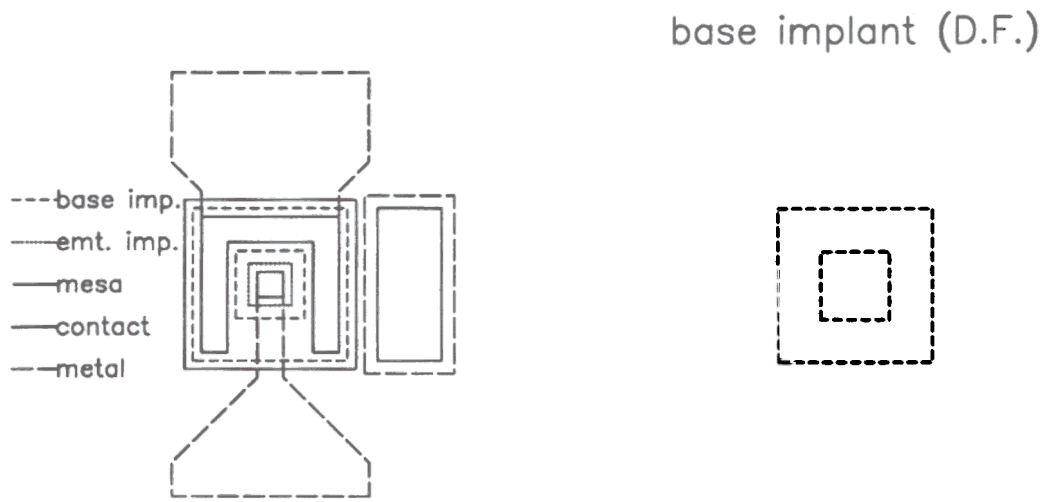


Figure B.1: Schematic layout of mask set for the fabrication of junction-isolated bipolar transistors with all masks superimposed (left), and base implant mask (D.F. = dark field mask, B.F. = bright field mask).

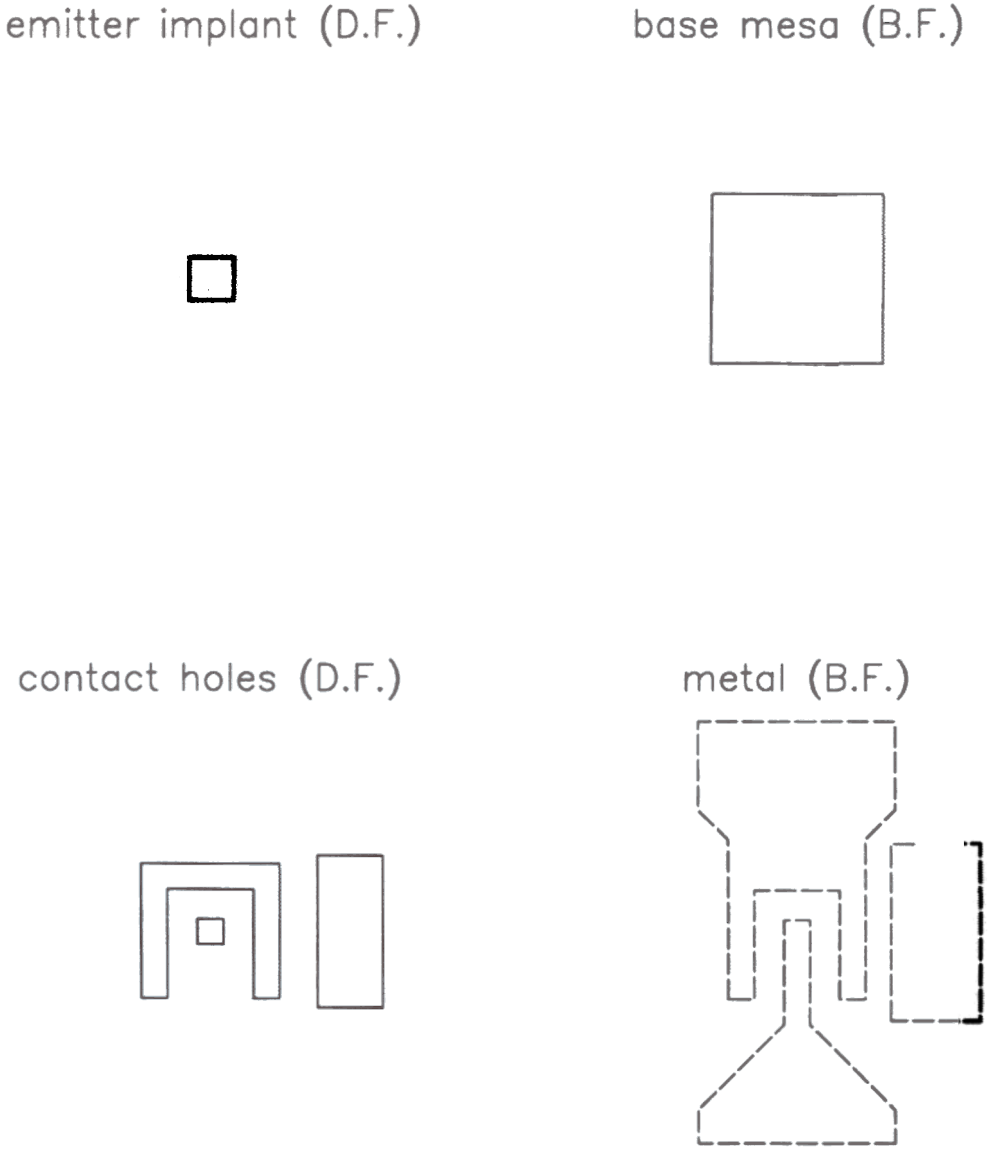


Figure B.2: Schematic layout of emitter implant, base mesa, contact hole, and metal mask used in this work. The base mesa mask was about 15 μm larger on each side than the outer edge of the base contact hole.

Table B.1: Base layers of graded-base HBT #448 grown at 625°C.

#448, 13–20% Ge				
time (sec)	Ge conc. (%)	Ge flow (sccm)	growth rate	B_2H_6 flow
30	20.0	105	100	11.4
33	19.2	95	90	10.3
37	18.4	85	81	9.3
42	17.7	76	72	8.2
48	16.9	66	63	7.2
57	16.1	56	53	6.1
68	15.3	46	44	5.0
86	14.6	37	35	4.0
115	13.8	27	26	3.0
188	13.0	17	16	1.8

with piecewise constant Ge and boron concentration. The growth rates and Ge flows were interpolated between previously determined growth parameters. The diborane flow rate was adjusted proportional to the estimated growth rate. Note that the Ge flow referred to 0.78% GeH_4 in H_2, and the B_2H_6 flow to 10 ppm B_2H_6 in H_2.

B.3 Sequencer Tables for the Growth of a HBT Layer Sequence

In the last runs (> #600) the RTCVD system was controlled by an IBM compatible computer which accessed lamp power, pressure, most valves, and all mass flow controllers. The infrared transmission setup developed at Princeton was used as the

Table B.2: Base layers of graded-base HBT #449. All layers with Ge concentrations above 13% were grown at 625°C, while the others were grown at 700°C.

#449, 7–20% Ge				
time (sec)	Ge conc. (%)	Ge flow (sccm)	growth rate	B_2H_6 flow
30	20.0	105	100	10.0
36	18.6	87	83	9.5
46	17.1	69	65	7.4
63	15.7	51	48	5.5
100	14.2	32	30	3.4
15	12.8	118	196	49
17	11.3	101	175	44
19	9.9	85	156	39
22	8.4	68	136	34
26	7.0	52	117	29

temperature measurement input of a feedback control. Here we print the sequencer tables for the growth of a $Si/Si_{1-x}Ge_x/Si$ HBT with a $Si/Si_{0.80}Ge_{0.20}/Si$ flat base doped 10^{20} cm^{-3} (#936) for future reference. They were adapted from a growth sequence designed by Peter V. Schwartz.

Table B.3: Base layers of graded-base HBT #450. The first three layers were grown at 625°C, and the others were grown at 700°C.

#450, 0–20% Ge				
time (sec)	Ge conc. (%)	Ge flow (sccm)	growth rate	B_2H_6 flow
30	20.0	105	100	10.0
41	17.8	77	74	8.5
64	15.6	50	47	5.4
15	13.3	124	202	51
17	11.1	99	173	43
21	8.9	74	143	36
27	6.7	49	113	28
34	4.4	30	87	22
47	2.2	15	64	16
75	0.0	0.0	40	10

Table B.4: Sequencer tables for flat-base HBT. In sequencer #0, all valves are shut, except for the hydrogen flow. At the end, sequencer #1 is called.

Sequencer Table #0		
Step #	Action	Comment
0	control on&	turn on control
1	scan on (0.3)	and scan simultaneously
2	set (sp7, 0)&	overrides power to zero
3	set (sp4, 0)&	turn off PID control
4	set (sp0, 0.6)	zero loop count
5	set (do0, 1)&	nitrogen off
6	set (do1, 0)&	hydrogen off
7	set (do2, 0)&	silane off
8	set (do3, 0)&	germane off
9	set (do4, 0)&	diborane off
10	set (do5, 0)&	phosphine off
11	set (do6, 0)&	X off
12	set (do7, 0)&	dichlorosilane off
13	set (do8, 0)&	HCl off
14	set (do9, 0)&	inject off silane
15	set (do10, 0)&	inject off germane
16	set (do11, 0)&	inject off diborane
18	set (do13, 0)	inject off dichlorosilane
19	set (ao0, 0.617)&	toxic lines flow
20	set (do15, 1)	vacuum on
21	set (do1, 1)&	hydrogen on
22	set (ao1, 0.01)&	silane flow
23	set (ao2, 0.01)&	germane flow
24	set (ao3, 0.01)&	diborane (high)
25	set (ao4, 0.01)&	phosphine (high)
26	set (ao5, 0.01)&	phosphine (low)
27	set (ao6, 0.537)&	dichlorosilane
28	set (ao7, 0.1)	diborane
29	set (ao8, 0.0)	pump out
30	sequencer on (0.3, 1, 0)	start sequencer #1
31		

Table B.5: Sequencer #1 is the top most control loop.

Sequencer Table #1		
Step #	Action	Comment
0	set (sp1, 1)&	set layer number
1	set (sp2, 0.0)&	reset loop counter
2	sequencer on (0.3, 6, 0)	call cleaning sequence
3	waituntil (sp2 > 0.5)	cleaning sequence
4	set (sp2, 0.0)&	reset loop counter
5		
6	sequencer on (0.3, 5, 0)	call buffer layer sequence
7	waituntil (sp2 > 0.5)	buffer layer sequence
8		
9	set (sp5, 3.51)&	set feedback temperature T=700°C
10	set (sp4, 1)&	turn on feedback loop
11	set (sp2, 0.0) &	reset loop control
12	sequencer on (0.3, 4, 8)	call silicon layer sequence
13	waituntil (sp2 > 0.5)	silicon layer sequence
14	set (sp2, 0.0)&	reset loop control
15		
16	sequencer on (0.3, 2, 0)	call base-emitter sequence
17	waituntil (sp2 > 0.5)	
18	inc (sp0, 1.0)&	increment loop counter
19	gotoif (sp0 > sp1, 11, 20)	loop check
20	set (sp2, 0.0)&	reset loop control
21		
22	sequencer on (0.3, 3, 0)	call cap layer sequence
23	waituntil (sp2 > 0.5)	cap layer sequence
24	set (sp2, 0.0)&	reset loop control
25		
26	sequencer on (0.3, 7, 0)	call reload sequence
27		
28		
29		
30		
31		

Table B.6: Sequencer #2 grows the p-$Si_{1-x}Ge_x$ base with intrinsic $Si_{1-x}Ge_x$ spacers on both sides.

Sequencer Table #2		
Step #	Action	Comment
0	set (sp5, 2.843)&	set T=700°C
1	wait (15)	temperature stabilizing
2	set (do10, 1)&	inject germane
3	wait (150)	intrinsic spacer I
4		
5		
6	set (do11, 1)&	inject diborane
7	wait (150)	growing base
8	set (do11, 0)&	diborane off
9	wait (150)	intrinsic spacer II
10	set (do10, 0)&	germane off
11	wait (10)	purge tube
12		
13	set (do4, 0)&	diborane select off
14	set (ao3, 0.01)&	diborane flow down
15	set (do2, 0)&	germane select off
16	set (sp7, 0.195)&	lamps to 850
17	set (sp4, 0)&	feedback off
18		
19		
20	set (do12, 1)&	phosphine on
21	wait (450)	growing emitter
22	set (do12, 0)&	phosphine off
23	set (do13, 0)&	dichlorosilane off
24	wait (10)	purge tube
25	ramp (sp7, -0.4, 0.0)	lamps off
26		
27		
28	sequencer on (0.3, 7, 0)	call reload sequence
29		
30		
31		

Table B.7: Sequencer #3 grows part of the emitter

Sequencer Table #3		
Step #	Action	Comment
0	set (sp5, 3.557)&	set T=700
1	set (ao3, 0.5)&	set up dopant flow
2	wait (10)	temperature stabilizing
3		
4	set (do11, 1)&	dopant
5		
6		
7	wait (60)	growing cap layer
8	set (do11, 0)&	dopant off
9	set (do13, 0)&	dichlorosilane off
10		
11	wait (5)	purge tube
12	set (sp4, 0)	feedback off
13	ramp (sp7, -0.4, 0.0)	lamps off
14	set (sp2, 1.0)	done
15		
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Table B.8: Sequencer #4 grows the n^- collector. The commands after step 15 are not executed.

Sequencer Table #4		
Step #	Action	Comment
0	set (sp5, 3.557)&	T=700°C
1	set (ao3, 0.213)	set up dopant flow
2	wait (10)	temperature stabilizing
3	set (do11, 1)&	inject dopant
4		
5	wait (300)	growing silicon layer
6	set (do11, 0)&	dopant off
7		
8	wait (60)	purge tube
9		
10		
11		
12		
13		
14	set (sp2, 1.0)&	
15	end	done
16	set (sp5, 2.800)&	set T=625°C
17	set (ao3, 0.213)&	set up germane flow
18	wait (10)	temperature stabilizing
19		
20	set (do19, 1)	germane on
21		
22	wait (60)	growing alloy layer
23	set (do10, 0)&	germane off
24		
25	wait (10)	purge tube
26		
27		
28		
29		
30	set (sp2, 1.0)&	done
31	end	

Table B.9: Sequencer #5 controls the growth of the n^+ buffer layer.

Sequencer Table #5		
Step #	Action	Comment
0	waituntil (ai29 < 10)	pumping out
1	waituntil (ai24 > 0.5)	open low pressure - GO for buffer
2	set (ao11, 1)&	low pressure select
3	waituntil (ai28 <5.5)	pressure stabilizing
4	set (ao8, 0.60)&	set pressure to 6 torr
5	waituntil (ai28 > 5.5)	pressure stabilizing
6	wait (10)	
7	set (do13, 1)&	inject dichlorosilane
8	set (do12, 1)&	phosphine on
9		
10	wait (600)	growing buffer layer
11	set (do13, 0)&	dichlorosilane off
12	set (do12, 0)&	dopant off
13		
14	wait (5)	purge tube
15	ramp (sp7, -0.4, 0.0)	lamps off
16	wait (420)	cool down period
17	set (do3, 1)&	select germane
18	set (ao2, 0.223)&	set up germane flow
19	set (ao3, 0.814)&	set up diborane flow
20	waituntil (ai24 > 0.5)	press GO for cold values
21	set (sp3, 1)&	get cold values
22	wait (1)	
23	set (sp3, 0)&	latch cold values
24	ramp (sp7, 0.4, 0.274)	lamps up to 1000°C
25	wait (60)	clean
26	set (do13, 1)&	dichlorosilane on
27	wait (180)	growing intrinsic collector
28	set (do11, 0)&	diborane off
29	ramp (sp7, -0.4, 0.155)	lamps down to 15%
30	set (sp2, 1.0)	done
31		

Table B.10: Sequencer #6 controls the hydrogen bake at ≈ 1000°C and 250 torr.

Sequencer Table #6		
Step #	Action	Comment
0	waituntil (ai24 > 0.5)	close LP - press go for clean
1	set (ao11, 0)&	high pressure select
2	set (ao8, 0.250)&	set pressure to 250 torr
3	set (ao0, 0.817)&	hydrogen flow = 4slpm
4	waituntil (ai29 > 250)	pressure stabilizing
5	set (ao1, 0.01)&	set flows — silane
6	set (ao2, 0.01)&	germane
7	set (ao3, 0.514)&	diborane
8	set (ao4, 0.01)&	phosphine high
9	set (ao5, 1.0)&	phosphine low
10	set (ao6, 1.0)&	diborane high
11	set (ao7, 0.0)&	diborane low
12		
13	set (do2, 0)&	select — silane
14	set (do3, 0)&	germane
15	set (do4, 1)&	diborane
16	set (do5, 1)&	phosphine
17	set (do7, 1)	dichlorosilane
18	wait (60)	purging mass flow controllers
19	set (ao1, 0.01)&	set up gas flows — silane
20	set (ao2, 0.01)&	germane
21	set (ao3, 0.05)&	diborane high
22	set (ao4, 0.05)&	phosphine high
23	set (ao5, 0.263)&	phosphine low
24	set (ao6, 0.537)&	dichlorosilane
25	set (ao7, 0.01)&	diborane low
26		
27	ramp (sp7, 0.4, 0.274)	lamps up to T=1000°C
28	wait (60)	cleaning
29	set (ao8, 0.0)&	pump out
30	(ao0, 0.617)&	set hydrogen flow to 3slpm
31	set (sp2, 1.0)	done

Table B.11: Sequencer #7 shuts all valves and leaves the system ready for unloading.

Sequencer Table #7		
Step #	Action	Comment
0	set (sp7, 0.0)	lamps off
1	set (do13, 0)&	injects off — dichlorosilane
2	set (do12, 0)&	phosphine
3	set (do11, 0)&	diborane
4	set (do10, 0)&	germane
5	set (do9, 0)&	silane
6	set (do7, 0)&	selects off — dichlorosilane
7	set (do5, 0)&	phosphine
8	set (do4, 0)&	diborane
9	set (do3, 0)&	germane
10	set (do2, 0)&	silane
11	set (do1, 0)	hydrogen
12	set (ao8, 0.0)	pump out
13	set (ao7, 0.0)&	flows off — diborane
14	set (ao6, 0.0)&	dichlorosilane
15	set (ao5, 0.0)&	phosphine low
16	set (ao4, 0.0)&	phosphine high
17	set (ao3, 0.0)&	diborane high
18	set (ao2, 0.0)&	germane
19	set (ao1, 0.0)&	silane
20	set (ao0, 0.0)	hydrogen
21	waituntil (ai28 < 0.5)	pump out
22	set (do15, 0)	vacuum off
23		
24	sequencer off (0)	sequencer 0 off
25	sequencer off (1)	sequencer 1 off
26	sequencer off (2)	sequencer 2 off
27	sequencer off (3)	sequencer 3 off
28	sequencer off (4)	sequencer 4 off
29	sequencer off (5)	sequencer 5 off
30	sequencer off (6)	sequencer 6 off
31	sequencer off (7)	sequencer 7 off

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