Think Big!

Thin-Film Electronics

For Large-Scale Hybrid Systems

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Abstract

Large-Area Electronics offers the potential for physically large, mechanically flexible, inexpensive sensing systems enabling interfaces on the human-scale. Though computational devices such as thin-film transistors (TFTs) can also be built using this technology, their low electrical performance tends to preclude their use in creating full sensing systems that also incorporate instrumentation, communication or power-management. We suggest an approach that combines large-area electronics with conventional, high-performance, silicon integrated circuits in order to realize complete system demonstrations.

The key challenge in these *hybrid systems*, however, lies in the ability to scalably interface the two technologies: thin-film large-area electronics and CMOS integrated circuits. In this thesis we explore a wide range of thin-film circuits and architectures to achieve this, namely circuits for non-contact powering from thin-film energy harvesting and storage devices, circuits for communication in the form of the first thin-film radio on plastic, circuits for interfacing wirelessly between large numbers of sensors and ICs and circuits for reducing interfaces through embedded variation-tolerant thin-film computation. These functionality blocks are presented as components of, for example, full systems for strain-sensing or image classification from image sensors. The limitations of thin-film electronics in terms of DC/AC electrical performance and noise is also carefully studied, with optimizations suggested, throughout this thesis, from the materials up to the systems level.

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Chapter 1

Introduction: From materials, to devices, to systems

1.1 Aim

Large-area electronic systems have the potential to transform the way in which information about the world around us is acquired and the way in which humans interact with their environment. An overarching goal has been the creation of electronic skins, rich in sensing and computation functionality; this is on the path to being made feasible thanks to the development of a plethora of electronic materials and devices that can be manufactured on substrates that span physically-large areas conformably, scalably and at low cost. Such soft and flexible electronic technologies, often based on thin-film semiconducting materials (amorphous silicon, organics, metal oxides...) are emerging as key candidates for realizing architectures for these physically-large platforms.

These technologies however, typically only offer modest electrical performance in contrast with crystalline-silicon based Complementary Metal Oxide Semiconductor (CMOS ICs), which have continued to gain in computation ability thanks to successful Moore's Law scaling. In order to realize complete systems, we believe that close integration of these two technologies will be required, though the challenges in interfacing the two are non-trivial. In this introduction we explore the strengths and weaknesses of Large-Area and CMOS electronics.

1.2 Large-Area Electronics

Large-Area Electronics (LAE) allows us to deposit thin-films of insulators and semiconductors at low temperatures. They thus offer the ability for depositing and patterning (rather than assembling) arrays of sensors and associated active circuits over the span of meters on a wide variety of plastic, glass, metal and even paper substrates. Thin-film semiconductors can also offer the benefit of making the system autonomous by integrating energy harvesting.

1.2.1 Thin-film electronics for sensing

A particular advantage of large-area electronics is the ability for sensing with *high spatial resolution*. A multitude of sensors have been demonstrated, some of which are illustrated in Figure 1.1. The rich diversity of materials available allows us to build, for example, sensors for visible light [25], x-rays [26], temperature [27], sound [28] and pressure [4], strain [3], moisture or gases/chemicals [29].

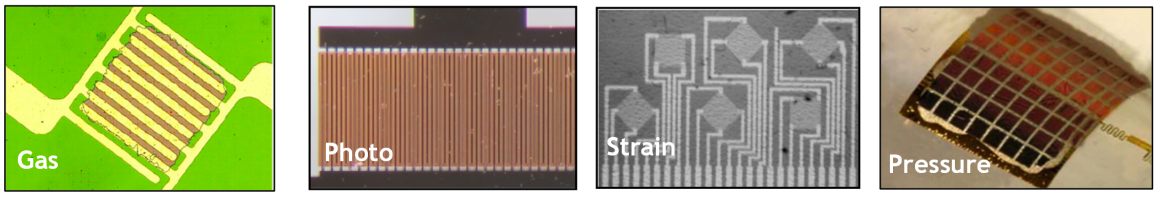


Figure 1.1: Examples of thin-film gas [1], light [2], strain [3] and pressure [4] sensors

In general, the materials used in these sensors are configured in simple structures such as capacitors, diodes or transistors, with the electrical properties of these modulated by the sensed quantity.

1.2.2 Thin-film electronics for energy-harvesting/storage

Since in many cases the power that can be extracted from energy-harvesters and stored scales with physical size, large-area electronics is an excellent option. Figure 1.2 illustrates some of the technologies available, such as solar modules, piezoelectric [11] or thermoelectric [30] harvesters.

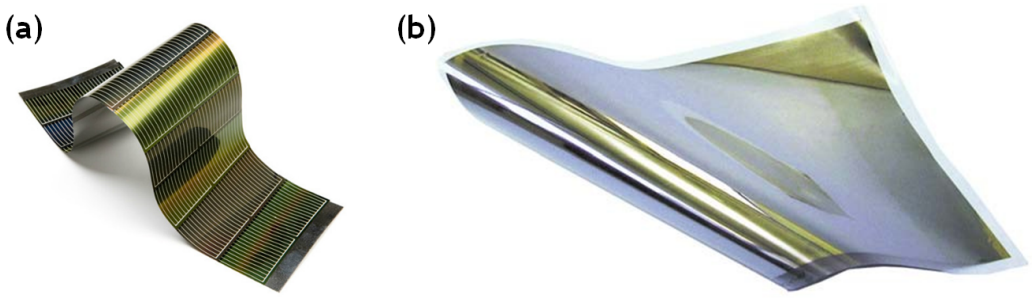


Figure 1.2: Examples of energy harvester: (a) solar module [5] (b) PVDF piezoelectric sheet [6]

Table 1.1 gives typical harvested power levels for some representative technologies; these can be seen to be quite substantial, which makes them attractive, in particular given the fact that, for example, amorphous silicon can be deposited cheaply over a physically large area.

Table 1.1: Typical harvested power levels

Harvesting Device	**Condition**	**Harvested Power Level**
Solar Module (a-Si)	Indoor lighting	$10\,\mu W\,cm^{-2}$
	Outdoor in full sunlight	$10\,mW\,cm^{-2}$
Piezoelectric (PZT of ZnO)	Mechanical vibration $2.25\,m\,s^{-2}$, 120Hz	$200\,\mu W\,cm^{-2}$
	Normal walking human	$330\,\mu W\,cm^{-2}$
Thermoelectric	ΔT=5C	$80\,\mu W\,cm^{-2}$

With regards to storage, either large supercapacitors or thin-film batteries may be used. For the latter, these are typically made out of micrometer thick layers of materials similar to those found in conventional lithium ion batteries (Lithium, Lithium Cobalt Oxide...) deposited for example by sputtering or chemical vapor deposition (CVD) [31]. This allows the batteries to be less than a millimetre thick, thus lightweight and mechanically flexible, with capacities in the few hundreds of microampere hours. An example is shown of such a thin-film Li-ion battery in Figure 1.3, which also shows a cross-section of the battery with many stacked layers of charge-storage materials.

1.2.3 Thin-film electronics for computation

Whilst computation is not a strength of large-area electronics, devices are nonetheless available to do so, namely Thin-Film Transistors (TFTs). Once again, these have been demonstrated using countless material systems, with the most dominant ones being amorphous silicon (which enabled the display revolution), organics, metal oxides and low-temperature polysilicon (LTPS). The latter

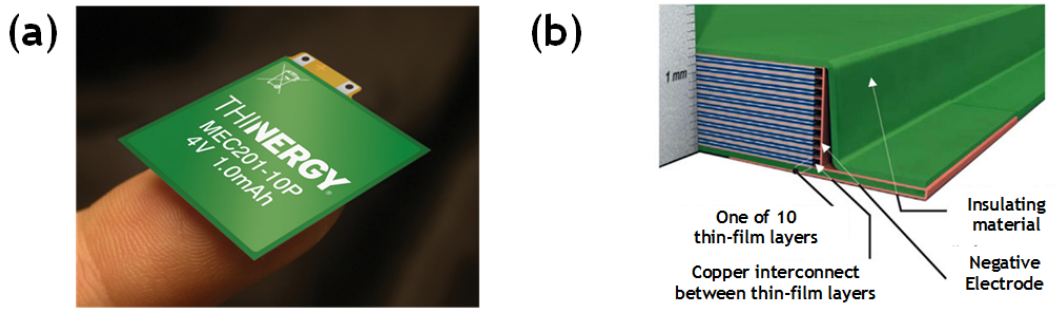


Figure 1.3: Thin-film lithium-ion battery: (a) flexible packaging [7] (b) cross-section of the Lithium-ion battery [8]

is receiving renewed interest presently as costs of the laser used in the crystallization technique required for the process have been going down. Whilst the first three technologies are almost exclusively unipolar, LTPS offers the potential for bipolar devices. In practice though, as a result of uniformity challenges, the fabrication areas possible using LTPS are substantially lower than, for example, in a-Si technology.

Much work has been done to combine the thin-film devices into circuits and fully integrated LAE building blocks. Some examples are shown in Figure 1.4. Figure 1.4(a) shows an analog to digital converter realized completely using organic thin-film transistors, Figure 1.4(b) shows a radio on plastic based on a-Si (which we present in this thesis) and Figure 1.4(c) shows an organic-based insole pedometer with PZT-based energy harvesting.

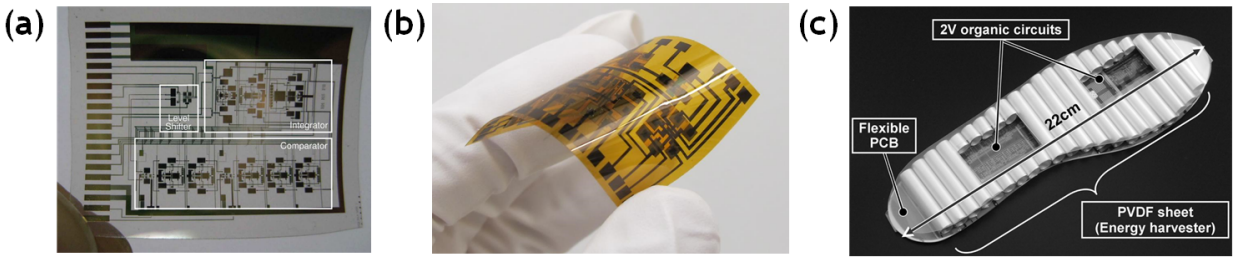


Figure 1.4: Fully-thin-film systems: (a) ADC [9] (b) radio [10](c) insole pedometer [11]

Whilst these systems demonstrate the viability of creating simple circuit and architectures using thin film devices, in practice though, it is much more likely that the circuits constructed in LAE will consist of a minimal number of interface blocks to sensing units. The complex computations will then be performed in the CMOS domain, where transistors exhibit mobilities which are several orders of magnitude higher.

Table 1.2 summarizes this discussion about the complementary strengths of thin-film and CMOS technologies.

Table 1.2: Complementary strengths of thin-film and CMOS technologies

Attribute	CMOS	Thin-Film
Sensors	*Only small, sparse sensing capability*	**Many, diverse sensors patternable on large flexible substrates**
Energy Harvesting	**Efficient power management circuits**	**Physically large harvesters for substantial power**
Energy Storage		**Flexible, thin-film batteries (moderate capacity)**
Display	**Able to drive large displays**	**Ability to pattern large displays based on TFT technology**
Communication	**High performance wireless and wireline transceivers**	**Low-loss interconnects**
Instrumentation/ Computation	**High performance, highly energy efficient CMOS transistors for computation and instrumentation**	*Low-performance transistors only*

1.3 Hybrid systems

So far, we have described a number of components that could be used in creating large-area systems. This number of components and the ability to integrate them is now becoming a key challenge to demonstrating the viability of electronics on conformable substrates as a platform for large-scale sensing.

A multitude of approaches to tackle this integration challenge have been proposed, some of which are highlighted in Figure 1.5. The Holy Grail of flexible electronics has long been considered the ability to monolithically pattern all components and functions required of a sensing platform onto a single (flexible) substrate as in Figure 1.5(a). To that end prototype systems have been built such as [32][33]. Whilst this assembly method may seem attractive as it follows the successful example of monolithic integration of microelectronic circuits, ultimately the scaling up of this approach to large areas is likely to prove unwieldy. Fully integrated assembly is excluded primarily

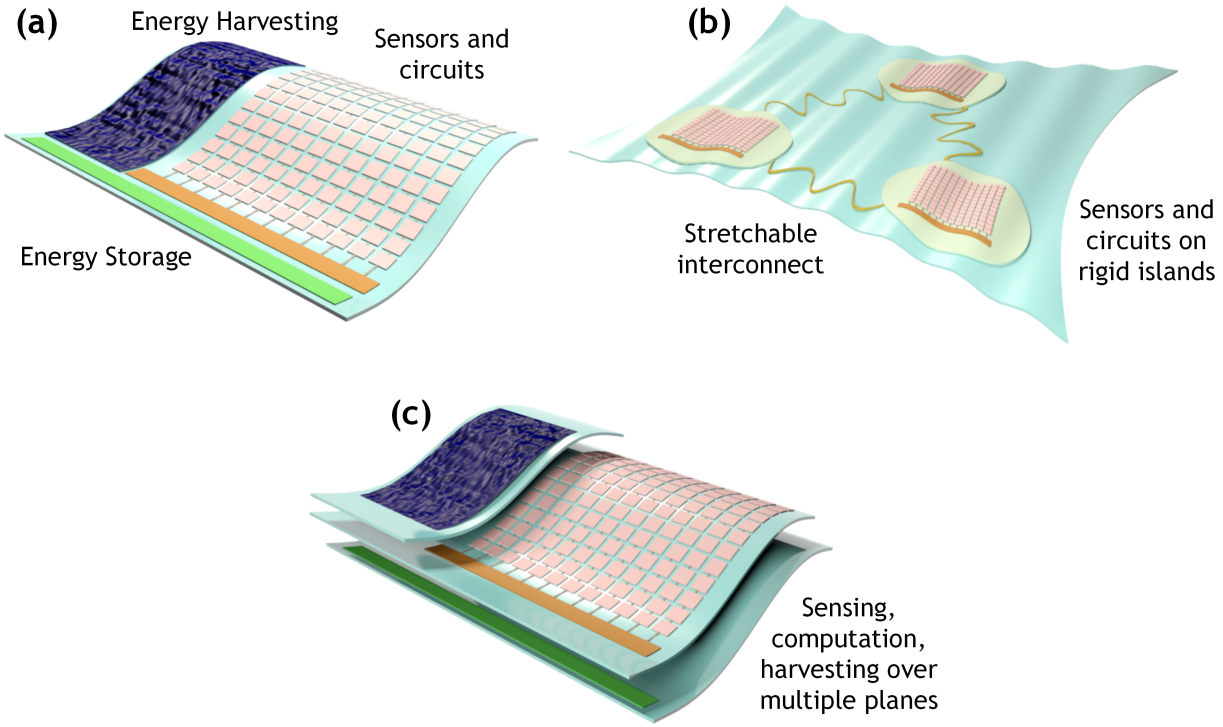


Figure 1.5: Three different approaches to achieving integration of functionality to create flexible electronic systems: (a) monolithic integration of all components on a single sheet (b) components on localized multi-functional more rigid islands, (c) separation of subsystems onto multiple functional planes

by the range of functions that a large-area electronic system will need as previously identified: from sensing over large surfaces with slow thin-film devices and circuits to the fast control, computation, and communication that only CMOS circuits can provide. The potential need to combine multiple material systems also precludes this integration type, even in the case of printing technologies where complex interconnection of multiple stacked layer structures has yet to be demonstrated. Monolithic integration will result in limited diversity and low yield, implying limited application scope and high cost.

An alternate approach shown in Figure 1.5(b) relies on the creation of localized, modular, functional islands, on top of a large flexible or stretchable substrate. This approach has most commonly been taken in the stretchable electronics community as a means of protecting active devices and circuits from mechanical strain when substrates are highly deformed or stretched [34][35][36][37][38][39]. When only bending is desired the mechanics become similar to that of

flip-chips on flexible substrates [40]. However, covering a large area with flexible chips by pick-and-place is too costly on the surface area scale of large-area electronics. On the other hand, processing high-performance circuits over large areas also is too costly when high-temperature materials must be integrated on low-temperature substrates (e.g. microcrystalline silicon on plastic [41]) or processed over large surfaces (e.g. microcrystalline silicon on steel foil [42]). Moreover, coplanar integrated circuits that are more rigid than the substrate become susceptible to the mechanical hence electrical weakness of interconnects at their transitions between the rigid circuit island and the deformable or stretchable substrate [43]. While engineered substrates can attenuate this transition from hard to soft [44], making these raises cost.

For building flexible systems we propose a contrasting approach, which shall be explored in depth in this thesis, in which components up to subsystems are separated into multiple functional layers rather than combined in a single plane. The approach is illustrated in Figure 1.5(c). It eases the integration challenge by replacing monolithic in-plane integration by pseudo-3D integration. In this approach different component modules of a flexible system are manufactured in different thin-film technologies, and CMOS integrated circuits are interfaced using chip-on-flex or chip-on-board techniques. This approach enables the modularization of functions and system customizability for modular mass production. The key challenge now becomes how to make robust yet simple interfaces between the different layers of this skin-like architecture.

Figure 1.6 shows the concept of our skin-like approach to assembling modular electronic systems, which consists of multiple sub-layers, each accomplishing a subset of functions. At the present stage of development each sub-layer consists of a passive interconnect backplane, onto which components are either:

- directly patterned (for flexible-compatible components e.g. thin-film solar modules, thin-film active devices) or
- assembled (for non-patternable components e.g. discrete thin-film batteries, integrated circuits).

In order to create a complete system, multiple such sub-layers are combined. A key to integration and modularity is the use of non-contact electrical interfaces between these sub-layers; these interfaces are capacitive or inductive. Such interfaces obviate the need for direct, via-type, metallic

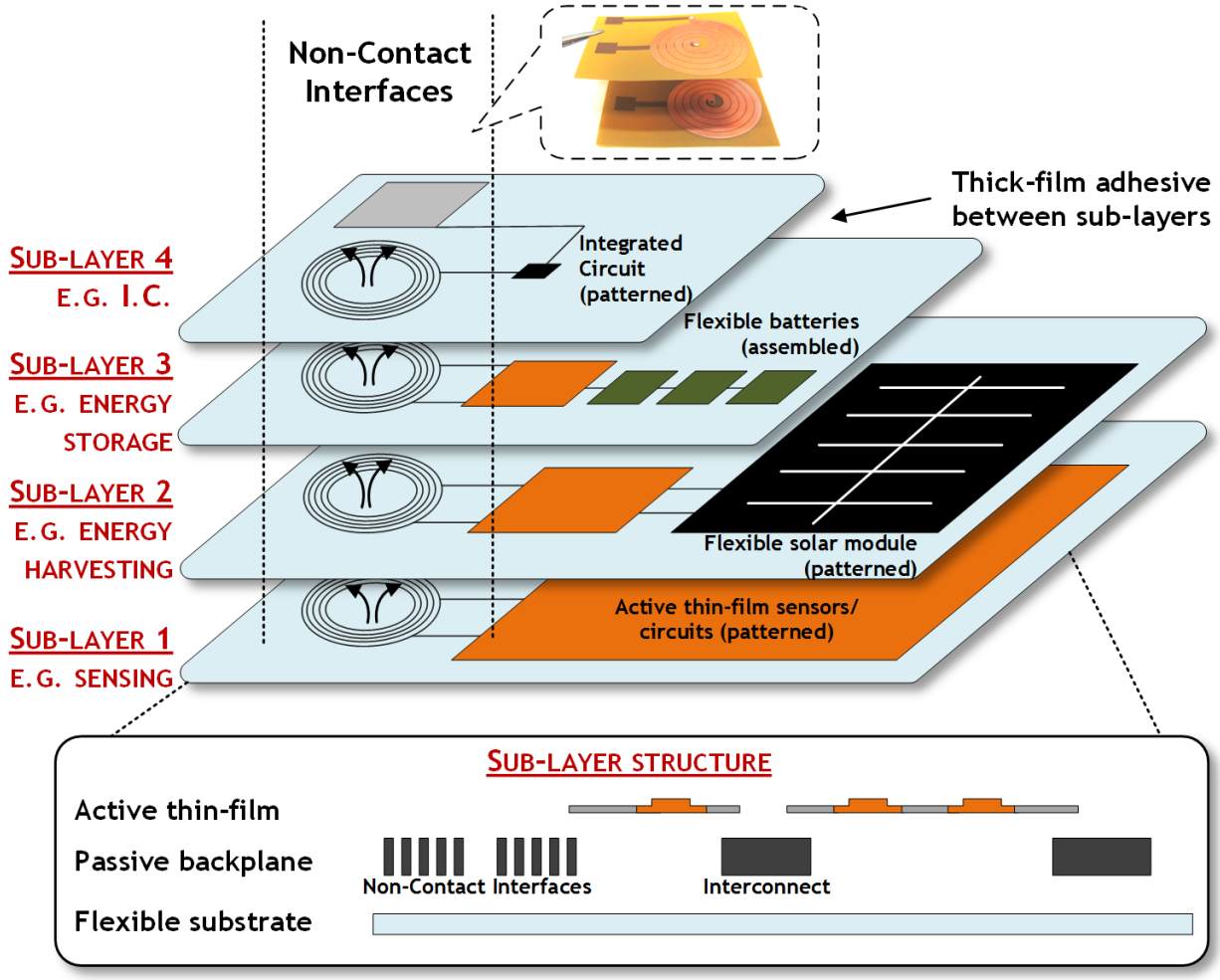


Figure 1.6: Skin-like architecture making use of multiple sub-layers [12]

contacts over large areas, and substantially facilitate sheet-to-sheet alignment. Along with such interfaces, a complementary focus for enabling scalable hybrid systems is architectural design for keeping the number of physical interfaces to a *minimum*.

For the few components that may require Ohmic interfaces, these can be achieved through anisotropic conductive film (ACF), or in the case of CMOS ICs, using chip-on-flex technology [40].

The overall system can then be assembled by applying adhesive to the sub-layer sheets, aligning them, and laminating the whole stack to obtain a complete system.

1.4 Thesis outline

In this thesis, we will demonstrate devices and circuits for hybrid systems that leverage the strengths of both thin-film and CMOS technologies. We will propose solutions for some of the interface challenges relying on device optimization, circuit design and large-scale assembly techniques. In Part I we present an introduction to large-area hybrid systems, the thin-film materials and devices used in this thesis as well as device characterization and modelling techniques for system design. In Part II, we present a number of systems for energy-harvesting and powering over non-contact interfaces for skin-like architectures. In addition, we demonstrate a fully thin-film battery management system for energy storage. In Part III we present a fully thin-film radio-on-plastic that explores the ability to do wireless communication with thin-film circuits. In Part IV we present thin-film interface circuits and devices for a strain-sensing system that perform sensor access and sensor readout. Finally, in Part V we present an image sensing system in which we introduce an algorithmic approach to minimizing interfaces to large-area sensing systems. We demonstrate machine learning techniques that help overcome thin-film defects and variability whilst achieving a high-level function, in this case classification of images. Overall, this thesis demonstrates a large number of components that together are able to be combined modularly to create complete systems.

Part I

Introduction to large-area hybrid systems

Chapter 1

Thin-film materials and devices

The thin-film universe is very rich in material systems which allow the creation of an incredibly diverse set of devices. Some of these technologies are currently in commercial production driven by AMLCD and AMOLED display panels; others are very much the subject of in-depth research. This material richness is very beneficial for the design of systems with rich functionality, but provides us with an enormous palette to choose from. In this chapter we introduce a number of materials and devices that we will use to create our hybrid systems.

1.1 The materials

In this thesis, the principal thin-film semiconducting material used is hydrogenated amorphous silicon (a-Si:H). A well-understood material that has been studied for decades, a-Si has become the mainstream semiconductor used in the commercial production of large, active-matrix displays. Although many of the circuits, topologies and principles that will be described in this thesis are very much transferable across thin-film technologies, a-Si provides us a solid base to explore these (thanks to the a-Si device predictability and reliability). A basic review is now presented of the material properties of a-Si, as well as the properties of the insulator most commonly used in tandem with a-Si: silicon nitride.

1.1.1 Amorphous silicon (a-Si)

Hydrogenated amorphous silicon (a-Si:H) has a structure as shown in Figure 1.1 contrasted with the microstructure of poly-crystalline and crystalline silicon (c-Si).

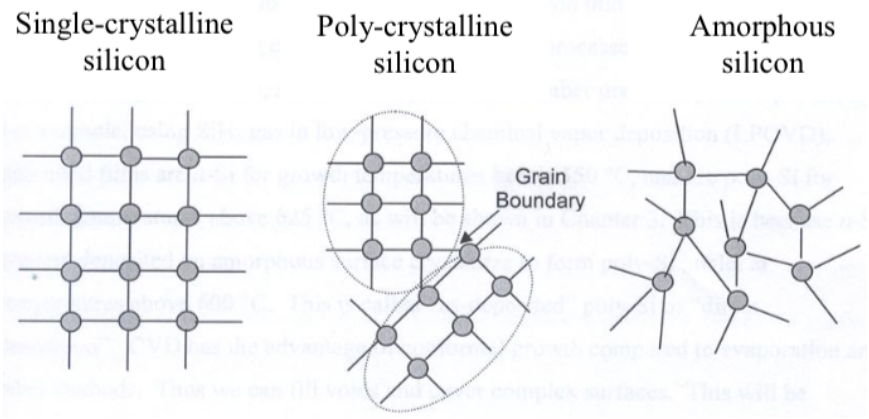


Figure 1.1: Microstructure of a-Si, poly-Si, c-Si (not to scale) [13]

Whereas in c-Si silicon atoms are arrange in a regular, periodic lattice, silicon atoms in a-Si can be found in a considerably disordered arrangement. Whilst the covalent four-fold coordination is mostly maintained, defects are present throughout the material, resulting in occasional missing atoms. The consequence of this is an abundance of dangling bonds throughout the material. The incorporation of hydrogen in the lattice *during deposition processes* to passivate these dangling bonds (as shown in Figure 1.2) was critical for reducing defect levels and was a transformational leap for the usefulness of a-Si as a semiconductor (opening the door for doping, photoconductivity...).

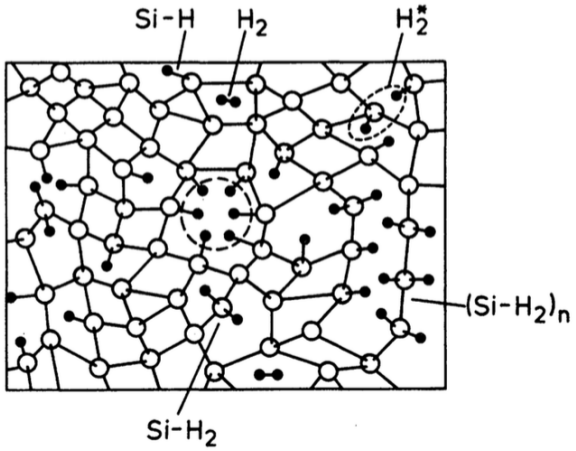


Figure 1.2: Incorporation of hydrogen in a-Si [14]

Amorphous-silicon is not a completely disordered material though and some short range order is maintained. This is because the variation in Si-Si bond lengths and angles deviate only slightly from their equilibrium values (less than 1% and 10% deviations respectively). The lack of long-range order though, has a significant on the electrical properties of a-Si, with the disorder resulting in the presence of significant densities of electronic trap states in the bandgap of the semiconductor. This is shown schematically in Figure 1.3.

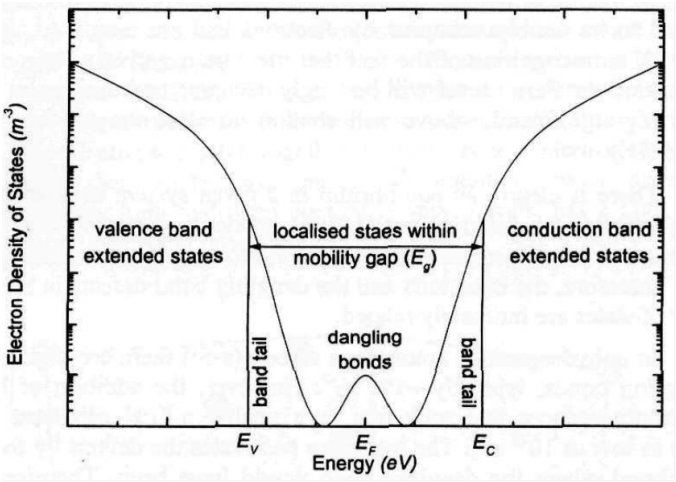


Figure 1.3: Schematic density of states in amorphous semiconductors [15]

In amorphous silicon, the mobility of a free electron is typically around 10-20 cm^2, orders of magnitude lower than its counterpart c-Si where it is typically at least 500 cm^2. Furthermore as shown in Figure 1.3, the fairly sharp band edges of c-Si are replaced by a smooth transition from the extended band states to (1) exponentially decaying localized states close to the band-edges (the 'band tails') and the presence of (2) defect states in the middle of the bandgap. The mobility gap separates the extended states and the localized states, as shown in Figure 1.3.

Electronic transport in a-Si takes places close to these mobility edges, through trapping and detrapping, as well as by hopping between localized states within the energy gap (though the latter is dominant only at low temperatures). This trap-limited transport reduces the effective mobility in the material even further. Further, the valence band tail is wider than the conduction band tail. This results in a significantly lower mobility for holes than for electrons, which makes the formation of p-type transistors basically unviable. The realization of doping in a-Si [45], even with low-efficiency cleared the path for the formation of complete devices. In practice though, doping

is only used to set Fermi levels at device contacts since doping induces a significant drop in bulk mobility as a result of defect creation.

1.1.2 Silicon nitride (SiN_x)

Silicon nitride is one of the most widely used dielectrics in tandem with amorphous silicon as a semiconductor. This is the result of the very good interface properties between the two materials. The deposited silicon nitride is however not stoichiometric (hence the nomenclature SiN_x) and in fact can have a large bulk defect density. Careful optimization of deposition conditions is thus necessary to minimize these and ensure a high dielectric strength for functional devices.

1.1.3 Material growth

Deposition of the materials just described is most commonly performed by Plasma-Enhanced Chemical Vapour Deposition (PECVD). This involves using or DC excitation to add energy to a mixture of source gases, creating a plasma. This aids in the dissociation of the source gases and, most commonly, reaction of the plasma constituents on the surface of substrates, at low temperatures lower than 350 °C. This key benefit of PECVD allows the deposition of materials on a wide range of substrates: glass, plastics, steel, etc. In this thesis, a four-chamber PECVD is used as pictured in Figure 1.4 with dedicated chambers for the deposition (from left to right) of (1) amorphous silicon, (2) doped amorphous silicon and (3) silicon nitride.

Typical base pressures of the PECVD deposition chambers are lower than 1×10^{-6}Torr. The following gases are typically used to deposit the various films:

- Amorphous silicon: SiH_4, H_2
- Doped amorphous silicon: SiH_4, PH_3 (for n-type), B_2H_6 (for p-type)
- Silicon nitride: SiH_4, H_2, NH_3

Typical deposition pressures are between 500mTorr and 1Torr, and temperatures between 150 °C and 350 °C.

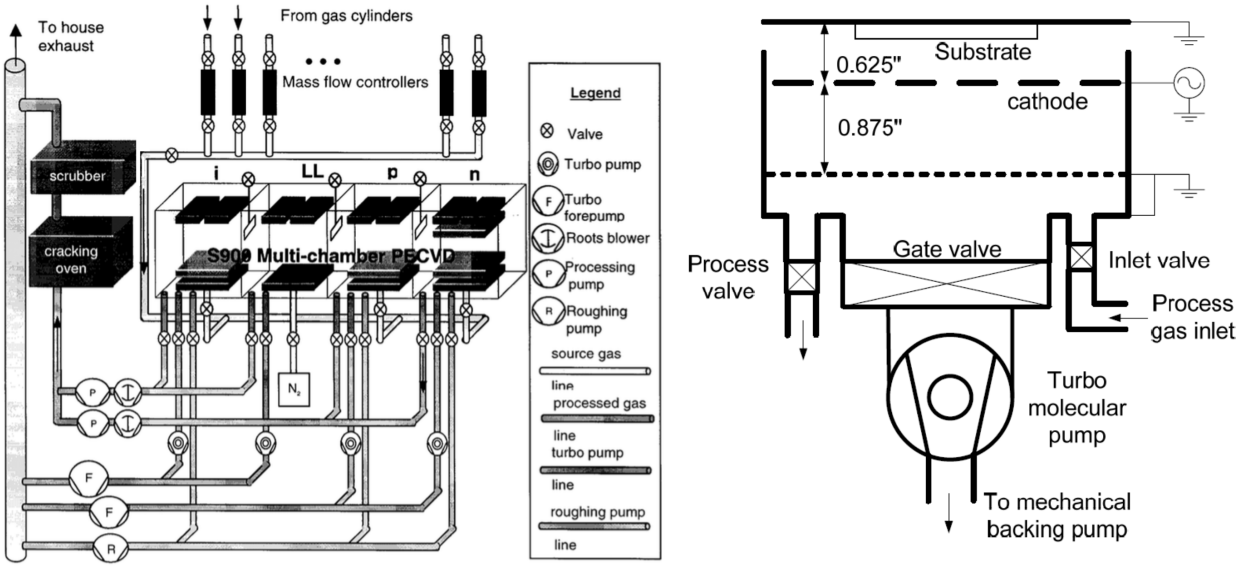


Figure 1.4: Schematic of one of four PECVD chambers at Princeton [16][17]

1.2 The devices

Having described some of the key materials required for the creation of devices, we now present a brief overview of some of the key structures and properties of these devices that will be used in this thesis. In particular we will discuss *Thin-Film Transistors* and *Thin-Film Diodes*.

1.2.1 Thin-Film Transistors (TFTs)

Thin-Film Transistors are a special type of transistor built using thin-films of metals, insulators and semiconductors. These can be fabricated in a range of materials; in this section we first present our core amorphous-silicon TFTs, but also include two other representative technology alternatives for comparison and later discussion.

1.2.1.1 Amorphous silicon TFTs

There are a number of traditional structures for TFTs. The structure of our typical thin-film transistor is shown in Figure 1.5, the so-called blanket passivated, inverted bottom-gate, back-channel etched TFT. This structure has been previously shown to be the most desirable for good electrical performance and simplicity of fabrication (although top-gate structures have recently been

shown approaching the performance of bottom-gate devices, albeit with more complex fabrication processes [17]).

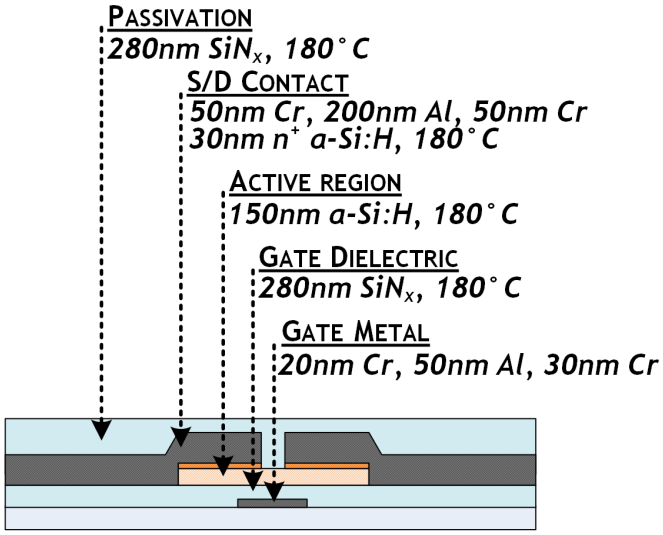


Figure 1.5: Back-channel etched Thin-Film Transistor structure

The a-Si TFT consists of a chrome (or chrome-aluminium-chrome) metal gate (typically 50-100nm), a silicon nitride dielectric (typically 300nm), an undoped amorphous silicon channel semiconductor (typically 150nm), n^+ doped amorphous silicon source and drain contact regions (typically 30nm), metal source/drains (typically 50-300nm) and finally a blanket-deposited film of silicon nitride for passivation (typically 150nm-300nm). All active and insulating layers are deposited between 150 °C and 350 °C. The PECVD layers are all deposited sequentially in a single step for optimal interface control. Further detailed processing steps are given in Appendix A.

In this configuration, the channel length is dictated by the separation between the source and drain contacts. In this work, the channel lengths typically range from 6 to 10 microns. Overlap regions between the source/drain and gate contacts are required in order to ensure low contact resistance, injection of carriers into the channel region and tolerance to accidental misalignment. We optimize these for processing on plastic, and these typically range between 5 to 15 microns. Large overlaps, however, result in larger parasitic capacitances.

A typical current-gate voltage transfer curve for the TFTs is shown in Figure 1.6. Typical electron mobility for these n-type TFTs are between 0.5 and 1cm^2/Vs, with threshold voltages

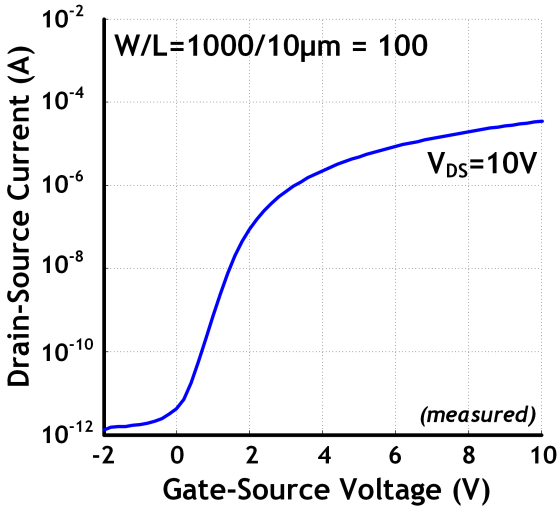


Figure 1.6: Typical a-Si TFT transfer curve

between 1 and 3V. This contrasts strongly with reported p-type TFTs who exhibit 2-3 orders of magnitude lower mobilities [46]. This makes the a-Si ecosystem a *unipolar* one.

1.2.1.2 Organic TFTs

A very wide range of organic transistor technologies have been developed, leveraging small organic molecules, polymers or single crystalline organic films. An attraction of organic TFTs (OTFTs) is the range of fabrication techniques available ranging from vacuum evaporation to direct printing at room temperatures.

In general, organic TFTs have similar structures to their a-Si counterparts with bottom-gate TFTs typically showing better electrical performance. Mobilities exhibited by organic transistors span several orders of magnitudes, with some of the best TFTs showing *hole* mobilities slightly above those of a-Si. Much research is in progress to create air-stable n-type OTFTs to match the performance of standard p-type OTFTs, though this is still an open field currently.

In this thesis we will focus, as a representative example, on one particular OTFT technology developed at the University of Tokyo which has shown excellent air-stability and good electrical performance. The structure of this OTFT is shown in Figure 1.7.

The bottom-gate organic TFT consists of a gold metal gate (typically 50nm), a Parylene-C dielectric (typically 100nm), a dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) active layer

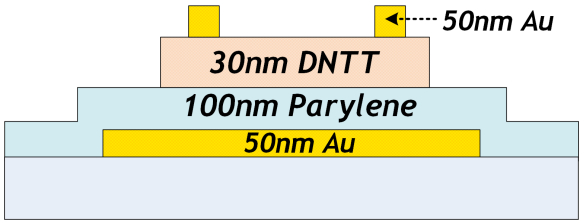


Figure 1.7: Bottom-gate Organic TFTs

(typically 30nm) and finally gold source/drain contacts (typically 50nm). A typical current-gate voltage transfer curve for the TFTs is shown in Figure 1.8.

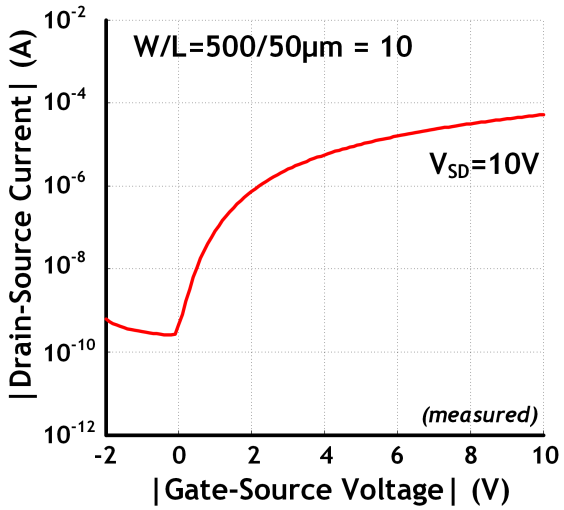


Figure 1.8: Typical DNTT organic TFT transfer curve

Typical hole mobility for these p-type TFTs is approximately 1cm^2/Vs. One key challenge with this particular organic technology is the fact that short channel lengths are difficult to realize since this process uses shadow masking to define the source/drain regions (this is because of the sensitivity of the organic layer to typical solvents used in photolithographic patterning).

1.2.1.3 Metal oxide TFTs

Metal oxide-based thin-film transistors (ZnO, IGZO...) seem very promising for large-area systems, and are beginning to appear commercially got display backplanes (e.g. Sharp recently established a Gen-8 [47] Indium-Gallium-Zinc-Oxide plant [18]). These devices show several attractive electrical properties: high mobility (at least 10-20x that of amorphous silicon), low leakage, wide bandgap (and hence transparency), stability and the ability to be deposited in an amorphous film. All of

these features are likely to enable systems that have lower power consumption with high device uniformity and lifetime.

In this thesis, the representative n-type metal oxide technology we demonstrate is PEALD (Plasma-Enhanced Atomic Layer Deposition) Zinc Oxide (ZnO) based TFTs, fabricated in-house [48]. The structure of this TFT is shown in Figure 1.9.

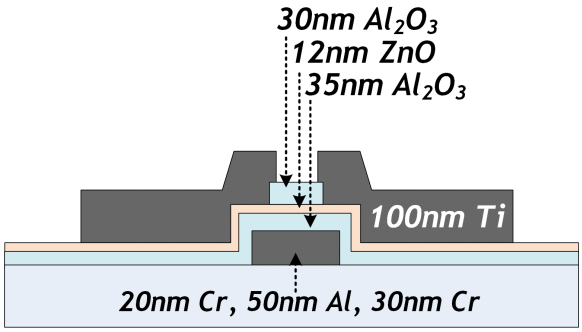


Figure 1.9: Bottom-gate zinc oxide TFTs

The bottom-gate ZnO TFT consists of a chrome (or chrome-aluminium-chrome) metal gate (typically 50-100nm), a PEALD Aluminium Oxide dielectric (typically 35nm), a ZnO active layer (typically 12nm) and finally titanium source/drain contacts (typically 100nm). A typical current-gate voltage transfer curve for the TFTs is shown in Figure 1.10.

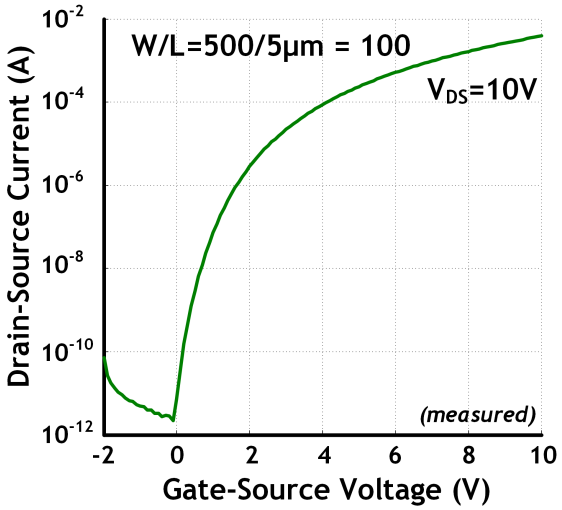


Figure 1.10: Typical zinc oxide TFT transfer curve

Typical electron mobility is between 15-20cm^2/Vs, resulting in significantly higher transconductances when compared with amorphous silicon. Two key challenges of this ZnO technology though

are the approximately 10× higher dielectric capacitance (with respect to AC properties) and the limited voltage scalability as a result of the thin oxide dielectric.

1.2.1.4 TFT summary

In this section we have looked at a number of TFT technologies (and omitted many other viable contenders such as LTPS). Figure 1.11 summarizes the mobility attributes of a number of transistor technologies as a function of processing temperature, and it is clear that whilst TFTs offer the great benefits of large-area scalability, a price is paid in terms of electrical performance.

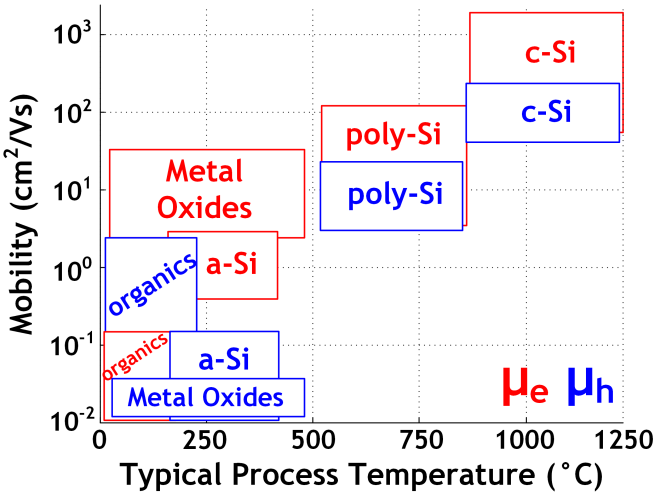


Figure 1.11: Mobility versus process temperature

Figure 1.12 shows an interesting survey of TFT backplane technologies [18] from a technology forecast, illustrating that no key player has yet been decided for the future of TFT technology.

Nevertheless, in this thesis we will demonstrate that despite their modest electrical performances, TFTs will form critical components of hybrid systems.

1.2.2 Thin-Film Diodes (TFDs)

The second key device that we will make use of in this thesis are thin-film diodes (TFDs), in particular two types:

- Amorphous silicon Schottky diodes
- Nano-crystalline silicon Schottky diodes

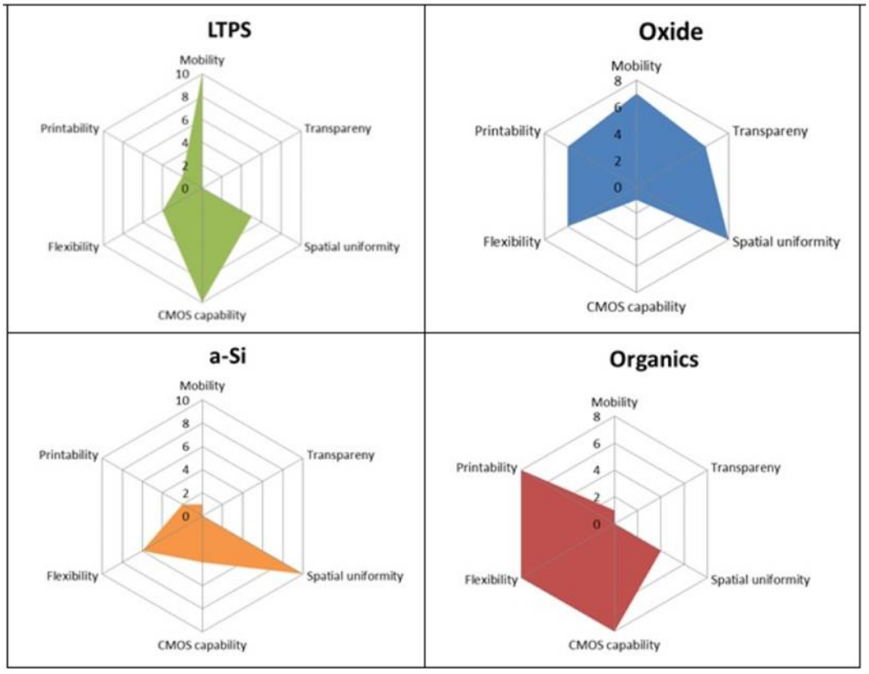


Figure 1.12: Comparison of backplane technologies [18]

We will see that these play a critical role as rectifying units. Schottky diodes are used instead of p-i-n diodes due to their lower forward voltage drop and simpler fabrication, avoiding the use of p-type thin-film silicon which is not part of a standard a-Si process as used in production of TFT AMLCD technologies. These diodes, where used, are fabricated separately and mounted onto the flexible sheet.

1.2.2.1 Amorphous silicon Schottky diodes

The structure of the designed amorphous silicon Schottky diodes is shown in Figure 1.13 along with measured I-V and C-V curves.

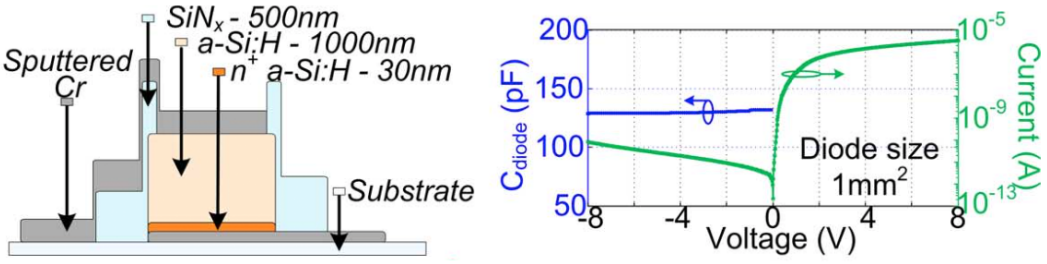


Figure 1.13: a-Si:H Schottky TFD structure and measured I-V and C-V curves [19]

To minimize the voltage drop of the diodes, thin-film a-Si:H Schottky-barrier diodes are developed, processed at 180 °C. Though thin-film diodes (TFDs) have been reported, the Schottky-barrier TFDs enable low voltage drop and give very good rectification characteristics, with a current of just under 1mA/cm^2 at 1V forward bias (reducing the thickness of the diode to 200nm can increase this to 100mA/cm^2). A key challenge, however, is their parasitic capacitance, which, due to AC conduction, would limit the demodulation of high input frequencies. For a 1 mm^2 area diode, this capacitance is approximately 130pF.

1.2.2.2 Nano-crystalline silicon Schottky diodes

Nanocrystalline-silicon (nc-Si) Schottky-barrier diodes are also developed in our lab [20]. These are also processed at 180 °C, as shown in Figure 1.14, and give over 1000× higher current density than our a-Si diodes, thereby enabling smaller structures for reduced capacitance. 0.09 mm^2 diodes are typically used giving a capacitance of approximately 35pF.

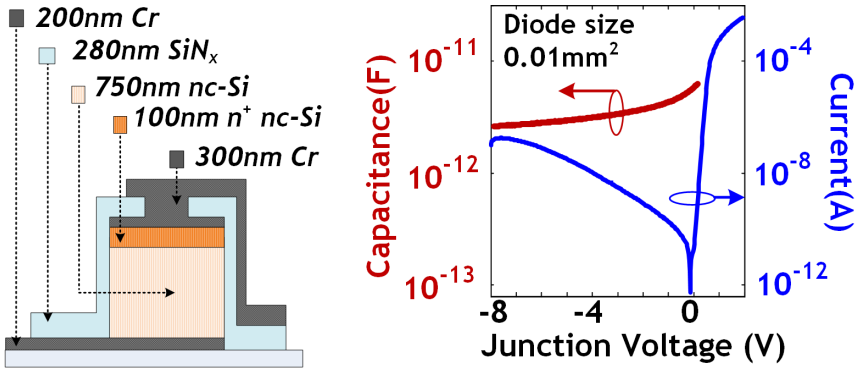


Figure 1.14: nc-Si Schottky TFD structure and measured I-V and C-V curves [20]

Chapter 2

Device characterization and modelling of TFTs for system design

Having identified the key devices that will be leveraged in this thesis, we now turn to a study of a number of metrics related to the electrical performance of TFTs. In particular, we look at DC, AC and noise characteristics of the transistors, since these are critical to their operation in large-area systems. In this chapter, we also present SPICE simulation models for our TFTs.

2.1 Electrical performance - DC

As a result of the large defect densities in thin-film materials, TFTs are not operated in depletion mode, but in *accumulation* mode. In accumulation, majority carriers are attracted to e.g. the a-Si/SiN_x interface forming a conductive channel. With a drain-source voltage applied, electrons drift through the channel. In the off-state, source-drain leakage is determined by the flat-band conductance of the amorphous silicon layer or conduction in a spurious back-channel.

In practice, TFTs can be modelled in a manner very similar to conventional CMOS transistors, in both saturation ($V_{DS} > V_{GS} - V_T$) and linear ($V_{DS} < V_{GS} - V_T$) regimes as described by:

$$I_{DS,linear} = \frac{\mu C_i W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$$

$$I_{DS,saturation} = \frac{\mu C_i W}{2L}(V_{GS} - V_T)^2$$

where C_i is the specific dielectric capacitance ($\epsilon_{SiN_x}/t_{SiN_x}$), W is the TFT width, L is the TFT channel length, μ is the field-effect mobility and V_T is the threshold voltage of the transistor. For silicon nitride, ϵ_{SiN_x} is approximately 7.5.

TFT DC performance is typically evaluated through *transfer* (I_{DS} vs V_{GS}) and *output* (I_{DS} vs V_{DS}) curves. Unless otherwise specified, the transfer curves presented in this thesis are measured at two drain-source voltages: 0.1V and 10V. Mobility and threshold voltage parameters quoted in this thesis are typically extracted in saturation from a $\sqrt{I_{DS}}$ vs V_{GS} curve.

Another device parameter that will be used frequently in this thesis is the TFT transconductance, g_m. This is defined as, in saturation:

$$g_m = \left.\frac{dI_{DS}}{dV_{GS}}\right|_{V_{DS}=constant} = \frac{\mu C_i W}{L}(V_{GS} - V_T)$$

and finally we also define the TFT output resistance r_0:

$$r_0 = \left.\frac{dI_{DS}}{dV_{DS}}\right|_{V_{GS}=constant}$$

In TFTs, the output resistances are typically on the order of 100s of kiloohms, whilst the transconductances are modest, on the order of 10 µS to 1 mS.

2.2 Electrical performance - AC

Many systems we will demonstrate in this thesis do not operate at DC, but instead require low to high frequency operation of the TFTs. The AC behaviour of the TFTs is determined by the capacitances associated with the device. As shown in Figure 2.1 these include the gate-channel dielectric capacitance itself, but also the parasitic source/drain to gate overlap capacitances.

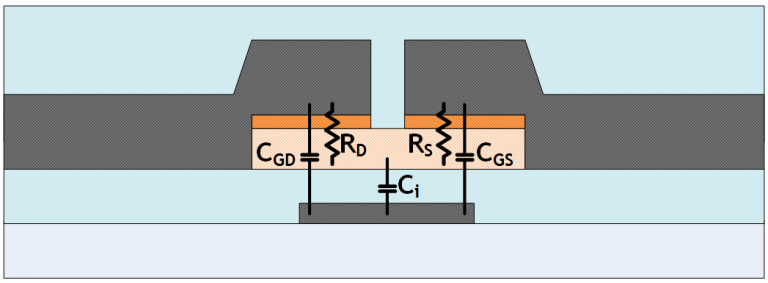


Figure 2.1: Key transistor parasitics

In this section, we explain why these parasitics are large and then present a key quantity, the TFT **cutoff frequency**, f_t.

2.2.1 Limits of optimizing overlap capacitance on plastic

Figure 2.2 shows a micrograph, highlighting the physical TFT features.

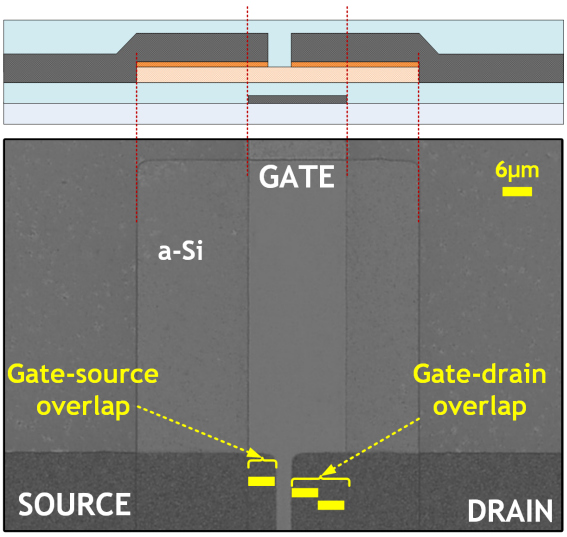


Figure 2.2: TFT source/drain-gate overlaps on polyimide [21]. Top: schematic cross-section, bottom: top-view micrograph

The necessity for large overlaps arises in particular for circuits processed on free-standing plastic (i.e. not bonded) due to substrate expansion/contraction during processing as well as built-in stresses of device films [5]. This results in a lower limit to gate-source/-drain overlap to maintain reliable alignment between mask stages during lithography, as illustrated in Figure 2.3.

Both the minimum gate length (L=6 µm) and the overlaps (x_{ov}=5-15 µm) in our process are chosen based on characterization of devices deposited at 180 °C in order to achieve high circuit yield on foil, over an area of approximately 60 cm^2. Note, while equal gate-source/drain (S/D) overlaps are nominally designed, the actual overlaps at our shown limit are unbalanced.

Figure 2.4 shows the overlap variation for TFTs affected by stresses and thermal expansion at a distance from the sample center (nominal x_{ov}=10 µm; positive variation indicates larger overlap). The sign of source- vs drain- overlap deviation depends on direction traversed from the center of the sample.

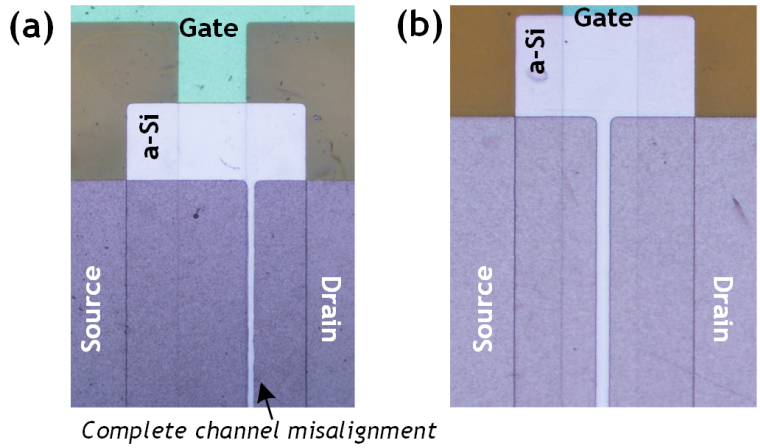


Figure 2.3: High temperature processing of silicon nitride at (a) 250 °C and (b) 140 °C on free-standing plastic. The higher temperature results in alignment challenges [22]. Micrographs taken at the same location on a 3x3in sample, near one of the edges

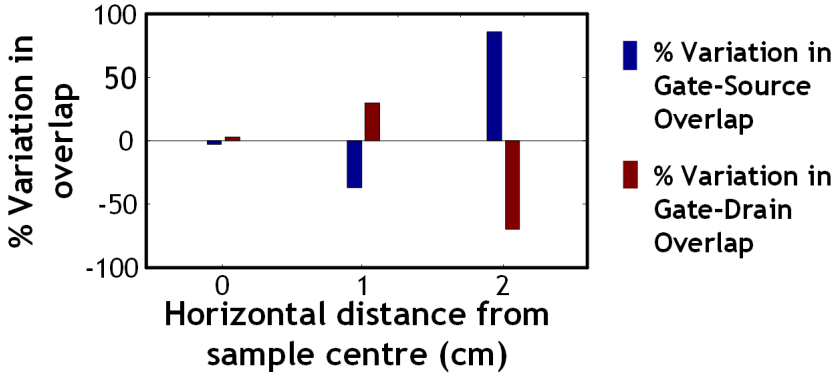


Figure 2.4: Source and Drain overlap variation across a sample due to substrate deformation, as a percentage variation compared to overlaps at the centre of a sample [21]

2.2.2 The cutoff frequency, f_t

The cutoff frequency, f_t, is an indicator of the intrinsic speed of a transistor, defined as the frequency at which the current gain (A_I) of the transistor has fallen to unity.

$$A_I = \frac{i_{out}(\omega)}{i_{in}(\omega)}\bigg|_{f_t} = 1$$

where ω is equal to the frequency of operation multiplied by a constant $2 \times \pi$. This frequency is in large part affected by the TFTs' entire input capacitance as we shall see in more detail. The chart in Figure 2.5 illustrates typical cutoff frequencies for a range of different technologies, thin-

film organic, silicon and metal oxides as well as thin-film polysilicon and 10s of nm CMOS; we can see that typical cutoff frequencies for thin-film amorphous silicon devices are around 1MHz.

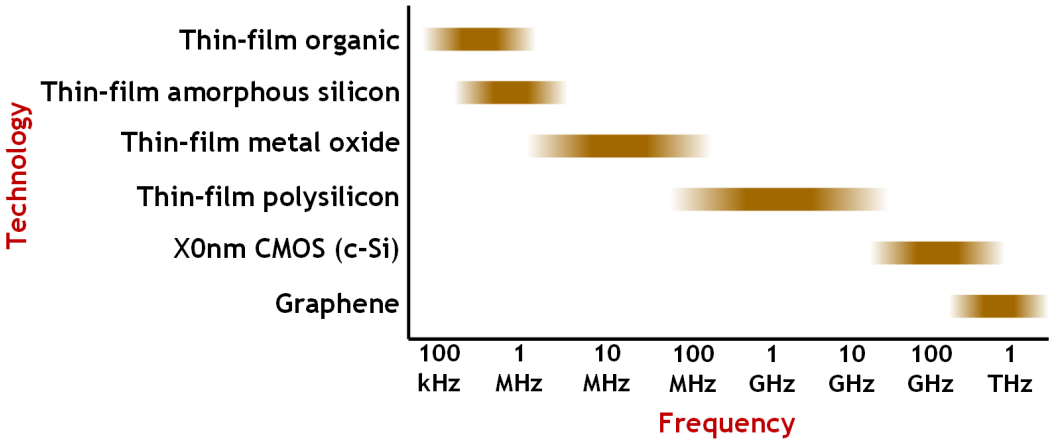


Figure 2.5: Cutoff frequencies in a range of different technologies

In order to derive an analytical expression for this cutoff frequency, we can consider the small signal model of the transistor shown in Figure 2.6, including notable parasitics such as the gate capacitances.

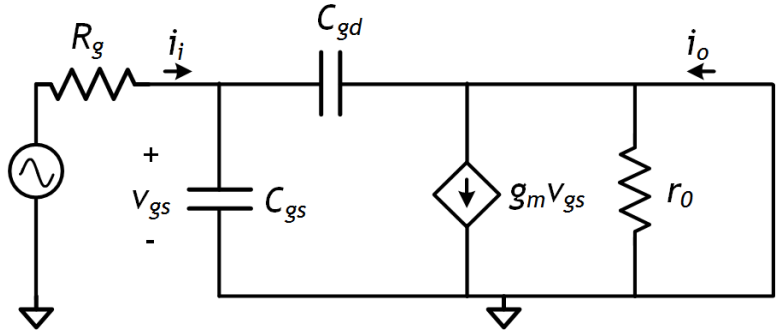


Figure 2.6: Small signal model for a TFT showing gate capacitance parasitics

Under the (initial) assumption that the magnitude of the transconductance (g_m) is greater than the quantity $2\pi \times f \times C_{gd}$ (frequency of operation x gate-drain capacitance), we can analyze expressions for input and output currents such that:

$$A_I = \frac{i_{out}}{i_{in}} = \frac{g_m - sC_{gd}}{s(C_{gs} + C_{gd})} \approx \frac{g_m}{s(C_{gs} + C_{gd})}$$

where $s = j2\pi \times f$. Subsequently, we can state that the frequency where the current gain is 1 corresponds to:

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

This shows a dependence on the transistor transconductance as well as the total gate capacitance. For thin-film technologies, the cutoff frequency is modest because of low transconductance but large parasitic capacitances as described previously. Plotting A_I vs frequency results in a curve with a slope of -20dB/decade, with the unity gain frequency (f_t) occurring when A_I=0 dB.

2.2.3 Measuring the cutoff frequency

Current gain A_I is measured from the two-port-network parameter H_{21} on TFTs biased in saturation, with a calibrated ENA5061B vector network analyzer (VNA). The measurement setup is shown in Figure 2.7.

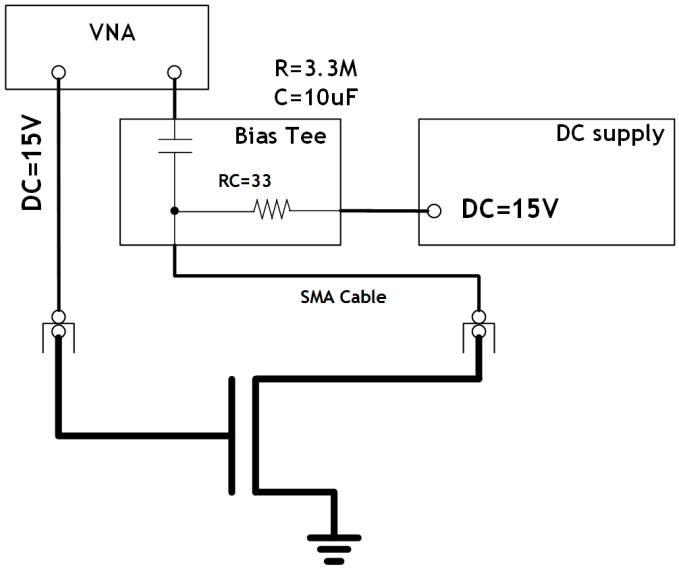


Figure 2.7: Cutoff Frequency Measurement Setup. Connections from SMA cables to the TFT are formed using either an SMA-BNC adapter or a BNC to alligator clip connection or a soldered connection to contact pads on the TFT sample. An improved connection can be formed with an SMA to N-type connector, with a wire soldered from the N-type connector to the TFT. In general, these configurations can add between 1-10pF of capacitance to ground, which it is important to minimize when measuring the cutoff frequency

Details on the 1-port calibration can be found in Appendix E. The current gain is computed mathematically by the VNA (in equation mode) using the formula:

$$A_I = H_{21} = \left| \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \right|$$

A typical measurement of the current gain vs frequency is shown in Figure 2.8.

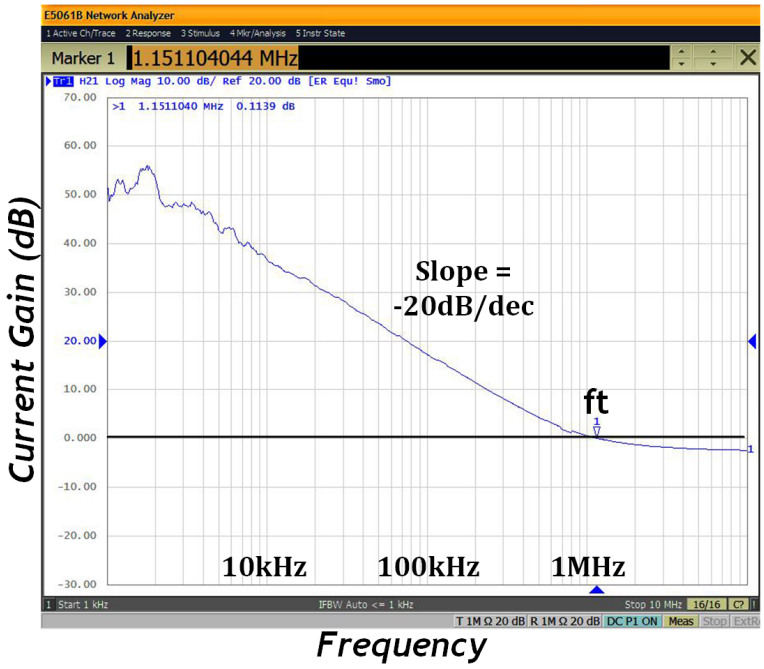


Figure 2.8: Typical cutoff-frequency measurement

As described earlier, at low frequencies, the slope can be expected to be 20dB per decade of frequency which is what is shown in the measurement. The cutoff frequency is defined where this curve crosses unity gain, or 0dB, for this device shown to be around 1.1MHz.

We can simplify the current gain expression derived earlier into its constituent physical parameters to get insight into the factors affecting the cutoff frequency:

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{\mu(V_{GS} - V_T)}{2\pi L(L + 2x_{ov})}$$

As can be seen, f_t to first order depends on material properties such as mobility, external parameters such as applied gate voltage, and geometric factors such as channel length and source/drain to gate overlaps (x_{ov}). The graph in Figure 2.9 confirms the effect of overdrive voltage, with the measured cutoff frequency linearly dependent on it.

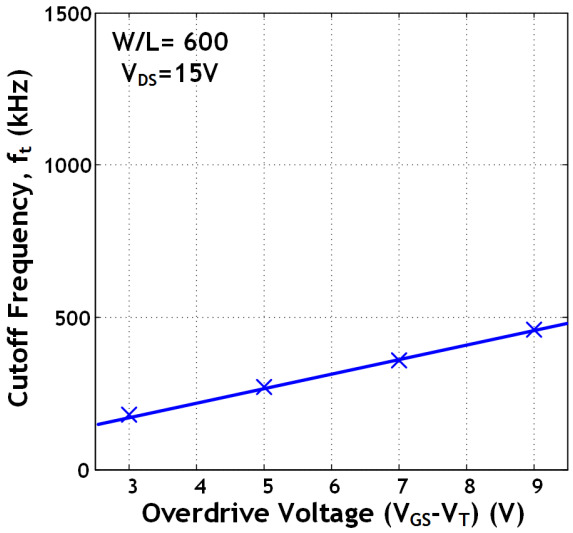


Figure 2.9: Cutoff frequency dependence on overdrive voltage

2.2.4 Cutoff-frequency for self-aligned TFTs

Our standard amorphous silicon technology has large source/drain-gate overlaps which lower the device f_t. In order to improve this, we can adopt a technique to reduce the source/drain overlaps by self-aligning them to the gate of the TFT [23]. Details are shown in Figure 2.10.

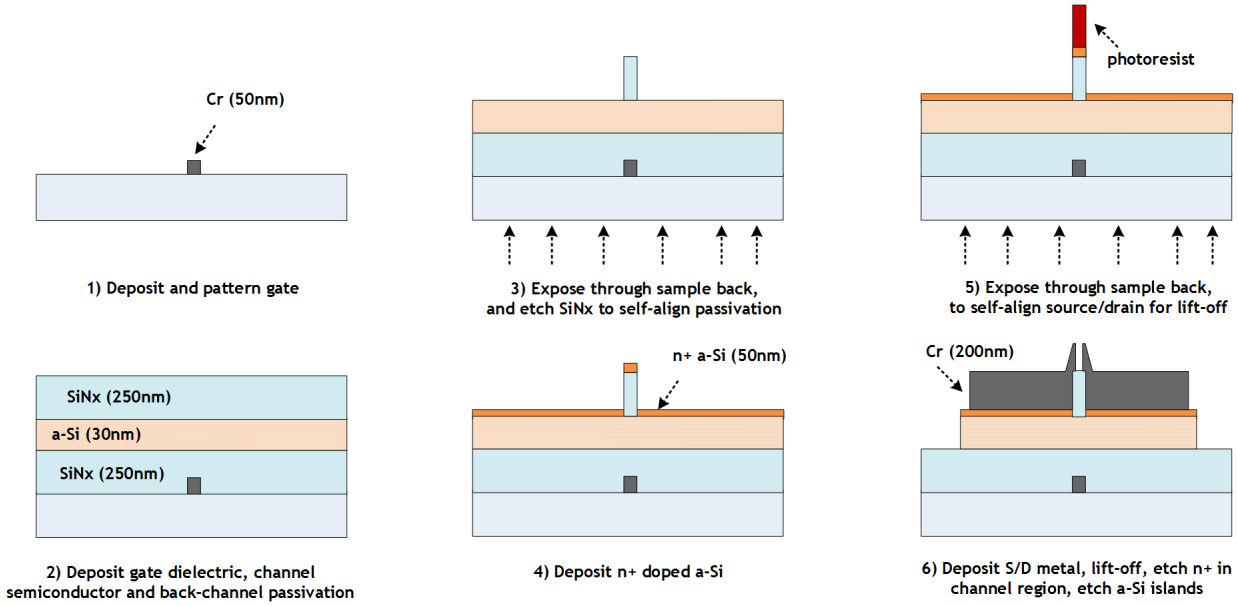


Figure 2.10: Fabrication steps for self-aligned thin-film transistors

The self-alignment is achieved by performing lithography through back-side UV exposure using the procedure described in Appendix A. Complete self-alignment is not possible as this would result in an unacceptably high contact resistance at the source and drain of the TFT. A minimal overlap for injection of carriers is thus created, through the use of angled exposure as shown in Figure 2.11 [23].

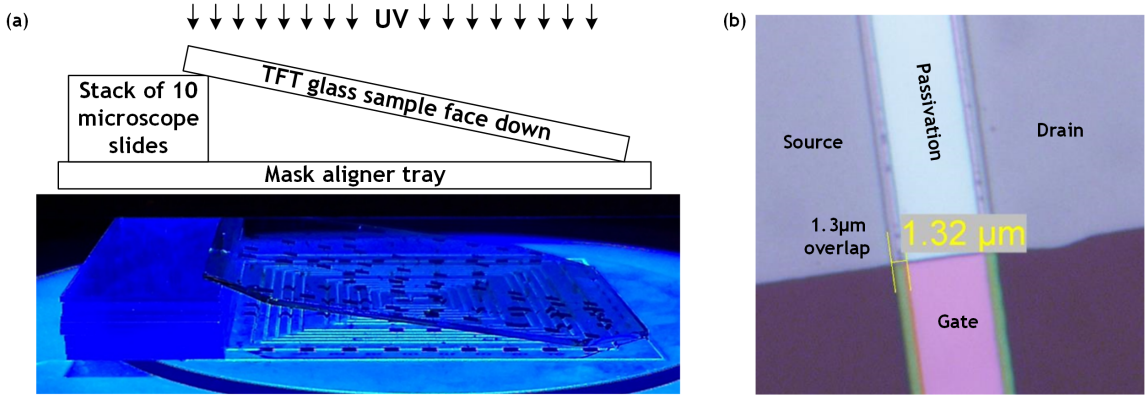


Figure 2.11: Self-aligned TFTs: (a) Use of angled exposure as described in [23] (b) micrograph of self-aligned TFT

Typical overlap capacitances are reduced substantially from 9pF to approximately 1.6pF as compared with our standard 15 µm overlap technology, due to the fact that the overlaps are now approximately 1 µm as shown in the TFT micrograph.

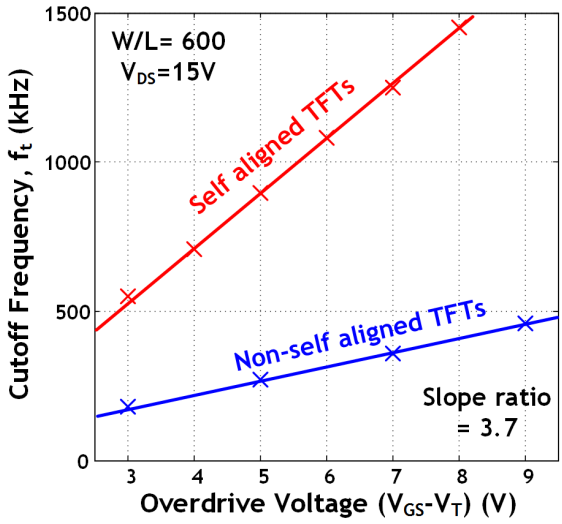


Figure 2.12: Cutoff frequency dependence on overdrive voltage for self-aligned TFTs

Figure 2.12 shows that the f_t of these devices also scales linearly with applied voltage. The ratio in the slope of the two sets of measurements (3.5) corresponds to the expected change in f_t due to the reduced x_{ov} term in the denominator of the f_t expression.

2.2.5 Current-gain behavior above cutoff frequency

Returning to Figure 2.8, we note that around the cutoff frequency, however, an interesting phenomenon is observed, where the current gain begins to flatten. To explain this, we need to consider some of the initial assumptions we made. One that turns out to be critical is that in arriving at a simple expression we neglected the sC_{gd} term. Computing this term however, we notice that around the frequencies of interest (i.e. roughly 1 MHz), its magnitude (6×10^{-5} S) is actually comparable to that of the device transconductance (7×10^{-5} S). This in essence causes a frequency dependent term in the numerator of the current gain expression which pulls up the current-gain curve (a zero), in this case, at frequencies around f_t.

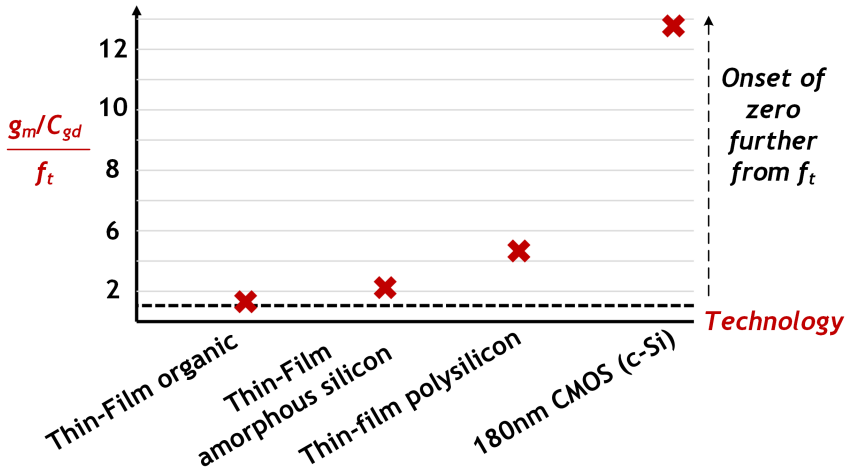
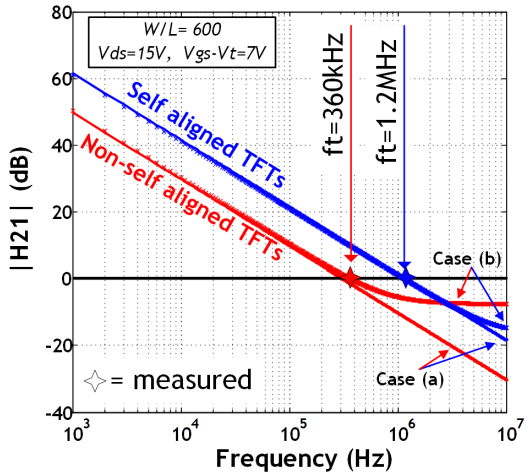


Figure 2.13: f_t normalized ratio of g_m to sC_{gd} indicates why the observed zero is observable only in thin-film technologies

This is observable in thin-film technologies and not noted in others, as in polysilicon or crystalline transistors device geometries result in the frequency at which this roll off occurs being further and further away from f_t, and can therefore be neglected in estimating transistor cutoff frequency. For thin-film technologies, as illustrated in Figure 2.13, this ratio is close to 1.



Case (a) $g_m >> \omega C_{gd}$

$$\left|\frac{\mu(V_{gs}-V_t)}{j\omega L(L+2x_{ov})}\right|=1$$

Case (b) $g_m \approx \omega C_{gd}$

$$\left|\frac{\mu(V_{gs}-V_t)-j\omega L x_{ov}}{j\omega L(L+2x_{ov})}\right|=1$$

Figure 2.14: Analytical modeling of the effect of the zero on the TFT current gain

Figure 2.14 summarizes the two models for f_t for the case of self-aligned and non self-aligned TFTs. In case (a), we ignore the contribution of C_{gd}, and roll-off continues linearly at 20dB per decade. For case (b) we observe the roll-off due to C_{gd}. Two further things are interesting to note: firstly, the roll-off actually increases the f_t for non self-aligned devices *slightly* and secondly, for self-aligned TFTs, the smaller C_{gd} results in the onset of roll-off shifting higher in frequency. How this roll-of impacts circuit performance is still under investigation, however other metrics like f_{max} that dictate, say, the maximum oscillation frequency of the thin-film transistors in our circuits bear close resemblance to the f_t metric, so it is expected that an impact may be noted.

2.2.6 Initial development of stepper TFTs

Since f_t is intimately dependent on the gate capacitance of the TFT, scaling of the channel lengths and overlaps of the transistors is beneficial. In order to push the limits of these, we have started the development of very short channel devices ($\leq$300nm) using a Canon FPA-3000i4 i-line optical stepper, as pictured in Figure 2.15. The stepper exposes a sample through complex optics to shrink exposed patterns on a mask by 5 times and then repeats the pattern multiple times on a single wafer. Fully-automated alignment is performed for both the mask alignment to the optics of the system, and for wafer alignment.

Figure 2.15: Canon FPA-3000i4 Optical stepper

The machine takes as substrate TFTs which are fabricated on 4 inch ultra-flat silicon substrates [1]. The mask pattern used is shown in Figure 2.16, using standard TFT structures with varying channel lengths (300nm to 10μm) and overlaps (300nm to 15μm). The patterns on the mask are designed at 5 times the dimension desired on wafer.

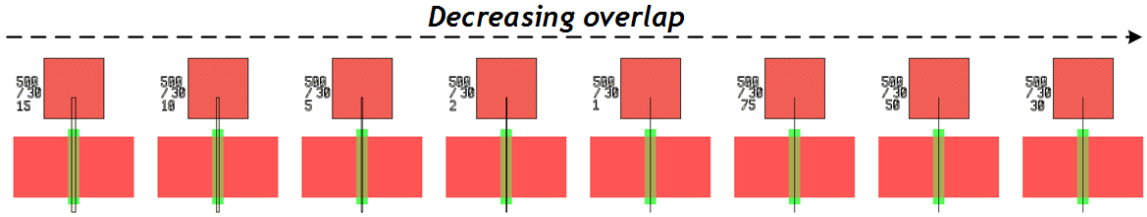


Figure 2.16: Mask layout for stepper TFTs; this pattern is repeated with channel lengths from 300nm to 10 µm

Special alignment marks are required for the auto-alignment process. These are pictured in Figure 2.17, along with the required positioning of the alignment marks. The FRA marks are used for alignment of the mask (reticle) to the optics whilst the AGA/TVPA marks are used for alignment of the mask to the wafer on the stepper stage. Masks for the stepper require high precision and were thus fabricated using a Heidelberg DWL66 4mm write head, on Quartz masks

[1]Nova Electronic Materials: p/Bo < 100 > 1-10 ohm-cm, 500-550μm thick, SSP Prime Grade Si wafers with 2 semi-std flats (Item STF8414-2)

which contract and expand by smaller amounts than soda-lime glass masks under temperature changes[2].

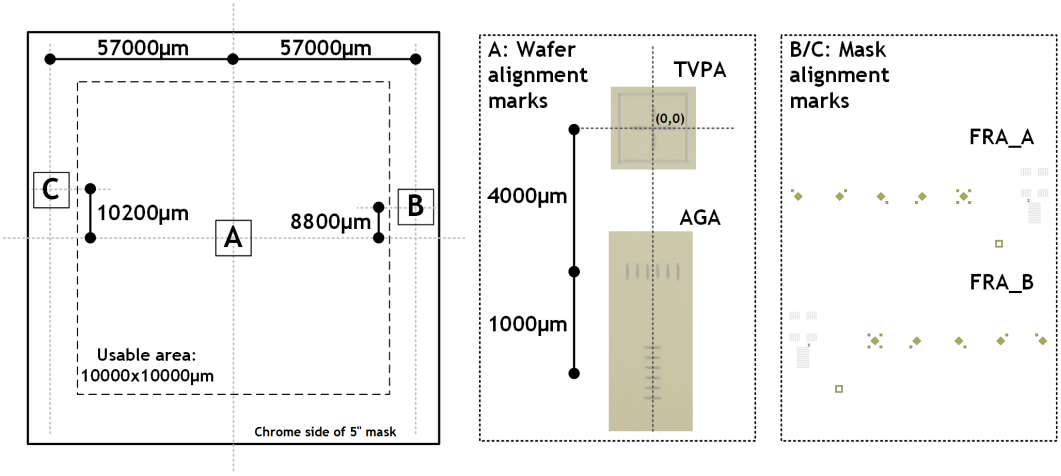


Figure 2.17: Stepper alignment marks; dimensions are 'on-mask' dimensions

A standard fabrication process is performed on a silicon substrate (passivated with 150nm PECVD silicon nitride), described in Appendix A, except with a different resist coating procedure (HDMS vapor prime followed by AZ701) and a procedure for removal of edge bead from the edge of the wafer. It is worth noting that for automatic alignment, the stepper is able to register the alignment marks on the bottom (gate) metal layer through 300nm of silicon nitride and 150nm of amorphous silicon. Completed devices are shown in Figure 2.18.

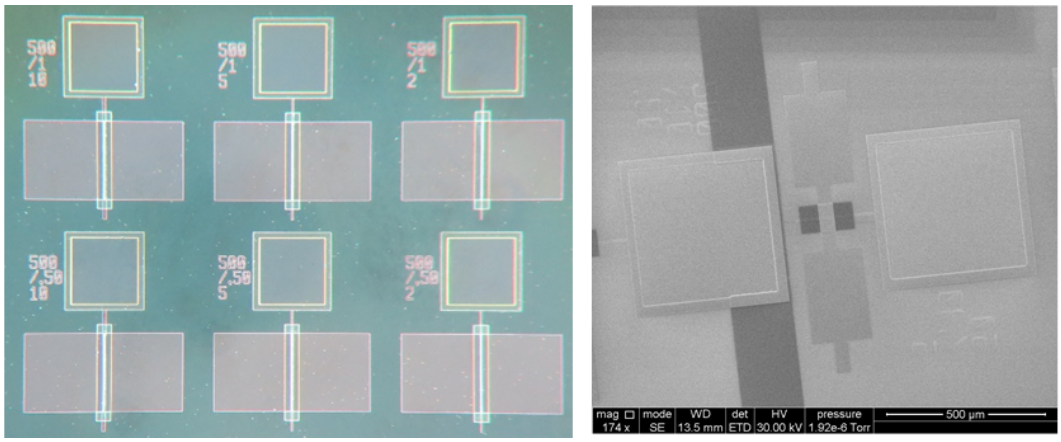


Figure 2.18: Fabricated stepper TFTs on silicon (SEM and micrograph)

[2]Nanofilm: 5X5X.090 QZ LRC 2M 1518 5K, Quartz 5" masks with optical density 2.8, 5300A resist thickness (1518), 12% reflectivity

The fabricated devices with channel length 10 µm and x_{ov} of 15 µm are comparable to the ones we fabricate on glass as shown in Figure 2.19, with a mobility of 0.55cm^2/Vs and a threshold voltage of 1.9V.

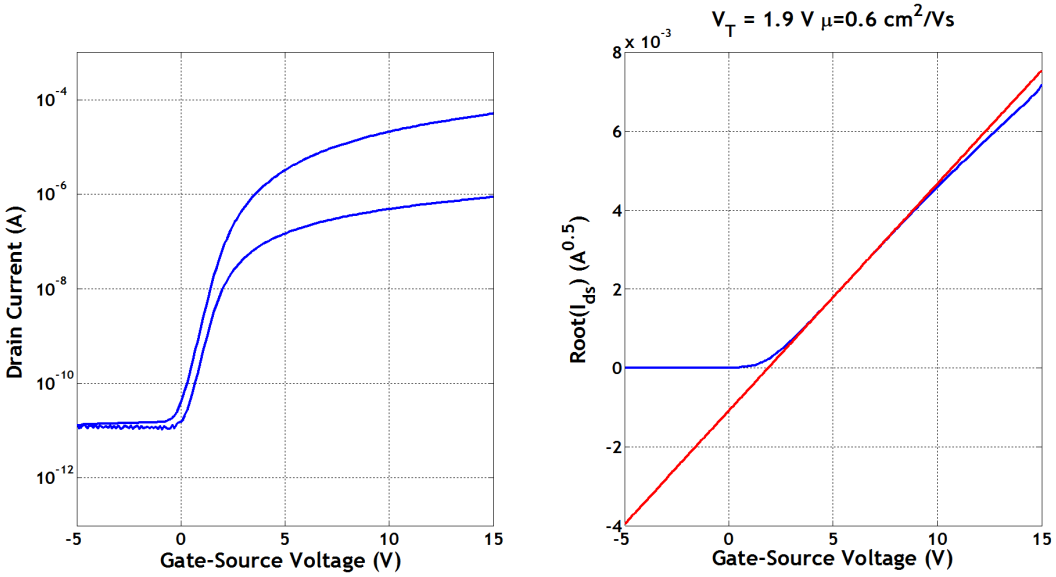


Figure 2.19: Stepper TFTs with 15 µm overlap, L=10 µm and W= 500 µm

Figure 2.20 illustrates the transfer curves for devices with progressively shorter channel lengths. As can be seen by the lack of scaling of on-current at shorter L dimensions, source/drain contact resistances begins to have a significant impact. In addition, high off-conductance can be observed for progressively shorter channels.

In order to determine the magnitude of this contact resistance, a transmission-line analysis measurement is performed as shown in Figure 2.21, plotting the normalized effective channel resistance (in the linear regime) vs the device channel length. The value obtained at L=0 µm corresponds to the sum of the contact resistances at the source and drain contacts, and is extracted to be 12.5 kΩ per contact for a source-drain overlap of 15 µm and a TFT width of 500 µm.

Of course, in practice this contact resistance shows a dependence related to the TFT gate voltage as shown in Figure 2.22. Contact resistance is likely to be caused by the thick intrinsic amorphous silicon layer used (150nm), which in future work should be reduced. This thinner channel material will require careful characterization of the doped amorphous silicon back-channel etching process.

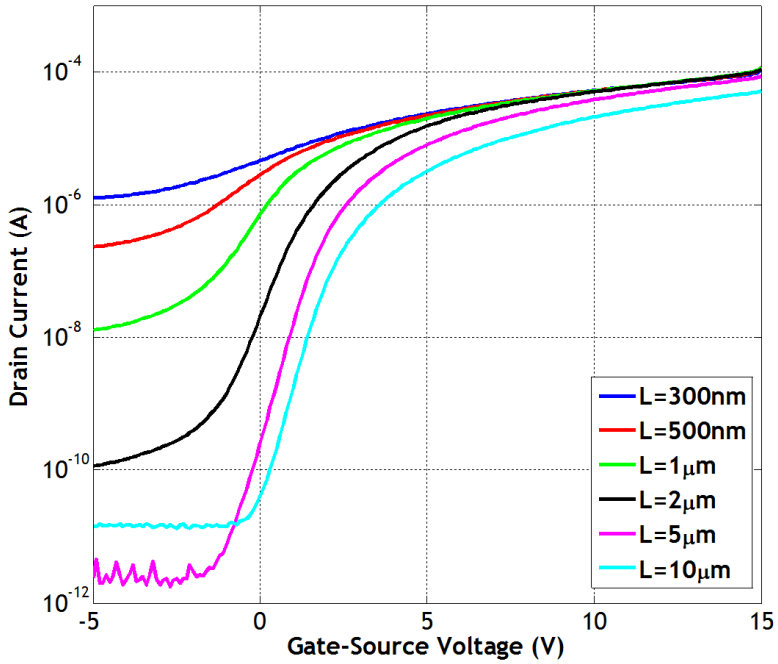


Figure 2.20: Stepper TFTs with L from 300 nm to 10 µm, at V_{DS}=10V

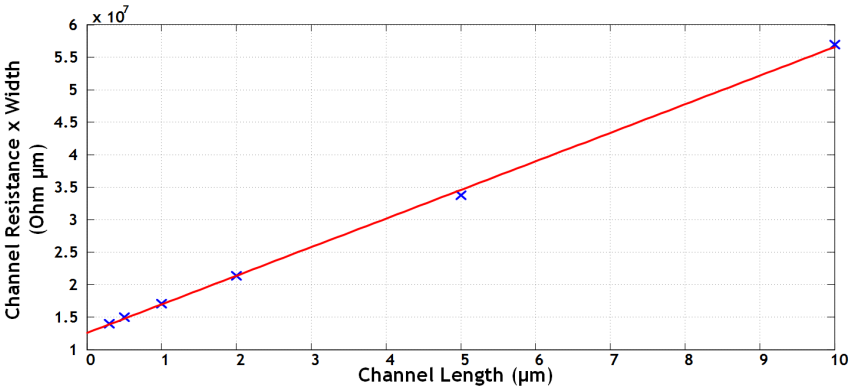


Figure 2.21: Contact resistance measurement for stepper TFTs

Since these devices were not fabricated on an insulating substrate, measurement of f_t was at this stage not feasible. However, in order to consider whether these shorter channel/smaller overlap transistors provide a path to higher cutoff frequencies, we can consider the formulations for f_t in the presence of contact resistance $R_{contact}$ (under the assumption that $R_{contact,source} = R_{contact,drain}$ and for simplicity that $C_{gs} = C_{gs,overlap} + C_i$).

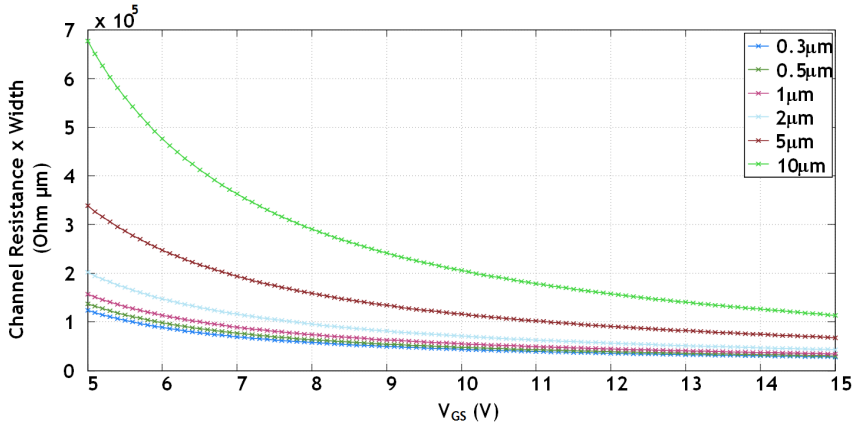


Figure 2.22: Gate voltage dependence of channel resistance for stepper TFTs

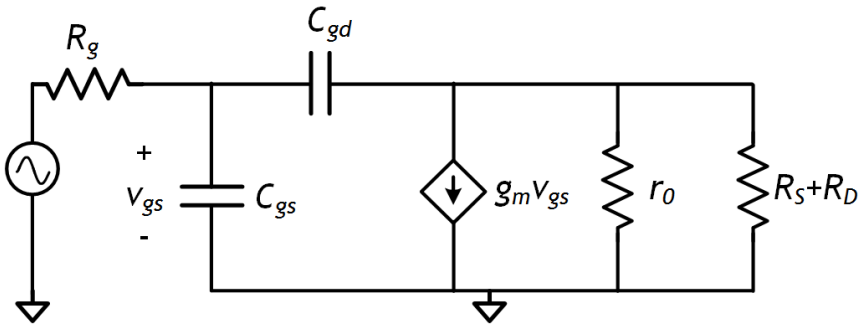


Figure 2.23: TFT small signal model with contact parasitics

Through small signal analysis of the circuit in Figure 2.23, we obtain:

$$f_t = \frac{g_{mi}}{2\pi(C_{gs} + C_{gd}(1 + 2g_{mi}R_{contact}))} = \frac{\mu(V_{GS} - V_T)}{2\pi L(L + 2x_{ov} + \frac{2g_{mi}R_{spec,contact}}{W})}$$

$$= \frac{\mu(V_{GS} - V_T)}{2\pi L\left(L + 2x_{ov} + \frac{2\mu C_i(V_{GS}-V_T)R_{spec,contact}}{L}\right)}$$

where $R_{spec,contact}$ is the specific contact resistance ($R_{contact} \times Wx_{ov}$ in Ohm cm^2) and where we have labelled g_m more correctly as g_{mi}, the intrinsic transconductance of the FET. To first order, this approximates to the following as a function of measured g_m [49]:

$$g_m = \frac{g_{mi}}{1 + g_{mi}R_{contact,source}}$$

A plot of f_t as a function of both source-drain overlap and channel lengths between 100nm and 10μm at a $V_{GS} - V_T$ of 10V is shown in Figure 2.24 (a), assuming the specific contact resistance measured earlier.

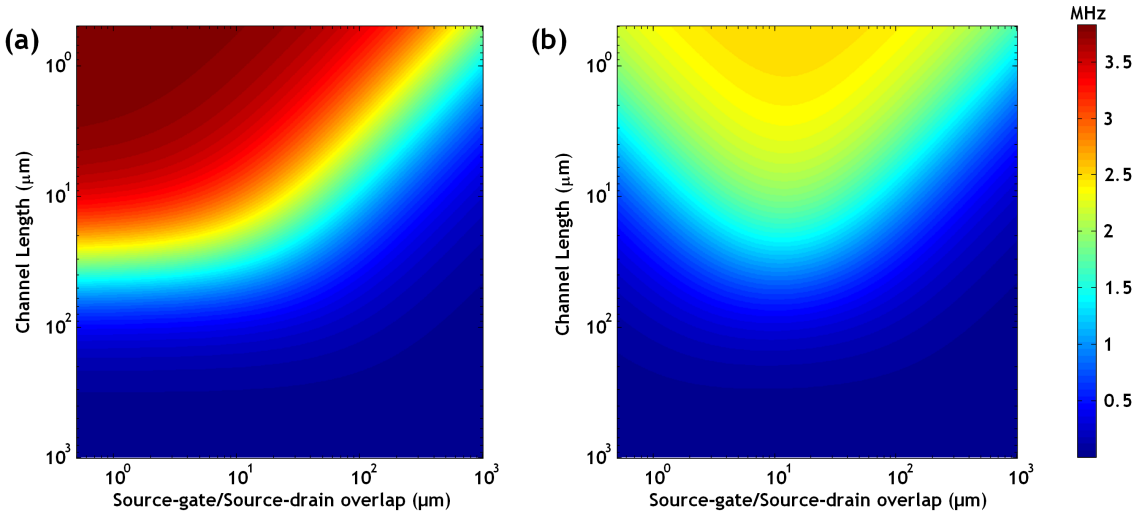


Figure 2.24: f_t as a function of source-drain overlap and channel length, (a) with and (b) without a contact-resistant dependent mobility

As can be seen, once both of these become small, saturation of f_t occurs as a result of the effect of the contact resistance (without this effect, simple f_t theory would predict a cutoff frequency of 2.7GHz at $L = x_{ov} = 100nm$!) Whilst this analytical formulation of f_t is helpful in understanding the effect of contact resistance, it leverages only the intrinsic transconductance. When the channel length becomes smaller than a few microns, the contact resistance begins to dominate and the effective field effect mobility μ_{eff} drops substantially. This is typically modeled as [50]:

$$\mu_{eff} \approx \mu \left(1 - \left(\frac{\mu C_i W R_{contact} (V_{GS} - V_T)}{L + \mu C_i W R_{contact} (V_{GS} - V_T)} \right)^2 \right)$$

Figure 2.24 (b) illustrates the effect of incorporating this variable mobility dependence in the earlier expression for f_t. Again, we can see saturation of the cutoff frequency, but another interesting observation can be made by taking a cross-section at a particular channel length. This is shown, for example, at 6 µm in Figure 2.25.

As can be seen, for the contact-resistance free model and our first contact resistance model, no optimal overlap length is present whereas such a length *does* exist when taking into account the full

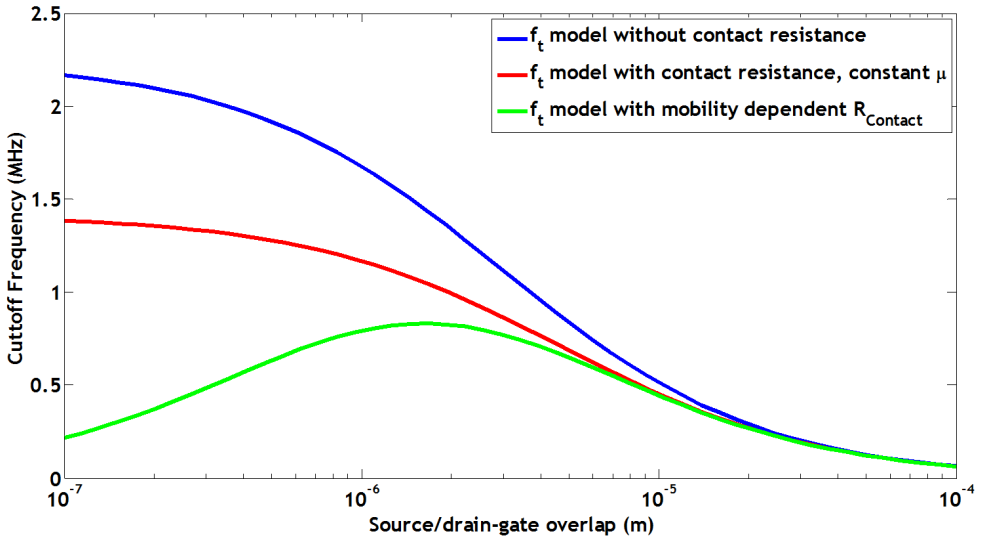


Figure 2.25: Cutoff frequency models for L=6 µm as a function of source-drain overlap

effect of contact resistance on g_m through the effective mobility. In particular for this example of L=6 µm we see that scaling of the overlap lengths below 2 µm does not bring additional benefit in terms of f_t. This is a clear illustration of the trade-off between dimension scaling for lower parasitic capacitances and the increased contact resistance that also arises through scaling.

2.3 SPICE modeling of TFTs

Having established the DC and AC performance of our a-Si TFTs (and TFTs in other technologies), we develop Level 61 SPICE models [51] for circuit simulation in Cadence (or Level 15 models for AIM SPICE, these are identical to the Level 61 models). A tutorial on the technique for model development is given in Appendix D.

Figure 2.26 illustrates the model developed for a-Si TFTs. The SPICE model is given below, and has been used successfully in the simulation of all circuits and systems in the remainder of this thesis.

```
.MODEL ModTFTaSi nmos level=61
+ alphasat = 0.5 cgdo = 3e-9 cgso = 3e-9 def0 = 0.6 delta = 5.0 el = 0.35
+ emu = 0.04 eps = 11 epsi = 7.4 gamma = 0.4 gmin = 0.9e23 iol = 3e-13
+ kasat = 0.006 kvt = -0.036 lambda = 0.0001 m = 2 muband = 0.0008 rd = 2000
```

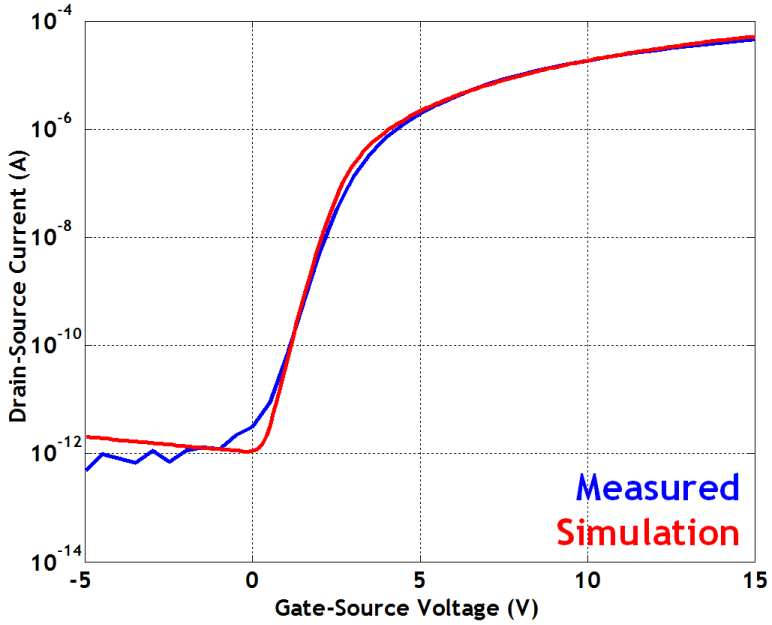


Figure 2.26: Simulation model matching for a-Si TFTs

```
+ rs = 2000 sigma0 = 1e-14 tnom = 27 tox = 2.75e-7 v0 = 0.2 vaa = 7.5e3 vdsl = 7
+ vfb = -1 vgsl = 7 vmin = 0.3 vto = 2
```

Similar models have been developed for e.g. organic (DNTT) TFTs (note the slightly different formatting, which is also acceptable for the model file):

```
.MODEL ModTFTDNTT pmos level=61
+ ALPHASAT=0.4, CGSO=8.9E-10, CGDO=8.9E-10 DEFO=0.5, DELTA=0.5, EL=0.7, EMU=0.06
+ EPS=10, EPSI=3.5, GAMMA=0.1, GMIN=2E+023 IOL=1E-012, KASAT=0.006, KVT=-0.036,
+ LAMBDA=0.26 M=6, MUBAND=0.00001, RD=100000, RS=100000 SIGMAO=5E-013, TNOM=27,
+ TOX=90e-9, V0=0.11 VAA=75000, VDSL=7, VFB=-4.5, VGSL=-2, VMIN=0.3 VTO=-3
```

2.3.1 Model development methodology

The SPICE Level 61 model has a very large number of parameters. In this section we provide some guidelines for the development of such a model from scratch. In the chosen simulation package:

1. Declare a basic Level 15/61 model and a basic MOSFET circuit with two DC voltage sources, one at the drain, one at the gate.

2. Appropriately set the Width and Length of the TFT being modeled in the simulator

3. In the model, set the appropriate semiconductor relative permittivity (EPS) and gate dielectric relative permittivity (EPSI)

4. Set the gate dielectric thickness in TOX

5. Set the nominal temperature TNOM to 27

6. Set the band mobility parameter MUBAND to a value close to the expected conduction band mobility in the TFT semiconducting material (e.g. 0.001 in a-Si); care must be taken as band mobility and field effect mobility are equivalent to each other in all material systems

7. Begin with low RD/RS of 0-a few hundred ohms

8. Set all the other parameters to their default value in Appendix D.

Once this has been completed, the following procedure should be used:

1. Fit the $\log(I_{ds})$-V_{gs} at one V_{ds} value first

2. Observe the fitting to the I_{ds}-V_{ds} curve for different V_{gs}

3. Make corrections to fit to the I_{ds}-V_{ds} curve

4. Verify that corrections did not affect the $\log(I_{ds})$-V_{gs} fit

Details of the parameters that can be used to fit the models and their effect can be found in Appendix D.

2.4 Noise measurements (1/f)

So far, we have started to describe how to build higher current and faster transistors; in the systems described in this thesis TFTs will be used as both digital and analog elements e.g. for realizing large-scale sensing functionality. As it turns out, the limitations on speed imposed by the low performance of the TFTs (e.g. low f_t) do not prevent the construction of useful systems since many signals that we wish to sense actually contain very low frequency content. However, it is also

the case that their signal amplitudes are very low, to the point where it becomes important for us to consider the effect of device noise if we are to use the TFTs as front-end instrumentation. A panorama of such signals is shown in Figure 2.27, as well as the typical location of thin-film noise.

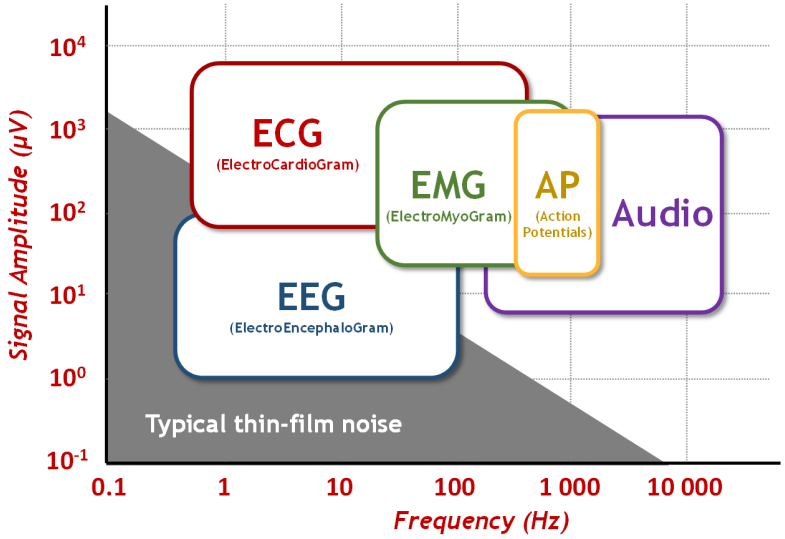


Figure 2.27: Sensing at low frequency brings us into the realm of thin-film noise levels

It is nevertheless desirable to construct elements of local amplification in thin-film technologies. Considering a large-area sensing-sheet as shown in Figure 2.28 with physically distributed sensors, transmission of low-amplitude sensor over long wired interfaces to distant computational unit can result in complete corruption of the signals. The introduction of local amplification, through the placement of an on-sheet thin-film amplifier can maximize the transmitted amplitude prior to noise corruption, resulting in a larger signal to noise ratio at the computational unit [52].

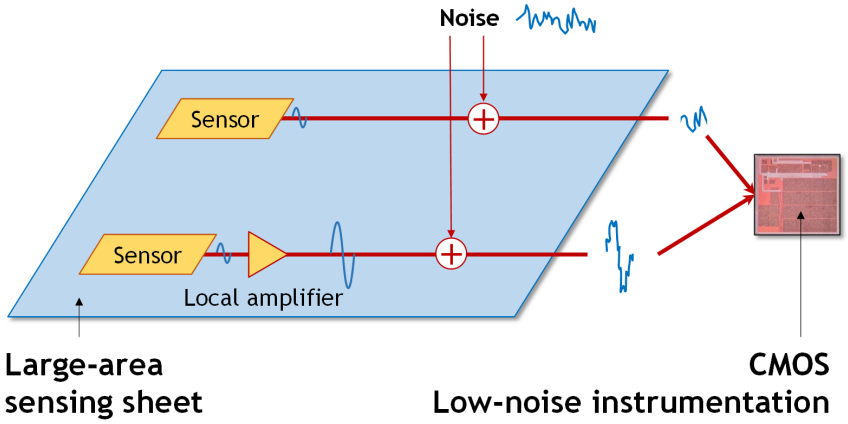


Figure 2.28: Local amplification can maximize signal to noise ratio at distant computational units

2.4.1 Sources of noise in TFTs

A number of sources of noise exist in thin-film transistors as shown figuratively in Figure 2.29, with respect to frequency.

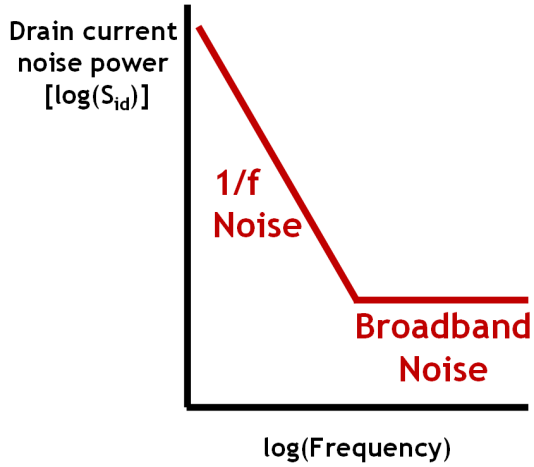


Figure 2.29: Schematic representation of sources of noise in TFTs

The first type of noise is broadband white noise, whose origin is debated but typically considered the result of either the random motion of electrons in the TFT channel or random thermal excitation of charges at the source/drain energy barriers. A strong ambiguity exists between two noise sources that are used to describe this frequency-independent noise content, *Thermal Noise* and *Shot Noise*. Expressions for the power-spectral density of the two sources are:

$$S_{id,thermal} = \overline{i_n^2} = 4kT\gamma g_m$$

$$S_{id,shot} = \overline{i_n^2} = 2qI_{ds}$$

where γ is the excess noise factor, which bears some relation to the channel length of the device. Calculation of these quantities for TFT currents however, which are typically on the order of 100s of microampere, indicate that the dominant source of noise below 10-50kHz at least, is in fact the frequency dependent *Flicker Noise*.

Although the physical origins of flicker noise, also known as 1/f noise, in MOSFET and TFTs have been studied for nearly half a century, they nevertheless still remain unclear and under active research. The general consensus is that the noise is the result of trapping/detrapping of charges at

the semiconductor/dielectric interface or in the channel layer of the transistors. The power-spectral density of flicker noise exhibits an inverse relation with frequency:

$$S_{id,thermal} = \overline{i_n^2} = \frac{K}{C_i W L} \times \frac{1}{f} \times g_m^2$$

where K is a process dependent parameter and WL is the area of the TFT. As such, three options are available for reducing flicker noise:

1. Reducing the process-dependent parameter K
2. Increasing the area WL of the transistor
3. Increasing the dielectric capacitance C_i

2.4.2 Measuring Flicker Noise

Drain-current noise in the TFTs was characterized at the University of Tokyo using an Agilent E5052B Signal Source Analyzer for different width transistors and under several bias conditions. TFTs were contacted using an automatic probe station. Input referral of the measured current noise is performed as shown in Figure 2.30 such that the noise is referred to the point where the signal is being applied, the gate of the TFT. This allows for direct comparison with the signal amplitudes being sensed.

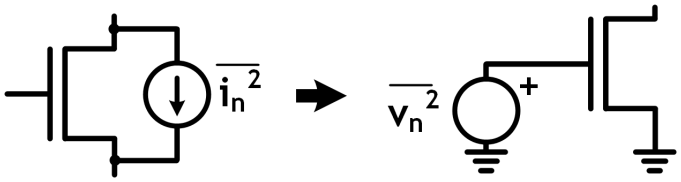


Figure 2.30: Input referral of noise

This results in a noise voltage expression as follows:

$$\overline{v_n^2} = \frac{S_{id}}{g_m^2} = \frac{K}{C_i W L} \times \frac{1}{f}$$

which we further normalize for area to be able to compare TFTs in different technologies:

$$\frac{S_{id}}{g_m^2} \times WL = \frac{K}{C_i} \times \frac{1}{f}$$

2.4.3 Representative flicker noise measurements for low-temperature a-Si, organic and ZnO Thin-Film Transistors

In this section, we show representative flicker noise measurements for the three different technologies described earlier in this chapter.

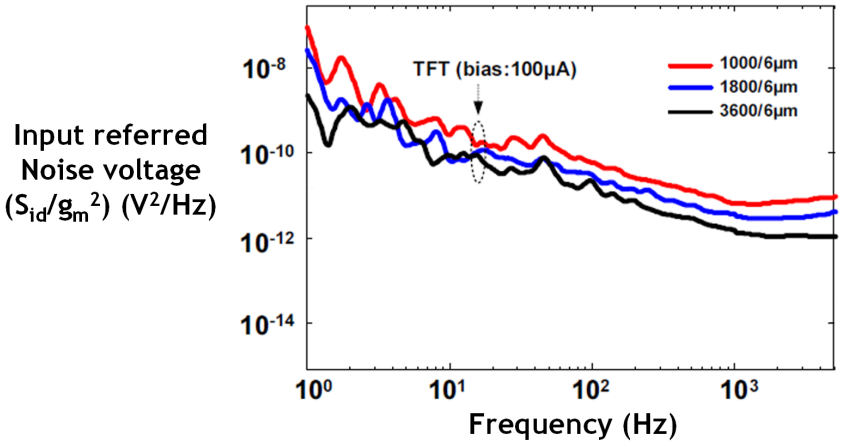


Figure 2.31: Raw input-referred 1/f noise is inversely proportional to area (data beyond 1000Hz is not representative of the broadband noise but is a measurement artifact)

Figure 2.31 illustrates the input-referred noise voltage scaling with area: increased TFT width (with fixed length) results in lower noise. This scaling is also shown in Figure 2.32 for a-Si and ZnO TFTs. In large-area systems, there is a clear potential for physically large devices, although in practice the scope for size increase is limited by pinhole density.

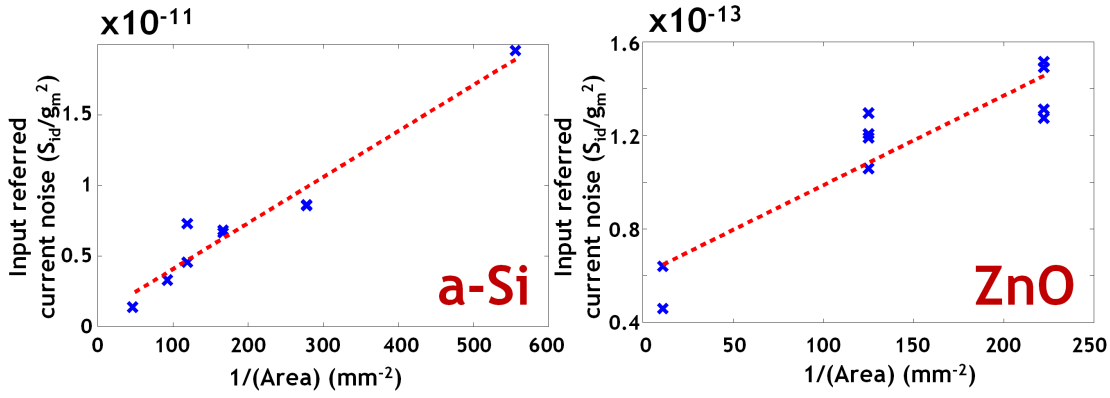


Figure 2.32: 1/f noise is inversely proportional to area in both a-Si and ZnO

Finally, we show representative measurements of 1/f noise in Figure 2.33 across all three technologies using the area-normalized input referred metric.

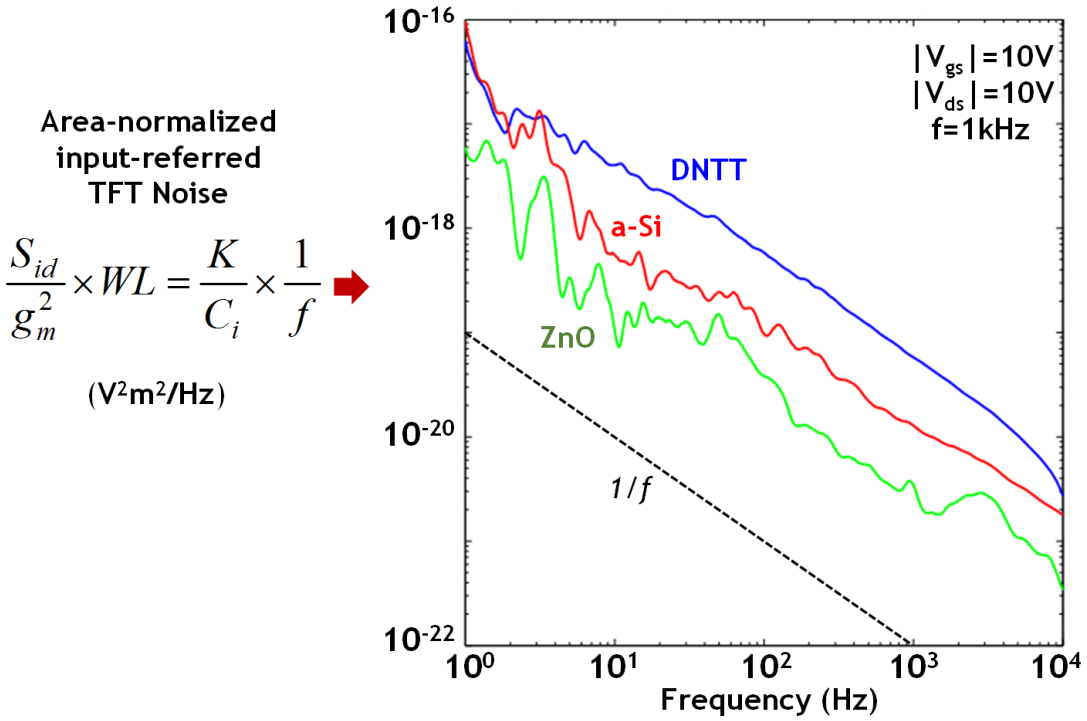


Figure 2.33: Representative examples of 1/f noise in low-temperature TFTs

It is first worth noting that the corner with the broadband noise is not reached for all these technologies as a result of the high 1/f noise. For a-Si, measurements up to 1Mhz do not show this corner; for ZnO, this corner is reached at just over 20kHz. Extracting the process dependent parameters for the three technologies gives:

$$K_{a-Si} = 3 \times 10^{-21} V^2 F$$

$$K_{Organic} = 1 \times 10^{-20} V^2 F$$

$$K_{ZnO} = 5 \times 10^{-21} V^2 F$$

These quantities can be seen to be relatively close to each other for all the technologies, within a factor of 3, and can serve as metrics for process optimization. In addition, the potential for (a) area scaling and (b) interface optimization may be different in the various technologies. The measured

noise for ZnO is the lowest out of all, likely helped in this metric by the 10 times larger dielectric capacitance.

All work in this part of the thesis was performed by the author, except for the a-Si/nc-Si diode design and fabrication (performed by Josue Sanz-Robinson), DNTT fabrication (performed by Ren Shidachi) and the ZnO TFT fabrication (performed by Yasmin Afsar).

Part II

Powering Systems

Chapter 1

Introduction

The explosion of battery-powered mobile devices and systems has revolutionized the way in which we interact with information anywhere and at any time (the market for mobile devices is estimated to be over 2 billion units in 2016 [53]). Autonomy of these systems has gradually increased over time thanks to both enhancements in battery technology, as well as incredible improvements in energy-efficiency of integrated circuits. Though non-contact charging of these devices is beginning to take-off, many of these still require daily charging using a physical charger connected to a conventional wall outlet. For convenience and practicality, non-contact delivery of power will quite possibly become the norm.

For next-generation systems on flexible substrates, as we started to introduce in earlier chapters, this is also strongly likely to be true given the need for unobtrusive and robust interconnections to these platforms. Flexible thin-film systems present us with the additional benefit of enabling the deposition and patterning of energy-harvesting devices directly on the substrates e.g. photovoltaic devices [54]. As described earlier though, monolithic integration of these on other functional layers is not likely to become viable as a result of the complex assembly processes required (in fact, making the challenge greater, most powering systems demonstrated until now combine different material technologies for various functions [11]). A need therefore exists to develop thin-film circuit blocks for management and, ideally non-contact, transfer of power between multiple functional planes of a thin-film system. In addition, in our work we will demonstrate all this functionality using a single material system: amorphous silicon technology.

To create thin-film power-circuits, a number of considerations arise due to the performance limitations of the thin-film devices; Table 1.1 summarizes these specific design challenges.

Table 1.1: Challenges For a-Si TFT Power Circuits

Property	**Cause**	**Implication**
Low transconductance ($g_m \approx 9 \times 10^{-5}$A/V for W/L=600, $V_{ds} = V_{gs}$=10V)	Disordered a-Si structure, low electron mobility ($\approx 1cm^2/Vs$), high threshold voltages ($V_T \approx 2.5$V)	Low-current switches
Only NMOS TFTs	Low field-effect hole mobility ($<0.1cm^2/Vs$)	CMOS topologies not viable
Large device parasitic capacitances	Large device features and process margins for processing on free-standing substrates	Reduced performance and increased switching losses

In the following sections we will demonstrate how to build powering systems in the presence of these challenges, and how to, in some cases, overcome these limitations. The work presented in this part leverages commercial a-Si solar modules fabricated on a 50 µm-thick polymer substrate, which are used for system demonstration purposes.

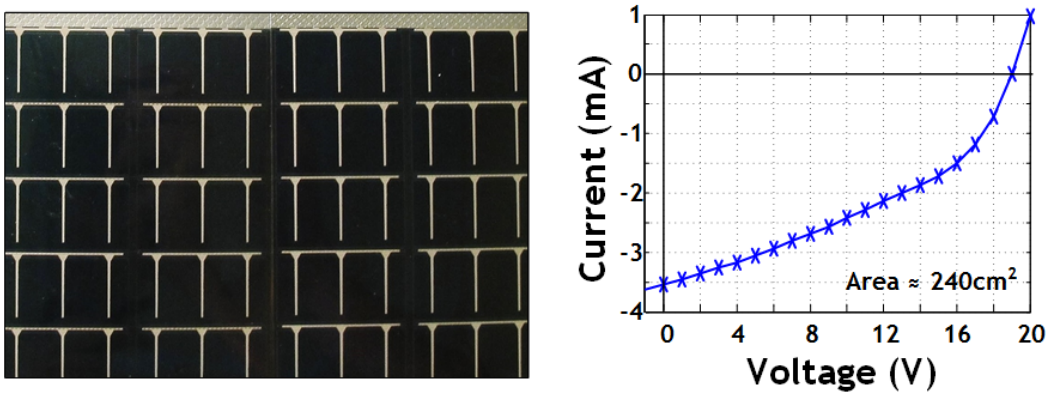


Figure 1.1: Solar modules used in this work

A typical module and a measured IV characteristic under indoor lighting conditions ($\approx$400 µW cm^{-2}) are shown in Fig. 1.1. In the demonstrated systems, the thin-film circuitry typically will draw modest current levels and as such the operating points are close to the open circuit voltage of the solar module (as opposed to the maximum power point). For the typical applications described under indoor lighting, areas on the order of 100 square centimetres may be

required, which is acceptable given the expected physical size of, for example, large-area sensor arrays.

The overall architecture of the systems that will be demonstrated is shown in Figure 1.2.

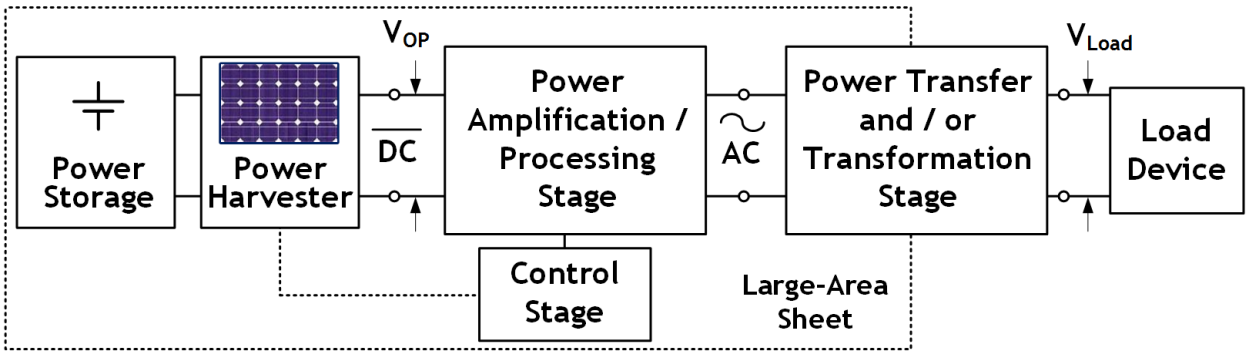


Figure 1.2: Components required for a powering system

In chapter 2 we describe the options available for the *power transfer stage* without physical interconnects. Chapter 3 introduces a *power processing stage* for capacitive transfer of energy from a solar module. Chapter 4 presents an alternative *power processing stage* using inductive transfer. Finally Chapter 5 extends the work to include *energy storage* on sheet-like systems.

Chapter 2

Non-contact transfer

The use of non-contact interfaces for the transfer of AC power (and later we will see, for signals) between sub-layers of a thin-film system substantially simplifies system assembly. Figure 2.1 shows the typical cross-section of non-contact interfaces across two sub-layers, separated by an adhesive, which is typically 50 µm thick.

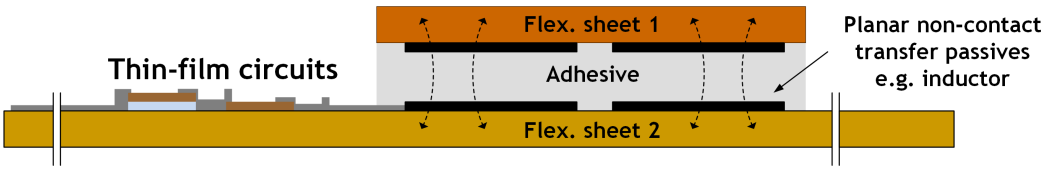


Figure 2.1: Schematic cross-section of non-contact interfaces. The ratio of passives diameter to adhesive thickness is on the order of 500

However, typically both power and signals will require appropriate modulation for transmission over non-contact interfaces (e.g. power harvested might be DC and signals generated might be baseband. The two key passives that aid in this are the copper inductor and capacitor plate illustrated in Figure 2.2.

In this chapter, we explore these two options.

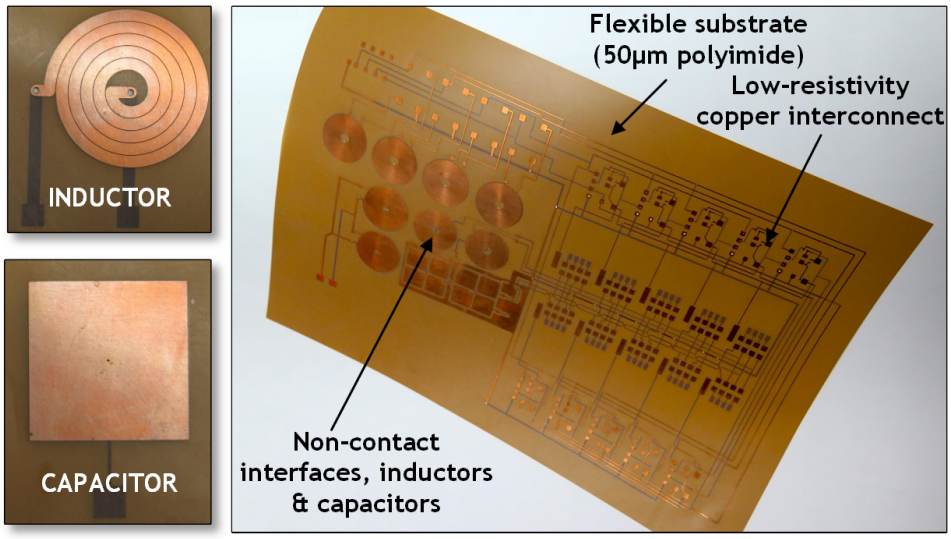


Figure 2.2: Sample passive copper backplane onto which components can be patterned or assembled

2.1 Capacitive interfaces

A typical 3x3cm capacitive interface constructed as in Figure 2.1 achieves a measured capacitance of 180pF (hence $\approx 20pF/cm^2$), with a measured dissipation factor due to non-idealities in the adhesive dielectric of 0.005-0.02 in typical signal frequencies of interest.

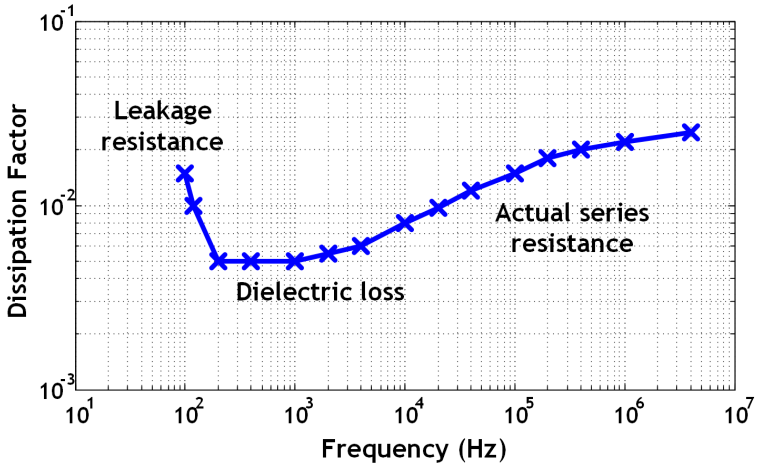


Figure 2.3: Measured dissipation factor frequency response for a 3x3cm copper capacitor with an $\approx 50\,\mu m$ thick adhesive as dielectric, and exhibiting three regions of non-idealities

This dissipation factor has a frequency dependence that is typical of non-ideal capacitor behavior as shown in Figure 2.3, showing three regions likely attributable to leakage resistance, dielectric

dissipation and actual series resistance [55]. In practice, the effect of this loss mechanism is low, and the capacitors behave nearly-ideally.

2.2 Inductive interfaces

Many considerations go into the design of inductors for the sub-layer interfaces. Three key parameters can be optimized: inductance (L), parasitic resistance (R) and self-capacitance (C). A unique benefit that can be leveraged to optimize these is that the passives can occupy substantial surface given the overall size of flexible skins.

In the design of the resonant oscillator circuits for non-contact power transfer that will be described in later chapters, we have observed that a key metric to optimize is the ratio of inductance to parasitic resistance (L/R). Making it as large as physically possible turns out to be critical to overcoming the performance limits set by the typically low electrical performance of thin-film active devices, notably low charge carrier mobility hence TFT transconductance.

The area of the inductor is the determining factor in increasing the L/R ratio. The inductance L scales in proportion to the radius of the inductor r and the square of the number of turns N,

$$L \propto N^2 r$$

The resistance R however scales as a function of the square of the number of turns only, given that the overall trace length scales with Nr and the trace width with r/N:

$$R \propto \frac{\rho N^2}{t}$$

where ρ is the trace resistivity ($70\,\mathrm{n\Omega\,m}$ in our copper inductors) and t is the trace thickness. This results in L/R, to first order, simply being proportional to the radius of the inductor, for a given passive technology. This relation is illustrated in Figure 2.4 for measured flexible copper inductors.

For the described copper passive backplane, the sheet resistance is sufficiently low for the fabrication of inductors with 4 cm radius, an inductance of 130 µH, and a series resistance of $\approx 50\,\Omega$. Table 2.1 shows a representative set of fabricated copper inductors and their corresponding parameters measured using an LCR meter and confirmed using a network analyzer.

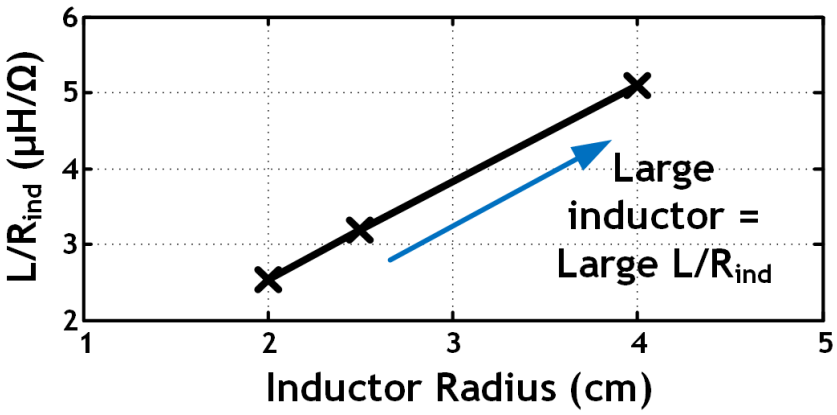


Figure 2.4: Measured scaling of L/R ratio as a function of inductor radius. Large radii are obtainable on large, flexible sheets

Table 2.1: Representative copper inductor examples

Inductor Radius	Number of Turns	Inductance (μH)	Series Resistance (Ohms)
1.5 cm	43	44	18
2 cm	15	8.5	1.5
2 cm	35	33	6
2 cm	55	73	18
2 cm	75	134	49
2.5 cm	73	143	28
3 cm	83	206	33

Unlike for the planar capacitors, the resistive loss mechanism associated with the inductive interface is substantial and causes a strong frequency dependence in the power transfer efficiency. This is illustrated in Figure 2.5, for an AC signal across sample copper inductors (15cm^2), taking into account parasitic losses in the inductor.

A manufacturing challenge that remains to be addressed is that the thickness of the backplane copper traces of 30 µm is very large compared to the thickness of the active thin-films of ≈1 µm, which could lead to step coverage challenges. The 30 µm thick passive copper together with its pattern are also likely to dominate the mechanical properties of the entire large-area system [40]. A reduction of copper thickness, enabled by higher TFT carrier mobility, would make the entire system more mechanically flexible.

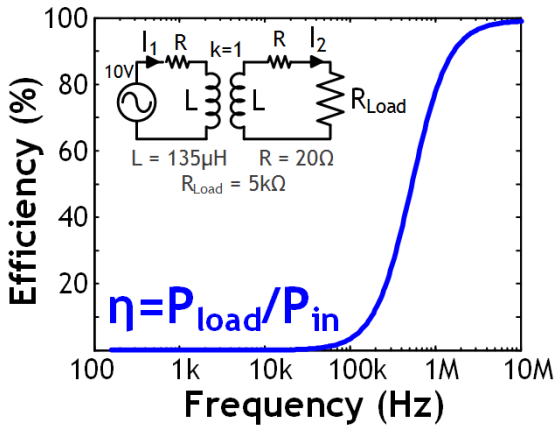


Figure 2.5: Transfer efficiencies η for inductive interfaces

2.3 Sensitivity to passive misalignment/proximity variations

An important advantage of interfacing with large-area inductors and capacitors is their low sensitivity to overlay, in-plane, misalignment. Taking the coupling to decrease proportionally to the relative loss of area overlap provides estimates of the loss of inductance and capacitance. When the centers of two circular planar inductors with radius r are misaligned by a distance d, their overlap area A changes from its perfectly aligned value of A_0 as $A/A_0 \approx 1 - 2d/\pi r$. When the centers of square capacitor plates with sides of length l are misaligned by a distance d, their overlap area changes as $A/A_0 \approx 1 - d/l$ for lateral and as $A/A_0 \approx 1 - 2d/l$ for diagonal displacement. In other words, inductors and capacitors of centimeter-size can tolerate misalignment of the order of a millimeter. This low sensitivity to misalignment greatly facilitates system assembly via lamination of subsystems on plastic sheets.

A key benefit of using inductive interfaces, in the near field, is that they are more robust against proximity variations than capacitive interfaces. The mathematical dependence of the ideal coupling coefficients as a function of distance [56] is shown in Figure 2.6. The inductive coupling coefficient is proportional to:

$$k \propto \frac{r^2}{(h^2 + r^2)^{\frac{3}{2}}}$$

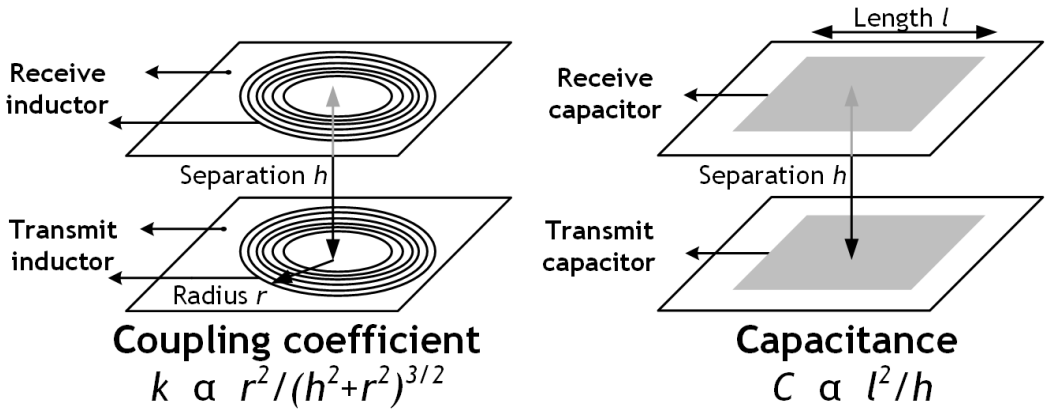


Figure 2.6: Scaling of key parameters with separation

In our present configuration, $r \approx 250 \times h$. Therefore the inductive coupling coefficient scales little with height until h becomes comparable with r. On the other hand, because capacitance does vary with $1/h$ it depends strongly on variations of proximity.

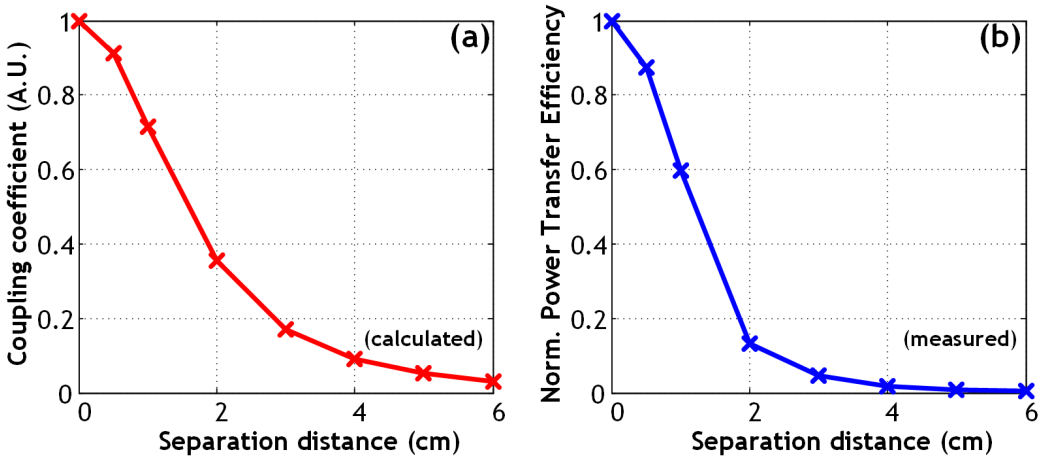


Figure 2.7: Computed coupling coefficient and measured normalized power transfer efficiency vs distance for an inductive power transfer system with $r = 2$cm.

Even for large separation distance h between inductors, Figure 2.7 (a) shows a relatively slow initial decline of the theoretical coupling coefficient, in this specific case between two 2 cm radius inductors. Figure 2.7(b) shows this trend as measured for the power management system that will be described in Section 4, which uses inductive transfer. The normalized power transfer efficiency between the transmitting coil and the receiving coil is seen to decrease in a manner similar to the computed coupling coefficient. Overall, this low dependence on small separation variations greatly

simplifies the assembly of multiple sub-layers, as it obviates the need for precise control of adhesive thicknesses between the layers.

2.4 Capacitive vs inductive interfaces

The choice of suitable passives for specific interfaces is critical and principally dictated by the AC performance of thin-film active devices, mainly thin-film transistors (TFTs) and thin-film diodes (TFDs). Nominally the operating frequencies are limited by the intrinsic cutoff frequencies (f_t) of the transistors. As mentioned earlier, f_t drops with increasing parasitic device capacitance; these capacitances can be large.

Comparing TFT f_t values with 2.5, it is clear that the comparatively low cutoff frequencies of the TFTs could make inductive power transfer unviable. Nevertheless, it may prove desirable to leverage the ability of inductors to decouple the load voltage from the transmitter voltage, which enables voltage/current step-up/step-down across interfaces. This can help address differences in circuit voltage levels and/or enhance power transmission in the face of current limitation in the thin-film devices.

Chapter 3

Solar energy-harvesting with capacitive transfer

In this chapter, we present a solar energy-harvesting system that uses the interface principles we have described to transfer power without metallurgical contact using 25 µm-thick copper capacitors.

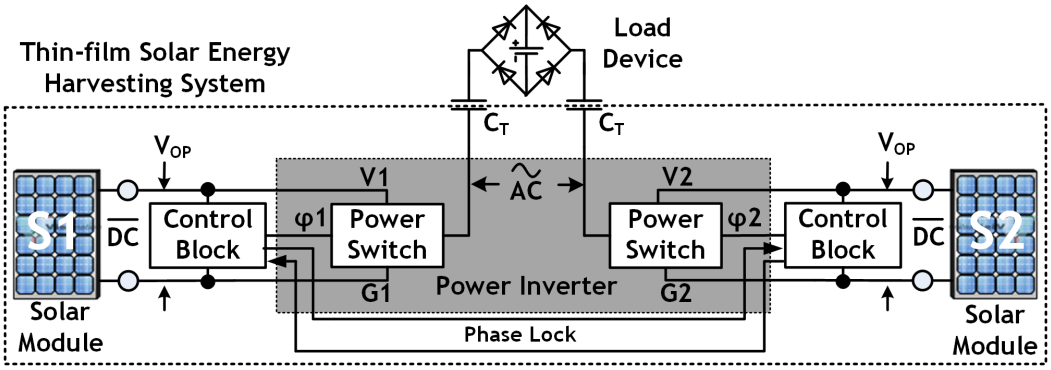


Figure 3.1: Architecture of the solar-harvesting system

Figure 3.1 shows the architecture of the charging system. The blocks generate AC power using a power inverter and control circuits, all powered by the solar modules (S1/2). Each module consists of solar cells in series and operates at an output voltage V_{OP} of 8.4V; AC power is then wirelessly delivered to load devices via transfer capacitors (C_T). The power is then stored on the load devices using a simple rectifier circuit.

3.1 System design

In this system, we consider a Class-D power stage, since this has the potential to achieve very high efficiency. In a Class-D stage, power processing is performed via switches, with the intention that all of the current drawn is delivered to the output. A critical challenge with TFT technology is that the absence of CMOS devices limits the ability to form high-quality switches at all of the voltage levels in the circuit (e.g. at high bias voltages, the extremely low current achievable with PMOS devices precludes efficient switching).

3.1.1 Operation of the inverter

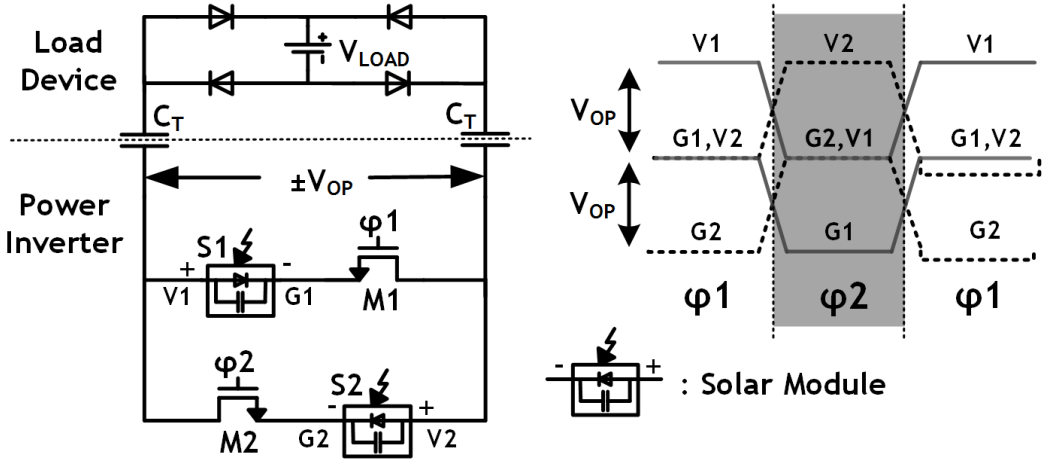


Figure 3.2: Class-D power-transfer stage, achieving switching using only NMOS devices. Power inverter using two solar modules to provide alternating current via only NMOS power switches; waveforms shown on right

Figure 3.2 shows a Class-D power-inverter stage, which achieves effective switching using only NMOS devices. This implies switching only at low bias voltages (with respect to the gate control voltage). Power inversion is thus achieved using two solar modules S1/2 (with operating voltage V_{OP}) whose polarity with respect to the output is reversed. Two NMOS TFT power switches M1/2, each at the cathode of a solar module, alternately gate the solar modules current to achieve an AC output.

However, this scheme results in switching connections between G1/V2 and G2/V1, causing the nodes to oscillate with respect to each other (see waveforms of Figure 3.2). With oscillating source

nodes, M1/2 are difficult to control simultaneously. To achieve synchronized, non-overlapping control signals (φ1/2), two control, coupled, oscillators (O1/2) shown in Figure 3.3 are used.

3.1.2 Operation of the control oscillators

Each ring oscillator is formed using five NMOS stages with pull-up thin-film resistors. The oscillators are separately powered by S1/2, and their last stages are cross-coupled via pull-down devices (M3/4) as shown in Figure 3.3. These ensure that one of the φ control signals is de-asserted before the other can be asserted.

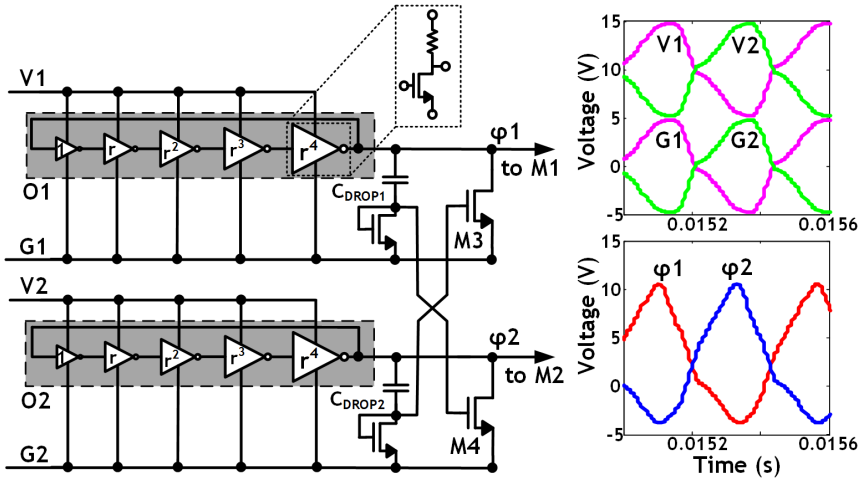


Figure 3.3: Coupled ring oscillators generate non-overlapping control signals

During φ1, V1/G1 are raised compared to V2/G2, as in the simulation waveforms of Figure 3.3. When φ1 is de-asserted by the inverter-delayed path (O1), M4 is switched off; the correct voltage levels required to control M4 are achieved through C_{DROP1}. This causes φ2 to be asserted, allowing V2/G2 to rise (due to the switching of M1/2). Then, φ1 is held low through control of M3 (with the correct voltage levels set by C_{DROP2}).

3.1.2.1 Thin-film oscillator design

Careful consideration must be given to the design of the ring oscillators, in particular the choice of resistive loads, in order to:

1. Reduce the static/active oscillator **power consumption**, P_{SUPPLY},

2. Increase the **oscillation frequency**, f_{OSC}, which is desirable for speed and power delivery (as described later)

For high voltage overdrive of the switches M1/M2 in the energy-harvesting system (increasing the output current of the TFT switches), large **output voltage swings**, V_{SWING}, for the oscillator are also desirable. This voltage swing is also affected by the choice of resistive loads as shown in Figure 3.4.

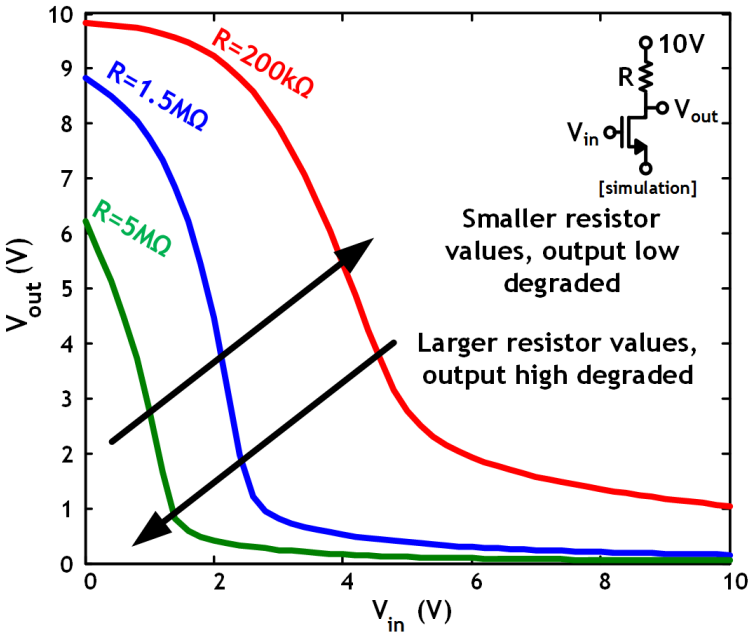


Figure 3.4: Effect of resistive load choice on the swing of the basic amplifier unit within ring oscillators O1/2

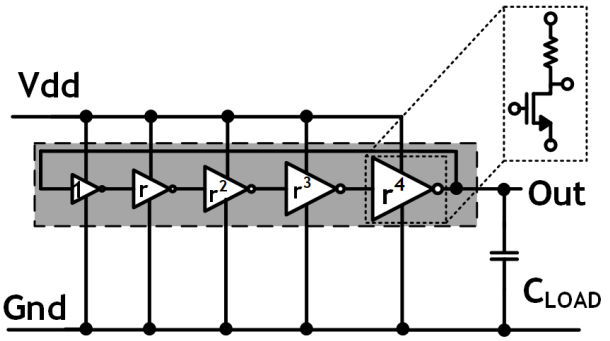
Taking into account these various desirable requirements, this allows us to propose a figure of merit, M_O for the design of such ring-oscillators:

$$M_O = \frac{f_{OSC} \times V_{SWING}}{P_{SUPPLY}}$$

This metric should be maximized and contrasts with the conventional power-delay figure of metric, which does not take into account the oscillator output swing:

$$M_{PD} = \frac{f_{OSC}}{P_{SUPPLY}}$$

In order to characterize the proposed metric in the context of the coupled oscillators O1/2, a number of individual 5-stage ring oscillators are fabricated as shown in Figure 3.5.



Stage	1	2	3	4	5
TFT W/L (µm)	600/6	960/6	1540/6	2460/6	3940/6
Load Res. (MΩ)	10xRSF	6.3xRSF	3.9xRSF	2.4xRSF	1.5xRSF

Figure 3.5: Ring oscillators with scaled resistive loads

The inverter stages are upsized by a constant ratio r=1.6. This enhances the drive capability of a reference capacitive load (C_{LOAD}=10pF-1nF) used to represent the gate capacitance of switches M1/2. Initial resistive loads are chosen to maximize the oscillator output swing for C_{LOAD}=10pF, and then scaled by a Resistor Scaling Factor (RSF) as shown in Figure 3.5. The RSF is scaled between 0.1 and 5 for evaluation of the proposed metric.

Power consumption scales inversely with stage load resistances as shown in Figure 3.6(a), dominated by on-state static current. For lower power, larger load resistances are required. Frequency is inversely proportional to the signal propagation delay through the oscillator, thus with fixed W/L ratios for the driver TFTs, frequency scales down with larger loads due to the larger RC time constants from the pull-up paths (Figure 3.6(b)). For decreasing output C_{LOAD}, the frequency increases until the 10pF range when C_{LOAD} becomes comparable with the gate capacitance of the first oscillator stage. Larger resistors limit the critical output swing as the pull-up paths become weaker (Fig. 3.6(c)), affecting the high output level. Conversely, with smaller loads, the low output level is degraded which also degrades the output swing. Increasing C_{LOAD} also significantly limits the rise time of the output which further degrades the voltage swing.

As a constant supply voltage is used, the conventional PD metric M_{PD} should remain fairly constant with load resistor scaling (Fig. 3.7(a)), but for large load resistors the metric increases due to reduced swings in the oscillator stages and hence weaker pull-down paths. The new metric

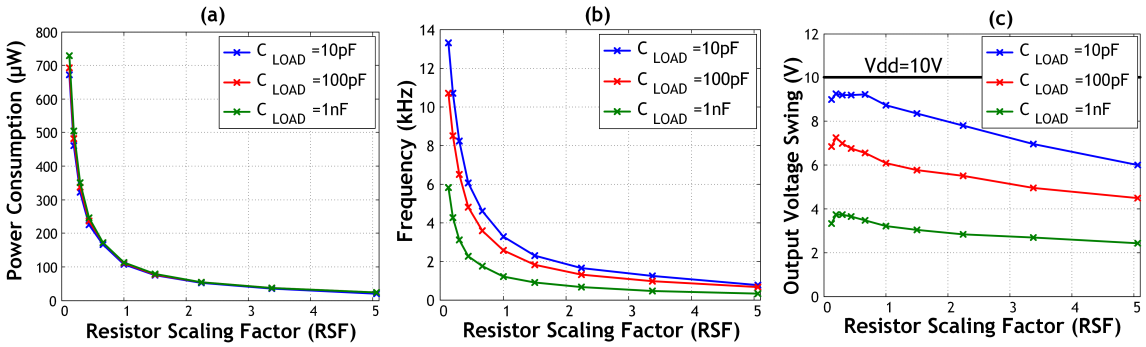


Figure 3.6: Effect of resistive scaling factor on oscillator power, frequency and output voltage swing

M_O shows qualitatively similarly behavior for low pull-up resistors, however differs substantially from the inverse power-delay product for large load resistors (large RSF) (Fig. 3.7(b)). Because of the reduced voltage swing at large resistances, M_O decreases rather than increases, leading to an optimum load resistor scaling. Maximizing this metric becomes particularly important for C_{LOAD} values comparable to gate capacitances in the oscillator, and an optimum choice of resistor loads is even clearer. A complication not embedded in our metric, however, is that low resistance loads built using the doped TFT a-Si layer, though achievable, require small L/W ratios as will be described in the next section, so load resistors may significantly dominate the area occupied by the oscillator compared to the driver TFTs.

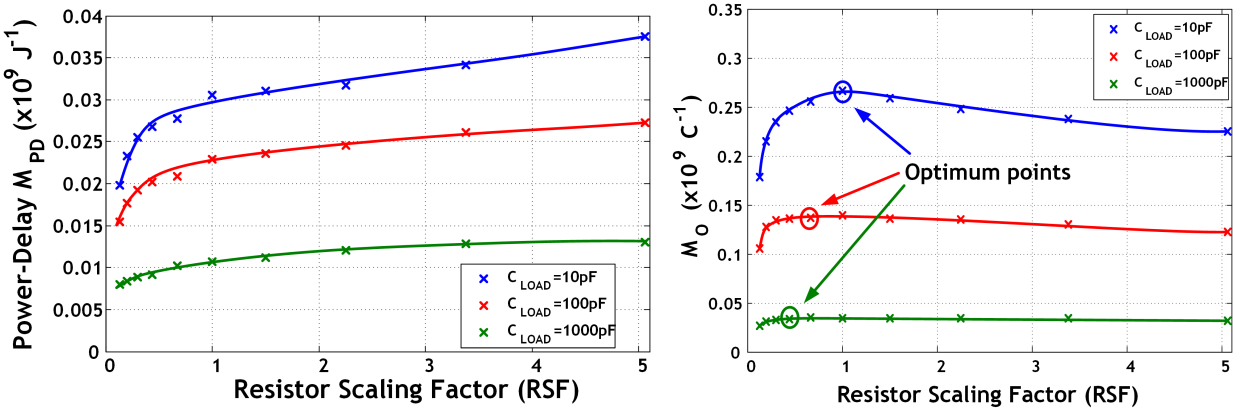


Figure 3.7: Performance of ring oscillator metrics as a function of resistor scaling factor

3.1.2.2 Doped amorphous silicon thin-film resistors

The thin-film resistors (TFRs) in the oscillators are fabricated using the n^+ doped a-Si layer, which also serves to form ohmic TFT source/drain contacts. This layer is deposited by PECVD using a 44/0.1 sccm SiH_4/PH_3 gas ratio, at a pressure of 500mT, with a pressure of 4W and a chamber temperature of 180 °C. This layer is 30nm thick with a resulting sheet resistance of 30 MΩ/square (implying a corresponding resistivity of 100 Ω cm). This value matches literature well [57], though it is worth noting that an anneal of 1h at 180C is typically required to achieve this low resistivity. A photo of a sample and micrographs of these resistors is shown in Figure 3.8.

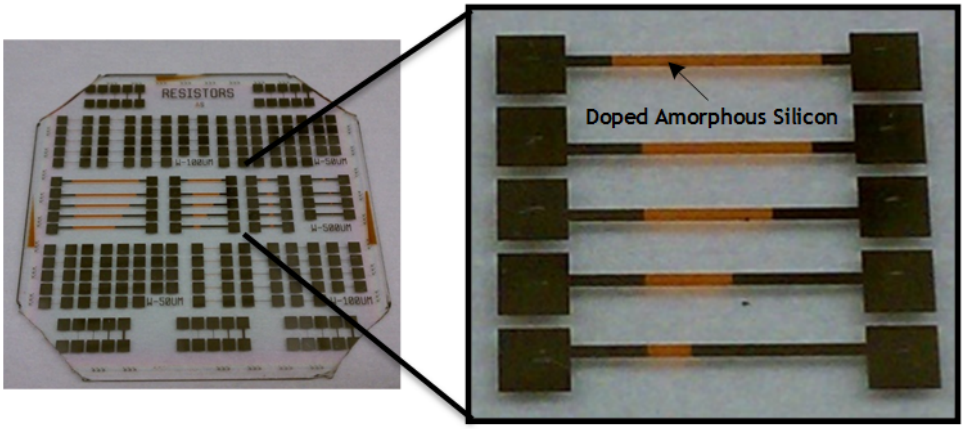


Figure 3.8: Photo and micrographs of thin-film resistor sample

Two fabrication methods were investigated as described below.

3.1.2.2.1 Fabrication by wet etching After PECVD deposition of the n^+ amorphous silicon layer (on top of a underlying layer of amorphous silicon), the top sputtered Cr/Al/Cr metallization layer is deposited and then subsequently patterned by wet etching with Cr7/Al11 etchants. This is shown in Figure 3.9.

This fabrication method resulted in highly unpredictable resistors (resistance should be directly proportional to resistor length (L)/resistor width (W)), with resistivities substantially lower than expected (<<100 Ω cm) as shown in Figure 3.10.

It is speculated that this unexpected performance is the result of either incomplete removal of the chrome layer by wet etching (despite considerable over-etching) or the formation of a conductive silicide at the surface.

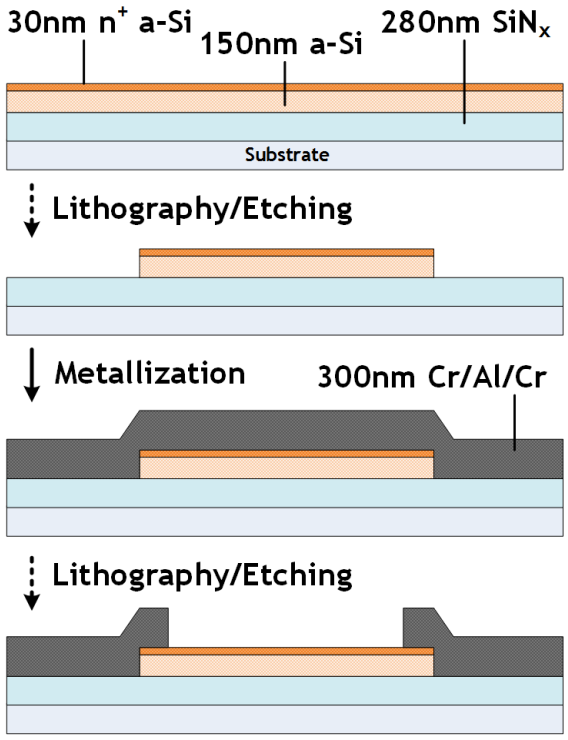


Figure 3.9: TFR fabrication process using wet-etching

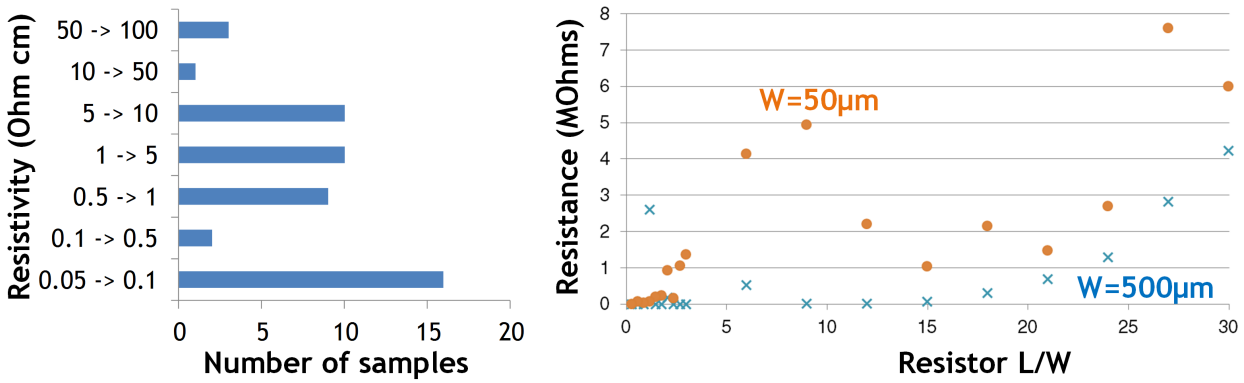


Figure 3.10: High variability in fabricated thin-film resistors (left) and unpredictable scaling of resistance as a function of L/W

3.1.2.2.2 Fabrication by lift-off An improved process flow was developed as shown in Figure 3.11.

In this process, lift-off using sonication in acetone is used to prevent contact of the metalization with the 'channel' region of the resistor. Excellent performance is achieved using this method, as shown in Figure 3.12, though more substantial variability is observed with smaller resistor lengths, most likely as a result of deviations in lithographic dimensions due to the lift-off process.

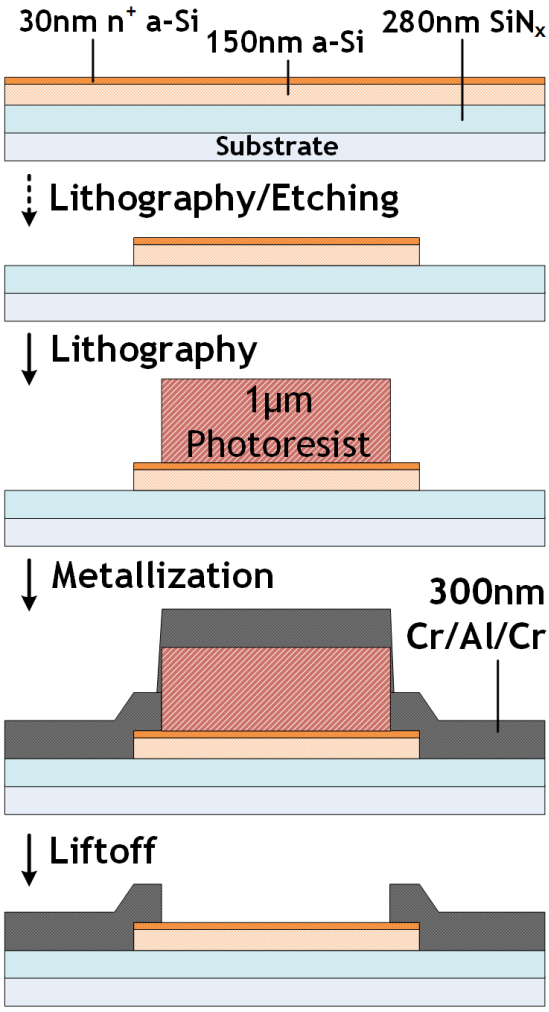


Figure 3.11: TFR fabrication process using liftoff

It is worth noting that in order to achieve resistances lower than 500 kΩ, interdigitated resistor structures can be adopted given that resistor widths are otherwise required to exceed several millimeters. We also manufacture such resistors as shown in Figure 3.13. These exhibit excellent scaling performances too for resistors with up to 100 interdigitated fingers.

It is worth noting that for additional stability over an extended period, we deposited a blanked passivation layer of ≈300nm silicon nitride over the resistors.

3.2 System performance

The circuits are fabricated and combined with solar modules on a flexible polyimide foil (Fig. 3.14). Table 3.1 gives a summary, with power and efficiency quoted for C_T from 0.5nF-2nF.

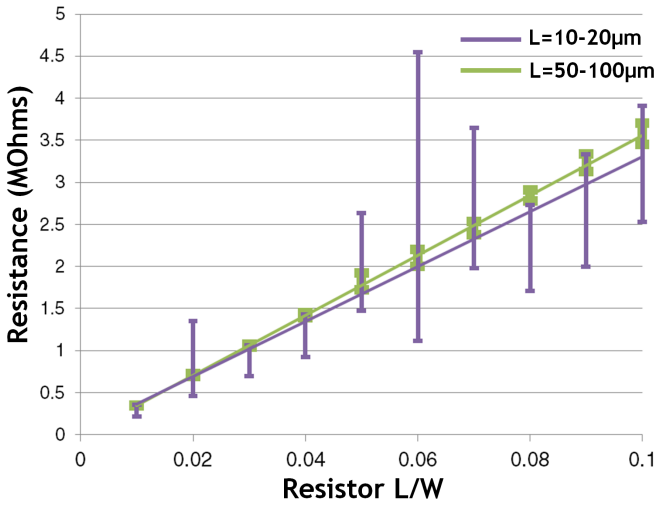


Figure 3.12: TFR scaling of resistance for two different ranges of resistor lengths

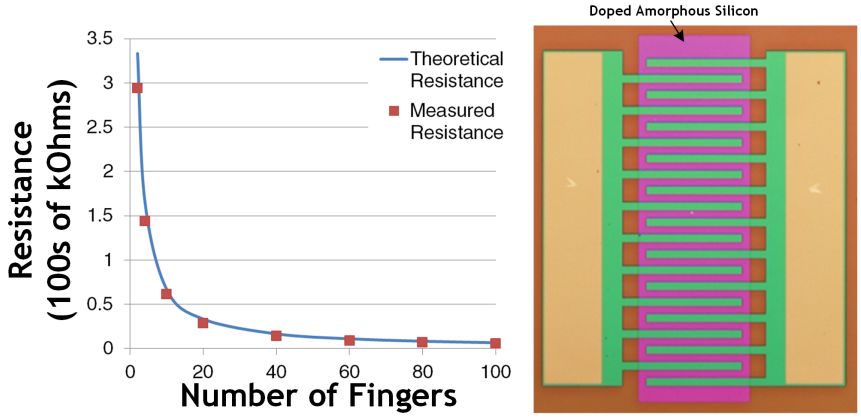


Figure 3.13: Interdigitated thin-film resistors

The next sections summarize the power-delivery of the energy-harvesting system.

3.2.1 Analysis of power delivery

With the power inverter outputs oscillating to $\pm V_{OP}$ (as desired), the output power to the load, assuming a regulated load voltage (V_{LOAD}) and an oscillator frequency of f_{OSC}, is

$$P_{LOAD} = I_{OUT} V_{LOAD} = 2(V_{OP} - V_{LOAD}) C_T f_{OSC} V_{LOAD}$$

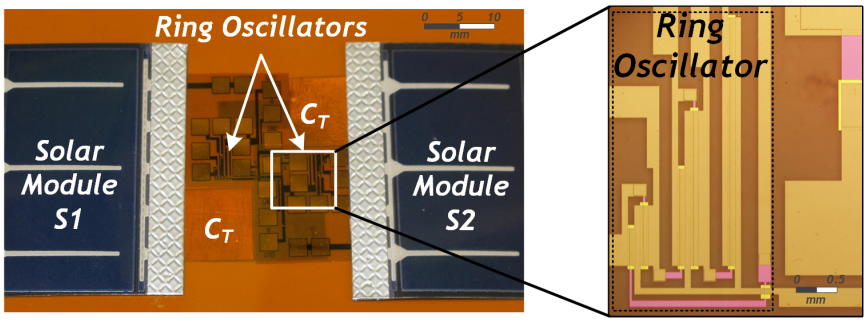


Figure 3.14: System implementation on 50 µm-thick polyimide foil

Table 3.1: Summary of system performance

V_{OP} (V)	Solar Modules (cm^2)	Power Switch Size (µm)	f_{OSC} (kHz)	P_{OSC} (µW)	P_{LOAD} (µW)	η (%)
8.4	100	3600/6	4.5	336	47 → 120	11 → 22

and the power drawn from S1/2 by the power inverter is

$$P_{DRAWN} = I_{OUT}V_{OP} = 2(V_{OP} - V_{LOAD})C_T f_{OSC} V_{OP}$$

The power-inverter efficiency is thus the ratio V_{LOAD}/V_{OP}. In an energy-harvesting system, however, the output power is typically a more important metric; P_{LOAD} is optimized at $V_{LOAD} = V_{OP}/2$, as can be seen by differentiating the expression for P_{LOAD}. Additional power is consumed by the coupled oscillators, whose static current (as a result of the NMOS-only logic) is set by the pull-up resistors. Resistor values are chosen as described earlier, maximizing the ring oscillator metric M_O.

The resulting oscillator power consumption can be modeled by considering the static power dissipation of each stage of the ring oscillator. Firstly we define, for each stage, the size of load resistances (R_{STAGE}) used, set by the TFT load capacitances (C_{STAGE} and $C_{GATE-M1/2}$) and the stage gate delays (t_{STAGE}) required. TFT capacitances thus impact the conduction losses, which, for t_{STAGE} (inversely proportional to f_{OSC}) switching at the 50% point, can be modeled as

$$P_{LOSSES\ IN\ CONTROL\ CIRCUITS} = \sum_{\text{N gates at logic 0}} \frac{V_{OP}^2}{R_{STAGE}} = \frac{ln(2)}{2} \sum_{\text{N gates at logic 0}} \frac{V_{OP}^2 C_{STAGE}}{t_{STAGE}}$$

For large switches M1/2, C_{STAGE} tends to be smaller than $C_{GATE-M1/2}$, and the power is dominated by the final stage such that :

$$P_{CONTROL\ LOSSES} = kV_{OP}^2 C_{M1/2} f_{OSC}$$

(with k as a scaling constant). This is illustrated in Figure 3.15.

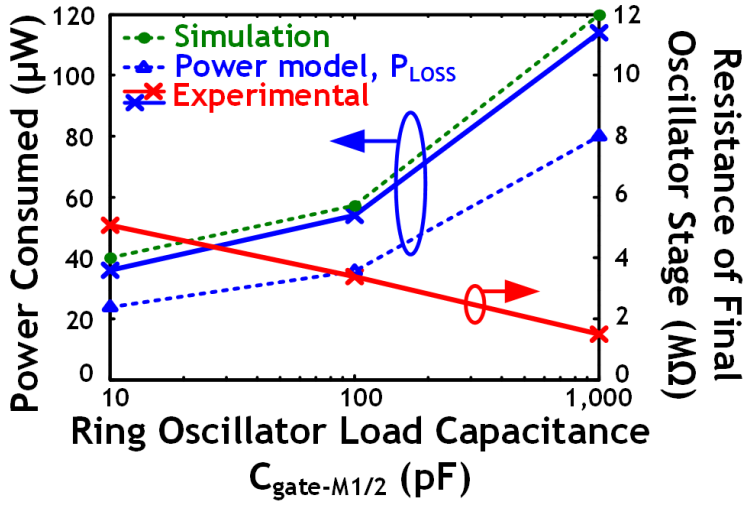


Figure 3.15: Reduction of oscillator power consumption (at constant oscillator frequency) can be achieved through reduction of $C_{GATE-M1/2}$ which allows for oscillator load resistance scaling. Power results are shown from simulation, a static power model and experimental measurements

The overall efficiency is thus given by:

$$\eta = \frac{P_{LOAD}}{P_{DRAWN} + P_{CONTROL\ LOSSES}} = \frac{2(V_{OP} - V_{LOAD})C_T f_{OSC} V_{LOAD}}{2(V_{OP} - V_{LOAD})C_T f_{OSC} V_{OP} + kV_{OP}^2 C_{M1/2} f_{OSC}}$$

Fig. 3.16 shows the effect of scaling C_T, from analysis and simulation (using the Level 61 SPICE model described earlier). In order to increase η, C_T must be increased; as indicated in the equation for P_{LOAD}, this permits higher output power without increasing $P_{CONTROL\ LOSSES}$.

Raising f_{OSC} does not affect η, until the point where M1/2 can no longer fully charge the outputs to $\pm V_{OP}$. Fig. 3.17 illustrates this by showing the output power from the system with respect to the switching frequency f_{OSC}. Three regimes set by the TFT operation are identified. Initially, output power increases with f_{OSC} according to the equation above for P_{LOAD}. However, at some frequency (f_{OSC} ≈10kHz) the output power saturates, because the TFT switches are

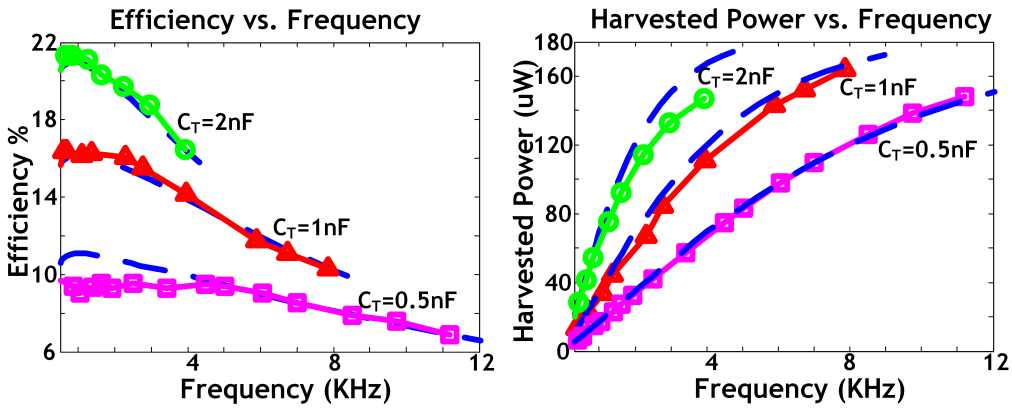


Figure 3.16: Efficiency and output power with different transfer capacitor C_T

unable to provide sufficient current to fully charge the transfer capacitors C_T to $\pm V_{OP}$. One could up-size M1/2 however, this also increases the loading on the control oscillators, increasing $P_{CONTROL\ LOSSES}$.

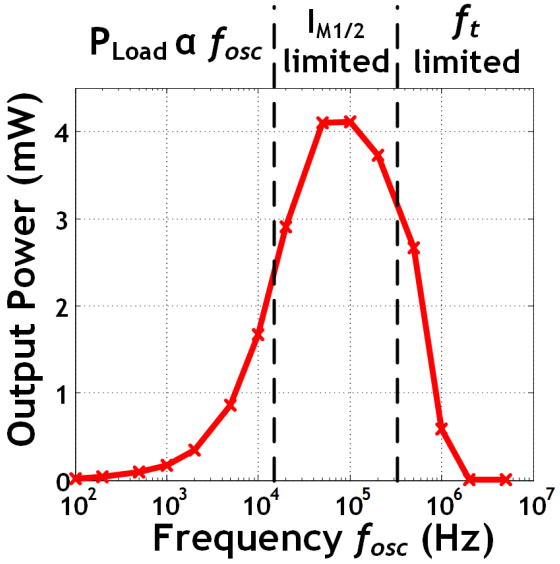


Figure 3.17: Output power versus oscillator frequency

Continued increase of f_{OSC} eventually leads to a f_T-limited regime where the TFT currents are shunted by their own capacitances rather than charging C_T. The f_T limitation in this topology makes capacitive transfer preferable. As we just described though, in a TFT technology, the power consumed by the oscillator control circuits can be significant; the control-circuit power increases with frequency, making the transition region between the first two regimes most efficient.

3.2.2 Measured power delivery

As mentioned, for maximum power and efficiency the system should operate at the highest f_{OSC} that permits output charging to $\pm V_{OP}$; f_{OSC} is thus set to 4.5kHz. Fig. 3.18 shows the efficiency and output power for various C_T values, as V_{LOAD} is swept. V_{LOAD} is optimized at $V_{OP}/2$ for output power and slightly higher for efficiency. Fig. 3.19 shows the measured maximum efficiency and output power versus C_T, illustrating that efficiencies beyond 22% and output powers beyond 120 µW are readily achievable.

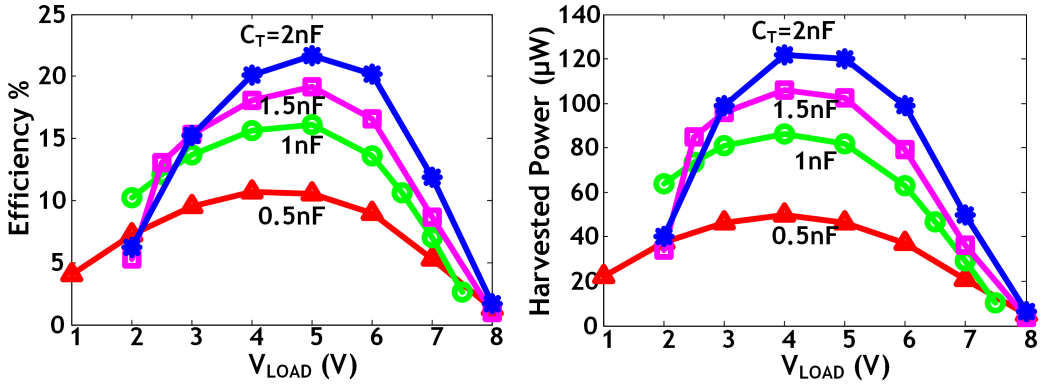


Figure 3.18: Efficiency and output power versus V_{LOAD}

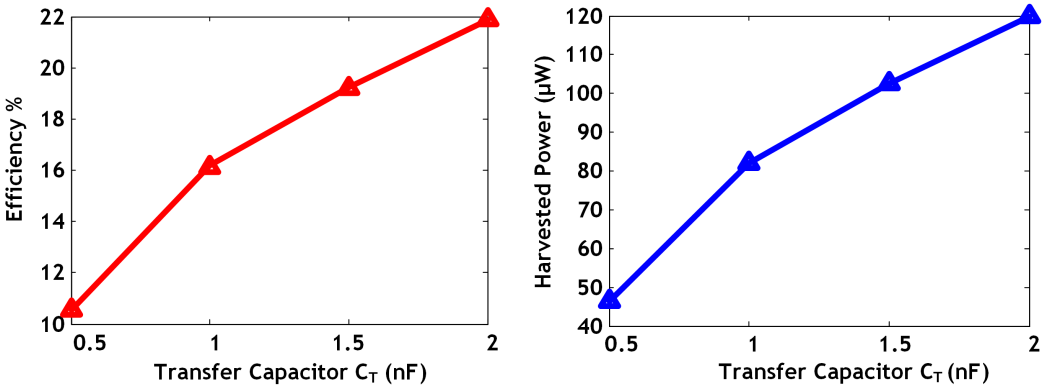


Figure 3.19: Efficiency and output power versus C_T

Chapter 4

Solar energy-harvesting with inductive transfer

In this chapter, we present a solar energy-harvesting system that uses the interface principles we described earlier to transfer power without metallurgical contact using 25 µm-thick copper inductors.

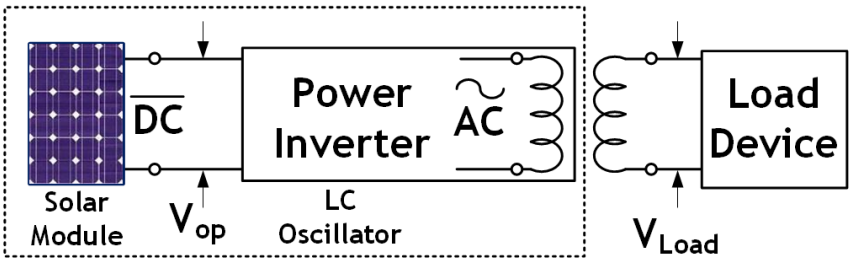


Figure 4.1: Block diagram of thin-film energy-harvesting system

Figure 4.1 shows the architecture of the charging system, substantially simpler than the one presented in Chapter 3. The key block generates AC power using a power inverter that does not require control circuits, all powered by the solar modules (S1). The solar module consists of solar cells in series and operates, typically, at a higher output voltage V_{op} of $\geq$10V; AC power is then wirelessly delivered to load devices via transfer inductors which are part of the inverter (L). The power is then stored on the load devices using a simple rectifier circuit or delivered to a resistive load.

4.1 System design: the LC oscillator

In this design we consider a Class-A stage. In a Class-A configuration, biasing currents are consumed within the stage, and only a portion of the current drawn is delivered to the output. This implies potentially lower efficiency than the Class-D stage. However, as described below, Class-A raises several advantages for overcoming TFT limitations.

4.1.1 Operation of the inverter

Figure 2.5 shows the Class-A stage considered, an LC Oscillator. A key aspect of the stage is that it is a resonant circuit. This has two important implications: (1) it resonates with TFT capacitances, enabling frequencies not limited by f_T, and thus making inductors viable; and (2) it precludes the need for explicit switching control, avoiding additional overheads.

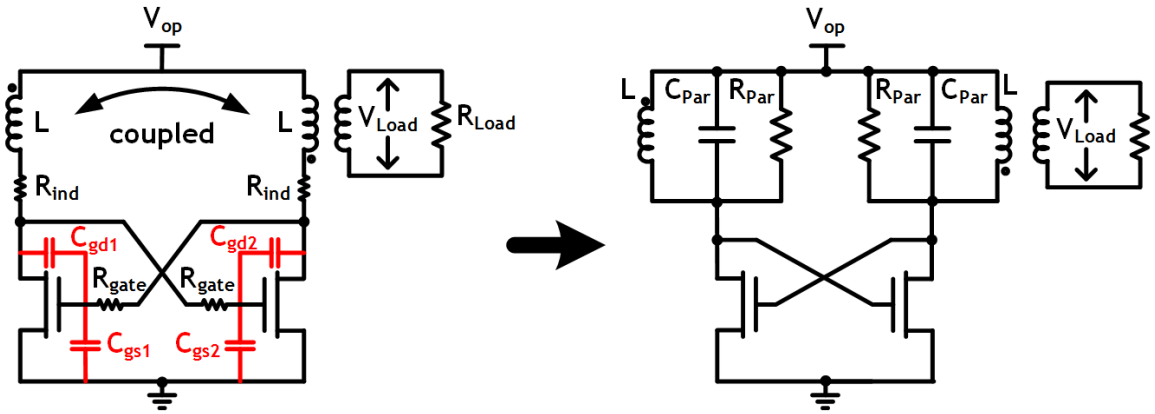


Figure 4.2: The LC Oscillator

Figure 2.5 also shows the circuit parasitics of importance. In addition to the TFT capacitances, the TFT gate resistances (R_{gate}) and inductor resistances (R_{ind}) are included. The gate resistances and capacitances are modeled as lumped elements since the frequencies of interest are much lower than that due to the associated time constant. Nonetheless, R_{gate} is significant for the analysis due to our use of a bottom-gate TFT structure, which requires thin gate metallization in order to ensure reliable gate dielectric formation. At resonance, the parasitics can be represented as shown in Fig. 2.5 (right), where R_{Par} can be estimated by:

$$R_{Par} \approx Q^2(R_{ind} + R_{gate}) = \frac{\omega^2 L^2}{R_{ind} + R_{gate}} = \frac{L}{C_{Par}(R_{ind} + R_{gate})}$$

and C_{Par} can be estimated by taking into account Miller multiplication effects:

$$C_{Par} = 2 \times (C_{gd1} + C_{gd2}) + C_{gs1,2} + C_i \approx 5 \times C_{ov} + C_i$$

where C_i is the gate to channel insulator capacitance and C_{ov} is an overlap capacitance, assuming the source-gate and drain-gate overlaps are the same.

With TFT output resistances being much larger than typical values for R_{Par}, the positive-feedback condition requires that $g_m R_{Par} > 1$ leading to the following requirement:

$$\frac{g_m}{C_{Par}} \frac{L}{(R_{ind} + R_{gate})} > 1$$

We will refer to this as the **oscillation condition**. While the first term on the left represents a dependence related to device f_T, which we presented in the first part of the thesis, the second term suggests that this can be overcome by a suitable inductor design. We will discuss optimizations of C_{Par} in the next section, but now we conside the effect of the second term. As described in Chapter 2, to first order, this is approximately proportional to the radius of the designed inductor. Thanks to large-area we are able to exploit the ability to create physically-large inductors on plastic, which can lead to large values of this ratio.

Though the L/R_{ind} ratio is to first order independent of the number ot turns N, as the number of turns is decreased, it becomes important to consider the effect of R_{gate} which becomes comparable or larger than R_{ind}. Figure 4.3 shows the ratio $L/(R_{ind} + R_{gate})$ where this effect is observed. Optimizations of the TFT gate resistance are described in the next section.

As described earlier, fabricated TFTs achieve a measured f_T of approximately 1MHz (i.e. a g_m/C_{Par} ratio of approximately 4×10^6rad/s) at 15V, thus suggesting that the oscillation condition can be met with sufficient margin.

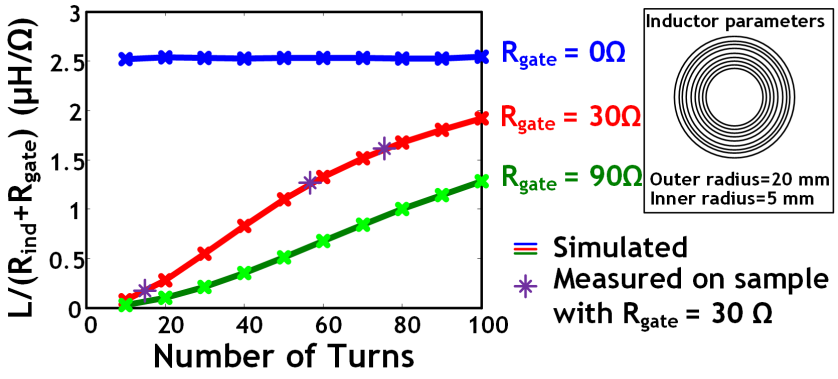


Figure 4.3: Gate resistance decreases the $L/(R_{ind} + R_{gate})$ ratio for planar copper inductors with fewer turns.

4.2 System performance

The energy-harvesting system is fabricated on 50 µm-thick flexible polyimide foil using patterned inductors of several sizes (i.e. radii of 2, 2.5, and 3 cm). A photograph of a sample is shown in Figure 4.4. TFTs with W/L of 3600/6µm are used, and the layout is optimized for minimum gate-source/drain capacitance, since maximizing ratio is critical for the oscillation condition. For TFTs with 5 µm gate-source/drain overlap, an f_T of 1.3MHz (at 15V) is measured.

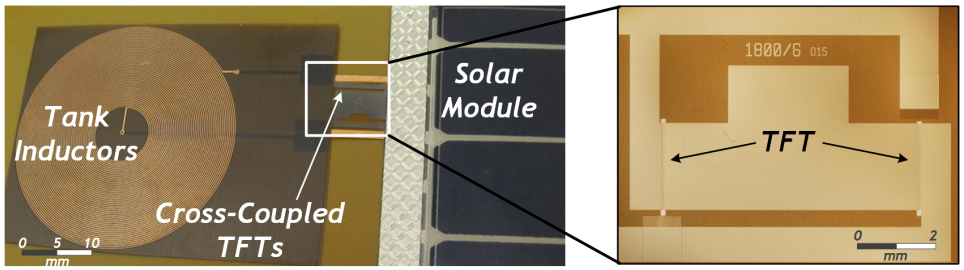


Figure 4.4: Micrograph of energy-harvesting system on flexible foil

Typical oscillator waveforms from measurement are in Figure 4.5; while nearly full swing oscillations are achieved at 2MHz, oscillations with reduced amplitude are also observed at 3.64MHz. A performance summary is shown in Table 4.1.

The next sections summarize the power-delivery of the energy-harvesting system.

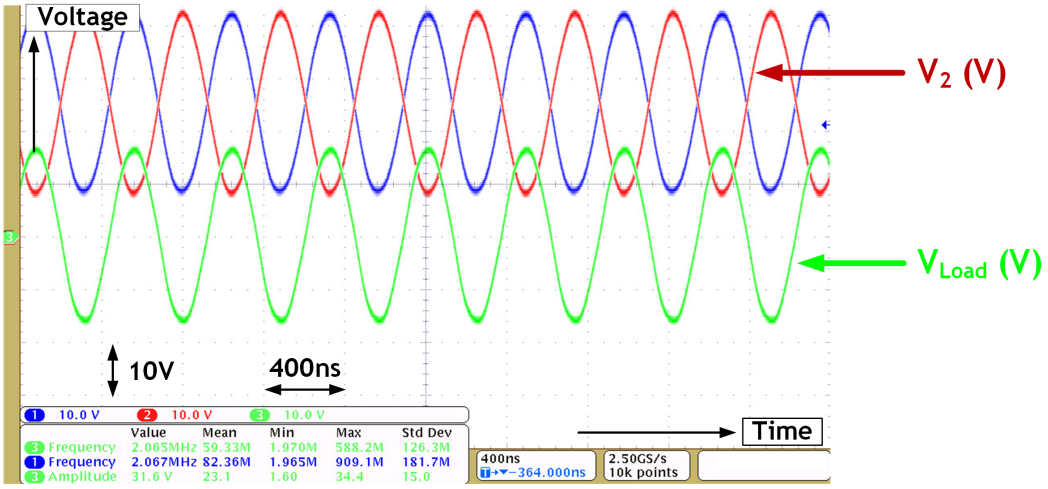


Figure 4.5: Measured waveforms from system captured via oscilloscope

Table 4.1: Prototype system performance

Inductor size	radius= 2, 2.5, 3cm		
TFT W/L	3600/ 6μm		
f_T	1.3MHz (V_{op}=15V)		
Max. Freq.	2.1MHz (V_{Load}=16V), 3.64MHz ($V_{Load} = 5V$)		
V_{op} **(V)**	15	25	25 (2 layer inductor)
Solar Modules	180 cm^2	300 cm^2	300 cm^2
Optimal R_{Load}	20 kΩ	8 kΩ	2 kΩ
Max. P_{Load}	2.6mW	20.3mW	22.1mW
Max. Efficiency	15.4%	22.6%	31%

4.2.1 Analysis of power-delivery

We start by analyzing the efficiency and power-transfer capabilities of the LC oscillator when used as power inverter with an inductively-coupled load. As shown in Fig. 4.6, power is delivered to a single load by coupling the inductors in the two LC tank branches. The load causes an associated resistance to be reflected to the oscillator outputs. For analysis, as in Fig. 4.6, we use an equivalent topology, with equal-valued inductors for each oscillator branch, independently coupled to load inductors with nearly-perfect coupling efficiency (i.e. $k \approx 1$, which is reasonable for proximity power transfer).

A reflected load (R_{Load}) hence appears in each branch. This has two effects: (1) R_{Load} impacts the positive-feedback condition, effectively altering the oscillation amplitude; and (2) R_{Load} splits the power extracted from the LC tank with R_{Par} in order to achieve the desired power delivery.

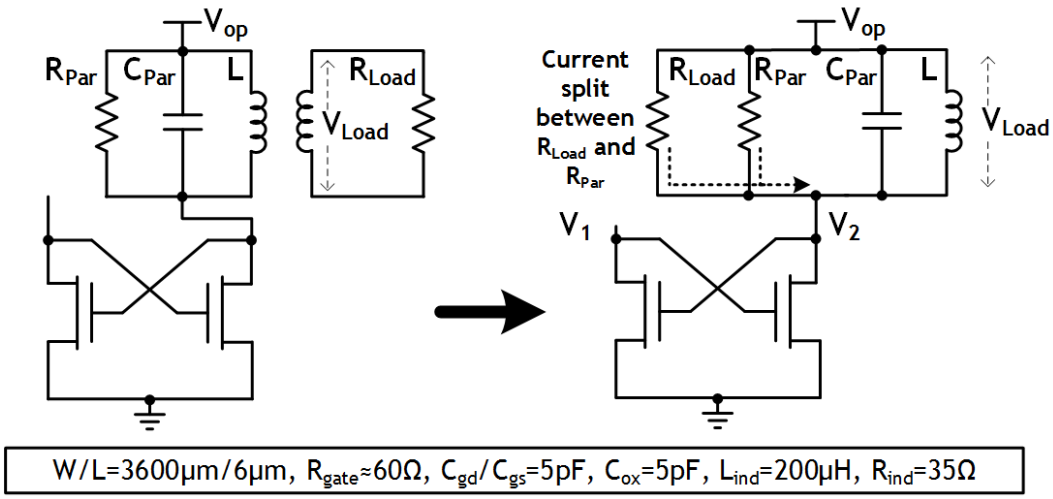


Figure 4.6: Oscillator circuit with reflected load resistance; parameter values from a fabricated sample are shown for illustration

These effects result in a design optimization methodology for maximum output power and efficiency. To analyze this, we define an oscillator strength parameter S; S is derived from the oscillation condition, and, as described in the following subsections, it suggests how the designer-selectable parameters, R_{Load} and g_m , should be set to maximize output power and efficiency:

$$S = g_m \times (R_{Load}||R_{Par})$$

An additional parameter of importance is the operating-point voltage of the solar-module (V_{op}), which affects both the absolute output power and efficiency that can be achieved.

4.2.1.1 Power-transfer optimization

For each oscillator branch, the power delivered to the load is:

$$P_{out} = \frac{V_{Load}^2}{2 \times R_{Load}}$$

where V_{Load} is the amplitude of the AC oscillations. This equation suggests that R_{Load} should be minimized for maximum power transfer; however, due to its impact on S, R_{Load} affects V_{Load}. In addition, if this oscillator delivers power to another thin-film sheet, the assumption of a small R_{Load} may not be valid.

In order to sustain oscillations, reducing R_{Load} thus requires g_m to be increased. This can be achieved in two ways: (1) by increasing V_{op}, which raises the gate-overdrive of the TFTs; or (2) by increasing the W/L of the TFTs. Figure 4.7(a) shows the effect of increasing V_{op} (based on transistor-level simulations using our SPICE Level 61 models for the TFTs; measurement results are also shown for $V_{op} = 20V$ to illustrate validity of the models). Due to the increased g_m, nearly full-swing oscillations can be achieved at reduced values of R_{Load} (as determined by S). Although increasing R_{Load} increases V_{Load} further, the effect saturates once sufficient S is achieved.

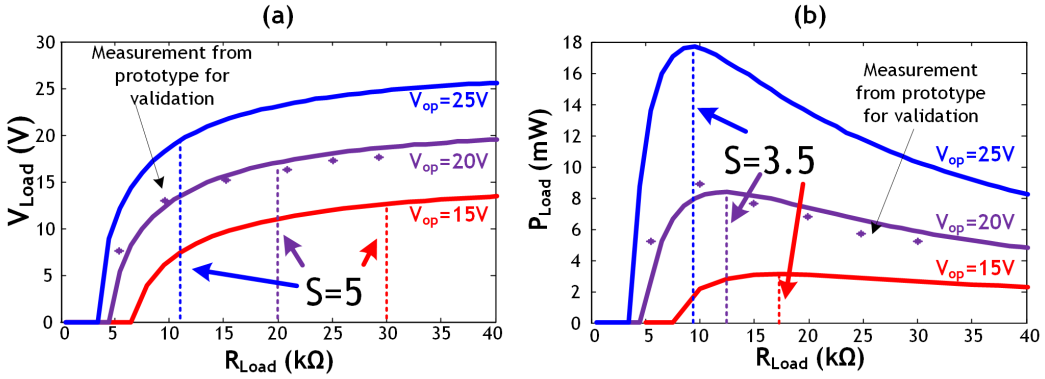


Figure 4.7: Effect of R_{Load} scaling on oscillation amplitude and output power

Combined with the inverse dependence in the equation for P_{out}, Figure 4.7(b) shows that an optimal point thus occurs by carefully selecting R_{Load}. The resulting optimal R_{Load} shown corresponds to a value of $S \approx 3.5$; however, as discussed later, efficiency optimization requires a higher value ($S \approx 5$) for V_{Load} saturation. Nonetheless, with regards to P_{Load}, increasing V_{op} also increases the achievable V_{Load}, causing the effect in Figure 4.8(a), where P_{Load} scales roughly cubically (as predicted by the equation for P_{Load}).

Similarly, increasing W/L increases g_m, enabling oscillations to be sustained at a lower R_{Load}. However, raising W/L also increases C_{Par}, thereby reducing R_{Par} in proportion. As a result, S remains unchanged, causing V_{Load} to also remain unchanged. As shown in Figure 4.8(b), P_{Load} thus scales linearly (due to R_{Load}).

4.2.1.2 Transfer-efficiency optimization

This section first examines the power consumed by the LC oscillator, and then uses this with the output power to analyze the power-transfer efficiency. Although the solar modules output voltage

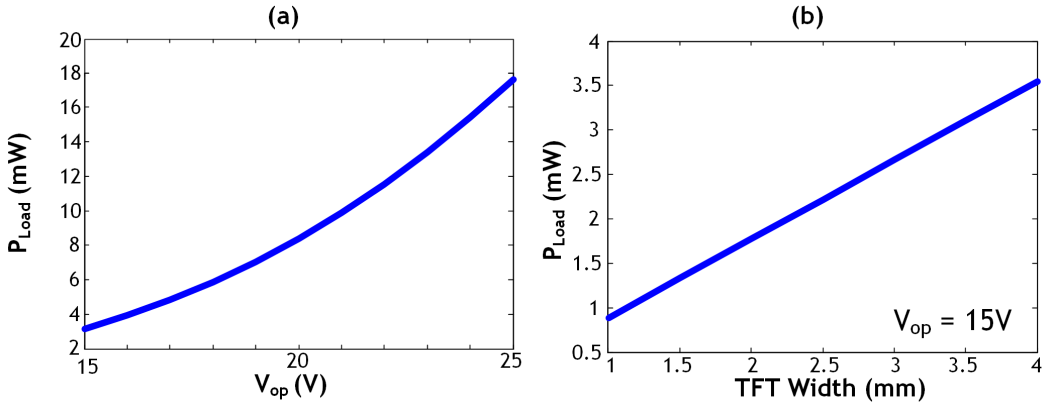


Figure 4.8: Scaling of output power through V_{op} / W/L

(V_{op}) and current are coupled, the circuit operates in a region close to the open-circuit module voltage, hence we approximate the average power consumed as:

$$P_{avg} = V_{op} \times I_{TFT,avg}$$

where $I_{TFT,avg}$ is the average current drawn by each TFT. During each cycle, the V_{gs} and V_{ds} of the TFTs oscillate in counter phase and the TFTs transition between operation regions as shown in Figure 4.9.

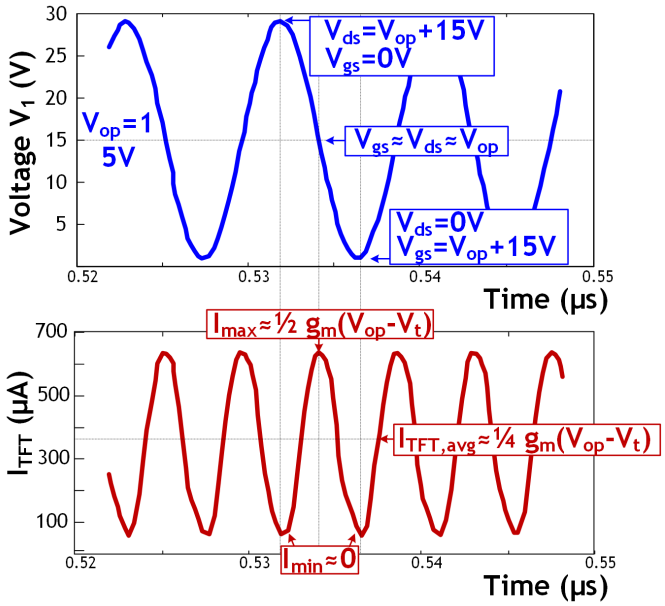


Figure 4.9: TFTs transition between several operation regimes during operation

For large oscillations of V_{load}, the instantaneous TFT current (I_{TFT}) is thus near zero both when V_{gs} is maximum (due to low V_{ds}) and when V_{ds} is maximum (due to low V_{gs}). As shown in the simulation of Figure 4.9, I_{TFT} is maximized when V_{gs}=V_{ds}=V_{op}, and the average current is thus roughly half this. As a result, the g_m in the equation for S is related to $I_{TFT,avg}$ as follows:

$$I_{TFT,avg} = \frac{1}{4} g_m (V_{op} - V_T)$$

Figure 4.10 shows $I_{TFT,avg}$ with respect to R_{Load} (plotted for the circuit parameters in Fig 4.6). $I_{TFT,avg}$ begins to saturate as R_{Load} is increased. This occurs due to increasing V_{Load}, which causes the current waveform (I_{TFT}) to reach the extreme values described above. This corresponds to $S \approx 5$.

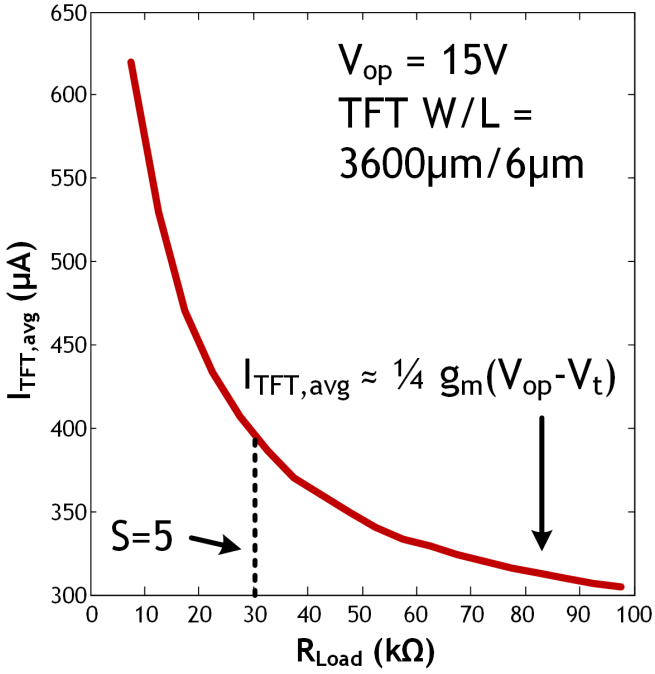


Figure 4.10: Transistor-level simulation of the effect of R_{Load} on TFT current

Now, the oscillator efficiency can be expressed as:

$$\eta = \frac{\frac{V_{Load}^2}{2 \times R_{Load}}}{V_{op} \times I_{TFT,avg}} = \frac{\frac{V_{Load}^2}{2 \times R_{Load} || R_{Par}}}{V_{op} \times I_{TFT,avg}} \times \frac{R_{Par}}{R_{Par} + R_{Load}} = \eta_{osc} \times \eta_{tank}$$

where two effective efficiencies are explicitly defined: η_{osc} corresponds to the efficiency of maintaining oscillations in the presence of R_{Par} and R_{Load} (i.e. ensuring sufficient S); and η_{tank} corresponds to the efficiency with which current is delivered to R_{Load} versus R_{Par}.

From the efficiency equation, the impact on η due to R_{Load} and g_m can be understood. In addition to its explicit impact, R_{Load} has an implicit effect through V_{Load} and thus $I_{TFT,avg}$; the profile in Fig. 4.7(a) shows the saturating effect of R_{Load} on V_{Load}. Thus, combined with the effect on $I_{TFT,avg}$ and the inverse impact of R_{Load} on η, the efficiency exhibits the optimal values shown in Figure 4.11(a) at $S \approx 5$.

On the other hand, increasing g_m through W/L sizing causes a linear increase in P_{Load}(Fig. 4.8(b)), but also a linear increase in $I_{TFT,avg}$, due to TFT width scaling. As a result, η exhibits no net change with W/L.

To understand the effect of increasing V_{op}, it is helpful to look at η_{osc} and η_{tank} separately. For η_{osc}, the achievable V_{Load} is increased linearly, $I_{TFT,avg}$ is increased quadratically (assuming square-law TFT behavior), and $R_{Load}||R_{Par}$ can be decreased linearly for a required value of S (thanks to increased g_m); as a result, η_{osc} remains unchanged. However, the reduction allowed to R_{Load} improves η_{tank}. As a result, the overall η initially improves, as shown in Figure 4.11(b). However, this improvement eventually saturates according to the expression for η_{tank}.

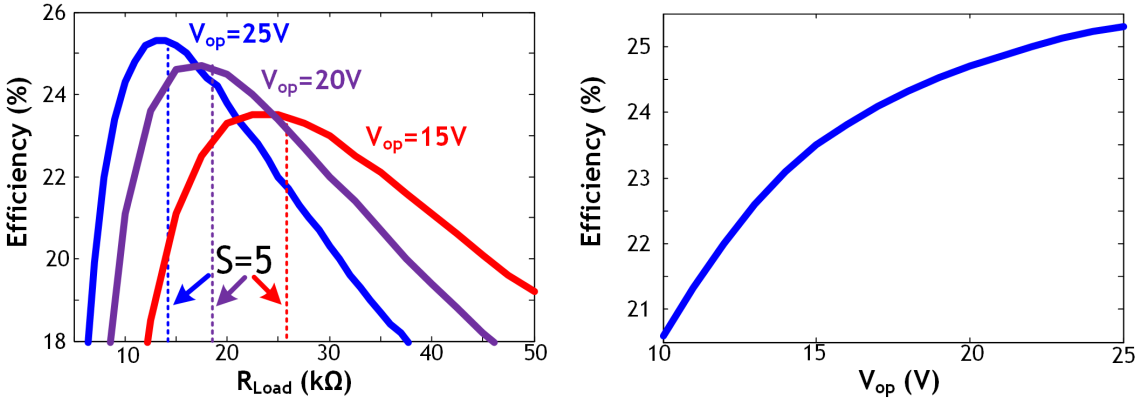


Figure 4.11: Simulations of harvester efficiency with respect to R_{Load} and V_{op}

Given these effects, we can estimate a bound for the maximum overall efficiency achievable by the topology. Using the equations defined previously, and assuming, $V_{op} >> V_T$ and $V_{Load} \approx V_{op}$

$$\eta_{max} \approx \frac{V_{op}^2 \times \frac{g_m}{S}}{2V_{op} \times \frac{1}{4} g_m V_{op}} = \frac{2}{S} \approx 40\%$$

where $S \approx 5$ has been used based on discussed optimizations.

4.2.2 TFT device optimizations for the LC oscillator

In the previous section, we identified a number of different TFT parameters that affect the power-delivery of the LC oscillator, and its basic operation through the **oscillation condition**, which we repeat here for clarity.

$$\frac{g_m}{C_{Par}} \frac{L}{(R_{ind} + R_{gate})} > 1$$

These parameters include the transconductance (g_m), the parasitic device capacitances (C_{Par}) and the TFT gate resistance (R_{gate}).

The transconductance is set by the choice of channel semiconductor (in our case a-Si), and the operating voltage V_{op} as described earlier. Switching to a higher-mobility thin-film material system such as metal oxides is a possibility for increasing this. Raising the charge carrier mobility will either reduce the value of L that is needed for efficient inductive power transfer or allow for a thinning of the, currently, thick-film inductors. Adopting oxide semiconductors for instance could enable a reduction by a factor of at least 10 in backplane conductor thickness. A challenge associated with this move though, is that these technologies sometimes do not permit the same scaling of V_{op} as a result of lower dielectric breakdown voltages compared to amorphous silicon.

Having presented the optimization of C_{Par} in our earlier discussion on f_T, we now focus in the remainder of this section on describing the scope for optimizing R_{gate}.

4.2.2.1 Mitigating the effect of of TFT gate resistance

In a bottom-gate staggered TFT, a thin gate metal is used (≈100nm) to ensure step coverage by the dielectric; however, this leads to large R_{gate}. Fig 4.3 earlier showed simulations and experimental

data suggesting a method for diminishing the impact of R_{gate} through larger numbers of turns. However, R_{gate} can also be substantially reduced through optimization of the deposited thin-films:

1. The gate metal can use an aluminium layer between chrome layers (Cr is required to prevent the growth of asperities of recrystallized aluminium into the gate dielectric, creating electrically-weak regions, and to improve adhesion to the substrate). This substantially lowers the sheet resistance to below $0.6\,\Omega$/sq, compared to $\approx 10\,\Omega$/sq. with solely Cr gate metal. This metal stack also substantially minimizes the impact of cracking of interconnect (Top-level Cr in Figure 4.12(a)) due to thermal stresses during processing on plastic substrates.

2. Circuit layout optimization, as illustrated in Figure 4.12(b), can employ thick (≈300nm) top-level interconnect (also Cr/Al/Cr) for TFT cross-coupling.

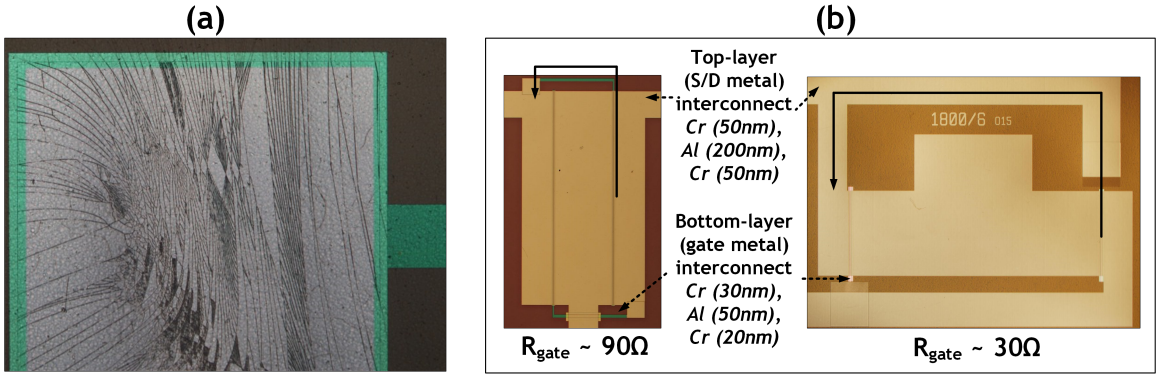


Figure 4.12: Means of optimizing R_{gate}: (a) Cracking of 300nm chrome-only top-level interconnect (b) Layout effects on gate resistance R_{gate}, with cross-coupling achieved using the bottom gate metal layer (left) or the top S/D metal layer (right).

4.2.3 Measured power delivery

4.2.3.1 Power and overall efficiency versus R_{Load}

The measured output power delivered to a load (P_{Load}) and the overall efficiency (η) are shown in Figure 4.13. Optimal values exist, as described in previous sections. Additionally, physically-larger inductors lead to larger R_{Par}, improving η_{tank}, and thereby increasing the overall efficiency.

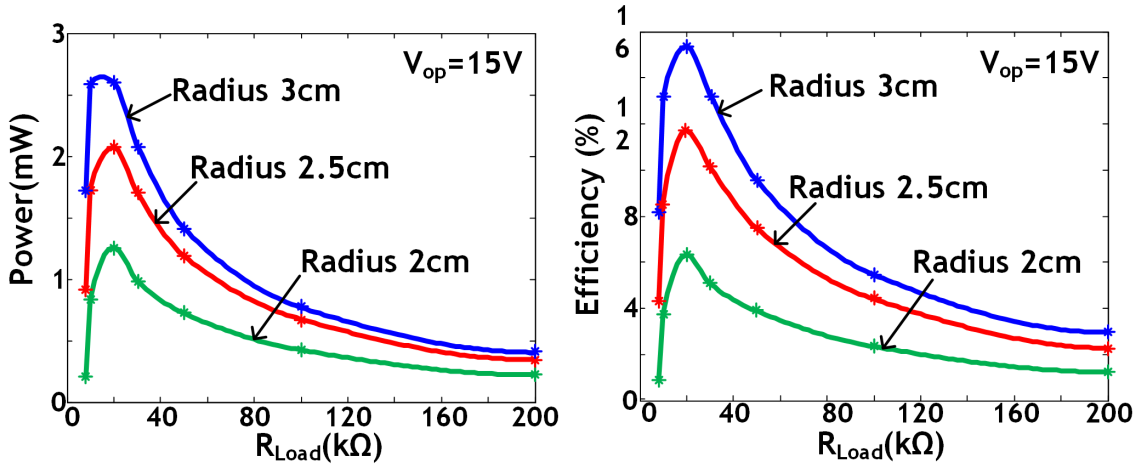


Figure 4.13: Output power and efficiency measurements with R_{Load}

4.2.3.2 Power and overall efficiency versus V_{op}

Figure 4.14(a) shows P_{Load} with respect to V_{op} (for an optimal R_{Load}), Figure 4.14(b) shows η with respect to V_{op} and R_{Load}, and Figure 4.14(c) shows the optimal η with respect to V_{op} (for an inductor radius of 3cm). As described, Figure 4.14(a) shows that P_{Load} increases approximately cubically with V_{op}. Larger inductors result in improved P_{Load} again as a result of improved η_{tank}.

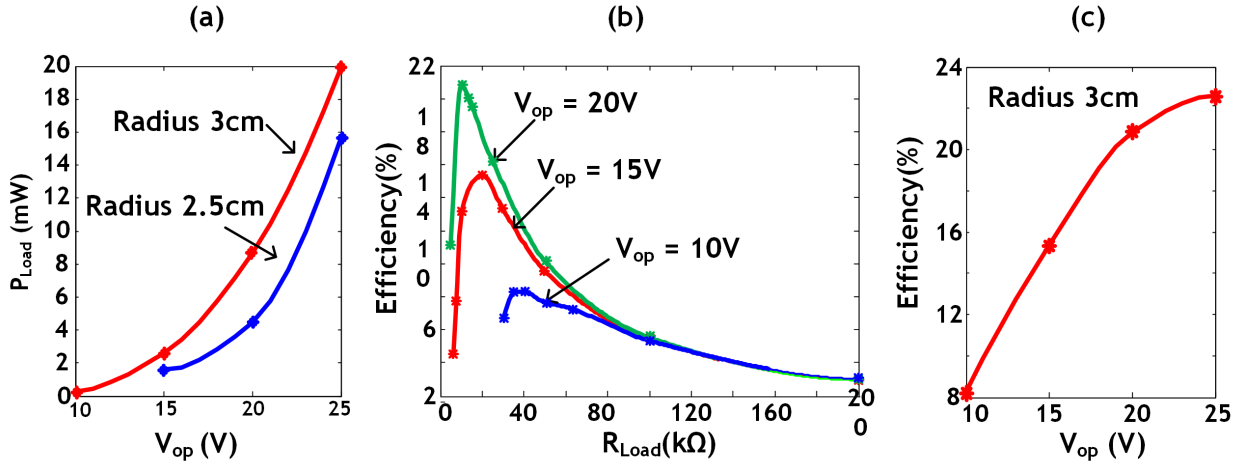


Figure 4.14: Power and efficiency measurements with respect to V_{op}

Further, as mentioned before, η initially increases with V_{op} due to resulting improvement in η_{tank} through reduced R_{Load}. Since Figure 4.14(c) approaches a fairly high voltage range for the TFTs, to further explore this effect, we increase η_{tank} by explicitly increasing R_{Par}. R_{Par} can be increased by further increasing the inductor size or by stacking inductors in multiple layers; this

causes the number of turns to effectively double, increasing L by a factor of four, while causing R_{ind} to increase by only a factor of two. The third column of Table 4.1 shows the measured results, demonstrating power-transfer efficiency approaching the efficiency bound of 40%.

4.2.3.3 Effect of low-temperature TFT processing

Close examination of Figure 4.9 reveals that the voltages at the drains and gates of the TFTs in the cross-coupled oscillator swing from 0V up to $2 \times V_{op}$. For a supply voltage of 30V, the latter is equal to 60V! It is well known however that the low-temperature TFT processing introduces degradations in electrical performance for the devices, notably increased susceptibility to TFT threshold shift which ultimately impact the performance of our energy harvesting systems over time. In this section we consider the effect of this on power-delivery.

In traditional TFT stability testing, DC stresses are applied to devices in order to understand degradation mechanisms. The performance degradation due to aging in the LC oscillator is more complicated though due to the AC nature of the stresses imposed on the devices.

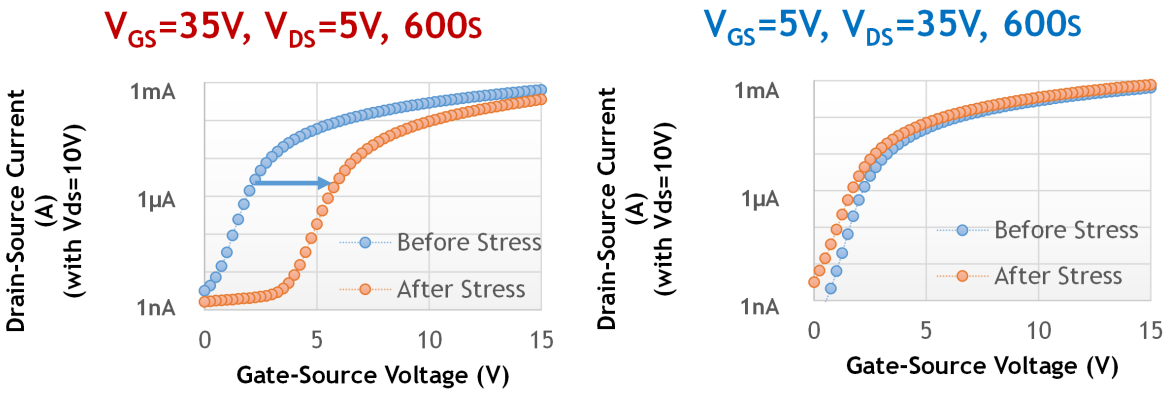


Figure 4.15: Threshold voltage shifting under linear and saturation regimes

As mentioned earlier, in the LC oscillator, the voltages at the two drain nodes of the oscillator are sinusoidal and in counter-phase. The oscillator TFTs switch between saturation, and linear regimes, about the large non-zero bias, V_{op}. A practical test using DC-bias stressing helps us identify in which regime the overall threshold-voltage shifting occurs. As can be seen from the two I-V transfer curves in Figure 4.15, the majority of the threshold shifting occurs when the TFTs are in the linear regime. The mechanism is likely due to tunneling of charge carriers in the channel

into traps or defects in the gate dielectric, silicon nitride [58]. We investigate this by depositing the gate dielectric at different temperatures.

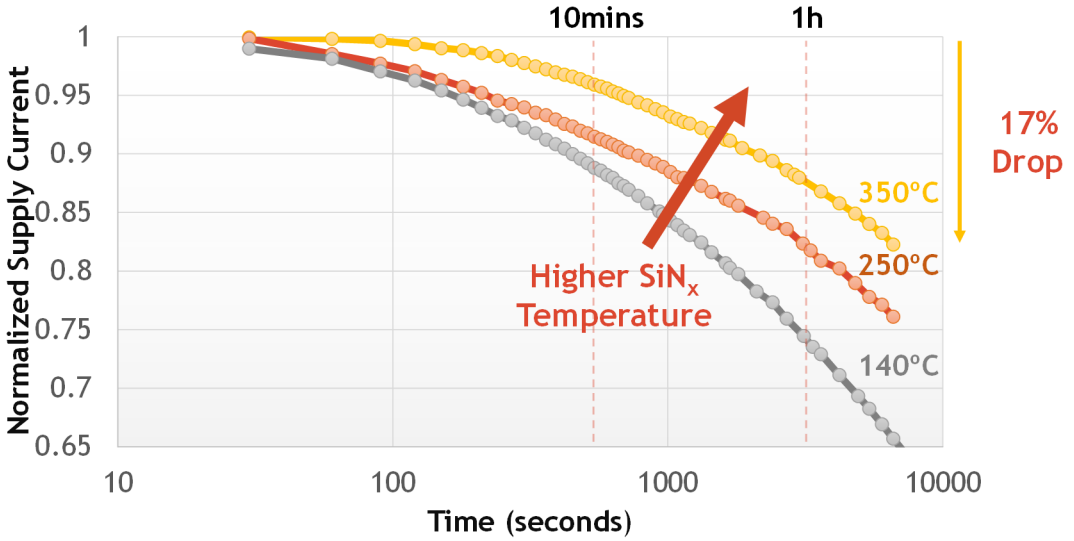


Figure 4.16: Power delivery decay as a function of time

In Figure 4.16 we show how V_T shifting as a result of the large gate fields affects the normalized supply current drawn by the oscillator, and by extension the power that is delivered to the load resistor. As can be seen for the oscillator constructed with TFTs deposited at 140 °C, a 35% drop in current is observed after 4000 seconds (this corresponds to a V_T shift of approximately 12V from an initial V_T of 2V).

By comparison, increasing the temperature of nitride deposition to 350 °C reduces this drop to only 17% as a result of an improved dielectric quality. Note though, that this temperature is generally unsuitable for processing on plastic substrates [23][41].

Upon removal of the power supply (e.g. by placing the solar module in the dark), a slow anneal is observed in the achieved normalized supply current relative to the initial current of the oscillator. As can be seen in Figure 4.17, the current returns to about 85% of its initial value after a period of about 20h. A fast increase is observed in the first 10h which is encouraging considering a typical diurnial cycle, which would give the oscillators time to recover during periods of darkness.

In addition to optimizing the TFTs to mitigate the effect of V_T shift, the same tricks used to achieve the oscillation condition can help here. Figure 4.18 shows oscillations in a TFT oscillator

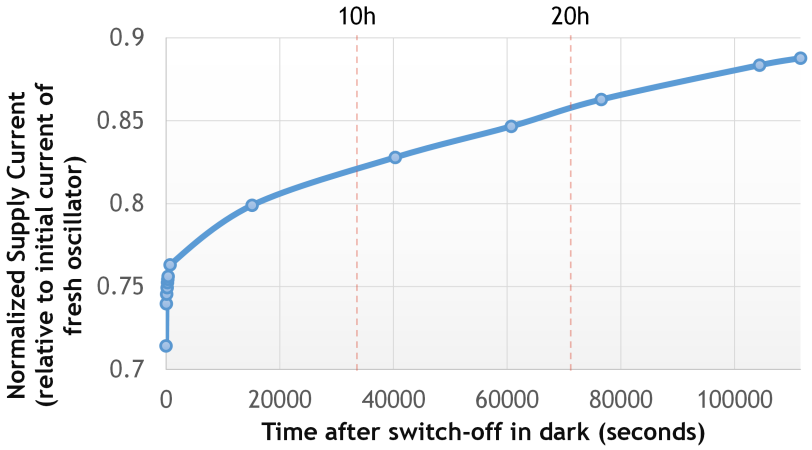


Figure 4.17: Recovery of the oscillator supply current upon removal of the solar power supply

with an inductor with a 20mm radius. By operating the oscillator for 1/4 hour with a supply voltage of 20V, the amplitude of the oscillations can be seen to decay by about 25%.

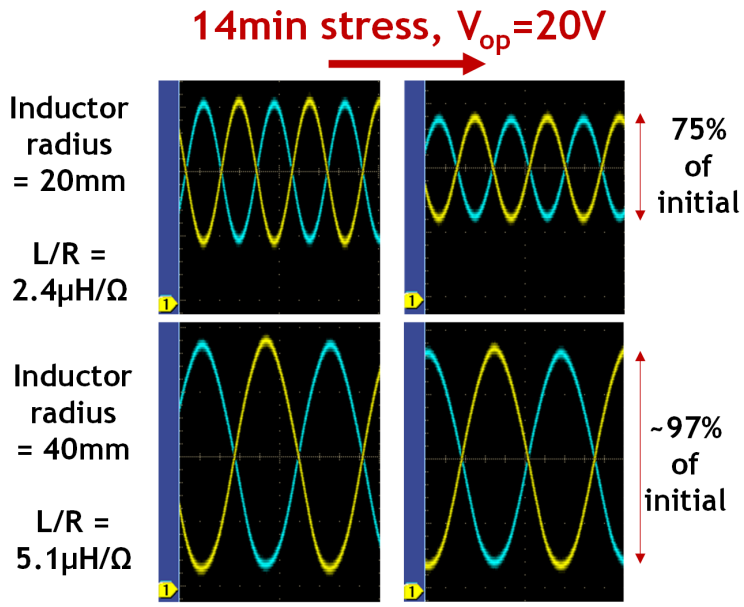


Figure 4.18: Inductors with larger L/R ratio compensate for reduced TFT g_m in oscillator from V_T shift

Using inductors with a larger L/R ratio however, a feasible option given that we are not restricted in physical size due to large-area patterning, makes the power-inverter less sensitive to long-term TFT drift. Even though the TFTs are not actually more robust to V_T shift, the circuit is able to maintain performance as a larger margin above the minimum oscillation condition is

achieved with the larger L/R ratio, and as such, the oscillation amplitude in the tank is, at least for a while, less susceptible to the drops in current.

4.2.3.4 Effect of TFT self-alignment

Our standard amorphous silicon technology which we use to build LC oscillators on plastic presents good characteristics for TFTs, but still the devices present only modest transconductance and have large capacitive device parasitics as a result of source/drain to gate overlaps. Overall as described in previous sections this results in a fairly low cutoff frequency, below 1 MHz. In order to improve this, we can adopt the technique described in Part I Chapter 2 to create self-aligned TFTs.

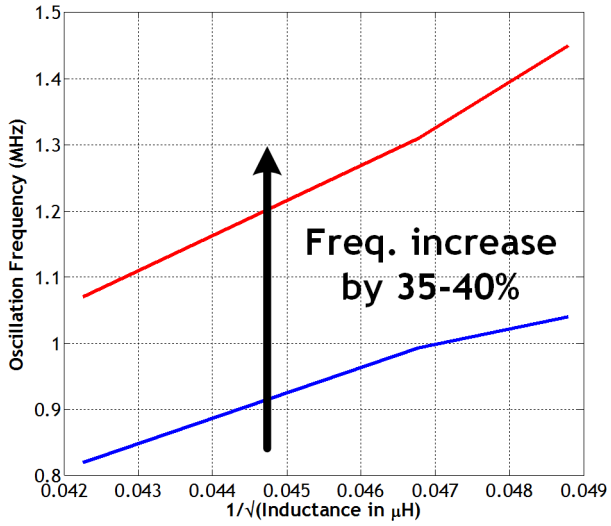


Figure 4.19: Increase in LC oscillator frequency as a result of reduced parasitic capacitances. Through self-alignment, TFT overlap capacitances are reduced from 9pF to approximately 1.6pF.

We integrate these self-aligned devices into the LC oscillator power inverter and investigate the effect on the frequency of the oscillator. Using self-aligned devices increases the TFT f_T by a factor of approximately 4 as shown earlier in this thesis. The improvement ratio for C_{Par} (self-aligned) vs C_{Par} (non-self-aligned) is about 2.1, so this should result in a 40% increase in frequency for the LC oscillators (since the frequency is proportional to the inverse square root of C_{Par}). This is indeed what is measured as shown in Figure 4.19 where oscillator frequency is shown for different inductance values.

We can however do better. Having reduced the parasitic capacitances C_{Par}, we are now in the position to reduce the L/R ratio of the inductors used in the oscillator, whilst still meeting the required oscillation condition. Decreasing C_{Par} by a factor of 2.1 allows a 2x decrease in L/R. As a result of the availability of only a certain number of fabricated inductor designs, we choose to do this by scaling the inductance by a factor of 4, which overall gives us an additional doubling of oscillator frequency as shown in Figure 4.20.

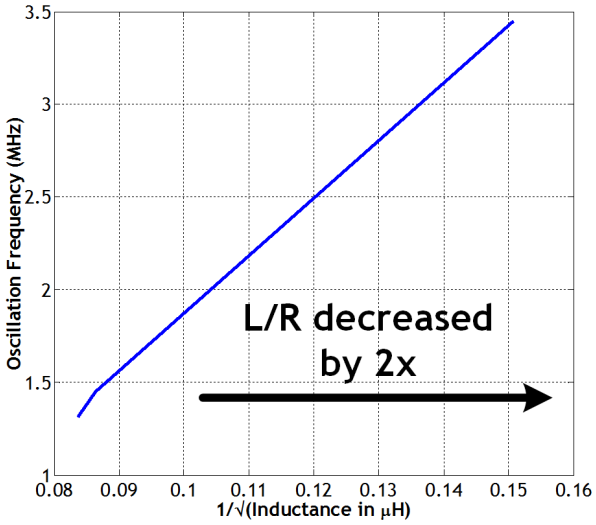


Figure 4.20: Higher oscillator frequency by optimized oscillation condition (as compared to Figure 4.19)

4.2.4 Examining the viability of thick-film inductors for organic LC oscillators

This section describes work performed at the University of Tokyo.

An interesting application of the LC oscillator could be as a sensing unit, with the sensed quantity being the frequency of the oscillator. This could be implemented in, for example, stretchable electronics where the inductance of the LC tank's inductor would be modulated by the stretching process, hence affecting the oscillator frequency [59].

To enable this though, a stretchable antenna is required with parameters suitable for use in the LC oscillator, in particular with respect to the L/R_{ind} ratio which we identified earlier as one of the critical quantities for achieving oscillations. The inductors we previously described (copper

on plastic) performed well with respect to this quantity thanks to the thick copper traces (about 30 µm) and the low resistivity of the copper.

A promising candidate for a stretchable conductor which could be used to create a stretchable inductor was recently developed at the University of Tokyo [60]. This conductor exhibits a stretchability of more than 200 percent and a conductivity of over 100 S/cm. As a baseline, the recipe consists of mixture of silver flakes (327077-50G from Sigma-Aldrich), fluorinated rubber (Daikin DAI-EL-G-801, 4-methyl-2-pentanone and a fluorinated surfactant (FS-300) in a ratio of 3:1:2:1. These materials are combined and mixed together using a stirrer at 200rpm for more than 12h.

The basic strategy for patterning consists of applying the ink to the desired substrate through a polyimide shadow mask, and subsequent curing at 120C. Figure 4.21 illustrates the resistance of a patterned rectangular trace, as a function of silver-flake concentration (over a range of ratios from 4.5:1:2:1 down to 3:1:2:1). As can be seen increase the silver content affects the resistance considerably, however this comes at the cost of reduced stretchability.

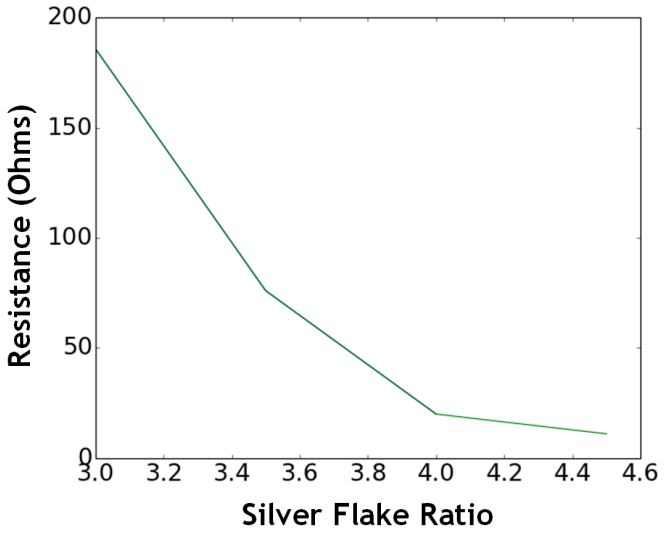


Figure 4.21: Effect of silver flake concentration

Such a shadow mask was created for a circular inductor and used to pattern the ink on a PDMS substrate. This is shown in Figure 4.22.

For a complex pattern such as the inductor however, this shadow mask approach is very challenging, however, and resulted in unreliable patterning, and extremely complex mask use due to

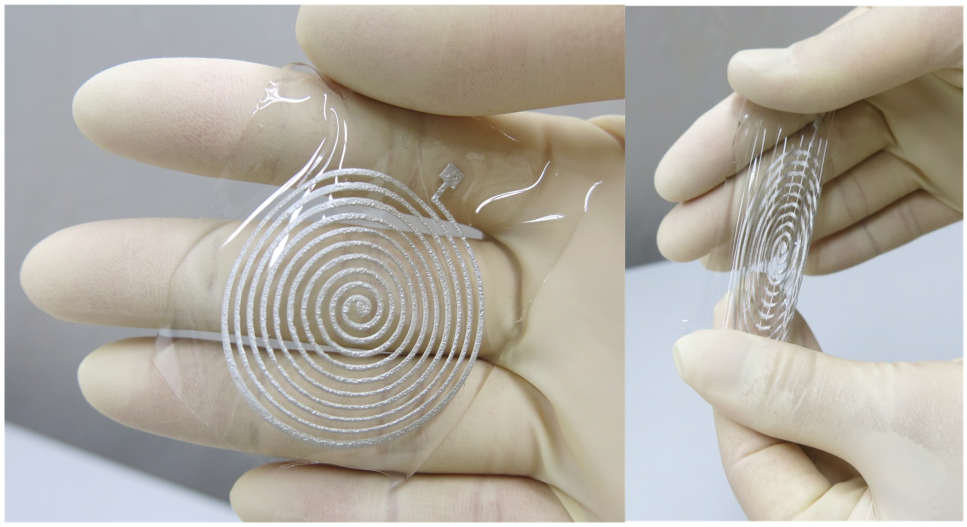


Figure 4.22: Stretchable conductor patterned on PDMS

(1) entanglement of the inductor turns on the mask and (2) positioning of the inductor turns prior to inking. This is illustrated in Figure 4.23.

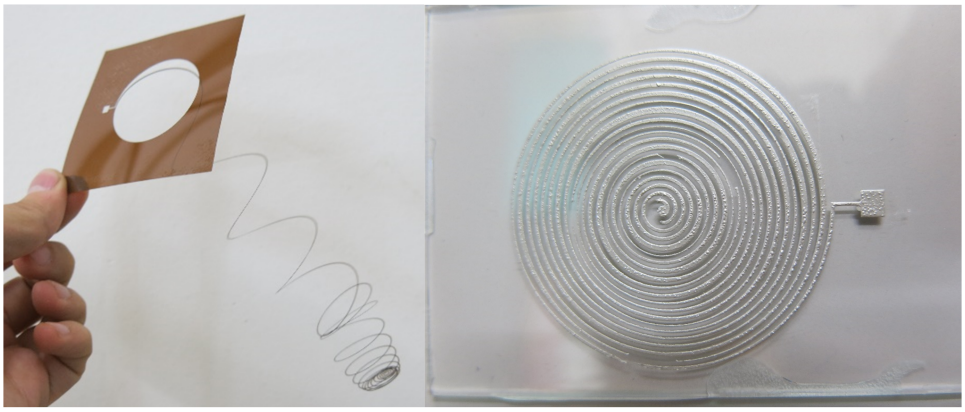


Figure 4.23: Shadow mask approach is challenging for inductor fabrication

In order to overcome this challenge, a printing solution was adopted, using a SHOTMASTER 300 micro-dispensing system as pictured in Figure 4.24. This system has a typical print speed of 120 mm/s, a best-case resolution of 250 µm and a maximum rated printing thickness of 500 µm

This machine is programmed as shown in Figure 4.25, using a series of commands that move the dispensing nozzle around the stage. Important parameters that define the final printing properties are the number of overprints, the pressure applied to the ink in a syringe during printing, the printing speed, and the height gap between the nozzle of the printing syringe and the printing

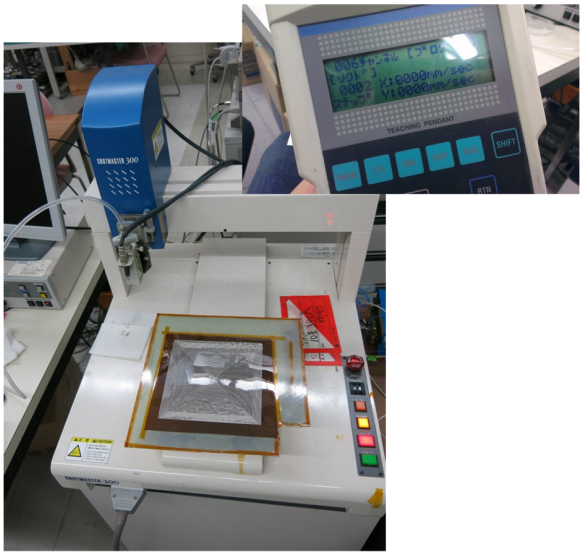


Figure 4.24: SHOTMASTER 300 micro-dispensing system

Program 005							
STEP	COMMAND	X	Y	Z	W	DATA	COMMENT
1	MOVE ABS	15	15				
2	PTP SPEED (16)						
3	SUBROUTINE CALL					Channel 100	Lower nozzle, dispense
4	MOVE INC	4	0				
5	MOVE INC	0	4				
6	MOVE INC	-4	0				
7	MOVE INC	0	-4				
8	SUBROUTINE CALL					Channel 101	Stop dispensing, lift Nozzle
9	PROGRAM END						

Figure 4.25: Commands used to program the SHOTMASTER 300 micro-dispensing system

surface. The effect of multiple printing is shown in Figure 4.26. The trace thicknesses is increased and the resistance drops in accordance.

Square inductors were patterned as shown in Figure 4.27 on 100 micron polyimide for testing. The inductance is expected to scale in a very similar manner than for the circular inductors presented earlier. In order to characterize the inductance of the printed antennas, a series resonant circuit is constructed (resistor - capacitor - printed antenna). The results of this measurement is shown in Figure 4.28, for a scaling of turns and a scaling of radii, indicating that the inductor performs as expected. In addition the figure summarizes the properties of the antennas, including the L/R ratio.

In order to satisfy the oscillation condition described earlier, the g_m/C_{par} ratio would need to be on the order of 7×10^6. For the Parylene/DNTT organic technology described earlier, this g_m/C_{par}

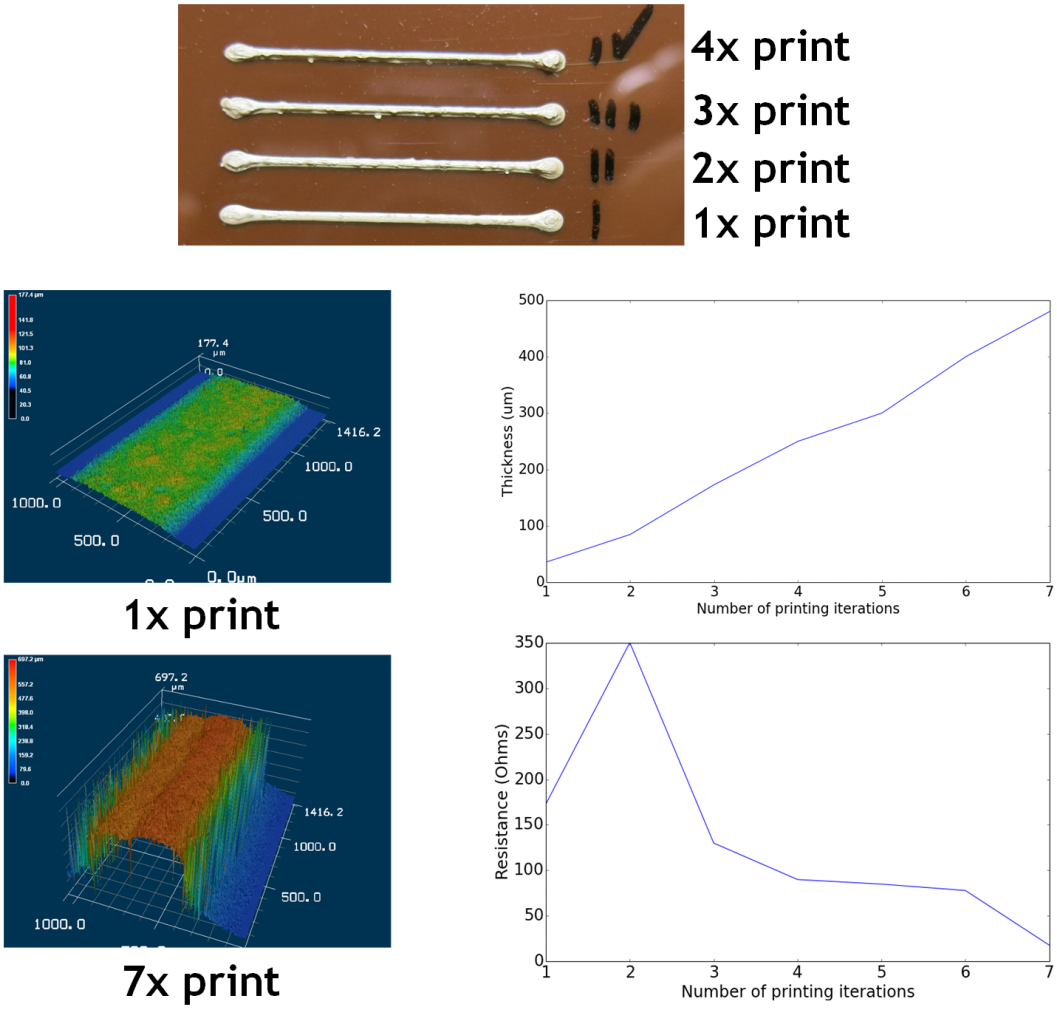


Figure 4.26: Multiple printing increases the trace thickness and decreases the trace resistance

is however, at best 7×10^5 (under assumption that the organic process could be modified to produce TFTs with a channel length of 10 microns and a source/drain-gate overlap of 10 microns- both very optimistic assumptions given the shadow mask processes used). With amorphous silicon, this g_m/C_{par} is achievable, so future work could involve combining printed inductors with amorphous silicon TFTs.

The printing process is a versatile one and Figure 4.29 illustrates additional topologies that were investigated using this micro-dispensing technique, for circular inductors or for active-matrix interconnect.

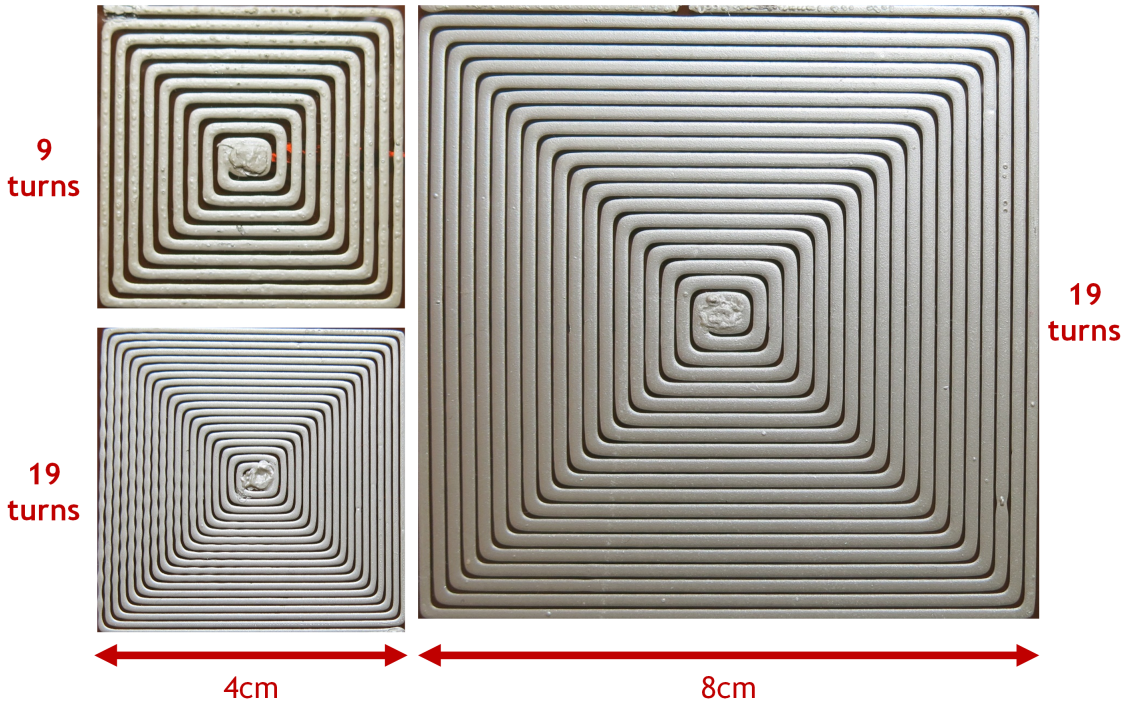
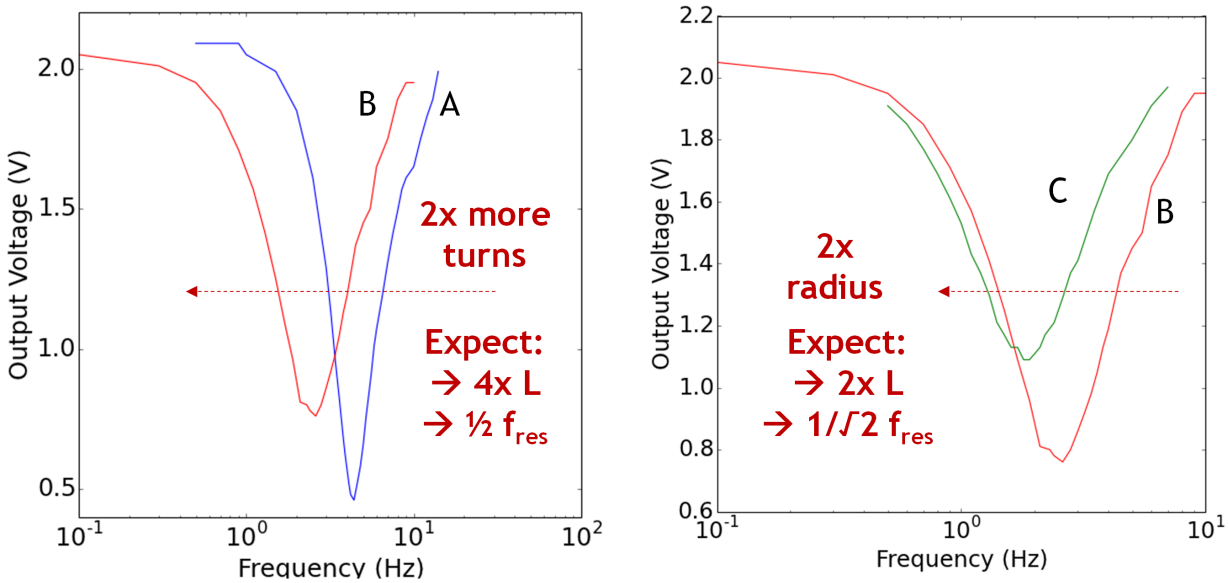


Figure 4.27: Patterning of Square Inductors



Inductor	Size	Number of turns	Resonant frequency	Extracted inductance	Series resistance	L/R_{ind}
A	4cm	9	4.1MHz	3uH	20 Ohms	1.5e-7
B	4cm	19	2.6MHz	14.5uH	130 Ohms	1.1e-7
C	8cm	19	1.9MHz	7.8uH	85 Ohms	1e-7

Figure 4.28: Measurement results for printed inductors scaling with number of turns and radius

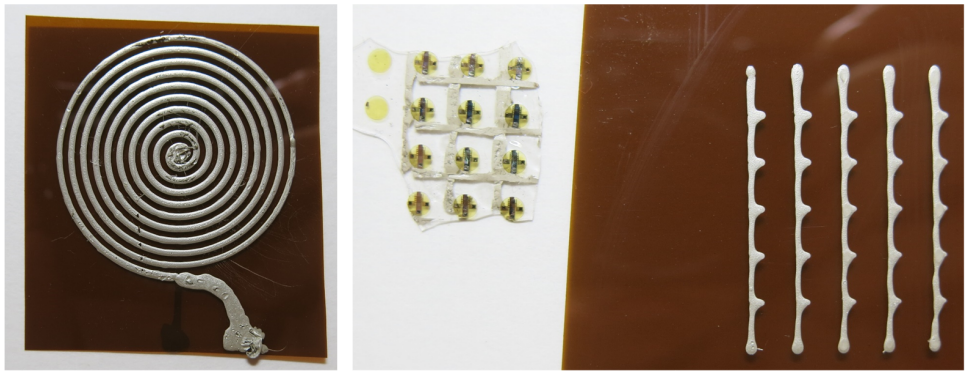


Figure 4.29: Demonstration of feasibility of circular inductors (left) and active matrix interconnect (right). The central image shows manually stencil-printed stretchable conductor interconnect on a PDMS substrate with rigid TFT islands

Chapter 5

Thin-film battery management system

5.1 Introduction

To exploit the highly promising sensing and actuation capabilities within large-area electronics in complete systems, integrated thin-film subsystems for continuous power-management will be required, by combining energy harvesting with local energy storage. This will allow self-powered systems to account for periods of diminished illumination of, for example, solar modules. In this chapter, we present a fully thin-film sheet that accomplishes this.

5.1.1 Thin-film energy storage

Commercial flexible thin-film lithium-ion (Li-ion) batteries [7] are used for energy storage. Batteries based on Li-ion technology are currently the dominant flexible energy-storage device [31]; these are based on a Lithium Cobalt Oxide cathode, a Lithium metal anode and a Lithium Phosphorus Oxynitride electrolyte. A typical structure of such a battery is shown in Figure 5.1.

As is typical with Li-ion battery technology, achieving safe and reliable charging/discharging is conditional on drawing charge from (or supplying charge to) the battery within a well-defined window of operating voltages. Failure to do so would result in permanent battery damage. Figure

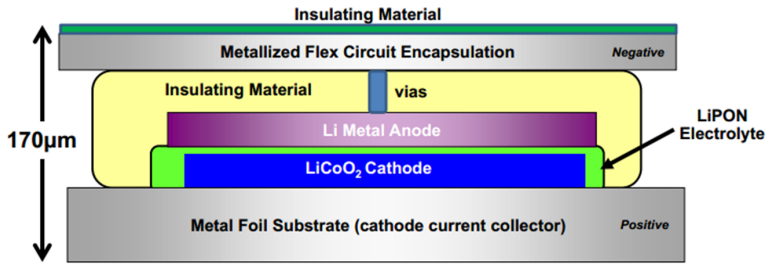


Figure 5.1: Structure of flexible Li-ion battery [7]

5.2 illustrates the permissible operating voltage range for the thin-film batteries used in the HMSD system, with an open-circuit (nominal output) voltage of 3.9V.

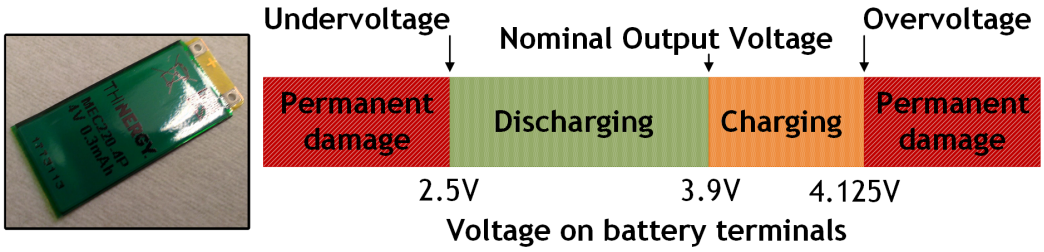


Figure 5.2: Permissible operating voltages for charging and discharging of thin-film Li-Ion batteries

During discharging, the nominal output voltage of the batteries is maintained until the batteries approach their fully-discharged state. At this point, the output voltage begins to drop rapidly as shown in Figure 5.3.

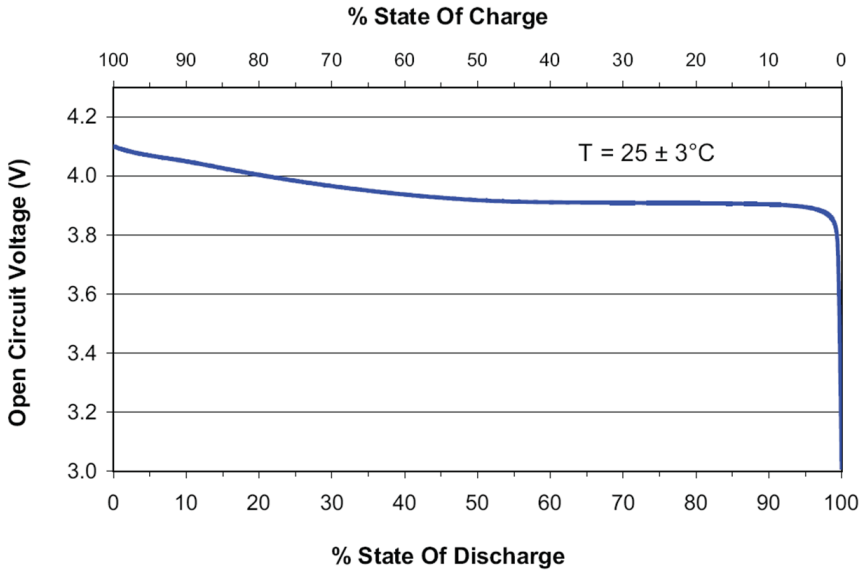


Figure 5.3: Manufacturer's discharge curve of the Thinergy Li-ion battery [7]

A method of managing the power drawn from the batteries is thus required to ensure that once the battery reaches the under-voltage condition, any load is cut-off, preventing further discharge until the battery has been partly or fully recharged.

5.2 System overview

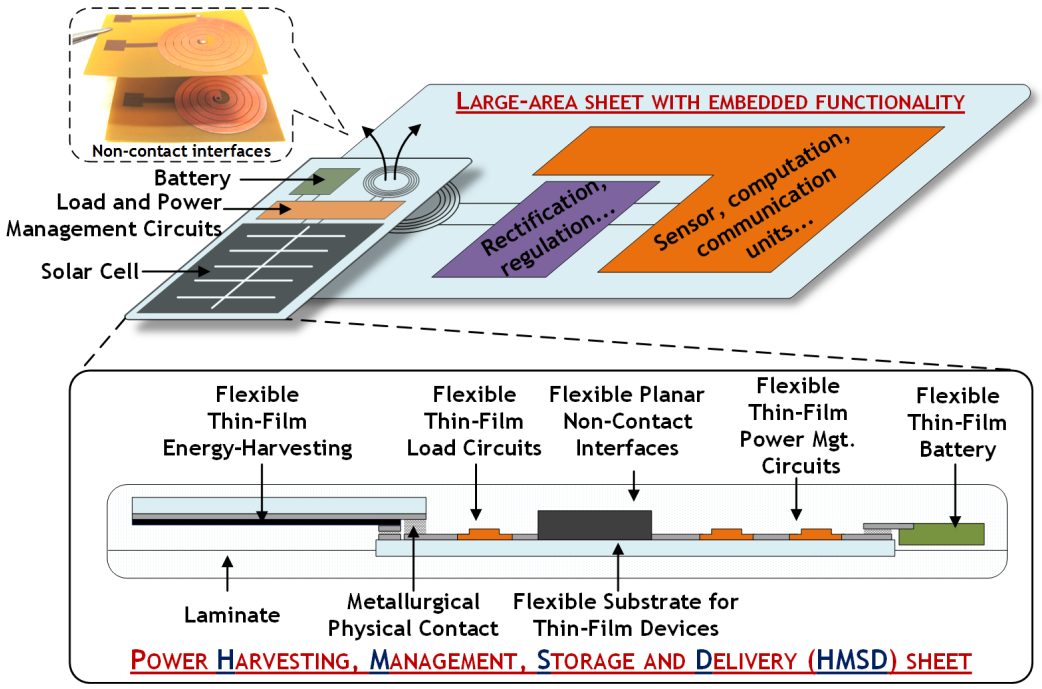


Figure 5.4: System concept and physical assembly of Power Harvesting, Management, Storage and Delivery (HMSD) sheet system components making use of sheet lamination

Figure 5.4 illustrates the system concept, showing the proposed power-harvesting, management, storage and delivery (HMSD) sheet for wireless power delivery to large-scale systems (e.g. a large-area sheet with embedded functionality).

Interfacing to general large-area sheets is simply achieved by placing the HMSD sheet onto a power-receiving surface without the need for complex metallurgical connections. The aim is a generalized and easy-to-integrate platform for powering various large-area sheets; a flexible HMSD sheet ensures that power delivery is not constrained by the physical form-factor of the large-area sheet. In addition to PV harvesters and power inverters for wireless power delivery, the HMSD sheet comprises a TFT-based subsystem for management of commercial, flexible, thin-film lithium-ion batteries, thus also enabling local energy storage and continuous powering of on-sheet loads.