Strain Relaxation of SiGe on Compliant BPSG and Its Applications

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Abstract

We have studied the strain relaxation of SiGe on compliant borophosphosilicate glass (BPSG). Through modeling and experiments it has been shown that strain relaxation in the SiGe film can be induced by lateral expansion and buckling of the SiGe film. Stress balance of a bilayer on the compliant oxide has been observed for the first time. Geometry has been successfully utilized to realize uniaxial and orthorhombic strain. Buckling on large islands can be suppressed using stress balance of SiGe/Si or SiGe/SiO_2 bilayers. Fully-relaxed, flat SiGe islands with edge width as large as 100 μm have been achieved.

We have explored two methods to achieve high Ge-content relaxed SiGe films: SiGe oxidation and stress balance of SiGe films on BPSG. We have demonstrated Ge content as high as 70%. Strain resulting from the increased Ge content has been found to relax by lateral expansion, which makes dislocations unnecessary.

To achieve tensile silicon, stress balance between Si and SiGe layers has been employed. Ten nm strained silicon on BPSG with low doping levels has been obtained by removing the top SiGe film after stress balance. Fully-depleted strained-Si n-channel MOSFETs on BPSG were fabricated and strain-induced electron mobility enhancement of 50% has been observed. The absence of SiGe in the final device structure overcomes any potential process or device drawbacks due to existence of a SiGe layer.

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Finally, I thank my wife, Yan Zhou, and my parents for their understanding and support. Nothing can be accomplished without their steadfast support.

Contents

Chapter 1

Introduction

1.1 Motivation

As CMOS technology enters the sub-100 nm regime, device scaling, which has been used to improve device performance for more than a decade, faces a formidable difficulty. Other measures for enhancing device performance have been under intensive investigation, among which the use of relaxed SiGe alloy in advanced CMOS is of particular interest for its easy integration with current silicon integrated circuit technology. Epitaxial Si, when commensurately grown on relaxed SiGe with a larger in-plane lattice constant than silicon, is under tension and has higher hole and electron mobility than that in unstrained silicon [1,2]. High-quality germanium can be deposited on relaxed SiGe and this has been used to fabricate Ge-channel MOSFETs for ultra-high hole mobility [3], which is usually lower than electron mobility and is a bottleneck in CMOS circuits. Besides the CMOS application, relaxed SiGe enables integration of III-V semiconductor with Si technology [4]. This finds many applications in opto-electronics.

The conventional route to relaxed SiGe relies on the formation of misfit dislocations in thick SiGe layers grown on silicon substrates. Even though the density of resulting threading dislocations has been reduced to ~10^5 cm^{-2} in compositionally graded SiGe layers, this number needs to be further improved to meet application demands. In addition, this lowered defect density comes at the expense of a very thick SiGe layer (a few microns), posing difficulty for high throughput.

To address these adverse effects associated with the conventional method, a compliant substrate scheme is used to produce thin (~30 nm), high-quality (inherently dislocation-free), relaxed SiGe. Strained SiGe, transferred onto compliant borophosphosilicate glass (BPSG) by wafer bonding and Smart-cut® processes, is patterned into islands before relaxation. The strain relaxation of SiGe islands on compliant BPSG is studied using both experiments and modeling. Lateral expansion and buckling contribute to strain relief of SiGe islands on BPSG. Stress balance between

SiGe/Si on BPSG has been observed, which is the first reported stress balance on compliant substrates. Defect etch on relaxed SiGe/BPSG has verified that dislocations don't play a role in the strain relaxation and that the relaxed films are of high quality.

Buckling of SiGe islands on BPSG turns SiGe rough and even results in fractures in islands larger than 80 micron in edge width. Large flat islands, indispensable as a platform for electronic devices, have been obtained by buckling-suppressing cap layers. Silicon and silicon dioxide have been tested as the capping layers. Flat SiGe islands as large as 200 micron have been achieved using SiO_2 caps and cap thinning.

To realize high germanium content, required for Ge-channel MOSFETs and integration of III-V semiconductors with silicon, two approaches are examined. Both rely on lateral expansion, not dislocation formation, to increase the in-plane lattice constant. They promise to yield high-quality, high germanium content, relaxed SiGe films.

Fully depleted strained-Si-on-insulator (SSOI) n-channel MOSFETs are fabricated. The absence of SiGe in the final structures provides numerous benefits in processing. This method has fewer fabrication steps than other SiGe-free SSOI approaches.

1.2 Thesis outline

Chapter 2 introduces SiGe alloy and SiGe/Si heterostructures. The band structure of SiGe/Si and electron transport in strained silicon are discussed.

In Chapter 3, the fabrication of SiGe on borophosphosilicate glass (BPSG) is detailed. The strain relaxation of SiGe on BPSG through lateral expansion and buckling is briefly discussed. Defect etching is carried out on strain-relaxed SiGe on BPSG to investigate dislocations.

Chapter 4 focuses on study of lateral expansion of SiGe islands on BPSG. Modeling and experiments are used to understand lateral expansion of SiGe islands. Stress balance, enabled by coherent lateral expansion of bi-layer structures, is observed in SiGe/Si and $SiGe/SiO_2$. Stress balance is the key technique for applications discussed in later chapters.

Chapter 5 presents experimental results on SiGe buckling and buckling suppression. The buckling of a single SiGe layer on BPSG is first examined and compared to the buckling theory. Various techniques are demonstrated in avoiding buckling in single

layer. A bi-layer structure, formed by silicon or silicon dioxide, is then investigated to suppress buckling.

In Chapter 6, high germanium content SiGe on BPSG is achieved through two methods. First, the combination of SiGe oxidation and BPSG allows germanium content to be enhanced while relaxing strain through lateral expansion. The observation of a super viscous silicon dioxide layer during SiGe oxidation is explained. Second, stress balance in layers with different germanium contents is successfully used to increase the in-plane lattice constant.

Chapter 7 addresses the device applications of stress balance on BPSG. Strained Si on insulator (BPSG) is fabricated using stress balance of SiGe/Si followed by selective SiGe removal. Adverse dopant diffusion from BPSG in high temperature processes is completely blocked by a silicon nitride diffusion barrier. Fully depleted strained-Si n-channel MOSFETs are demonstrated and characterized.

Chapter 8 summarizes the contributions of this thesis and points out possible directions for future work.

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Chapter 2

SiGe/Si Heterostructures

2.1 Introduction to SiGe/Si lattice structures

Both silicon and germanium are column IV elements and they can randomly mix in a diamond lattice structure, forming $Si_{1-x}Ge_x$ alloys. As the lattice constant of pure germanium (a_{Ge} = 5.658Å) is larger than that of pure silicon (a_{Si} = 5.428Å), the lattice constant of SiGe can be, based on linear interpolation between a_{Si} and a_{Ge}, estimated as follows:

$$a_{SiGe}(x) = a_{Si} + (a_{Ge} - a_{Si})x, \tag{2.1}$$

where x represents the fraction of atoms which are germanium.

High-quality SiGe substrates are not available, as a result of various difficulties in growing bulk SiGe crystals [1]. SiGe alloys, in the form of thin films, are usually formed on silicon substrates by chemical vapor deposition (CVD) or molecular beam epitaxy (MBE). The lattice constant of relaxed SiGe alloys is larger than that of silicon substrates. When the SiGe film is thin, its lattice structure is compressed laterally to fit with relaxed silicon (Fig. 2.1(a)): the in-plane lattice constant $a_{\|}$ is the same as silicon and the in-plane strain are given by $\varepsilon_{11} = \varepsilon_{22} = \frac{a_{Si} - a_{siGe}(x)}{a_{SiGe}(x)}$. The strain along the growth direction ε_{33} can be extracted from the following linear stress-strain equation:

$$\begin{pmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{12} \\ \sigma_{13} \\ \sigma_{23} \end{pmatrix} = \begin{pmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{44} \end{pmatrix} \begin{pmatrix} \varepsilon_{11} \\ \varepsilon_{22} \\ \varepsilon_{33} \\ \varepsilon_{12} \\ \varepsilon_{13} \\ \varepsilon_{23} \end{pmatrix} \tag{2.2}$$

where c is the elastic tensor; σ is the stress tensor; ε is the strain tensor; the indices 11, 22, and 33 denote components xx, yy, and zz, respectively; the indices 12, 13, and 23 are the shear components yz, zx, and xy respectively. Note that x, y, and z are aligned along

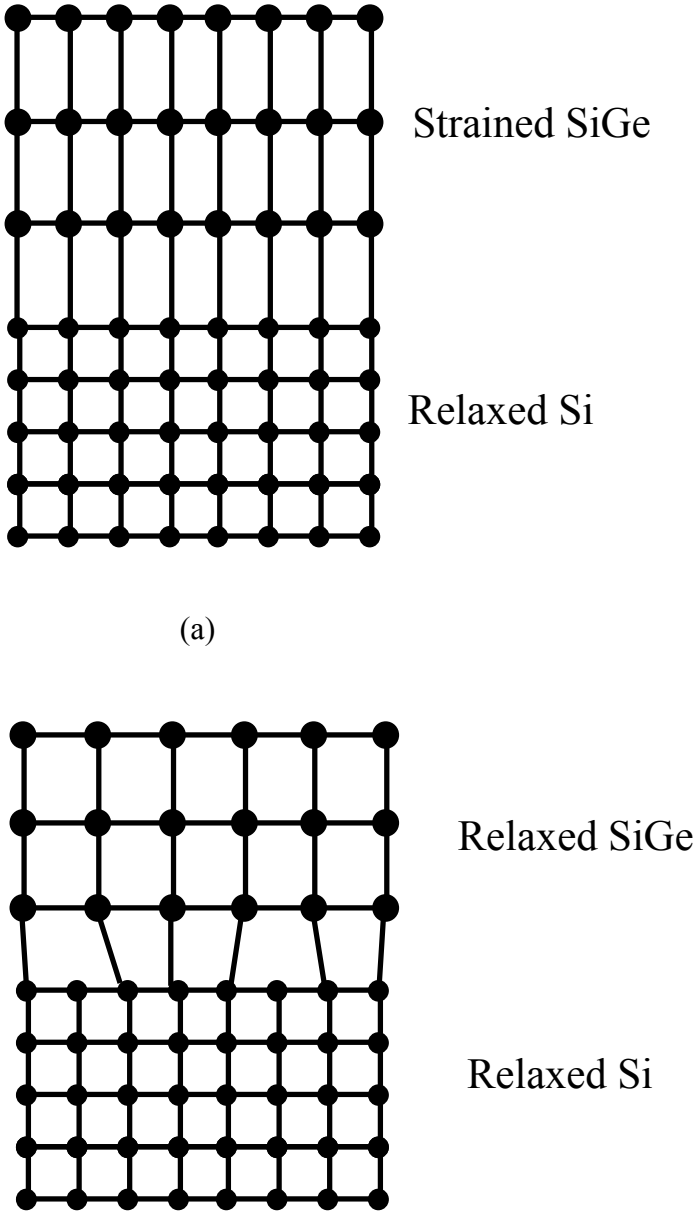


Figure 2.1: Schematic lattice structure of SiGe on relaxed silicon substrates: (a) when the SiGe layer is thin, SiGe is commensurately deposited on the silicon substrate and under compressive strain, with the in-plane lattice constant the same for both materials; (b) when the SiGe layer is thick, SiGe is relaxed by misfit dislocations at the SiGe/Si interface.

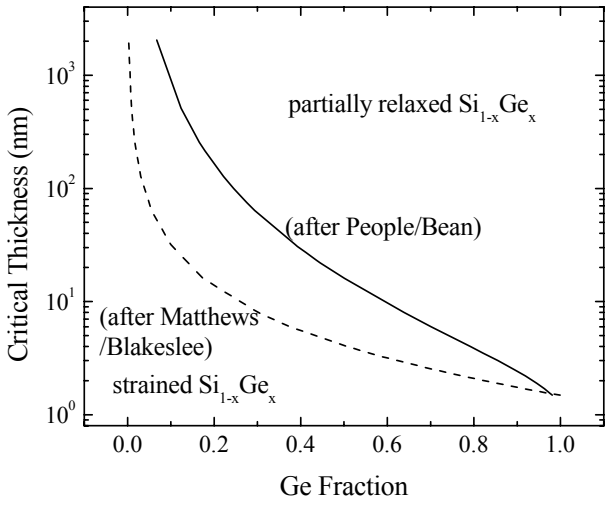


Fig. 2.2: Critical thickness of pseudomorphic $Si_{1-x}Ge_x$ grown on (100) silicon substrates as a function of germanium concentration. Dashed line represents equilibrium critical thickness [2]. Solid line shows metastable thickness [3].

the [100], [010], and [001] crystal directions. Solving Eqn. 2.2 with the condition of zero stress in the growth direction ($\sigma_{33} = 0$) leads to

$$\varepsilon_{33} = -\frac{2c_{12}}{c_{11}}\varepsilon_{11} \qquad (2.3)$$

When the strain energy stored in the compressively strained SiGe is not enough to generate dislocations, the SiGe layer and the relaxed Si substrate remain coherent and the SiGe layer is pseudomorphic. When the SiGe film exceeds a certain thickness, it is energetically favorable to form dislocations as the released strain energy is more than that needed for dislocation formation (Fig. 2.1(b)). The equilibrium critical thickness, beyond which dislocations start to form, has been modeled by Matthews and Blakeslee (Fig. 2.2) [2]. Strained SiGe films of thickness less than the critical thickness remains pseudomorphic at all temperatures. In the case where no high temperature processes are involved, pseudomorphic SiGe films can be obtained well beyond the equilibrium critical thickness, being in a meta-stable state (Fig. 2.2) [3]. But any exposure to high temperatures will relax the strain and introduce dislocations.

When a thin silicon film is deposited pseudomorphically on a thick relaxed SiGe layer, the in-plane lattice constant of silicon is stretched and tensilely-strained silicon is formed (Fig. 2.3(a)). There is also a limit on the thickness of the pseudomorphic silicon on relaxed SiGe. Partially relaxed silicon will result when its thickness is large enough that dislocations are energetically favorable to occur to reduce the tensile strain (Fig. 2.3(b)).

Depending on the requirements of individual electronic device applications, strain in SiGe and Si layers should be relaxed, compressive, or tensile. For example, strained SiGe is required for the base of hetereojunction bipolar transistors (HBTs), while relaxed SiGe is needed to form tensile silicon to enhance electron mobility for MOSFET applications

2.2 Band structures of SiGe/Si heterostructures

2.2.1 Bandgap and band extrema in relaxed layers

The band structure of SiGe/Si heterojunctions is important for understanding their applications and limitations. Both the germanium fraction and strain can alter the band structure significantly. Silicon and germanium are both indirect bandgap materials. The conduction band in unstrained silicon and unstrained SiGe up to x = 0.80 has six degenerate minima at the Δ points in the Brillouin zone. The four Δ-point valleys perpendicular to growth direction and the two Δ-point valleys parallel to growth direction are referred to as Δ_4-minima and Δ_2-minima, respectively. The valence band maximum is located at the Γ point, which includes degenerate heavy holes (HH) and light holes (LH).

The bandgap of relaxed SiGe alloys has been measured using optical absorption by Braunstein [4] (Fig. 2.4). The energy bandgap of relaxed SiGe narrows as the germanium fraction increases, in agreement with the change of the bandgap from 1.12 eV for pure silicon to 0.66 eV for pure germanium. The rapid decrease of bandgap for germanium content larger than 80% stems from the transition of the conduction band from Si-like with minima at the Δ points in the Brillouin zone to Ge-like with minima at the L points.

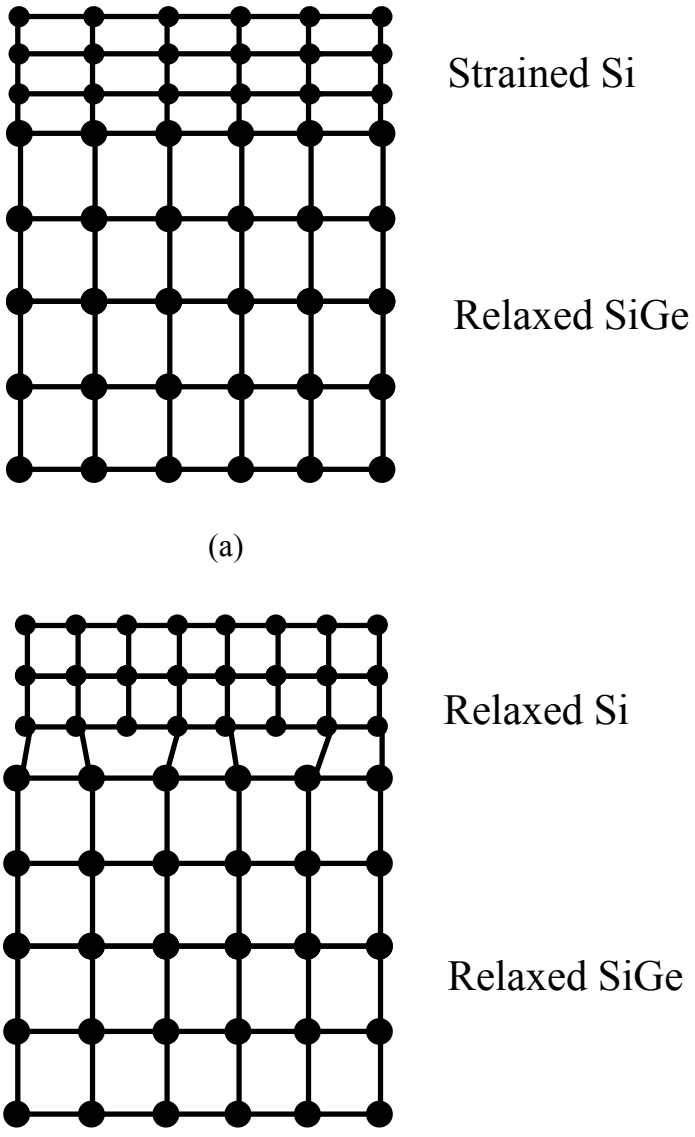


Figure 2.3: Schematic lattice structure of Si on relaxed SiGe: (a) when the Si layer is thin, it is pseudomorphic and under tensile strain, with the in-plane lattice constant the same for both materials; (b) when the Si layer is thick, Si is relaxed by dislocations.

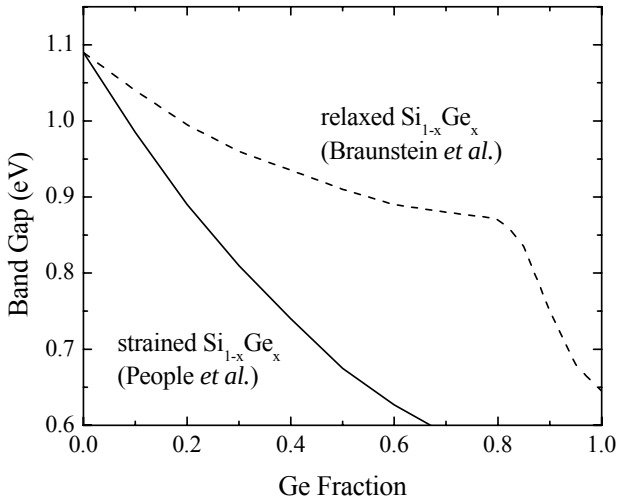


Figure 2.4: Band gap of SiGe (both relaxed and strained) as a function of germanium content [4,7].

2.2.2 Band alignments

a. Pseudomorphic $Si_{1-x}Ge_x$ on relaxed Si(100) substrates

When SiGe films are commensurately grown on (001) silicon substrates, the SiGe films are under compressive strain. The six-fold degeneracy at the Δ points is lifted: the Δ_2-minima ([001] and $[00\bar{1}]$) go up and the Δ_4-minima become the CB minima. The two-fold degeneracy in the valence band (VB) at the Γ points splits with the heavy-hole band being the new VB maximum. The resulting bandgap (People et al. [5]), as shown in Fig. 2.4, is smaller than the relaxed SiGe and it decreases more rapidly with increasing germanium content.

The band alignment determines which type of carriers can be confined and in which material they will be confined. In the case of strained $Si_{1-x}Ge_x$ on Si(100) substrates, most of the band offset stems from the discontinuity ΔE_v in the valence band edge [6,7] :

$$\Delta E_V = 0.74x \text{ (eV)}. \qquad (2.4)$$

With the valence band edge higher in strained SiGe than in Si substrates, strained SiGe is often utilized to create a quantum well to confine holes. This has found its way into applications such as modulation-doped PFETs [8]. The conduction band offset is small

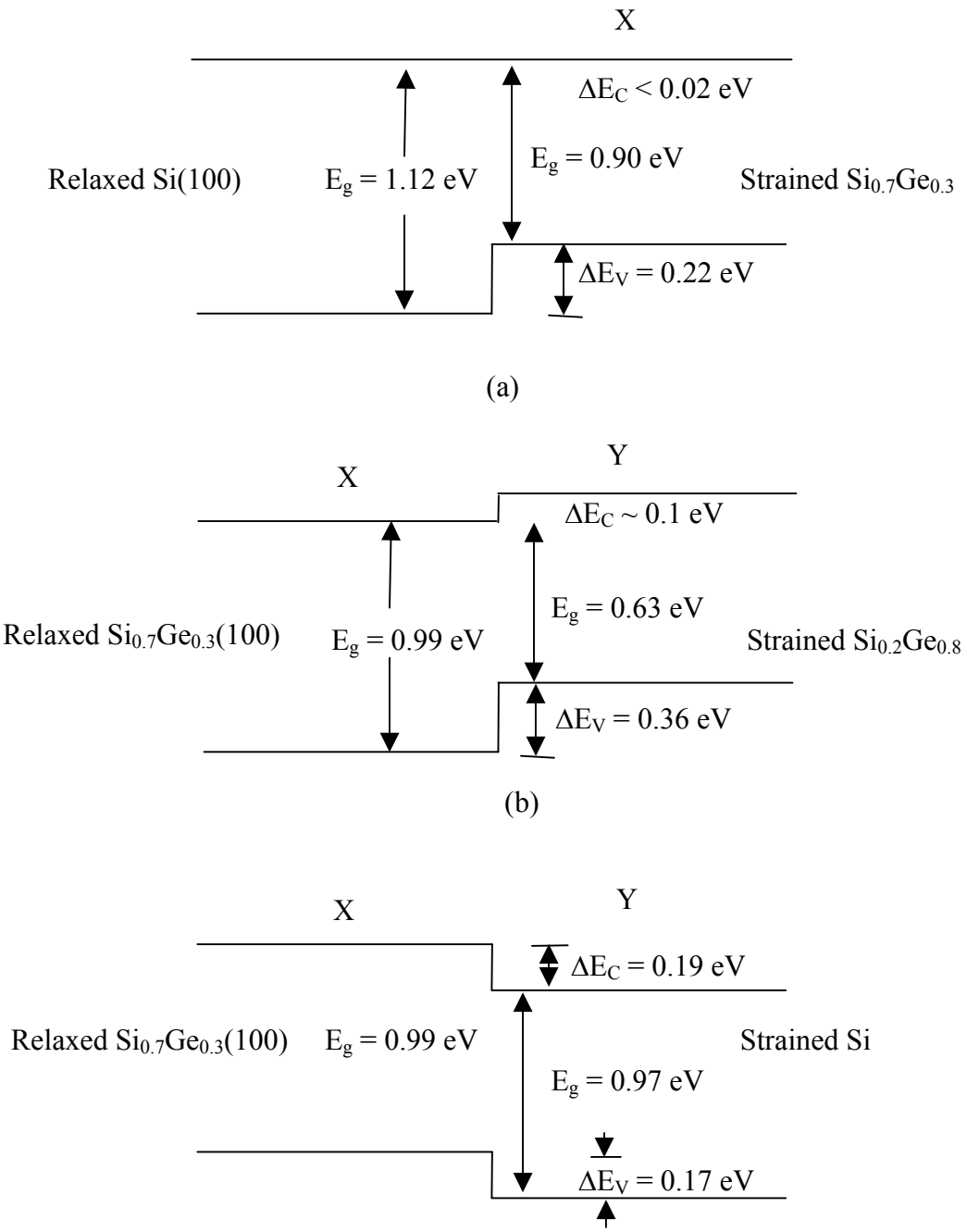


Figure 2.5: Band alignments of $Si_{1-x}Ge_x/Si_{1-y}Ge_y$ hetetrostructures for various configurations [11]: (a) strained $Si_{0.7}Ge_{0.3}$ on relaxed Si(100), (b) Strained $Si_{0.2}Ge_{0.8}$ on relaxed $Si_{0.7}Ge_{0.3}$(100), and (c) strained Si on relaxed $Si_{0.7}Ge_{0.3}$(100).

and this configuration usually is not used in device applications. Figure 2.5(a) shows the band alignment of commensurately strained $Si_{0.7}Ge_{0.3}$ on relaxed Si(100) (commonly used in the HBT base region and for two-dimensional hole gas (2DHG)) [9] .

b. Pseudomorphic $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$(100) substrates

The band structure of relaxed $Si_{1-x}Ge_x$ as a function of germanium content is shown in Fig. 2.6, which is important for understanding the band lineup in SiGe layers with different germanium contents. In relaxed $Si_{1-x}Ge_x$, the conduction band minima at the Δ points remain degenerate, while the splitting between the heavy and light holes grows as the germanium content increases. The valence band edge offset for commensurately strained $Si_{1-y}Ge_y$ grown on relaxed $Si_{1-x}Ge_x$ ($y > x$), extracted using Eqn. 2.4 along with the work done by Van de Walle [10], is expressed as follows:

$$\Delta E_V = (0.74 - 0.53x)(y-x) \text{ (eV)}. \qquad (2.5)$$

Figure 2.5(b) shows the band alignment of strained $Si_{0.2}Ge_{0.8}$ on relaxed $Si_{0.7}Ge_{0.3}$, commonly used for high mobility PFET (Fig. 2.7(b)) [9].

c. Pseudomorphic Si on relaxed $Si_{1-x}Ge_x$ substrates

When pseudomorphic silicon is grown on relaxed $Si_{1-x}Ge_x$, the tensile strain in silicon shifts its band structure. The Δ_2-minima are lowered and become the conduction band edge. The conduction band offset can be calculated from ΔE_V [7], strained-Si bandgap $E_{g\_strained\text{-}Si}$ [7], and the relaxed-SiGe bandgap $E_{g\_relaxed\text{-}SiGe}$ [4] as follows:

$$\Delta E_C = \Delta E_V + E_{g\_strained\text{-}Si} - E_{g\_relaxed\text{-}SiGe} = 0.64x \text{ (eV)} \qquad (2.6)$$

The ΔE_C predicted by Eqn. 2.6 is in good agreement with the theory from Ref. [7] when the germanium content is less than 40%. For high germanium contents ($x > 0.4$), the theory from Ref. [7] predicts a peak in ΔE_C around $x = 0.45$. The experimental ΔE_V data from Ref. [11] agrees with the theory when $x < 0.4$ [7]. The conduction band and valence band offsets are plotted in Fig. 2.7 [11]. As the conduction band edge is lower in strained Si than in relaxed SiGe, strained silicon is often used as a quantum well to confine electrons, which is of special interest for modulation-doped NFETs. Figure 2.5(c) illustrates the band alignment of strained Si on relaxed $Si_{0.7}Ge_{0.3}$ (commonly used in 2DEG and NFETs).

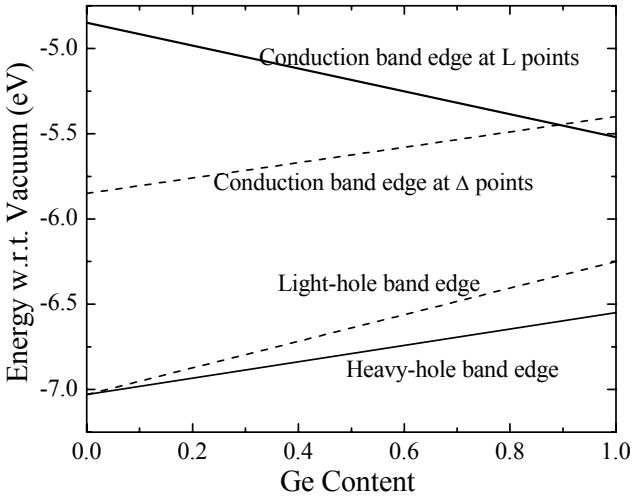


Figure 2.6: Energies of band extrema of relaxed SiGe based on linear interpolation between bulk silicon and bulk germanium [9].

2.3 Electron transport in tensile silicon

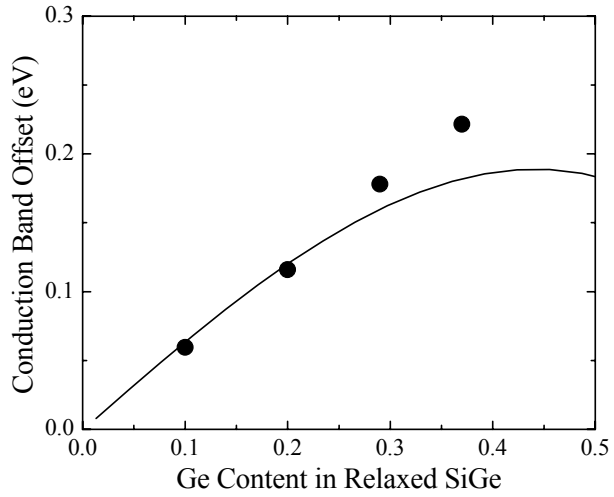
Mobility (μ) is an important parameter of electron transport in semiconductors and can be expressed in low fields as:

$$\mu = \frac{q\tau}{m^*} \tag{2.7}$$

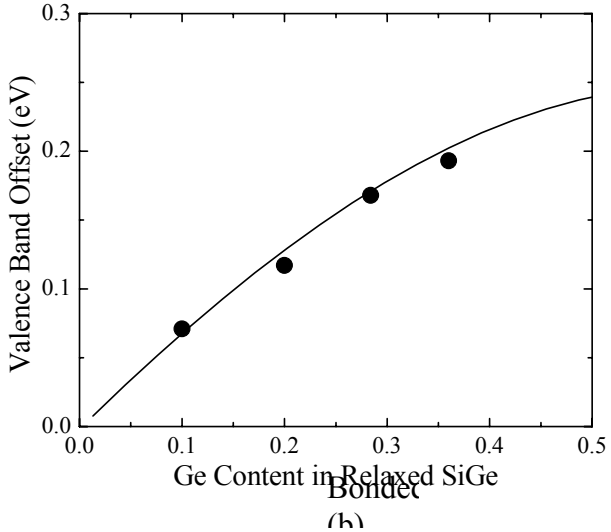
where q is the electron charge, τ is the momentum relaxation time and m^* is the effective electron mass. The momentum relaxation involves multiple scattering mechanisms, whose weight in the overall relaxation time depends on doping concentration and varies with emperature and electrical field. The mobility can be treated as a collective effect of decoupled mobilities:

$$\frac{1}{\mu} = \frac{1}{\mu_{op}} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{ii}} + \frac{1}{\mu_{surf}}, \tag{2.8}$$

in which μ_{op} is optical phonon scattering mobility, μ_{ac} is acoustic phonon scattering mobility, μ_{ii} is ionized-impurity scattering mobility and μ_{surf} is surface charge/roughness scattering mobility. In the case of low doping concentration, the mobility is limited by phonon scattering when the carriers are not confined near a surface by large vertical electrical field.



(a)



(b)

Figure 2.7: Dependence of band offsets for commensurately strained Si/relaxed SiGe on germanium content: (a) conduction band edge offset and (b) valence band edge offset. The solid line is based on Ref. [7] and the symbols are based on the MOS C-V data of Ref. [10].

The mobility enhancement observed in tensile silicon compared to that in relaxed silicon is of great interest for application in high performance CMOS. The mechanism of electron mobility enhancement in tensile silicon is well understood. Figure 2.8(a) shows the constant energy contour in k-space at conduction minima for unstrained silicon [12]. For each individual valley, the effective mass along the axis (the longitudinal effective mass m_L) is $0.92m_e$ while the effective mass perpendicular to the axis (the transverse effective mass m_T) is $0.19m_e$. As a result of the cubic symmetry and the six-fold degenerate conduction minima, the conductivity effective mass is isotropic and can be related to m_L and m_T as follows:

$$\frac{1}{m^*} = \frac{1}{3}\left(\frac{1}{m_L} + \frac{2}{m_T}\right) = \frac{1}{0.26m_e}. \qquad (2.9)$$

As biaxial compressive strain is applied in silicon (in x-y plane), the out-of-plane conduction minima are lowered and electrons preferentially populate in the Δ_2-minima. For sufficiently large splitting so that all electrons are in the lower minima, the in-plane transport is solely dependenton the transverse effective mass, and therefore the conductivity effective mass for the in-plane transport is

$$\frac{1}{m^*} = \frac{1}{m_T} = \frac{1}{0.19m_e}. \qquad (2.10)$$

Thus the strain decreases the conductivity effective mass for in-place transport from $0.26m_e$ to $0.19m_e$. Besides decreasing the in-plane effective mass, the lifting of degeneracy for the conduction band minima helps increase mobility by reducing inter-valley phonon scattering. The mobility enhancement factor as a function of the strain calculated by Takagi et al [13] is plotted in Fig 2.9, which assumes room temperature and low doping levels. Once the strain is increased from zero, the number of low mobility electrons residing in the Δ_4-minima diminishes, leading to a rapid increase of mobility enhancement. When the strain exceeds 0.8%, nearly all electrons are shifted to Δ_2-minima, and the increase in mobility over the unstrained value is 70%. Any additional increase in strain does not contribute to mobility enhancement, resulting in the saturation of the mobility enhancement. The upper axis shows the germanium fraction of the $Si_{1-x}Ge_x$ substrate on which the strain silicon is commensurately grown. A strain level of 0.8% requires a germanium fraction in the substrate of 20%. Because devices are often

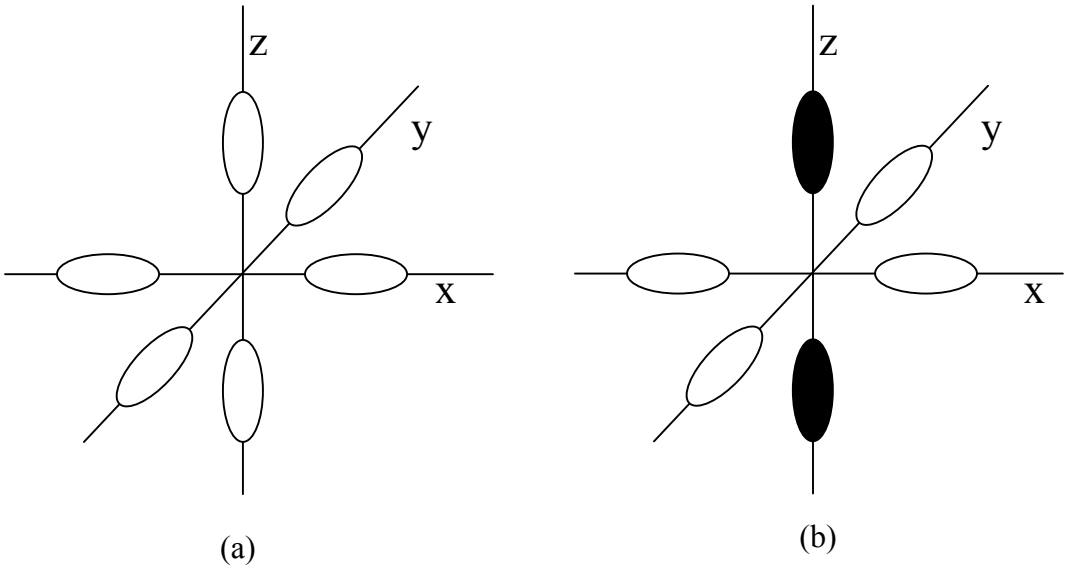


Figure 2.8: Constant-energy surfaces of the conduction band minima in silicon. (a) The conduction band minima are six-fold degenerate when there is no strain. (b) The two conduction band minima along [001] directions are pulled down when silicon is under tensile strain in x-y plane. The six-fold degeneracy is lifted and the Δ-minima are split into Δ_2 and Δ_4-minima [12].

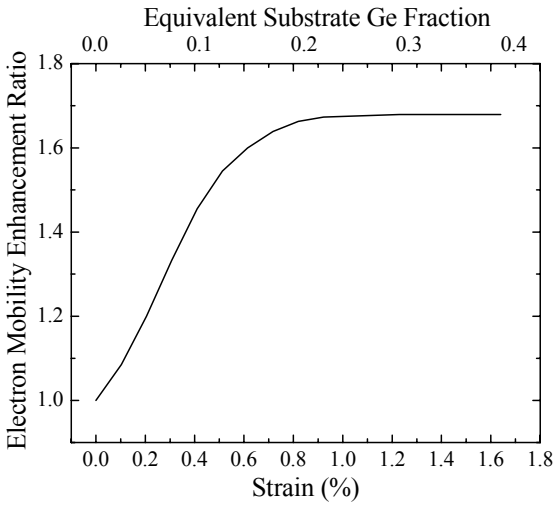


Figure 2.9: Calculated electron mobility enhancement ratio for lateral transport in silicon as a function of biaxially compressive strain [13].

significantly hotter than room temperature during operations, a large amount of the work in this thesis will be done with x=0.3 in the relaxed substrate.

2.4 Summary

Two critical properties of SiGe/Si heterostructures, the atomic arrangements and the band structures, have been reviewed. The strain stemming from the lattice mismatch between SiGe and Si can cause defect formation in SiGe and Si films above critical thickness, thus imposing a limit on SiGe/Si designs. However, the changes in band-structures induced by strain in Si and SiGe offer various opportunities for different device applications. In the next chapter, a novel approach will be presented for manipulating stain without defect formation, which can be leveraged for device implementation.

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Chapter 3

Overview of the Strain Relaxation of SiGe on Compliant Borophosphosilicate Glass (BPSG)

Conventionally, relaxed $Si_{1-x}Ge_x$ has been obtained by growing compositionally graded $Si_{1-x}Ge_x$ much thicker than critical thickness so as to introduce dislocations to relax strain in the $Si_{1-x}Ge_x$ [1]. Although the density of dislocations in relaxed SiGe by this approach has been greatly reduced over time, the control of dislocations is still challenging and requires optimization for dislocation suppression. In addition, the thick $Si_{1-x}Ge_x$ films needed for strain relaxation through dislocations (on the order of a few microns, with a typical grading rate of 10% germanium increment per 1 μm) poses a serious bottleneck for throughput [1, 2].

The work in this thesis is focused on the realization of high-quality relaxed SiGe on compliant BPSG. This chapter serves as an introduction to the relaxation of the strain in SiGe on compliant BPSG. First, concepts of compliant substrates will be reviewed and explained. The term "compliant substrate" refers to a substrate that allows a strained layer to relax with a minimum level of defect creation in this layer. The process flow of strained SiGe on BPSG, the compliant material in this work, will then be discussed in detail, including wafer bonding and layer transfer. Two strain relaxation mechanisms, lateral expansion and buckling (film roughening), will be briefly presented and some preliminary experimental results will be discussed. Finally, the film quality of relaxed SiGe on BPSG has been studied using defect etching.

3.1 Introduction to compliant substrates

Compliant substrates have been under intensive study since the concept was proposed in 1991 as a means to achieve high quality hetero-epitaxial thin films in cases where lattice-matched substrates are not available [3]. The concept of a "compliant substrate" is to utilize the substrate material to adopt the lattice-mismatched films in such

a ways so that misfit dislocations need not to be generated, or that their generation will not affect the hetero-epitaxial films. In conventional lattice-mismatched heterostructures, thick substrates cannot allow strain relaxation in epitaxial thin films through substrate deformation. The thickness of high-quality epilayers is limited to critical thickness [4], beyond which dislocations are introduced to release strain.

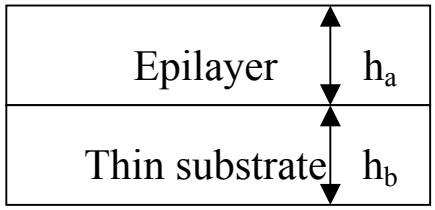
There have been various ways to realize compliant substrates. The 1st method is to employ a substrate with a small thickness comparable to that of the top epilayer, as shown in Fig. 3.1(a). The strain energy is distributed between the substrate and epilayer so that the total strain energy is smaller compared to that in a bulk-substrate case, resulting in a significant increase in critical thickness. In the extreme case where there is no substrate (the thickness of the substrate is zero), the epilayer becomes effectively free standing and the strain energy in it can be fully released regardless of its thickness. The effective equilibrium critical thickness (t_{eff}) for an epilayer on thin substrates can be related to the critical thickness (t_c) on infinitely thick substrates [3]:

$$\frac{1}{t_{eff}} = \frac{1}{t_c} - \frac{1}{h_b}, \qquad (3.1)$$

where h_b is the substrate thickness. Figure 3.1(b) plots the effective critical thickness as a function of the substrate thickness. Note that the effective critical thickness become infinite when the substrate thickness is smaller than the critical thickness on bulk substrate, in which case the roles of substrate and epilayer are swapped, and substrate can be deformed freely by the top epilayer.

A 2nd approach is an interface that allows top layers to easily slide or move. For example, dislocation-free $In_{0.35}Ga_{0.65}P$ (~1% stain) with a thickness of 300 nm, thirty times the equilibrium critical thickness on rigid bulk substrates, has been successfully grown on a 10-nm GaAs epi-seed layer transferred at a rotated angle onto a GaAs substrate [5].

A 3rd compliant substrate method utilizes soft materials. When the strained semiconductor layers are transferred onto a soft substrate, the soft substrate allows the strained layers to expand or shrink laterally to release strain without dislocations. This thesis pursues this approach using borophosphosilicate glass (BPSG) as the “soft” layer, because its viscosity drops at relatively low temperature allowing it to flow.



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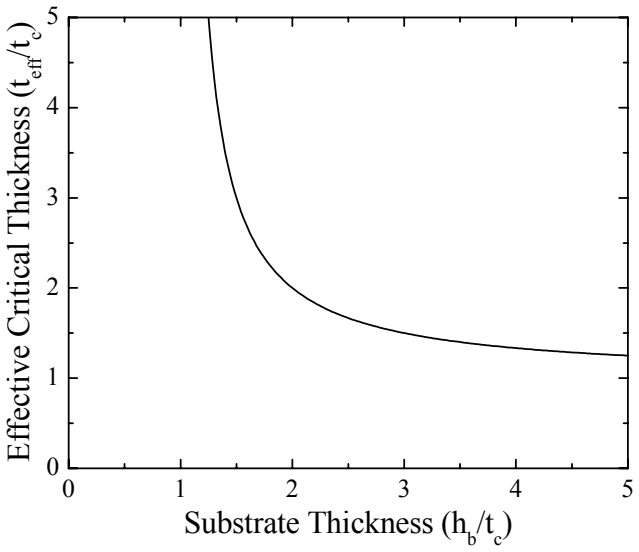


(b)

Figure 3.1: (a) Schematic of epilayer A grown on a thin substrate. (b) Dependence of the effective critical thickness (t_{eff}) on the substrate thickness (h_b). Both axes are normalized to the critical thickness for an infinitely thick substrate (t_c) [3].

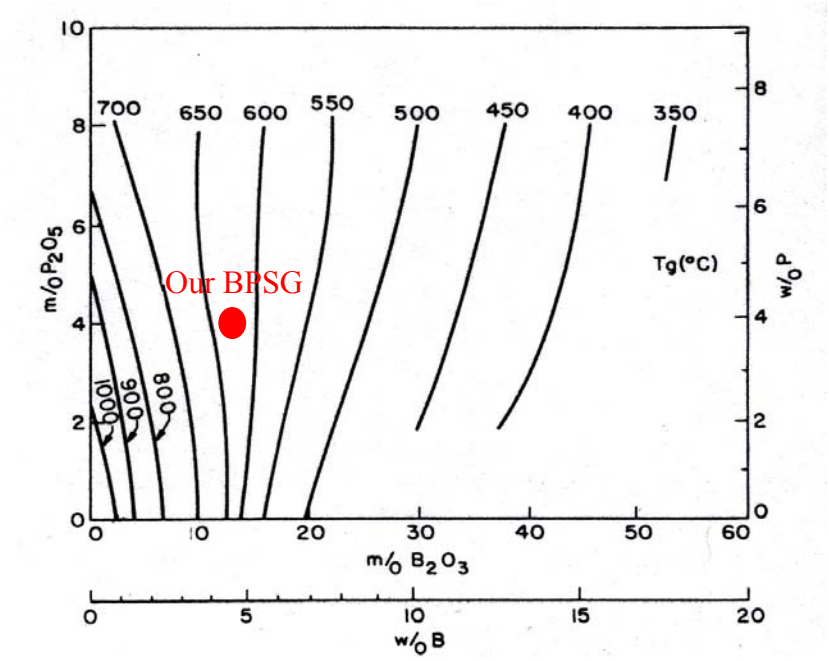
The rest of this chapter will serve as an introduction to SiGe on compliant BPSG. The fabrication of strained SiGe on BPSG will be discussed in the next section. Two strain-measurement techniques will be described in the 3rd section. Some preliminary studies on strain relaxation of SiGe on BPSG will be briefly presented. In the last section, film quality after strain relaxation is investigated using a defect-etch technique.

3.2 Strained SiGe on BPSG

3.2.1 Properties of BPSG

Borophosphosilicate glass (BPSG), a ternary oxide system B_2O_3-P_2O_5-SiO_2, is widely used in the fabrication of integrated circuits [6]. It can be produced by chemical vapor deposition with precursors SiH_4, B_2H_6, PH_3, and O_2/N_2. Since BPSG is viscous at relatively low temperatures, it is used to form tapered contours over steep steps of oxide and polycrystalline silicon in the device topography. This is imperative to ensure continuity and maintenance of subsequently deposited metal-conductor interconnect lines used in integrated circuits.

The mechanism of the viscous flow of BPSG involves the breaking of oxide bonds. The melting points of the oxides parallel the variations in viscosity: SiO_2, 1710^{o}C; P_2O_5, 580^{o}C, B_2O_3, 450^{o}C [7]. The linked-ring structure of B_2O_3 is probably the reason for the low viscosity of this oxide, since the bonds between rings are expectedly weaker than those within the rings [7]. The P_2O_5 network contains sheets of PO_4 tetrahedra where each tetrahedron is bonded to three others instead of four as for SiO_2, resulting in a much lower viscosity than that of SiO_2 [7]. When forming the BPSG, the mixed oxides have broken the silica network-forming lattice resulting in local distortions of the structure and consequently a lower viscosity [7]. The glass transition temperature T_g occurs in all oxide glasses at a viscosity of 10^{12} N*sec/m^2. Figure 3.2(a) shows the glass transition isotherms of BPSG for different boron and phosphorus concentrations [7]. When the boron weight percentage (wt%) is less than 4.5%, any increase of the phosphorus concentration will reduce the viscosity. Due to the hygroscopic character of B_2O_3 and P_2O_5, the boron wt% and phosphorus wt% should be less than 5% and 7%, respectively, to be relatively stable chemically during storage and exposure to a humid ambient. For the BPSG used in this thesis, we have chosen the boron and phosphorus wt% to be 4.4% and 4.1%, respectively.



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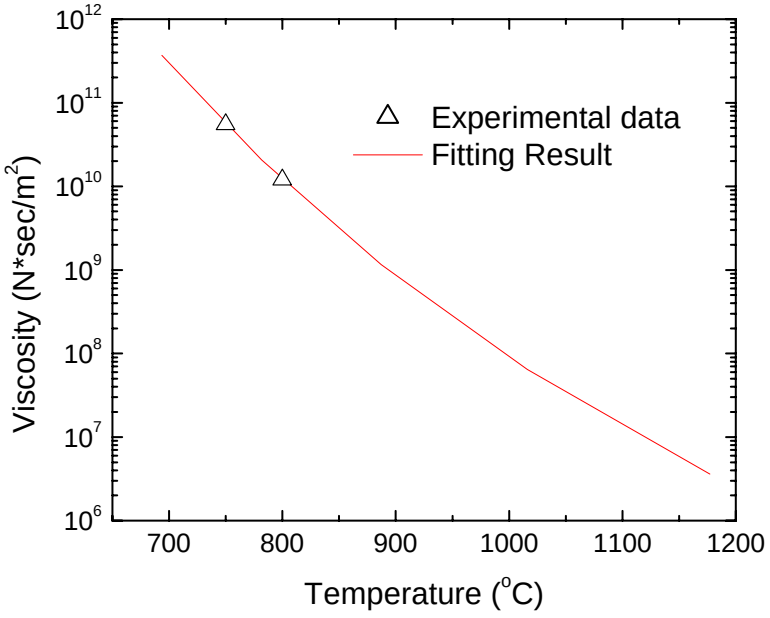


(b)

Figure 3.2: (a) Glass transition isotherms for the borophosphosilicate glass system [8]. The solid circle denotes the BPSG used in this thesis. (b) Temperature dependence of the viscosity of the BPSG used in this thesis. The solid line represents the fitting results based on an exponential decay function. The experimental data are described in Sec. 4.1.3.

The BPSG viscosity has an exponential dependence on temperature, which is plotted in Figure 3.2(b) for the BPSG used in this thesis.

3.2.2 Fabrication of strained SiGe on BPSG

A wafer with a psuedomorphic $Si_{0.7}Ge_{0.3}$ film on BPSG was fabricated using a "host" wafer and a "handle" Si(100) wafer. The basic fabrication process is shown in Fig. 3.3 [8]. The "host" wafer was a silicon wafer on top of which 30-nm commensurately strained $Si_{0.7}Ge_{0.3}$ was deposited followed by a 2-nm silicon cap. The 2-nm silicon cap was used to facilitate the wafer bonding process. The "handle" wafer was coated with 200-nm BPSG (4.4% B and 4.1% P by weight) by chemical vapor deposition (CVD). The boron and phosphorus contents in the BPSG have been chosen to minimize viscosity [7]. The "host" wafer was implanted with H_2^+ at an ion energy of 180 keV and a dose of 4.5×10^{16} cm^{-2} for a "Smart-cut®" process [9]. Both wafers were cleaned using a CO_2 snow jet to remove dust particles and UV ozone to remove organic residues. They were then turned to a hydrophilic surface condition by a treatment of $NH_4OH:H_2O_2:H_2O::1:1:4$ and $HCl:H_2O_2:H_2O::1:1:4$, and then bonded at room temperature. The bonded wafers were annealed at 250°C for four hours to enhance the bond strength and then at 550°C in nitrogen ambient to separate the top layer from the host substrate at the depth (~ 800 nm) of the hydrogen implant where micro-cavities form (Smart-cut®) [9]. We later confirmed that 550°C was low enough so no SiGe relaxation occurred. The remaining wafer had a stack of Si/SiGe/Si/BPSG on top and was dipped into KOH solution (10% by weight) at 80°C to selectively remove the approximately 800-nm silicon on top. The initial silicon cap was sandwiched between SiGe and BPSG films. Since ~1-nm silicon was removed from the thin silicon cap during the cleaning, the residual 1-nm cap (now between the SiGe and BPSG) had a minimal impact on the mechanic property, and it was ignored in subsequent mechanical analysis. Any oxide formed during the chemical treatment was also ignored.

The wafer was diced into samples of 1 cm x 1 cm and the continuous SiGe film was patterned into arrays of square islands of various sizes (from 10 to 200 μm) by reactive ion etching (RIE) in a SF_6/O_2 mixture (Appendix II). The bonding, splitting and KOH etching were performed by Karl Hobart at the Naval Research Lab [8]. The hydrogen

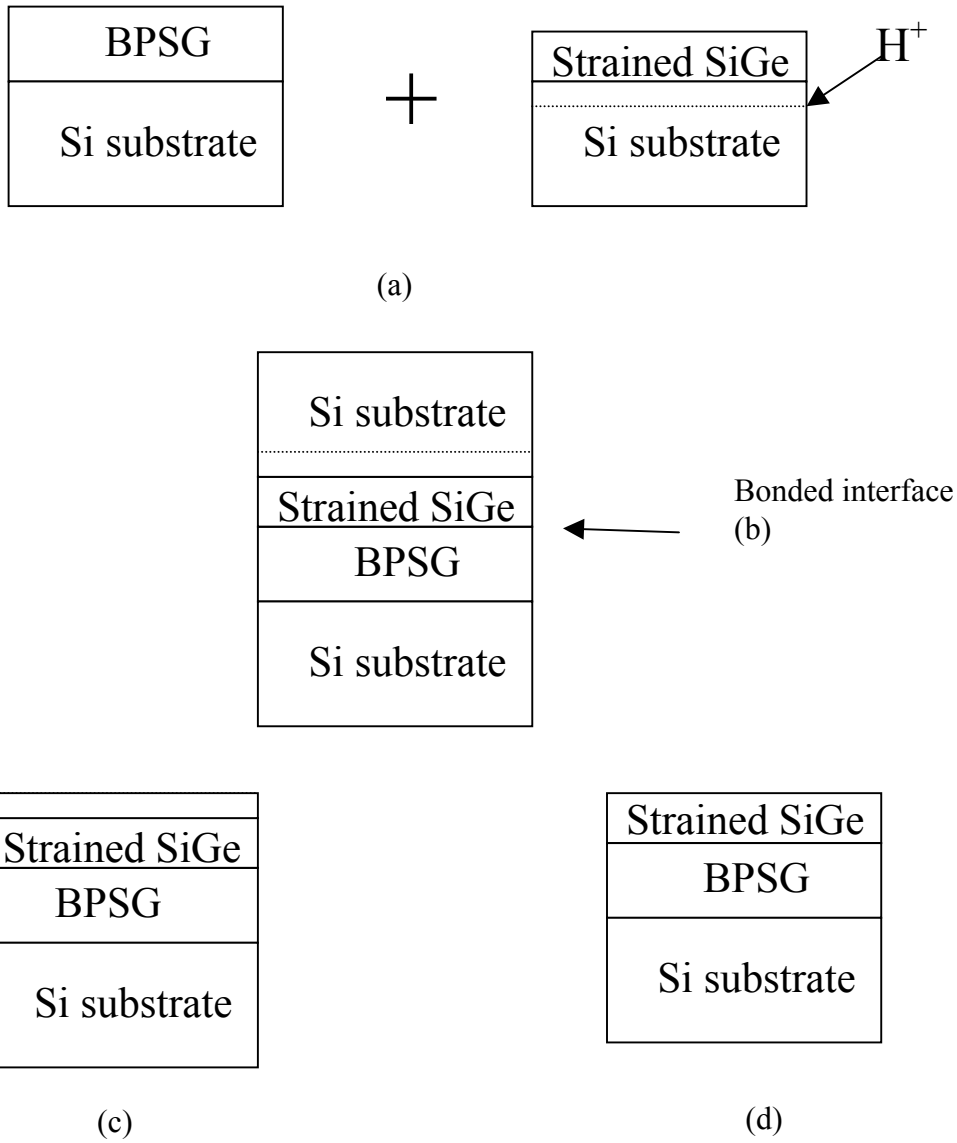


Figure 3.3: Process flow for fabrication of strained SiGe on BPSG: (a) The handle wafer is coated with BPSG, deposited by CVD. The host wafer has a pseudomorphic SiGe layer and is implanted with hydrogen ions. (b) The wafers are cleaned and bonded. (c) The bonded wafer pair is annealed at 550^{o}C to split at the depth of hydrogen implantation. The top silicon substrate is gone, leaving a thin silicon layer. (d) The residual silicon layer is selectively etched using a KOH solution. A thin (2 nm) silicon layer on top of the SiGe on the host wafer is not shown for simplicity.

implantation and the original SiGe epi on the "host" wafers were done by outside vendors. The BPSG-coated wafers were supplied by Tony Margarella at Northrop-Grumman.

3.3 Strain characterization

3.3.1 X-ray diffraction

Two techniques, X-ray diffraction (XRD) and micro-Raman spectroscopy, were used to measure strain in SiGe films. Since the X-ray beam size used in our system is large (~ 0.1 x 1 cm^2), XRD has to be carried out on arrays of identical SiGe islands (Fig. 3.4(a)). The need for islands will be described in the next section. The sample structure in Fig. 3.4(a) is 30-nm $Si_{0.7}Ge_{0.3}$ on 200-nm BPSG. A pair of (004) rocking curves are used to extract the perpendicular lattice constant $a_\perp$ (Fig. 3.4(b)). It is assumed that the as-grown SiGe films are commensurately strained without misfit dislocations, so that the perpendicular lattice constant is expected to be uniform throughout the depth of the SiGe. It is also assumed that the transfer process with a maximum temperature of 550^{o}C did not result in any strain relaxation. After annealing to relax strain, the strain may be non-uniform across islands. The spatially-averaged perpendicular lattice constant across an island measured by XRD is

$$a_\perp(average) = \frac{1}{Area_{Island}} \int_{Island} a_\perp(x,y)dxdy \,. \qquad (3.2)$$

The strain in the SiGe is typically determined by the difference in the Bragg condition between the SiGe and Si substrate peaks. In this case, the (001) axis of the SiGe may not be parallel to that of the handle substrate, since the SiGe film was transferred from a different wafer. The error of the SiGe XRD peak position of SiGe on BPSG, introduced by misalignment of the SiGe vertical crystalline orientation with respect to that of the Si substrate, can be removed by averaging the observed SiGe peak positions in two measurements in which samples are rotated by 180^o [10] (Fig. 3.3(b)). The in-plane lattice constant of the SiGe is calculated from [10]

$$a_\perp - a_r = -2(c_{12}/c_{11})(a_\parallel - a_r), \qquad (3.3)$$

where a_r is the fully relaxed lattice constant of the SiGe, and $a_{||}$ is the in-plane lattice constant, and c_{12} and c_{11} are the elastic constants of the SiGe [11]. The strain fraction of the SiGe is defined as follows:

$$(a_r - a_{||})/(a_r - a_{Si}), \tag{3.4}$$

where a_{Si} is the lattice constant of silicon [11]. This refers to the amount of the original strain in the SiGe (caused by its commensurate growth on silicon) that remains after annealing of the SiGe on BPSG.

When the SiGe film buckles, as it often does during relaxation on BPSG (buckling is introduced in Sec. 3.4 and examined in detail in Chapter 5), the SiGe XRD peak will vanish because the Bragg condition can no longer be satisfied simultaneously by the entire film. Figure 3.3(c) shows the X-ray spectra measured on islands of different sizes after annealing. When the island size reaches 40 x 40 μm^2, the SiGe X-ray diffraction peak is blurred by the background noise. Therefore, for most of our work, the strain was characterized by micro-Raman spectroscopy, not X-ray diffraction.

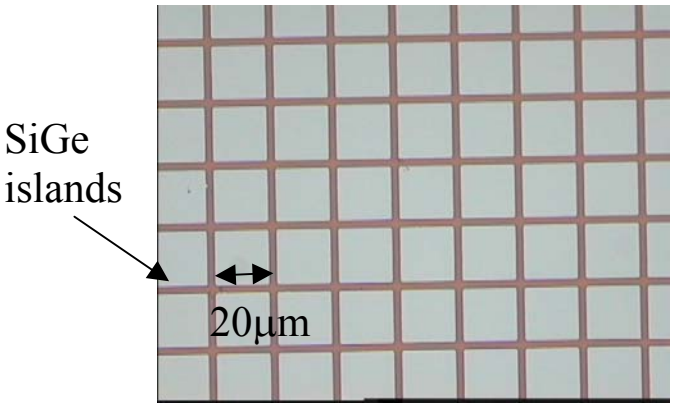
3.3.2 Raman spectroscopy

Raman spectroscopy was used to locally probe the strain in the SiGe and Si films using the apparatus in the lab of Prof. Thomas Duffy of the Geosciences Department at Princeton University. An Ar^+ laser (514.5 or 488 nm) was focused using a microscope objective to a diameter of ~3 μm on the sample surface (Fig. 3.5(a)). The Raman frequency shift due to emission of a Si-Si optical phonon in the SiGe and Si films was measured with an accuracy of ±0.5 cm^{-1}. Fig 3.5(b) shows the Raman spectra measured at the center of a 30 x 30 μm^2 $Si_{0.7}Ge_{0.3}$ island on BPSG before and after strain relaxation. The phonon energy (and thus Raman shift) depends on both the strain and the Ge fraction [12]. The strain ε_{Si} in the Si layer and the strain ε_{SiGe} in $Si_{0.7}Ge_{0.3}$ layer were inferred from the Si-Si optical phonon frequency $\omega_{Si\text{-}Si}$ according to

$$\omega_{Si\text{-}Si}(Si) = 520\ cm^{-1} - 715\varepsilon_{Si}\ cm^{-1}\ [12], \tag{3.5}$$

$$\omega_{Si\text{-}Si}(Si_{0.7}Ge_{0.3}) = 500\ cm^{-1} - 815\varepsilon_{SiGe}\ cm^{-1}\ [13]. \tag{3.6}$$

These relations assume biaxial strain and zero stress in the perpendicular direction, as is the case for our experiment.



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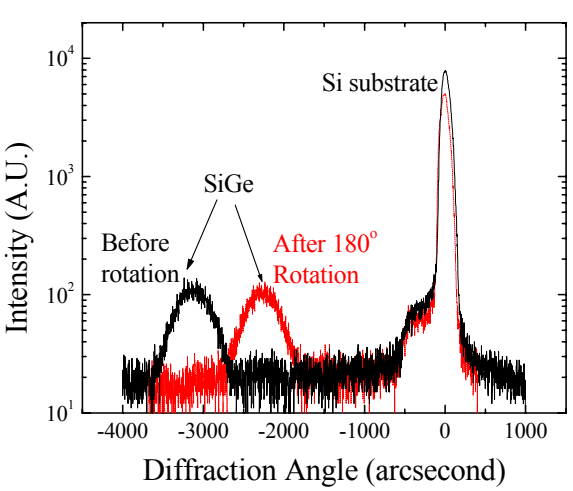

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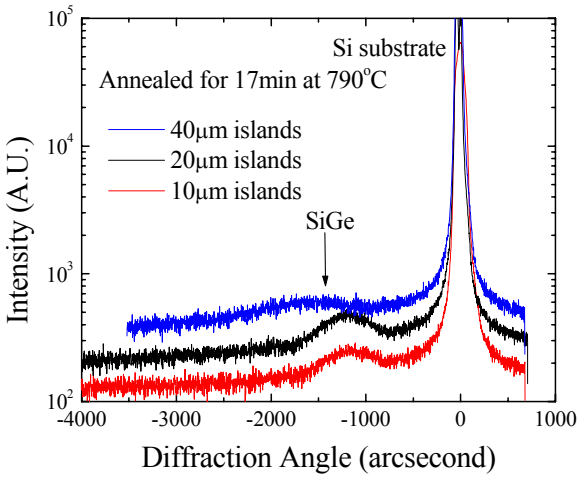
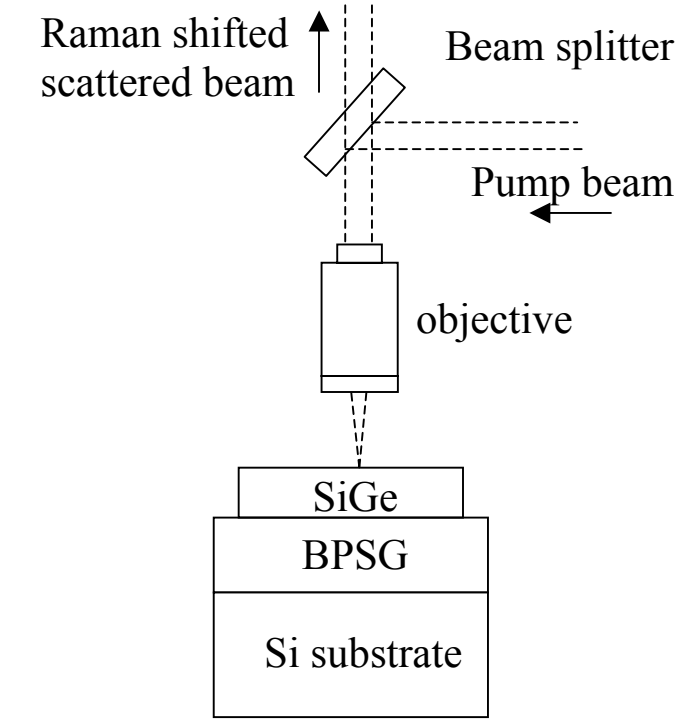


(c)

Figure 3.4: (a) Optical micrograph of 20 x 20 μm^2 30-nm $Si_{0.7}Ge_{0.3}$ island array on BPSG. (b) X-ray diffraction spectra measured on 30-nm $Si_{0.7}Ge_{0.3}$ on BPSG before and after 180° rotation. (c) X-ray diffraction spectra measured on different $Si_{0.7}Ge_{0.3}$ islands after annealing. The zero point of the x-axis is set at the location of the silicon substrate peak.



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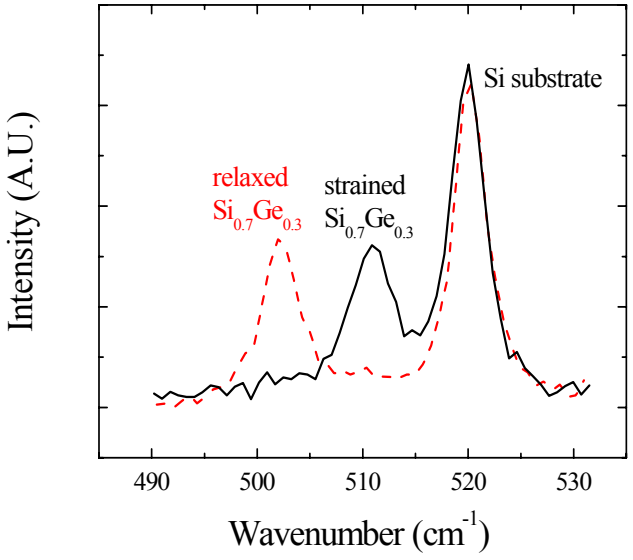
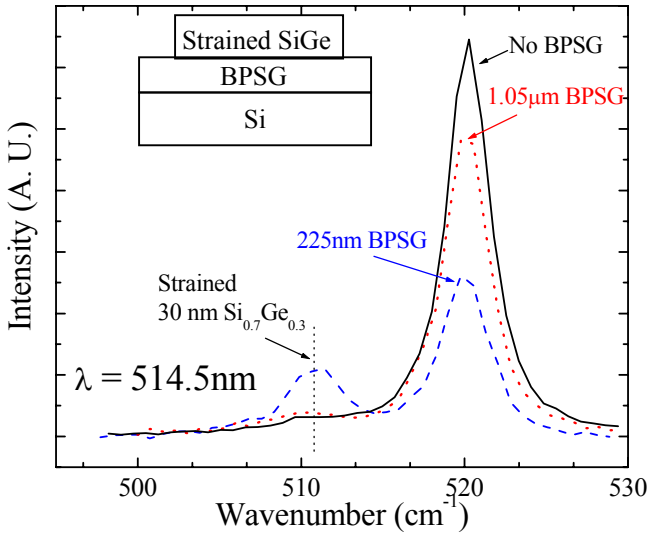


(b)

Figure 3.5: (a) Schematic for micro-Raman spectroscopy. (b) Raman spectra measured on a $Si_{0.7}Ge_{0.3}$ island before and after strain relaxation.



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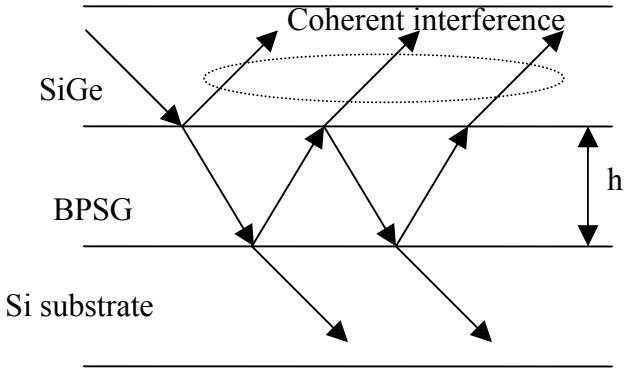


(b)

Figure 3.6: (a) Measured Raman spectra of fully-strained 30-nm $Si_{0.7}Ge_{0.3}$ with various BPSG thicknesses. (b) Schematic diagram of the multiple reflections at the BPSG interfaces. The reflected light gives rise to optical interference.

The BPSG layer has a significant effect on the Raman intensity from the SiGe film due to interference effects. Figure 3.6(a) shows the Raman spectra measured on 30-nm strained $Si_{0.7}Ge_{0.3}$ with different BPSG thicknesses using a visible 514-nm excitation laser. For the sample without BPSG, the SiGe Raman peak (512 cm^{-1}) was much weaker than the silicon substrate Raman peak (520 cm^{-1}), which suggests that most of the Raman signal comes from the silicon substrate. This is consistent with the large penetration depth (~ 340 nm) for the 514-nm wavelength. The small SiGe Raman peak, obscured by the strong substrate Raman peak, makes it difficult to accurately determine the peak position and thus strain value. When a 225-nm BPSG layer (measured by ellipsometry) was sandwiched between the SiGe film and the substrate, the substrate Raman peak was greatly reduced whereas the SiGe Raman peak was enhanced. The height ratio of the SiGe Raman peak to the substrate Raman peak increased by about ten times compared to the BPSG-free sample and the SiGe Raman peak position could be readily determined. However, when the BPSG thickness was around 1.05 μm, no relative enhancement of the SiGe signal was observed.

Before we understood this interference effect, we first thought the absence of the SiGe Raman signal for the sample with a 1.05-μm BPSG layer compared with the strong signal for a 225-nm layer indicated that the SiGe was missing or non-crystalline. To understand the effect of BPSG on the Raman measurement, the light reflection at the BPSG interfaces needs to be identified. The sandwiched BPSG film forms two reflection interfaces: SiGe/BPSG and BPSG/Si-substrate (Fig. 3.6(b)). The reflectivity at a single SiGe/BPSG interface for normal incident light is $R_{SiGe/BPSG} = (n_{BPSG} - n_{SiGe})^2 / (n_{BPSG} + n_{SiGe})^2$, where n represents the refractive index [14]. In contrast, the reflectivity of SiGe/BPSG/Si-substrate (SiGe/BPSG and BPSG/Si-substrate interfaces) is much more complex owing to the optical interference of the multiple reflections (Fig. 3.6(b)). The interference can be either constructive or destructive and depends on the phase shift $\delta = 2\pi n_{BPSG} h / \lambda$, where h and λ are the BPSG thickness and excitation wavelength, respectively. Given the similarity between the SiGe/BPSG/Si-substrate and the well-known Fabry-Perot structure [14], the reflectivity formula of the Fabry-Perot structure can be applied to SiGe/BPSG/Si-substrate:

$R_{SiGe/BPSG/Si} = F\sin^2\delta/(1+F\sin^2\delta)$, where F is defined as $4R_{Si/BPSG}/(1-R_{Si/BPSG})^2$. For simplicity, the refractive index is assumed the same for silicon and SiGe. The refractive indices of silicon and BPSG are approximately 4.3 and 1.5, respectively. When the multiple reflections are in phase and thus constructively interfere, the reflectivity of the SiGe/BPSG/Si structure reaches the maximum value of 0.62, which is nearly three times the reflectivity (0.24) at a single SiGe/BPSG interface.

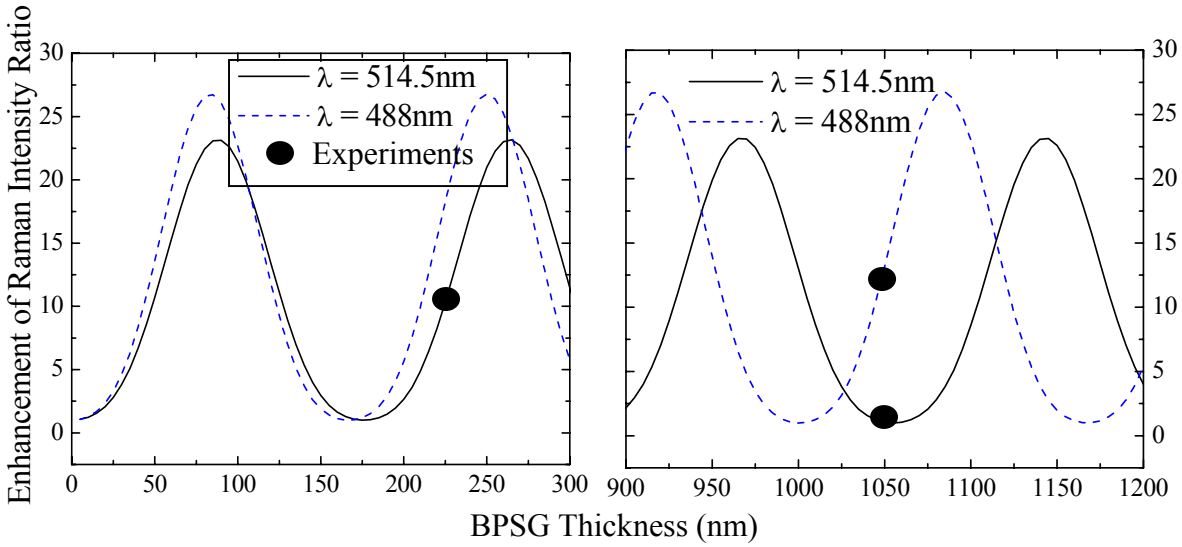
The reflection at the BPSG interfaces affects the Raman measurement by increasing the observed Raman signal from the SiGe film while suppressing the observed Raman signal from the substrate. First, as a result of the reflection, the excitation intensity in the SiGe film is increased and the excitation intensity in the substrate is reduced (Figure 3.6(b)). Since Raman scattering is linearly proportional to the excitation intensity, the Raman signal intensity from the SiGe film increases and that from the substrate decreases. After taking into account of the multiple reflections at the SiGe/air and SiGe/BPSG/Si interfaces, the enhancement in the excitation intensity ratio of the SiGe film to the substrate can be expressed in terms of reflectivity at the interfaces as

$$(1+R_{SiGe/BPSG/Si}R_{SiGe/Air})/\{(1-R_{SiGe/BPSG/Si}R_{SiGe/Air})(1-R_{SiGe/BPSG/Si})\}, \quad (3.7)$$

which varies from unity for $R_{SiGe/BPSG/Si}$=0 to 5.5 for $R_{SiGe/BPSG/Si}$=0.62. The light absorption in the SiGe film is not included in Eqn. 3.7, which is a reasonable approximation since the SiGe thickness (30 nm) is far less than the optical penetration depth (~340 nm).

The second contribution enhancing the Raman intensity ratio of the SiGe film to the substrate by the reflection at SiGe/BPSG/Si-substrate relies on the improved Raman signal collection from the SiGe film while reducing Raman signal collection from the substrate. Some Raman scattered light in the SiGe film that would otherwise have been absorbed in the substrate is reflected by the SiGe/BPSG/Si-substrate interfaces and then detected. On the other hand, since only part of the Raman signal in the substrate is transmitted past the interfaces to be detected, the observable Raman scattered light from the substrate is reduced. The enhancement in the Raman signal collection ratio of the SiGe film to the substrate is

$$(1+R_{SiGe/BPSG/Si})/(1-R_{SiGe/BPSG/Si}) \ . \quad (3.8)$$



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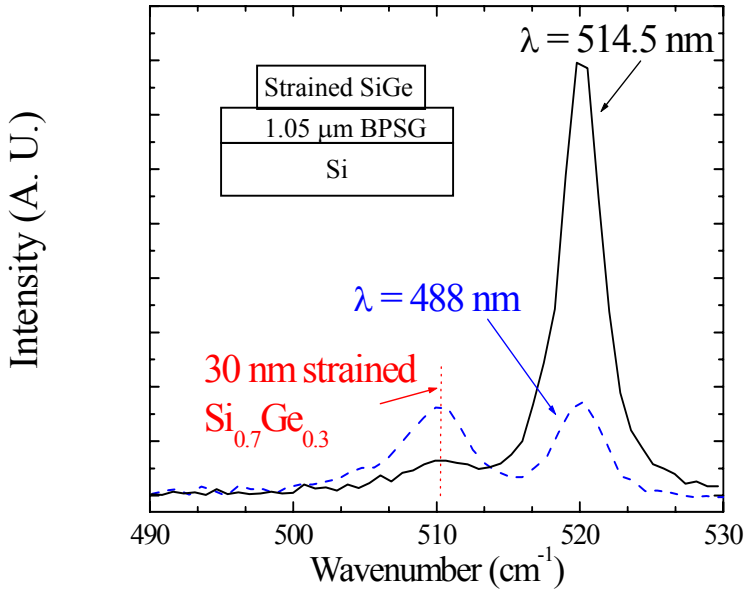


(b)

Figure 3.7: (a) Calculated enhancement in Raman intensity ratio of the SiG film to the silicon substrate as a function of BPSG thickness for two excitation wavelengths. Solid circles are experimental data. (b) Measured Raman spectra of 30-nm $Si_{0.7}Ge_{0.3}$/1.05 μm BPSG for two excitation wavelengths.

Combining the excitation intensity enhancement and Raman signal collection enhancement, one can estimate the total enhancement in Raman peak ratio of the SiGe film to the substrate by multiplying Eqns. 3.7 and 3.8. Figure 3.7(a) shows the calculated Raman peak ratio enhancement as a function of the BPSG thickness for two excitation wavelengths. The SiGe Raman peak height can be enhanced by more than twenty times relative to the substrate Raman peak.

The strong change in Raman signal intensity with BPSG thickness shown in Fig. 3.6(a) can be predicted by Fig. 3.7(a). At 514.5-nm excitation, the Raman signal ratio enhancement for SiGe/BPSG/Si-substrate samples over the SiGe/Si-substrate sample is calculated to be 10.3 and 1 for 225-nm and 1.05-μm BPSG, respectively. The observed ratio enhancement in Fig 3.6(a) is 10.6 and 1.3 for the two BPSG thicknesses, in good agreement with the calculation. The small ratio enhancement measured for 1.05-μm BPSG is owing to the out-of-phase reflections at 514.5-nm excitation. When the excitation wavelength is changed from 514.5 nm to 488 nm, the multiple reflections are no longer out of phase and the ratio enhancement is calculated to be 13.2, in line with the observed value of 12 (Fig. 3.7(b))

3.4 Qualitative study of strain relaxation of SiGe islands on BPSG

30-nm $Si_{0.70}Ge_{0.30}$ islands on 200-nm BPSG were annealed under various conditions to examine the strain relaxation. Because the SiGe islands are squeezed, they want to expand to release the compressive strain. There are two ways for the film to expand: either laterally on BPSG (as desired) or buckling (Fig. 3.8). Both elongate the SiGe film and relax the compressive strain. When lateral relaxation dominates the relaxation process, the film remains flat, whereas the film becomes rough when buckling dominates the strain relaxation. Since lateral expansion relies on lateral displacement of the film, it happens first on the edge of islands and propagates towards the island center. Therefore, the smaller the islands are, the faster lateral expansion reaches the center. On the other hand, the buckling mechanism is not a boundary effect and, consequently, is independent of island size.

Figure 3.9 shows an optical micrograph of a corner of a 100×100 μm^2 SiGe island after a 90-min anneal at 790^oC. It shows three distinct relaxation regions: (1) Buckling is

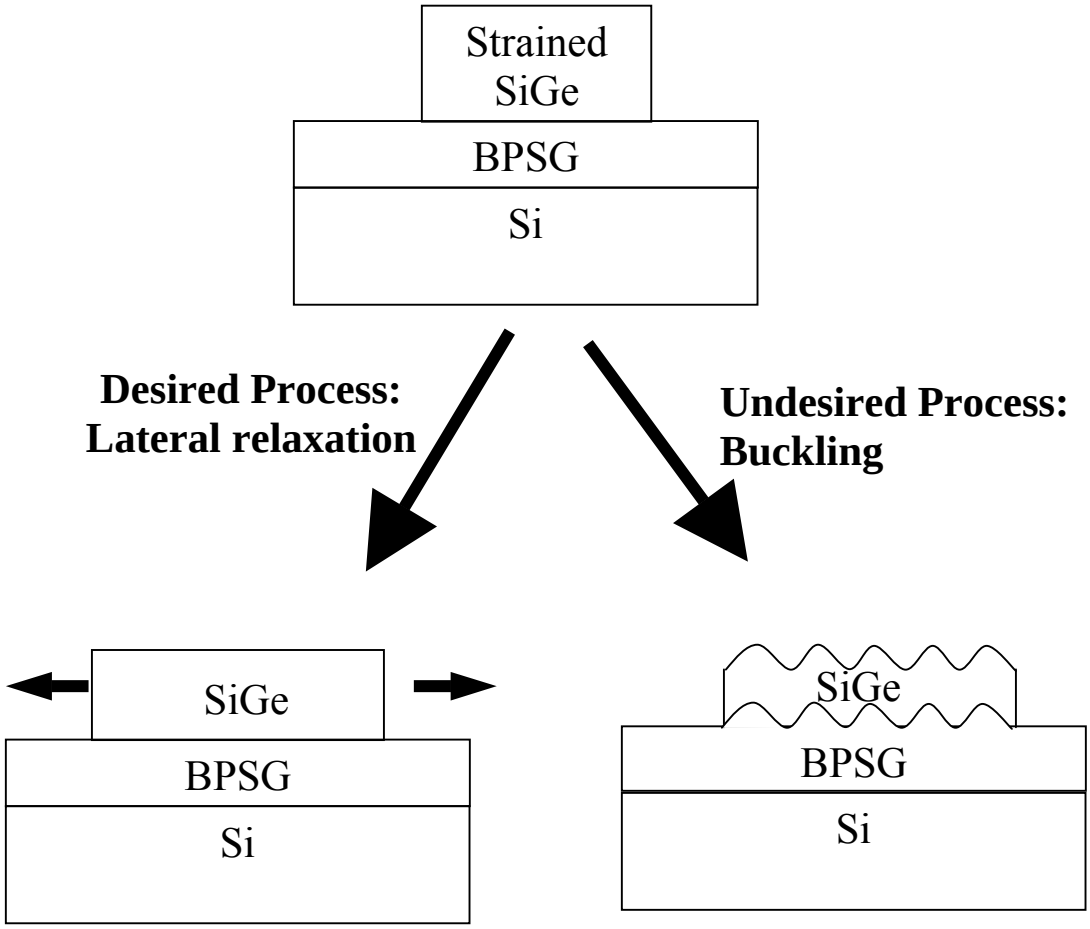


Figure 3.8: Diagram of relaxation mechanisms: lateral relaxation vs. buckling. Both mechanisms are enabled when the BPSG becomes "soft" and can flow.

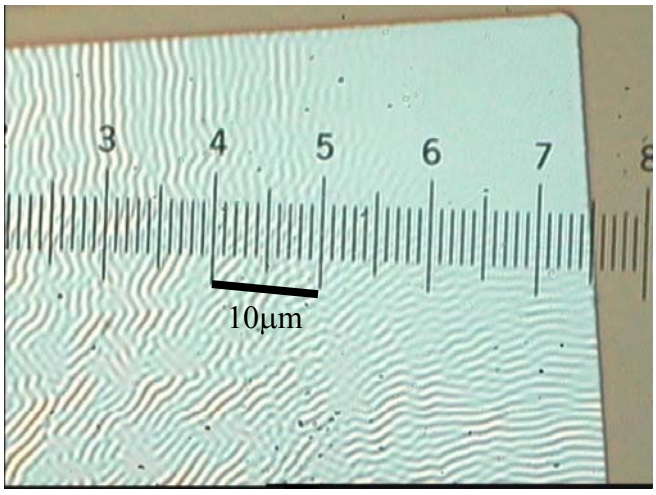


Figure 3.9: Optical micrograph of a corner of a 100 × 100 μm^2 $Si_{0.7}Ge_{0.3}$ island after a 90-min anneal at 790^{o}C in nitrogen.

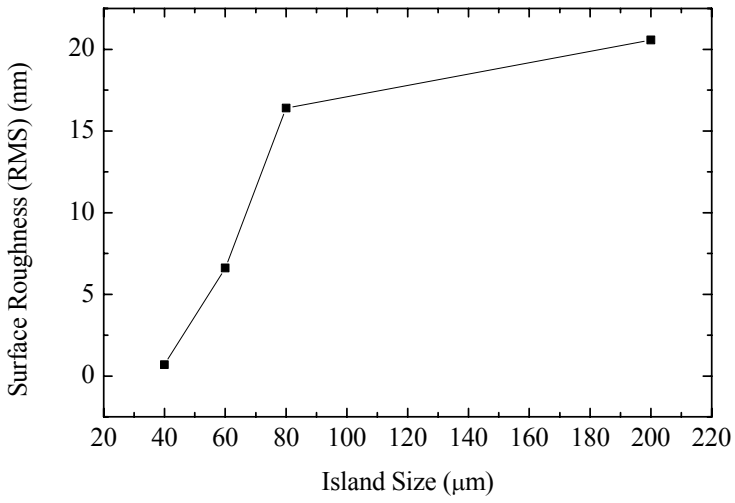


Figure 3.10: Surface roughness measured at the center of square islands of various edge sizes after a 90-min anneal at 790^{o}C in nitrogen.

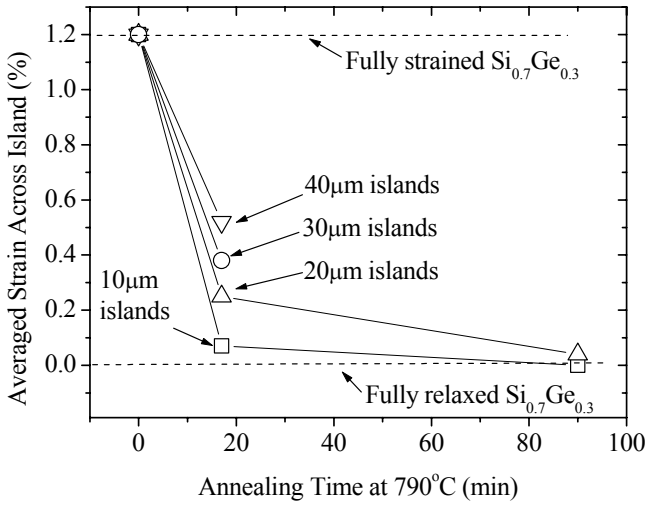


Figure 3.11: Spatially-averaged strain across islands (measured by XRD) vs. annealing time at 790°C in nitrogen.

entirely avoided in the corner close to edge where in-plane expansion takes place quickly to relax strain, (2) buckling appears in areas where in-plane expansion only releases strain along one direction, i.e., normal to the edge, and (3) in the island center where strain is only relaxed by buckling. Indeed, the need to avoid buckling is why the SiGe film on BPSG was patterned into islands in the first place (Sec. 3.3.1). Figure 3.10 summarizes the buckling behavior as a function of island size. The surface roughness was measured at the island center using atomic force microscopy (AFM). Small islands (e.g. less than 40 x 40 μm^2) relaxed quickly by lateral expansion before buckling could occur and remained flat. For large islands (e.g. larger than 80 μm x 80 μm), the lateral relaxation was negligible at island center and strain was only relaxed by buckling, with the RMS surface roughness saturating around 20 nm when island size was larger than 80 x 80 μm^2.

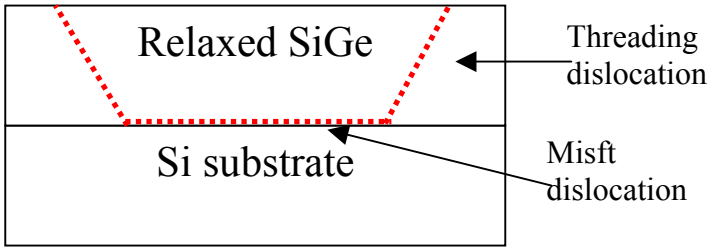
Strain relaxation by lateral expansion was investigated in small islands, in which lateral expansion is the sole contributor of the strain relaxation, since strain is relaxed quickly by lateral expansion before any sizable buckling can occur. Figure 3.11 shows the strain relaxation measured in small islands after annealing at 790°C in nitrogen. Since the data in Fig. 3.11 were obtained by XRD on arrays of islands, the measured strain is spatially averaged across islands. Note that the average strain in small islands goes to zero after sufficient annealing. It is clear from Fig. 3.11 that small islands relax much

faster than large islands. After a 17-min anneal at 790^{o}C, 10 x 10 μm^2 islands were nearly fully relaxed, whereas 40 x 40 μm^2 islands were only half relaxed. For large islands, the surface tends to roughen by buckling after a long time anneal, and accordingly, the XRD peaks of large SiGe islands broaden and vanish. This accounts for the disappearance of XRD peaks of 30 μm and 40 μm islands after 90 min annealing at 790^{o}C.

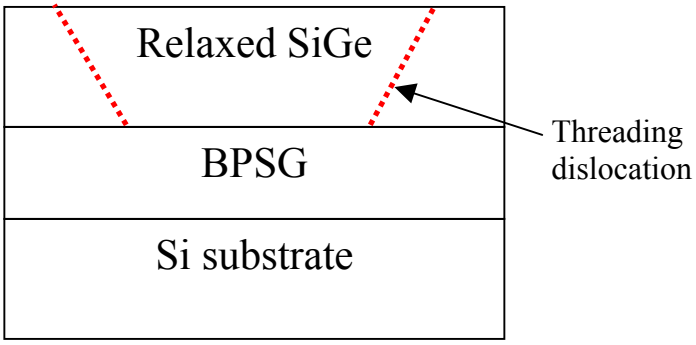
A detailed study of lateral expansion and buckling of SiGe islands on BPSG will be presented in Chapters 4 and 5. Various schemes will be then discussed for enhancing the lateral expansion and suppressing the buckling.

3.5 Defect study of relaxed SiGe on compliant BPSG

The relaxation of strained SiGe on silicon substrates is usually induced by the formation of dislocations, which degrade the film quality and render it unsuitable for device application. The relevant "edge" dislocations in this case can be thought of as the boundary of an extra plane of atoms within the crystal. In the case of heteroepitaxy of SiGe on silicon substrates, the edge dislocations can be divided into two types: misfit and threading dislocations [(MDs) and (TDs), respectively], as shown in Fig. 3.12(a). MDs lie in the epitaxial interface and accommodate the lattice mismatch between the SiGe and the silicon substrate. TDs lie within the SiGe and run from the interface to its surface. Since there is no epitaxial interface in SiGe on BPSG, only threading dislocations can form in the SiGe (Fig. 3.12(b)). To determine the role of dislocations in the strain relaxation of SiGe on BPSG, the threading dislocation density of SiGe on BPSG was studied. Plan-view transmission electron microscopy (PV-TEM) was first tried to determine the dislocation density. The threading dislocations manifest themselves as short segments when they are seen in PV-TEM. 30-nm $Si_{0.7}Ge_{0.3}$ on BPSG was patterned into 40 x 40 μm^2 islands, which were annealed at 800^{o}C in nitrogen for 1 hr to achieve full relaxation. SiGe islands were then released from the substrate by using a HF(49%) solution to dissolve the BPSG. The floating islands were caught onto copper TEM meshes by hand with tweezers for TEM observation. No dislocations were found in all area inspected by PV-TEM (Fig. 3.12(c)). The work was performed using Leo/Zeiss 910 TEM at PRISM with assistance from Dr. Nan Yao. The stripes in Fig. 3.12(c) reflect the stress field caused by the bending of the SiGe film.



(a)



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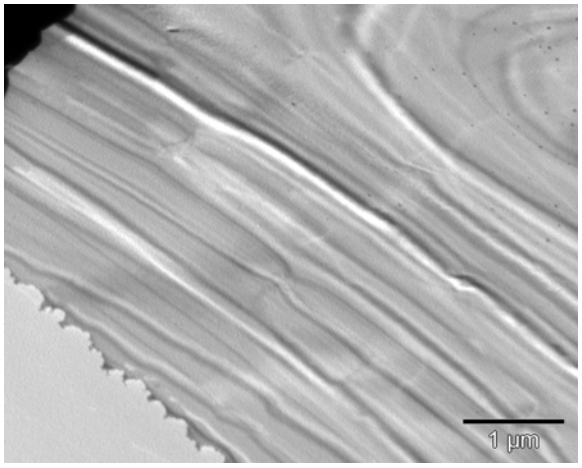
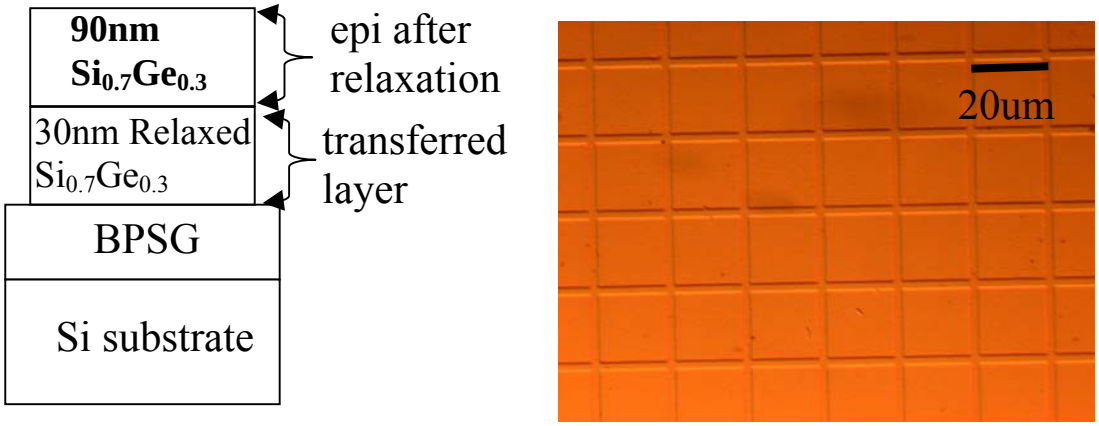
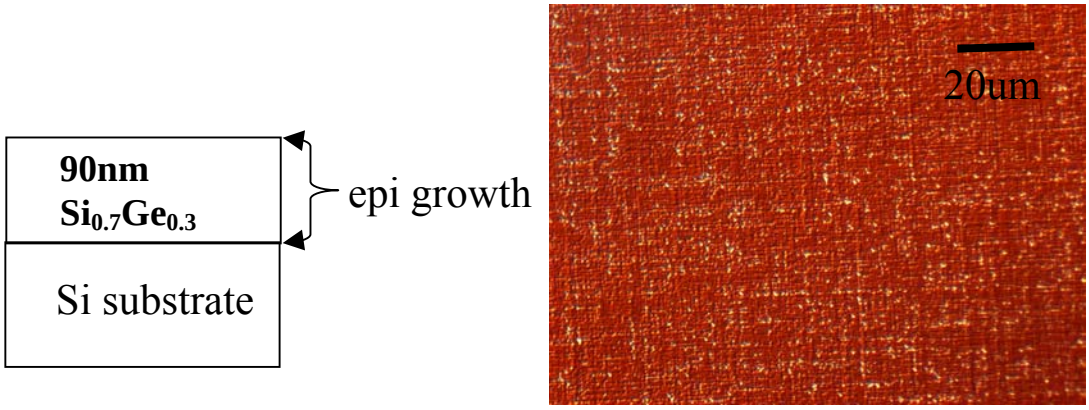


(c)

Figure 3.12: (a) Both misfit and threading dislocations form in SiGe on silicon. (b) Only threading dislocations can form in SiGe on BPSG. (c) Plan-view TEM micrograph of a part of a 30-nm $Si_{0.7}Ge_{0.3}$ island of edge width 40 µm after a 1-hr anneal at 800°C.



(a)



(b)

Figure 3.13: Nomarski optical micrographs of SiGe films after 60-sec Schimmel etch [15]: (a) 90-nm $Si_{0.7}Ge_{0.3}$ was grown on relaxed $Si_{0.7}Ge_{0.3}$ islands. (b) 90 nm $Si_{0.7}Ge_{0.3}$ was grown on a silicon bulk substrate, followed by a 150-min anneal at 800^{o}Cto release strain.

Because the area examined by PV-TEM is limited (up to about 7 x 7 μm^2 at one time), it is not a reliable tool used to determine low dislocation densities. Assuming no defects in these regions, this places an upper limit on the defect density of $2x10^6$ cm^{-2}, which is still a technologically large number. To inspect a larger area, defect etching was used to delineate dislocations [15]. Since defect etching etches preferentially at defect sites but still slowly removes materials in regions without defects, it does not work for thin films (less than about 30 nm). They are completely etched before dislocations can be decorated by the preferential etch. Therefore, before defect etching, a 90-nm $Si_{0.7}Ge_{0.3}$ film was selectively grown on top of the strain-relaxed 30 nm $Si_{0.7}Ge_{0.3}$ islands at 625^oC using the rapid thermal CVD tool in our group, increasing the total thickness to 120 nm. Since threading dislocations end at the surface, it is presumed that all dislocations present in the original film would propagate upward and reach the top surface. The defect density in the top film should be similar to that in the buried layer. As a control sample, a 90-nm $Si_{0.7}Ge_{0.3}$ film was also grown on a bulk silicon substrate. The control sample was then annealed at 800^oC for 150 min to release strain. Because this layer is far above the critical thickness (8 nm) and no grading or other attempts were made to reduce the defect density, this layer should have a very high defect density. The samples were dipped into the etch solution, composed of 4 parts 49% HF and 5 parts 0.3M CrO_3, for 60 sec and inspected under a Nomarski microscope. A high density of dislocations was seen in the control sample, whereas there were very few dislocations (less than 5 x 10^5 cm^{-2}) observed in the SiGe islands on BPSG (Fig. 3.13). The high quality of the relaxed SiGe islands on BPSG indicates that defect formation does not play a dominant role in the strain relaxation process and that most of the strain relaxation occurs by the mechanism of straightforward lateral expansion. It should also be noted that in Sec. 6.2, the amount of lateral expansion was directly measured and found to be in good agreement with the assumption that dislocations do not play a major role in the SiGe relaxation.

Note that conventional approaches for relaxed SiGe of graded buffer layers grown directly on silicon have a threading defect density of ~ 10^5 cm in the best work, which has been optimized for nearly 15 years. Whether this is acceptable for applications is not clear. In our case measuring defect densities of less than $5x10^5$ cm^{-2} would require

measuring over a larger area with cleaner processing than we are capable of. Nevertheless we feel that our approach is capable in principle of a near-zero defect density.

3.6 Summary

Compliant substrates are an approach for allowing strained epitaxial layers to relax and thus change their in-plane lattice constant without introducing a high defect density. This provides a low defect "substrate" for the growth of subsequent pseudomorphic epitaxial layers with a lattice constant different than that of the original substrate. BPSG layers were presented as a novel compliant substrate for SiGe layers which were initially commensurately grown on silicon substrates and then transferred to the BPSG. The lowered viscosity of BPSG at high temperatures enables expansion of the compressive SiGe to reach strain relaxation. Two types of relaxation mechanisms, lateral expansion and buckling, were differentiated and their characteristics were investigated. Defect etching was used to examine dislocation densities in the relaxed SiGe on BPSG and high quality was confirmed. This shows that the relaxation of strained SiGe islands occurs through lateral expansion enabled by the compliant BPSG film, and not through dislocation formation.

In the next a few chapters, studies on the relaxation mechanisms will be thoroughly explored and some novel applications will be demonstrated, completing a systematic study of the SiGe-on-BPSG system. Specifically, Chapter 4 studies the desired lateral expansion of strained SiGe on BPSG in detail and then the lateral relaxation of bi-layer structures, Chapter 5 studies the SiGe buckling issue, Chapter 6 discusses methods to reach high germanium content in the SiGe on BPSG and Chapter 7 presents a way of fabricating strained silicon on BPSG without SiGe in the final structure and its use for n-channel MOSFETs.

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Chapter 4

Lateral Expansion of SiGe Islands on BPSG

Lateral expansion contributes to the relaxation of strained layers on compliant substrates, which has been assumed in many studies [1,2]. However, little work has been done to investigate and confirm the lateral expansion, the foundation of the compliant method. In chapter 3, we have qualitatively discussed the behavior of SiGe lateral expansion on BPSG. In this chapter, lateral expansion has been quantitatively studied on single SiGe layers and bi-layers made of SiGe and Si or SiO_2. Three main sets of results are presented: (1) Experiments on SiGe lateral expansion have been compared with modeling, which allows viscosity extraction of the compliant BPSG. The good agreement between experiments and modeling confirms the lateral expansion assumption (Sec. 4.1). (2) The theory for lateral expansion of bi-layer structures has been developed and compared to experiments. The stress balance of bi-layer structures on compliant BPSG is observed for the first time, indicating that BPSG is a perfectly compliant substrate and after annealing does not exert any significant force on the layers above it (Sec. 4.2-4.4). (3) The geometry dependence of the lateral expansion has been utilized to control strain separately in different directions. Using long stripe structures, uniaxial stress has been demonstrated in SiGe films. Orthorhombic strain has been achieved by controlling stripe geometry and stress balance (Sec. 4.5-4.6).

4.1 Lateral expansion of SiGe single-layer islands on BPSG

4.1.1 1-D model of lateral expansion

The goal of this section is to quantitatively understand the single-layer lateral expansion of SiGe islands on BPSG as shown in Fig. 3.4. The one-dimensional (1-D) model of the lateral expansion of strained islands on a viscous layer was formulated by different groups [3,4] .

Consider a strained elastic film of thickness h_f on a viscous layer of thickness h_g, as shown in Fig. 4.1(a). In our case, the viscous layer is made of BPSG and the elastic film

is SiGe. The island is of length L. The surface of the film is along y direction, and the coordinate z is normal to the surface. No roughening is considered in the process. The SiGe film is subject to the in-plane stress σ_{yy} and the shear traction, τ_y, at the film/glass interface. The equilibrium of the film island requires

$$\frac{\partial \sigma_{yy}}{\partial y} = \frac{\tau_y}{h_f} \tag{4.1}$$

In the 1-D case, we have the simple stress-strain relation in the y direction:

$$\sigma_{yy} = E\varepsilon_{yy}, \tag{4.2}$$

where E is the Young's modulus.

Before relaxation, the film is compressive with a strain ε_0 and the lateral displacements are zero. During relaxation, the strain component in the y direction is

$$\varepsilon_{yy} = -\frac{\partial u}{\partial y} - \varepsilon_0, \tag{4.3}$$

where u represents the displacement in the y direction.

The viscous BPSG glass layer is subject to the shear stresses, τ_y, at the top surface and is fixed at the bottom. The glass is assumed to be linearly viscous, and variation of the flow velocity is linear from the bottom to the top surface. The displacements at the top surface of the glass are assumed to be identical to the displacements of the film. Consequently, the shear stresses are

$$\tau_y = \frac{\eta}{h_g}\frac{\partial u}{\partial t}, \tag{4.4}$$

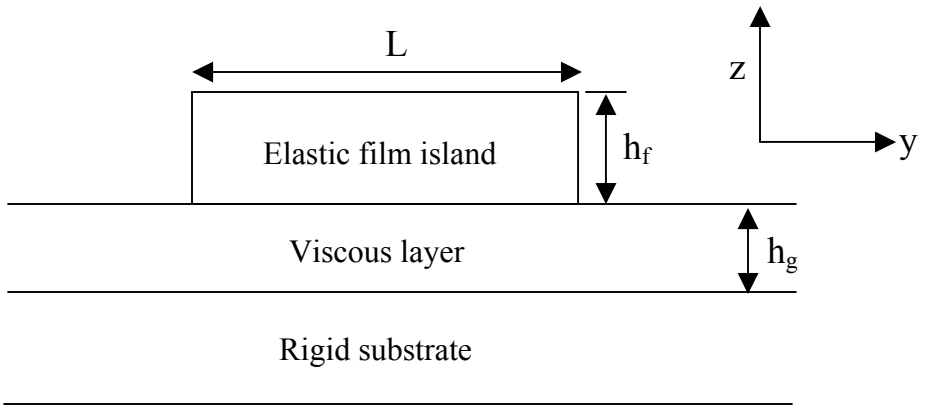
where η is the glass viscosity.

The time evolution equation for the in-plane displacement can be obtained by substituting Eqns. 4.2, 4.3 and 4.4 into Eqn. 4.1:

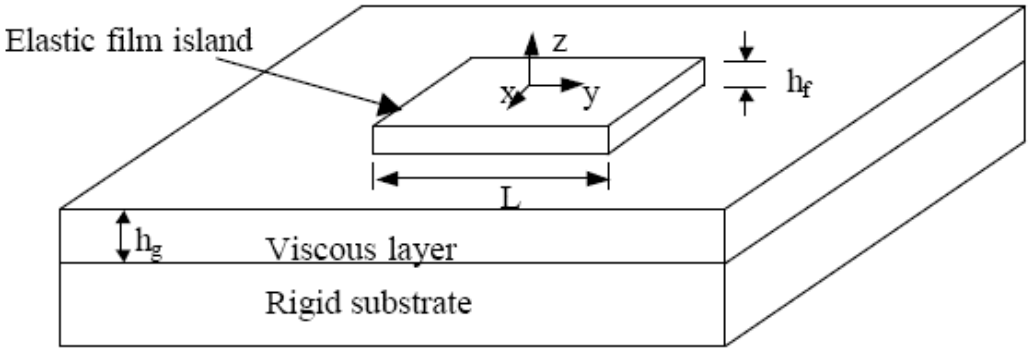
$$\frac{\partial u}{\partial t} = D_{1D}\frac{\partial^2 u}{\partial y^2} \tag{4.5}$$

where

$$D_{1D} = \frac{Eh_f h_g}{\eta}, \tag{4.6}$$



(a)



(b)

Figure 4.1: Illustration of an elastic island (e.g. SiGe) on a viscous layer (e.g. BPSG) on a rigid (e.g. silicon) substrate for 1-D (a) and 2-D (b).

The quantity D_{1D} has the dimensions of diffusivity, and Eqn. 4.5 has the form of a diffusion equation. The island size L and the coefficient D_{1D} define the characteristic time scale for the 1-D lateral relaxation:

$$t_{L\_1D} = \frac{L^2}{D_{1D}} = \frac{\eta L^2}{E h_f h_g}. \tag{4.7}$$

4.1.2 2-D model of lateral expansion

Recently Huang *et al*. [5] have developed a generalized model for the two-dimensional (2-D) square islands and found that the time scale of the lateral relaxation is similar to that of the 1-D model, as described in the following.

In the 2-D case (Fig. 4.1(b)), the film island is subject to the in-plane stresses, σ_{xx}, σ_{yy}, and σ_{xy}, and the shear tractions, τ_x and τ_y, at the film/glass interface. The equilibrium of the film island requires

$$\frac{\partial \sigma_{xx}}{\partial x} + \frac{\partial \sigma_{yx}}{\partial y} = \frac{\tau_x}{h_f}, \quad \frac{\partial \sigma_{xy}}{\partial x} + \frac{\partial \sigma_{yy}}{\partial y} = \frac{\tau_y}{h_f}. \tag{4.8}$$

Assuming that $\sigma_{zz} = 0$ and the material is of cubic crystal symmetry, we can express the strain in the z axis using the strains in the x-y plane as follows:

$$\varepsilon_{zz} = -\frac{c_{12}}{c_{11}}(\varepsilon_{xx} + \varepsilon_{yy}). \tag{4.9}$$

By substituting Eqn. 4.9 into the elastic stress-strain relation (Eqn. 2.2), one obtains that

$$\sigma_{xx} = \hat{c}_{11}\varepsilon_{xx} + \hat{c}_{12}\varepsilon_{yy}, \sigma_{yy} = \hat{c}_{12}\varepsilon_{xx} + \hat{c}_{11}\varepsilon_{yy}, \ \sigma_{xy} = 2c_{44}\varepsilon_{xy}, \tag{4.10}$$

where $\hat{c}_{11}=c_{11}-c^2_{12}/c_{11}$ and $\hat{c}_{12}=c_{12}-c^2_{12}/c_{11}$.

Before relaxation, the film is compressive with a biaxial strain ε_0 and the lateral displacements are zero. During relaxation, the in-plane strain components are

$$\varepsilon_{xx} = -\frac{\partial u}{\partial x} - \varepsilon_0, \ \varepsilon_{yy} = -\frac{\partial v}{\partial y} - \varepsilon_0, \varepsilon_{xy} = \frac{1}{2}\left(\frac{\partial u}{\partial y} - \frac{\partial v}{\partial x}\right). \tag{4.11}$$

where u and v represent the displacements in the x and y directions, respectively.

The viscous glass layer is subject to the shear stresses, τ_x and τ_y, at the top surface and is fixed at the bottom. Consequently, the shear stresses are

$$\tau_x = \frac{\eta}{h_g}\frac{\partial u}{\partial t},\ \tau_y = \frac{\eta}{h_g}\frac{\partial v}{\partial t}. \tag{4.12}$$

The 2-D time evolution equations for the in-plane displacements can be obtained by substituting Eqns. 4.12, 4.11 and 4.10 into Eqn. 4.8:

$$\frac{\partial u}{\partial t} = D_{2D}\left[\check{c}_{11}\frac{\partial^2 u}{\partial x^2} + \check{c}_{44}\frac{\partial^2 u}{\partial y^2} + (\check{c}_{12}+\check{c}_{44})\frac{\partial^2 v}{\partial x \partial y}\right], \tag{4.13a}$$

$$\frac{\partial v}{\partial t} = D_{2D}\left[\check{c}_{11}\frac{\partial^2 v}{\partial y^2} + \check{c}_{44}\frac{\partial^2 v}{\partial x^2} + (\check{c}_{12}+\check{c}_{44})\frac{\partial^2 u}{\partial x \partial y}\right], \tag{4.13b}$$

where

$$D_{2D} = \frac{c_{11} h_f h_g}{\eta}, \tag{4.14}$$

and $\check{c}_{11} = \hat{c}_{11}/c_{11}$, $\check{c}_{12} = \hat{c}_{12}/c_{11}$, and $\check{c}_{44} = c_{44}/c_{11}$. The characteristic time scale for the 2-D lateral relaxation is

$$t_{L\_2D} = \frac{L^2}{D_{2D}} = \frac{\eta L^2}{c_{11} h_f h_g}. \tag{4.15}$$

The time scale difference in the 1-D and 2-D lateral relaxation is solely due to the difference between E and c_{11}. E can be expressed by c_{11} and c_{12} as follows:

$$E = \frac{(c_{11}-c_{12})(c_{11}+2c_{12})}{c_{11}+c_{12}} = c_{11}\left(1 - 2\frac{c_{12}^2/c_{11}^2}{1+c_{12}/c_{11}}\right). \tag{4.16}$$

Therefore, E is always smaller than c_{11}, meaning the lateral relaxation is faster in the 2-D case than in the 1-D case. However, the value difference between E and c_{11} is small and E is generally about 80% of the c_{11} value (See Table 4.1). Since buckling is not included in the lateral expansion model, it is only applicable to small islands that do not suffer buckling.

4.1.3 Experiments

To demonstrate that the lateral relaxation indeed quantitatively scales as predicted by Eqn. 4.15, the time dependence of strain during the 790°C annealing of 30-nm $Si_{0.7}Ge_{0.3}$ islands of different sizes on 200-nm BPSG in Fig. 3.9 has been re-plotted by normalizing the time axis with respect to the square of island edge width (Fig. 4.2). The normalization

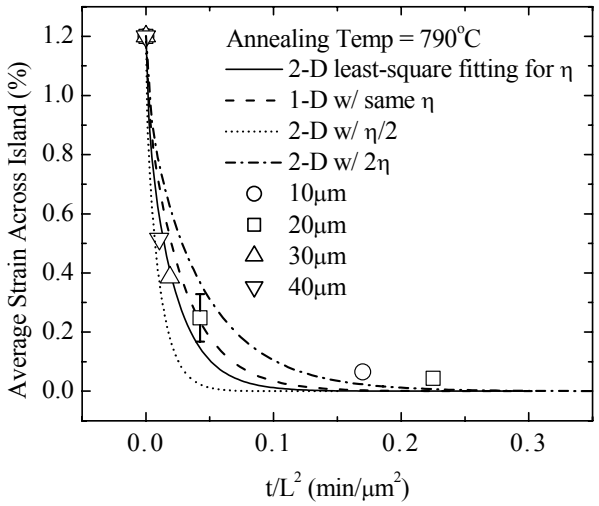


Figure 4.2: Averaged strain across islands, measured by XRD, as a function of normalized annealing time at 790°C for island sizes from 10 μm to 40 μm. Open symbols are experimental data. The typical error bar in the strain measurement is +/-0.075%, as shown on one data point. Least-square fitting based on the 2-D model [5] gives rise to the solid line with the only fitting parameter (viscosity) of 1.3×10^{10} N*sec/m^2. The dashed line is the 1-D model using the same viscosity. The short-dot line and the dash-dot line reflect the 2-D model with half and twice, respectively, of the extracted viscosity to show the sensitivity of the fit to the viscosity.

removes the time dependence of the strain on the island size. Therefore, all data points for different island sizes during the annealing will fall on a single curve if the relaxation scales in time as predicted by Eqn. 4.15. The prediction of the 2-D model [5] using a least square fit to all data points with viscosity as a single fitting parameter (1.3×10^{10} N*sec/m^2) is shown, along with the 1-D model using the same viscosity. The difference between the 1-D and 2-D models is small, within the error bar of the experimental data. Fitting results with 2η and $\eta/2$ are also plotted. They do not fit the experimental data well, which shows the viscosity accuracy η extracted by this method has an error less than a factor of two. Table 4.1 [6] lists the values used for the mechanical properties. All data points from different island sizes fall on a single curve as expected.

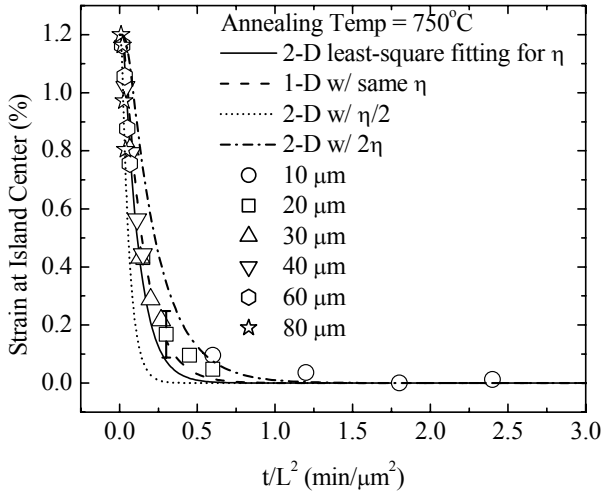
Table: 4.1: Mechanical properties [6] of Si and SiGe films (linearly interpolated between Si and Ge). E is Young's modulus and ν is the Poisson ratio, defined as $\nu = \frac{c_{12}}{c_{11} + c_{12}}$.

	E (10^{10} N/m^2)	c_{11} (10^{10} N/m^2)	c_{12} (10^{10} N/m^2)	ν
Si	13.0	16.5	6.35	0.28
$Si_{0.7}Ge_{0.3}$	12.2	15.4	5.89	0.28
$Si_{0.4}Ge_{0.6}$	11.4	14.3	5.43	0.28

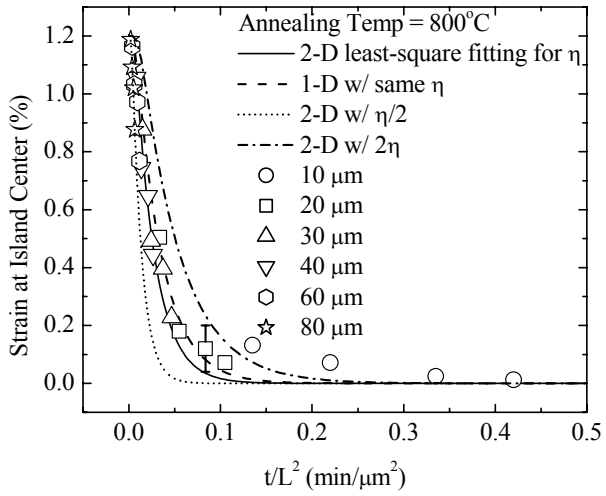
Figure 4.3 shows the strain at the center of islands, measured by Raman scattering, over time for islands of various sizes at different temperatures from above, 750°C and 800°C. Because the strain first relaxes at the island edges, the strain at the island center is slower to relax than the average strain. Again, the viscosity value is extracted by fitting data to the 2-D model, with resulting values of 5.5 × 10^{10} N*sec/m^2 at 750°C and 1.1 × 10^{10} N*sec/m^2 at 800°C.

Figure 4.4 shows the strain distribution measured by Raman spectroscopy across a 60 μm x 60 μm island along the diagonal direction after a 17-min anneal at 790°C. As described qualitatively in Sec. 3.4, the strain relaxes first on the boundary and the relaxation propagates towards the center.

The viscosities (1.1 x 10^{10} N*sec/m^2 at 800°C) we extracted by fitting our data to models are higher than those expected based on the composition of the BPSG film and prior characterization of BPSG(1 - 3 x 10^8 N*sec/m^2 at 800°C for a glass with 4.4% B and 4.1% P by weight) [7]. The boron and phosphorus content values were provided by the supplier of the BPSG films (K. Hobart of NRL and T. Margarella of Northrop-Grumman) and we did not independently measure to confirm them. The viscosity discrepancy could be due to uncertainty in the BPSG composition, an uncertainty in the relationships between composition and viscosity and/or viscosity and temperature, or an unknown enhancement of viscosity in very thin films or the fact that the model we used has a consistent bias. If the error were due to the BPSG composition, boron content of 2% would be required to explain the high viscosity we measured. Nevertheless, this section



(a)



(b)

Figure 4.3: Strain at the island center, measured by Raman scattering, as a function of normalized anneal time at (a) 750°C and (b) 800°C for island size from 10 μm to 80 μm. Open symbols are experimental data. The typical error bar in the strain measurement is +/-0.075%, as shown on one data point. Least-square fitting based on the 2-D model [5] gives rise to the solid line with the only fitting parameter (viscosity) of 5.5×10^{10} N*sec/m^2 (750°C) and 1.1×10^{10} N*sec/m^2 (800°C). The dashed line is the 1-D model using the same viscosity. The short-dot line and the dash-dot line reflect the 2-D model with half and twice, respectively, of the extracted viscosity to show the sensitivity of the fit to the viscosity.

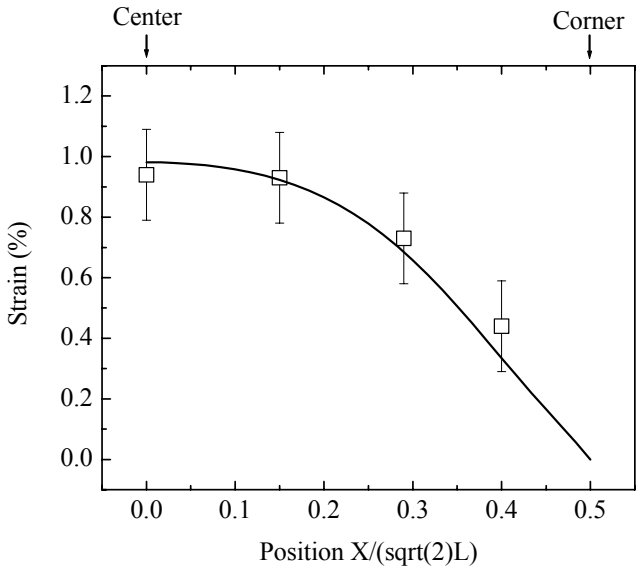


Figure 4.4: Strain distribution along the diagonal of a 60 μm x 60 μm island after a 17 min annealing at 790°C. Open squares are experimental data and the solid line is the fitting based on the 2-D lateral expansion theory [5] using viscosity of 1.3×10^{10} N*sec/m^2. The surface roughness RMS of the island center is about 1 nm due to buckling, and has negligible contribution to strain relaxation. L denotes the island edge length, which is 60 μm in this case.

demonstrates that we can quantitatively model the average lateral island relaxation as well as the profile of the relaxation across the island.

4.2 Accelerated lateral expansion in bi-layer structures on BPSG

To achieve a faster lateral expansion and strain relaxation of SiGe islands on BPSG, one can simply increase the SiGe thickness (h_f), as thicker films are elastically stronger and thus laterally expand faster as indicated by Eqn. 4.15. However, the SiGe film thickness is limited by critical thickness constraints due to original growth on the Si(100) substrate.

To circumvent the critical thickness constraint, a capping film of a different material is added onto the SiGe layer to accelerate lateral expansion (Fig. 4.5). Assuming a capping layer A on top of the SiGe, Eqn. 4.15 can be easily modified when layers relax

elastically. Following the same derivation detailed in the previous section, the time constant for lateral expansion of bi-layer square islands on BPSG becomes

$$\tau_L = \frac{\eta L^2}{(c_{11SiGe} h_{SiGe} + c_{11A} h_A) h_g}, \tag{4.17}$$

where c_{11A} and h_A refer to the elastic constant and the thickness of the film A. Compared with the single layer formula Eqn. 4.15, it is clear that the bi-layer can be treated as a single SiGe layer with an effective thickness:

$$h_{SiGe}(effective) = h_{SiGe} + \frac{c_{11A}}{c_{11SiGe}} h_A . \tag{4.18}$$

This increased effective SiGe thickness speeds up the lateral expansion of the islands. We will see in the next chapter that capping layers suppress buckling in addition to speeding lateral relaxation so they are especially attractive from a technological point of view.

In our experiments, the bi-layer structure comprising 30-nm initially strained SiGe on top of 25-nm initially unstrained Si on 200-nm BPSG was fabricated using the wafer-bonding and Smart-Cut® processes mentioned in the previous chapter. Note that even though in this case the silicon layer is underneath the SiGe as opposed to on top as in Fig. 4.5, this does not affect the lateral expansion study of this bi-layer structure and Eqn. 4.18 still applies. The strain at the center of islands ranging from 30 μm to 60 μm in edge width was measured as a function of annealing time at 800°C in nitrogen. Figure 4.6 shows the strain relaxation of islands made of a single 30-nm SiGe layer on 200-nm BPSG, along with the theoretical calculations based on parameters listed in Table 4.1 and the viscosity η extracted in the single layer experiment using the 2-D model. The x axis is the annealing time normalized by the square of the island edge width, which removes the time dependence of the strain on the island size as in Fig. 4.3. It is clear that the bi-layer islands reached equilibrium faster than their single-layer counterparts, confirming the accelerated lateral expansion in bi-layer structures. The good agreement between experimental data and the calculation, as shown in Fig. 4.6, stresses the validity of the modified theory (Eqn. 4.17) for the bi-layer structure. Finally, the data for the 30 μm and 60 μm islands in each case can be modeled via a single curve, showing that the relaxation time indeed scales as the square of the island edge width L.

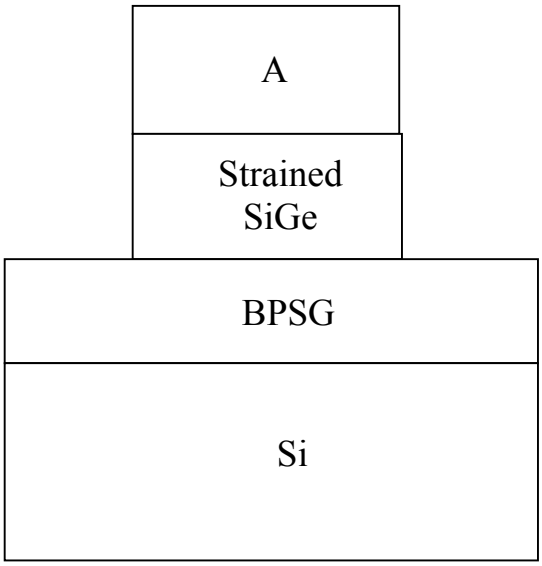


Figure 4.5: Schematic of a bi-layer structure (SiGe with a capping layer A) on BPSG.

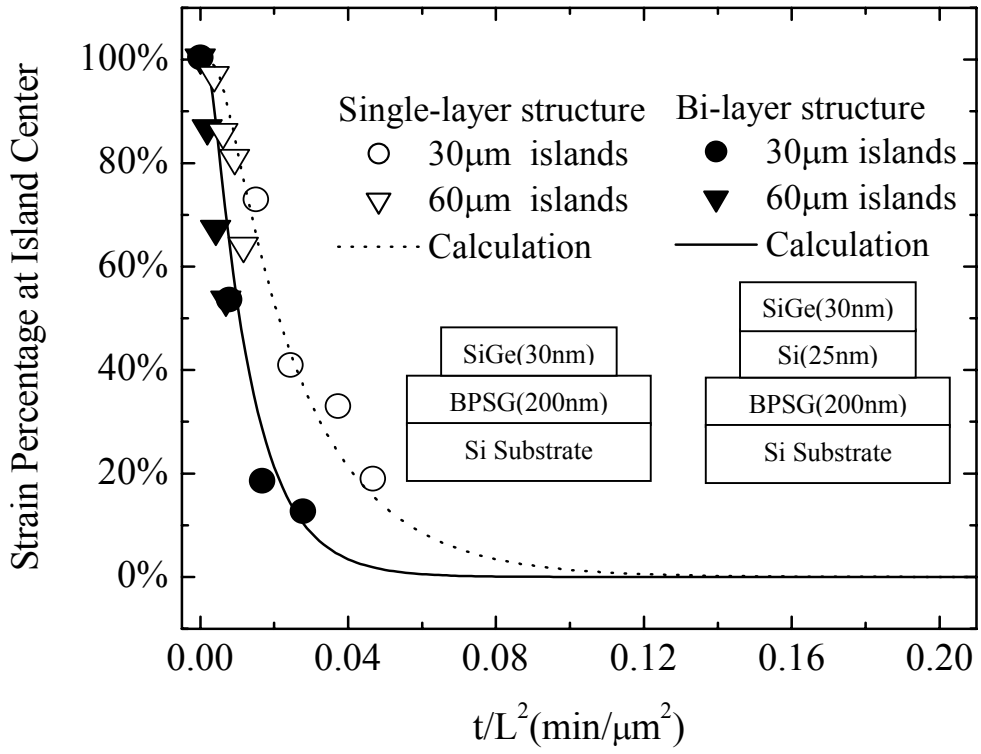


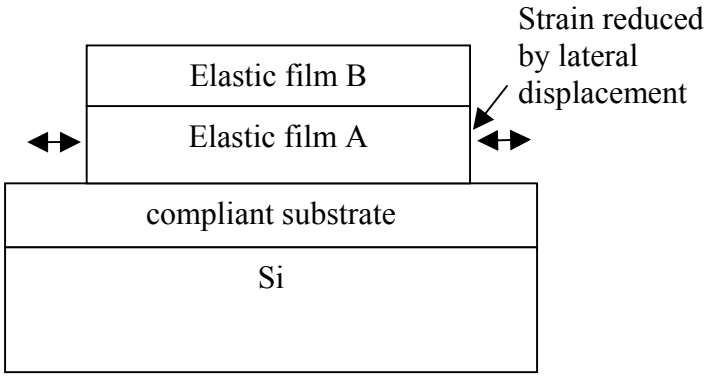
Figure 4.6: Strain percentage at the SiGe island center, defined as 100% before relaxation and 0% upon equilibrium and measured by Raman spectroscopy, as a function of normalized annealing time at 800°C for island size of 30 μm and 60 μm. Symbols are experimental data. The curved lines are from the 2-D lateral expansion model based on the parameters in Table I [5]. The single-layer and bi-layer islands are made of 30 nm $Si_{0.7}Ge_{0.3}$ and 30-nm $Si_{0.7}Ge_{0.3}$/25-nm Si, respectively.

4.3 Introduction to stress balance on compliant substrates

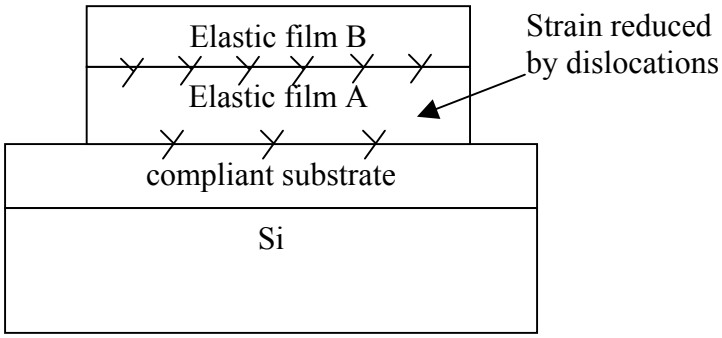
The ideal compliant substrate allows a thin film above to expand or shrink, thus reducing the strain energy in the system, without the formation of defects such as dislocations. In practice, pseudomorphic strained layers are often grown on top of these templates (such as the SiGe/Si bi-layer structures discussed in the previous section) and the whole structure is then annealed to further adjust the lattice constant. Ideally, this relaxation step is also accomplished without dislocations (e.g. at the interface between the template and the top layer) so that all layers remain coherent, as has been commonly assumed in many compliant substrate studies [1,2,8-10]. In such a coherent case, the strain in both layers change at the same rate. However, in the case where such a structure has been examined in detail, coherence was not observed [11], leading to uncertainty about the nature of the compliance mechanism.

Consider two layers on top of a compliant substrate (Fig. 4.7). When the strain energy is minimized by coherent displacement of the top two layers and the compliant substrate (Fig.4.7(a)), the introduction of dislocations or other kinds of defects is not required. The original strain is partitioned between layers. When the strain energy in the system is reduced by dislocation formation (Fig. 4.7(b)), there are no longer coherent interfaces between layers. The compliancy, however, manifests itself by modifying the dislocation dynamics. For example, the dislocation density in lattice-mismatched SiGe grown on thin silicon-on-insulator (SOI) is found to be dramatically decreased because the image force from the Si/SiO_2 interface hinders dislocation propagation into the top SiGe layer [12]. The fact that dislocations render interfaces between layers no longer coherent suggests that stess balance in layers on a compliant substrate is a key test on the mechanism of compliancy. Without clear evidence of strain partitioning, it has been suspected that some approaches of compliant substrates in III-V materials actually take advantage of the change in dislocation dynamics [11,13].

In the next section, we clearly show a coherent relation of bi-layers made of Si/SiGe and of SiO_2/SiGe on a compliant BPSG film. The coherence is shown by measuring the time dependence of strain and the final strains in these two films.



(a)



(b)

Figure 4.7: Schematic diagram of compliance mechanisms. (a) Strain energy is minimized by lateral displacement of the elastic layers and the compliant substrate. Coherent interfaces between them are retained. (b) Strain energy is reduced by the formation of dislocations, which render the interfaces incoherent. (Dislocations are only relevant at the lower interface for a crystalline compliant substrate)

4.4 Coherent interface and stress balance between Si/SiGe and SiGe/SiO_2 on BPSG

The coherent relaxation of different samples of four structure types on BPSG was studied. In the first experiment, compressively strained $Si_{0.7}Ge_{0.3}$ (30nm, strain ε_0 = -1.2%) on relaxed-Si (25nm), transferred onto BPSG, was patterned into 30 x 30 μm^2 islands (Figure 4.8 inset). Upon annealing at 800°C in nitrogen to reduce the viscosity of BPSG and thus remove the mechanical constraint from the substrate, the compressively strained SiGe layer expands to lessen the strain and the Si layer is stretched to become tensile (Fig. 4.8). That the same increase in strain (~0.6%) in both layers is seen clearly implies an absence of slippage or misfit dislocations between the Si and SiGe layers. Further, one can predict the final strains of the annealed samples by stress balance between the layers:

$$\sigma_{SiGe} h_{SiGe} + \sigma_{Si} h_{Si} = 0\,, \tag{4.19}$$

where σ represents film stress under equal biaxial stresses ($\sigma_{11} = \sigma_{22} = \sigma$) and h refers to film thickness. Along with the assumption of a coherent interface between the Si and SiGe layers, Eqn. 4.19 predicts:

$$\varepsilon_{SiGe} = \varepsilon_0 \frac{(1-\nu_{SiGe})E_{Si}h_{Si}}{(1-\nu_{Si})E_{SiGe}h_{SiGe} + (1-\nu_{SiGe})E_{Si}h_{Si}} = \text{-0.56\%}, \tag{4.20}$$

$$\varepsilon_{Si} = -\varepsilon_0 \frac{(1-\nu_{Si})E_{SiGe}h_{SiGe}}{(1-\nu_{Si})E_{SiGe}h_{SiGe} + (1-\nu_{SiGe})E_{Si}h_{Si}} = 0.64\%. \tag{4.21}$$

E and ν refer to the films' Young's Modulus and Poisson's ratio, respectively, whose values are listed in Table 4.1. The good agreement of the observed final strains with the predictions by stress balance is further evidence of the relaxation by compliant BPSG without dislocations. Note that in such a bi-layer, it is also expected that curling should occur with the compressively-strained SiGe to force the silicon to bend down. Since this involves a large mass flow of the underneath BPSG, it is a slow process and only affects the regions really close to the island edges. Therefore, this effect is ignored in our study.

A second experiment was performed to verify that the stress balance between the layers governs the mechanical equilibrium. Epitaxial unstrained silicon of various thicknesses was grown at 700°C by rapid thermal chemical vapor deposition (RT-CVD)

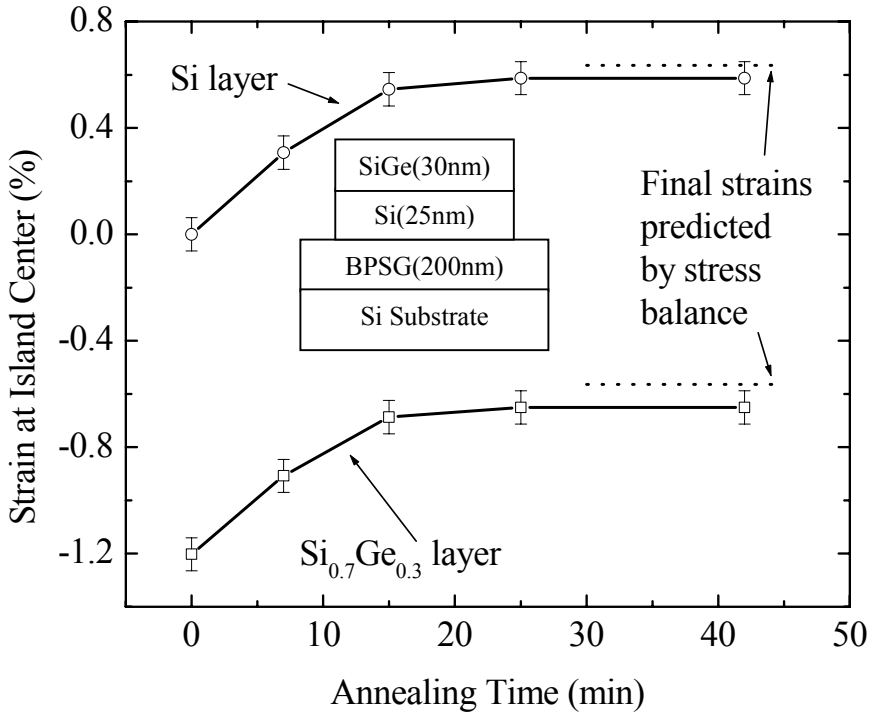


Figure 4.8: Strain evolution of Si and $Si_{0.7}Ge_{0.3}$ films as they reach stress equilibrium during an anneal at 800°C. The strains are measured at the center of a 30 μm x 30 μm island. The final equilibrium state agrees with the predicted stress balance between Si and $Si_{0.7}Ge_{0.3}$ films, depicted by the dotted lines. The strains in the two layers change at the same rate, showing that the two layers remain coherent.

on a compressively strained 30-nm $Si_{0.7}Ge_{0.3}$ layer on BPSG before relaxation (Fig. 4.9 inset). This structure was patterned to 30-μm square islands and then annealed in nitrogen at 800°C long enough to reach mechanical equilibrium (1 to 3 hrs). Figure 4.9 shows the final equilibrium strains in the two layers as a function of the top Si thickness, both experimentally measured and also predicted by stress balance (Eqns. 4.20 and 4.21). Again, excellent agreement was observed.

Up to this point, the strain partition has been examined only during the lateral expansion of elastic layers. To demonstrate the full capability of strain engineering using the viscous BPSG film, the lateral shrinkage of elastic layers during the stress balance process was also examined. In a third experiment, 30-μm square islands of 30-nm $Si_{0.7}Ge_{0.3}$ on BPSG were first almost fully relaxed at 800°C. A 30-nm Si layer was commensurately and selectively deposited on the relaxed $Si_{0.7}Ge_{0.3}$ islands by RT-CVD (Fig. 4.10 inset). The measured tensile strain in the Si layer was about 1.1%, as expected for pseudomorphic epitaxial Si on relaxed $Si_{0.7}Ge_{0.3}$. This structure was annealed for 1 hr at 800°C in nitrogen to reach equilibrium (Figure 4.10). Again, stress balance accurately predicts the final strains.

Finally, we show stress balance with a deposited amorphous oxide layer, instead of epitaxial, crystalline layers. A SiO_2 layer was deposited on a compressively-strained 30nm $Si_{0.7}Ge_{0.3}$ layer on BPSG by plasma-enhanced CVD at 250°C. The SiO_2/SiGe stack was patterned to 30-μm square islands and was then annealed at 800°C for 2 hr to reach an equilibrium state (Fig. 4.11 inset). Because we were not familiar with an easy way to measure the strain in the oxide layer on a small island, only the strain in SiGe layer was measured (Fig. 4.11). It was observed that thicker oxides lead to less relaxation of the SiGe than that expected from stress balance. The data was modeled assuming zero stress in the as-deposited oxide layer and stress balance between the SiGe and oxide layers. A single fitting parameter of $\frac{E_{oxide}}{1-\nu_{oxide}}$ (best fit of 8.5 x 10^{10} N/m^2) was used to describe the oxide. A fitting parameter was used because the oxide properties are known to vary with deposition conditions. Again good agreement of the data with stress balance theory was observed, implying that the SiGe relaxed only through lateral expansion and not via dislocations.

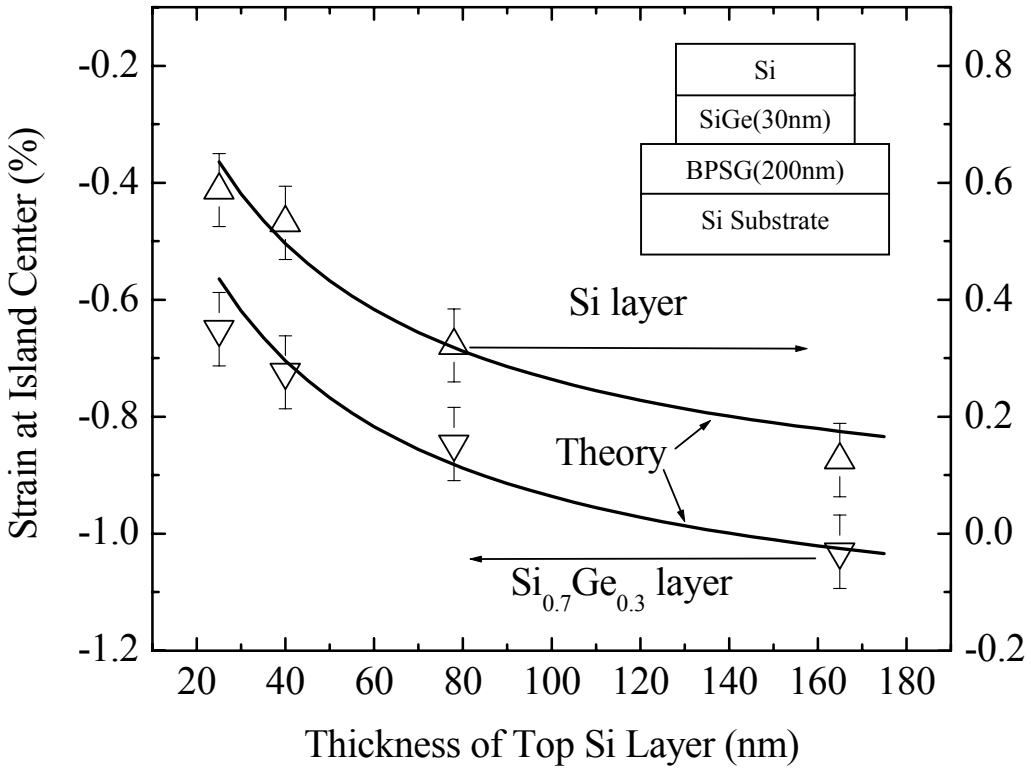


Figure 4.9: Biaxial strains of 30-nm $Si_{0.7}Ge_{0.3}$ and Si at the center of a 30 μm x 30 μm island as a function of silicon thickness after anneals (1 to 2 hr) at 800°C to reach equilibrium. Open symbols are experimental data. Lines are calculation of stress balance based on the elastic parameters in Table 4.1 assuming the two layers remain coherent.

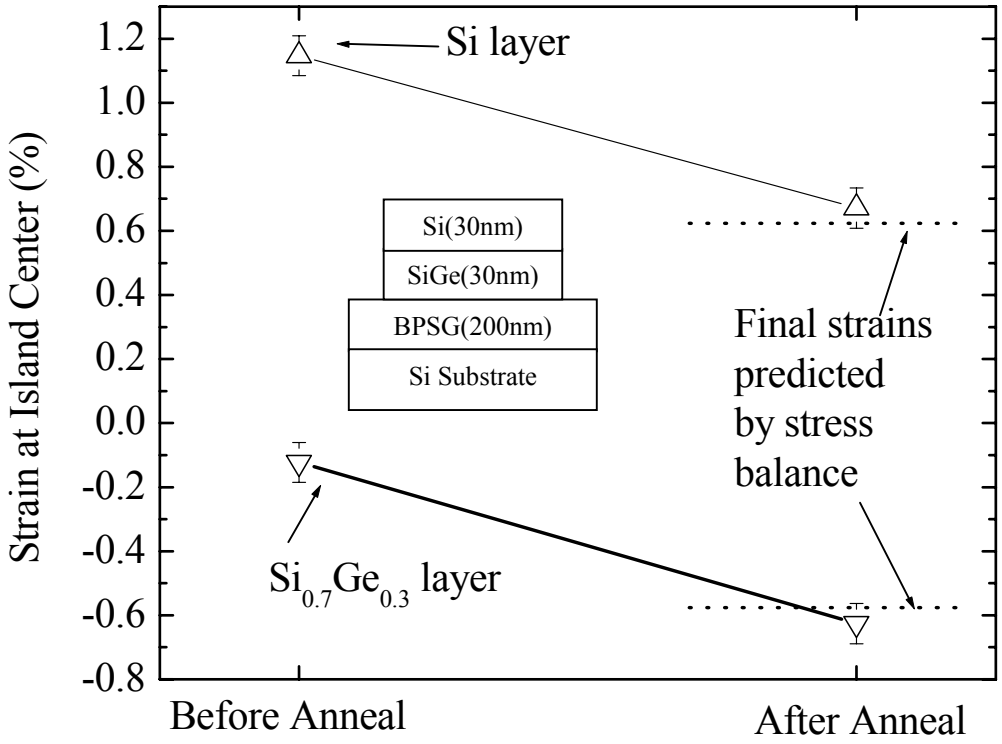


Figure 4.10: Biaxial strain of $Si_{0.7}Ge_{0.3}$ and Si at the center of an initially relaxed 30 μm x 30 μm $Si_{0.7}Ge_{0.3}$ island before and after an anneal. Open symbols are experimental data and dotted lines are calculation of stress balance.

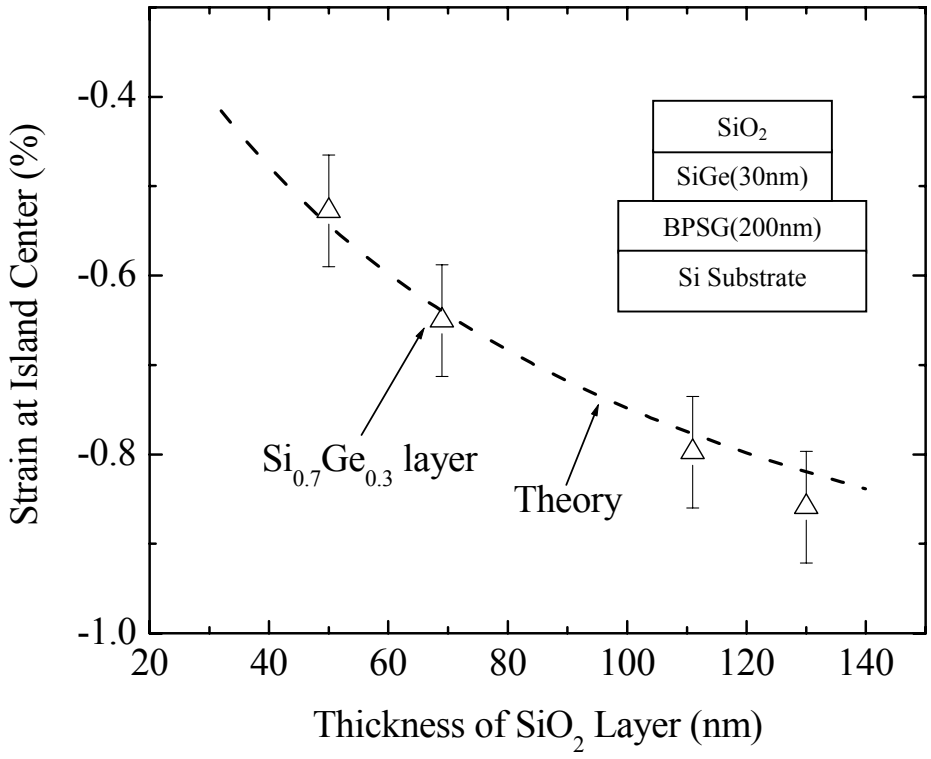


Figure 4.11: Biaxial strain of the initially compressively-strained 30nm $Si_{0.7}Ge_{0.3}$ at the center of a 30 μm x 30 μm island, after deposition of PECVD-SiO_2 and an anneal, as a function of PECVD-SiO_2 thickness. Open symbols are experimental data and the dashed line is a fitting based on stress balance.

4.5 Use of geometry to create uniaxial stress

Recently, uniaxial strain in silicon has been reported to enhance hole mobility much higher than expected [14] and the enhancement was found to hold up at high vertical electric field, at which biaxial-strain induced enhancement usually diminishes [15]. These all suggest that anisotropy in strain delivers much more improvement in carrier transport than people have expected.

In this section, rectangular islands were used to create different strain in the x and y directions [16-18]. In the next section, this was combined with the stress balance of SiGe/Si bi-layers to create orthorhombically-strained thin Si films on BPSG [16-18].

The two-dimensional nature of the SiGe patterns on BPSG gives us a unique opportunity to vary the dimensions in the two in-plane directions separately, enabling independent control of in-plane strain along different directions. The SiGe geometry can be made with different sizes in different directions, leading to dramatically different relaxation rates in different directions. In one extreme case, consider a long, narrow, compressively strained SiGe stripe aligned in [010], as shown in Figure 4.12(a). The SiGe stripe is initially under biaxial, compressive strain ε_0 (Fig. 4.12(b)). When the viscosity of the BPSG is reduced at high temperature, the stress in the [100] direction, $\sigma_{SiGe}[100]$, quickly reaches zero as the lateral expansion along this short direction is fast, whereas the strain $\varepsilon_{SiGe}[010]$ in the long direction remains unchanged at ε_0, resulting in a uniaxial stress in the [010] direction.

Note that the SiGe lattice in the [100] and [001] directions actually expands beyond its strain-free state according to the Poisson ratio to give tensile strain in these directions as a result of the compressive strain in the [010] direction (Fig. 4.12(c)) [17]. One should pay special attention to the difference between stress and strain: strain is lattice deformation whereas stress is a force. In the above case after relaxation, the SiGe lattice is strained in all directions: tensile in the [100] and [001] directions and compressive in the [010] direction. But it is only under stress (compressive) in the [010] direction. The stress in the [100] direction is zero because the BPSG has allowed the layer to flow in this direction, so that it applies no force to the film in this direction. The stress in the [001] direction is zero as it is a free surface.

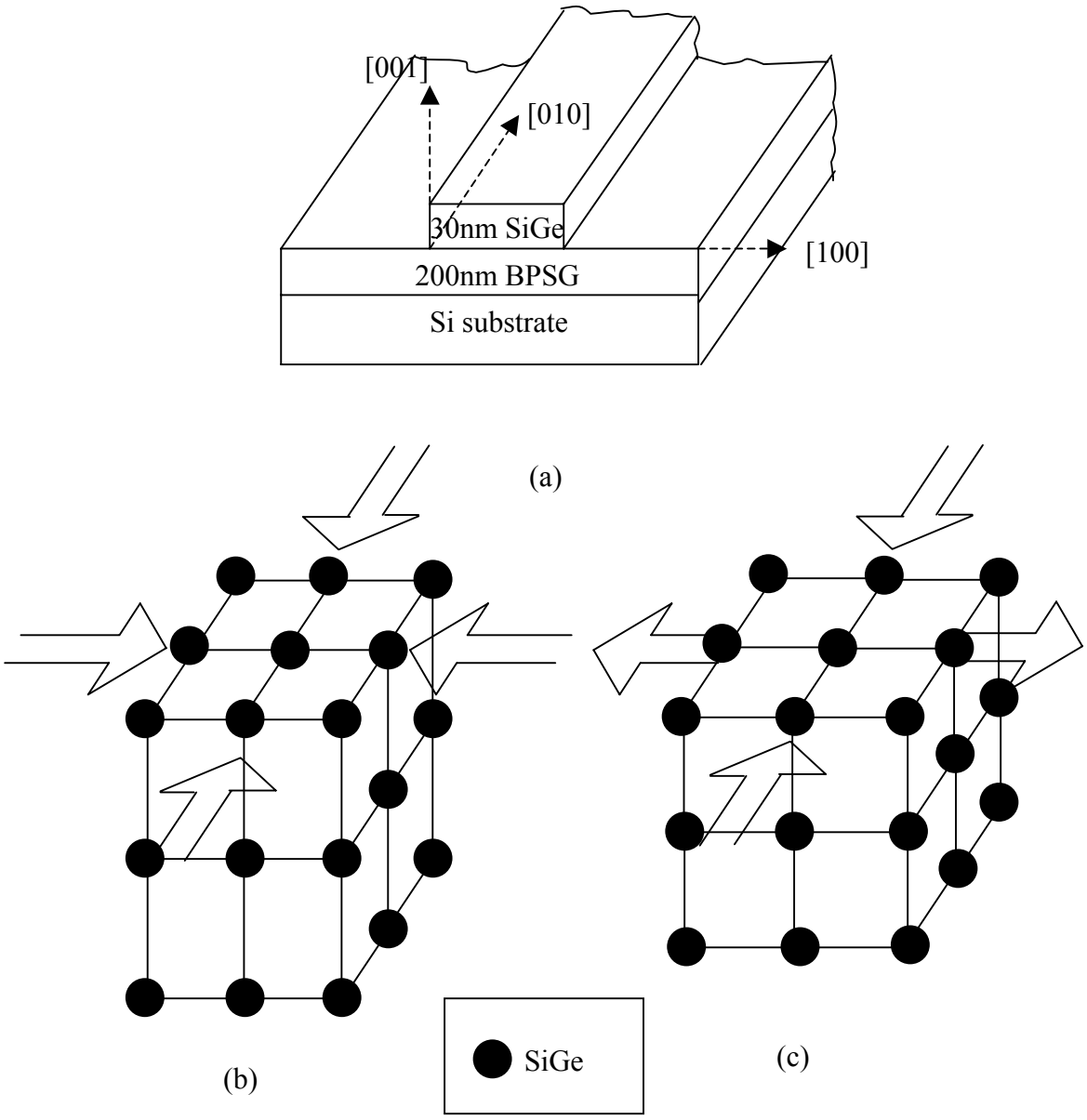


Figure 4.12: Uniaxial stress in a SiGe stripe. (a) Schematic diagram of a SiGe stripe on BPSG with long direction in the [010] direction. (b) Atomic structure of the SiGe stripe illustrates that SiGe is initially under biaxial, compressive strain. The inward arrow denotes a compressive strain. (c) Atomic structure of the SiGe stripe after stress relaxation in [100] shows the strain in [010] does not change while the strain in [100] becomes tensile according to Poisson ratio. The outward arrow denotes a tensile strain. The strain in the [001] direction is not shown by arrows.

To realize the strain control using the island geometry as described above, the anneal time needs to be carefully chosen: long enough to relax the strain in the short direction but not too long to change the strain in the long direction. Since the time scale of the strain relaxation is a strong function of the dimension (Eqn. 4.15), there is a large process window in which strain can be readily controlled by geometry. Figure 4.13 shows the calculated strain percentage versus anneal time at 800°C for a 150 μm x 10 μm 30-nm $Si_{0.7}Ge_{0.3}$ stripe on 200-nm BPSG. The process window is between 7 and 208 mins.

In the experiments, we patterned 30-nm fully biaxial-strained (ε_0 = 1.2%) $Si_{0.7}Ge_{0.3}$ films on 200-nm BPSG into 150-μm-long stripes aligned in the [010] direction with various widths ranging from 10 to 150 μm, followed by a 15-min anneal at 800°C in nitrogen. Figure 4.14(a) shows the smoothed Raman peaks for the Si-Si phonon measured at the center of $Si_{0.7}Ge_{0.3}$ stripes for different widths. The 511 cm^{-1} peak represents full biaxial strain. The Raman peak for full biaxial relaxation should be at 502 cm^{-1}. The Raman peak for narrow stripes was observed to stabilize around 505.5 cm^{-1}, in agreement with uniaxial stress in [010] with strain level at 1.2% (Appendix III). Figure 4.14(b) summarizes the stress relaxation in the short direction calculated from the Raman peak shift (Appendix III). For stripes wider than 100 μm, little strain relaxation was observed and the original biaxial strain was retained. For stripes narrower than 20 μm, the stress was fully relaxed in [100], yielding a uniaxial, compressive stress in [010], the long direction. Modeling, based on a one-dimensional lateral expansion theory, is also shown in Fig. 4.14(b). The orientation of the uniaxial stress obtained in narrow stripes is always along the long direction and is readily controllable. While the above results were obtained with the stripes along the [010] direction, uniaxial stress along [110] direction has also been obtained by rotating the stripe by 45 degrees.

In the above experiments, annealing times have been chosen to avoid SiGe buckling, which can take place for longer annealing times. Buckling will be addressed in the next chapter. Since buckling is driven by compressive stress [19], it is expected that buckling only occurs in the long direction on stripes, in contrast to buckling in two directions for biaxial stress on very large islands. Figure 4.15 shows optical micrographs of the buckling patterns at the center of a 150 x 150 μm^2 SiGe island and a 150 x 10 μm^2 SiGe stripe, after a 70-min anneal at 800°C. Unlike the two-dimensional buckling pattern on

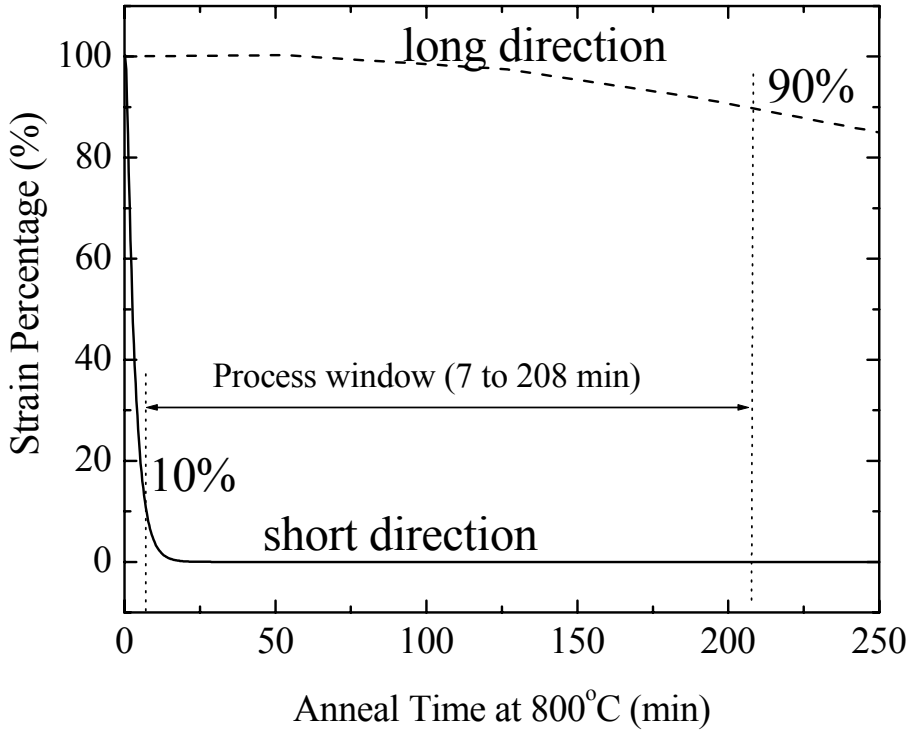
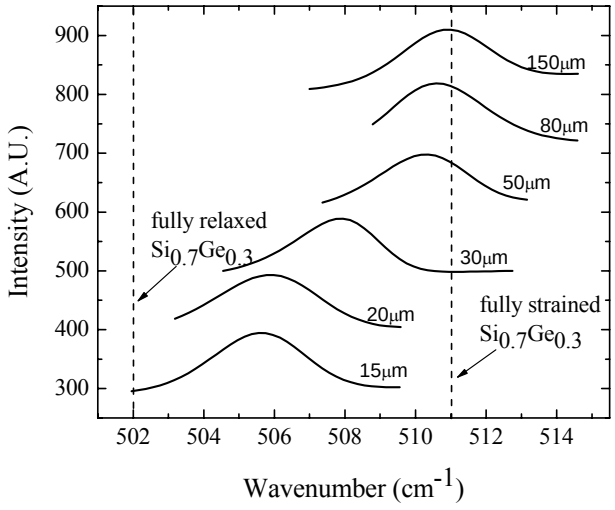
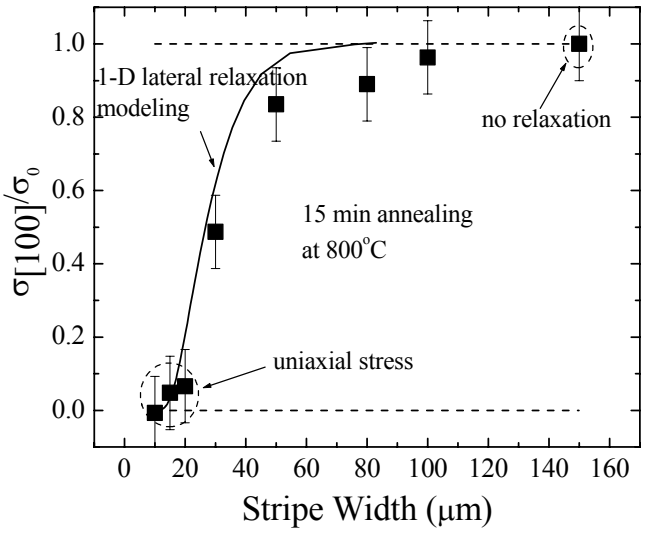


Figure 4.13: Calculated strain percentage of a 150 μm x 10 μm 30-nm $Si_{0.7}Ge_{0.3}$ stripe on 200-nm BPSG annealed at 800°C. The calculation is based on the 1-D lateral relaxation model described in Sec. 4.1.1. The process window is the anneal time range during which the strain in the short direction is less than 10% of the initial strain and the strain in the long direction retains more than 90% of the original strain.

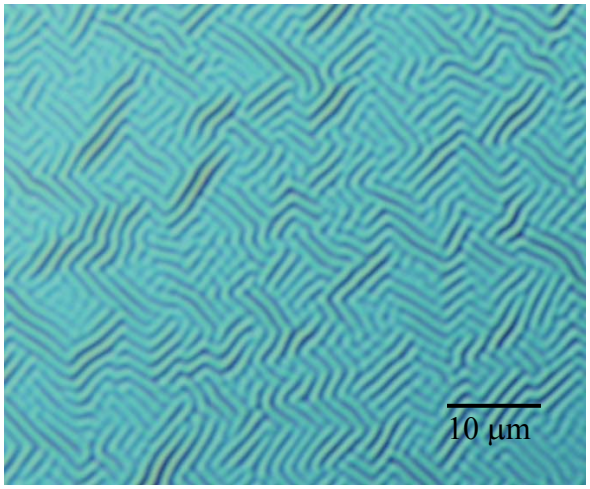


(a)



(b)

Figure 4.14: (a) Smoothed Raman peaks for Si-Si phonons measured at the center of 150-μm-long $Si_{0.7}Ge_{0.3}$ stripes with different widths after a 15-min anneal at 800°C in nitrogen. The Raman peak position shifted from 511 cm^{-1} (biaxial-strain of 1.2%) for wide stripes to 505.5 cm^{-1} (uniaxial stress in [010] with strain of 1.2%) for stripes narrower than 20 μm. (b) The measured ratio of the stress along [100] to the initial stress as a function of the strip width. The solid line is calculated from one-dimensional lateral expansion theory. A unity ratio means no strain relaxation, with the original biaxial strain retained. When the ratio equals to zero, the $Si_{0.7}Ge_{0.3}$ stripe is under uniaxial stress in the [010] direction. The BPSG thickness was 200 nm and a viscosity of 1.1 x 10^{10} N*sec/m^2 was assumed at 800°C for modeling.



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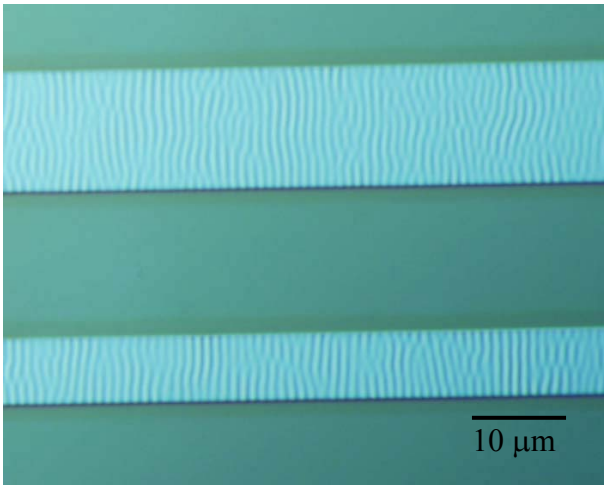

(b)

Figure 4.15: Optical micrographs of buckled 30-nm $Si_{0.7}Ge_{0.3}$ surface on 200-nm BPSG after a 70 min anneal at 800°C. (a) The biaxial, compressive stress at the center of a 150 x 150 μm^2 island gives rise to the two-dimensional buckling pattern. (b) Buckling only occurred along the long direction of the 150-μm strips, suggesting a uniaxial, compressive stress.

the SiGe square island (Fig. 4.15(a)), there is buckling only along the long direction on the SiGe stripe (Fig. 4.15(b)), which confirms the nature of uniaxial compressive stress in the SiGe stripe after annealing.

4.6 Orthorhombic strain in silicon by bi-layer structures

In this section, 150-μm-long SiGe/Si stripes, composed of compressively-strained (ε_0 = 1.2%) 30-nm $Si_{0.7}Ge_{0.3}$ and relaxed 25-nm silicon on 200-nm BPSG and aligned in the [010] direction, were annealed for 15 min at 800°C to generate orthorhombic strain in the initial strain-free Si film (Fig. 4.16). It has been shown in Sec. 4.4 that silicon and SiGe films could maintain a coherent interface and the final strains in SiGe and Si are governed by a biaxial-stress balance between the SiGe and Si films when square islands are used.

In the case of long SiGe/Si stripes, the strain of the films in the long direction, i.e. [010], were not altered after 15-min annealing at 800°C, since from Sec. 4.1 and Sec. 4.2 it is known that the 15-min annealing time is orders of magnitude smaller than that needed for the lateral expansion to traverse 150 μm. Therefore, after annealing, the strains along [010] in the SiGe and silicon films are

$$\varepsilon_{SiGe}[010] = \varepsilon_0 ,\ \varepsilon_{Si}[010] = 0 , \tag{4.22}$$

where ε_0 is the original value of the strain (biaxial) in the as-grown pseudomorphic SiGe film.

In the [100] direction, the SiGe film expanded quickly to release the compressive stress during the annealing. As a result, the underlying Si film was stretched in [100]. The coherent interface between SiGe and silicon films indicates that the strain changes by the same amount in both films

$$\varepsilon_0 - \varepsilon_{SiGe}[100] = 0 - \varepsilon_{Si}[100] \tag{4.23}$$

The lateral expansion of the SiGe/Si stripe in [100] proceeded until it reached a stress balance in [100]:

$$\sigma_{SiGe}[100]h_{SiGe} + \sigma_{Si}[100]h_{Si} = 0 \tag{4.24}$$

The silicon film was therefore under orthorhombic strain: zero strain in [010], tensile strain in [100] as a result of stretching, and compressive strain in [001] to accommodate

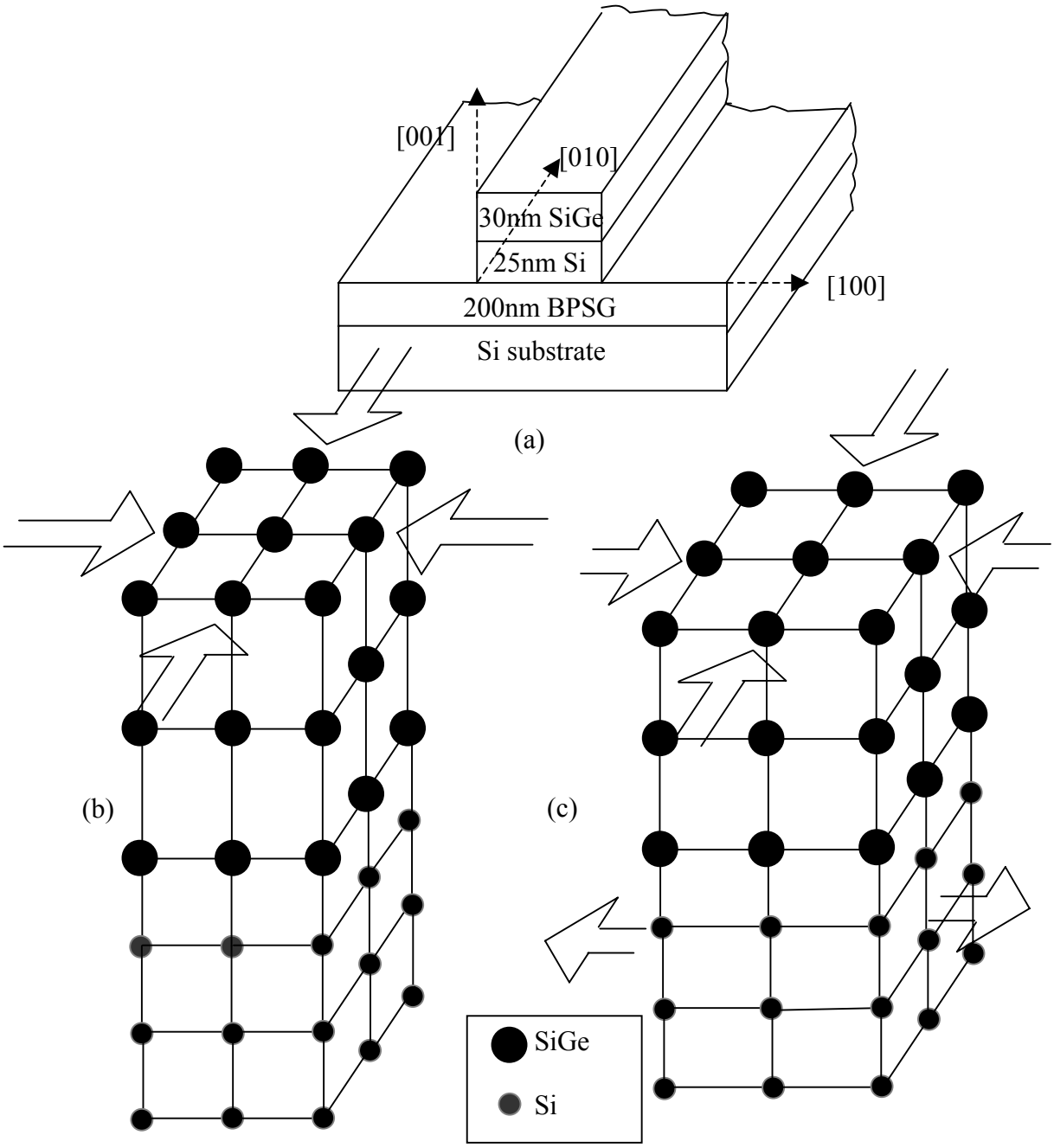

Figure 4.16: Orthorhombic strain in silicon using a SiGe/Si stripe. (a) Schematic diagram of a SiGe/Si stripe on BPSG with long direction in the [010] direction. (b) Atomic structure of the SiGe/Si stripe before annealing illustrates biaxially compressive SiGe and unstrained silicon. The inward arrow denotes a compressive strain. (c) Atomic structure of the SiGe/Si stripe after reaching stress balance in the [100] direction shows that the strain in the SiGe and silicon films along [010] does not change while the strain in the silicon film along the [100] direction becomes tensile as the compressive strain in the SiGe film along the [100] direction is partially relaxed.

the tensile strain in [100]. Note that although the strain $\varepsilon_{Si}[010]$ in the Si film is zero, the stress $\sigma_{Si}[010]$ in the Si film was non-zero in this case, otherwise the silicon lattice along [010] would shrink and become tensile according to the Poisson ratio to allow for elongation in [100]. The strains in SiGe and silicon films along the normal direction (namely, [001]) can be derived from the free surface condition ($\sigma_{SiGe}[001]=\sigma_{SiGe}[001]=0$) to be

$$\varepsilon_{SiGe}[001] = -\frac{c_{12\_SiGe}}{c_{11\_SiGe}}(\varepsilon_0 + \varepsilon_{SiGe}[100]),\ \varepsilon_{Si}[001] = -\frac{c_{12\_Si}}{c_{11\_Si}}\varepsilon_{Si}[100]. \qquad (4.25)$$

Substituting Eqns. 4.22, 4.23, 4.25 along with the linear stress-strain Eqn. 2.2 into 4.24, one can calculate the strain in the silicon film along the [100] direction:

$$\varepsilon_{Si}[100] = -\varepsilon_0 \frac{(c_{11\_SiGe} + c_{12\_SiGe} - 2c_{12\_SiGe}^2 / c_{11\_SiGe})h_{SiGe}}{(c_{11\_Si} - c_{12\_Si}^2 / c_{11\_Si})h_{Si} + (c_{11\_SiGe} - c_{12\_SiGe}^2 / c_{11\_SiGe})h_{SiGe}} \qquad (4.26)$$

Raman spectroscopy was again used to characterize strain in the silicon film. Figure 4.17 shows the Raman spectra for 150-μm-long SiGe/Si stripes with width of 15 and 150 μm after a 15-min anneal at 800°C. The Si film in the 150-μm wide stripe was still strain-free after the anneal, as expected from slow lateral expansion in wide stripes, while the Raman peak from the Si layer for the 15-μm-wide stripe shifted to a lower wavenumber, suggesting a tensile strain. Using the strain coefficient b = 361 cm^{-1} for orthorhombically-strained silicon (Appendix III), the tensile strain in the 15-μm-wide Si stripe along the short direction was calculated to be 0.77%, in good agreement with the prediction from Eqn. 4.26 (0.81%) using the elastic constants from Table 4.1. It is interesting that the orthorhombically-tensile strain generated in the SiGe/Si stripes is considerably larger than the biaxial tensile strain in SiGe/Si square islands (~0.60%) generated in the silicon film using the same SiGe/Si bi-layer. This can be explained by the fact that the SiGe film needs to stretch in only one direction in the stripe configuration, leading to increased strain in the stretched direction, in contrast to stretching in both ways for the biaxial case.

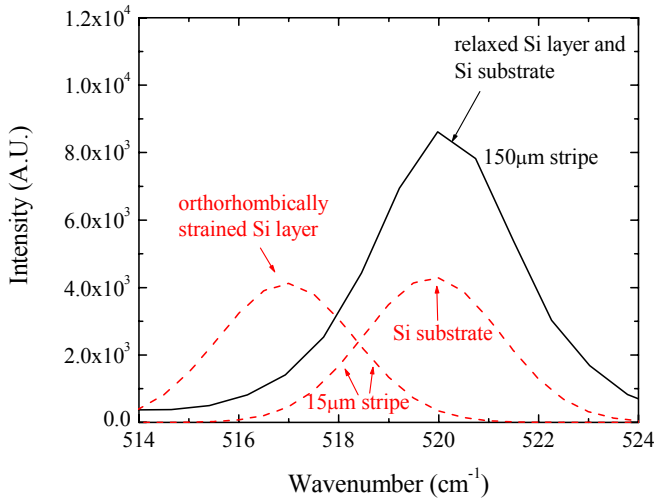

Figure 4.17: Raman spectra at the center of 150-μm long 30nm-SiGe/25nm-Si stripes after a 15-min anneal at 800°C for widths of 15 and 150 μm on 200-nm BPSG. The solid line represents the raw data for the 150-μm-wide stripe and the dashed lines are the de-convoluted curves after peak fitting for the 15-μm-wide stripe. The Si film in the 150 μm wide stripe remains relaxed, while the Si film in the 15-μm wide stripe is under stress along the short direction.

4.7 Summary

The lateral expansion of single layer (SiGe) and bi-layers (SiGe/Si and SiGe/SiO_2) on BPSG has been analyzed in detail. Lateral expansion experiments were carried out at various temperatures for different island sizes and agreed with modeling. We have confirmed coherent interfaces and stress balance in Si/SiGe and SiO_2/SiGe on viscous BPSG films. Governed by stress balance, the layers can either shrink or expand on the viscous BPSG to minimize strain energy. The formation of dislocations is unnecessary in this process. Various types of strain and stress, uniaxial and orthorhombic, have been realized using long stripe structures. In the next chapter, a second mechanism (buckling) for strain relaxation of SiGe on BPSG will be investigated.

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Chapter 5

Buckling of SiGe Islands on BPSG

The buckling of compressively-strained SiGe islands on viscous BSPG occurs because it lengthens the film and thus relaxes strain. It roughens the surface and causes serious problems for subsequent processing. It thus limits the size of islands that can be successfully laterally relaxed. In this chapter, we investigate the buckling of SiGe on BPSG and its suppression by modeling and experiments. The main points of this chapter are as follows. (1) Interplay of lateral expansion with buckling is the key factor determining the surface roughness. Buckling is initially dominant in large and thin islands. (Sec. 5.1) (2) Raising the temperature to lower the viscosity of BPSG enhances the rate of both processes equally and does not change the surface topology. For very long annealing times, however, the buckling disappears when lateral expansion reaches across islands. The flattening is effective only on islands up to 60 μm, since irreversible cracks form when buckling is above a certain value on larger islands. (Sec. 5.2) (3) To suppress buckling and thus avoid crack formation, a cap layer was used during the relaxation of SiGe on BPSG. Both epitaxial silicon and amorphous silicon dioxide (SiO_2) caps were investigated. Caps stiffen the islands to reduce buckling and accelerate the lateral relaxation, so that larger flat relaxed SiGe islands can be obtained. Using a 31-nm silicon cap, flat $Si_{0.7}Ge_{0.3}$ islands up to 200 μm x 200 μm were achieved. However, germanium diffusion in the SiGe/Si structure took place during relaxation anneals and lowered the germanium fraction of the final fully relaxed SiGe film. Silicon dioxide caps, which are not prone to germanium diffusion, allowed suppression of SiGe buckling without lowering the germanium percentage. Full relaxation of SiGe islands was achieved by a controlled multi-cycle procedure of silicon dioxide removal and anneal. (Sec. 5.3).

5.1 Quantitative study of buckling

The theory of buckling of a compressively-strained continuous film on a viscous layer was first developed by Sridhar *et al.* [1] and then refined by Huang *et al*. [2,3] and Sridhar *et al*. [4]. Surface buckling may be modeled as a superposition of many exponentially growing modes when the buckling amplitude is small in comparison to the thickness of the viscous layer. Each mode is a sinusoidal surface profile with a different wavelength, whose amplitude rises exponentially over time [1]:

$$A(t) = A_0 e^{t/\tau_B} \tag{5.1}$$

where A is surface roughness, A_0 is the initial surface roughness, and τ_B is the buckling time constant, which is determined by [1]

$$\frac{1}{\tau_B} = \frac{1}{\eta}\frac{E}{24(1-\nu^2)}\left[\frac{\sinh(2h_g k) - 2h_g k}{1+\cosh(2h_g k)+2(h_g k)^2}\right]\left[\beta(h_f k) - (h_f k)^3\right]. \tag{5.2}$$

k is the wavenumber of the mode and $\beta = 12\varepsilon_0(1+\nu)$. Using the parameters in Table 4.1 and Eqn. 5.2, the product of viscosity and the inverse of exponential time constant (η/τ_B) as a function of the buckling wavenumber is plotted in Fig. 5.1. Due to the exponential growth of the modes over time, it is assumed that the fastest growing mode will eventually dominate the final surface topology, which greatly simplifies our comparison between the theory and experiments. This single mode assumption leads to a predicted exponential growth of the surface roughness as long as the buckling does not significantly alter the strain. This model also neglects any reduction of strain from lateral relaxation, so it is valid for an infinite film or near the center of large islands.

Figure 5.2 shows the RMS surface roughness at the center of 200 μm × 200 μm islands as a function of anneal time, which is expected to be similar to that of a continuous film. The data represented by open squares (SiGe thickness of 30 nm) are discussed at this point and the other set will be addressed in the next section. The surface roughness at small amplitude grows exponentially with time as predicted. It then saturates for long annealing times because buckling reduces the strain, which is the driving force for the buckling.

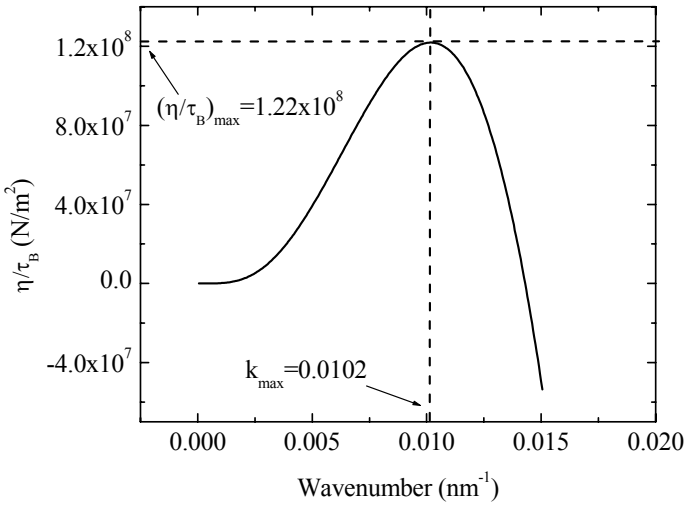


Figure 5.1: Product of the viscosity and the inverse of the exponential buckling time constant (η/τ_B) as a function of buckling wavenumber, based on Eqn. 5.2 and the parameters in Table 4.1. The values of h_f and h_g are 30 nm and 200 nm, respectively.

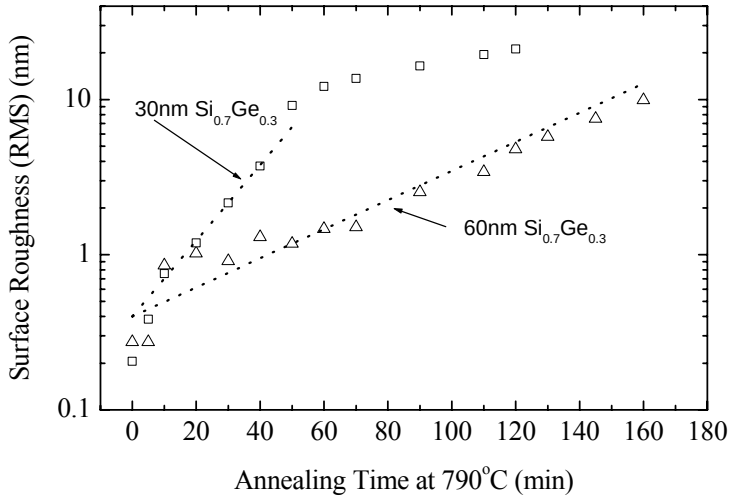


Figure 5.2: Surface roughness vs. annealing time at 790°C for $Si_{0.7}Ge_{0.3}$ of thickness 30 nm and 60 nm, measured at the center of 200μm x 200μm square islands. Open symbols are experimental data and dotted lines are fits to a simple exponential growth. The fitted buckling time constants are18 min (30 nm) and 46 min (60 nm).

5.2 Achieving lateral relaxation vs. buckling

In this section, the trade-off between desired lateral relaxation and undesired buckling is examined using the models developed for lateral relaxation (Chapter 4) and for buckling (Sec. 5.1) as well as experiments. Modeling in this regime where both lateral expansion and buckling are present is more complicated than that discussed above for regimes where only lateral relaxation (small islands) or buckling (large islands) are considered [3,5]. The cases examined are (i) varying the temperature (and/or the glass viscosity), (ii) increasing the SiGe thickness, and (iii) using very long annealing times.

5.2.1 Varying temperatures and viscosity

First, the annealing temperature was varied from 750^{o}C to 800^{o}C to change the viscosity from 5.5×10^{10} to 1.1×10^{10} N*sec/cm^{2}, as measured in chapter 4. The lower viscosity allows a faster lateral relaxation, as expected from Eqn. (4.15) and as observed by comparing the time scale of Figs. 4.3(a) and 4.3(b). From Eqn. 5.2, the buckling time constant also is expected to decline as viscosity is decreased. Both time constants scale similarly with viscosity, namely to the first power. Therefore, one expects lowering the viscosity (either by temperature or by changing the glass composition) will increase the rate of both processes equally, but not favor one over the other. This is supported experimentally. Note that Fig. 5.3 shows the evolution of surface roughness versus strain in the center of the islands at 750^{o}C and 800^{o}C. For all island sizes, as the sample is annealed the strain decreases and the surface roughness increases. Large islands roughen more than small islands for the same amount of relaxation. The evolution is similar for 750^{o}C and 800^{o}C for each island size as annealing progresses. Most significantly, although the points plotted represent very different time spans at 750^{o}C and 800^{o}C (240 vs. 40 min, respectively) the evolution of roughness vs. strain is very similar. Therefore, simply changing the viscosity does not solve the buckling problem.

5.2.2 SiGe thickness

Eqn. 4.15 predicts a faster lateral relaxation for thicker SiGe layers, as discussed in Chapter 4. A thicker SiGe layer is also expected to have a larger buckling time constant

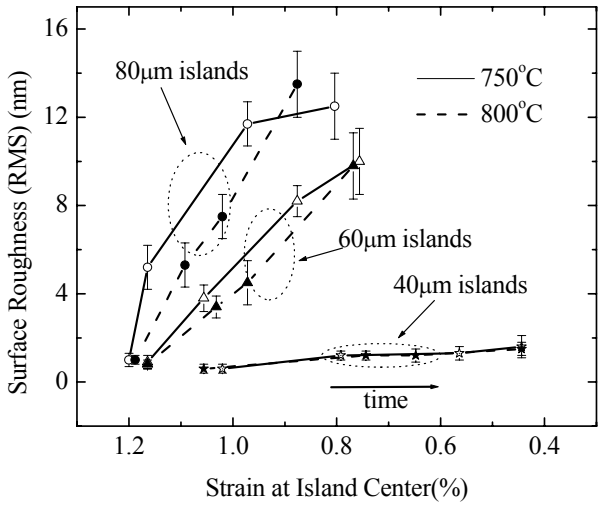


Figure 5.3: Experimental data for the evolution of surface roughness vs. strain at the center of square islands at 750°C and 800°C for 40, 60 and 80 μm islands. For each island size and temperature, multiple anneal times were used to progressively decrease strain. The longest anneal times at 750°C and 800°C are 240 min and 40 min, respectively.

because the SiGe layer is stiffer. For example, Eqn. 5.2 predicts that raising the SiGe thickness from 30 to 60 nm should increase the buckling time constant by a factor of 2.6. More sophisticated modeling supports these trends of preferred lateral relaxation vs. buckling for thick islands [5].

Experimentally, it is difficult to increase the original SiGe strained layer thickness because of the critical thickness constraint. Therefore, after a 30-nm $Si_{0.70}Ge_{0.30}$ layer was transferred to the BPSG and the original substrate was removed, a further layer of 30-nm $Si_{0.70}Ge_{0.30}$ commensurately strained film was grown by RT-CVD on the existing fully strained 30-nm $Si_{0.70}Ge_{0.30}$/BPSG, making the total thickness of $Si_{0.7}Ge_{0.3}$ to be 60-nm. A short low temperature (800°C) hydrogen bake was able to remove the native oxide before the epitaxial growth without contributing to relaxation or buckling [6]. The growth temperature was 625°C, low enough to avoid any glass flow during the growth. (Relaxation is negligible at temperatures lower than 700°C [7]). This structure was then annealed at 790°C and the time dependence of the surface roughness (RMS) at the center of 200 μm × 200 μm islands was measured (see open triangles in Fig. 5.2). The buckling

growth of the 60-nm SiGe film is clearly much slower than the 30-nm SiGe film, as predicted.

5.2.3 Long annealing times

A third approach to achieve flat relaxed SiGe islands is to anneal buckled islands for very long times. The buckled surface is not a minimum energy state because of the strain energy stored in the buckled surface. The lateral expansion is expected to smoothen surface roughness because it releases this strain energy. Therefore, annealing islands for a long time allows lateral expansion to reach the island center and should subsequently flatten entire islands. Figure 5.4 shows the surface roughness at the center of islands of various sizes after annealing at 790^{o}C and 850^{o}C. The buckling of 60 μm islands after 100 min at 790^{o}C was 6 nm, which decreased to ~1.3 nm after 280 min at 790^{o}C. This reduction in surface roughness can be dramatically improved by higher temperature and lower viscosity: at 850^{o}C the buckling at the center of 60 μm islands is reduced to 0.7 nm after 64 min, and to ~1.3 nm after 195 min on 80 μm islands. Therefore buckling grows for short time scales, when lateral expansion is slow, and then decreases at large time scales, when lateral expansion reaches the island center. Qualitatively, the curves of surface roughness vs. strain (Fig. 5.3) will eventually turn over and come down.

Even though annealing for a long time is supposed to flatten buckled islands of any size, it is found that cracks form on islands larger than 80 μm when the buckling amplitude exceeds a critical value (Fig. 5.5). The largest crack-free, flat, relaxed 30-nm $Si_{0.70}Ge_{0.30}$ island with surface roughness less than 2 nm obtainable by this approach was only 60 μm wide. A more aggressive measure will be discussed in the next section for buckling suppression.

5.3 Suppression of buckling using bi-layer structures

Given that the relative rate of these two simultaneous processes (lateral expansion and buckling), independent of the absolute time scale, determines the surface roughness, the key to improve surface roughness is to increase the ratio of the rate of lateral expansion over that of buckling. This should be achievable by either speeding up lateral

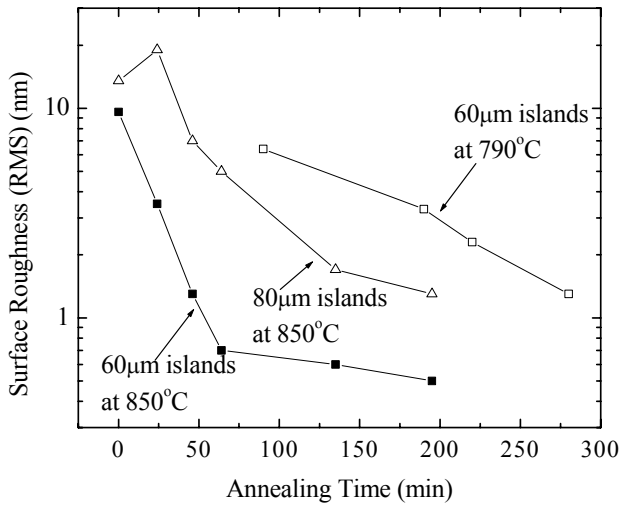


Figure 5.4: Surface roughness at island center of 60 and 80 μm islands as a function of annealing time at 790°C and 850°C for $Si_{0.70}Ge_{0.30}$ thickness of 30 nm on 200-nm BPSG. Samples annealed at 850°C initially have a buckled surface because they first went through an annealing of 35 min at 800°C.

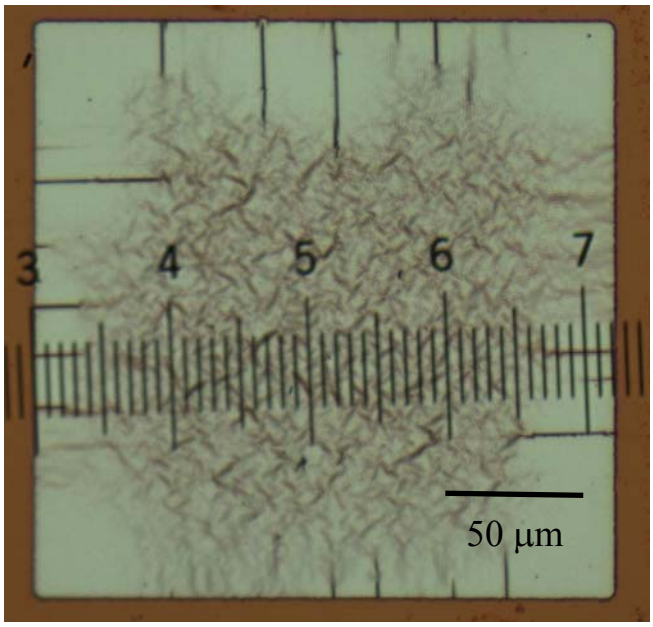


Figure 5.5: Optical micrograph of a 200 μm × 200 μm $Si_{0.7}Ge_{0.3}$ island on 200-nm BPSG after a 5-hr anneal at 800°C in nitrogen. The RMS surface roughness is larger than 15 nm. Many cracks formed during the annealing.

expansion or slowing down buckling. A bi-layer structure, discussed in chapter 4 for faster lateral expansion, should fulfill both requirements, since the increased total thickness is likely to slow down buckling, just as we observed on a thick uniform SiGe film (Sec. 5.2.2).

5.3.1 Suppressed buckling in bi-layer structures

To understand the effect of bi-layer structures on buckling, we need to extend the buckling theory for single-layer on compliant BPSG to bi-layers. In the case where a capping film A is on the SiGe layer, following the derivation in Ref. [1] for layers without caps, one can derive the new equation for the buckling growth rate:

$$\frac{1}{\tau_B} = \frac{1}{2\eta}\left[\frac{\sinh(2h_g k) - 2h_g k}{1+\cosh(2h_g k) + 2(h_g k)^2}\right] * \left[\frac{(E_{SiGe}\varepsilon_{SiGe}h_{SiGe} + E_A\varepsilon_A h_A)k}{1-\nu} - \frac{(E_{SiGe}h_{SiGe}{}^3 + E_A h_A{}^3)}{12(1-\nu^2)}k^3\right] \quad (5.3)$$

E_A and ε_A represent the Young's Modulus and strain of the film A, respectively. Its Poisson's ratio is assumed to be the same as the SiGe film for simplicity, which is a good approximation for Si and SiO_2 used in this study. Note that in the limit of h_A becoming zero, Eqn. (5.3) exactly reduces to Eqn. (5.2). To illustrate the effect of the capping film A on the buckling, the buckling growth rate versus the buckling wavenumber is plotted in Fig. 5.6 based on Eqn. (5.3), using Si as the capping layer. The initial strain in the capping silicon layer is set to be zero because the SiGe film still has the in-plane lattice constant of its original Si substrate. Note that the dominant buckling occurs at the wavelength where the buckling growth rate is highest. The addition of a 30-nm silicon layer can lower the maximum buckling growth rate by a factor of two from 8.2 x 10^{-3} to 3.8 x 10^{-3} s^{-1} (Fig. 5.6). Two physical effects cause the reduction in the buckling growth rate: (i) the bi-layer structure is more mechanically rigid and thus less likely to bend, and (ii) the buckling driving force, the average strain, is now less with a cap than without a cap because the added film is initially strain-free. This predicted buckling suppression by a silicon layer was verified in experiments. Epitaxial Si films of several thicknesses were deposited on fully compressive 30-nm $Si_{0.7}Ge_{0.3}$/200-nm BPSG using RT-CVD at 700°C. The Si/SiGe bi-layers were then annealed and the time dependence of the surface

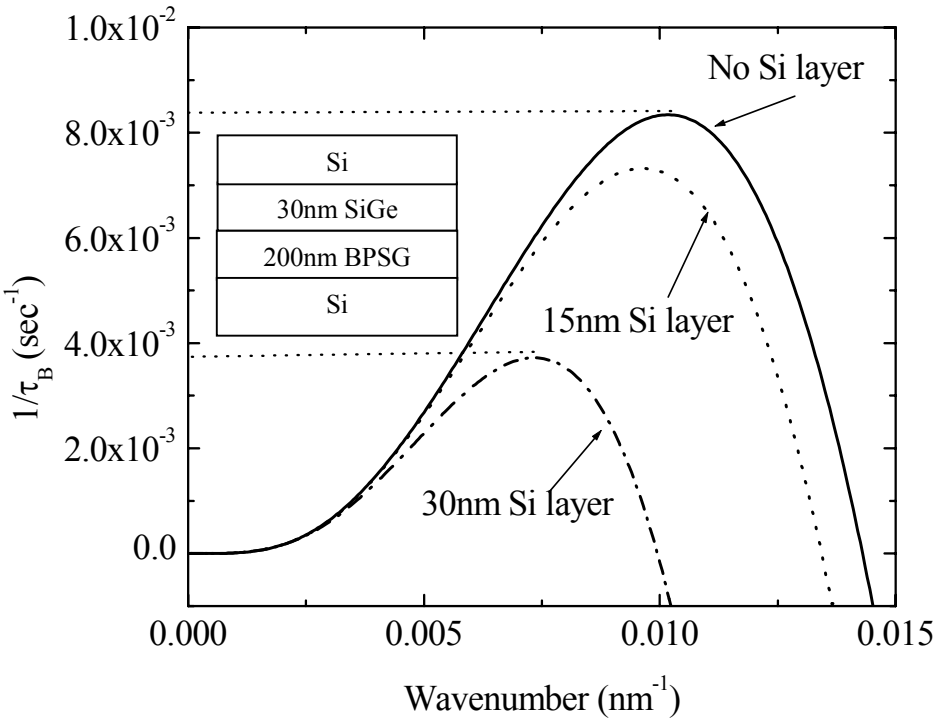


Figure 5.6: Calculated buckling growth rate ($1/\tau_B$) as a function of buckling wavenumber, based on Eqn. (5.3) and parameters in Table 4.1. This calculation assumes an infinite film, where lateral expansion is absent.

roughness at the center of 200 μm x 200 μm islands was measured for different cap thicknesses (Fig. 5.7). Because negligible lateral expansion occurred at the center of 200 μm islands during the anneal, the buckling behavior of the islands is the same as that of infinite films. A 19-nm silicon cap can reduce the RMS buckling amplitude after a 2-hr anneal from 20 nm to less than 2 nm, and with a 31nm cap, the RMS buckling amplitude is decreased to 1 nm.

5.3.2 Large, flat, and fully-relaxed SiGe islands

A capping layer speeds up lateral expansion while the buckling growth rate is suppressed. Therefore, much larger flat islands should be achievable using the bi-layer structures than using a single SiGe film alone. We have explored both silicon and silicon dioxide as capping materials.

5.3.2.a Epitaxial silicon cap layers

The first experiment utilized a 19-nm silicon cap layer selectively deposited by RT-CVD on patterned 30-nm SiGe as mentioned in the previous section. The surface roughness at the center of islands was measured versus annealing time for islands of edge width 100 μm, 200 μm and 500 μm. Fig. 5.8(a) shows that the 100 μm island remained flat (RMS ~1 nm) throughout the entire anneal. This is far larger than the largest flat island of 60 μm achieved using a single 30-nm SiGe film without a cap as shown in Sec. 5.2.3 and Fig. 5.4. The 200-μm island initially buckled to an RMS roughness of ~5 nm after 300 min annealing at 800^{o}C and then flattened out (RMS < 2 nm) when the lateral expansion finally reached the center after long annealing (22 h at 800^{o}C and 6.5 h at 850^{o}C) (Fig. 5.8(b)). The 500-μm island still buckled dramatically (RMS > 10 nm) and many cracks resulted from the local strain in the buckled regions, however (Fig. 5.8(c)). To achieve larger flat islands, a thicker Si cap layer (~31 nm) was then tested. Figure 5.9(a) shows the surface roughness at the center of 200 and 500 μm islands as a function of annealing time. The buckling on the 200-μm island previously observed in Fig. 5.8(a) disappeared and the roughness was less than 2 nm. Although the roughness grew on the 500 μm island, the growth was much slower than that with a 19-nm silicon cap, and in this case, only one crack is seen on the 500-μm island (Fig. 5.9(b)).

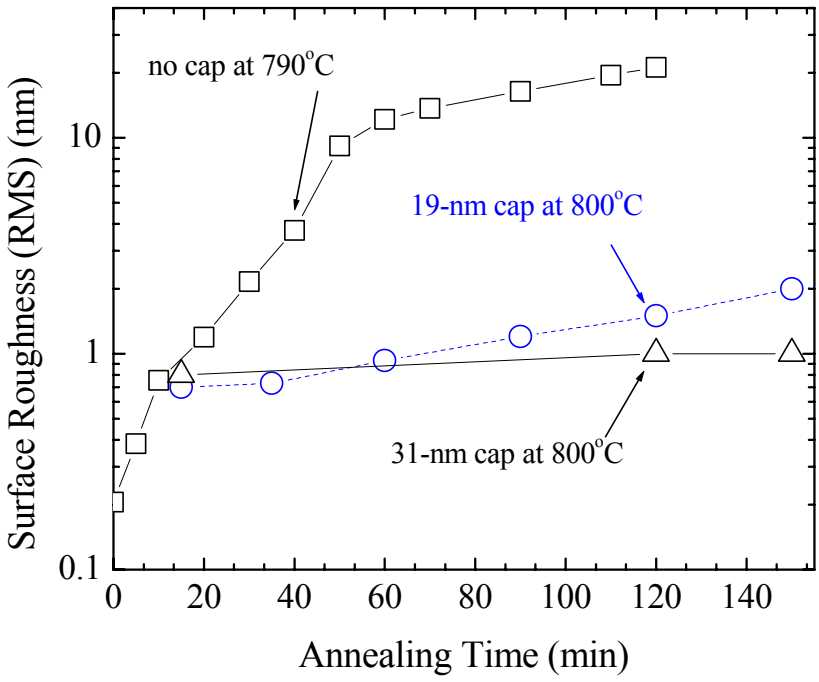
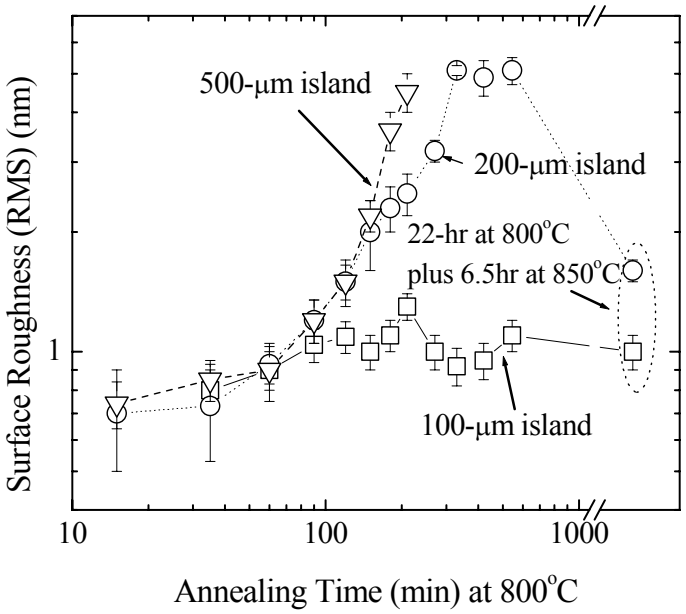


Figure 5.7: Surface roughness vs. annealing time in nitrogen for a bi-layer of 30-nm $Si_{0.70}Ge_{0.30}$ with a silicon cap of thickness 0 nm, 19 nm or 31 nm, measured at the center of 200 μm x 200 μm islands.



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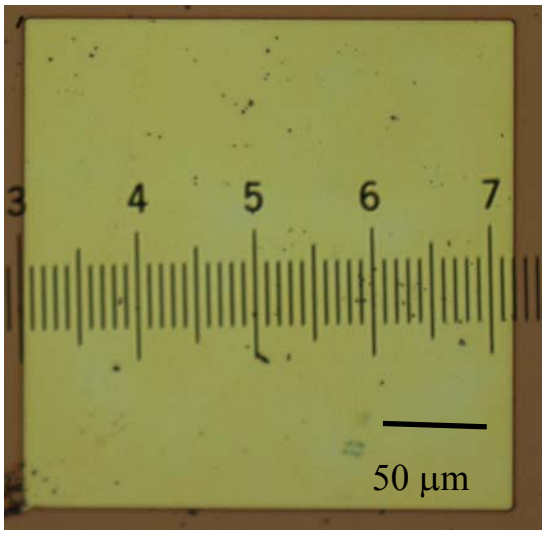

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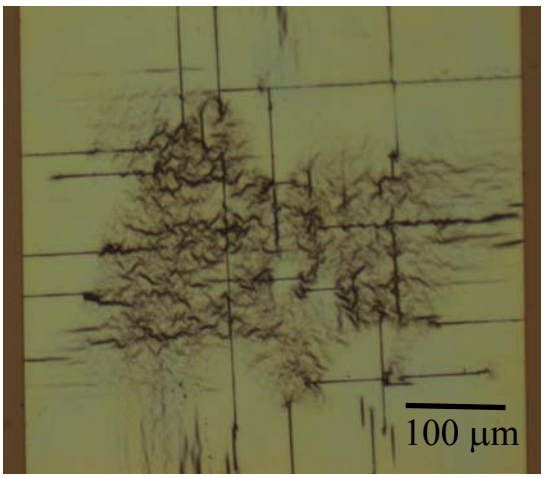
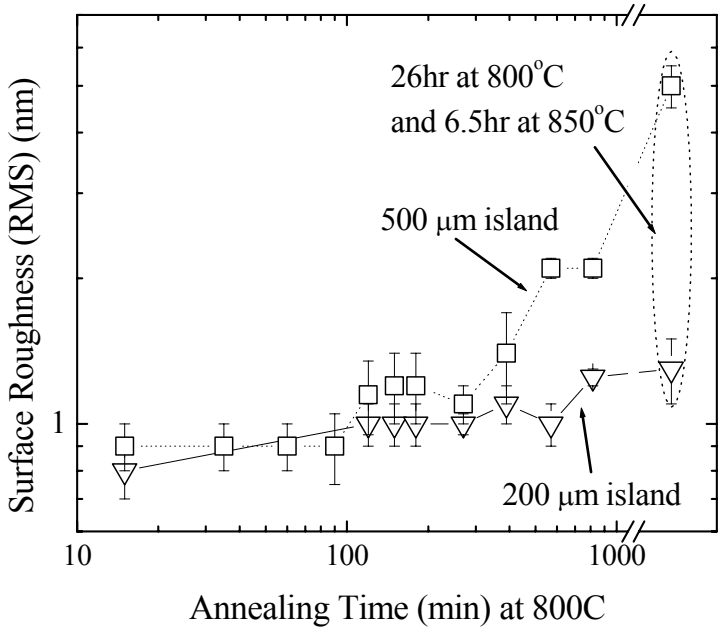
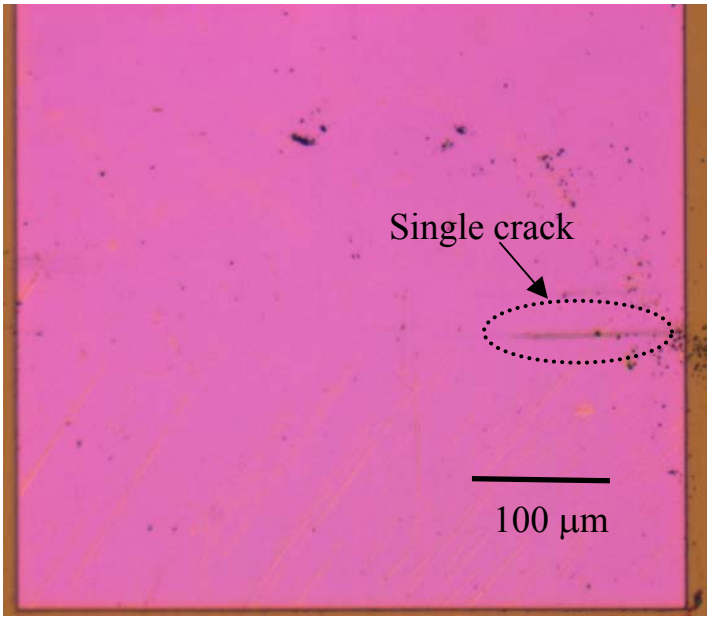


(c)

Figure 5.8: (a) Surface roughness vs. annealing time in nitrogen at 800°C for a 19-nm silicon cap on 30-nm $Si_{0.7}Ge_{0.3}$ on 200-nm BPSG, measured at the center of islands of size 100 μm, 200 μm, and 500 μm. The points after the break on the time axis represent 22-hr annealing at 800°C, followed by another 6.5-hr anneal at 850°C. (b) Optical micrograph of a 200 μm x 200 μm island after annealing. RMS surface roughness at the island center is about 1.6 nm. (c) Optical micrograph of a 500 μm x 500 μm island after annealing. The RMS surface roughness at the island center is larger than 10 nm and cracks have occurred.



(a)



(b)

Figure 5.9: (a) Surface roughness vs. annealing time at 800°C for a 31-nm Si cap on 30-nm $Si_{0.7}Ge_{0.3}$ on 200-nm BPSG, measured at the center of islands of 200 μm and 500 μm in edge width. (b) Optical micrograph of a 500 μm x 500 μm island after a 26-hr anneal at 800°C, followed by a 6.5-hr anneal at 850°C. The RMS surface roughness at the island center is about 5 nm.

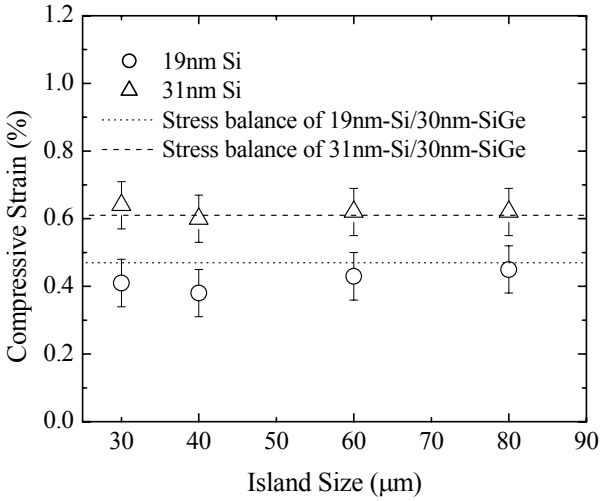


Figure 5.10: Biaxial strain of a 30-nm $Si_{0.70}Ge_{0.30}$/Si bi-layer at center of square islands as a function of the island edge sizes after a 3-hr anneal at 800°C. Open symbols are experimental data. Lines are calculation of final strain based on stress balance. All Si/SiGe islands have reached equilibrium and the silicon cap clearly prevents full relaxation of the strain in SiGe films.

Although the Si cap considerably increases the size of obtainable flat SiGe islands, the SiGe is not fully relaxed upon equilibrium. The final strain in the SiGe film is governed by the stress balance between the Si and SiGe films (Eqn. 4.19). Figure 5.10 shows the final strain in the SiGe films on islands up to 80 μm in edge width upon equilibrium (annealed for 3 hrs at 800°C). Germanium diffusion during this relaxation anneal is negligible as the annealing time needed for small islands to reach stress balance is relatively short. From an initial strain of 1.2%, a final strain 0.43% in the SiGe film with a 19-nm silicon cap is observed, independent of the island size, which agrees well with the prediction of Eqn. (4.19) of 0.47%. Increasing the cap thickness to 31 nm increases the final strain in the SiGe film to 0.61%, which also shows good agreement between the experimental data and the stress balance theory. A thicker silicon cap clearly results in more final strain in the SiGe film from the stress balance condition.

To realize full relaxation in the SiGe film, the silicon layer should be removed after the initial anneal and a further anneal should be performed. In this second anneal, buckling is less likely to be a problem, even without the cap, because the strain in the

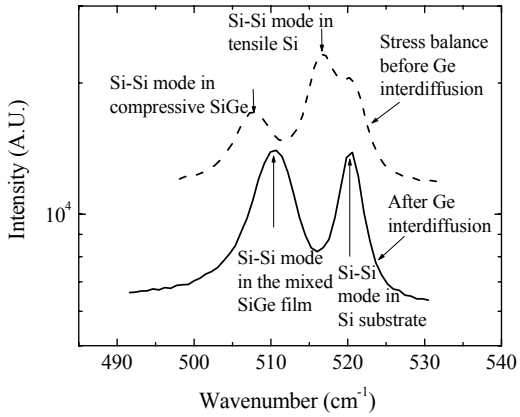


Figure 5.11: Raman spectra measured at the center of a 30 μm x 30 μm island comprising 31-nm Si/30-nm $Si_{0.7}Ge_{0.3}$. The dashed line reflects the stress balance between the Si and $Si_{0.7}Ge_{0.3}$ films after a short anneal (210 min at 800°C). The solid line indicates that the Si and $Si_{0.7}Ge_{0.3}$ films have intermixed after a long anneal (13 hr at 850°C). The peak at 520 cm^{-1} comes from the silicon substrate.

SiGe film is less than that before the first anneal and the buckling time constant depends on the strain in the SiGe film (Eqn. 5.2). The removal of the Si cap is feasible only if little germanium diffusion occurs during the relaxation annealing. Otherwise the Si and SiGe films can intermix and form a single SiGe layer with a lower germanium percentage. Given the long annealing required to reach equilibrium on large islands, considerable germanium diffusion does take place between the Si and SiGe films. This was confirmed by Raman spectroscopy for a 30-nm $Si_{0.7}Ge_{0.3}$ layer with a 31-nm silicon cap. Before long annealing, two distinct Si-Si phonon peaks (516 cm^{-1} for the Si layer and 507 cm^{-1} for the $Si_{0.7}Ge_{0.3}$ layer) were visible (Fig. 5.11). After 13 h annealing at 850°C, a single Si-Si phonon peak was observed at 510.5 cm^{-1}. This corresponds to a relaxed $Si_{0.85}Ge_{0.15}$ layer, which would be expected from mixing 31-nm Si and 30-nm $Si_{0.7}Ge_{0.3}$ films. (The Raman peak at 520 cm^{-1} comes from the silicon substrate and relaxed $Si_{0.7}Ge_{0.3}$ would have a Raman peak at 501 cm^{-1}) This single SiGe film is undesirable because its in-plane lattice constant is not as large as the fully relaxed SiGe film with the original germanium percentage. To avoid germanium diffusion during the relaxation annealing, a different material is needed for the cap layer.

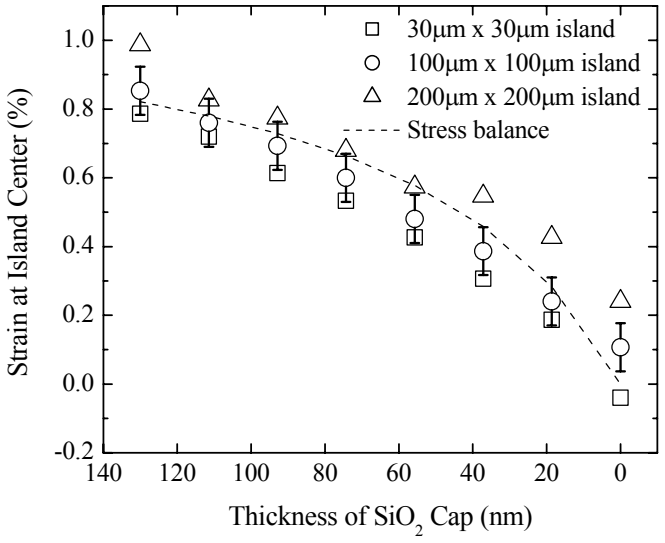
5.3.2.b Silicon dioxide cap layers

1. Experiments

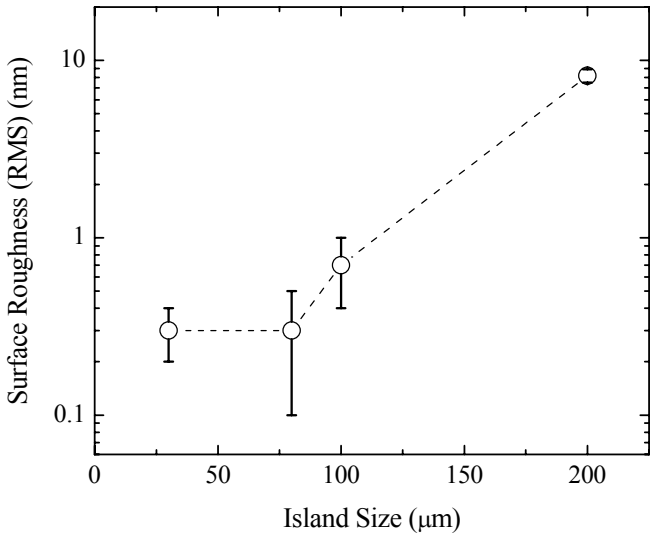
The suppression of buckling depends solely on the mechanical properties of the cap layer. Therefore, in principle, any rigid film that will not crack or flow can be used as the cap to suppress buckling. Since germanium diffusion in silicon dioxide is very slow, silicon dioxide is a good candidate for the cap material. Technologically, it is also easier to deposit SiO_2 than to grow epitaxial films. The conformal SiO_2 deposition also results in SiO_2 between the SiGe islands. Its effect was ignored for all analyses in this Chapter.

A layer of 130-nm SiO_2 was deposited on 30-nm $Si_{0.7}Ge_{0.3}$ by PE-CVD at 250^{o}C to form an alternate bi-layer structure, which was then patterned into islands of edge width from 30 μm to 200 μm. After a 3-hr anneal at 875^{o}C, the $Si_{0.7}Ge_{0.3}$ and SiO_2 films in islands up to 100-μm wide reached stress balance. The compressive strain in the SiGe film, measured by Raman spectroscopy, decreased from 1.2% to 0.8%, which is consistent with the stress balance theory. In addition, all islands remained smooth (RMS < 1 nm) after this anneal.

To further relax the strain, the oxide cap needs to be removed. The residual strain in the SiGe film can still lead to buckling if the oxide cap is removed entirely at once. In the extreme case when all oxide was removed after the initial stress balance, it was found that during the subsequent annealing, the 0.8% strain in the SiGe film caused dramatic buckling on islands as small as 60 μm wide. Therefore, a multi-cycle process was performed, where the cap was thinned and then annealed again to reach stress balance in each cycle. After the initial relaxation process to achieve stress balance, about one-seventh (19 nm) of the SiO_2 cap was removed using dilute hydrofluoric acid (HF). This thinned SiO_2/SiGe sample was annealed again to reach a new stress balance, at which the SiGe film was less compressive and thus less likely to buckle. This etch-and-anneal process was repeated seven times to remove the entire cap and allow the SiGe layer to fully relax without buckling. The strain in the SiGe film measured by Raman spectroscopy at the island center after each cycle is plotted for square islands of edge size 30 μm, 100 μm and 200 μm (Fig. 5.12(a)). Also shown is the calculated strain after each cycle based on the oxide thickness and assuming stress balance was reached after each anneal. The final surface roughness for islands of various sizes after the cap removal and



(a)



(b)

Figure 5.12: (a) Progression of biaxial strain in the $Si_{0.7}Ge_{0.3}$ film after an initial 3-hr anneal at 875°C and seven cap thinning cycles with an anneal at 875°C for 3 hr for each. The open symbols represent the measured strain at the center of islands of 30 μm, 100 μm, and 200 μm in edge width. The dashed line is a prediction by stress balance theory using the oxide thickness of each step. (b) RMS surface roughness of islands as a function of island size after seven cap thinning cycles. Islands up to 100 μm remain flat.

final anneal is shown in Fig. 5.12(b). Islands up to 100 μm in edge width remained flat (RMS ~ 1 nm) and reached full relaxation after the oxide cap was removed completely, whereas the 200-μm island was quite rough (RMS ~ 8 nm) and retained some residual strain. Note that the strain in the 200 μm island is generally above the strain predicted by the stress balance during the thinning process, indicating that stress balance has not been reached in the large islands after annealing. The rough surface on the 200 μm island arose from the last thinning step, where the strain (0.25%) was still large and all of the oxide cap, which suppresses buckling, was removed.

2. Theoretical analysis of multi-step cap-thinning approaches

To potentially reduce the final roughness and reduce the number of etch-and-anneal cycles, we theoretically analyzed the thinning process. Two different thinning strategies were considered: an "equal-step" thinning process and an "unequal-step" thinning process. For both processes, the structure is first annealed to stress balance before the cap is thinned. For the equal-step process, as in the above experiment, the SiO_2 cap is thinned by an equal amount in each cycle, with each thinning followed by an anneal. For the unequal-step process, the oxide cap is thinned by half of its remaining thickness in each cycle (except for the last one when all residual oxide is removed), with each etch step followed by an anneal. For each cycle in the thinning process, one can calculate the maximum buckling growth rate $1/\tau_B$. Note the wavelength at which the largest $1/\tau_B$ occurs will vary as the strain and thickness change (as was seen in Fig. 5.1). The final roughness is assumed to be dominated by the buckling mode with the largest $1/\tau_B$. Therefore, the effectiveness of buckling suppression in these two different thinning processes can be compared, to first order, using the highest buckling growth rate of all cycles. This is shown in Fig. 5.13, as a function of the number of annealing cycles for both equal-step and unequal-step processes. Because the strain relaxed in each etch-and-anneal cycle decreases as the number of annealing cycles increases, a thinning process with more annealing cycles is less prone to buckling. The superior buckling suppression by the unequal-step thinning process over the equal-step thinning process as shown in Fig. 5.13 stems from a better-controlled balance between relieved strain in each cycle and the thickness of the remaining oxide cap. Using the unequal-step thinning process, more

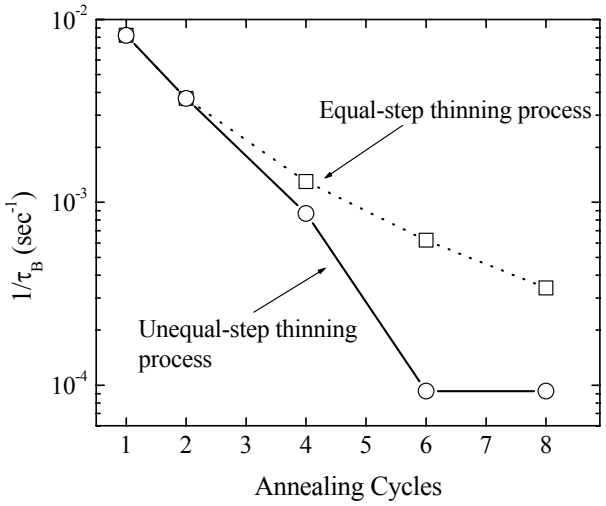


Figure 5.13: The maximum buckling growth rate as a function of the annealing cycles for a 130 nm SiO_2 cap on 30 nm $Si_{0.7}Ge_{0.3}$, calculated from Eqn. (5.3) based on parameters in Table 4.1. The open squares represent the equal-step thinning process, in which same amount of the oxide cap is etched at each step. The open circles represent an unequal-step thinning process, in which the oxide cap is thinned down 50% in each cycle. Note that for the final cycle in either case, the cap is completely removed before annealing, which is equivalent to the no-cap case (Eqn. (5.2)).

strain is relaxed when the oxide cap is thicker. This translates to less strain relaxed when the oxide cap is thin, when the structure is most prone to buckling. However, the highest buckling growth rate in the unequal-step thinning process does not always decrease as more annealing cycles are added. In the unequal-step thinning scheme, only when the highest buckling growth rate occurs at the last cycle can the addition of annealing cycles further decrease the highest buckling growth rate. This explains why the highest buckling growth rate remains unchanged when the number of annealing cycles increases from six to eight, as the highest buckling growth rate for the eight-cycle process takes place in the fourth cycle. To further optimize the thinning process so as to minimize annealing cycles while maintaining a small buckling growth rate, one should consider the competition

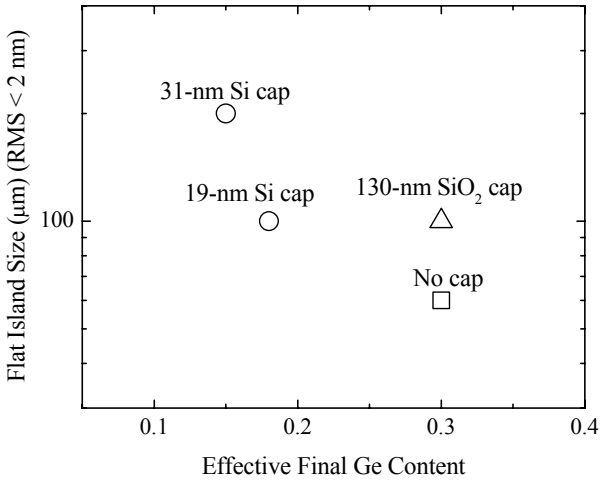


Figure 5.14: Summary of the maximum edge size and effective germanium fraction of flat, crack-free, relaxed, square islands obtained using various cap techniques from an initial 30-nm fully-strained $Si_{0.7}Ge_{0.3}$ film on 200-nm BPSG. Capping layers made of either epitaxial Si or SiO_2 dramatically increase the size of achievable flat islands.

between buckling and lateral expansion at each step and devise a more efficient thinning scheme, which could combine the equal-step, unequal-step, or other thinning processes.

5.4 Summary

Both a high effective germanium percentage and a large size of flat, relaxed SiGe islands are desirable for relaxed-SiGe based applications. By effective germanium percentage, we mean the germanium content of an equivalent fully-relaxed SiGe layer that has the same in-plane lattice constant as the island. With the use of capping layers to suppress buckling and cap removal to allow full relaxation, we have been able to obtain large flat (RMS roughness < 2 nm) islands with 30% germanium. Figure 5.14 summarizes our results obtained through various cap techniques, beginning with a 30-nm $Si_{0.7}Ge_{0.3}$ compressive film on 200-nm BPSG. Without any capping film, the size of largest, flat, relaxed 30-nm $Si_{0.7}Ge_{0.3}$ islands is limited to 60 μm, beyond which islands buckle and crack during relaxation. Using a 31-nm silicon cap, flat islands as large as 200

μm have been made but the effective germanium percentage is lowered (~ 15%) as a result of stress balance between the Si and SiGe layers. The adoption of oxide as the capping material circumvents the germanium diffusion problem and enables cap removal after stress balance, increasing the achievable flat island size (100-μm islands for 130-nm SiO_2) for 30% germanium layers. In the next chapter, we will increase the effective germanium percentage beyond the 30% of the initial film.

The buckling of single-layer (SiGe) and bi-layer (SiGe/Si and SiGe/SiO_2) structures on BPSG has been studied. Although annealing for a long time might flatten buckled SiGe islands eventually in theory, buckling-driven cracks damaged all islands larger than 60 μm. Using bi-layer structures, buckling is substantially suppressed while the rate of lateral expansion is increased. Flat islands as large as 200 μm were obtained using a 31-nm silicon cap. The use of SiO_2 as caps avoided the germanium diffusion problem, which limited the application of silicon caps. Finally, a multi-cycle SiO_2 thinning process enabled fully-relaxed $Si_{0.7}Ge_{0.3}$ islands on BPSG to be achieved.

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Chapter 6

Relaxed SiGe with High Germanium Content on BPSG

Relaxed SiGe with high germanium content is of great interest for many device applications. In this chapter, the background and applications for relaxed SiGe with high germanium content are briefly reviewed (Sec. 6.1). Two novel approaches for achieving relaxed SiGe with high germanium content on BPSG are then investigated. (1) The first method takes advantage of preferential Si consumption in SiGe oxidation, which increases germanium content in the remaining SiGe film (Sec. 6.2). Lateral expansion observed can account for all strain relaxation, suggesting that dislocations are not involved. A super-viscous interfacial layer is observed during SiGe oxidation and is explained by stress-induced viscosity reduction (Sec. 6.3). (2) The second method utilizes stress balance between SiGe films with different germanium contents (Sec. 6.4). Relaxed SiGe with low germanium content (~30%) on BPSG serves as a template on which SiGe with 60% [1] is pseudomorphically grown. High-temperature annealing softens the BPSG and the two layers arrive at stress balance, partially relaxing the top SiGe film and resulting in a coherent layer with an in-plane lattice constant equal to that of a relaxed SiGe layer with a germanium content higher than the original 30%.

6.1 Introduction

Psuedomorphic germanium can be directly deposited on relaxed $Si_{1-x}Ge_x$ with a germanium content of 70% to form a channel for high-performance p-type metal-oxide-semiconductor field-effect transistors (MOSFETs) [2]. Because the lattice constant of germanium is close to that of GaAs (4% larger than that of silicon), relaxed $Si_{1-x}Ge_x$ with a germanium content close to 100% is often used as a buffer layer for integrating III-V semiconductors with silicon substrates [3]. Thus there is a great interest in relaxed SiGe with high germanium fraction. Conventionally, relaxed $Si_{1-x}Ge_x$ with high germanium content has been obtained by growing compositionally-graded $Si_{1-x}Ge_x$ much thicker than critical thickness so as to introduce misfit dislocations to relax strain in the $Si_{1-x}Ge_x$ [4].

Although the density of dislocations in relaxed SiGe by this approach has been greatly reduced over time, the control of threading dislocations is still challenging (with minimum densities ~10^5 cm^{-2}). In addition, such a graded buffer layer approach requires a typical grading rate of less than 10% germanium increment per 1 μm for low defect density. Thus the required thick films (≥ 5 μm) pose a serious bottleneck for throughput [3,4].

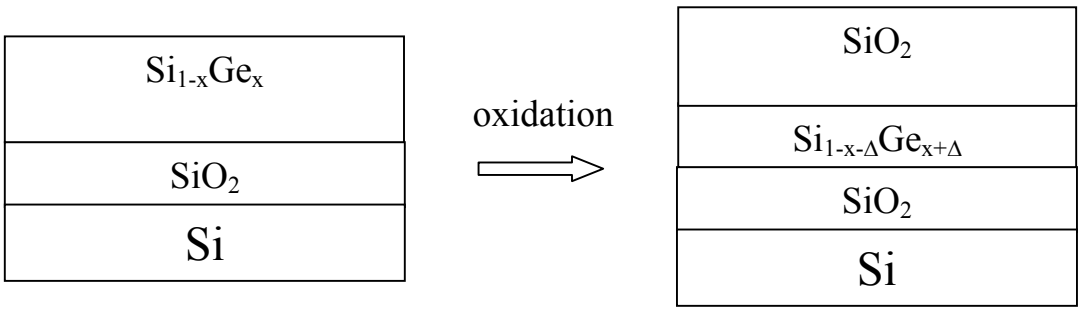
Even though the approach of relaxed SiGe on compliant BPSG is free of the above issues (thick layers and high defect density), the germanium content in the SiGe layer on BPSG is limited for practical reasons. To avoid severe buckling, the SiGe layer needs to be thick (Sec. 5.2.2). However, for a thick SiGe layer, the germanium content needs to be small to satisfy the critical thickness constraint (Fig. 2.2). Therefore, we chose 30-nm $Si_{0.7}Ge_{0.3}$ as the initial layer to make a compromise between the germanium content and the film thickness. In the rest of this chapter, two methods for germanium-content enhancement are presented with a 30-nm $Si_{0.7}Ge_{0.3}$ layer as the starting material.

6.2 Ge content enhancement using SiGe oxidation

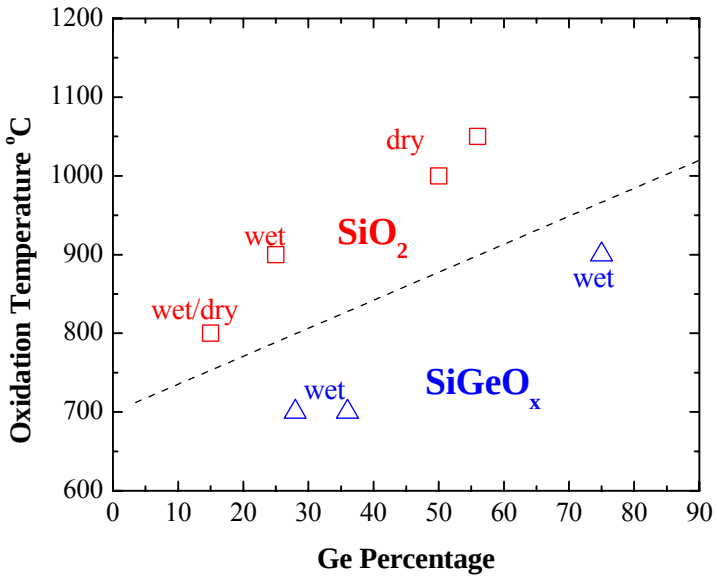
6.2.1 Introduction

A new approach for achieving high germanium content in relaxed $Si_{1-x}Ge_x$ has been reported which takes advantage of the selective removal of silicon atoms from a SiGe film on insulator by $Si_{1-x}Ge_x$ thermal oxidation (Fig. 6.1(a)) [5]. The SiGe-on-insulator (SGOI) structure can be made by separation by implanted oxygen (SIMOX) on SiGe/Si-substrate [6] or germanium diffusion into silicon-on-insulator (SOI) [7]. During oxidation of this structure, when the supply of silicon atoms by diffusion from the SiGe to the oxidation interface can meet the consumption of silicon atoms during oxidation, only the silicon atoms are oxidized because silicon oxidation is preferred to germanium oxidation [8] (Fig. 6.1(b)). This leads to increased germanium content in the $Si_{1-x}Ge_x$ layer as the film is thinned down. However, film quality degrades considerably as the added strain, arising from the germanium content enhancement, is relaxed by dislocation formation during the oxidation and subsequent annealing [5].

We tested the use of SiGe oxidation on SiGe layers on insulating BPSG to obtain high-quality relaxed SiGe on oxide with high germanium content. The compliant BPSG,



(a)



(b)

Figure 6.1: (a) Schematic for enhancement of germanium content by SiGe oxidation: oxidation of SiGe produces pure thermal SiO_2, and the germanium content in the remaining SiGe film increases as a result of conservation of germanium atoms. (b) Oxidation conditions for formation of SiO_2 and $SiGeO_x$ [8].

replacing the thermal silicon dioxide in SGOI, should serve as an excellent substrate to relax the strain introduced by germanium enhancement in the oxidation. Pre-deposited oxide caps are shown to be critical to achieving high quality in the final layer.

We studied two types of samples, type A and type B. Type A consisted of fully-strained 30-nm $Si_{0.7}Ge_{0.3}$ islands on BPSG and type B was fully relaxed 55-nm $Si_{0.84}Ge_{0.16}$ islands on BPSG, formed through germanium diffusion between 30-nm $Si_{0.7}Ge_{0.3}$/25-nmSi islands by annealing at 850°C for 16 hrs. The island size varied from 10 μm to 500 μm. The strain and germanium content in SiGe and Si films were locally measured by micro-Raman spectroscopy. The Si-Si phonon frequency $\omega_{Si\text{-}Si}$ and Si-Ge phonon frequency $\omega_{Si\text{-}Ge}$ were employed to extract germanium content x and biaxial strain ε_{SiGe} as follows [9]:

$$\omega_{Si\text{-}Si}(cm^{-1}) = 520 - 68x - 815\varepsilon_{SiGe}, \quad (6.1)$$

$$\omega_{Si\text{-}Ge}(cm^{-1}) = 400.5 + 14.2x - 575\varepsilon_{SiGe}. \quad (6.2)$$

Note that Eqn. 6.1 reduces to Eqn. 3.6 for 30% germanium content. The surface roughness of SiGe films was measured by atomic force microscopy (AFM).

6.2.2 Direct oxidation

We first examined the direct oxidation of type A and B samples. 20-μm type-A square islands (30-nm $Si_{0.7}Ge_{0.3}$ on BPSG) were annealed at 800°C in forming gas for 30 min to reach full relaxation, which was confirmed by micro-Raman measurements. Subsequently, dry oxidation was carried out at 850°C on the relaxed islands. In this condition, we expected pure silicon dioxide to be formed on top [10]. The germanium content of the type-A sample as a function of oxidation time is shown in Fig. 6.2. After a 2-hr dry oxidation at 850°C, the germanium content increased on average to 50% from 30%. The germanium content in a 200-μm type-B island (55-nm $Si_{0.84}Ge_{0.16}$ on BPSG) increased from 16% to 36% after a 4-hr dry oxidation at 850°C. This confirmed the expected increase in the germanium content.

The surface quality of the SiGe islands after this direct oxidation was not good (Fig. 6.3(a)). The 200-μm type-B island after oxidation has RMS surface roughness of more than 4 nm. In addition, the variation of germanium content across the island is more than

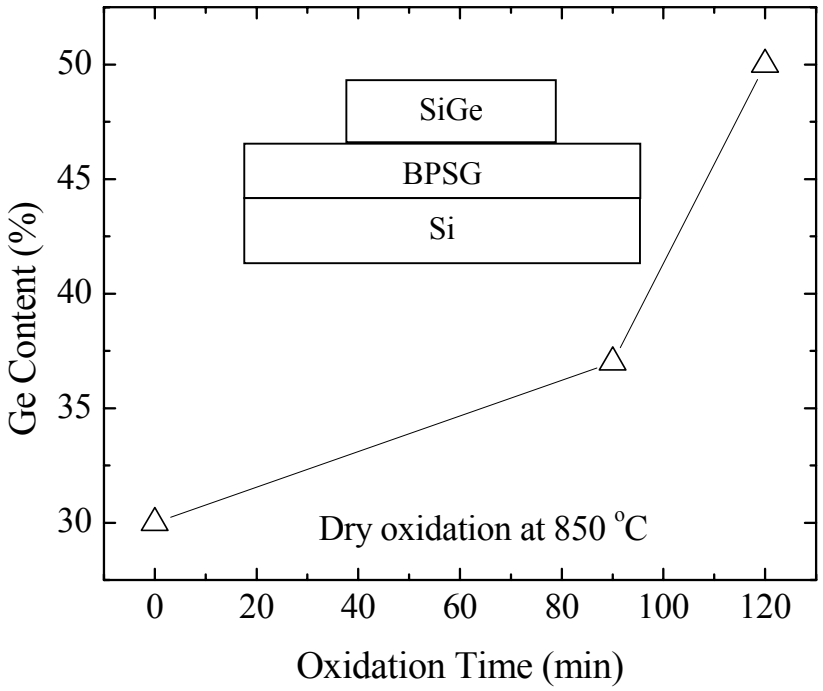


Figure 6.2: Germanium content as a function of dry oxidation time at 850°C, performed on 30-nm $Si_{0.70}Ge_{0.30}$ square islands of width 20 μm on 200 nm BPSG. The islands are nearly strain-free.

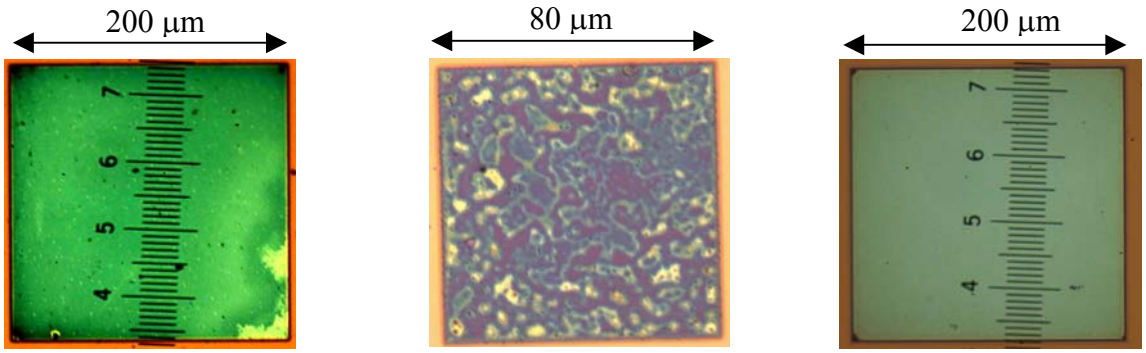


Figure 6.3: Optical micrographs of 55-nm $Si_{0.84}Ge_{0.16}$ islands on BPSG after dry oxidation: (a) A 200 μm x 200 μm island after 4-hr dry oxidation at 850°C. The germanium content reached 36% and the surface roughness was larger than 4 nm. (b) An 80 μm x 80 μm island after 3 hr dry oxidation at 850°C, SiO_2 etch by HF, and another 2-hr dry oxidation at 850°C. The germanium content was around 65% and the surface roughness was larger than 15 nm. (c) A 200 μm x 200 μm island, capped by 70-nm PECVD-SiO_2, after dry oxidation at 850°C for 3.5 hr and at 900°C for 2.5 hr and annealing in nitrogen at 875°C for 5.5 hr. The germanium content and strain were 57% and –0.27%, respectively. The surface roughness (RMS) was less than 2 nm.

10%. Figure 6.3(b) shows an 80-μm type-B island after a 3-hr dry oxidation at 850°C, oxide removal by hydrofluoric (HF) wet etch, and another 2-hr dry oxidation at 850°C. The final germanium content was ~65%, but varied from 50% to 80% across the island and the surface roughness was larger than 15 nm. The surface of 20-μm type-A islands was also poor with a RMS surface roughness higher than 4 nm after 3-hr dry oxidation at 850°C. The rough surface and non-uniform germanium content on islands after oxidation probably originates from the strain-induced surface roughening on compliant BPSG (similar to buckling observed during strain relaxation of SiGe islands on BPSG) and/or a non-uniformity of the oxidation rate. It has been observed that oxidation rate depends on stress [11], and surface roughening can cause variation of stress across SiGe islands on BPSG [12]. Furthermore, it is expected that oxidation rate also depends on the local germanium content.

6.2.3 Oxidation through pre-deposited oxide caps

To improve uniformity of the oxidation rate across islands, a 70-nm SiO_2 capping layer was deposited on type-B samples before oxidation using plasma enhanced chemical vapor deposition (PE-CVD) at 250°C. For such a thick silicon dioxide cap, the oxidation rate is mainly controlled by the oxygen diffusion time through the silicon dioxide cap, which is determined by the thickness of the SiO_2 cap. Thus the oxidation rate will have a weak dependence on the surface reaction rate which depends on strain and surface condition of the remaining SiGe layer. In our earlier work (Sec. 5.3.3), silicon dioxide caps have been successfully used to suppress buckling of SiGe islands on BPSG. The underlying mechanism is an increased film rigidity with a silicon dioxide cap, which makes strain relaxation by buckling less likely. Therefore, besides controlling the oxidation rate, the silicon dioxide caps have a second benefit: a smoother SiGe surface, which in turn leads to less strain variation across islands, reducing strain-induced oxidation variation across islands.

The SiO_2-capped type-B sample was oxidized in dry oxygen for 3.5 hrs at 850°C and then 2.5 hrs at 900°C (Fig. 6.3(c)). The longer time and higher temperature were required because the presence of the cap lowered the oxidation rate. The sample was then annealed in nitrogen for 5.5 hrs at 875°C to further relax strain. The improvement in film

quality was dramatic. The surface roughness was less than 2 nm (Fig. 6.3(c)). The germanium content increased to 57% and was uniform (+/- 3%) across the island. The strain in SiGe was -0.27% and therefore, its in-plane lattice constant was the same as fully relaxed SiGe with germanium content of 52%. Surprisingly, the layer was nearly fully relaxed despite the thick SiO_2 cap which should inhibit relaxation by stress balance (Sec. 4.3). The decoupling of the SiO_2 cap from the underlying SiGe layer is fortuitous, and we think it is caused by the creation of an ultra-low viscosity slippage layer during oxidation between the SiO_2 and SiGe layers. This will be discussed in the next section.

6.2.4 Direct measurement of island expansion to confirm relaxation mechanism

The compressive strain in SiGe islands, caused by Ge-enhancement during oxidation, could relax by plastic relaxation of the lattice or by simple lateral expansion of the islands, a process that does not need defects. If the compressive strain relaxes by islands expanding laterally on the BPSG, the island size would increase. If the mechanism is plastic relaxation, there is no macroscopic change in the islands and no lateral expansion would be expected. Without a heteroepitaxial interface, the plastic relaxation is essentially removal of vertical planes of atoms by emission of interstitials – analogous to growth of misfit dislocations in a hetero-epitaxial interface. The removal of lattice planes to reduce the strain would not lead to an increase in island size. To determine the relaxation mechanism, the lateral expansion of the islands was measured by AFM. The gap between adjacent 100 μm islands was chosen to be ~2 μm, comparable with the magnitude of island expansion. The small amount of island expansion could be inferred from shrinkage of the island gaps more accurately than the direct measurement of island size (Fig. 6.4). 100 μm type-B islands were dry oxidized at 870^{o}C for 80 min, followed by an anneal in nitrogen at 850^{o}C for 2 hrs to facilitate strain relaxation. The final compressive strain and Ge content, measured by Raman spectroscopy, were 0.07% (+/- 0.06%) and 27% (+/- 0.8%), respectively. This is equivalent to fully relaxed SiGe with germanium content of 25% (+/- 1.5%). The lateral expansion to relax the strain would require an island expansion of 390 nm (+/- 60nm). After subtracting the thickness of the oxide grown on island sidewalls, the observed island expansion was 345 nm (+/-

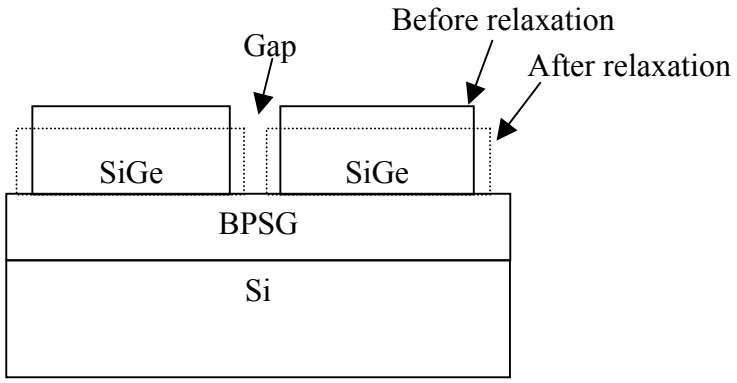


Figure 6.4: Schematic illustration of lateral expansion measurement of SiGe islands after strain relaxation.

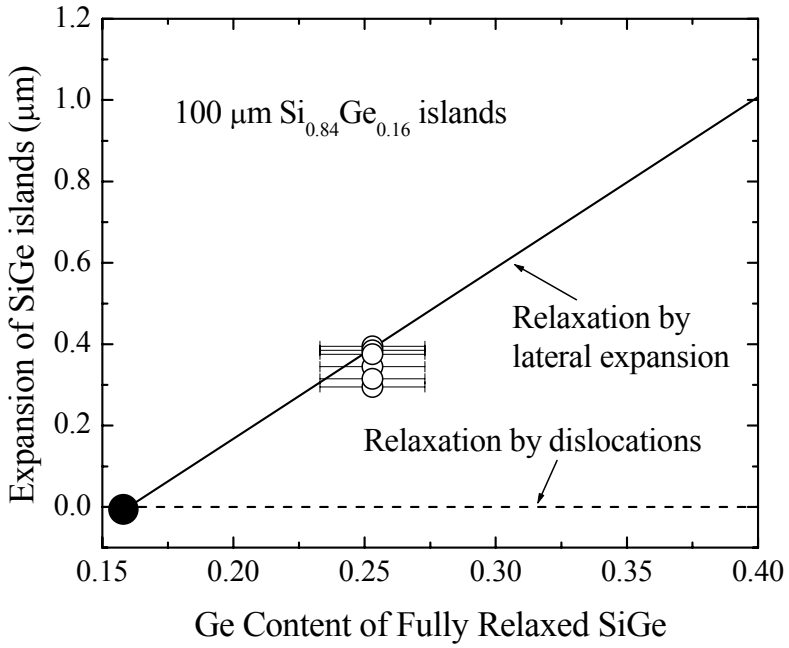


Figure 6.5: Lateral expansion of SiGe islands as a function of germanium content for 100 μm x 100 μm islands with initial fully relaxed $Si_{0.84}Ge_{0.16}$. The solid line is a prediction assuming that all strain caused by germanium enhancement is relaxed by lateral expansion, and the horizontal dashed line assumes all strain relaxation is through removal of vertical lattice planes by interstitial emission. The open symbols are experimental data, measured on islands after dry oxidation at 870°C for 80 min and annealing at 850°C in nitrogen for 2 hr.

50 nm) (averaged over four locations), which was near that expected for relaxation by lateral expansion (Fig. 6.5). This shows that defects (e.g. plastic relaxation) do not play a dominant role in the strain relaxation process.

6.3 Super-viscous interfacial layer between SiO_2 and SiGe

6.3.1 Experimental observations

When no oxidation is involved, the coherent interface between SiO_2 and SiGe films (Fig. 4.11) on BPSG has been maintained during strain relaxation (i.e. an identical strain change in the SiO_2 and SiGe films) and the final strain is governed by stress balance. However, in the case of oxidation of SiGe covered by a PECVD-SiO_2 cap (Fig. 6.6), the data of the previous section showed that the SiGe island under oxidation relaxed more than expected by stress balance with its oxide cap. To investigate this lack of coherence between the SiGe and SiO_2 during oxidation, islands of various sizes, made of 70-nm PECVD-SiO_2 on 30-nm fully strained $Si_{0.7}Ge_{0.3}$ on 200-nm BPSG, were annealed and then dry oxidized. After annealing at 850^{o}C for 2 hrs and at 875^{o}C for 2 hrs in nitrogen, the strain in the $Si_{0.7}Ge_{0.3}$ layer on islands up to 80 μm in edge width changed from –1.2% to –0.65%, in line with calculation based on stress balance and coherence interface between the PECVD-SiO_2 and $Si_{0.7}Ge_{0.3}$ layers. Dry oxidation at 900^{o}C for 2 hrs was subsequently carried out on these islands, followed by an anneal at 875^{o}C for 2 hrs to ensure that strain in the islands reaches equilibrium. The strain and germanium content of the final SiGe layer, measured by Raman spectroscopy, are plotted in Fig. 6.7. Also shown are predictions assuming coherent interface and stress balance between the top PECVD-SiO_2 and bottom SiGe layers, with the newly formed thin thermal SiO_2 ignored. Note that even though large stress is generated in newly formed thermal oxide, the stress is rapidly relaxed during the subsequent high-temperature process (an 875^{o}C anneal in our case) during which the viscous flow of the silica is activated [13]. Therefore, oxidation-induced stress can be ignored in the final stress balance. It can be estimated from Ref. [14] that the residual compressive stress in the newly formed thermal oxide after an anneal at 875^{o}C for 2 hrs is less than 5×10^8 Nm^{-2}, whose contribution to the strain in the SiGe layer upon stress balance is comparable to the strain measurement inaccuracy.

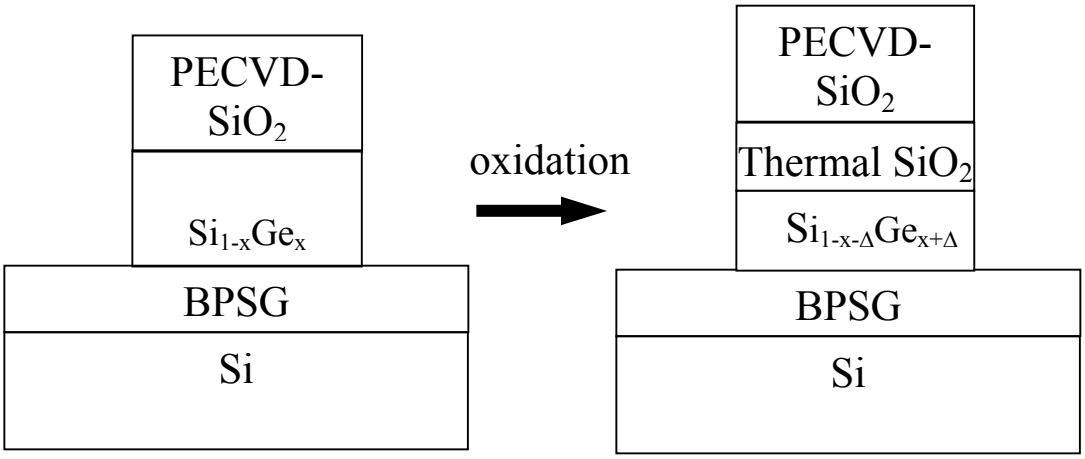


Figure 6.6: Schematic diagram for the oxidation of SiGe covered by PECVD-SiO_2. A thermal SiO_2 layer is formed between PECVD-SiO_2 and SiGe layers during oxidation and the germanium content in the remaining SiGe layer is enhanced.

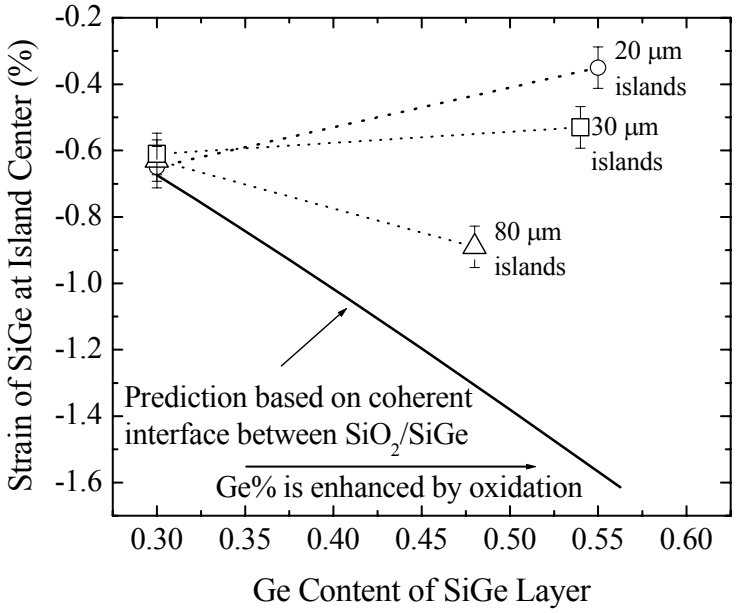
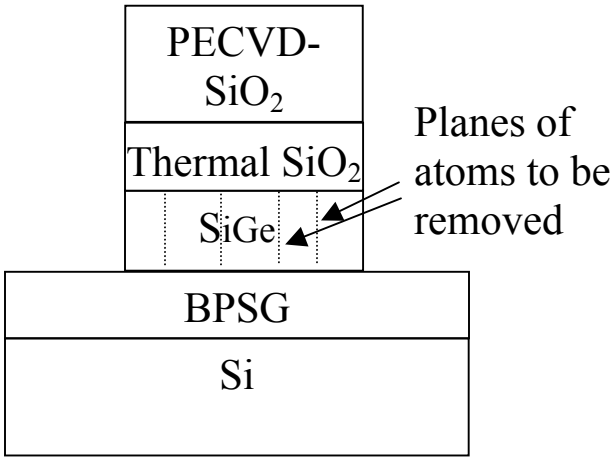


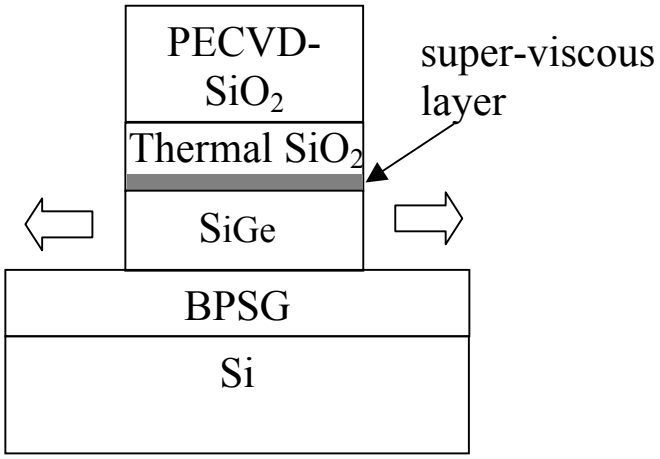
Figure 6.7: Strain and germanium content at the center of SiGe islands for different sizes (20, 30 and 80 μm) before and after oxidation. The starting material was composed of 70-nm PECVD-SiO_2 on 30-nm $Si_{0.7}Ge_{0.3}$ and was annealed in nitrogen for 2 hrs at 850 and 875°C before oxidation. It was then dry oxidized at 900°C for 2 hrs, followed by annealing at 875°C for 2 hrs. The open symbols are experimental data. The solid line is a prediction assuming a stress balance between the PECVD-SiO_2 and the remaining SiGe films.

Stress balance predicts that the strain built up from germanium enhancement during oxidation is nearly fully retained, since any relaxation of strain requires stretching the top PECVD-SiO_2, which is relatively more difficult as the bottom SiGe layer becomes thinner during oxidation. The observed strain in the SiGe layer, however, does not agree with the stress balance prediction and is much less, with strain varying from –0.9% on 80 μm islands to –0.35% on 20 μm islands. In theory, this lack of coherency could also be caused by the strain in the SiGe being relaxed by the removal of vertical lattice planes (Fig 6.8(a)), as described in the previous section. However, this would not lead to the island getting wider, as was observed in the previous section. Thus possible reasons are (a) a super-viscous layer in the newly formed silicon dioxide which decouples the cap from the underlying SiGe (Fig. 6.8(b)) or (b) poor bonding between the SiGe and SiO_2 layers (due to weak SiO_2-Ge bonds). In the former case, top PECVD-SiO_2 layer is decoupled from the bottom SiGe layer by a super-viscous layer during oxidation, which allows the strain in the SiGe layer to laterally expand to relax beyond the point set by the stress balance (Fig. 6.8(b)). The lateral expansion assumed in this case can easily explain the observed trend of lower strain on smaller islands. In the latter case, the strain relaxation relies on the weak SiGe/SiO_2 interface, which can be easily tested by switching to a Si/SiO_2 interface.

To investigate the possible role of poor bonding of the SiGe/SiO_2 interface, a 30 x 30 μm^2 island, made of 79-nm Si on 30-nm $Si_{0.7}Ge_{0.3}$ on 200-nm BPSG, was first annealed at 800^oC in nitrogen to reach stress balance and then wet oxidized at 850^oC (Fig. 6.9). During oxidation, a Si/SiO_2 interface is formed instead of a SiO_2/SiGe interface. The evolution of strain in the Si and SiGe layers as a function of Si layer thickness during the oxidation is plotted in Fig. 6.10. The solid lines in Fig. 6.10 represent the prediction of stress balance between the $Si_{0.7}Ge_{0.3}$, remaining Si, and top thermal SiO_2 layers. The strain in Si and SiGe layers clearly changed almost identically as the strain in SiGe layer was relaxing and the strain in Si layer turned more tensile during oxidation, showing that the Si and SiGe remain coherent as expected. Most significantly, the measured final strain is in fair agreement with the expected stress balance solely between the Si and SiGe layers without any effect of the SiO_2. The top thermal silicon dioxide, formed during the oxidation, was not stretched as the underlying Si and SiGe layers expanded, in



(a)



(b)

Figure 6.8: Illustration of possible mechanisms for violation of stress balance: (a) The strain in the SiGe film relaxes by removal of vertical planes of atoms in the SiGe by emission of interstitials, similar to growth of misfit dislocations across a pseudomorphic interface when there is a crystalline substrate. (b) A super-viscous layer allows strain relaxation of the SiGe film without stretching the top oxide films. Both mechanisms allow a decoupling of strain in the SiGe and PECVD-SiO_2.

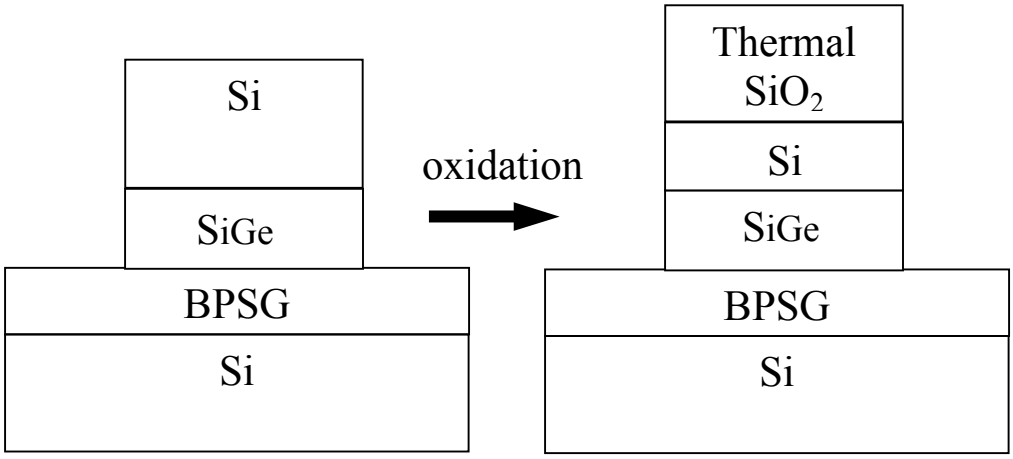


Figure 6.9: Test design to examine whether poor bonding of the SiGe/SiO_2 interface is responsible for the loss of coherency between the SiGe and the thermal SiO_2. In the case of oxidation of the top silicon layer, a poor SiO_2/SiGe interface could not be responsible for the loss of coherency between the Si and SiO_2 layers.

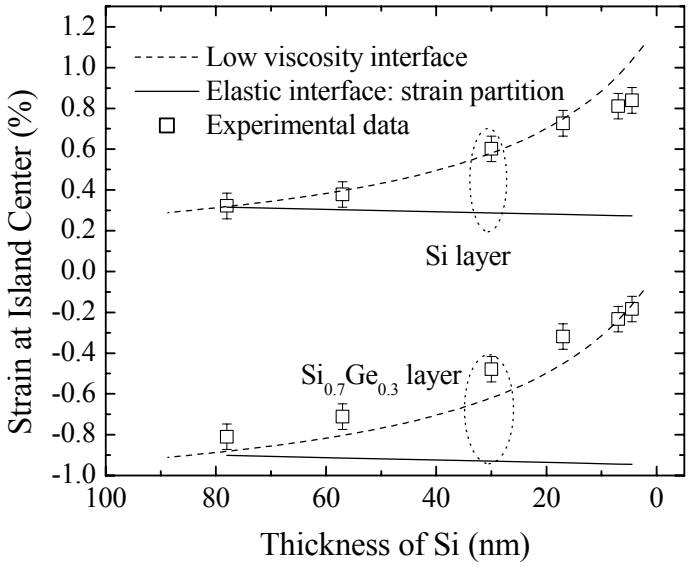


Figure 6.10: Strain of Si and SiGe in a 30-μm island during oxidation. The starting material was composed of 79-nm epitaxial Si on fully-strained 30-nm $Si_{0.7}Ge_{0.3}$ and was annealed in nitrogen at 800°C to reach stress balance. It was then oxidized at 850°C in wet ambient. The open symbols are experimental data. The solid line represents prediction of stress balance between thermal-SiO_2/Si/SiGe and the dashed line is calculated based on stress balance of Si/SiGe. In both models, coherency between the Si and SiGe is assumed.

line with the presence of a super-viscous layer. In this case, the lack of coherency between the Si/SiGe and the SiO_2 cannot be blamed on a weak SiGe/SiO_2 interface. Therefore, we propose that this lack of coherency is due to a super-viscous layer in the SiO_2 itself in both the Si/SiO_2 and SiGe/SiO_2 cases during oxidation.

6.3.2. Super-viscous SiO_2 films under high stress

We attributed the super-viscous layer to the well-known, stress-induced viscosity reduction during silicon oxidation, with viscosity η in stressed thermal oxide [15]:

$$\eta = \eta_0 \frac{\sigma_s / \sigma_c}{\sinh(\sigma_s / \sigma_c)}, \tag{6.3}$$

where η_0 is low stress viscosity, σ_c is a threshold stress, and σ_s is the shear stress in the oxide. The high stress results from the volume expansion during silicon oxidation. The threshold stress σ_c at which the viscosity starts to decline nearly exponentially has a weak dependence on temperature and is usually on the order of 10^8 N/m^2 for temperatures ranging from 800^{o}C to 1000^{o}C [13]. The dependence of viscosity on stress σ_s for dry oxidation at 850^{o}C is plotted in Fig. 6.11 (σ_c = 4.3 x 10^7 N/m^2 and η_0 = 8 x 10^{21} Poise from Ref. [13]). It has been demonstrated in chapter 3 that the time scale for layer decoupling using a viscous layer is proportional to

$$\tau_L \propto \frac{\eta_{viscous\_film}}{h_{viscous\_film}}, \tag{6.4}$$

where $h_{viscous\_film}$ and η_{viscou_film} denote the thickness and viscosity of the viscous layer, respectively. A time scale of tens of minutes was observed for η_{viscou_film} = 1.1 x 10^{11} Poise and $h_{viscous\_film}$ = 200 nm in Chapter 4. For the thermal silicon dioxide to be as efficient in layer decoupling, its viscosity thus has to be smaller than 10^{11} Poise since thickness of viscous thermal silicon dioxide is usually less than 200 nm. To reduce the viscosity to 10^{11} poise or smaller, the stress in oxide should be higher than 10^9 N/m^2, according to the dependence of viscosity on stress in Fig. 6.11.

As Si is converted into SiO_2 during oxidation, a 120% molar volume expansion occurs and creates huge compressive stress, which leads to significant viscosity reduction. Figure 6.12 shows average stress of thermal SiO_2 formed during dry oxidation

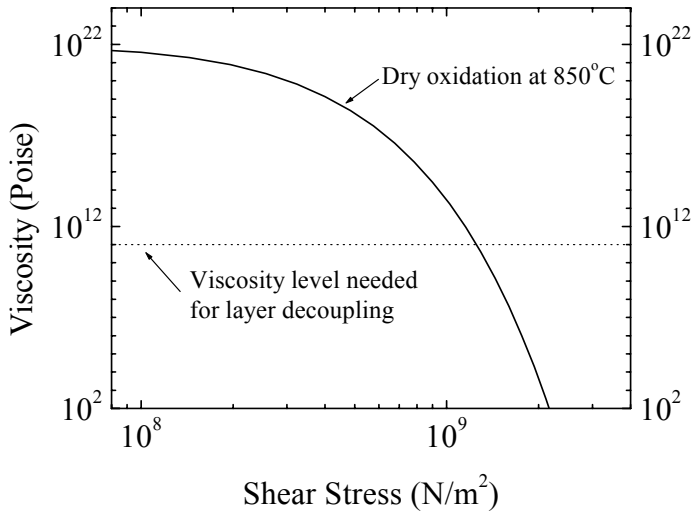
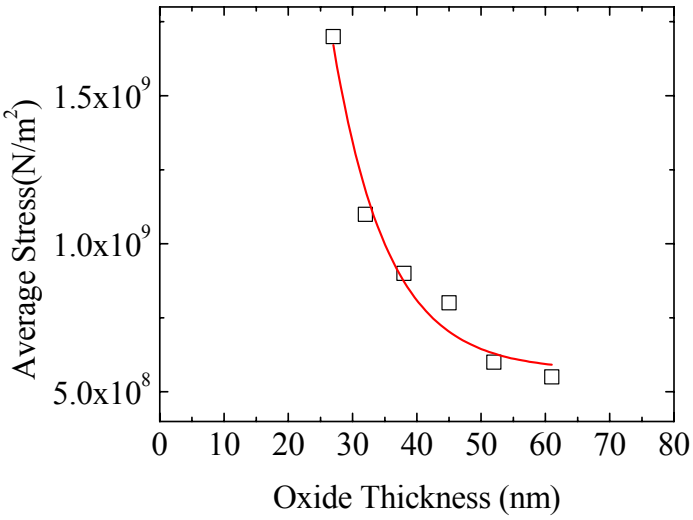


Figure 6.11: Stress dependence of viscosity during dry oxidation at 850°C [13].



at 850°C [14]. The high stress in thin thermal SiO_2, along with the trend of exponential increase in stress for decreasing SiO_2 thickness, indicates that the stress in the freshly formed oxide is huge (>1.5 x 10^9 N/m^2). Therefore, the viscosity in the fresh SiO_2 at the Si/SiO_2 oxidation interface is considerably reduced, much lower than the 10^{11} Poise we just determined as necessary for layer decoupling. The rapid decrease of stress as SiO_2 grows thicker, observed in Fig. 6.12, arises from stress relaxation by viscous flow in SiO_2 [16] and justifies the omission of stress in the thermal SiO_2 layer in consideration of stress balance.

To account for varying viscosity in the thermal SiO_2 layer, the time scale for layer decoupling can be calculated by treating the layer as a stack made of infinite layers, each of which has a single viscosity value. Following the derivation in Sec. 4.1, we arrive at the layer-decoupling time scale:

$$\tau_L \propto \frac{1}{\int_{SiO_2} \frac{dx}{\eta_{SiO_2}(x)}}. \qquad (6.5)$$

Due to the exponential nature for both the dependence of viscosity on stress and the dependence of stress in SiO_2 on the distance from the interface, the decoupling efficiency in fresh thermal SiO_2 can be estimated by only considering the thin thermal SiO_2 layer close to the oxidation interface. As seen in Fig. 6.12, 27-nm SiO_2 has an average stress of 1.7 x 10^9 Nm^{-2} , corresponding to a viscosity of 4.3 x 10^6 poise from Fig. 6.11. After plugging all these values in Eqn. 6.4, it is found that the fresh thermal SiO_2 is more than three orders of magnitude efficient in decoupling than the 200-nm BPSG annealed at 800°C. This validates the existence of a super-viscous layer in oxidation. Thus we conclude that the fortuitous decoupling of the oxide cap and underlying SiGe we observed during SiGe oxidation is due to a low-viscosity layer inherent in the thermal SiO_2 layers, and not poor bonding at the $SiGe/SiO_2$ interfaces.

6.4 High germanium content using stress balance of SiGe films

In this section, we attempt to increase the effective germanium content of relaxed SiGe layers on BPSG not by oxidation, but by adding layers with a higher germanium content on top of them. Stress balance of Si and $Si_{0.70}Ge_{0.30}$ on BPSG has been discussed

in Chapter 4, in which the Si layer impedes the lateral expansion of the compressively strained $Si_{0.70}Ge_{0.30}$ layer. The lattice constant of relaxed Si is smaller than that of $Si_{0.70}Ge_{0.30}$, resulting in a smaller effective germanium content. When adding a SiGe layer with germanium content greater than 30% on top of the original $Si_{0.70}Ge_{0.30}$ layer to form a bi-layer, a larger in-plane lattice constant, equivalent to higher effective germanium content in relaxed SiGe, can be obtained as the top SiGe stretches the $Si_{0.70}Ge_{0.30}$ to reach stress balance (Fig. 6.13(a)).

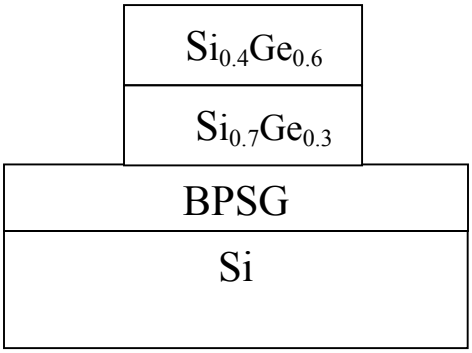
In the first experiment, a 30-nm $Si_{0.4}Ge_{0.6}$ film was selectively grown on relaxed 30-nm $Si_{0.70}Ge_{0.30}$ islands on BPSG using RT-CVD at around 500^{o}C. Raman spectroscopy was also used to measure strain in the $Si_{0.4}Ge_{0.6}$ film. Because the Si-Si phonon peak in Ge-rich films is typically weak, the position of the Si-Ge phonon peak is used for measuring strain in the $Si_{0.4}Ge_{0.6}$ films. The biaxial strain $\varepsilon_{Ge=60\%}$ in the $Si_{0.4}Ge_{0.6}$ layer was inferred from the optical Si-Ge phonon frequencies $\omega_{Si\text{-}Ge}$ as follows:

$$\omega_{Si\text{-}Ge}(Si_{0.4}Ge_{0.6}) = 405\ cm^{-1} - 660\varepsilon_{Ge=60\%}\ cm^{-1}\ [17,18]. \qquad (6.6)$$

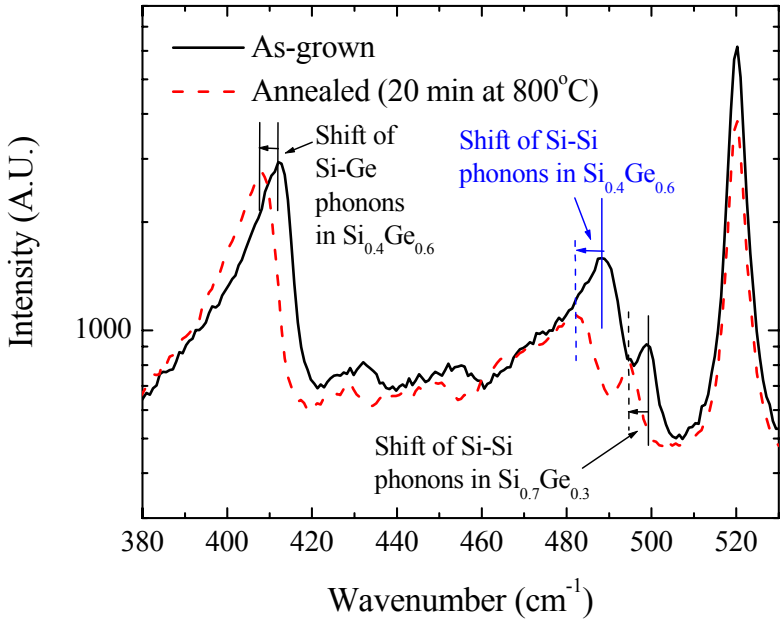
After epitaxy, Raman spectroscopy shows strain of 0.0% in the $Si_{0.70}Ge_{0.30}$ layer and an initial strain ε_0 of –1.1% in the $Si_{0.4}Ge_{0.6}$ layer, in good agreement with that of –1.2% expected from the compositions of the two layers. This sample was then annealed at 800^{o}C for 20 min. Given the thick BPSG and island thickness, the duration of this anneal should be adequate for islands to reach stress balance. As shown in Fig. 6.13(b), all phonon peaks from $Si_{0.70}Ge_{0.30}$ and $Si_{0.4}Ge_{0.6}$ films shift toward lower wavenumbers upon stress balance, indicating stretching of the films. This is consistent with expected lateral expansion of the $Si_{0.70}Ge_{0.30}$ and $Si_{0.4}Ge_{0.6}$ films. The final strains in the $Si_{0.70}Ge_{0.30}$ and $Si_{0.4}Ge_{0.6}$ layers are 0.55% and –0.50%, respectively. The fact that the strain in both films increased almost identically by about 0.60% indicates that the two layers remained coherent within experimental error. The strain data from Raman measurement is summarized in Fig. 6.14. Along with the coherent bilayer condition, the stress balance equation (Eqn. 4.19) can be used to predict the final strain:

$$\varepsilon_{Ge=30\%} = -\varepsilon_0 \frac{E_{Ge=60\%} h_{Ge=60\%}}{E_{Ge=30\%} h_{Ge=30\%} + E_{Ge=60\%} h_{Ge=60\%}} = 0.54\% \qquad (6.7)$$

$$\varepsilon_{Ge=60\%} = \varepsilon_0 \frac{E_{Ge=30\%} h_{Ge=30\%}}{E_{Ge=30\%} h_{Ge=30\%} + E_{Ge=60\%} h_{Ge=60\%}} = -0.57\% \qquad (6.8)$$



(a)



(b)

Fig. 6.13: (a) $Si_{0.4}Ge_{0.6}$ is grown on $Si_{0.70}Ge_{0.30}$ to form a bi-layer structure. (b) Raman spectra, measured at the center of a 20 μm x 20 μm island comprising 30-nm $Si_{0.4}Ge_{0.6}$/30-nm $Si_{0.7}Ge_{0.3}$, before and after 800°C annealing for 20 min. All phonon peaks from both films shift toward lower wavenumbers after an annealing to reach stress balance, consistent with coherent lateral expansion of the island.

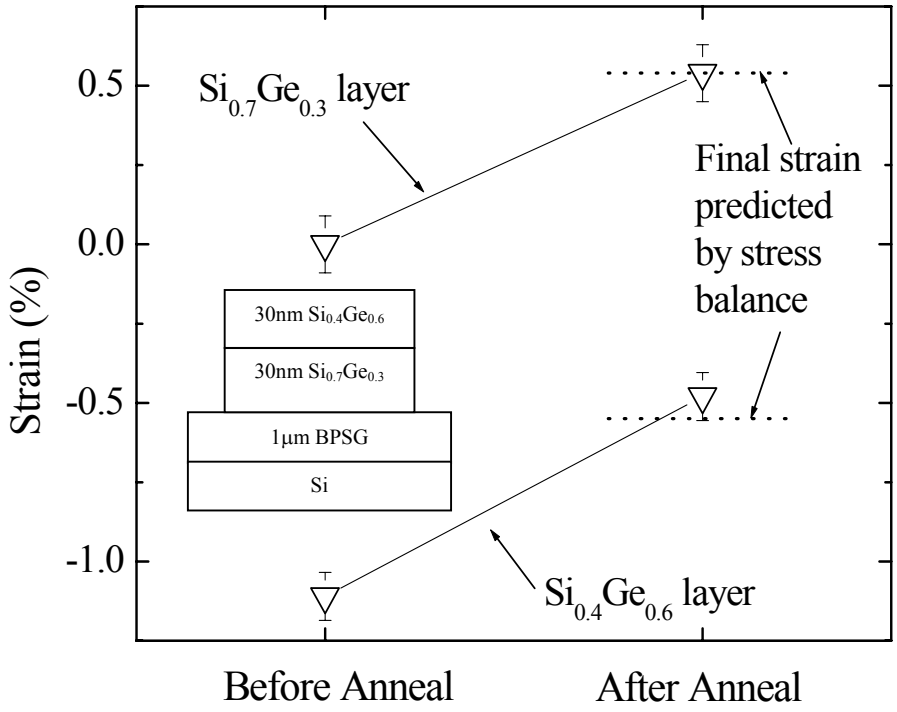


Figure 6.14: Biaxial strain of $Si_{0.7}Ge_{0.3}$ and $Si_{0.4}Ge_{0.6}$, measured by Raman spectroscopy at the center of a 20 μm x 20 μm island, before and after 20-min annealing at 800°C. Open symbols are experimental data and dotted lines are based on calculation of stress balance.

where Poisson's ratio is taken to be the same in both films for simplification, and $E_{Ge=60\%}$ is 11.4 x 10^{10} N/m^2. Clearly, the stress balance theory accurately predicts the final strain in the films. The in-plane lattice constant of the bilayer at stress balance is equivalent to that of a relaxed $Si_{1-x}Ge_x$ layer with x equal to the average Ge content of this bilayer, which is 45% in this case.

A larger final in-plane lattice constant could in principle be achieved with a thicker $Si_{0.4}Ge_{0.6}$ film or a film of higher Ge content. However, thick layers and/or high Ge content are difficult to grow in practice due to the critical thickness constraint. Alternatively, thinner starting $Si_{0.70}Ge_{0.30}$ layers will lead to a higher average germanium content in the bilayer and thus more relaxation of the $Si_{0.4}Ge_{0.6}$ film and a larger in-plane lattice constant. The dependence of the final strain in the 30-nm $Si_{0.4}Ge_{0.6}$ film on the thickness of the $Si_{0.7}Ge_{0.3}$ layer, based on Eqn. (6.8), is plotted in Fig. 6.15, which also shows the effective germanium content (defined as the Ge-content of a fully-relaxed SiGe film with the same in-plane lattice constant as that of the layer) of this bilayer. We therefore thinned the original 30-nm fully-relaxed $Si_{0.7}Ge_{0.3}$ layer in a solution of HNO_3:H_2O:HF(0.5%) = 35:20:10 [19], followed by deposition of a 30-nm $Si_{0.4}Ge_{0.6}$ layer. This bilayer was annealed at 800^{o}C for 20 min to reach stress balance. It is difficult to know the exact thickness of the $Si_{0.7}Ge_{0.3}$ layer after etching because of uncertainty in etch rate, but the thickness can be calculated from the measured final strain in the $Si_{0.4}Ge_{0.6}$ and $Si_{0.7}Ge_{0.3}$ layers, based on Eqns. (6.7) and (6.8) (Fig. 6.15). The thickness of the etched $Si_{0.7}Ge_{0.3}$ layer was estimated to be 13 nm and 6 nm (Fig. 6.15).The equivalent Ge content reached 51% and 55%, respectively, which shows that this thinning method is very effective in achieving relaxed, high Ge content films.

6.5 Summary

In conclusion, two approaches to increasing germanium content in relaxed SiGe films on BPSG have been demonstrated. The combination of SiGe oxidation and compliant BPSG enables strain relaxation through lateral expansion while increasing germanium content. The strain relaxation observed in SiGe oxidation with an oxide cap is greater than expected due to a super-viscous layer formed by stress-induced viscosity reduction. Growing SiGe with higher germanium content on relaxed SiGe/BPSG can

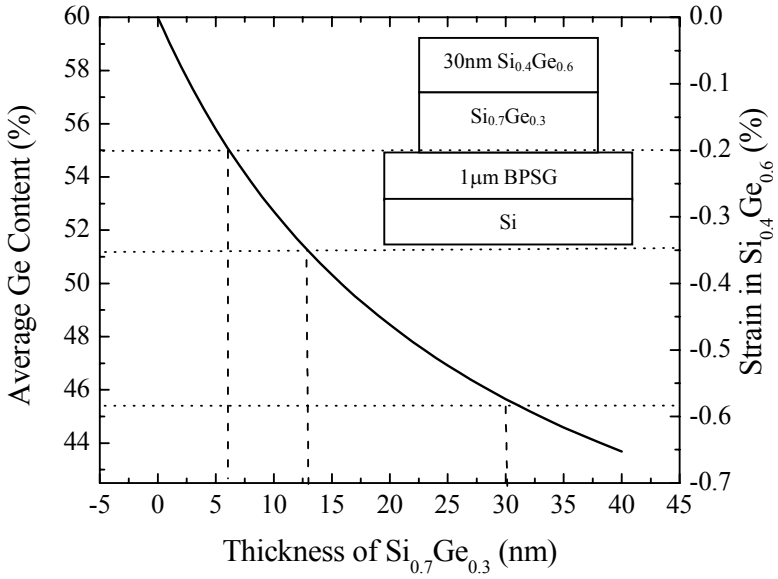


Fig. 6.15: Average Ge content, predicted by stress balance, as a function of the $Si_{0.7}Ge_{0.3}$ thickness for 30-nm $Si_{0.4}Ge_{0.6}$. Right Y-axis reflects the expected strain in the $Si_{0.4}Ge_{0.6}$ film. The dotted lines show the equivalent Ge content based on the measured strain in the $Si_{0.4}Ge_{0.6}$ and $Si_{0.7}Ge_{0.3}$ films, which is then used to estimate the thickness of the $Si_{0.7}Ge_{0.3}$ film.

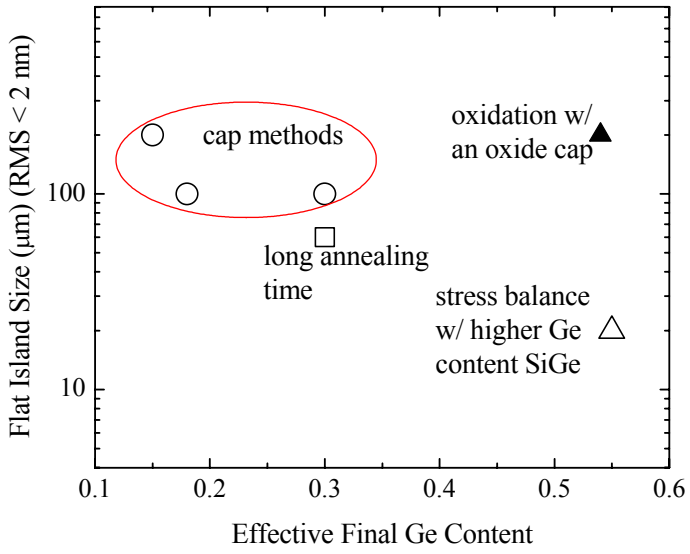


Figure 6.16: Summary of the maximum edge size and effective germanium fraction of flat (RMS roughness < 2 nm), crack-free, relaxed, square islands obtained using various cap techniques from an initial 30-nm fully-strained $Si_{0.7}Ge_{0.3}$ film on 200-nm BPSG.

result in larger in-plane lattice constant after stress balance is achieved, leading to a higher effective germanium content in the structure. The advantage of both methods lies in the fact that in principle both methods can provide film of very low defect density.

Figure 6.16 summarizes the effective germanium content and flat island size obtained through various techniques, beginning with a 30-nm $Si_{0.7}Ge_{0.3}$ compressive film on 200-nm BPSG. The use of SiGe oxidation and stress balance with higher Ge-content SiGe enables us to achieve effective germanium contents higher than 50%

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Chapter 7

Ultra-thin Strained-Si n-channel MOSFETs on BPSG

The enhancement of mobility due to strain has emerged as an option to boost CMOS transistor technology performance as scaling enters the sub-100 nm regime. In this chapter, the background of strained silicon MOSFETs, including the current approaches used in industry, will be reviewed. The process flow to create strained silicon on BPSG without SiGe, which was developed as part of this thesis, will be described. The detrimental dopant diffusion from BPSG to active layers has been studied and a nitride layer has been successfully utilized to completely block the diffusion. Finally, the fabrication and characteristics of n-channel MOSFETs in ultra-thin strained silicon will be discussed.

7.1 Motivation and background

The common techniques for strain generation used by the industry fall into two categories: substrate-induced strain and more recently process-induced strain.

7.1.1 Substrate-induced strain

The use of substrates for strain creation usually relies on relaxed SiGe buffer layers grown on bulk silicon wafers (so-called "virtual" SiGe substrates). Figure 7.1 shows a schematic diagram of a strained Si MOSFET fabricated on a virtual SiGe substrate. This is the leading technology at present and substrates are commercially available. There are still outstanding issues with these substrates. For example, the best defect density in SiGe virtual substrates is ~10^5 cm^{-2}, which may impact device yields. They require thick graded SiGe buffers (~ 3 μm for 30% Ge). Making things even more complicated, the presence of SiGe in the substrates gives rise to new integration problems, such as the diffusion of germanium, difficulty in forming low-resistance silicides and altered dopant diffusion compared to that in silicon [1]. Therefore, the substrate-induced strain comes at a much higher cost and risk than using process-induced strain at present. But the strain

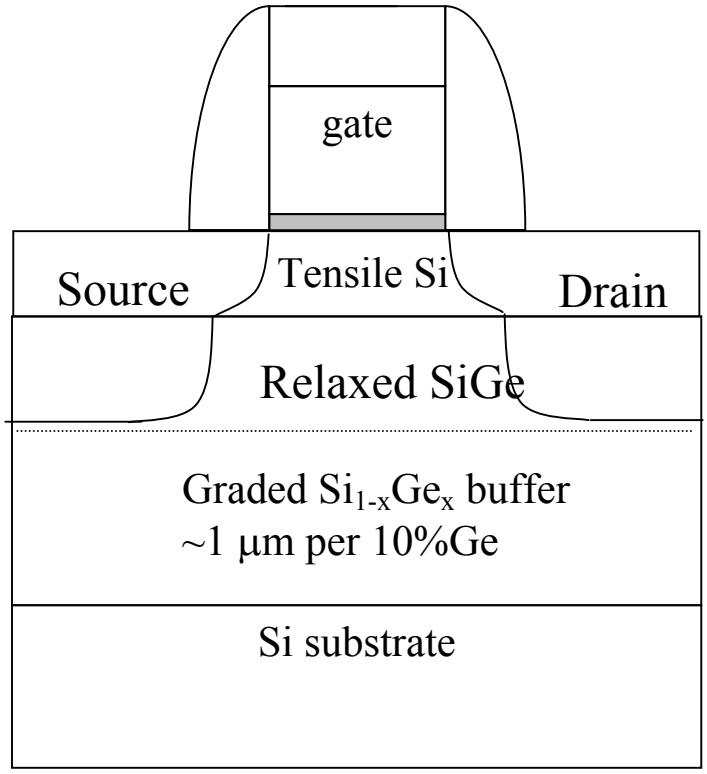


Figure 7.1. Schematic diagram of a strained Si MOSFET fabricated on a graded SiGe buffer layer. Often a buffer of a uniform germanium content is grown on top of the graded buffer (at the fixed germanium level) before the strained silicon is grown.

induced by substrates is usually one order of magnitude higher than the process-induced strain, leading to much more device performance improvements.

7.1.2 Process-induced strain

Figure 7.2 illustrates various ways to engineer strain using processing steps (i.e. without directly growing strained silicon on a relaxed SiGe layer). Capping layers, often made of highly compressive nitride films, are the most common approach to strain the silicon channel [2-5]. They are deposited after the FETs are fabricated. The stress from the compressive nitride gives rise to a tensile strain in the channel. In another approach, shallow trench isolation (STI) can also be employed to strain the silicon channel [2]. The proximity of source/drain (S/D) relative to the channel region makes it possible that steps which also cause strain in the S/D region will cause strain in the channel region [2]. Most notably, Intel refilled the S/D region using selective SiGe regrowth after etching the S/D silicon to generate compressive strain in the channel to enhance hole mobility [4,5]. Intel's implementation of strained silicon devices improves drive current about 25 percent in PMOS and about 10 percent in NMOS with its 90-nm process while only increasing the manufacturing cost by two percent [6]. The low cost shows that these approaches enable performance improvement at little cost.

7.1.3 Strained silicon on insulator

The silicon-on-insulator (SOI) structure has long been known for its superior properties over its bulk counterparts, such as reduced parasitic capacitance and lower leakage current [7]. In addition, SOI structures facilitate the fabrication of multi-gate devices designed to suppress short channel effects (SCE) [8]. Therefore, the combination of strained silicon and SOI offers a promising opportunity for device performance improvement.

There have been numerous efforts to date towards achieving this hybrid structure. The first type involves the formation of relaxed SiGe on insulator (SGOI) followed by epitaxial Si regrowth [9,10]. However, the thickness of the combined layers usually exceeds 100 nm, which is too thick to suppress SCE. Furthermore, the SiGe presence can cause process technology problems as mentioned earlier. Therefore, a strained-silicon-on-

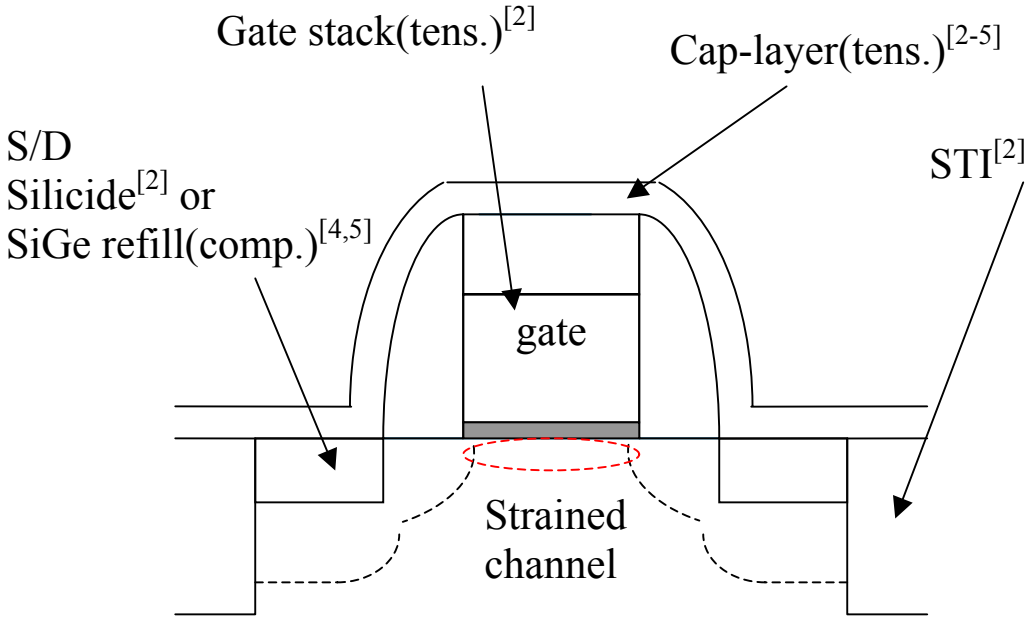


Figure 7.2: Shallow trench isolation (STI), source/drain (S/D) processing, gate stack and capping layers are used to induce strain in the channel region for device performance improvement that does not involve epitaxy. Usually one method is used alone. The S/D methods are used to give compressive strain, and the gate stack or capping layers are engineered to give tensile strain.

insulator (sSOI) structure without SiGe is very attractive. The common approach to such SiGe-free layers involves transferring strained silicon grown on relaxed, compositionally graded SiGe buffers directly onto silicon dioxide, followed by the removal of the transferred SiGe buffer [11-14]. In all of these approaches, the quality of the strained silicon depends on the quality of the original relaxed SiGe buffer layers, of which is limited in practice by threading defect density of $\geq 10^5$ cm^{-2} [15]. Furthermore, these relaxed buffer layers in practice require thick epitaxial graded layers and chemical-mechanical polishing (CMP) steps to overcome roughening [16].

Here, a novel approach, based on stress balance on insulating BPSG was explored to achieve ultra-thin sSOI without SiGe [17]. It involves the growth of only very thin (tens of nm) epitaxial layers, which enables us to fabricate fully-depleted strained-Si n-channel MOSFETs.

7.2 Fabrication of SiGe-free, strained Si on insulating BPSG layers

In Chapter 4, it was demonstrated that strained SiGe, pseudomorphically grown on a silicon substrate and then transferred onto BPSG, can relieve strain through lateral expansion of the SiGe when BPSG is turned viscous during high temperature anneals [18]. Strained Si could then be grown on the relaxed SiGe/BPSG, but the SiGe would be present in the structure.

To obtain SiGe-free sSOI using the compliant BPSG insulator, a different structure was used. Unstrained 25-nm Si /30-nm strained $Si_{0.7}Ge_{0.3}$ was commensurately grown on a silicon "host" wafer. The "handle" wafer was a silicon wafer coated with a BPSG layer. A SiGe/Si/BPSG stack was formed after the Si/SiGe structure on the "host" wafer was transferred onto the "handle" wafer using the wafer bonding and Smart-cut® process that was described in chapter 3. Positioning the SiGe at top of the stack allows SiGe removal later. After the layer transfer the strain in the SiGe and Si were unchanged as the BPSG viscosity is very high at the temperatures used during layer transfer and the BPSG provided a constraining force to prevent strain relaxation. The process flow of strain generation in the silicon is described in Figure 7.3(a). The SiGe/Si structure was

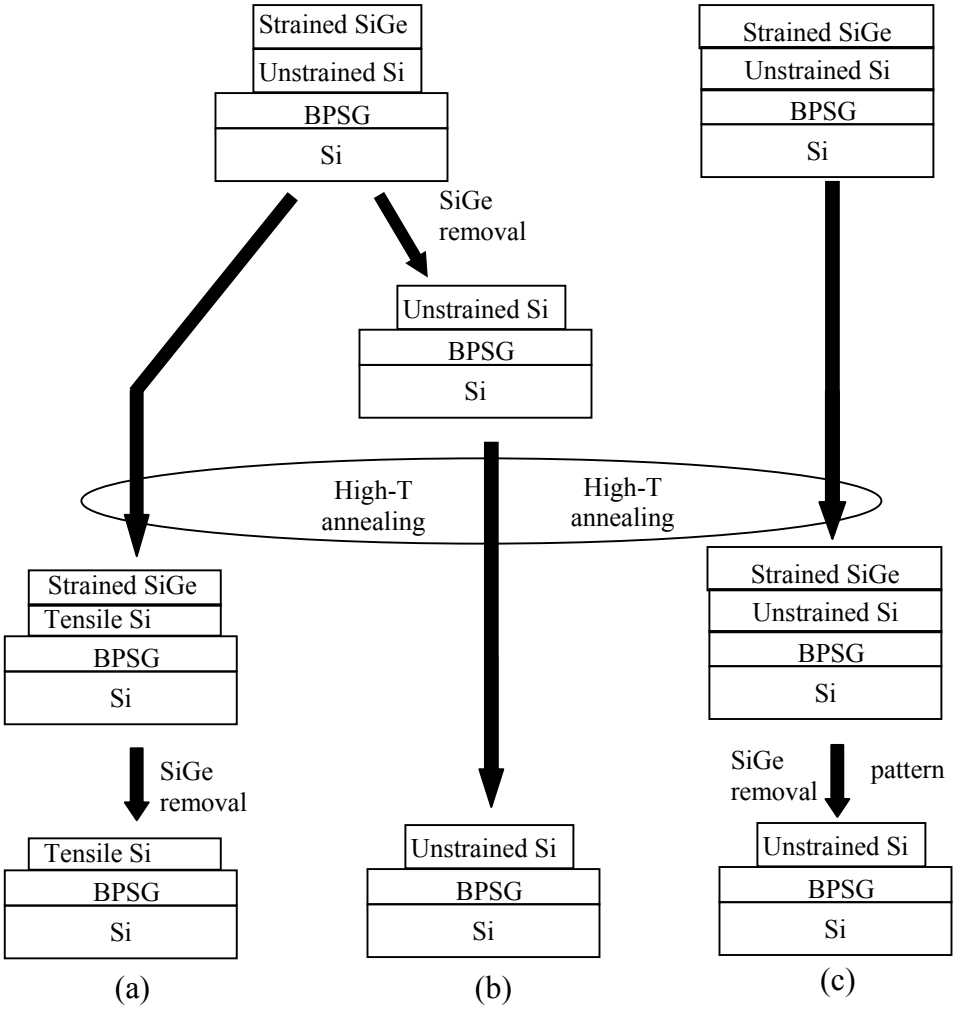


Figure 7.3: Process flow of (a) strained Si on a BPSG insulator and (b),(c) unstrained Si on a BPSG insulator, which is integrated with the process of (a). The process (b) relies on the removal of the SiGe prior to the high-T anneal. The process (c) uses the slow lateral expansion of continuous/large features.

patterned into square islands of edge width from 30 to 200 μm. Annealing at 800°C softened the BPSG and the compressive strain in the SiGe film drove the lateral expansion of the SiGe film, stetching the underlying Si film because the silicon and SiGe are coherent. The lateral expansion process of the structure ended when the SiGe and Si films reached a stress balance condition. The final strain ε_{Si} in the Si film upon stress balance is expressed by Eqn. 4.19. The magnitude of the tensile strain created in the Si film upon stress balance depends on the original strain and thickness of the SiGe film and silicon, which determines its stretching ability when the SiGe film is viewed as a type of stressor. It is clear that a thick SiGe film with high strain (i.e. high germanium content) is preferred for achieving large tensile strain in the Si film. However, the thickness and germanium content one can use in the stretching SiGe film are limited by the equilibrium critical thickness [19], beyond which the strain in the SiGe film is released by dislocations during its original growth.

The generation of tensile strain in the Si film during an 800°C anneal, accompanied by strain relaxation in the SiGe film, is shown in Figure 7.4. The size of the SiGe/Si square islands ranges from 30 to 60 μm. All strain data were collected by Raman scattering at the center of islands. Also shown in Figure 7.4 are the strain values predicted based on the stress balance theory (Eqn. 4.19), in good agreement with the final measured strain levels. As the compressive strain in the SiGe film decreased from 1.2% to 0.6%, the tensile strain in the silicon film increased from zero to about 0.6% at the same rate. As expected, the relaxation of large islands is slower than that of small islands.

Raman spectra collected after the layer transfer (solid line) and after stress balance (dashed line) are plotted in Figure 7.5. After the layer transfer, the silicon film remained unstrained and its Raman peak overlaid that of the silicon substrate. When stress balance was reached, the Raman peak from the silicon film shifted to a smaller wavenumber, indicating a tensile strain. At the same time, the Raman peak from the SiGe film also moved to a smaller wavenumber due to partial strain relaxation.

Once the silicon film was strained, the top SiGe film has served its purpose and was removed to produce a SiGe-free sSOI. Because the silicon film (25 nm) was thin compared to the SiGe (30 nm), a selective SiGe etch was used to remove the top SiGe

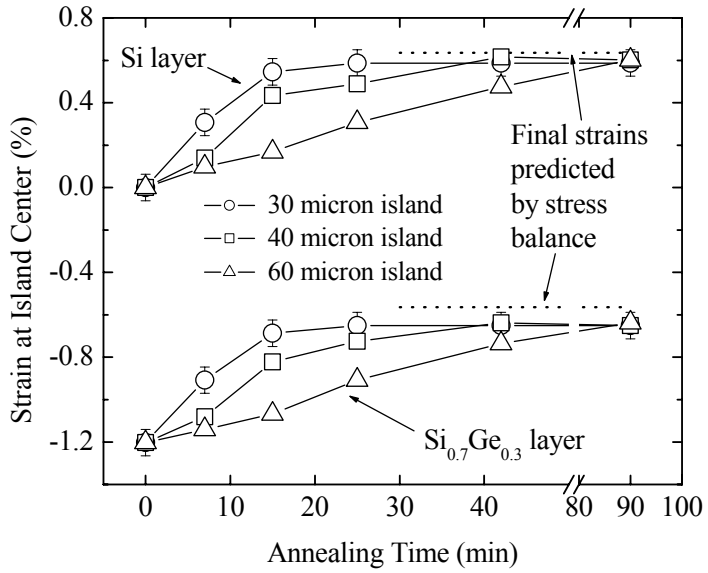


Figure 7.4: Biaxial strain (from micro-Raman spectroscopy) of 30-nm $Si_{0.7}Ge_{0.3}$ and 25-nm Si films at the center of a 30 μm x 30 μm island as a function of annealing time at 800°C, showing the evolution of strain in the silicon and SiGe layers. Dashed lines are calculations of stress balance.

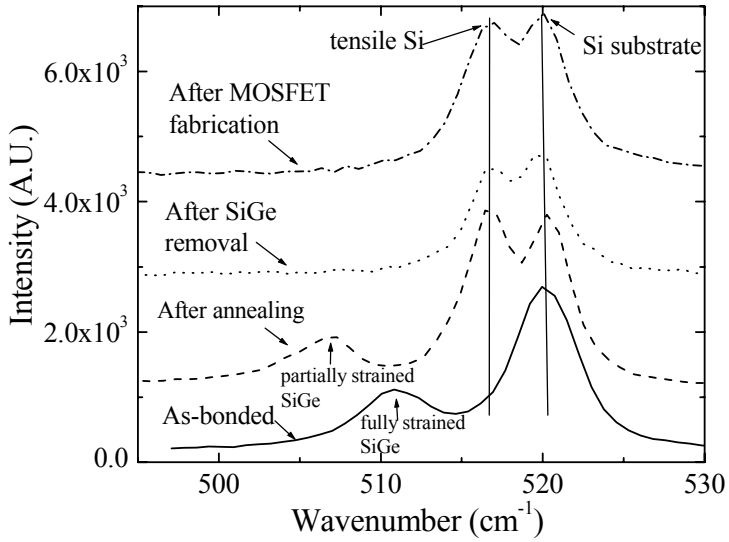


Figure 7.5: Raman spectra measured at the center of a 90 μm x 90 μm island at various stages of processing. The peak positions depend on composition and strain. The annealing reduces the compressive strain in the SiGe and adds tension in the Si. The missing SiGe Raman peak after the SiGe etch confirms the complete removal of the SiGe. The FET process does not alter the strain in the silicon.

film. A solution consisting of HF(6%):H_2O_2(30%):CH_3COOH (99.8%):(1:2:3), chosen for its good selectivity (> 30) and fast SiGe etch rate, was used at room temperature. The solution is known to vary over time [20], so its etch properties was measured as a function of storage time (Fig. 7.6). The SiGe etch rate nearly doubled after three weeks, but the selectivity did not degrade and remained better than 30. Also, no dependence of the etch rate on strain was observed for SiGe. With the good etch selectivity, less than 1-nm Si over-etch in the SiGe removal process was achieved. The thickness of thin SiGe and Si films on BPSG was measured using spectroscopic reflectometry, which had a repeatability of ~ 1 nm. The disappearance of the SiGe Raman peak after the SiGe etch indicates that all SiGe was removed and the strain in a silicon layer as thin as 25 nm can clearly be measured (Fig. 7.5). Figure 7.7 depicts a 10 x 10 μm^2 AFM scan, with a 0.18 nm RMS surface roughness. The absence of crosshatch in the strained Si film indicates dislocations were not involved in the stress balance process.

There are a few schemes for integrating strained and unstrained silicon on the same wafer (Fig. 7.3), which may be advantageous for applications where strain levels need to be tailored for different devices. The first method involves the selective removal of the SiGe before the stress balance anneal (Fig. 7.3(b)). Without SiGe, no strain in the silicon will develop. The second method takes advantage of the slow lateral expansion of large islands (Fig. 7.3(c)). For finite annealing times, no relaxation in the large areas will occur. Both of them can be readily implemented using a lithographic step to either define the selective etch areas or large islands.

7.3 Suppression of dopant diffusion from BPSG

Our work requires a (~800^{o}C) high-temperature anneal to soften the BPSG to allow its viscous flow. The BPSG viscosity can be reduced by a factor of five when annealing temperature is elevated from 750^{o}C to 800^{o}C (Sec. 5.2.1), which effectively speeds up strain generation rate by five times, allowing strain generation in large islands within a reasonable time frame. However, these anneals could result in the diffusion of boron and phosphorus from BPSG into the silicon film. Figure 7.8(a) shows the doping profile, measured using secondary ion mass spectroscopy (SIMS), in a thin silicon layer on BPSG after 1-hr annealing at 800^{o}C and 850^{o}C, respectively. Little diffusion was seen after the

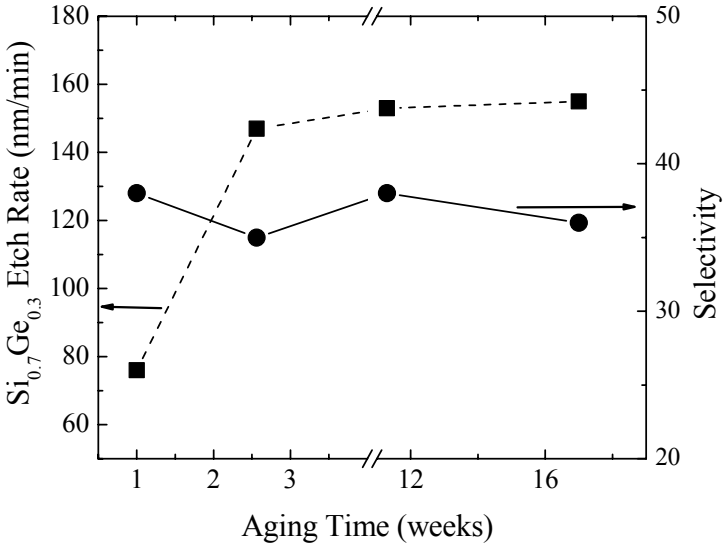


Figure 7.6: Aging effect on the SiGe etch rate and the selectivity relative to silicon of a buffered $HF:H_2O_2:CH_3COOH$ etch. The etch rate stabilizes after two weeks.

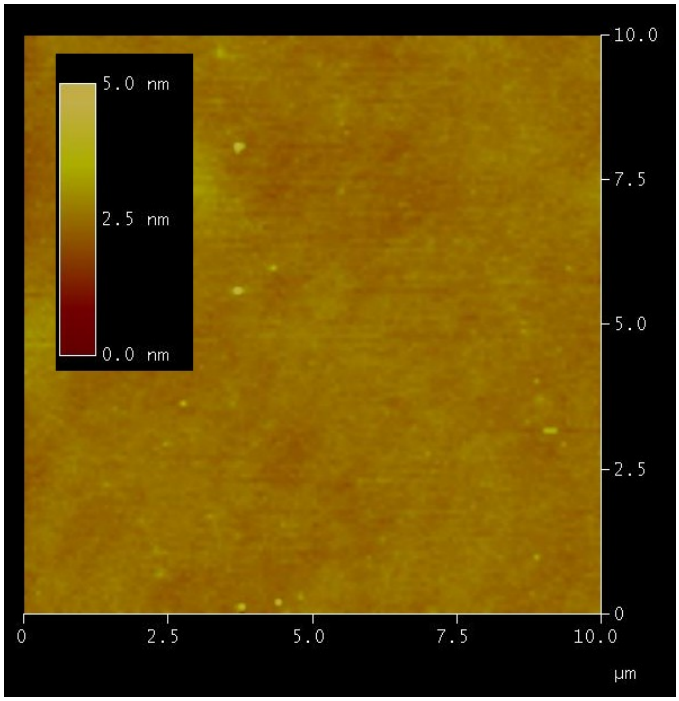
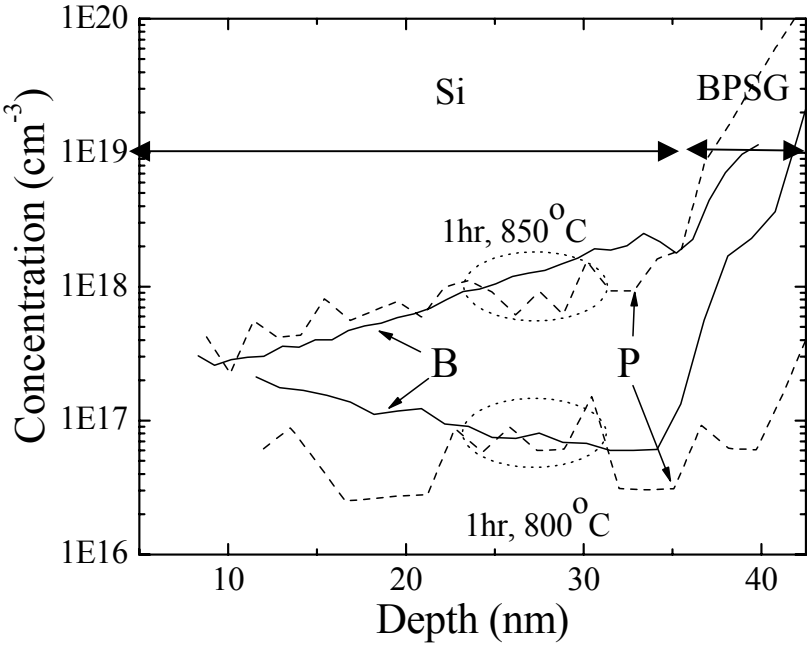
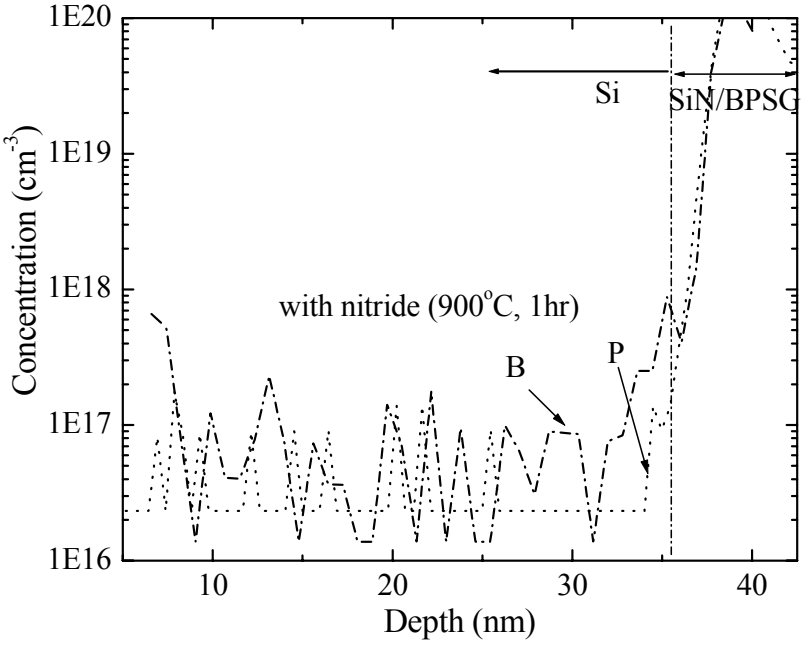


Figure 7.7: AFM 10 x 10 μm^2 scan of 25-nm strained Si on BPSG after SiGe removal. The RMS surface roughness is 0.18 nm.



(a)



(b)

Figure 7.8: Doping concentration in the Si film on BPSG after annealing. The vertical line denotes the Si/BPSG interface. (a) Samples without a nitride layer annealed for 1 hr at 800°C or 850°C. (b) A sample with a 5-nm nitride layer between the BPSG and silicon to block dopant diffusion, annealed at 900°C for 1 hr.

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800°C anneal and devices with enhanced mobility in such films will be reported later in this chapter. The 850°C anneal caused considerable boron and phosphorus diffusion into the silicon film. Because silicon nitride layers are known dopant barriers [21], in a separate experiment a thin (~5 nm) silicon nitride layer was deposited onto a 10-nm Si/30-nm $Si_{0.7}Ge_{0.3}$ structure using LP-CVD at 725°C prior to the layer transfer. The tri-layer structure (Si_3N_4/Si/SiGe) was then transferred onto BPSG, sandwiching the nitride layer between the BPSG and SiGe/Si. The structure was annealed at 900°C for 1 hr to test the barrier against dopant diffusion. The boron and phosphorus levels in the silicon layer were now below SIMS detection limit (5 x 10^{16} cm^{-3}) (Fig. 7.8(b)), indicating the effectiveness of the thin barrier.

Since the silicon nitride film is elastic, the SiGe layer would stretch the nitride layer along with the Si layer, potentially generating a smaller strain level than the nitride-free structure. In the stress balance relationship (Eqn. 4.19), the silicon nitride contributes to an effectively thicker silicon layer. This is why the silicon nitride layer was kept so thin. In this case, the effective silicon thickness in Eqn. 4.19 becomes

$$h_{Si,eff} = h_{Si} + \frac{E_{Si_{33}N_4}(1-\nu_{Si})}{E_{Si}(1-\nu_{Si_3N_4})} h_{Si_3N_4} \qquad (7.1)$$

To investigate this effect, the tri-layer structure was patterned into islands and then annealed to reach stress balance. Figure 7.9 shows the Raman spectra taken before and after annealing. The strain level in the silicon film is 0.73%, even higher than the strain (~0.6%) obtained in the nitride-free 30-nm $Si_{0.7}Ge_{0.3}$/25-nm Si sample. The higher strain stems from the much thinner (10 nm) Si layer used in the sample with a nitride layer. With the nitride, the effective silicon thickness $h_{Si,eff}$ (as defined in Eqn. 7.1) is 20.8 nm. When the silicon nitride layer is accounted for as an effective silicon layer, the final strain in the 10-nm silicon film is in line with stress balance prediction (Fig. 7.10). The strain would have been much higher (0.89%) if the silicon nitride layer had not been considered. The excellent dopant diffusion suppression of the 5-nm nitride film discussed above suggests that an even thinner silicon nitride layer can be used to suppress diffusion and allow more strain in the silicon.

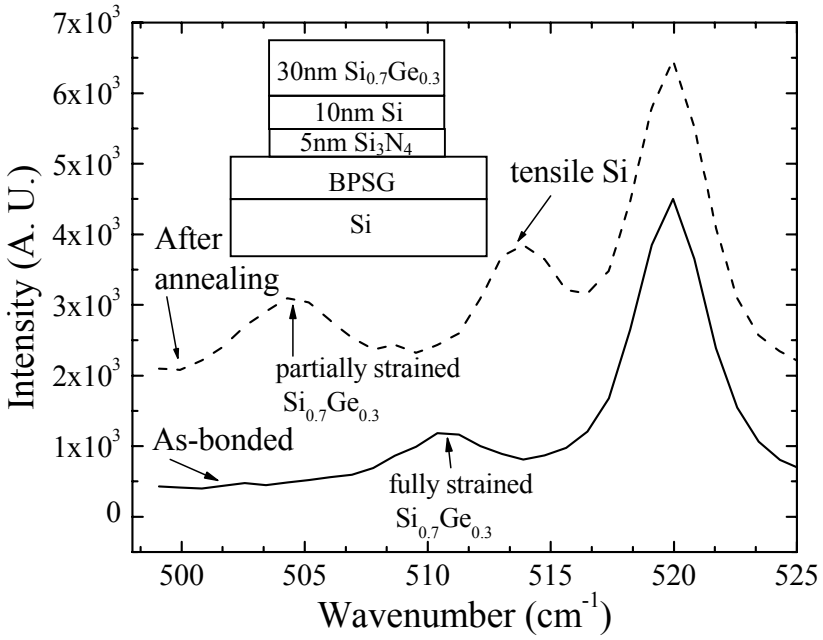

Figure 7.9: Raman spectrum (Si-Si neighbor vibration mode) measured at the center of a 30 μm x 30 μm island (30nm-SiGe/10nm-Si/5nm-Si_3N_4/1μm-BPSG) after annealing at 800°C for 30 min. The Si layer was still stretched by compressive SiGe even when the Si_3N_4 layer was present.

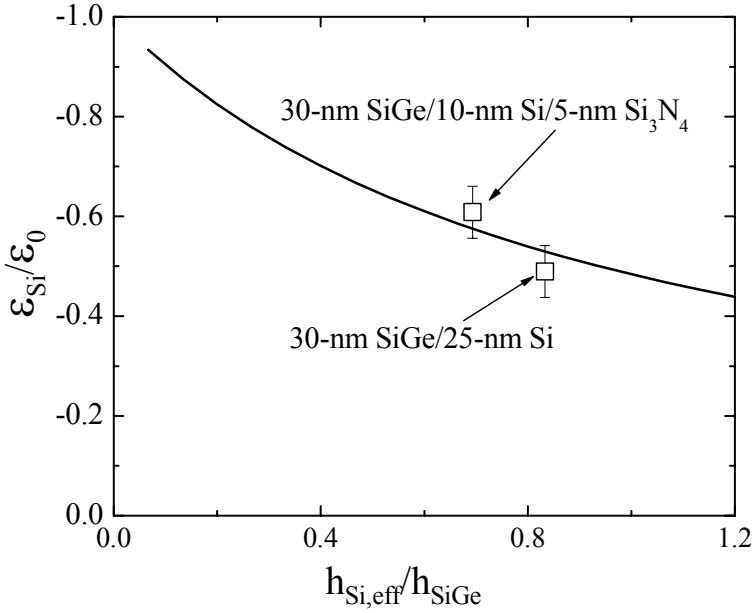

Figure 7.10: Ratio of the final strain in the silicon after stress balance to that in the initial SiGe layer as a function of the ratio of the effective silicon thickness to that of the SiGe layer. Data points for 30-nm SiGe/25-nm Si and 30-nm SiGe/10-nm Si/5-nm Si_3N_4 are given.

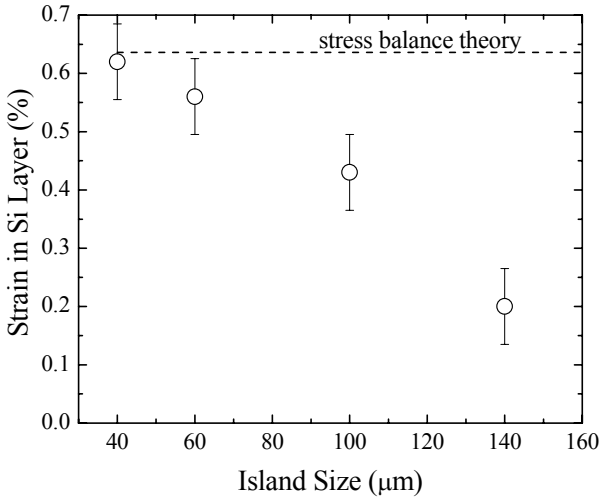

Figure 7.11: Island-size dependence of the silicon strain, measured at island center, in 30-nm $Si_{0.7}Ge_{0.3}$/25-nm Si on 200-nm BPSG after 1 hr annealing at 800°C.

One outstanding question, however, is the electrical quality of the nitride/Si interface. Because the silicon film is so thin, FET operation will require modulation of the Fermi level at the lower as well as the upper silicon interfaces, so that traps at this interface could limit our ability to turn the device on/off. Fixed charges would also affect the threshold voltage.

7.4 Device fabrication

Self-aligned long-channel n-channel MOSFETs were fabricated using the strained silicon film, obtained from 30-nm $Si_{0.7}Ge_{0.3}$/25-nm Si on 200-nm BPSG as described in the previous section, for the device channel. In this case, the nitride layer from the previous section was not used. The SiGe/Si bi-layer was annealed for 1 hr at 800°C and the generated strain level in the silicon varied with island size (Fig. 7.11). Strain was negligible in island size larger than 200 μm due to the slow lateral relaxation of large islands. For fair comparison, the control (unstrained) devices were fabricated on the same sample using islands larger than 3 mm, where strain in the silicon layer was nearly zero (Fig. 7.3(c)). The gate stack was comprised of TEOS oxide and poly-silicon, both deposited at 625°C using low-pressure chemical vapor deposition (LP-CVD). Two gate

oxide thicknesses (26 nm and 300 nm) were used. The use of the TEOS oxide, instead of thermal SiO_2, for the gate dielectric, was intended to minimize thermal budget to avoid relaxation of the strained silicon film during the gate dielectric formation. During such oxidation, there would be no thick layers on top of the channel to prevent strain relaxation. Phosphorous implantation (35keV, $1x10^{15}cm^{-2}$) was used to dope the source/drain and the gate poly. A blanket of 300-nm low-temperature PE-CVD SiO_2 was deposited prior to a 1 hr anneal at 800^oC, which was to activate and drive in implanted dopants. The thick stack on top of the channel, consisting of PE-CVD SiO_2, gate poly and TEOS gate dielectric, helped to retain the strain in the channel during the 800^oC anneal, during which the underlying BPSG was viscous. After device fabrication, Raman spectroscopy was performed on a device channel (L = 10 μm) after removing the gate poly silicon (Fig. 7.5). No strain relaxation was observed during the device processing.

7.5 Device results

7.5.1 Threshold voltage and subthreshold swing

Both strained and unstrained n-channel MOSFETs were well behaved with strained devices exhibiting much higher drive current (Fig. 7.12) than the unstrained control devices on the same substrate. The buried BPSG serves as a backgate and the voltage applied to the substrate can also modulate the carriers in the channel. Figure 7.13 depicts the transfer characteristics of a strained device with 26-nm TEOS gate dielectric at different substrate biases. The substrate bias not only shifted the transfer characteristic, suggesting a changed threshold voltage, but also affected the subthreshold swing. Figure 7.14 plots the dependence of the top-gate threshold voltage on the voltage applied to the silicon substrate. The threshold voltage was extracted by linearly extrapolating drain current vs. gate-source bias to the x-axis intercept for a fixed drain-source voltage of 0.01V. The threshold voltage is similar in both strained and unstrained devices. The linear dependence of the threshold voltage on the applied substrate voltage indicates the devices operate in the fully-depleted mode, which is consistent with the thin silicon channel (~ 25 nm) used here. The measured large negative threshold voltage (-32 V for 300-nm TEOS and -2.1 V for 26-nm TEOS) when the substrate was grounded is attributed to the high density of positive interface charges at the bonding interface of the

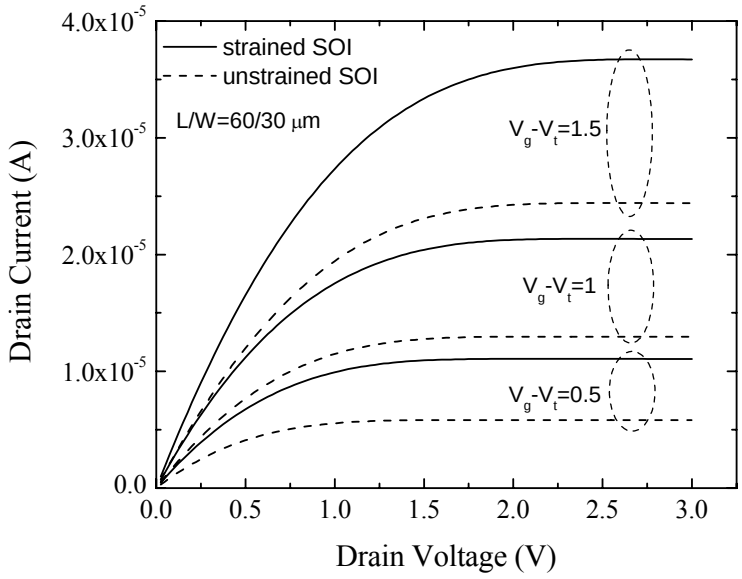

Figure 7.12: I_d-V_{ds} characteristic of the strained (ε=0.56%) device and the control (relaxed silicon on insulator) device on BPSG. The substrate-source bias was -15V.

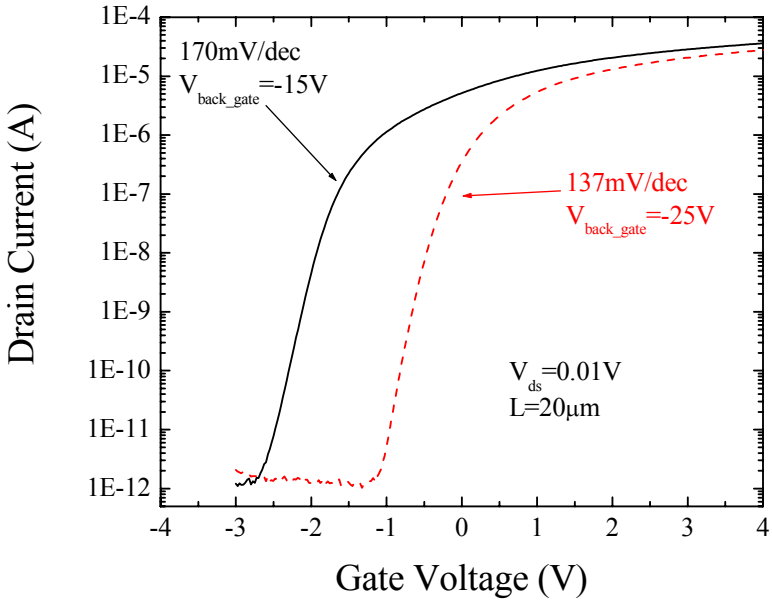

Figure 7.13: Drain current as a function of gate voltage measured on a strained device at different substrate-source biases.

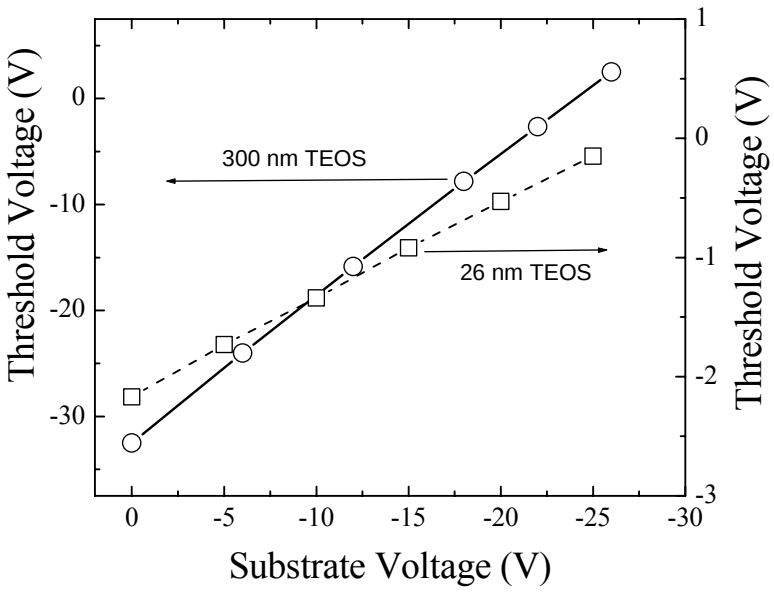

Figure 7.14: Substrate-voltage dependence of top–gate threshold voltage, measured on strained NFETs. The linear dependence shows that the devices operate in the fully-depleted mode. The source was grounded.

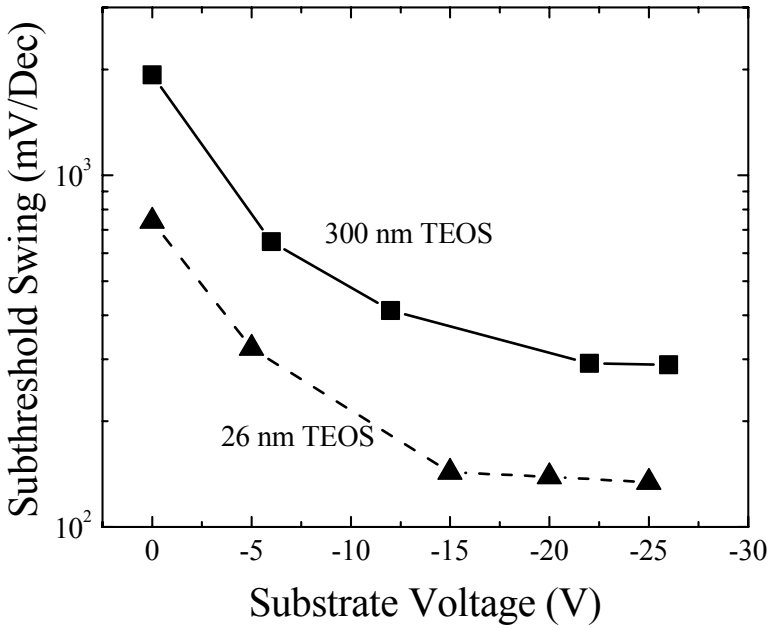

Figure 7.15: Substrate-voltage dependence of subthreshold swing, measured on strained NFETs. Negative substrate voltage greatly improves the subthreshold swing of the NFETs fabricated on BPSG. A thin (26 nm) TEOS gate dielectric shows much better subthreshold swing due to its increased gate control over the channel compared to the thick (300 nm) TEOS gate dielectric.

strained silicon and BPSG layers. The interface-charge density is estimated to be ~ 2 x 10^{12} cm^{-2}. In NFETs with 300-nm TEOS gate oxide fabricated on bulk silicon substrates, the threshold voltage is 2.7 V, which indicates that the interface of TEOS/Si-channel is not the cause of the large negative threshold voltage observed in devices fabricated on BPSG.

Even though a close-to-ideal subthreshold swing is expected for fully-depleted devices, the observed subthreshold swing of the devices on BPSG is much degraded (300 mV/dec for 300-nm TEOS and 140 mV/dec for 26-nm TEOS) (Fig. 7.15). Strained and unstrained devices have similar subthreshold characteristic. In devices fabricated on bulk silicon substrates, the subthreshold swing is better (~ 170 mV/dec for 300-nm TEOS). We think the poor subthreshold swing also stems from the poor electrical properties of the bonding interface since the high interface-state density adds to parasitic capacitance and reduces the gate control over the channel region [22]. Figure 7.15 compares the substrate-bias dependence of the subthreshold swing at different gate dielectric thicknesses for strained devices. The thinner gate dielectric gave a better coupling between the gate and the channel and thus a smaller subthreshold swing than the thicker gate dielectric. The trend of improving subthreshold swing with increasing negative substrate bias can be explained by nature of the initial conduction. When the substrate is biased at a voltage more negative than -15 V with respect to the source, it appears that the initial conduction (controlled by the top gate) is occurring at the usual interface between the top of the SOI and the top gate oxide. Because of the fully depleted nature of the SOI, even when the conduction initiates in the top channel, the turn-on can be degraded to some degree by the interface states at the lower Si/BPSG interface, since the electrical field from the top gate extends through this interface. When the substrate source bias is more positive than -15 V, the initial conduction is at the lower Si/BPSG interface, and the subthreshold swing will be more severely affected by any interface states at this interface, leading to the very poor subthreshold swing. It is expected that the interface of silicon and thermal silicon dioxide would have superior quality to that of Si/BPSG. One might try to overcome the poor Si/BPSG interface by a modification of the bonding process: forming a thin thermal silicon dioxide on the silicon prior to the wafer bonding.

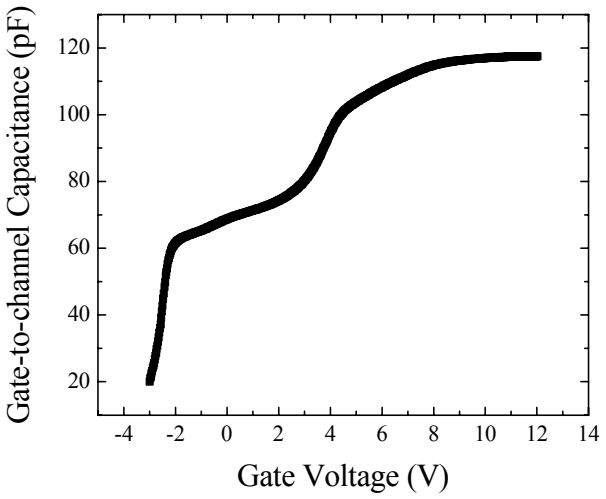

Figure 7.16: Gate-to-channel capacitance measured on a 300 x 300 μm^2 device with a source-substrate bias of -15 V. The frequency of 40 kHz was used to reduce the series resistance effect. The 120 pF plateau corresponds to a gate oxide of 26 nm, close to the expected value of 30 nm. Based on the data in Fig. 7.14, the expected value of the threshold voltage is -1 V.

7.5.2 Mobility enhancement

As shown in the previous section, the strained silicon devices exhibited enhanced current due to a higher mobility. We now analyze the mobility enhancement. The effective electron mobility was extracted from the drain current I_{DS} in the linear regime:

$$I_{DS} = (W/L)\mu_{eff} Q V_{DS}\,, \qquad (7.2)$$

where Q is the carrier concentration per unit area and V_{DS}=10 mV. The V_{GS} dependence of the gate-to-channel capacitance was measured and integrated from $V'_{GS} = V_T$ (threshold voltage) to V_{GS} to obtain the carrier concentration Q as a function of V_{GS}. The capacitance was measured on a large source-drain shorted device (300 x 300 μm^2) at a frequency of 40 kHz to minimize the error from the series resistance (Fig. 7.16). Fig. 7.17 shows the measured effective electron mobility as a function of carrier concentration for both strained and unstrained NFETs on BPSG with same device geometry. The source-substrate bias was set at -15 V to ensure that conduction occurred at the top Si/TEOS interface. The peak mobility enhancement was about 53%. The mobility enhancement

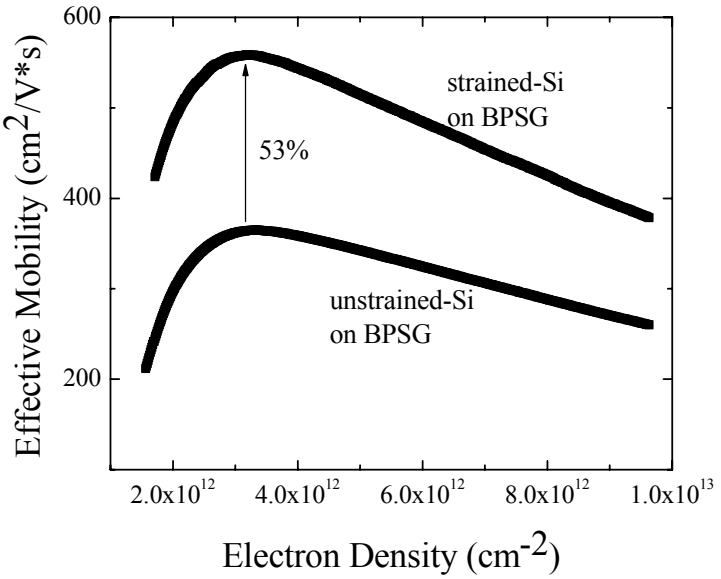

Figure 7.17: Effective electron mobility dependence on carrier density, measured on devices fabricated in 60 μm islands on BPSG (ε=0.56%). The substrate voltage was -15 V. The upper limit of electron density (10^{13} cm^{-2}) corresponds to a gate voltage of 12 V.

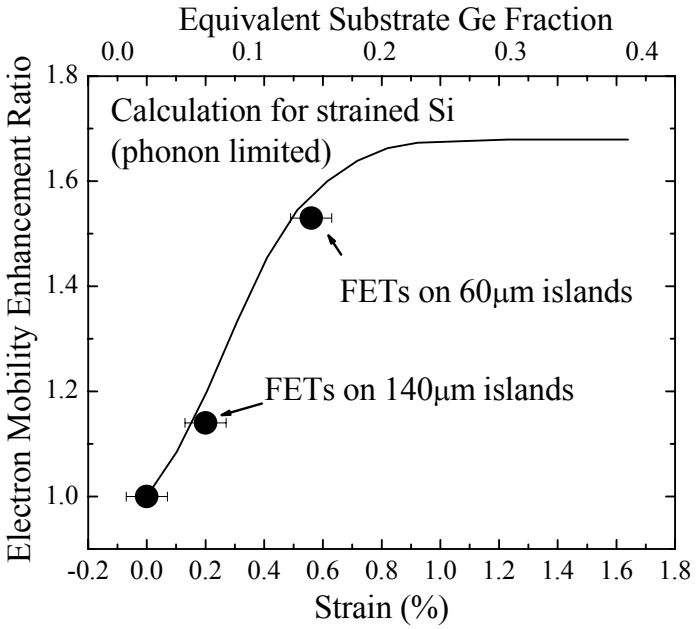

Figure 7.18: Enhancement of electron mobility in the strained silicon devices on BPSG compared to control silicon devices on BPSG as a function of strain in the silicon channel layer. Also shown on the top x-axis is the Ge fraction in relaxed SiGe buffers in conventional strained Si on relaxed SiGe structures to give the same strain as that on the lower x-axis.

was lower in devices fabricated on larger islands as a result of the lower strain on larger islands. On 140-μm islands, where the strain was only ~0.15% due to insufficient lateral relaxation, the mobility enhancement was 13% (Fig 7.18).

We also made NFETs with a very thin silicon layer (~10 nm) and a 5-nm nitride layer to block dopant diffusion as in Sec. 7.3. The NFETs did not "turn on" to give a reasonable S/D current. This could be due to a high interface-state density at the nitride interface preventing device turn-on, or a contact/series resistance problem associated withthe thin silicon. Contact and series resistance problems in such ultra-thin silicon FETs are well known.

7.6 Summary

Ultra-thin strained-silicon-on-insulator without a SiGe layer was successfully fabricated using stress balance between SiGe and Si films on compliant BPSG, with the silicon thickness as small as 10 nm. The use of a thin SiGe layer and the compliant substrate, instead of a thick SiGe buffer, enabled a process which avoids the generation of misfit dislocations and which avoids the growth of very thick epitaxial layers. To the best of our knowledge, this is the first time strained silicon FETs have been made in a final structure without any SiGe and with a process without thick SiGe epitaxial layers. Dopant diffusion from BPSG could be completely suppressed by a thin silicon nitride film. NFETs fabricated in 25-nm strained silicon films show good characteristics with mobility enhancement of 50%. The process possesses many attractive features for widespread applications.

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Chapter 8

Conclusion

8.1 Summary

Mechanisms and applications of compliant BPSG for strain engineering have been investigated in this thesis.

The viscous flow of the BPSG driven by the strained layers on top enables two simultaneous strain-relaxing processes, lateral expansion and buckling of the strained films. Various factors influencing the two processes were studied and varied to facilitate the desirable lateral expansion while hindering the unfavorable buckling.

The observation of stress balance between bi-layer structures on BPSG forms the cornerstone for strain engineering schemes discussed in this thesis. It also confirms that the strain relaxation occurs primarily without dislocations.

In demonstration of the versatility of compliant BPSG for strain manipulation, relaxed SiGe with high germanium content and strained Si were fabricated.

The realization of ultra-thin strained Si on insulator with no SiGe layers by stress balance has numerous advantages over the conventional methods. Work remains, however, to improve the electrical properties of the interfaces in these structures, especially the Si/BPSG interface.

8.2 Directions for future work

With the mechanisms of the compliant BPSG understood for strain engineering, we are in a good position to exploit its ability in strain-related applications. Furthermore, the demonstration of various strains (compressive and tensile or biaxial, orthorhombic and uniaxial) in SiGe and Si films lays a groundwork for optimization of device performance through strain manipulation. The possible directions of the future works are summarized as follows:

(a) Device application in relaxed SiGe with high germanium content

Low hole mobility has been a bottleneck for improving CMOS devices as it is only half of the electron mobility. Using tensile-strained Si improves electron mobility much more than hole mobility, simply worsening the disparity between p-channel and n-channel MOSFETs. Unlike tensile strain, the compressive strain, which is readily available in SiGe layers grown on silicon substrates, can substantially enhance mobility. The effective hole mass is also smaller in SiGe materials. Therefore, SiGe with high germanium content has been seen as an enabling material for high-speed p-channel MOSFETs. The two novel approaches to fabricating SiGe with high germanium content addressed in Chapter 5 offer an opportunity for achieving optimal performance in p-channel MOSFETs.

(b) Investigation of the effect of anisotropic strain on hole mobility

Recently, uniaxial strain in silicon has been reported to enhance hole mobility much higher than expected [1] and the enhancement was found to hold up at high vertical electric field, at which biaxial-strain induced enhancement usually diminishes [2]. These all suggest that anisotropy in strain has a much more favorable effect on hole transport than people have expected. Our unique ability to achieve orthorhombic strain and uniaxial stress, as discussed in Chapter 4, should enable one to investigate the influence of anisotropic strain on hole transport.

(c) Strain engineering in other material systems

The demonstration of a variety of strains in this work suggests broad applications of the manipulation of strain through lateral movements on a viscous layer. It can be scaled for systems of different sizes from this work. The thickness and viscosity of compliant viscous layers, along with geometry and size of the elastic films, are all readily tunable parameters for optimization of strain control. The underlying strain control mechanism, lateral displacement of strained films on substrates, is valid for any elastic films on viscous layers and can be extended to materials beyond Si and SiGe, such as III-V compound semiconductors, metal and insulators. For example, a nitride layer might replace the epitaxial SiGe film to serve as a stressor to generate strain in silicon films.

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Appendix A

Sharp Turn-on of Phosphorus Doping

In cases where the sharp turn-on of phosphorus doping profile is needed, the typical ramp rate of the phosphorus incorporation in silicon or SiGe is often not sufficient. Phosphorus tends to accumulate on the wafer surface before incorporating into the epi-layer when the phosphine (PH_3) source is turned on during the CVD growth at low temperature [1]. This is the limiting factor in the ramping of the doping level after PH_3 is switched on, not the rate of increase of the partial pressure of PH_3 in the growth chamber. The usual ramp rate of phosphorus observed in our reactor is 15 nm/dec.

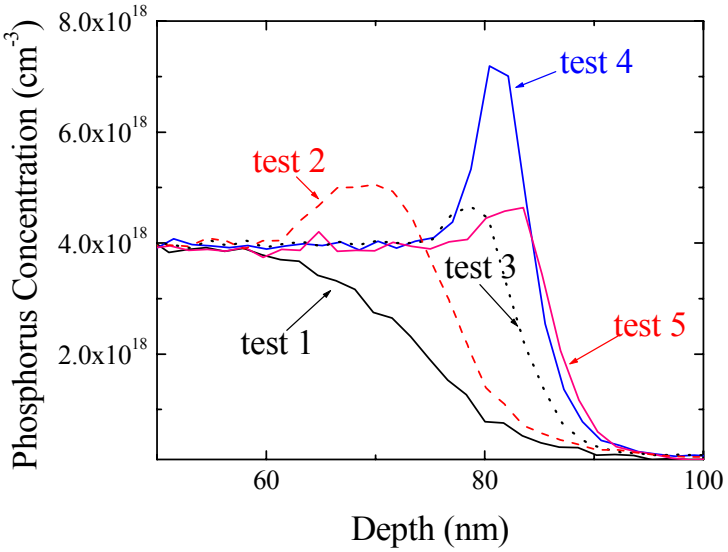
The key to increase the ramping rate of the doping is to rapidly saturate the wafer surface with phosphorus by exposing it to a high partial pressure of PH_3 in the growth chamber. One can modify the short period right after PH_3 is turned on in which the PH_3 flow rate can be much higher than its equilibrium flow rate needed for the desirable doping level and/or the silicon precursor (dichlorosiline in our case) can be reduced to lower the silicon growth.

A growth condition (T = 725^{o}C, PH_3(30 ppb) = 10 sccm and DCS = 26 sccm) was tested. The growth rate is 5 nm/min. The equilibrium doping level is 4 x 10^{18} cm^{-3}. The experimental results are summarized in the table below. With a regular growth sequence (DCS and PH_3 remained unchanged) (test 1), the phosphorus slope was slow (18 nm/decade). When the DCS flow rate was reduced to lower the growth rate for a period of five minutes after the PH_3 gas was turned on (tests 2 and 3), the phosphorus slope improved considerably (12.6 nm/dec for 5-sccm DCS and 8 nm/dec for zero DCS (i.e. five minutes with no growth)). A noticeable doping overshoot (~5 x 10^{18} cm^{-3}) occurred in the 5-min period because of a lower DCS flow. The 5-min period can be shortened to avoid the doping overshoot. In tests 4 and 5, both DCS and PH_3 flow rates were changed for only one minute after the PH_3 turn-on and the PH_3 flow rate was temporarily increased by eleven times. The phosphorus slope was the sharpest in all tests (7.5 nm/decade in test 4 and 6.4 nm/decade in test 5). The doping overshoot in test 4 is the

worse (7.1 x 10^{18} cm^{-3}). For both cases, a low growth rate leads to higher phosphorus incorporation and doping overshoot than a zero-growth rate.

In conclusion, the ramping rate of phosphorus can be greatly improved by reducing the flow rate of DCS while increasing the PH_3 flow rate in a short period after the PH_3 turn-on. Stopping the growth leads to less doping overshoot for the conditions tested than just reducing the growth rate.

Test#	Time (min)	DCS (sccm)	PH_3 (sccm)	Doping Overshoot	P slope nm/decade
1	0				18
2	5	5	10	$5.1x10^{18}$	12.6
3	5	0	10	$4.8x10^{18}$	8
4	1	5	110	$7.1x10^{18}$	7.5
5	1	0	110	$4.5x10^{18}$	6.4



Measured phosphorus levels for various tests by SIMS. The steady state growth condition after the transient period in the table was: T= 725°C, PH_3 = 10 sccm and DCS = 26 sccm. Before PH_3 was turned on, undoped silicon was grown at 725°C with 26-sccm DCS. All growth was done with 3-lpm hydrogen gas flowing at a chamber pressure of 6 torr.

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Appendix B

Various Recipes Used in This Work

1. Growth Conditions of SiGe with High Ge Fraction

Pressure = 6 torr

Flow rate of hydrogen carrier = 3 lpm

Ge Percentage	Growth Rate (nm/min)	Temperature(^{o}C)	DCS(sccm)	GeH_4(sccm) (0.8% in H_2)
52.5	19	550	10	500
58	28	625	5	500
60	3	500	10	500
68	5	500	5	500

2. Etch recipes

Tool	Gas (sccm)	Pressure	Power	Etch rate
PlasmaTherm 790	SF_6=25 O_2=6	150 mT	25W	SiGe > 100nm/min
PlasmaTherm 790	CF_4=25 H_2=4sccm	50 mT	200W	SiO_2=56nm/min

Appendix C

Measurement of Non-biaxial Strain by Raman Spectroscopy

The strain-induced shift of the Si-Si optical phonon frequency $\omega_{Si\text{-}Si}$ for Si and SiGe films can be generally expressed as [1]

$$\Delta\omega = \frac{\omega_0}{2}(p\varepsilon_{33} + q(\varepsilon_{11} + \varepsilon_{22})) \quad (1)$$

for Raman measurement on (100) surface in backscattering geometry. Here ω_0 refers to the phonon position for the strain-free case. Any shear strain is neglected. Here p and q are phonon deformation potentials and are equal to -1.45 and -1.95 respectively at room temperature for both silicon and germanium [2]. They describe the changes in the "spring constant" of the optical phonons with strain.

1. Uniaxial stress (Sec. 4.5)

In Sec. 4.5, long SiGe stripes were used to achieve uniaxial stress in the long direction of the stripes. Raman spectroscopy was employed to monitor the process. Since Eqns. 3.5 and 3.6 are only applicable to biaxial strain, the following analysis is carried out to interpret the shift of the phonon frequency observed during the process.

When a SiGe film is under a biaxial strain ($\varepsilon_{11} = \varepsilon_{22} = \varepsilon_0$) with no stress in the z direction, the strain in the z direction can be derived from Eqn. 2.2 to be

$$\varepsilon_{33} = -\frac{2c_{12}}{c_{11}}\varepsilon_0 . \quad (2)$$

When expressing ε_{11}, ε_{22}, and ε_{33} in terms of ε_0, Eqn. 1 becomes

$$\Delta\omega_{biaxial\_strain} = \omega_0(q - \frac{c_{12}}{c_{11}}p)\varepsilon_0 . \quad (3)$$

If the SiGe film is under a uniaxial stress along the [010] direction with a strain $\varepsilon_{22} = \varepsilon_0$ and there is no stress in the [100] and [001] directions, the strain in the [100] and [001] directions are equal:

$$\varepsilon_{11} = \varepsilon_{33} = -\frac{c_{12}}{c_{11}+c_{12}}\varepsilon_0 \qquad (4)$$

Then the strain-induced shift in the phonon frequency can be deduced from Eqn. 1 to be

$$\Delta\omega_{uniaxial\_stress} = \frac{\omega_0}{2}\left(q - \frac{c_{12}}{c_{11}+c_{12}}(p+q)\right)\varepsilon_0 \qquad (5)$$

Therefore, when the film with a biaxial strain ε_0 relaxes to a condition of a uniaxial stress in [010] with the same strain ε_0 in the [010] direction (as described in Sec. 4.5), the Si-Si phonon frequency would shift by

$$\Delta = \Delta\omega_{uniaxial\_stress} - \Delta\omega_{biaxial\_strain} = \omega_0 \frac{c_{11}+2c_{12}}{2(c_{11}+c_{12})}\left(\frac{c_{12}}{c_{11}}p - q\right)\varepsilon_0, \qquad (6)$$

After plugging the values of the elastic constants listed in Table 4.1 into Eq. 6 and using ω_0 = 510 cm^{-1} and ε_0 = 1.2% for $Si_{0.7}Ge_{0.3}$, one finds $\Delta\omega_{biaxial\_strain}$ = 8.5 cm^{-1}, $\Delta\omega_{uniaxial\_stress}$ = 3.1 cm^{-1} , and the shift Δ = 5.3 cm^{-1}. This shift Δ represents 64% of the difference between the biaxially strained and unstrained $Si_{0.7}Ge_{0.3}$. Note that the stress in the [100] direction relaxes to zero during the process. The stress is linearly proportional to the shift of the phonon frequency. This was used to infer the ratio of the stress in [010] to the original stress (Fig. 4.14(b)).

2. Orthorhombic strain (Sec. 4.6)

In Sec. 4.6, orthorhombic strain was generated in the silicon film using long SiGe/Si stripes in the [010] direction. Eqn. 6 does not apply since there is still stress in the [100] direction, caused by the stress balance between the silicon and SiGe films. Thus the films will have zero strain change in the [010] direction, but different strains in the [100] and [001] directions, and zero stress in the [001] directions. In the silicon film, with zero strain in [010], the strain along [001] can be expressed by the strain in [100] (Eqn. 4.17) as follows

$$\varepsilon_{33} = -\frac{c_{12}}{c_{11}}\varepsilon_{11}. \qquad (7)$$

Combining Eq. 7 and Eqn. 1, one can relate the shift of the phonon frequency in the silicon film from its unstrained state to the strained state in the [100] direction:

$$\Delta\omega_{orthor\,hom\,bic\_strain} = \frac{\omega_0}{2}(q - \frac{c_{12}}{c_{11}}p)\varepsilon_{11} = 361 * \varepsilon_{11}\ \text{cm}^{-1}, \qquad (8)$$

where the values listed in Table 4.1 for the silicon elastic constants and ω_0 = 520 cm^{-1} were used. This is half of the phonon frequency shift of a biaxially strained film with the same strain (Eqn. 3)

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Appendix D

Publications and Presentations Resulting from this Thesis

Referred Journal and Conference Papers

1. (Invited) J.C. Sturm, Haizhou Yin, R.L. Peterson, K.D. Hobart, and F.J. Kub, "Strain Engineering in SiGe/Si-on-Insulator Structures using Compliant Substrate and Stress Balance Approaches," ISTDM, 2004.

2. H. Yin, K.D. Hobart, S.R. Shieh, R. L. Peterson, T.S. Duffy, and J.C. Sturm, "Interference-enhanced Raman Scattering in Strain Characterization of Ultra-thin Strained SiGe and Si Films on Insulator," Mat. Res. Soc. Symp. Proc. **809**, pp. B3.6.1-B3.6.6 (2004).

3. R.L. Peterson, H. Yin, J.C. Sturm, "Island Scaling Effects on Photoluminescence of Strained SiGe/Si (100)", Mat. Res. Soc. Symp. Proc. **809**, pp. B8.4.1-B8.4.6 (2004).

4. H. Yin, K.D. Hobart, S.R. Shieh, T.S. Duffy, F.J. Kub, and J.C. Sturm, " High Ge content relaxed SiGe on compliant substrate by SiGe oxidation", Applied Physics Letter **84**,2624 (2004).

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15. X.Z. Bo, L. Rokhinson, H. Yin, D.C. Tsui and J.C. Sturm, "Si/SiGe Nanostructure fabricated by atomic force microscopy oxidation", MRS Symposium Proceedings, vol. **695**, L3.14, November 2001.

Book Chapters

1. J.C. Sturm and H. Yin, “Si/SiGe/Si heterojuction bipolar transistors”, book chapter in *Properties of Silicon Germanium and SiGe:Carbon*, London, United Kingdom, 2000.

Conference Presentations

1. R.L. Peterson, H. Yin, K.D. Hobart, T.S. Duffy, and J.C. Sturm, "Uniaxially-tensile strained ultra-thin silicon-on-insulator with up to 1.1% strain," EMC 46th Electronic Materials Conference, Notre Dame, IN, 2004.

2. (Invited) J.C. Sturm, H. Yin, R.L. Peterson, K.D. Hobart, and F.J. Kub, "Strain Engineering in SiGe/Si-on-Insulator Structures using Compliant Substrate and Stress Balance Approaches," ISTDM, 2004.

3. H. Yin, K.D. Hobart, S.R. Shieh, R. L. Peterson, T.S. Duffy, and J.C. Sturm, "Interference-enhanced Raman Scattering in Strain Characterization of Ultra-thin Strained SiGe and Si Films on Insulator," MRS Spring Meeting, San Francisco, CA, 2004.

4. R.L. Peterson, H. Yin, J.C. Sturm, "Island Scaling Effects on Photoluminescence of Strained SiGe/Si (100)", MRS Spring Meeting, San Francisco, CA, 2004.

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