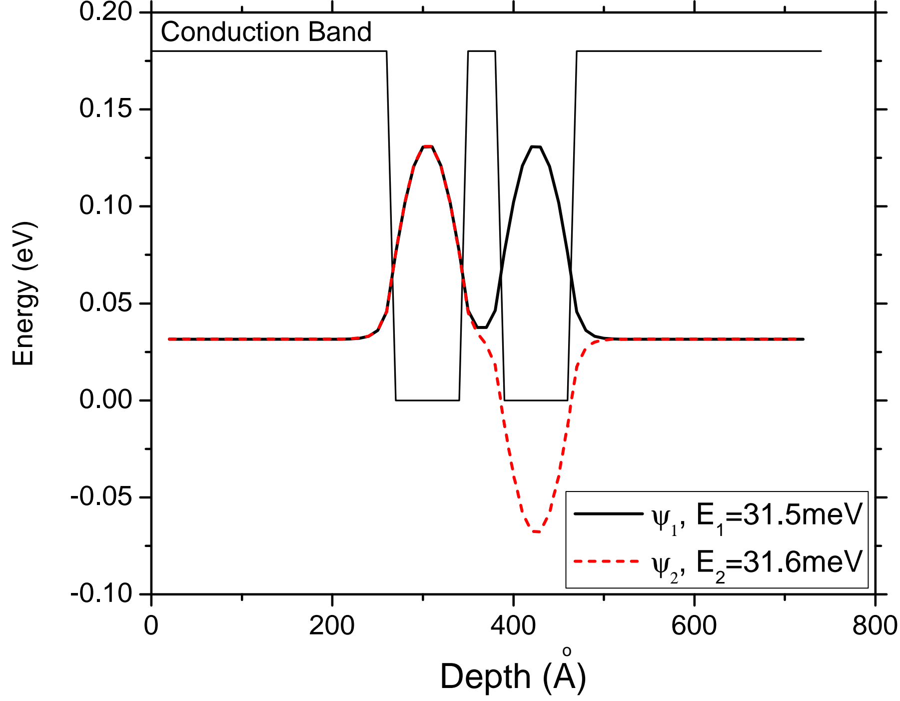


Figure 4.9: The conduction band edge and the electron wave functions of the lowest two quantized states in the symmetric double quantum well structures. The strained Si conduction band is at V = 0.

can be tuned by top-gating. However, the exact band alignment below the bottom well is very sensitive to the background impurities and substrate doping, making the accuracy of predetermination of density in the bottom well very poor. Since the structure is asymmetric, we cannot directly compute the symmetric anti-symmetric splitting as in the symmetric double well case. We expect the strength of subband interaction is similar to that in the symmetric double well given their similar quantum well width and same tunneling barrier thickness.

For the symmetric double quantum wells with two supply layers, our calculation shows the presence of symmetric and anti-symmetric pairs in the two-level system. The splitting Δ_{SAS} is a fraction of 1 meV which indicates a weak interaction, but it should also depend largely on the tunneling barrier thickness, doping level and

other growth parameters. The main drawback of the symmetric design is the tail of dopant out-diffusion and perhaps increased background impurities level from the bottom doping supply layer during the growth.

4.3 Characterization of the Double Quantum Well Systems

4.3.1 Growth of Si/SiGe Double Quantum Wells

We first attempted to grow an asymmetric double quantum well on our relaxed SiGe buffers. Sample #4692 has the same layer structures as shown previously in Fig. 4.4 (a) with an additional 4-nm thick silicon cap. Sample #4652 has a thicker SiGe barrier of 8 nm for SIMS analysis. The most critical technology issue is the abruptness and flatness of Si/SiGe/Si interfaces in the active DQW region. Since the barrier between the two strained silicon channels is only 4 nm or thinner, a growth rate of no more than 10 nm/min is desirable for improved abruptness and flatness.

Fig. 4.10 shows the Ge profile in sample #4652. The two thin silicon wells are clearly present. The Ge slope at all Si/SiGe interfaces is about 7% Ge per nm, which may be the SIMS limit. There are no fluctuations in oxygen and carbon profiles during these switchings. The rising end at the top surface is a pure SIMS effect.

Fig. 4.11 shows a cross section TEM image of the asymmetrical DQW sample. The clear contrast between the Si and SiGe layers demonstrates abrupt Si/SiGe interfaces with fluctuations on the order of a few Å. From the high resolution image (b) we also confirmed that the top quantum well is narrower than the bottom well. The thickness of both Si channels are about 2 nm less than the nominal values. Since the overall growth was mostly maintained at 625 °C for epitaxial SiGe, when the samples were heated to 700 °C or 750 °C for Si epitaxy, the temperature fluctuated for about

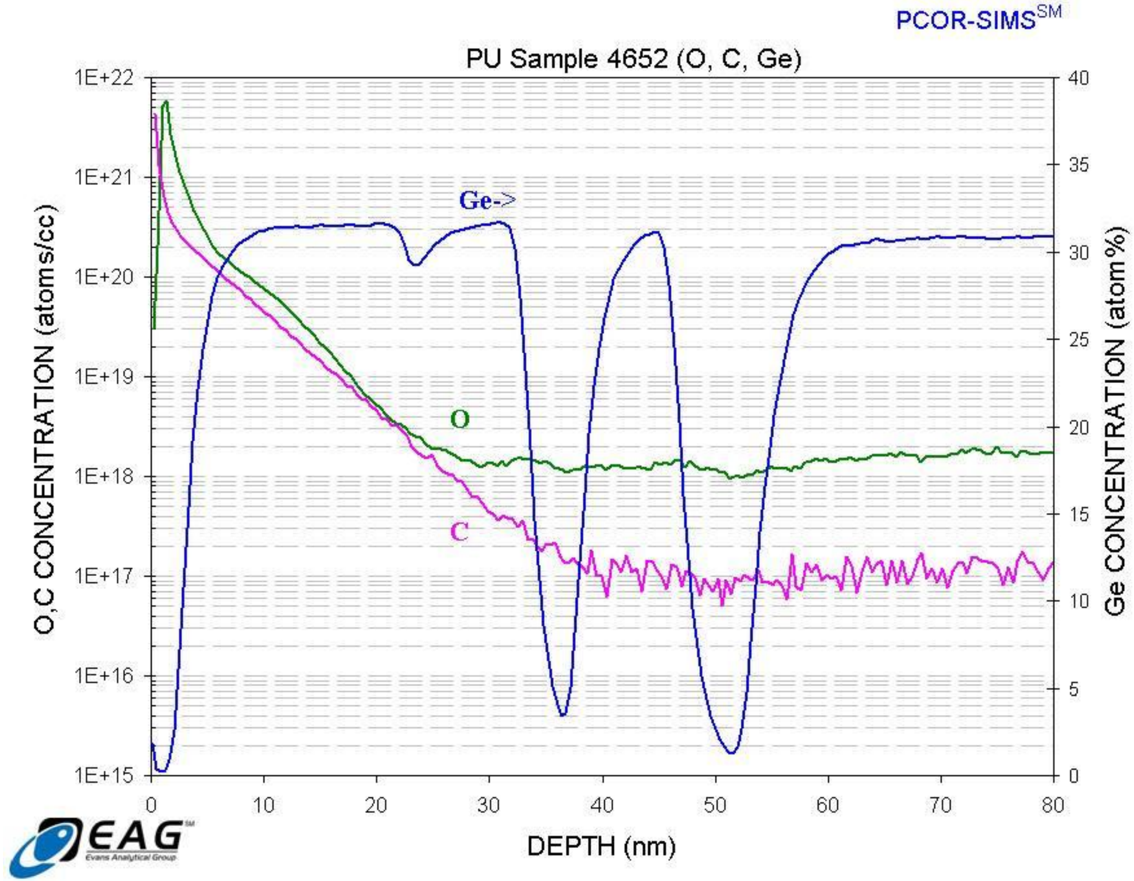
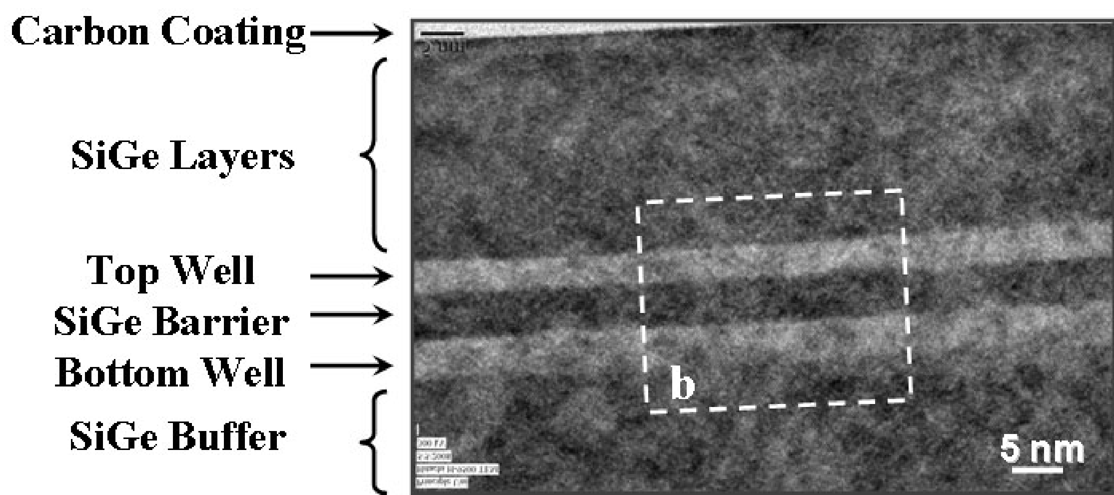


Figure 4.10: SIMS analysis of an asymmetric double quantum well structure with a 8nm barrier between the two wells.

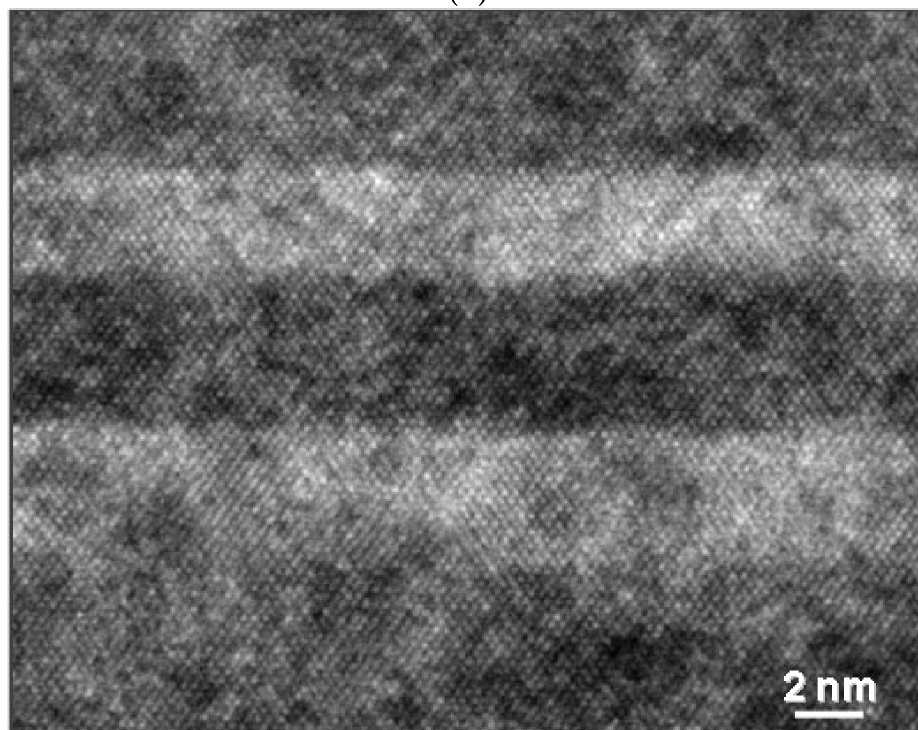
10 seconds when switching to these higher temperatures. This could cause a slower initial growth rate. Since the growth time was based on the steady-state growth rate of these layers, we naively did not allow for this transition time. We could take this into account in future growth design and compensate simply by increasing the growth time for thin silicon layers on top of SiGe.

4.3.2 Modulation of Si/SiGe Parallel Two-Dimensional Electron Gases

There are three types of experimental techniques that are commonly used to study the band structure and interactions between layers in double quantum wells. First a



(a)



(b)

Figure 4.11: (a) A cross section TEM image of an asymmetric double quantum well structure on $Si_{0.7}Ge_{0.3}$ relaxed buffers. (b) A high resolution TEM image showing the Si/SiGe/Si double quantum wells. The TEM was prepared by Dr. Nan Yao at Princeton and Hitachi laboratory, CA.

prominent negative transconductance was observed in the channel conductance characteristics due to resistance resonance [76, 77]. The second and also the most powerful tool is the Shubnikov-de Haas (SdH) oscillations originating from the sequential passage of Laudau levels through the Fermi level in external magnetic field. The intersubband transitions in DQW altered the SdH oscillations substantially and caused beating due to the mixing of the symmetric and anti-symmetric states [78, 79, 80]. A relatively new technique is to study the microwave induced absorption between the subbands. One recent example was interference oscillations of microwave photoresistance in GaAs/$Al_xGa_{1-x}As$/GaAs double quantum wells [81]. However, to the best of our knowledge, none of these effects were observed and reported in Si/SiGe systems.

The negative transconductance effect was observed in a Si/SiGe asymmetric double quantum well sample #4822. The sample has the same structure parameters as #4692 we described before, and an Al metal gate on top of 72-nm ALD Al_2O_3 was deposited for gating. The usual MOSFET structure with a Hall bar geometry was measured at T = 4.2 K and below. Both I-V and magneto-transport measurements were performed through collaboration with Professor Leonid Rokhinson's laboratory at Purdue University. The channel conductance G of the FET is shown in Fig. 4.12. A valley feature with negative transconductance is seen between $V_g = -2$ and –1 V.

In the following we will try to qualitatively explain these unusual characteristics. The measured conductance can be divided into three regions as labeled in the figure. In region I, G increases monotonously with V_g, which can be attributed to the increase of electron density in the bottom well. In this region no electrons were populated in the top well as shown in our previous theoretical calculations (see Fig. 4.5). In region III, G also increases which is mostly due to the increase of electron density in the top well, while the bottom well density remains roughly constant. In region II, G drops down from 1.28 to 1.22 mS, although the total electron density should continue to increase. In this region densities in both wells increase and the delocalized

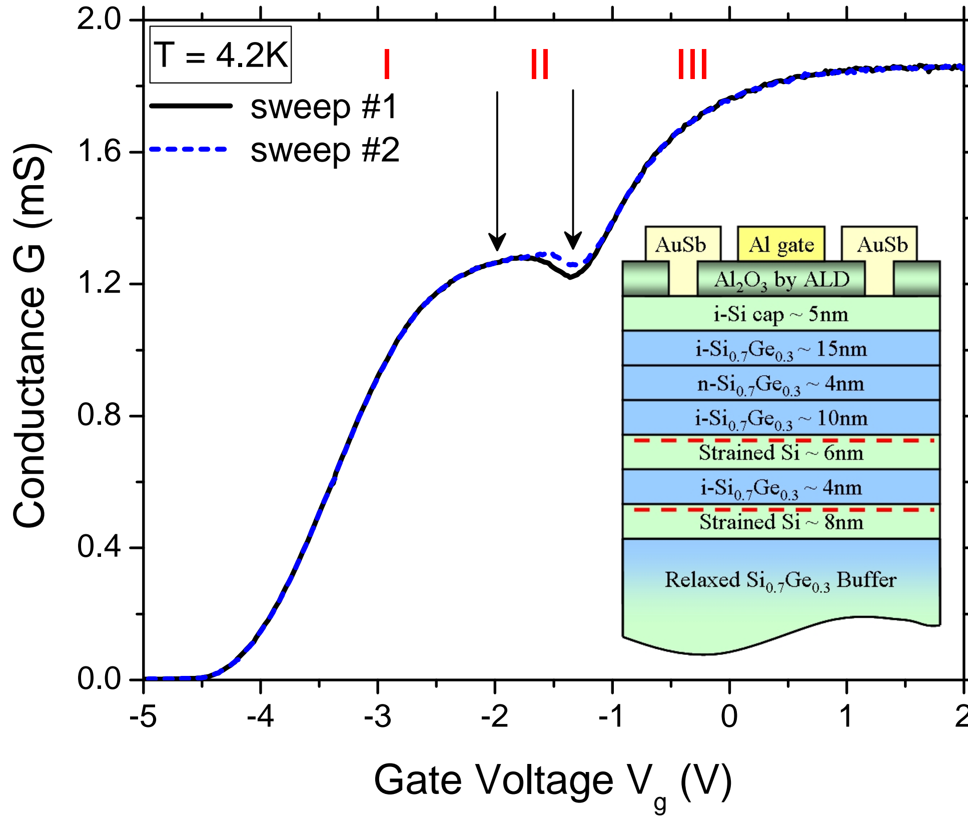


Figure 4.12: The sheet conductance measured as a function of gate voltage at T = 4.2 K.

electron wave functions interact strongly. The drop in G is influenced by the resonant coupling between two wells and the mobility modulation. The additional scattering from intersubband transitions and the alloy scattering from the thin SiGe barrier layer should decrease the 2DEG mobilities. The mobility reduction had a stronger effect on conductance than the increased total density, thus resulting in negative transconductance.

By a magnetic field dependent Hall measurement, we were able to extract the total electron density and mobility with varied gate voltage, as shown in Fig. 4.13. A substantial drop of mobility in the resonant coupling region II is clearly present. The

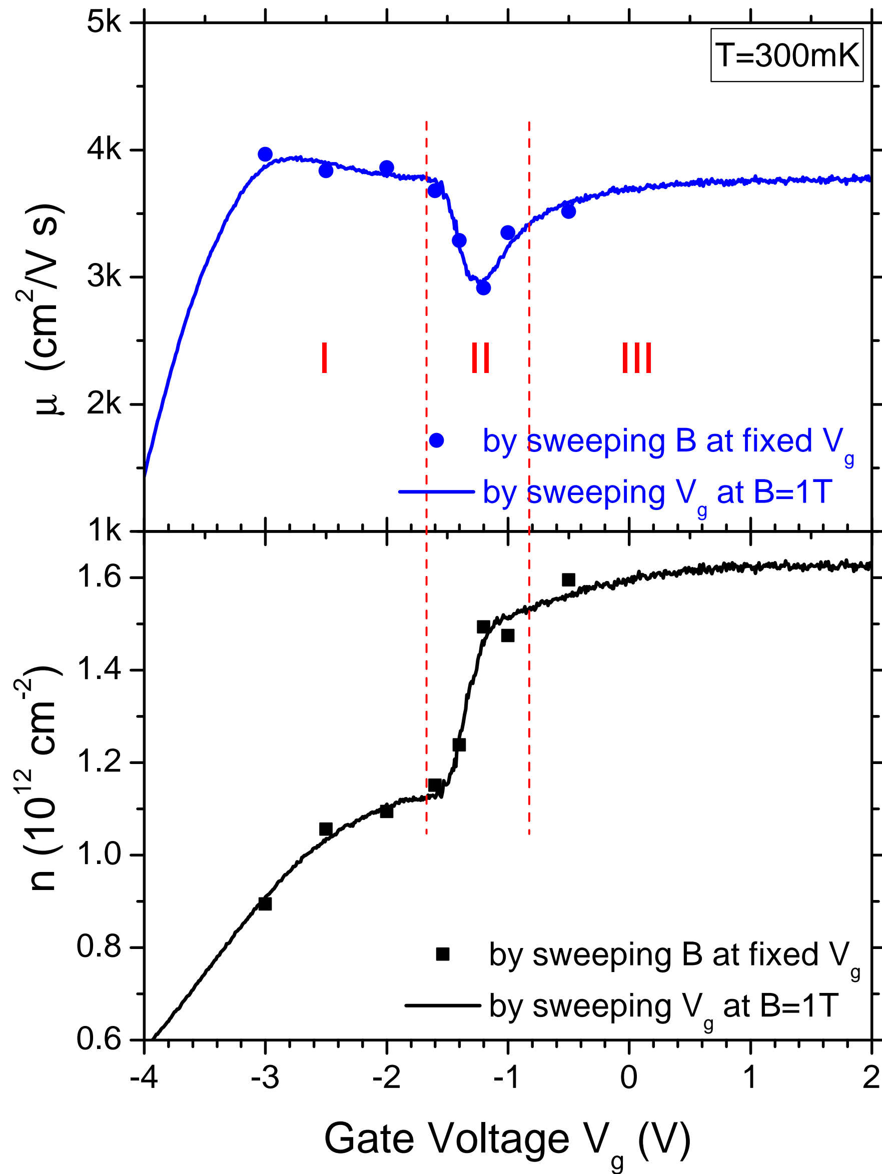


Figure 4.13: DQW 2DEG density and mobility vs. applied gate voltage at T = 300 mK. The data were extracted from Hall slope and sheet resistance by either sweeping the gate voltage at B = 1 T or sweeping the field at certain fixed gate voltages..

non-linear valley characteristics of mobility match the valley of channel conductance very well. In the same valley region we also found a sharp increase of the total electron density as a function of gate voltage. This could be explained by noting that with resonant tunneling, the two 2DEG's are coupled thus eliminating the capacitance associated with the interlayer barrier. This interlayer capacitance will manifest itself only when the two 2DEG's are decoupled. As a final note on the extracted mobility, the region III mobility is mostly due to the 2DEG confined in the bottom well, and both wells contribute to the measured mobility in region I. For the asymmetric DQW structure, the bottom well should yield a higher mobility since it has a larger effective set-back from the remote dopants. Our measurement suggests very little difference in the two mobilities, which again can be attributed to the background doping scattering as the limiting scattering mechanism for decoupled 2DEG's. On the other hand, the region II mobility can be used to evaluate the interlayer scattering strength.

Magneto-transport data were also taken at 300 mK with varied applied gate voltages, as shown in Fig. 4.14. We could not resolve any beating features in the SdH oscillations, only single oscillation period was found in FFT spectrum of ρ_{XX} magnetoresistance oscillations. We believe the missing of the SdH beating is due to the fact that the symmetric anti-symmetric splitting Δ_{SAS} in our sample could be much less than the Landau level broadening at these temperatures. We do not have direct calculation of Δ_{SAS} in asymmetric DQW structures. Our calculation for the symmetric case gives a Δ_{SAS} of 0.1 meV for a 4 nm barrier, which is rather small as our previously estimated Landau level broadening is $\Gamma \approx 0.46$ meV. No other experimental data were reported in Si/SiGe systems. We hope that a reduced background doping level and a thinner barrier would help to resolve the beating in future Si/SiGe DQW systems.

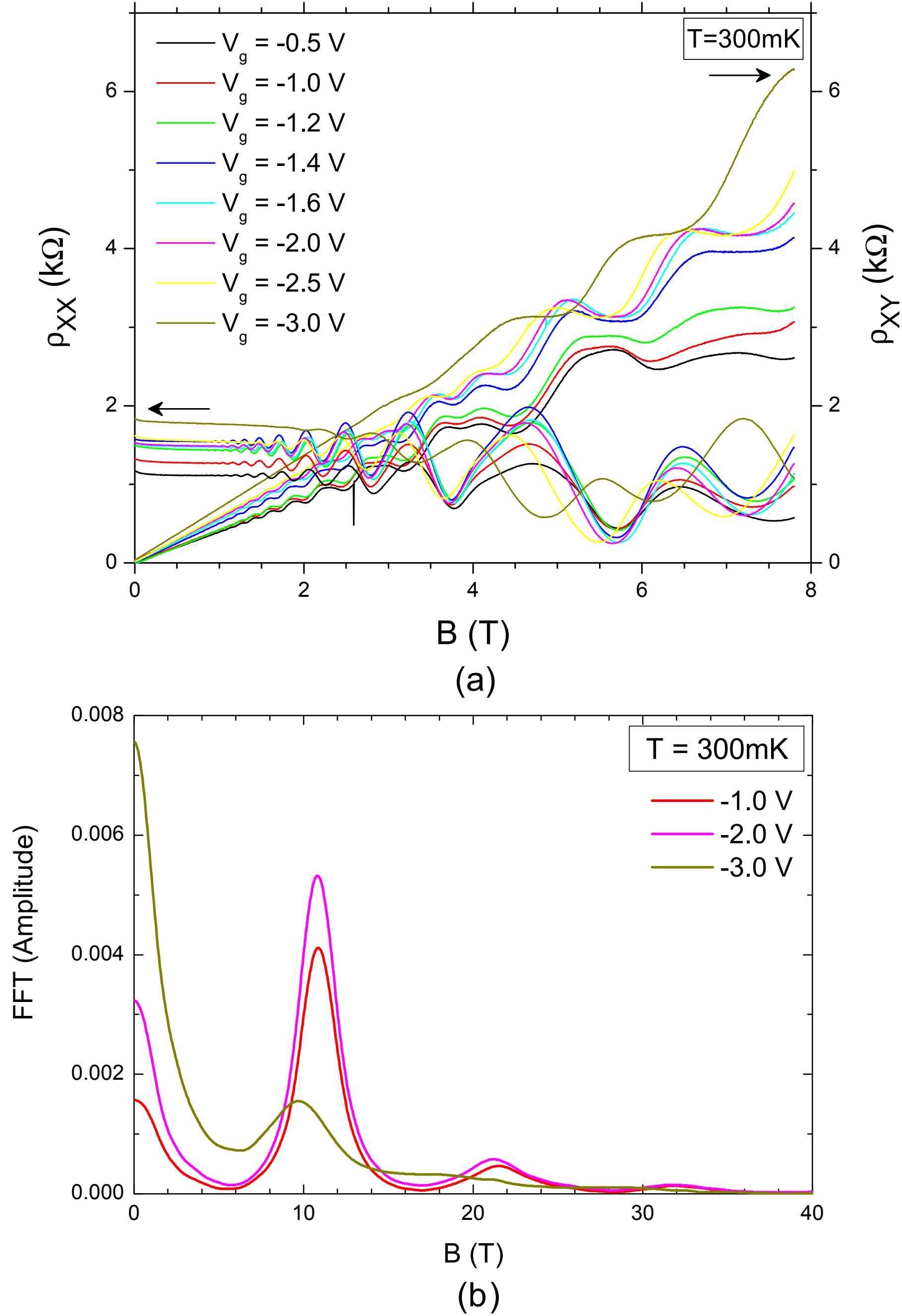


Figure 4.14: (a) Longitudinal resistance ρ_{XX} and Hall resistance ρ_{XY} vs. magnetic field at T = 300 mK, with an applied top gate voltage Vg from –0.5 to –3 V. (b) The Fourier spectrum of the longitudinal resistance at Vg = –1, –2 and –3 V.

4.4 Summary

This chapter is dedicated to the coupled double quantum well systems based on Si/SiGe heterostructures, a subject that has been extensively studied in III-V semiconductor systems but is relatively new in the Si-Ge field. Successful realization of Si/SiGe DQW systems can have a great impact on the study of many-body physics phenomenon such as electron interactions and intersubband transitions. Our emphasis of the potential applications of such DQW systems is on their role as quantum dimer for two-qubit exchange interactions in the Loss-DiVicenzo quantum computer proposal. The use of such quantum dimers allows a novel, simple "flying-qubit" architecture for silicon-based quantum computing.

Two types of DQW system designs were theoretically studied with self-consistent calculations of the Poisson and Schrödinger equations: asymmetric and symmetric double quantum wells. Conduction band alignment with different surface barrier height is calculated to determine electron density distribution in the two wells. The conditions at which the balancing of two wells can occur were obtained for both structures. For symmetric structures at balanced condition, the formation of symmetric and anti-symmetric states is shown with an energy gap $\Delta_{SAS} = 0.1$ meV. In reality, the symmetric structures are more difficult for growth control than the asymmetric structures due to the dopant out-diffusion from the bottom supply layer.

Asymmetric double quantum well growth on relaxed SiGe buffer was successfully demonstrated in the Princeton RTCVD system, with precise control of thin layer thickness and a high degree of interface abruptness and flatness. With ALD Al_2O_3 gate dielectric and top-gating, we successfully observed a negative transconductance effect in the asymmetric DQW structure as a result of resistance resonance for the first time in Si/SiGe. A substantial mobility drop is found over a region when electrons in two well delocalize and interact strongly. However, further magento-transport study of the sample did not reveal any beating of Shubnikov-de Haas oscillations. We

suggest a small energy gap Δ_{SAS}, which is less than the Landau level broadening with our sample growth and measurement conditions. Further improvement of the growth to enhance a stronger tunneling coupling between the parallel 2DEG's is needed to study the SdH beating effect.

Chapter 5

Fabrication Methods for Quantum Dot Applications

5.1 Introduction

With the improvements in techniques to relieve strain such as the relaxed buffer layers or silicon-on-insulator (SOI) substrates [82], SiGe layers grown on 300-mm-diameter scale have become available for use in research and development. Similarly, progress in the fabrication techniques for nano-device applications have seen many recent advances. The technological challenge for semiconductor quantum dot applications is to create structures as small as possible to increase the quantization energy and the charging energy of single electrons or holes. For example, it is well known that the quantization energy of electrons confined in a 1-D quantum well is inversely proportional to the square of the well width. Such devices usually require patterns with at least one lateral dimensional between the size of an individual atom and approximately a few hundred nanometers.

This work will focus on directly etching the semiconductor containing the quantum dot for side gating other than patterning a top gate to modulate the electrostatic

potential in the dot. Side gates were created in the same 2DEG layer by the same etch step that created the dot – a narrow trench separates the dot and the side gates, as shown in Fig. 5.1. In this process flow, the two most critical fabrication steps are nanolithography for defining the nanopatterns and etching for the pattern transfer. It is the purpose of this chapter to report on the development of fabrication methods that are relevant for quantum dot applications of this thesis.

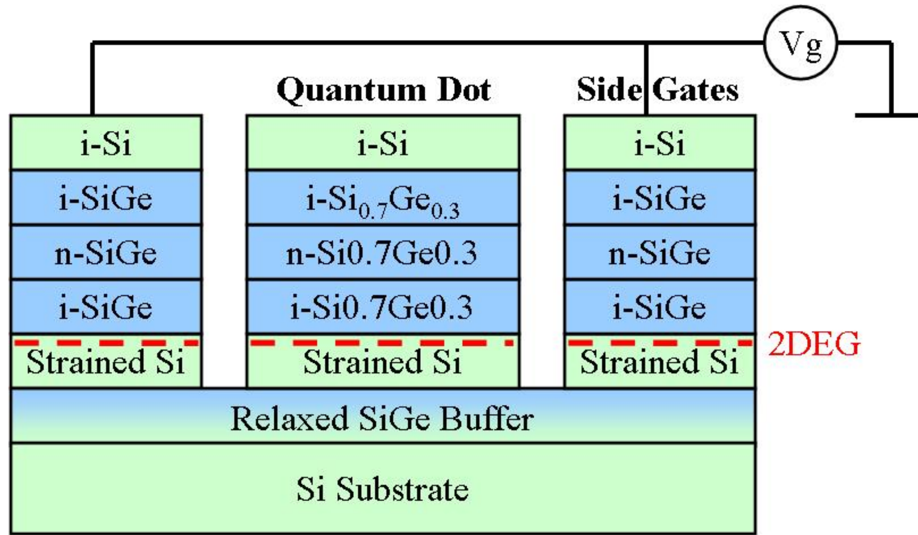


Figure 5.1: Schematic cross-section of side-gating structures for a 2DEG quantum dot.

The three popular nanolithography techniques seen in quantum dot applications are electron-beam (e-beam) lithography (EBL), scanning probe lithography (SPL) and nanoimprint lithography (NIL). EBL is the conventional nanolithography technique that is most commonly used. SPL such as atomic force microscope (AFM) lithography combined with wet etching is a novel low-energy process that can avoid radiation and etching damage thus can lead to better device surface/interface. Both EBL and AFM lithography are used in this thesis and will be discussed. NIL [83] is a promising scheme that allows high throughput and uniformity. It has two basic steps. First a mold with nanostructures on its surface is pressed into a thin resist on a substrate, followed by removal of the mold. The second step uses an anisotropic

etching process to transfer the pattern in to the entire resist.

Compared to other steps in growth and fabrication, the etching process has been a more mature technology with less new breakthrough advances. Selectivity and isotropy are considered as the two figures of merit. The two fundamental types of etchants are liquid-phase (wet) and plasma-phase (dry). Both wet and dry etching, as well as a mix of both, were used and investigated, and will be presented in this chapter.

5.2 Nanolithography Methods

5.2.1 Electron-Beam Lithography at Princeton

E-beam lithography, derived from the early scanning electron microscope (SEM), can be traced back as early as in the late 1960s. EBL is a direct-write technique that uses a beam of high-energy of electrons to produce a pattern in a resist - typically a common polymer such as PMMA (polymethyl methacrylate) [84]. The main attributes of EBL are [85]:

1. It is capable of very high resolution, almost to the level of a few nanometers.
2. It is a flexible technique that can work with a variety of materials and an almost infinite number of patterns.
3. It is slow, being one or more orders of magnitude slower than optical lithography.
4. It is expensive and complicated - EBL tools can cost many millions of dollars and require frequent service to stay properly maintained.

The e-beam lithography work in this thesis was all performed at Princeton in a Raith e_Line system and nanoengineering workstation by nanolithography specialist

Dr. Mikhail Gaevski. The Raith e_Line uses thermal field emission filament technology and a laser-interferometer controlled stage. It is also equipped with a load lock, an automatic height sensing, and a fixed beam moving stage (FBMS). The typical column voltage is 10 kV. A typical aperture of 30 μm is used to control the e-beam current.

Before the critical dimension nanopatterns are written by nanolithography, an optical lithography step is employed to define large design features on the wafer such as contact pads and alignment marks. Fig. 5.2 shows the design view of the two active device geometries in L-Edit, Tanner EDA. In Fig. 5.2 (a) the core structure is a Hall bar, which is commonly used for quantum point contact fabrication or cutting through a conducting path for a leakage test across a gap. Fig. 5.2 (b) uses a square island with multiple contact leads which can be implemented for a variety quantum dot applications. Both active regions are small enough to fit in one writing field (typically 50$\times$50 μm) to avoid stitching error caused by moving the stage in EBL. The placement and separation of contact leads can also allow relaxed alignment tolerance ($\sim$ a few hundred nm) for EBL. Both layouts share the same four alignment marks for subsequent e-beam writing.

A key in successful EBL is the choice of proper resist. It is remarkable that even today much work continues to be done with PMMA resist on converted SEMs. 950k PMMA 4% diluted in chlorobenzene is the standard resist. In this work we also used an alternative resist of ZEP-520, which has better dry etching resistance compared to conventional PMMA. The ZEP-520 was coated to the sample by 40-sec spin-on at 4000 rpm. The sample is then post-baked at 180 °C for 10 minutes. For the e-beam writing in Raith, a typical area dose of 35 μC/cm^2 is used. After the e-beam exposure and development of the nanopatterns using developer ZED-N50, the ZEP-520 resist is hard baked at 130 °C for 3 minutes on a hot plate. Then the patterns are etched in the substrate by either wet-chemical etching or RIE. After etching the resist is removed

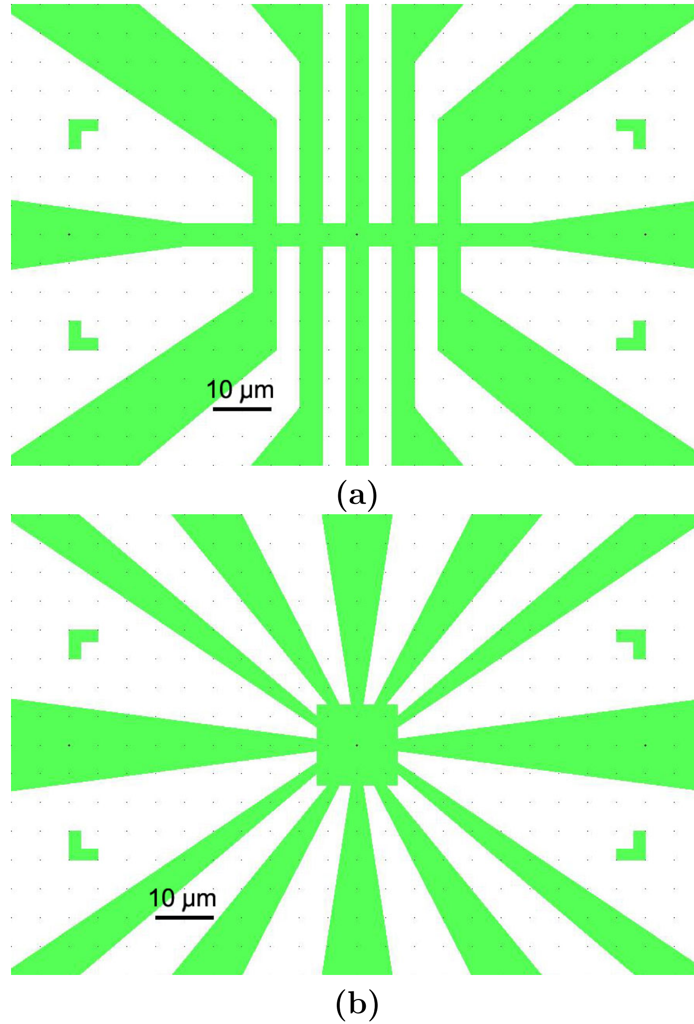


Figure 5.2: Design view of optical photolithography masks with alignment marks for (a) a Hall bar geometry for e-beam patterning of multiple quantum point contacts or gaps for leakage tests; (b) a symmetric square island geometry for complex quantum dot structures. The mask is designed in L-Edit, Tanner EDA.

by ZDMAC remover, and a solvent clean (acetone/isopropyl alcohol). Finally an optional UV/ozone clean in a UVOCS cleaner can be used to remove residual e-beam resist [86].

The feature size and surface cleanliness of the final nanopatterns will depend on the choice of etching process after the resist development, and will be discussed in the next Section 5.3.

5.2.2 PFOTS-aided AFM Lithography

The scanning probe microscopy (SPM) field began with the invention of the scanning tunneling microscope (STM) [87, 88] in 1981. It has enabled the researchers to image the world at the atomic scale. Among the many established types of SPM, atomic force microscopy (AFM) [89] is one of the foremost methods for imaging, measuring and manipulating matter at the nanoscale. With the discovery of AFM anodic oxidation, AFM lithography demonstrated a powerful tool to pattern a H-passivated Si (100) surface down to 10 - 30 nm size [90].

At Princeton we developed AFM lithography based on a Digital Instruments (DI) Dimension 3100 AFM. Three functionalities are added to the microscope to enable lithography, as shown in Fig.5.3:

1. The "nanoman" software package from DI which provides the flexible, yet accurate control of the in-plane position and movement of the AFM tips.

2. The Signal Access Modules (SAM) in-line hardware accessories that can apply a DC-voltage to the AFM tip during the local anodic oxidation.

3. A home-made humidity-controlled chamber environment which supplies water-vapor as the electrolyte for anodic oxidation.

AFM lithography can be used to pattern Si (or SiGe) by anodic oxidation of silicon under the tip with applied negative voltage. Because the oxide thickness is limited to $\sim$ 4 nm, only about 2-nm silicon can be oxidized [92]. To pattern thicker SiGe layers, a two-step wet etching can be used as shown in Fig. 5.4. A thin silicon cap on top of the SiGe is first oxidized by AFM, then with a dilute HF dip to remove the oxide, followed by a selective wet etching (CH_3COOH:H_2O_2:HF = 1:2:3) [93] to transfer the pattern into underlying SiGe. This is difficult to control in practice since the thin silicon is not a perfect barrier for the selective etching. This limitation is overcome by

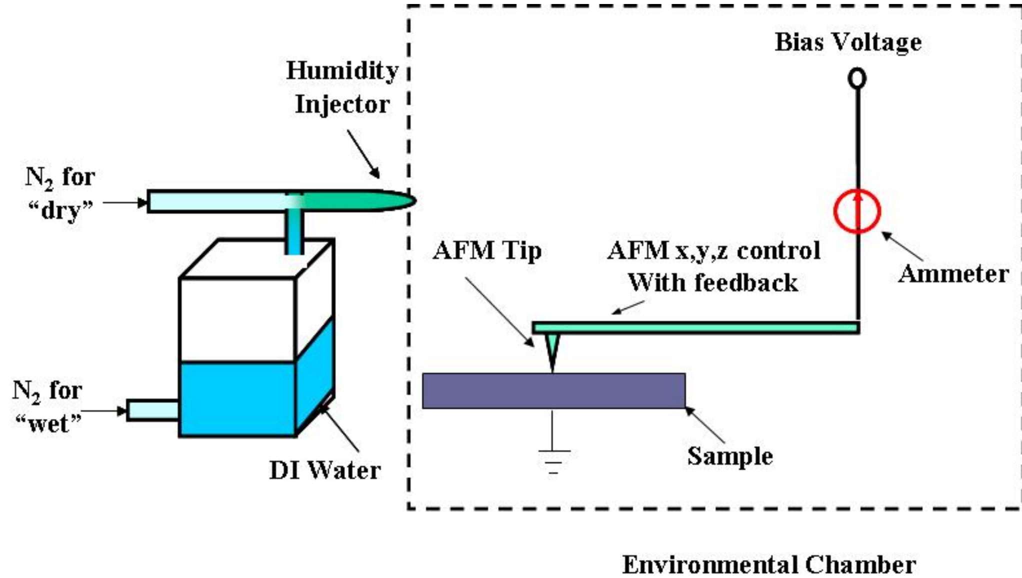


Figure 5.3: The instrument setup for AFM lithography [91].

adding a self-assembled monolayer perfluorooctyl trichlorosilane (PFOTS) [94] before AFM oxidation as an etch resist to improve the uniformity and repeatability.

Since only a 2-nm silicon surface layer will be oxidized by AFM oxidation, ultra-smooth PFOTS monolayers need to be obtained before the AFM lithography. We first removed native oxide on silicon substrates by an HF dip. Then the silicon substrates were heated in a 1:3 solution of H_2O_2 and H_2SO_4 at 80 °C for 30 minutes, to provide a smooth oxide surface for the PFOTS film growth. This acid treatment was followed by an extensive DI water rinse and nitrogen blow dry. For growth, the substrates were immersed at room temperature in a 1 mM solution of PFOTS in dodecane for 3 hours in a nitrogen glove box environment with minimal exposure to the ambient. The long immersion time can ensure a complete monolayer formation [94]. After growth of the self-assembled monolayers, the surface roughness was measured by AFM to be 1.8 Å. The monolayer thickness is estimated to be $\sim$ 2.6 nm.

AFM lithography was then performed on PFOTS-coated substrates at room temperature in tapping mode. The relative humidity was kept at $\sim$ 40% by bubbling nitrogen through water into an environmental chamber surrounding the scanning tip.

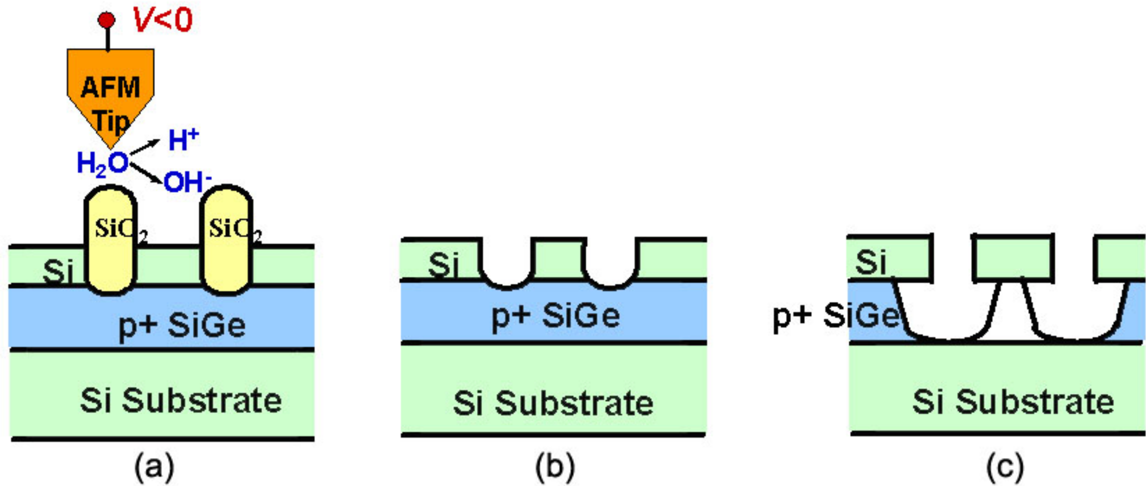


Figure 5.4: Process of nanopatterning Si/SiGe layers with AFM lithography and two-step wet etching: (a) AFM local oxidation, (b) Remove oxide by HF, (c) SiGe selective wet etching.

By applying a negative bias (~ -20 V) to the tip at a scanning speed of 0.4 μm/s, a 2-nm silicon surface layer underlying the PFOTS is locally oxidized. Oxide linewidths well under 100 nm can be achieved. By a dilute HF dip and a selective SiGe wet etching (HF:H_2O_2:CH_3COOH = 1:2:3), the pattern is transferred to the underlying SiGe layer and stops at the silicon layer. Fig. 5.5 shows the complete process. The FWHM of the SiGe linewidth is on the order of 100 nm, which is comparable to the resolution of AFM lithography without PFOTS. High-resolution can be achieved by optimizing the bias voltage and writing speed [95].

Compared with the previous direct AFM lithography of Si/SiGe layers, the use of PFOTS monolayers as an etch resist greatly improved the pattern transfer uniformity and repeatability. When only the thin silicon cap layer itself was used as the selective etch barrier, the pattern transfer from AFM oxidation by wet etching were very non-reproducible, and the etch was limited to a short time ($\sim$ 20 seconds). An increased surface roughness after the wet etch was also observed. With this additional PFOTS film as a resist, now the selective etch can be several minutes long, so now thicker SiGe layers with lower Ge content can be patterned with far improved uniformity

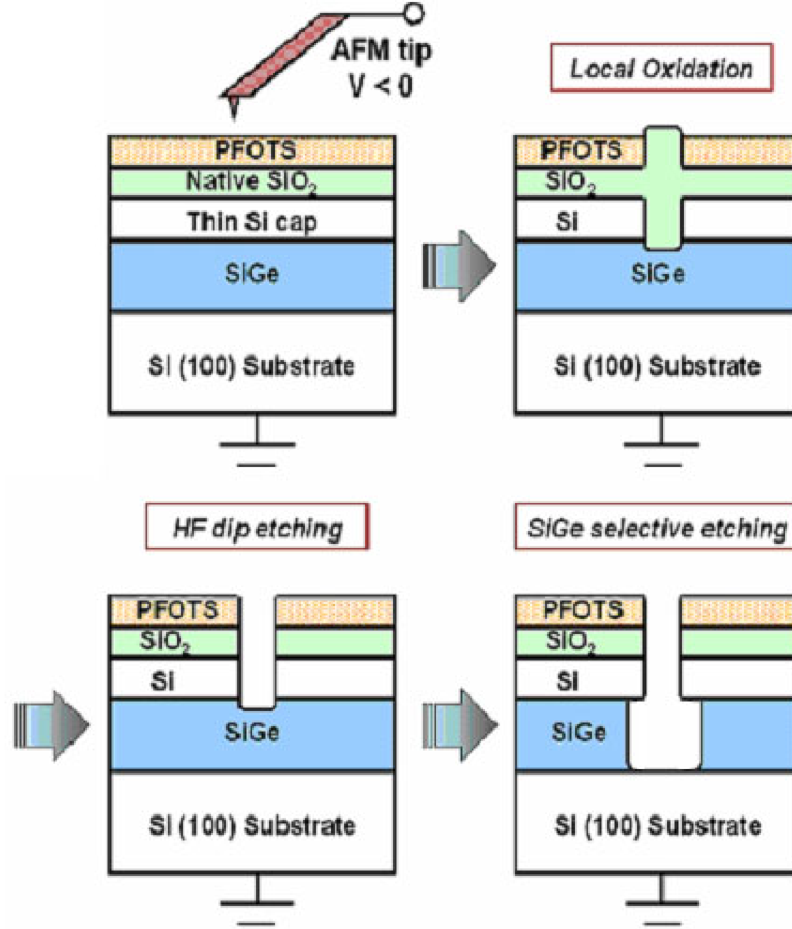


Figure 5.5: Process of PFOTS-aided AFM lithography. PFOTS is deposited on native oxide (for bonding) to prevent etching through 2-nm silicon surface layer during SiGe patterning for improved uniformity. The two-step etching process is used to pattern SiGe thicker than $\sim$ 2 nm.

than without PFOTS. Fig. 5.6 shows a comparison of the etching profile without and with the additional PFOTS. When etching time is 40 seconds or longer, undesirable pinholes were found on the silicon surface without PFOTS.

As a demonstration of AFM lithography with PFOTS of Si/SiGe nanostructures for quantum device application, we first grew a 2-D hole gas in compressively strained $Si_{0.7}Ge_{0.3}$ channel with a $Si_{0.9}Ge_{0.1}$ supply layer in sample #3716. The mobility and hole density are 1300 cm^2/Vs and 6×10^{11} cm^{-2} at T = 4.2 K. A Hall bar mesa was fabricated on the 2DHG. Then we cut a line through the Hall bar as shown in Fig. 5.7. Ohmic contacts are made to the 2DHG by lift-off of aluminum and subsequent

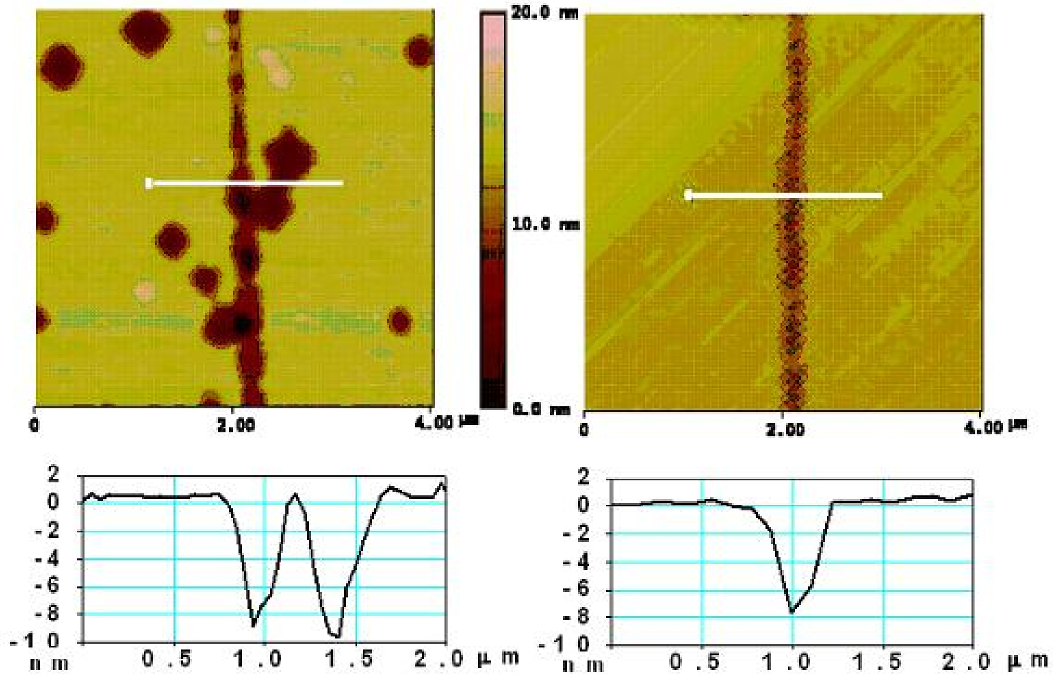


Figure 5.6: Surface image and profile along the labeled white line for a Si/SiGe pattern with (right) and without (left) PFOTS as a resist, the HF dip to remove silicon oxide and the SiGe selective wet etch for $\sim$ 40 sec.

annealing at 450 °C for 10 minutes. The two-terminal resistance after the line cutting was raised from 300 kΩ without cutting to larger than 10 GΩ. This shows the 2-D carriers are localized by nano-patterning of the 2DHG.

As one final comment on the PFOTS-aided AFM lithography, the use of PFOTS or other organic polymers as resist can also enable a much wider range of wet etching chemical selections. For example, PFOTS is an excellent mask against the HF/HNO_3/dilute system, the most popular etchant for isotropic silicon wet etching, which would be otherwise incompatible with the direct AFM lithography that uses either a thin Si-cap or SiO_2 as an etch mask. It makes AFM lithography a more convenient and versatile technique that can pattern complex Si/SiGe structures with a surface that can be locally oxidized by AFM.

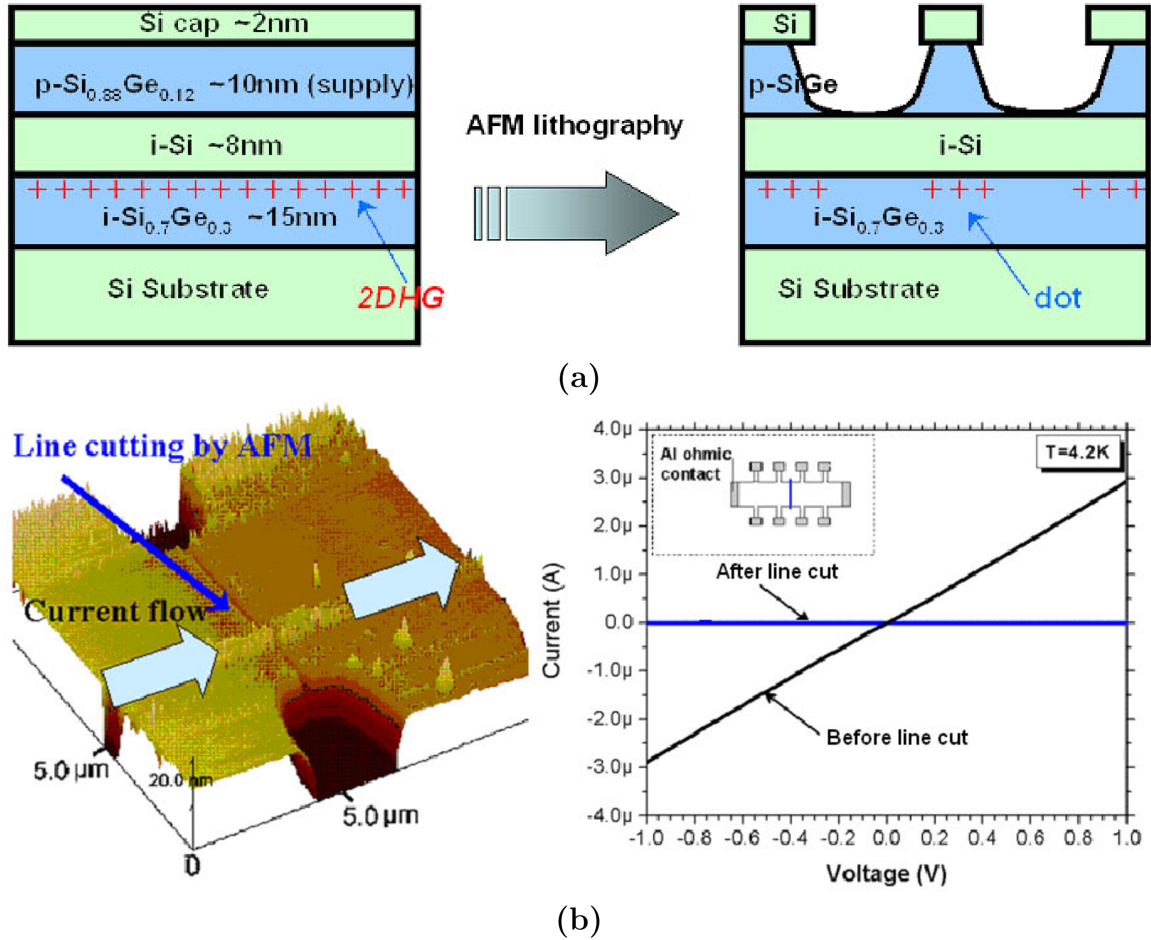


Figure 5.7: (a) Schematic structures of the 2-D hole gas structure with $Si_{0.9}Ge_{0.1}$ supply layer for patterning by AFM lithography; (b) AFM image and I-V curve of Hall showing conducting path cut by PFOTS-aided AFM lithography of supply layer and increased resistance at 4.2 K after the cut.

5.2.3 Comparison of Nanolithography Methods

As a comparison of e-beam lithography and AFM lithography, we list both methods' advantages and drawbacks.

E-beam lithography is the most mature technique. It offers the highest throughput and fastest writing speed. Both lithography hardware packages and simulation/design softwares are commercially available and meet the industry standards. The main drawback for quantum dot applications is the lack of convenience due to the complexity of the system. The irradiation from the higher-energy electron beams may

also cause an undesirable charging effects [96]. Proximity effects due to electron scattering is also well known to limit the ultimate feature resolution [97]. However, at present most quantum dot applications do not require lines and spaces below 20 nm.

In comparison, AFM is a much more convenient tool than SEM as it can operate perfectly in ambient and does not require high voltage. It can completely avoid radiation and charging effects. In addition, AFM as an imaging tool can produce a true 3-D surface profile with higher resolution, while it is difficult to obtain height information of the surface topology with SEM.

One disadvantage of AFM lithography is the low throughput. There are several reasons for this in practice. First the technique is very surface-sensitive and the reproducibility is poor especially for more complex patterns. Second, there has been plenty of work showing 0-D dots and 1-D lines at nanoscale but few for larger features, for example, a 2-D square box consisting of many AFM scan lines can be very slow and requires a lot of calibration efforts. Third, the conventional AFM tips suffer from rapid wear which degrades the quality of the AFM local anodic oxidation. Another inconvenience of AFM lithography is that only wet etching can be used for pattern transfer because the SiO_2 and PFOTS are too thin to serve as a dry etch mask. The reliance on wet etching not only increases the minimum feature size due to undercut from isotropic etching, it also limits the materials and layer structures that can be etched.

Both e-beam lithography and AFM lithography can produce nanopatterns with about 50 nm minimum linewidth for our modulation-doped Si/SiGe heterostrutures. Because of difficulty with reproducibility and linewidth control with our early work in AFM lithography, even with PFOTS, the installation of the Raith e_Line system at Princeton, and the ability to use anisotropic RIE, the quantum dot devices discussed in this thesis will be mostly based upon e-beam lithography.

5.3 Etching Methods

5.3.1 Wet Etching of Si and SiGe

Wet etching is an etching method where the material is dissolved in a wet chemical solution. It is the simplest etching technology. In particular for Si, three types of wet chemicals are commonly used: HF/HNO_3 solution, potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH) solution, and HF/H_2O_2/CH_3COOH mixtures for etching SiGe.

HF/HNO_3 diluted in H_2O or CH_3COOH is the most popular isotropic wet etch of silicon. Various compositions give different etch rates, since the activation energy of the etching process is different in the different composition regions [98]. Composition in the high-HNO_3 region is generally preferred due to lab safety concerns. The typical etch rate of Si is very fast, about 100 nm/min for a composition such as HF:HNO_3:H_2O = 1:5:10. The solution etches SiGe much faster than Si, making it very hard to control the etch thickness in Si/SiGe multi-layer structures. The HF/HNO_3 solution is well suited for making big mesas where precise control of the etch stop is not required, for example, a Hall bar mesa defined by optical lithography for Hall measurement. It is also applied in the semiconductor industry for the removal of contamination and lattice defects generated by the lapping of Si wafers.

The other group of commonly-used silicon etchants is alkali metal hydroxides or quaternary ammonium hydroxides based, such as KOH and TMAH solutions. Both solutions are non-flammable, and TMAH is gaining more popularity because it contains no alkali metal ions and hence is CMOS compatible. The etching characteristics are very different from the HF/HNO_3 wet etching. First, KOH and TMAH etch Si anisotropically, meaning that the etch rate is dependent on the crystallographic directions. The most slowly etched planes are the {111} planes. The {100}, {110}, and all other high-index planes are etched much faster. For this reason, the etched cavities

are bounded between {111} planes, resulting in the shape of V-grooves, truncated or full pyramids on regular (100) wafers. Second, unlike the acid-based solutions or KOH, TMAH does not not attack SiO_2 and therefore offers more selectivity. Moreover, recent studies showed that TMAH etching is also selective with respect to SiGe, which can be very useful for nanopatterning Si/SiGe by all selective wet-chemical etching [99]. The reported TMAH etch rates correspond to selectivities of 20:1 for $Si_{0.76}Ge_{0.24}$ and better than 4200:1 for SiO_2.

In our set-up, the anisotropic Si wet etching was performed in an aqueous solution of TMAH (25 weight %) at 120 °C. The etch rate on Si (100) substrate is extremely fast (on the order of μm/min). For SiGe with 30% Ge content, the etch rate is found to be less than a few nm/min.

Much work exists on wet etching of pure Si. With the rapidly growing field of SiGe technology, the properties of wet-chemical etchants targeting SiGe were also investigated. Selective SiGe etching with respect to Si has been done by acidic solutions such as $HF/H_2O_2/CH_3COOH$ [93]. The etch rate has been found to depend strongly on Ge content. For $Si_{0.7}Ge_{0.3}$ etched in $HF:H_2O_2:CH_3COOH = 1:2:3$ solution, the etch rate is about 40 nm/min at room temperature and corresponds to a selectivity of 400 over Si. Fig. 5.8 shows the etch selectivity as a function of Ge content. Reasonable selectivity can be achieved for SiGe vs. Si with more than 20% Ge.

To compare all the above wet etching methods for Si/SiGe heterostructures, Table 5.1 shows their properties with regard to the isotropy and selectivity on different materials.

Table 5.1: Common properties of Si/SiGe wet-chemical etchants on planar substrates.

	Isotropy	Selectivity (target material)		
Solution		Si	SiGe ($\geq$ 20% Ge)	SiO_2
HF/HNO_3	isotropic	yes	yes, much faster	yes
KOH (heated)	anisotropic	yes	no	yes, much slower
TMAH (heated)	anisotropic	yes	no	no
$HF/H_2O_2/CH_3COOH$	isotropic	no	yes	yes

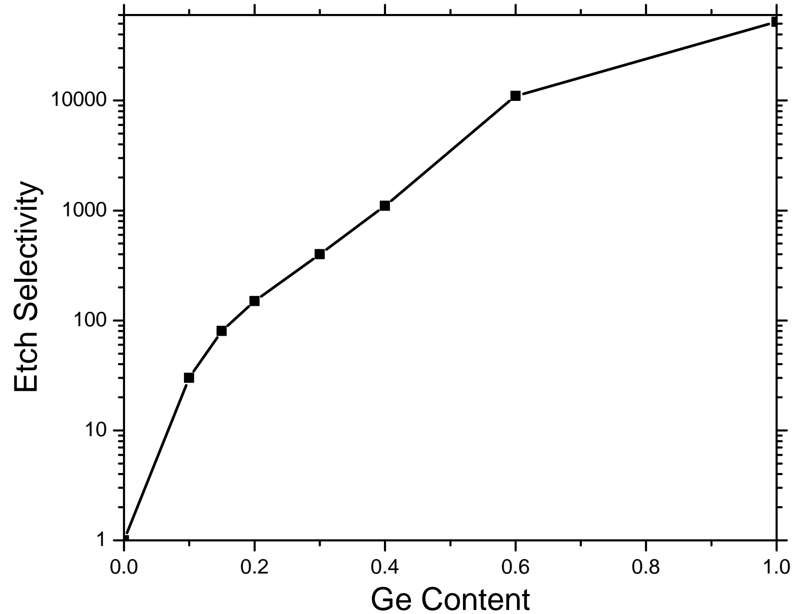


Figure 5.8: Etch selectivity vs. Ge content with respect to Si for p-type SiGe etched in HF:H_2O_2:CH_3COOH = 1:2:3. The etch rate data are obtained from [93].

The two-step wet etching process (SiO_2 etch and SiGe etch) can be combined and used as a low-damage fabrication technique for lateral nanopatterning of Si/SiGe heterostrutures. In fact, our first quantum point contact (QPC) type of nanodevice in Si/$Si_{0.7}Ge_{0.3}$ 2DEG was made by e-beam lithography and selective wet etch (see Chapter 7 for more details).

Fig. 5.9 shows the process and cross-sectional view of device fabrication after etch lithographic and etching steps. The 2DEG surface was first treated in H_2O_2/H_2SO_4 acid to form native oxide as an extra TMAH-resistant mask for better selectivity. High resolution QPC lithography was achieved by using a thin layer of 950K PMMA and e-beam exposure. Then both the thin oxide and Si cap in open paths were etched by a brief RIE. Wet etch could also be used here, for example, HF and TMAH dips. But RIE is the preferred method as it can also provide descumming of the positive PMMA resist in the exposed regions. The lithographically defined patterns

were first transferred into the SiGe supply and spacer layers by $HF/H_2O_2/CH_3COOH$ wet etching for about 20 seconds. The isotropic etch will result in an undercut of about 70% of the etch depth, and will stop at top of the Si channel. Finally the Si channel is also selectively removed by TMAH wet etching for about 10 seconds. Both SiO_2 and/or SiGe are excellent masks for TMAH etching even if the thin PMMA was stripped in previous etching steps.

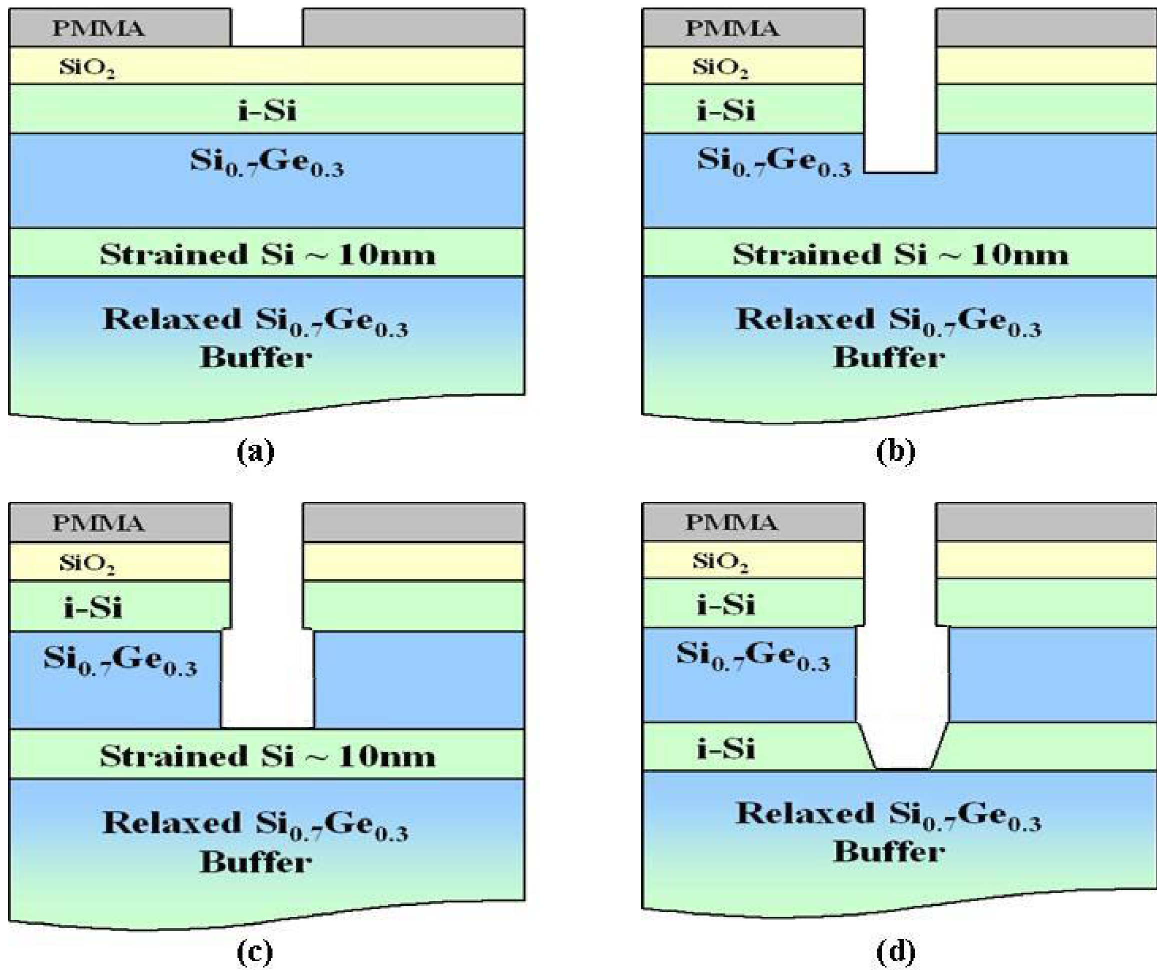


Figure 5.9: Process of QPC in Si/SiGe heterostructure 2DEG fabricated by e-beam lithography and selective wet-etching. (a) E-beam lithography and development of PMMA; (b) a shallow RIE to remove SiO_2 and Si; (c) SiGe wet etch; (d) Si wet etch.

Fig. 5.10 shows the SEM image of Si/SiGe QPC after all etching steps and the removal of PMMA resist. The micrograph was taken by the same SEM in the Raith e_Line system that is used for e-beam lithography. The narrowest gap between the

lateral gate and the central electron channel is about 200 nm wide. No significant undercut was observed in the active QPC region defined by e-beam lithography. The surface of area which was only etched by wet chemicals appears to be smoother than the surface surrounding the Hall bar mesa which was fabricated by optical lithography and RIE.

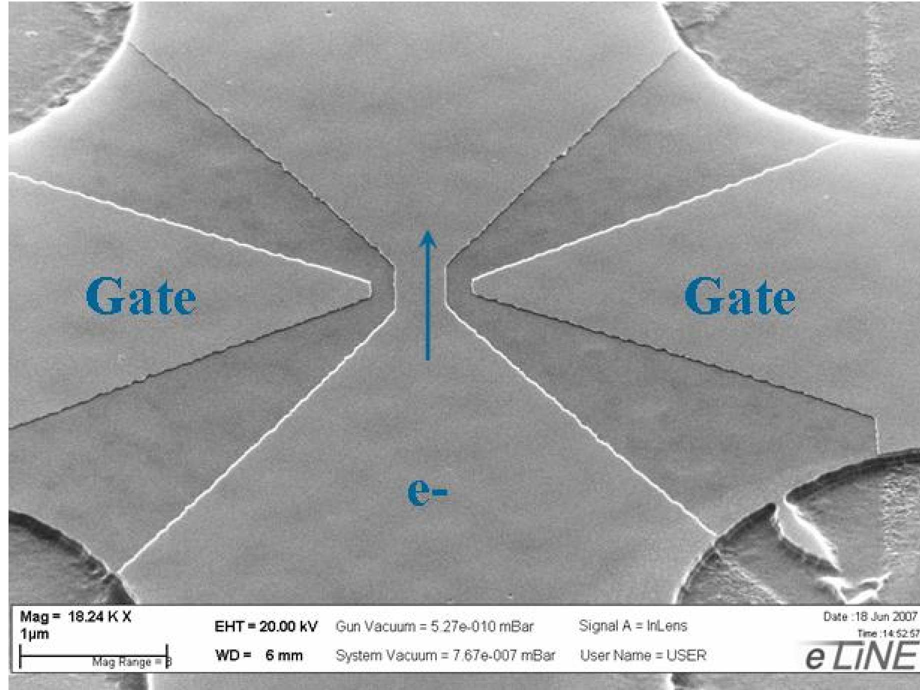


Figure 5.10: A SEM image of Si/SiGe QPC after all etching steps and the removal of PMMA resist.

After the QPC nanopatterns were created by e-beam lithography and selective wet etching, the whole sample surface was then passivated by Si/SiGe epitaxial regrowth for better surface/interface control, which will be the main topic in the next chapter. The final QPC device characteristics will be discussed in detail as part of Chapter 7 of this thesis.

5.3.2 Dry Etching of Si and SiGe

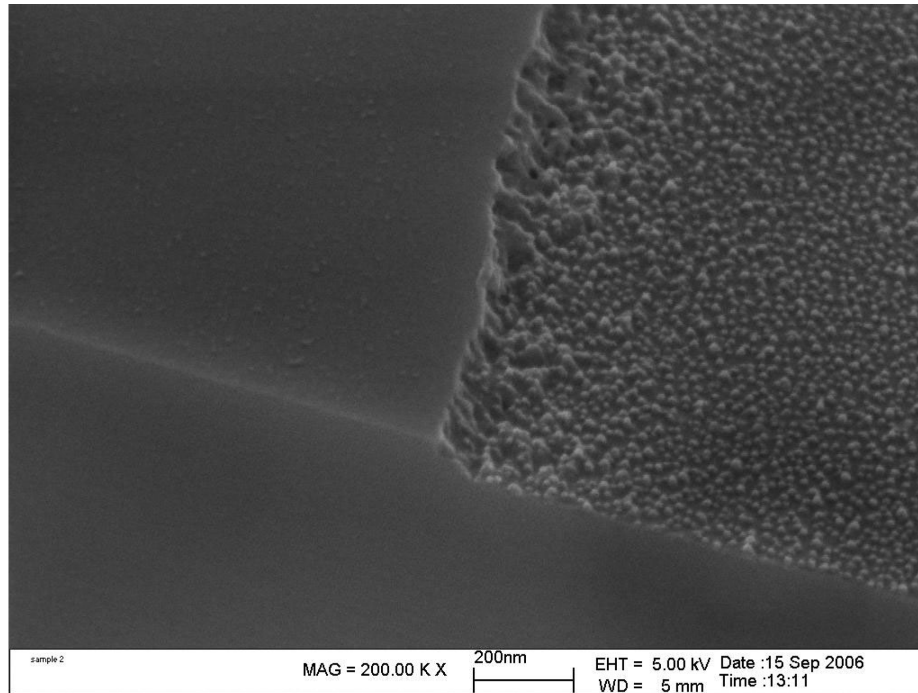
Dry etching is the second class of semiconductor etching methods. Reactive ion etching (RIE) is a form of dry etching that involves a plasma of reactive gases as

the etchant. High-energy ions from the plasma reach the substrate and physically or chemically react with it, which can lead to a product that is volatile. Unlike many of the wet etching methods, the fundamental dry etching process is anisotropic, or directional. There are several mechanisms which can lead to anisotropy. The first is the formation of thin polymer coating on the sample's surface, which can be from the fluorocarbon etch gases themselves and/or the erosion of the photoresist in the plasma. In flat areas this is physically removed by the bombardment of positive ions from the plasma in the vertical direction. The coating is not removed on the sidewalls of etched feature as they are not bombarded. The etching process from the neutral radicals is masked by the polymer and thus only occurs on horizontal surfaces, not vertical ones. This leads to preferential etching in the vertical direction. In other words, the etch is anisotropic. The modern CMOS industry has long since adopted dry etching to achieve small features and vertical sidewalls with high precision.

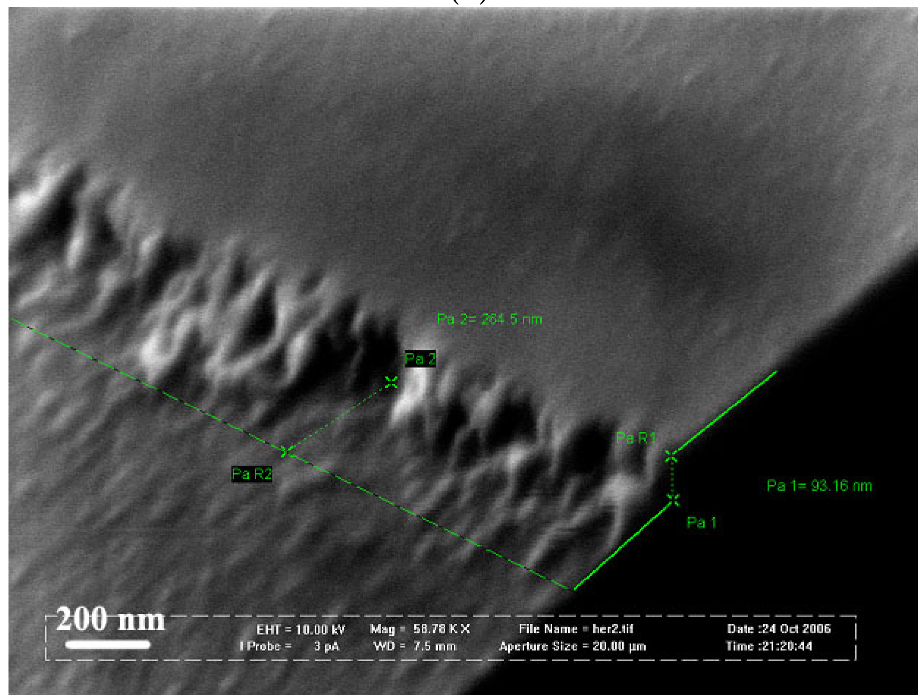
An ideal RIE recipe for quantum dot applications is sought to have the following properties: highly anisotropic for vertical sidewalls, steady and slow etch rate for precise control of the etched depth, and low Si/SiGe etch selectivity to avoid the need for multiple etches. Since anisotropic dry etching of Si-based materials is usually carried out with either chlorinated or fluorinated gases, we characterized common Cl or F-based gases by performing a shallow etch on planar Si substrates and subsequent SEM imaging.

All RIE were performed in a PlasmaTherm 720 SLR Series RIE system. It is a single-chamber system with a load lock and a turbo pump. For highly anisotropic etch we chose very low system pressures (< 10 mTorr) for low ion collisions and high ion energies. For most gas mixtures that we tried, SEM images revealed some excess polymer buildup on either planar surfaces or vertical sidewalls. Fig. 5.11 shows two examples of formations of such polymer products.

Pure chlorine-based chemistry is not well suited for our purpose as the Cl contam-



(a)



(b)

Figure 5.11: SEM images of Si/SiGe structures etched by RIE using: (a) Cl_2/Argon gas mixtures; (b) SF_2/CCl_2F_2 gas mixtures.

inant increases the roughness of bottom surfaces, as shown in Fig. 5.11 (a). It is also hazardous and corrosive and thus require special safety-related processing equipment. Next, we investigated the mix of chlorine and other fluorinated gases and its effect on polymerization. In general, polymer residuals are composed of carbon-fluorine polymers, and a low fluorine/carbon ratio should lead to increased polymerization. Among all the difference gas combinations that we tried, the chlorine in any of the etch gases (as Cl_2 or CCl_2F_2) did not reduce the excess polymerization on the sidewalls. Therefore, our only choices seem to be the pure F-containing etchants, such as SF_6 or CF_4. Fluorocarbon gases have often been used to produce deposition inhibiting lateral etching, resulting in anisotropy [100, 101, 102]. Indeed our best etching result was obtained in CF_4/O_2 gas mixture. Fig. 5.12 shows a SEM image of an etched Si/SiGe quantum dot structure. Compared to previous etched structures, both a straight sidewall profile and a clean bottom surface were achieved. It also shows an undercut of SiGe below Si layer in the heterostructure, which is due to faster plasma etching of SiGe than that of Si. Fluorocarbon gases with lower fluorine/carbon ratio such as C_4F_8 can produce more sidewall protection compared to CF_4 hence lead to a more straight sidewall profile through the different Si/SiGe layers [103].

Table 5.2 summarizes the dry etching characteristics of Si/SiGe heterostructures using different etch gases. The fluorocarbon plasma etching is clearly the most promising choice despite its preferential etching of SiGe. However, one inconvenience of the CF_4/O_2 gas chemistry is that it noticeably attacks PMMA or other polymer resist due to the presence of O_2 plasma, at an etch rate about the same as that of Si. Using pure CF_4 or CF_4/H_2 mixture does not improve the selectivity, since the etch rates of Si and SiGe also decrease proportionally. Therefore, for nanopatterning Si/SiGe heterostructures with CF_4-based gases, it is important that the patterned resist mask is at least as thick as the etch depth. The use of resists more resistant to dry etching, such as ZEP-520, is desirable for future work.

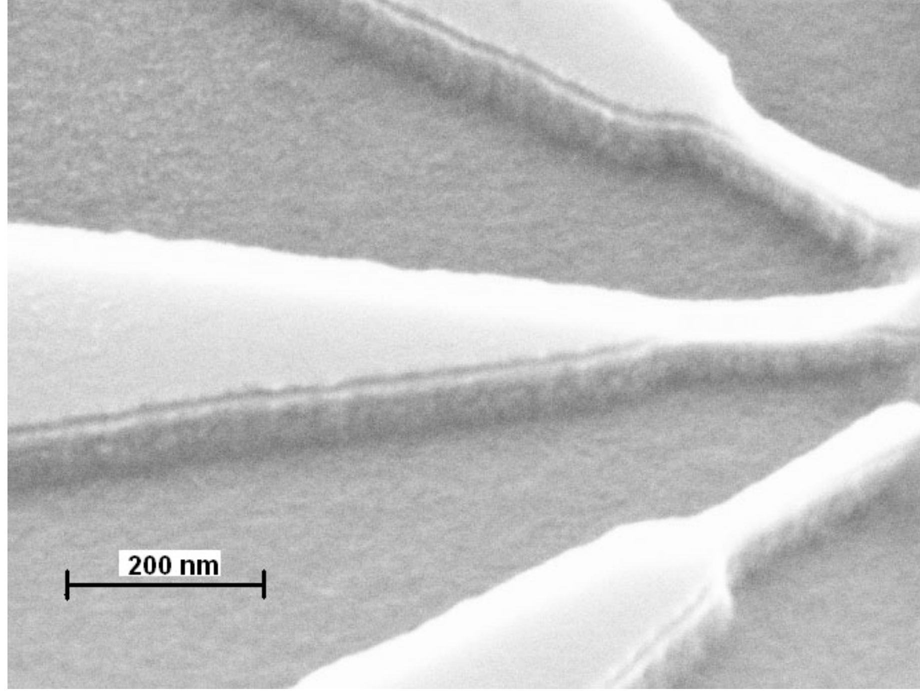


Figure 5.12: A SEM image of Si/SiGe quantum dot structure etched by RIE using CF_4/O_2 gas mixture showing a straight sidewall profile and a clean bottom surface.

Table 5.2: Properties of Si/SiGe RIE using different etch gases on planar substrates.

Gas flow rate (sccm)	RF Power (W)	Etch rate ratio ($Si_{0.7}Ge_{0.3}/Si$)	Sidewall	Bottom surface
SF_6/CCl_2F_2=20/2	50	1.07	very rough	rough
SF_6/Cl_2=10/10	50		rough	rough
CCl_2F_2/O_2=50/5	100	1.09	rough	rough
Cl_2/Ar=10/20	100	1.47	vertical	very rough
CF_4/O_2=50/5	100	1.6	vertical	smooth

The typical dry etch rate we used for Si/SiGe quantum dot applications is about 50 nm/min, which is about one to two orders magnitude slower than the wet etching. It is easier for fine tuning the dry etch rate by changing plasma source power and gas flow rates. So we chose RIE over wet etching for more complex device features such as multiple quantum point contacts and quantum dots.

5.3.3 Mix of Dry and Wet Etching of Si/SiGe

One potential worry when using dry etching methods is that the crystal surface is bombarded by ions and defects could be generated. This ion-induced damage could result in the deterioration of the device characteristics, especially in the high mobility 2DEG structures [104]. The bombardment damage induced in the material may occur both at top surfaces and at sidewalls. For unmasked top surfaces the mechanism for damage penetration is the accidental channelling of the incoming ion flux creating defects as they dissipate their final energy [105, 106]. For the sidewall case the damage channeling may occur from both ion bombardment and ricochet particles and materials ejected during etching [106, 107]. Penetration depths of over tens of nanometers may occur for some high-energy etch processes. The possible diffusion of defects in following fabrication steps can also modify the final defect distribution.

Much work has been devoted to minimize the dry etch damage, especially in III-V semiconductor systems since they cannot subsequently be anneal-treated. Here we propose a simple method using wet etching to remove potential sidewall defects created during dry etching. The Si/SiGe heterostructures were first etched by RIE to the desired depth, then immersed in HF/HNO_3 or $HF/H_2O_2/CH_3COOH$ for about 5 - 10 seconds to remove a thin sacrificial layer of Si/SiGe on the sidewalls and bottom surfaces of the trenches. This would remove etch-induced defects and shallow damage at these surfaces due to bombardment. The wet etch clean-up step will increase the minimum feature size due to the undercut from isotropic etch, but with only a fraction of the undercut created by a pure wet etching, since the wet etching is intended to remove only a very thin layer.

As one example, Fig. 5.13 shows a SEM image of Si/SiGe heterostructures etched by mix of CF_4/O_2 RIE and $HF/H_2O_2/CH_3COOH$ wet etching. The uneven features on the top surface are PMMA residuals and were later cleaned in 1165 stripper and ozone. Compared to the SEM (Fig. 5.12) obtained after only dry etching, the

undercut feature is $\sim$ 40 nm, about twice as wide as before.

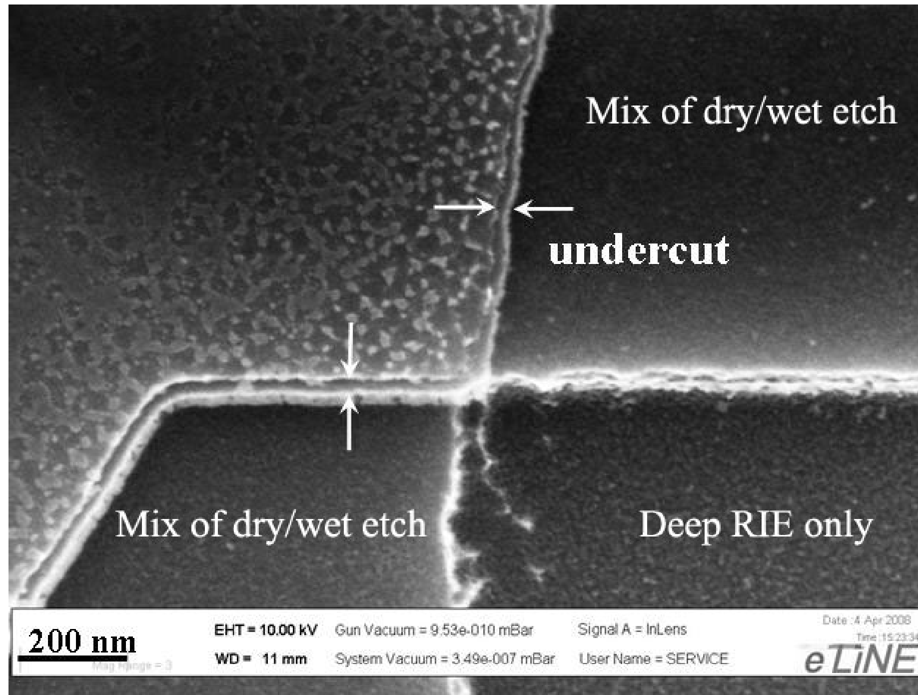


Figure 5.13: A SEM image of Si/SiGe heterostructures etched by RIE using CF_4/O_2 gas mixture and a subsequent 10-sec $HF:H_2O_2:CH_3COOH$ = 1:2:3 wet etching. The finished undercut features are marked by arrows.

5.4 Summary

With the demonstration of successful epitaxial growth of the 2DEG in strained Si and the enhanced electron mobility, realistic device applications will rely on fabrication techniques with a level of control consistent with quantum computing. For quantum dots using a lateral side-gating scheme, nanolithography and etching are the two most critical steps. In this chapter we discussed many options for each of the fabrication step. We focused on the advantages and limitations of each method, and an assessment of the possible role of each method in Si/SiGe heterostructure quantum dot applications is given.

Both e-beam lithography and AFM lithography directly write accurate nanopat-

terns on the substrate. E-beam lithography is commercially available and can provide high throughput with full compatibility with most etching techniques. AFM lithography by local anodic oxidation (LAO) represents a technological advance as a low-energy nanopatterning technique. The use of self-assembled monolayers such as PFOTS as a resist can improve the reproducibility of wet etching. It also extends the versatility of the technique by allowing the use of most of the wet etching methods.

As for the different etching methods for Si/SiGe systems, the main concerns are the minimum feature size and surface defects induced. A combination of successive selective wet etching can achieve precise control of etch stop in complicated multi-layer structures, but the undercut is still on the order of the total etched thickness and can be hard to control. Among the different dry etch plasma chemistries discussed, the fluorocarbon gas mixtures such as CF_4/O_2 yield the straightest sidewalls and clean bottom surfaces. We hypothesize that the use of a short wet etching as the finishing step can reduce dry etch induced surface damage by removing a thin sacrificial layer. The exact lateral undercut size will depend on the Si/SiGe heterostructure and the choice of etching method, and should be considered in nanolithography mask design.

Fig. 5.14 shows all the fabrication possibilities described in this chapter. For Si/SiGe quantum dot applications with feature size no smaller than 50 nm, our overall preference is e-beam nanolithography and the mix of dry and wet etching methods. This route adopts the standard CMOS fabrication technologies that offer high throughput and accurate control of all critical device profile dimensions, and adds a simple step to relieve defects associated with these high-energy processes.

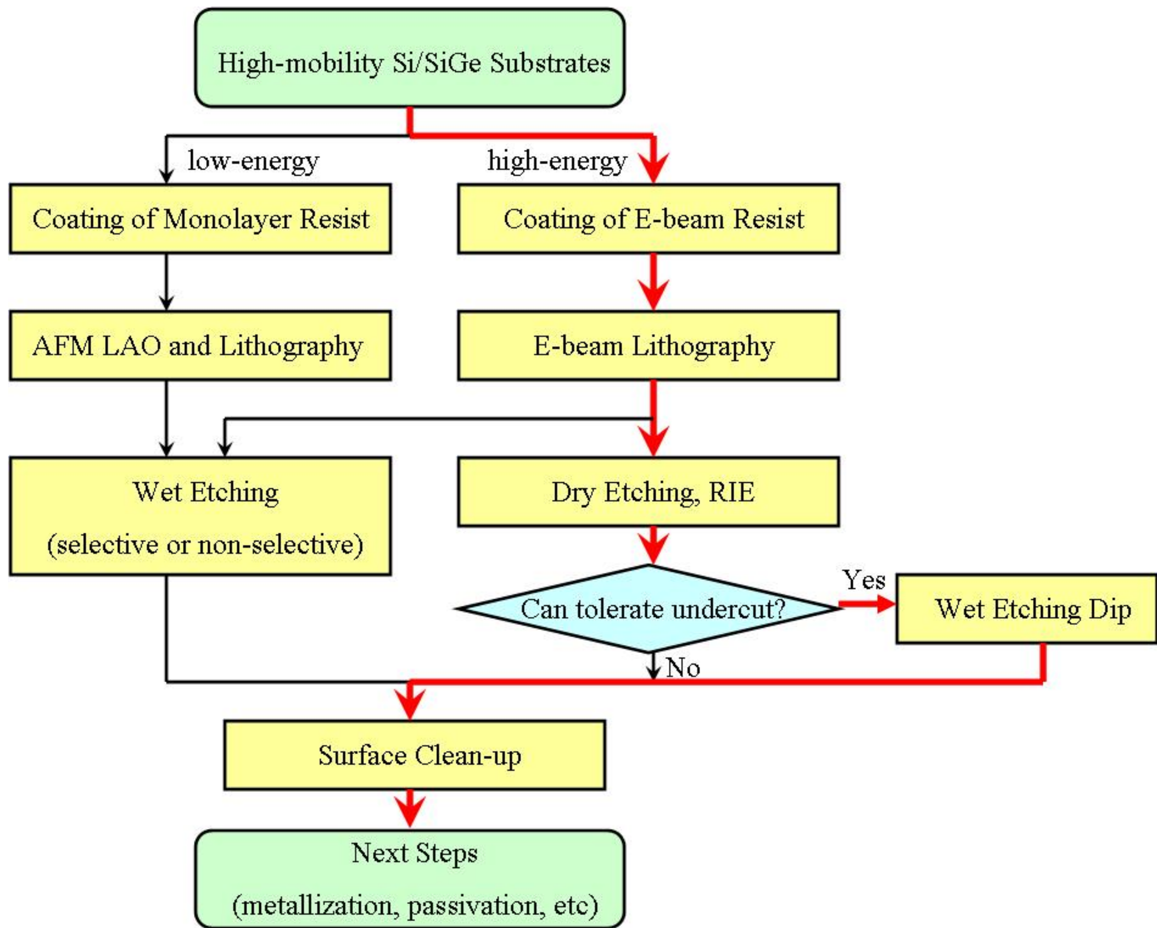


Figure 5.14: Flowchart of the fabrication possibilities for quantum dot applications combining different nanolithography and etching methods. Highlighted (thick red) line gives the overall preference for quantum dot device fabrication described in this thesis.

Chapter 6

Si/SiGe Epitaxial Regrowth

6.1 Introduction

In a quantum dot defined by etching, either by wet-chemical or reactive ion methods, the device surface is often left unpassivated. Single electron effects such as Coulomb blockade can be suppressed by trapping defects related to surface states. Even the best quality thermal SiO_2/Si interface has defect state density around 10^{11} cm^{-2} [108]. Considering the low thermal budget limited by the SiGe layer, the surface of such heterostructures, even with oxide passivation, is very vulnerable. As a result, unpassivated or poorly passivated Si/SiGe quantum devices often exhibit parasitic quantum dot characteristic and hysteresis [109], making it less desirable for the study of quantum computing.

To achieve better surface/interface control, we propose to use Si/SiGe epitaxial regrowth to cover the surface. Fig. 6.1 shows the passivated device structure. Since the overgrown interface is coherent, meaning that the lattice structure is continuous without dislocations or dangling bonds, the interface states due to the dangling surface bonds are therefore expected to be removed by such passivation. For strained Si/SiGe heterostructures on a SiGe relaxed buffer, the regrown layer is lattice-matched SiGe,

which will cause no strain if it has the same Ge content as in the buffer. Therefore, we can overgrow thick epitaxial layers so that surface effects can be minimized. A similar silicon epitaxial regrowth technique was first developed at Princeton and used in SiGe quantum dot single-hole transistor fabrication [110].

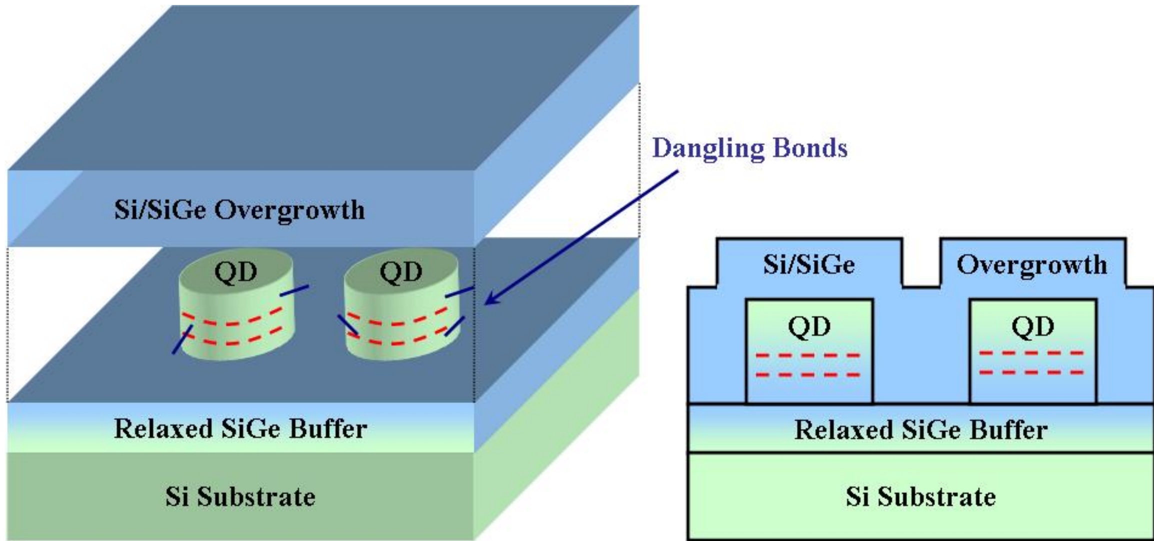


Figure 6.1: Schematic of Si/SiGe quantum dot devices with SiGe epitaxial regrowth. The regrowth ideally creates a coherent interface with no defect states.

The presence of the strained Si layer as well as dopants in the patterned Si/SiGe nano-structure requires a low thermal budget process, a major obstacle that prevents wide use of the epitaxial regrowth. Pre-cleaning processes with low thermal budgets have been studied by many groups [111, 112]. Recently, carbon-free and oxygen-free silicon surface with H_2 baking at 800 °C has been achieved with the Princeton RTCVD system [113]. As a novel alternative, thermal etching of silicon with chlorine is also capable of preparing smooth and contamination-free surface [114]. However, most work to date addresses silicon wafers other than nanopatterned quantum dot surfaces on SiGe relaxed buffers. We will conduct a thorough investigation of these specific issues.

6.2 Cleaning Processes for Si/SiGe Epitaxial Regrowth

6.2.1 Low-temperature Surface Cleaning by H_2 Bake

CVD epitaxial growth processes generally use an *ex situ* wet clean such as an RCA clean. In our system, for both growth and regrowth we use the same wet chemical clean of H_2SO_4/H_2O_2 solution (3:1) at room temperature for 15 minutes followed by a highly diluted HF (1:1000) dip for 2 minutes. In ultrahigh vacuum CVD (UHVCVD), no *in situ* cleaning step at all is required, but often residual carbon and oxygen contamination still are found at the interface [111]. Other conventional CVD methods have relied on high temperature *in situ* cleaning steps such as high pressure H_2 baking at above 1000 °C.

In our Princeton RTCVD system, the standard cleaning recipe is a 1000 - 1100 °C prebake at 250 Torr, with a H_2 flow of 4 slpm. Prebakes at or below 700 °C have not been effective at removing existing surface oxides and carbon, presumably because the temperature is too low for rapid enough desorption. Carroll et. al. [113] examined the pressure dependence of the interface cleaning at 800 °C and demonstrated that hydrogen bakes between 1 and 10 Torr can effectively remove contamination on the Si wafer surface. However, little work has been done to understand cleaning a Si/SiGe structure surface for further SiGe regrowth. For example, Fig. 6.2 shows a SIMS analysis for a regrowth with 800 °C H_2 bake on a modulation-doped Si/SiGe heterostructure. After the growth of the modulation-doped Si/SiGe layers, the wafer was removed from the RTCVD chamber and reloaded after a standard wet clean. The *in situ* clean of the regrowth was done by 2 minutes baking in H_2 at 800 °C. An oxygen peak is still present at the interruption interface between the original silicon cap and the regrown SiGe.

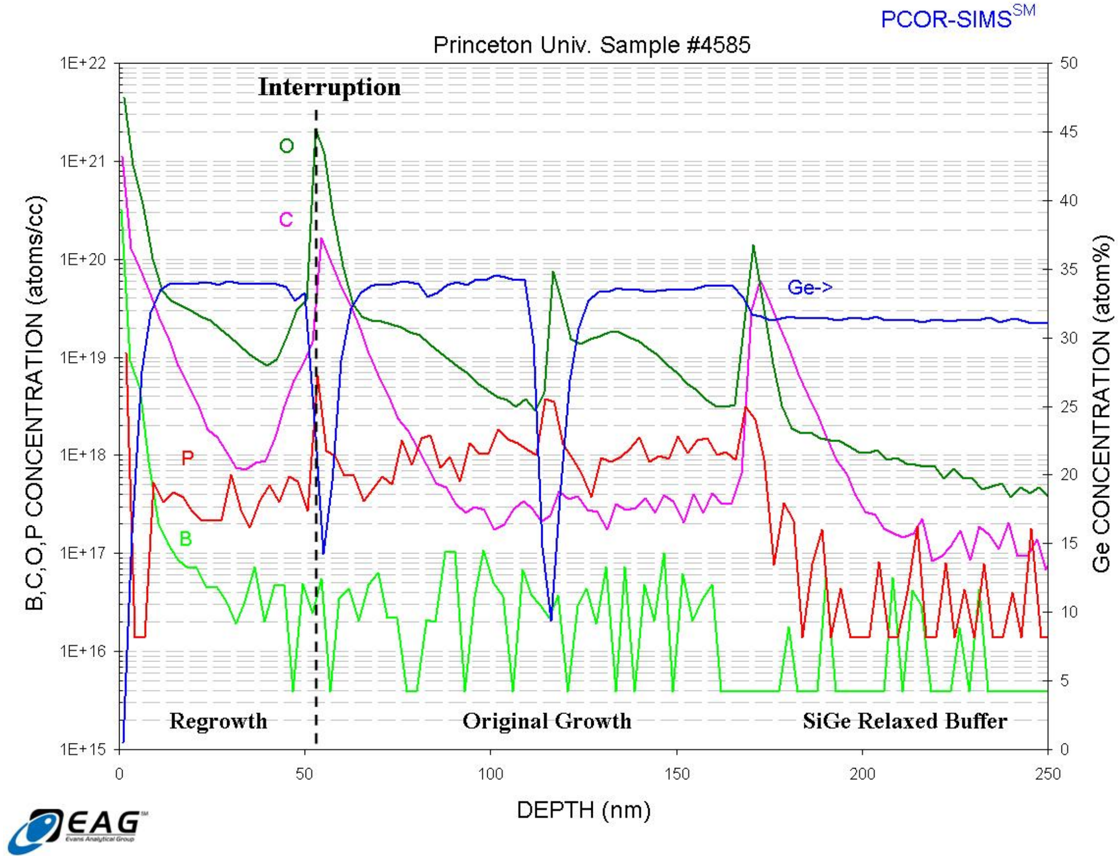


Figure 6.2: SIMS analysis of sample #4585 with epitaxial $Si_{0.7}Ge_{0.3}$ regrowth on a 2DEG in Si/SiGe on $Si_{0.7}Ge_{0.3}$ relaxed buffers. The *in situ* cleaning is a 800 °C 3 slpm H_2 bake at 6 Torr for 4 minutes.

In our modulation-doped Si/SiGe heterostructures, all SiGe layers are relaxed and the total strained Si thickness is well below the (metastable) critical thickness, so thus we could use slightly higher temperature to achieve regrowth of pristine interfaces without worrying about the relaxation of the strained silicon channel. To estimate the effect of phosphorus diffusion, we first note that the silicon intrinsic carrier density around 800 °C is already on the order of 10^{18} cm^{-3}, so we can use the diffusivity under intrinsic inert conditions. Recent measurements of the intrinsic diffusivity of phosphorus in silicon yield the following fit [115]:

$$D_p = 1.71 \times 10^{-3} exp\left(-\frac{2.81\ eV}{kT}\right)\ cm^2/s. \tag{6.1}$$

Unlike the arsenic diffusion in the relaxed SiGe buffers case as we discussed earlier in Chapter 3, the supply and spacer SiGe layers have very few dislocations and the phosphorus diffusion in relaxed SiGe was found to be enhanced by about a factor of three compared to in Si [117, 116]. For example, the reported P diffusivity in $Si_{0.74}Ge_{0.26}$ is about 2.5×10^{15} cm^2/s. Hence the diffusion length for 1 minute of 850 °C bake is $l_p = \sqrt{D_{p(sige)}t} = 3.9$ nm, an acceptable length considering our intrinsic supply layer is usually 10nm or thicker. Higher temperatures would be clearly not feasible.

6.2.2 Chlorine Etching for Low-temperature Surface Cleaning

Recently the use of a thermal step in chlorine as pre-clean before epitaxy has been proposed, as it could lead to a pristine surface (with low interfacial carbon and oxygen concentration) and hence allow a lower temperature prebake. Such *in situ* thermal etching of Si or SiGe with gaseous hydrogen chloride (HCl) or chlorine (Cl_2) removes a thin layer from the surface and substantially reduces reduces surface phosphorus, carbon and oxygen spikes. In a hydrogen ambient the temperature for such chlorine-based etching is still around 800 °C as the etch rate was negligible at lower temperatures.

However, the usefulness of the chlorine etching for regrowth on Si/SiGe nanostructures is severely limited by two factors. First, in practice it is difficult to achieve precise control of the etched surface layer thickness. Typical modulation-doped Si/SiGe heterostructures contains a thin silicon cap. The silicon may act as an etch stop for the SiGe layers, as the etch rate of SiGe in chlorine chemical vapor increases with Ge content and is much faster than that of Si [118]. The exact thickness of such a silicon cap will vary depending on the fabrication process. Second, for the quantum device area that was etched during the fabrication, all strained silicon

were removed and only SiGe was left. The chlorine etching in these area will result in over-etching and increased surface roughness. In fact, we observed very non-uniform epitaxial regrowth with *in situ* chlorine etching - some of the device area without the thin silicon cap was not covered by epitaxial regrowth. Fig. 6.3 shows a cross section TEM image of a gap near an etched Si/SiGe edge #4547. Poor crystalline quality would result from the regrowth on the bottom of trench.

Figure 6.3: A cross section TEM image a narrow gap etched in a 2DEG in Si/SiGe on $Si_{0.7}Ge_{0.3}$ relaxed buffers with Si/SiGe regrowth using chlorine etching as a pre-clean step. The TEM was prepared by Dr. Nan Yao at Princeton and Hitachi laboratory, CA.

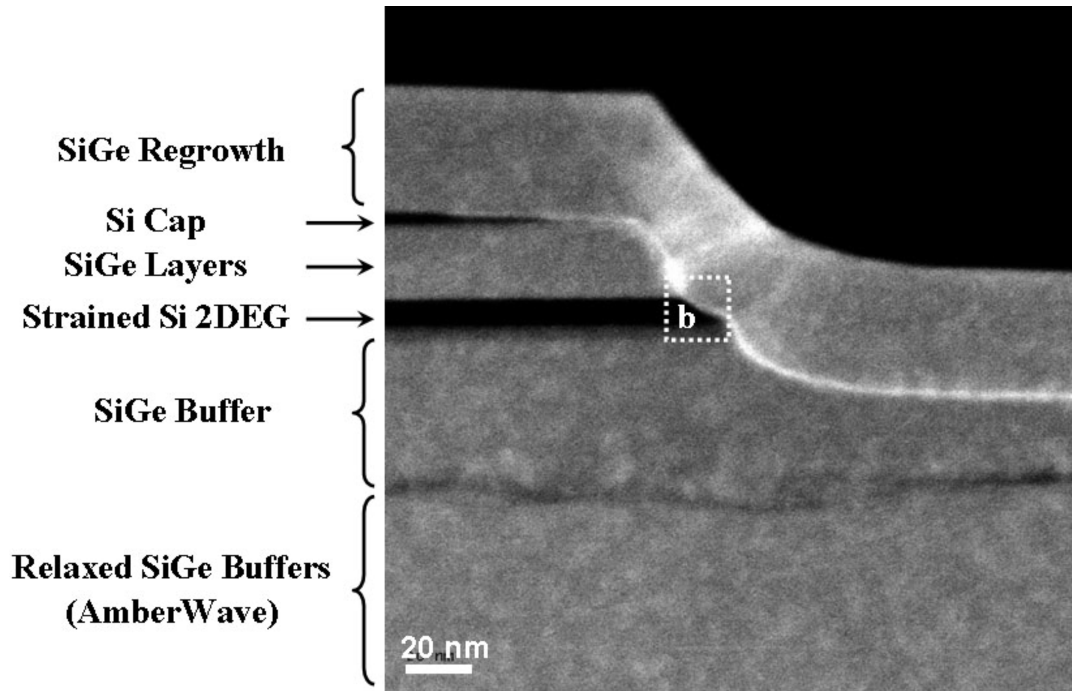
Therefore, the novel technique of etching a thin Si/SiGe layer with chlorine cannot be used prior to epitaxial regrowth on already patterned surfaces. Such etching will cause serious non-uniformity in the regrown layer and should be avoided unless the surface cap layers are very thick ($\sim$ a few tens of nanometers). Therefore this approach was ruled out for our critical device fabrications.

6.2.3 Conformal Epitaxial Regrowth on Sidewalls

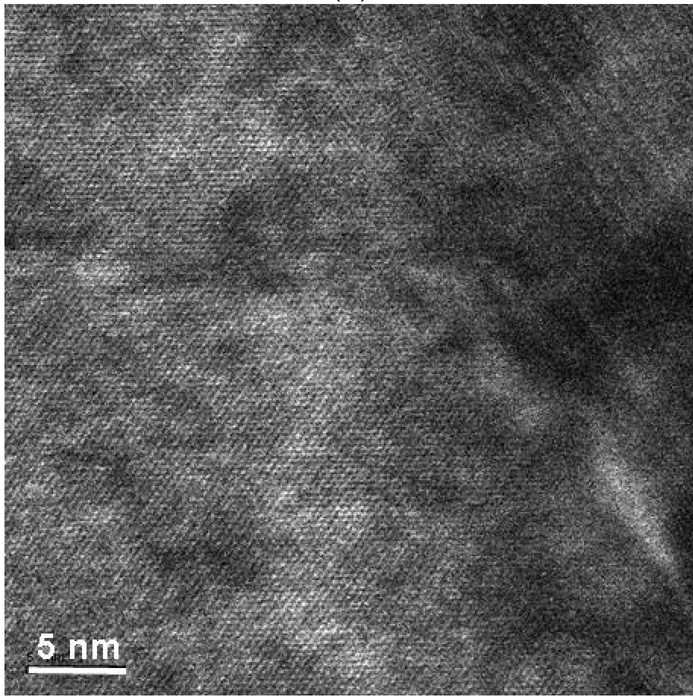
With a better understanding of the surface cleaning issues and the elimination of *in situ* chlorine etching on patterned heterostructure surfaces, we achieved conformal epitaxial regrowth on sidewalls at nano-scale and uniform coverage over the whole wafer. Dr. Nan Yao at the PRISM Imaging and Analysis Center at Princeton University and the Hitachi Labs of California performed high resolution cross section TEM on a patterned Si/SiGe sample with epitaxial regrowth.

The starting sample is a strained Si 2DEG on 30% SiGe buffers. A series of 600-nm-wide, 50-nm-deep lines were defined by E-beam lithography and etched in a CF_4/O_2 gas mixture by RIE. This was followed by epitaxial regrowth of 50 nm thick SiGe capped by a 4-nm Si layer at 625 °C and 700 °C, respectively. The *insitu* pre-clean of the regrowth was done by 5 slpm hydrogen baking at 800 °C for 2 minutes at 6 Torr. Fig. 6.4 shows the cross section TEM image of a narrow gap near an etched Si/SiGe edge #4607 with a zoom-in view of the sidewall. The first noticeable feature is that we clearly achieved crystalline regrowth of SiGe on such a structure. The atomic lattice is continuous at both sides of the interface. 3-D heterojunction confinement surrounding the whole nano-structure was achieved. Fig. 6.4 (a) represents dramatic improvement of the epitaxy uniformity on etched surfaces over the prior poor regrowth. However, the interface is not perfect. Some stacking faults can be observed in the regrown region near the vertical sidewalls. The horizontal interfaces at both the bottom and the top of the trenches appear to be defect-free.

The exact mechanism of defect formation during the regrowth is still unknown. One possibility that we suggest is the strain field induced by the presence of the strained silicon. For the thin tensilely strained silicon, its in-plane silicon lattice matches the SiGe lattice, therefore the regrown SiGe over either strained silicon or relaxed SiGe will bear no strain. On the other hand, when the SiGe regrowth matches



(a)



(b)

Figure 6.4: (a) A cross section TEM image of a narrow gap etched in a 2DEG in Si/SiGe on $Si_{0.7}Ge_{0.3}$ relaxed buffers with conformal epitaxial regrowth on sidewalls. (b) A high resolution TEM image of the sidewall coverage, showing that the regrowth over the sidewall is epitaxial. The TEM was prepared by Dr. Nan Yao at Princeton and Hitachi laboratory, CA.

the perpendicular lattice constant of the strained silicon on the sidewalls, to form a coherent interface the regrown SiGe has to be under compressive strain. Such a strain field effect will only affect the sidewalls.

While the overgrown interface is not perfect, the process shows a route to defect densities which are probably lower than that of the SiO_2/Si interface. Such defect state density is around 10^{10} cm^{-2} for the best quality thermal SiO_2/Si process on perfect (100) surfaces, and it is known to be much higher on other crystalline phases and on SiGe surfaces [119]. We believe that SiGe epitaxial regrowth on etched strained Si quantum dots has the potential to give the best interface control technique and passivation for Si/SiGe quantum dots and related quantum devices.

6.3 Electrical Properties of Si/SiGe Epitaxial Regrowth

6.3.1 The Effect of Si/SiGe Regrowth on 2DEG's

The first critical electrical property of Si/SiGe epitaxial regrowth for quantum dot applications is its effect on the 2DEG quality. As shown in previous calculation, the dopant diffusion during the regrowth is expected to be a few nanometers. The dopant segregation or diffusion towards the 2DEG channel will cause degradation in the electron mobility as well as an increase in the electron density.

We compared electron density and mobility on two sets of 2DEG samples before and after the regrowth. The first set of 2DEG were grown by Princeton RTCVD system with relatively low mobilities. The second set of high quality samples were grown by Dr. Ya-Hong Xie's research group at UCLA in MBE. Both regrowth were done in Princeton RTCVD with low-temperature surface cleaning by 5 slpm H_2 baking at 800 °C for 2 minutes at 6 Torr. Table 6.1 summarizes the results of the two sets of

samples from low-temperature Hall measurement. As a result of the dopant diffusion, the effective spacing between the 2-D electrons and their ionized dopants should be reduced. The electron density increases as more carriers can be transferred to the channel, and the mobility degrades due to the enhanced Coulombic scattering from remote doping. We observed 3% and 10% reduction in electron mobility for the low-mobility and high-mobility 2DEG samples, respectively.

Table 6.1: Effects of SiGe epitaxial regrowth on 2DEG.

Sample		#4478	LJ196
Growth		Princeton CVD	UCLA MBE
Ge content		30%	20%
Spacer thickness (nm)		10	20
Density (cm^{-2}))	Before regrowth	1.16×10^{12}	3.50×10^{11}
	After regrowth	1.47×10^{12}	4.0×10^{11}
Mobility ($cm^2V^{-1}s^{-1}$)	Before regrowth	6,500	290,000
	After regrowth	6,300	260,000

In general, one expects that regrowth has a more detrimental effect on the mobility for high-mobility samples in which remote doping scattering dominates. This can be seen from equation (3.20) and (3.22) in Chapter 3. Diffusion and segregation will reduce the effective spacing thickness h_{eff}. Therefore the mobility component μ_{remote} should decrease with a smaller h_{eff}; while $\mu_{background}$ remains unchanged approximately. From the device aspects even 10% degradation in mobility is acceptable considering the sample-to-sample variations over the wafer scale, other effects due to the later fabrication etc. In addition, the sheet resistance of the sample actually decreased in both cases as a net result because of the increased electron density.

6.3.2 The Leakage Across Si/SiGe Regrown Layers

The second concern of the regrowth is leakage. The regrown layer could add extra leakage paths for electrons. Fig. 6.5 shows an example for regrowth over a strained silicon 2DEG from a side gate to the quantum dot. In the original 2DEG structure,

electrons exist either in the strained silicon channel or in the doped SiGe supply layer due to excess dopants. These electrons can travel through the regrown material from a side gate to the quantum dot and cause extra leakage. In an ideal case both leakage paths would not be conducting at zero temperature. The excess electrons in the supply layer should freeze out if their doping level is below the Mott-transition level. The free electrons in the Si channel should not tunnel through the SiGe due to the barrier from the conduction band discontinuity. However, with the possible defects at the interfaces, the band discontinuity might not suppress the current, which could be caused by the dislocation "pipes" similar to the substrate leakage issue that was addressed in Chapter 3. We will perform electrical measurement to test such leakage.

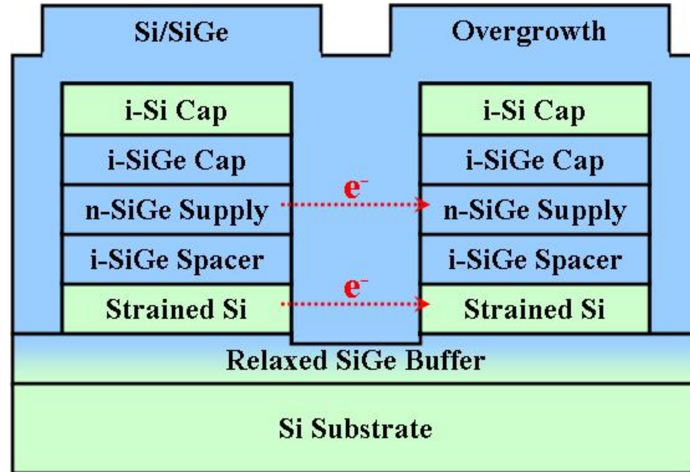
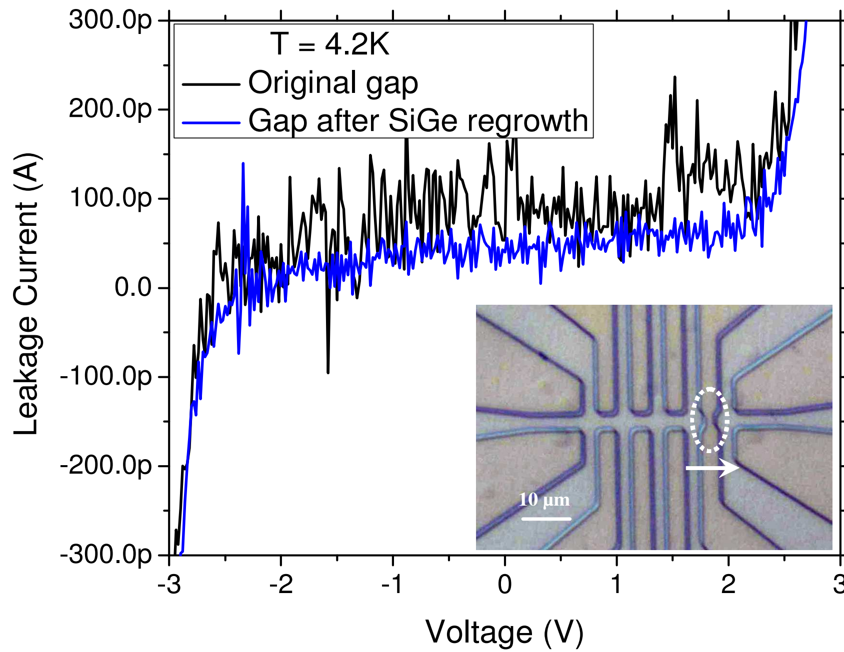


Figure 6.5: Schematic view of SiGe epitaxial regrowth over an etched 2DEG showing possible new leakage paths for electrons. (For example, from a side gate to a laterally adjacent quantum dot.)

We measured the leakage current after regrowth across narrow gaps of two different sizes etched into a conducting path of 2DEG. The first gap is about 2 μm wide, defined by optical photolithography. The second gap is only about 100 nm wide, defined by e-beam lithography. Fig. 6.6 shows the I-V characteristics across gaps of the two different sizes. The substrate was floating. More leakage was found at smaller gap sizes by comparing the leakage current from Fig. 6.6 (a) and (b). For the submicron scale that is more relevant for quantum dot applications, up to 0.5 V



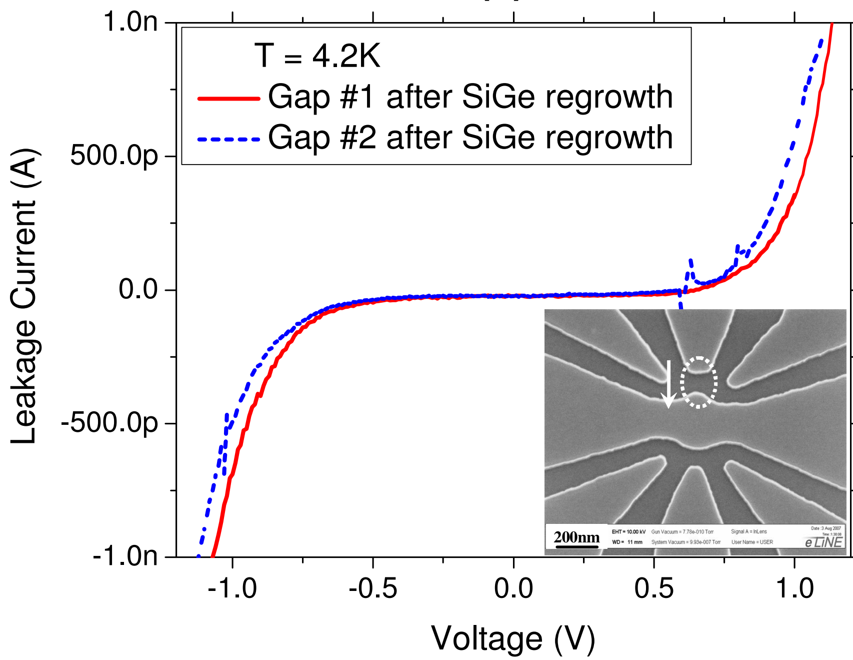


Figure 6.6: I-V curves of the leakage current vs. gate voltage across narrow gaps of (a) micron scale (2 μm defined by optical lithography); (b) sub-micron scale (100 nm defined by e-beam lithography).

of voltage can be applied on the side gate with the leakage current less than 100 pA, and current less than 1 nA for up to 1 V. From Fig. 6.6 (a) we can also see that the regrowth process does not significantly affect the leakage magnitude. Thus the dominant leakage should be from the strained Si 2DEG layers to the relaxed SiGe buffers, which was not affected by the regrowth process.

Therefore, with the regrowth technique the patterned nanostructures with narrow gaps can be used for side gating if the voltage applied is within ± 1 V. The gate leakage is sufficiently low. The gate voltage would be high enough for planar gates to be used to modulate the electrostatic potential and electron density of the strained Si 2DEG.

6.4 Summary

In this chapter we developed a novel Si/SiGe epitaxial regrowth technique for surface passivation on quantum dot devices. The motivation is to achieve perfect surface/interface control that can eliminate trapping/detrapping of carriers due to the presence of defects and surface states. Our approach is to regrow epitaxial Si/SiGe over the patterned devices.

We first investigated the growth issues related with the Si/SiGe epitaxial regrowth. A low-temperature bake in hydrogen (less than 850 °C) has shown success in reducing carbon and oxygen contamination without significant dopant diffusion in existing layer structures. Additional thermal etching of surface by chlorine can achieve cleaner surface/interface but will likely cause surface roughness. By choosing proper surface cleaning process, we achieved conformal epitaxial regrowth sidewalls over the whole wafer.

The interface quality and regrown crystalline structure were studied by TEM. We clearly confirmed the single crystalline nature of the regrowth by TEM. However, it

also shows some stacking faults at the vertical sidewall interfaces of regrown SiGe. This may be due to the strain around the strained Si 2DEG channel. By comparing the 2DEG density and mobility with and without regrowth, we found less than 10% degradation of the electron mobility, while the electron density increased slightly. The sample sheet resistivity was reduced as a net result. The leakage in regrown side-gating structure is negligible if the voltage applied is within ±1 V, which is reasonabe for tuning the potential of the patterned quantum dot devices.

In conclusion we have demonstrated successful SiGe/Si epitaxial regrowth for surface passivation of Si/SiGe quantum dot applications to avoid potential defect states. Such passivation will hopefully reduce the undesirable surface effects, so that improvement in the device characteristics can be expected.

Chapter 7

Characterization of Quantum Dot Devices

7.1 Introduction

The quantum dot, as the name suggests, represents a tiny region of matter only a few atoms across, in which carriers are confined in all three spatial dimensions. The term "Quantum Dot" was coined by Texas Instruments scientists Mark Reed et al. [120], who is now a professor at Yale University. Semiconductor quantum dots provide highly tunable structures for trapping and manipulating individual electrons. Such quantum dots are proposed to function as "qubits" to achieve semiconductor-based quantum computation, which may eventually replace today's transistors, just as transistors replaced the vacuum tubes half a century ago. In the past several years, the development of Si/SiGe quantum dots have made significant progress.

So far in this thesis we have already addressed technology issues ranging from material growth and regrowth quality to fabrication techniques such as gating and nanopatterning. In this chapter, we will demonstrate simple quantum device applications of these technologies. Two types of devices are of special interest: the quantum

point contact (QPC) and the single-electron transistor (SET).

A QPC consists essentially of a short, narrow constriction connecting two conducting reservoirs. In a QPC, quantized conductance is observed as a result of the 1-D quantization, which directly proves the ballistic transport process. QPCs are often used as mesoscopic charge sensors adjacent to quantum dots for a noninvasive read-out of the spin state [121]. In Si/SiGe heterostructures, QPCs were first fabricated by a metal split-gate [122]. Wet-chemical etch-defined Si/SiGe QPCs have also been reported, in which the 1-D subband energy spacing was successfully extracted [123].

A single Si/SiGe quantum dot is a special type of SET with carrier confinement in all three dimensions. It consists of two tunnel junctions on both sides of a quantum dot. The electrical potential of the dot can be tuned by a coupled gate. The dot may contain zero, a few, to a few thousand carriers. The single electron tunneling effect is significant. The coulomb blockade effect will cause oscillations in the QD conductance as a function of the gate voltage. For the purpose of quantum computing, quantum dots are the key component at the heart of quantum information processing. For example, Loss and DiVincenzo themselves proposed to realize the qubit as the spin of the excess electron on a single-electron quantum dot [13]. SET development in Si/SiGe is not as established as those for III-V materials. The fabrication of Si/SiGe quantum dots using both Schottky top-gating [58, 59] and etch-defined side-gating [124] were reported recently, while there also exist more sophisticated schemes mixing of both trench isolation and Schottky gating [125, 126]. It is noteworthy, although most people propose to use a double-dot device of two laterally coupled single dots for spin exchange operations, with our proposed novel double quantum well structures described in Chapter 4, a single QD without any gate may be sufficient for such interaction functions.

7.2 Charactierizaton of Quantum Point Contact Devices

7.2.1 A Single Quantum Point Contact Device

We combined e-beam lithography, RIE and selective wet etching to fabricate single QPC devices on a Si/SiGe 2DEG. The 2DEG sample #4491 had a 2-D electron density of 1.5×10^{12} cm^{-2}, and a low-temperature mobility of $\mu = 6400$ cm^2/Vs. The details of the fabrication techniques were discussed in Section 5.3.1 of Chapter 5. A shallow RIE followed by $HF/H_2O_2/CH_3COOH$ and TMAH etching were used to etch the narrow gaps. After the lithography, the sample surface was passivated by epitaxial regrowth of 50 nm $Si_{0.7}Ge_{0.3}$ followed by a thin Si cap. Finally, ohmic contacts to the 2DEG were formed by lift-off of AuSb evaporation and forming gas anneal at 400 °C for 10 min.

Fig. 7.1 shows a SEM image of the completed QPC device. The confinement of the channel is about 200 nm wide. The 2DEG itself was also used for side-gating by etch-defined lateral gates that are placed about 200 nm away on both sides from the central channel area. Electrical measurements were conducted at 1 K in a dilution refrigerator by Professor Leonid Rokhinson's laboratory at Purdue University.

Our measurement of channel conductance with applied side-gate voltage is shown in Fig. 7.2. The side gates work well up to ±2 V with gate leakage less than 1 nA. At a gate voltage of –2.2 V pinch-off is reached, the channel constrictions become completely depleted and the channel is shut off.

In an ideal semiconductor QPC structure, one of the most striking features was the discovery of the conductance quantization in units of $2e^2/h$ as the gate voltage is swept in the absence of a magnetic field [127, 128]. The factor 2 comes from the spin degeneracy $g_s = 2$. In SiGe heterostructures, the additional valley degeneracy $g_v = 2$ will lead to a total conductance quantization in multiples of $4e^2/h$. In our

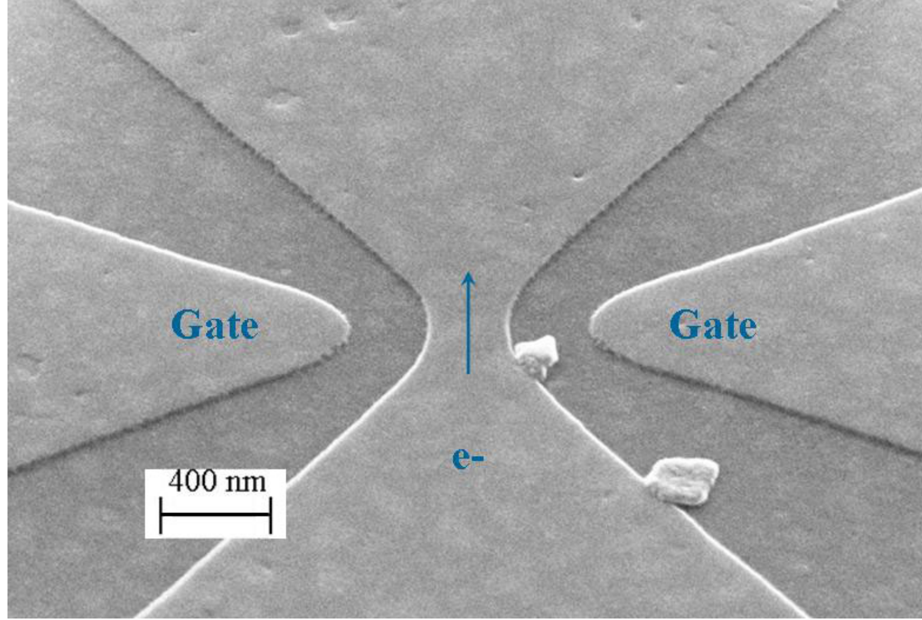


Figure 7.1: A SEM image of Si/SiGe QPC patterned by low-damage wet etch and epitaxial dot passivation.

QPC devices, the quantization of conductance at $G = 4e^2/h$ is missing, and a fairly flat plateau at $G = 2 \times 4e^2/h$ is observed. The discrepancy between the conductance quantization measure in our QPC and that from a high quality QPC is due to the low electron mobility, which can cause the electron transport in the confined QPC region to deviate from ballistic. We will evaluate the ballistic transport assumption by first calculating the electron mean free path.

In a 2DEG, the electron scattering rate can be derived from the measured mobility:

$$\mu = \frac{e\tau}{m^*} \Rightarrow \tau = \frac{\mu m^*}{e}. \tag{7.1}$$

An estimate of the elastic mean free path can then be calculated by assuming a Fermi velocity between scatterings:

$$\lambda_{elastic} = v_{Fermi}\tau = \frac{\hbar\mu}{e}\sqrt{\frac{4\pi n_{2D}}{g_s g_v}}. \tag{7.2}$$

For the 2DEG sample #4491, using parameters μ and n_{2D} as mentioned above,

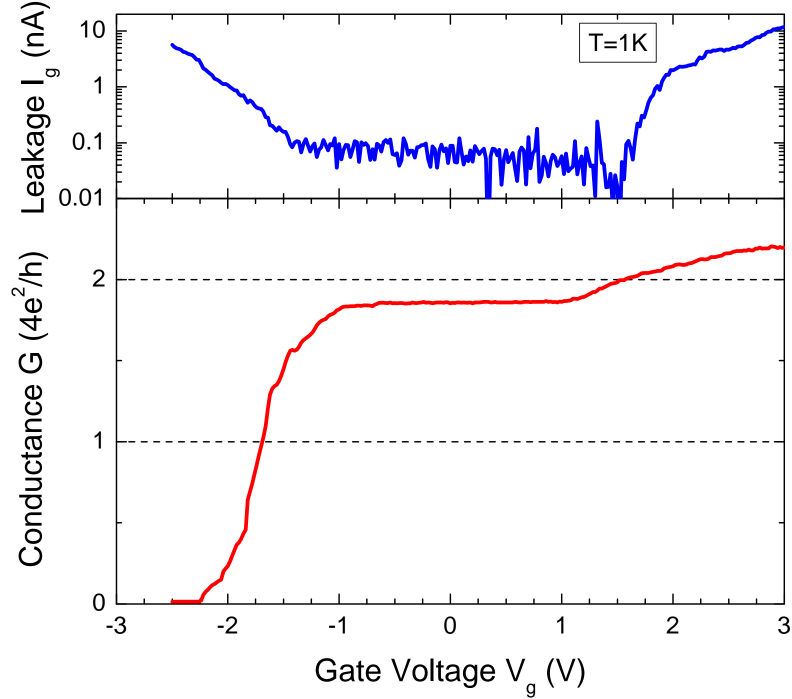


Figure 7.2: Channel conductance and leakage current through the gate in a quantum point device as a function of the applied gate voltage at zero magnetic field.

and $g_s = g_v = 2, m^* = 0.19\ m_0$, we found the electron mean free path $\lambda_{elastic}$ to be 92 nm, which is comparable but certainly smaller than the QPC feature size of about 300 nm. Therefore, the electron transport through our quantum point contact devices is not totally ballistic. To observe ballistic transport, higher mobility 2DEG or smaller QPC confinement size by a factor of at least three are needed, and will be a subject of future work.

7.2.2 Quantum Point Contacts Used as Tunnel Junctions in A Quantum Dot

The successful pinch-off of QPC has allowed us to fabricate more complicated quantum dot devices with etch-defined side gates in 2DEG itself. Fig. 7.3 shows a SEM

image of a single quantum dot confined with six etch-defined side gates. The quantum dot is fabricated on 2DEG sample #4811 with an electron density of 8×10^{11} cm^{-2}, and a low-temperature mobility of $\mu = 6800$ cm^2/Vs. We used only one dry etch (CF_4/O_2 RIE, see Section 5.3.2 of Chapter 5) to define the quantum dot area. The high etching anisotropy has enabled us to achieve a channel width as narrow as 150 nm and a gap width below 100 nm between the channel and gates. Epitaxial regrowth SiGe was done to passivate the dot surfaces.

In such a quantum dot structure, the two quantum point contacts (confined between gate 3 - 11, and 5 - 9, as labeled in Fig. 7.3) are intended to define tunnel junctions between the dot and the source/drain. The other pair of split gates 4 - 10 is used to tune the electrical potential of the dot. Before we move to more complicated quantum dot characteristics, each individual side gate was electrically tested independently, i.e., when a voltage is applied to one gate all other side gates are grounded.

Fig. 7.4 shows the channel conductance with applied gate voltage on each individual side gate at 4.2 K. First we noticed that all side gate are normally "off". When no voltage is applied the channel is pinched off. This can be attributed to the surface depletion induced by the ion damage during the dry etch. A positive gate voltage of a typical value of 0.4 V is required to remove such depletion regions. Second, since the tunneling junction area and even the central dot are small, we observed some channel conductance characteristics similar to the quantization in a single QPC. Especially when the channel is tuned by gate 3, a nice conductance plateau at $G = 4e^2/h$ is clearly present. Due to the low mobility and the presence of possible electrical damage near the edges, we do not expect the electron transport to be totally ballistic. The fact that all six side gates are working properly with complete pinch-off and sufficiently low leakage is very promising for our further pursue of quantum dot devices.

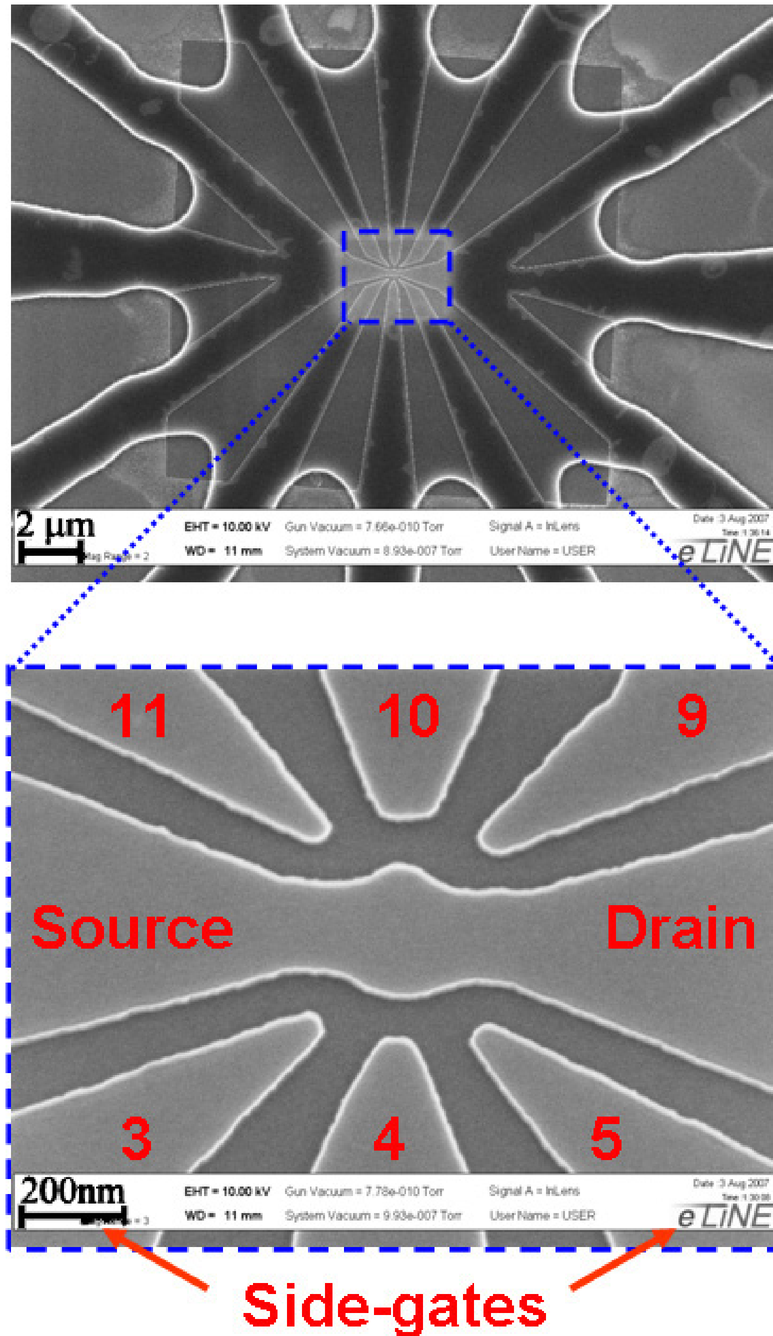


Figure 7.3: A SEM image of a single Si/SiGe quantum dot with six side gates patterned by RIE dry etch and epitaxial regrowth.

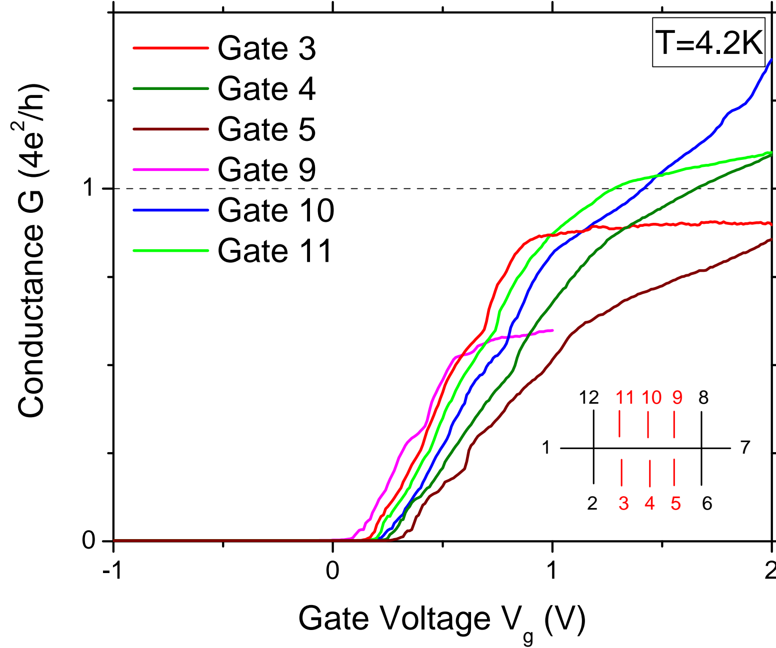


Figure 7.4: Channel conductance in a quantum dot device at T = 4.2 K as a function of the applied gate voltage at zero magnetic field. When a voltage is applied to each individual gate, all other five side gates are held grounded.

7.3 Characterization of Single Quantum Dot Devices

7.3.1 Coulomb Blockade and Quantum Dot Energies

Fig. 7.3 shows a single quantum dot, which contains a small island which is coupled to electron reservoirs through two tunneling junctions. Such a quantum dot is one of the simplest devices that exhibit Coulomb Blockade (CB), a single electron tunneling effects.

Fig. 7.5 describes the energy levels in a single quantum dot system. Assuming the energy spacing ΔE in the dot is greater than the thermal energy for low temperatures, electron transport through the dot is determined by Coulomb charging. When the

applied source-drain bias is small, in the blocking state, there are no accessible energy levels within tunneling range of electrons from the source to the drain. All energy levels on the dot with lower energies are occupied, as a result no current can flow.

When a gate voltage is applied so that the energy levels of the dot are lowered and a previous vacant level is brought within the source-drain bias, the electron can now tunnel onto the island then from there it can tunnel onto the drain. This is the transmitting state of the dot, and the conductance will become non-zero. Sweeping the gate will change the total number of occupied states of the dot and thus the conductance has periodic peaks rising from zero to a set of sharp peaks.

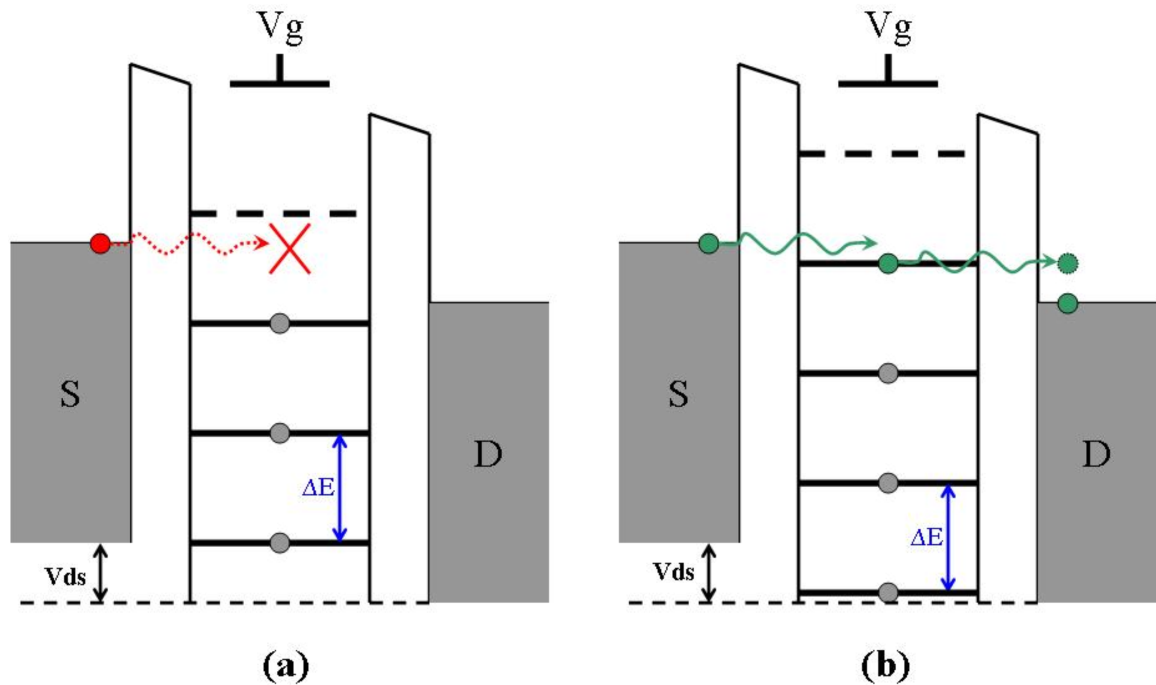


Figure 7.5: Energy levels of a single quantum dot for (a) the blocking state, and (b) the transmitting state.

The energy spacing of the levels in the quantum dot is defined as the "addition energy", and it can be estimated by the sum of the "charging energy" and the quantum well energy spacing. Since the dot has a finite capacitance C, to add one electron costs a charging energy of e^2/C. The second term $\Delta\epsilon$ origins from the splitting between the energy quantization in the quantum well itself, and can be computed from solving

the eigen-energies in a 2-D square potential well, for example. Therefore,

$$\Delta E = e^2/C + \Delta\epsilon. \tag{7.3}$$

The dot's self-capacitance can be estimated with a simplified isolated thin conducting disk model. If the disk has a radius of r in a dielectric-filled space, its capacitance is given by

$$C = 8\epsilon_r\epsilon_0 r. \tag{7.4}$$

For an estimate of $\Delta\epsilon$, since the energy levels for 2D-confined electrons are give by

$$E_{2D} = \frac{\hbar^2}{2m}\left[\left(\frac{2\pi n_x}{2r}\right)^2 + \left(\frac{2\pi n_y}{2r}\right)^2\right], n_x, n_y = 0, \pm 1, \pm 2, \ldots, \tag{7.5}$$

where 2r is the length of the 2D box. For a system that contains only a few electrons, the energy spacing can be assumed approximately to be a constant

$$\Delta\epsilon \approx \hbar^2/m^* r^2. \tag{7.6}$$

The total addition energy in a single quantum dot is now

$$\Delta E = \frac{e^2}{8\epsilon_r\epsilon_0 r} + \frac{\hbar^2}{m^* r^2}. \tag{7.7}$$

In a strained silicon dot the addition energy is very sensitive to the dot size, as shown in Fig. 7.6. From the graph we can see that the dominant component of the addition energy is the charging energy for a dot size over a few nm. For a dot size of r = 100 nm, the estimated addition energy is around 2 meV. In real quantum dot devices with complex structures and interfaces, the dot is coupled to nearby source, drain and gates rather than isolated. For side-gated devices surrounded by trenches, the interfaces also have a strong effect. The general form of the dot capacitance can

be written as

$$C_{dot} = C_{source-dot} + C_{drain-dot} + C_{gate}. \tag{7.8}$$

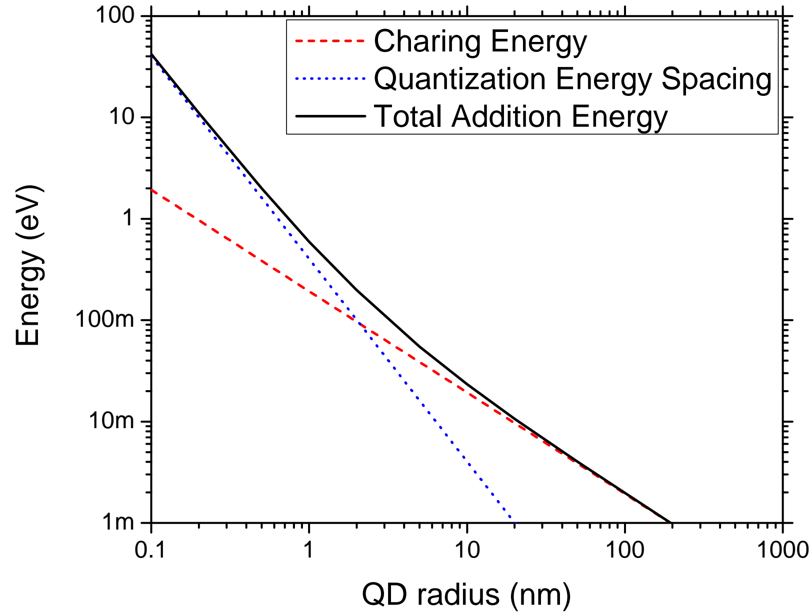


Figure 7.6: Addition energy in a silicon quantum dot and its components of charging energy and quantization energy spacing as a function of dot size.

Finally we list the three criteria that have to be met to achieve observable Coulomb blockade:

1. The source-drain bias voltage can't exceed the addition energy.
2. The thermal energy $k_B T$ must be below the addition energy, or else electrons will be able to suppress blocking via thermal excitation.
3. The tunneling junction resistance should be greater than h/e^2, which is a result from the uncertainty principle.

7.3.2 A Single Quantum Dot Device

As the final quantum dot device application of this thesis, we will describe a single quantum dot device characteristics. The fabrication details and a SEM image were discussed in Section 7.2.2. Electrical measurements were conducted at 30 mK in a dilution refrigerator by Professor Leonid Rokhinson's laboratory at Purdue University.

In the original quantum dot design, the two pairs of split gates on the sides were intended to be used for controlling the tunneling junction and define the central dot area, with one pair each is placed on the source and drain sides. However, in the measurement we encountered great difficulties in locating the exact dot. When any of two pairs of the split gates were applied a fixed voltage, sweeping voltage on the remaining pair of split gate would show similar conductance oscillation behavior. We think this could be caused by three possible problems. First, as shown in Fig. 7.4, our tunneling junctions are normally "off". So there could be many possible tunnel junctions in the narrow etch-defined region even without the side gates, the tunnel barriers in these junction will be high enough. If this is true, any pair of the split gates could define a quantum dot if there are two tunneling junctions close enough on both the source and the drain sides. Second, our achieved mobilities in these samples are still low so that the electron mean free path is less than 100 nm. The inelastic scatterings may be significant within the quantum dot area and effectively alter the dot size. Third, this particular single quantum dot sample #4811 was etched only by RIE, the surface depletion and possible defects from the ion damage will form a lot of charge traps. Such traps could also change the dot geometry significantly. Moreover, the conductance blockade in our measurement showed a lot of parasitic patterns such as missing or extra peaks as well as hysteresis due to the existence of the excess electron traps.

Fig. 7.7 shows typical conductance oscillations through the quantum dot as the voltage on one pair of side split gates is varied. The source-drain bias was held

constant at V_{DS} = 10 mV. When the gate voltage on the dot is less than –0.5 V, we did not observe any channel conductance which suggests there is no electron on the dot. As the gate voltage increases, both scans exhibit a few initial oscillation peaks with similar positions and linewidths. We believe that these successive peaks correspond to an increment of one electron in the dot [129]. After passing about eight quantized electron states on the dot, we find many parasitic peaks and strong hysteresis from the two scans, presumably due to the increased electron interactions between the electrons on the dot with the surrounding environment as well as among themselves.

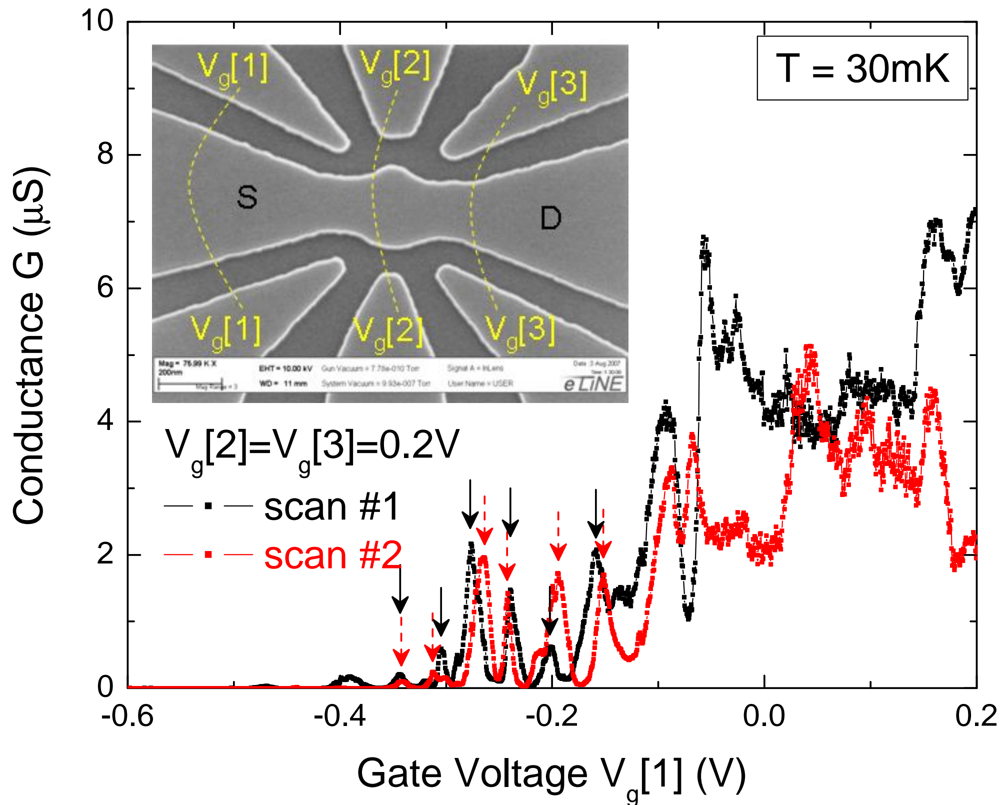


Figure 7.7: Quantum dot conductance oscillations as the gate voltage on split gate $V_g[1]$ is varied with zero magnetic field at T = 30 mK. The arrows indicate the positions of conductance peaks that were included to calculate the gate capacitance.

To further study the gate capacitance in our single quantum dot devices, we choose to fit the first six conductance oscillations from both scans with a Lorentz broadening model. The underlying equation for data fitting is

$$G = G_0 + \frac{2A_i}{\pi} \frac{w_i}{4(V - V_{ci})^2 + w_i^2}, i = 1, 2, \ldots, 6, \quad (7.9)$$

where G is the conductance axis and V is the gate voltage axis.

We assume $G_0 = 0$ for both curves. The fitted V_{ci} and w_i correspond to the peak positions and their full width at half magnitude (FWHM), respectively. Table 7.1 summarizes the numerical results. The average spacing between consecutive peaks ΔV_g is about 36 mV, which is governed primarily by the gate capacitance

$$C_{gate} = \frac{e}{\Delta V_g} = 4.4\ aF. \quad (7.10)$$

Table 7.1: Fitted curve parameters of quantum dot conductance oscillation peaks (All units are in Volts).

	Scan #1			Scan #2		
i	V_i	FWHM w_i	$\lvert V_i - V_{i-1}\rvert$	V_i	FWHM w_i	$\lvert V_i - V_{i-1}\rvert$
1	-0.3436	0.0052		-0.3415	0.0041	
2	-0.3043	0.0041	0.0393	-0.3115	0.0044	0.0300
3	-0.2754	0.0119	0.0289	-0.2659	0.0130	0.0356
4	-0.2383	0.0071	0.0371	-0.2418	0.0044	0.0241
5	-0.2020	0.0048	0.0363	-0.1952	0.0146	0.0466
6	-0.1568	0.0242	0.0452	-0.1510	0.0108	0.0442
Average	$\lvert\Delta x_i\rvert = 0.037 \pm 0.006$			$\lvert\Delta x_i\rvert = 0.036 \pm 0.009$		

The resulting gate capacitance is on the order of 11 aF reported in a similar etch-defined six side-gate dot by other groups [130]. Due to the charge noise and poor stability in this particular single quantum dot device, we were not able to further identify Coulomb blockade diamonds [129] by varying both side-gate voltages and the source-drain voltages simultaneously, which prevents us from experimentally extrapolating the total dot capacitance and the addition energy.

In the six-gate dot fabrication work [130], it was also noted that the CF_4 etch which we used as well can cause a higher density of trapping states, and a correspondingly larger depletion width. Although we performed regrowth and the work [130] did not, any etch damage defects below the surface would not be removed by passivation (excpet perhaps the thermal annealing effect of the pre-expitaxial cleaning step). We believe that the lack of precise surface control is our current limiting factor that led to suppression of Coulomb blockade. We anticipate that improvements in dry etching technique facilitated by a shallow wet-etch will enable continued progress towards clean quantum dot devices.

7.4 Summary

With respect to technology, we have developed a versatile side-gated strained Si/SiGe quantum dot devices fabrication process. Two rudimentary types of device applications are presented as prototype of functionality that exhibits significant quantum effects: the quantum point contact (QPC) and the single quantum dot.

A single QPC device was fabricated with selective wet etch and Si/SiGe epitaxial regrowth. The channel can be fully depleted with negative gate voltage beyond –2 V. Strong evidence of 1-D quantization in the QPC channel was identified, as more positive gate voltage applied the conductance showed steplike conductance characteristics. The poor electron mean free path in our 2DEG samples will require a fabrication resolution well below 100 nm to achieve ballistic transport. With the successful demonstration of the QPC, we can use multiple side-gates close to a quantum dot to tune the electrostatic potential on the dot as well as the tunnel couplings between the dot and its source and drain. Successful pinch-off of all side gating in a six-gate quantum dot geometry were demonstrated, while the source-drain transport conductance $< e^2/h$ can be maintained so that the dot was weakly coupled with

tunnel junctions to the source and drain.

In the six side-gate single quantum dot device, we observed channel conductance blockade behavior with periodic oscillation peaks while sweeping each pair of split gates and keeping all other gate voltages constant. This is a direct result of Coulomb blockade effect, in which the addition energy of the dot is much larger than the source-drain bias and the thermal energy so that single electron tunneling can only occur within certain energy level alignment. By calculating the gate voltage spacings between adjacent conductance peaks, we estimated a typical gate-to-dot capacitance of about 4.4 aF for each pair of side gates. The detailed Coulomb blockade diamond characteristics was suppressed by the excess parasitic charge noise and hysteresis of different scans. Thus the surface passivation by Si/SiGe epitaixal regrowth itself may not be sufficient to remove the ion damage and surface depletion arising from the use of RIE, low-damage dry etch chemistry and/or the use of a shallow wet etch is desirable for future quantum dot device applications.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

The motivation of this work is to explore the physical realization of a silicon-based electron spin-based quantum computer to meet the ever-growing computation and information processing needs. We focus on the epitaxial growth and nanofabrication technologies for modulation-doped Si/SiGe heterostructures because of their straightforward potential towards large-scale integration and manufacturing. The main contribution of this work is threefold. First, we developed a complete growth and fabrication flow for both mesoscopic physics studies and quantum dot device applications in Si/SiGe heterosturctures. Second, we experimentally fabricated and studied electron transport in double quantum well 2DEG structures. They are good candidates of quantum dimers for the physical implementation of a scalable architecture map of qubit devices. Third, we demonstrated the three-dimensional confinement and surface passivation of quantum dot devices with a novel Si/SiGe epitaxial regrowth technique. In addition, uniform high-κ gate dielectric deposition was developed for additional passivation and top-gating.

Three similar but distinctive Si/SiGe epitaxy cycles have been implemented and

optimized for their roles at different fabrication stages. The growth of SiGe relaxed buffers is optimized for low dislocation density while maintaining a high throughput by our collaborators at AmberWave Systems. At Princeton, the growth of the modulation-doped Si/SiGe heterostructures is optimized for 2DEG that allows meaningful transport properties without sacrificing electron density depending on specific desired quantum devices applications. The growth conditions for the final epitaxial regrowth passivation require minimal thermal treatment and deleterious interfacial effects. The main challenge for devices fabrication process remains in the development of a viable etching technique for high anisotropy and low damage. While existing reactive ion dry etching is the most prevalent and advanced choice, we feel the urgent need for a breakthrough with non-selective etch chemistry with regard to SiGe and possible inclusion of a shallow wet etching.

On the new scalable architecture map for implementation of the Loss-DiVicenzo silicon-base quantum computer, our key contribution is the proposed concept of 3-D confined "double quantum dot" dimers that can eliminate gating for precise control of exchange couplings in a qubit array. We presented a theoretical study of the band alignment and the interwell interactions in two possible double quantum well structures. A negative transconductance effect was observed experimentally in a top-gated asymmetric double quantum well to show a strong evidence of interactions between the delocalized electrons in the two wells. At present, more understanding of the double quantum well interactions and the transport properties is required before the dimers can be integrated in the arrangement of many qubits.

Finally, a pseudomorphic epitaxial step by Si/SiGe epitaxial regrowth is demonstrated for device surface passivation and 3-D confinement of quantum dot devices. Such a epitaxial regrowth can provide a conduction band discontinuity at the strained Si/regrown SiGe interfaces and in principle avoid surface states and electrically active defects. We also developed a low temperature atomic layer deposition of Al_2O_3 rou-

tine that enables final surface passivation and top gating in addition to existing side gating. Quantum dot devices applications such as quantum point contacts and single electron transistors based on nanolithography and Si/SiGe exitaxial regrowth were demonstrated. The observation of single electron tunneling effect certainly shows significant prospects for future fabrication of quantum computing circuits.

8.2 Future Work

We already addressed many of the possible future directions throughout this thesis. In the following section, we will list some of these aspects that are of considerable research interest.

8.2.1 Short-term Outlook

This thesis raised some specific issues concerning our Princeton RTCVD system. It is clear that background doping limits our achieved electron mobilities, we have to adapt improvements by modifying growth conditions, introducing new silicon/germanium gas precursors, and hardware upgrades such as additional gas purification. The *in situ* etching with chlorine-based gas chemistry is also worth closer investigations. With a better understanding of selectivity and the etching mechanism, it may be possible to overcome the roughness problem and develop a reproducible cleaning procedure for growth and regrowth with superior interfacial qualities.

Further assistance from experiments is needed to harness double quantum wells for exchange interactions of electrons. These experiments should follow and focus on magneto-transport measurement, from which the individual electron densities and mobilities in the double wells can be derived directly. In addition, by introducing a SiGe alloy with a small amount of Ge in one of the double quantum wells (Fig. 8.1), we hope to find extra signatures of electrons in the two quantum wells. The electrons

confined in the $Si_{0.95}Ge_{0.05}$ should have a much lower mobility, if the alloy scattering other than the Coulombic scattering limits the mobility. Therefore a larger negative transconductance effect can be expected. Also electrons in the double quantum wells should have very different g-factor shift with respect to the direction of external magnetic field, so electron spin resonance spectrum can also be a convenient tool to monitor electron occupancy in the two wells.

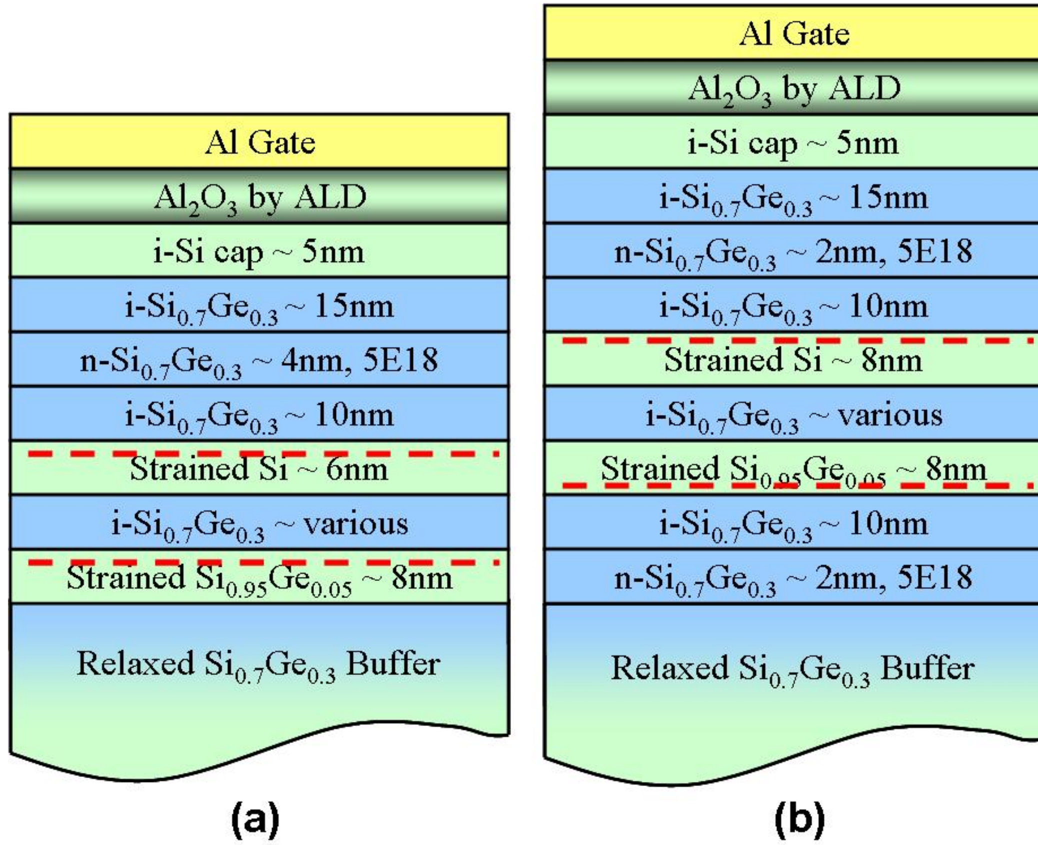


Figure 8.1: Schematic view of layer structures of two gated double quantum well systems with one SiGe alloy well: (a) asymmetric DQW with only one supply layer, (b) symmetric DQW with double supply layers.

The final concern is the successful fabrication of quantum dots, either based on single quantum well 2DEG (for qubit) or double quantum well 2DEGs (for interation dimer), as the implementation of our "flying qubit" architecture or essentially any silicon-based quantum computers will rely on such building blocks. Quantum point contacts or similar 1-D conducting wires with various width shall be first studied for

better control of edge depletion and any other surface effects. Consequently, we hope that we can remove the surface depletion and avoid the parasitic and hysteresis effects in quantum dot and observe Coulomb blockade diamonds.

Fig. 8.2 shows a prototype device of a more ambitious double quantum dot. The device consists of a central dot of vertical double quantum wells, a top gate for tuning the interaction between the two wells, and three side gates (or alternatively, using a more complicated six-gate geometry) for tuning the tunneling junctions and the electrostatic potential of the dot. For simplicity, the Si/SiGe epitaxial regrowth passivation is not shown. While either top-gating nor side-gating is not required for the interaction dimers for our "flying qubit", the versatility will be potential useful for study many-body physics, for example, the direct measurement of symmetric anti-symmetric splitting, and electron spin-relaxation times in such a two-level system.

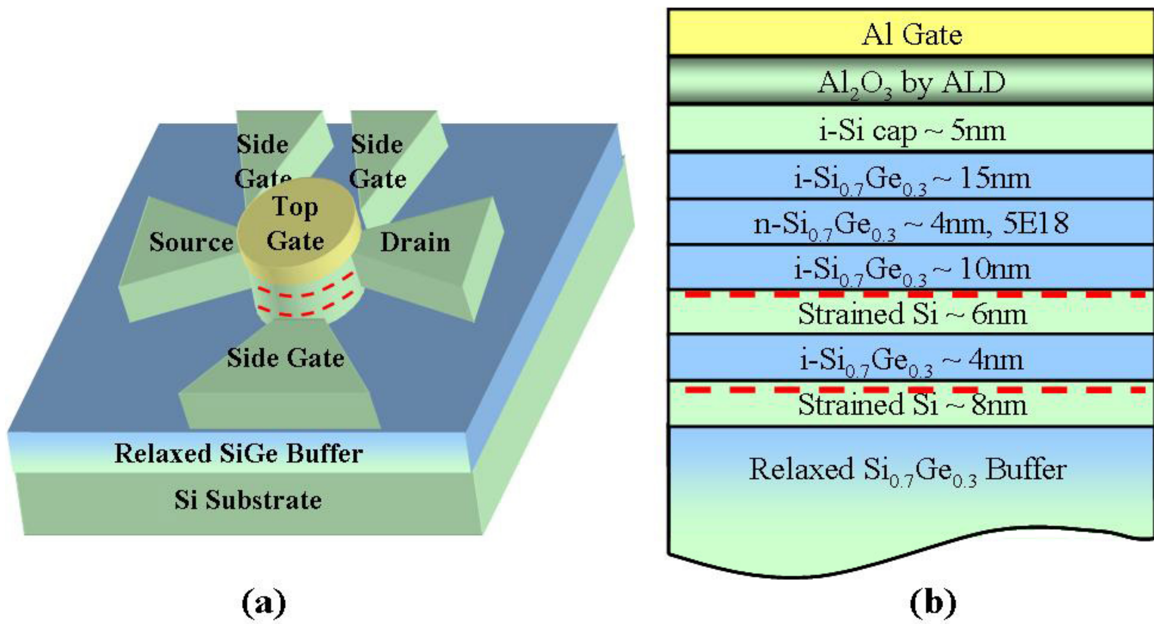


Figure 8.2: (a) Top-view of a double quantum dot based interaction dimer device. (b) Schematic, cross-sectional view of the central quantum dot in the interaction dimer device.

8.2.2 Long-term Outlook

In this thesis our emphases are on epitaxy and nanofabrication for the side gating of modulation-doped Si/SiGe heterostructures for implementation of silicon-based qubit and quantum devices. Meanwhile the other different, but similarly promising Schottky top-gating approach has made considerable progress. Our fabrication techniques, in particular, the Si/SiGe epitaxial regrowth and ALD Al_2O_3 passivation, could definitely be implemented in top-gated quantum dot devices as well. As one example, Fig. 8.3 shows a novel multiple quantum dots defined by Schottky gating across a nanowire of Si/SiGe modulation-doped heterostructures. The use of Si/SiGe epitaxial regrowth prior to the gate fabrication will provide a sharp 3-D confinement to electrons in the nanowire due to conduction band discontinuity, and also a surface passivation to eliminate defects and interface states. It might be simpler to implement than the quantum dot structures described in Chapter 7 because it does not depend on the properties of a narrow gap, making e-beam lithography and etching easier in practice because of a more tolerable process window.

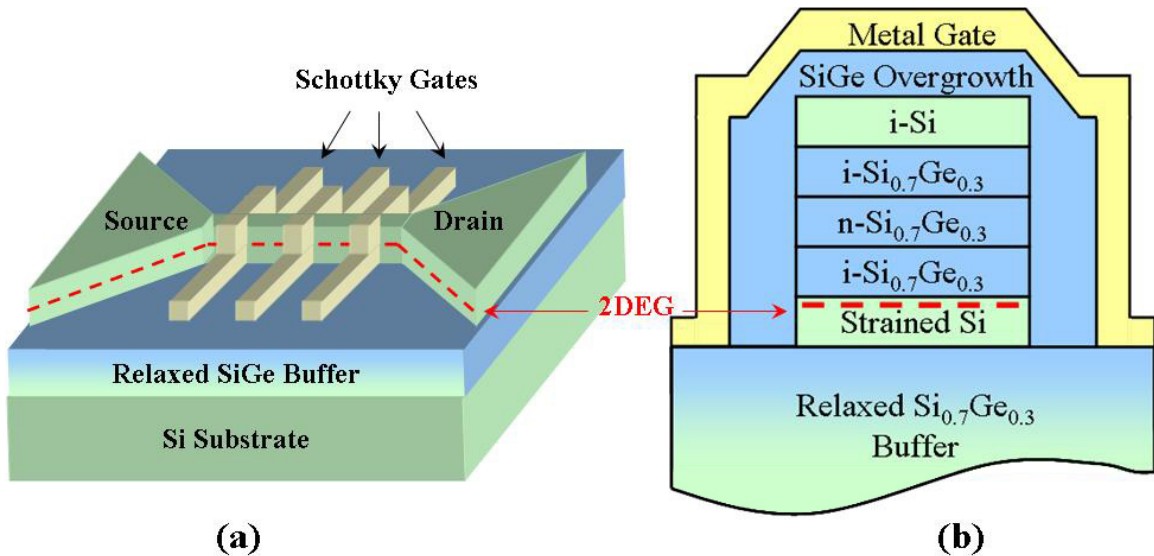


Figure 8.3: (a) A multiple quantum dots device defined by Schottky finger gates on a nanowire. (b) Schematic view of the Si/SiGe heterostructure nanowire with epitaxial regrowth passivation.

With the successful realization of two-level quits and the logic operations of these qubits, the experimental results should help us to answer two critical questions about the ultimate feasibility of electron spin-based quantum computing. The first one is a fundamental physics question: what is the quantum decoherence time in these Si/SiGe qubits? Given this much sought quantity, we can then turn to the second technology question: can we achieve an error rate low enough for precise control of exchange interactions of these qubits? The answer to the second question will depend on high-speed pulses and voltage amplitude control of the gates. For example, for a target rate error rate of 10^{-5} or less per gate, controlling the exchange will require pulse edges to be defined to better than 10^{-5} of the decoherence time with gate amplitude switched to approximately less than 50 dB of the peak. With favorable answers to both questions, we are confident that all of the five Loss-DiVincenzo's criteria can be met and quantum computing will no longer be a fantasy or mirage.

If indeed a quantum computer is fantasy or mirage beyond what we can currently envision, the rich variety of phenomena in the field is still sure to be a source of inspiration for the future.

> 'Would you tell me, please, which way I ought to go from here?'
>
> 'That depends a good deal on where you want to get to,' said the Cat.
>
> 'I don't much care where–' said Alice.
>
> 'Then it doesn't matter which way you go,' said the Cat.
>
> '– so long as I get SOMEWHERE,' Alice added as an explanation.
>
> 'Oh, you're sure to do that,' said the Cat, 'if you only walk long enough.'

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Appendix A

Sample RTCVD Growth Sequences

A.1 Introduction

Our Princeton RTCVD system is controlled using the AzeoTech DAQFactory software. Each hardware input/output interface is defined as a channel in the software, be it analog I/O (AI, AO), or digital I/O (DI, DO). The channels are monitored and controlled by sequences, which are basically a scripting programming language for data acquisition. The sequences can also use PID loops to automatically control the process variables based on different set-points (SP). This appendix provides the RTCVD growth sequences for two sample structures discussed in this thesis (modulation-doped Si/SiGe asymmetric double quantum wells and Si/SiGe regrowth on patterned devices). All growth start with an initialization routine sequence 0 and end with a shut-down routine sequence 7. Only the actual growth sequences 1 and 6 are given.

A.2 Growth Sequences #4822: Asymmetric Double Quantum Well

intrinsic Si ∼ 4nm
intrinsic $Si_{0.7}Ge_{0.3}$ ∼ 12 nm
n-doped $Si_{0.7}Ge_{0.3}$ ∼ 4 nm, 5×10^{18} cm^{-3}
intrinsic $Si_{0.7}Ge_{0.3}$ ∼ 10 nm
intrinsic Si ∼ 7 nm
intrinsic $Si_{0.7}Ge_{0.3}$ ∼ 6 nm
intrinsic Si ∼ 8 nm
intrinsic $Si_{0.7}Ge_{0.3}$ ∼ 80 nm
relaxed SiGe buffers and substrate

for comments only

```
// Sequence_1
EndSeq SEQUENCE_0
// call for growth squence
SP2 = 0
BeginSeq Sequence_6
WaitFor SP2 > 0.5, 0.300
EndSeq Sequence_6
BeginSeq SEQUENCE_7

// Sequence_6
// cold transmission acquisition
STATUS_MESSAGE = “PRESS SOFT_GO for Cold Values”
WaitFor SOFT_GO > 0.5, 0.300
```

SP3 = 1

Wait 1

SP3 = 0

// raise pressure to max

AO00_MAIN = 1 — *H_2 flow = 5 slpm*

AO08_PRESS = 0 — *butterfly valve fully open*

// pre-flow process gases

STATUS_MESSAGE = "Pre-flow Process Gases"

AO06_DCS = 0.534 — *DCS flow = 26 sccm*

DO07_DCS_SEL = 1

AO02_GeH4 = 0.45 — *GeH_4 flow = 225 sccm*

DO03_GeH4_SEL = 1

AO05_PH3_LOW = 0.2 — *PH_3 flow = 2 sccm*

DO05_PH3_SEL = 1

// 900C clean

STATUS_MESSAGE = "Ramp Up Lamp"

SP4 = 0

RAMP_GOAL = 0.24 — *Lamp power = 24%*

RAMP_RATE = 0.1

BeginSeq RAMP_SP7

WaitFor SP1 > 0.5, 0.300

STATUS_MESSAGE = "Baking"

Var.wait_time = 300

Wait 300 — *5 minutes baking*

// pump down and ramp down

STATUS_MESSAGE = "Pump Down and Ramp Down Lamp"

AO00_MAIN = 0.618 — *H_2 flow = 3 slpm*

AO08_PRESS = 0.6 *main pressure = 6 Torr*

Wait 15

SP1 = 0

RAMP_GOAL = 0.16

RAMP_RATE = -0.2

BeginSeq RAMP_SP7 WaitFor SP1 > 0.5, 0.300

Wait 5

// grow SiGe

SP5 = 2.941 *set point for* $T = 625\,^{\circ}C$

SP4 = 1

STATUS_MESSAGE = "Press SOFT_GO for 625C Growth"

WaitFor SOFT_GO > 0.5, 0.300

STATUS_MESSAGE = "Growing SiGe buffer"

DO13_DCSandSi2H6_INJ = 1 *DCS inject on*

Wait 10

DO10_GeH4_INJ = 1 GeH_4 *inject on*

Var.wait_time = 400

Wait 400 *400 seconds SiGe growth*

DO10_GeH4_INJ = 0 GeH_4 *inject off*

Wait 15

// grow Si

SP5 = 4.294 *set point for* $T = 750\,^{\circ}C$

STATUS_MESSAGE = "Growing Si channel"

Var.wait_time = 50

Wait 50 *50 seconds Si growth*

// grow SiGe

SP5 = 2.941 *set point for* $T = 625\,^{\circ}C$

STATUS_MESSAGE = “Press SOFT_GO for 625C Growth”

WaitFor SOFT_GO > 0.5, 0.300

STATUS_MESSAGE = “Growing SiGe spacer”

DO10_GeH4_INJ = 1 *GeH_4 inject on*

Var.wait_time = 30

Wait 30 *30 seconds SiGe growth*

DO10_GeH4_INJ = 0 *GeH_4 inject off*

Wait 10

// grow Si

SP5 = 4.294 *set point for $T = 750\,^{\circ}C$*

STATUS_MESSAGE = “Growing Si channel”

Var.wait_time = 40

Wait 40 *40 seconds Si growth*

// grow SiGe

SP5 = 2.941 *set point for $T = 625\,^{\circ}C$*

STATUS_MESSAGE = “Press SOFT_GO for 625C Growth”

WaitFor SOFT_GO > 0.5, 0.300

STATUS_MESSAGE = “Growing SiGe spacer”

DO10_GeH4_INJ = 1 *GeH_4 inject on*

Var.wait_time = 50

Wait 50 *50 seconds SiGe growth*

STATUS_MESSAGE = “Growing n+SiGe supply”

DO12_PH3_INJ = 1 *PH_3 inject on*

Var.wait_time = 20

Wait 20 *20 seconds n-doping*

DO12_PH3_INJ = 0 *PH_3 inject off*

STATUS_MESSAGE = “Growing i-SiGe cap”

Var.wait_time = 60

Wait 60 *60 seconds SiGe growth*

DO10_GeH4_INJ = 0 *GeH_4 inject off*

Wait 15

// grow Si

SP5 = 4.294 *set point for $T = 750\,^\circ C$*

STATUS_MESSAGE = "Growing Si cap"

Var.wait_time = 20

Wait 20 *20 seconds Si growth*

// close process gases

STATUS_MESSAGE = "Shutting Down Growth Squence"

DO13_DCSandSi2H6_INJ = 0 *DCS inject off*

SP4 = 0

// ramp down

STATUS_MESSAGE = "Ramp Down Lamp"

SP1 = 0

RAMP_GOAL[0] = 0.0

RAMP_RATE[0] = -0.3

BeginSeq RAMP_SP7 WaitFor SP1 > 0.5, 0.300

DO05_PH3_SEL = 0

DO03_GeH4_SEL = 0

STATUS_MESSAGE = "Done with Growth Squence"

SP2 = 1 *return to SEQUENCE_1*

A.3 Growth Sequences #4827: Epitaxial regrowth on #4811-Quantum Dot

intrinsic Si ~ 4 nm
intrinsic $Si_{0.7}Ge_{0.3}$ ~ 60 nm
#4811 Quantum Dot Patterns
relaxed SiGe buffers and substrate

for comments only

```
// Sequence_1
EndSeq SEQUENCE_0
// call for growth squence
SP2 = 0
BeginSeq Sequence_6
WaitFor SP2 > 0.5, 0.300
EndSeq Sequence_6
BeginSeq SEQUENCE_7

// Sequence_6
// cold transmission acquisition
STATUS_MESSAGE = "PRESS SOFT_GO for Cold Values"
WaitFor SOFT_GO > 0.5, 0.300
SP3 = 1
Wait 1
SP3 = 0
// raise pressure to max
AO00_MAIN = 1                                   H2 flow = 5 slpm
```

AO08_PRESS = 0 *butterfly valve fully open*

// pre-flow process gases

STATUS_MESSAGE = "Pre-flow Process Gases"

AO06_DCS = 0.534 *DCS flow = 26 sccm*

DO07_DCS_SEL = 1

AO02_GeH4 = 0.45 *GeH_4 flow = 225 sccm*

DO03_GeH4_SEL = 1

// 800C clean

STATUS_MESSAGE = "Ramp Up Lamp"

SP4 = 0

RAMP_GOAL = 0.23 *Lamp power = 23%*

RAMP_RATE = 0.1

BeginSeq RAMP_SP7

WaitFor SP1 > 0.5, 0.300

STATUS_MESSAGE = "Baking"

Var.wait_time = 120

Wait 120 *2 minutes baking*

// pump down and ramp down

STATUS_MESSAGE = "Pump Down and Ramp Down Lamp"

AO00_MAIN = 0.618 *H_2 flow = 3 slpm*

AO08_PRESS = 0.6 *main pressure = 6 Torr*

Wait 15

SP1 = 0

RAMP_GOAL = 0.16

RAMP_RATE = -0.2

BeginSeq RAMP_SP7 WaitFor SP1 > 0.5, 0.300

Wait 5

// grow SiGe

SP5 = 2.941 *set point for* $T = 625\,^{\circ}C$

SP4 = 1

STATUS_MESSAGE = “Press SOFT_GO for 625C Growth”

WaitFor SOFT_GO > 0.5, 0.300

STATUS_MESSAGE = “Growing SiGe cap”

DO13_DCSandSi2H6_INJ = 1 *DCS inject on*

Wait 10

DO10_GeH4_INJ = 1 GeH_4 *inject on*

Var.wait_time = 300

Wait 300 *5 minutes SiGe growth*

DO10_GeH4_INJ = 0 GeH_4 *inject off*

Wait 15

// grow Si

SP5 = 3.554 *set point for* $T = 700\,^{\circ}C$

STATUS_MESSAGE = “Growing Si cap”

Var.wait_time = 90

Wait 90 *90 seconds Si growth*

// close process gases

STATUS_MESSAGE = “Shutting Down Growth Squence”

DO13_DCSandSi2H6_INJ = 0 *DCS inject off*

SP4 = 0

// ramp down

STATUS_MESSAGE = “Ramp Down Lamp”

SP1 = 0

RAMP_GOAL[0] = 0.0

RAMP_RATE[0] = -0.3

BeginSeq RAMP_SP7 WaitFor SP1 > 0.5, 0.300

DO03_GeH4_SEL = 0

STATUS_MESSAGE = "Done with Growth Squence"

SP2 = 1 *return to SEQUENCE_1*

Appendix B

Sample Structures Numerically Solved by 1D Poisson Program

B.1 Introduction

In this appendix we provide input files for two sample structures that were numerically solved by the 1D Poisson Program: the top-gated modulation-doped Si/SiGe heterostructure (solve for Poisson's equation only) and the symmetric double quantum well (solve Poisson and Schrödinger equations self-consistently). The FreeWare program we used is PC version beta 8c. The following three new materials must be added to the original materials datafile before the sample input files can run (all band offset parameters are relative to the $Si_{0.7}Ge_{0.3}$ bulk):

	SiGe	s-Si	Al2O3
	$Si_{0.7}Ge_{0.3}$ bulk	strained Si	Al_2O_3
Energy gap (eV)	1.04	0.92	7.00
Conduction band offset (eV)	0	-0.18	2.50
Relative dielectric constant	13.13	11.7	9.0
Electron effective mass (m_0)	0.328	0.19	1
Conduction band degeneracy	6	2	6
Heavy hole effective mass (m_0)	0.49	0.49	1
Light hole effective mass (m_0)	0.16	0.16	1
Donor level (eV)	0.003	0.003	0.003
Acceptor level (eV)	0.01	0.01	0.005

B.2 Top-gated Modulation-doped Si/SiGe heterostructure Input File

Al_2O_3 = 90 nm
Si = 5 nm, background 10^{17} cm^{-3}
$Si_{0.7}Ge_{0.3}$ = 15 nm, background 10^{17} cm^{-3}
n-doped $Si_{0.7}Ge_{0.3}$ = 2 nm, 5×10^{18} cm^{-3}
$Si_{0.7}Ge_{0.3}$ = 15 nm, background 10^{17} cm^{-3}
Si = 10 nm, background 10^{17} cm^{-3}
$Si_{0.7}Ge_{0.3}$ = 100 nm, background 10^{17} cm^{-3}
intrinsic $Si_{0.7}Ge_{0.3}$ = 1μm
substrate

```
surface schottky=0 v1
Al2O3   t=900   no electrons      dy=1
```

s-Si t=50 Nd=1e17 dy=1

SiGe t=150 Nd=1e17 dy=1

SiGe t=20 Nd=5e18 dy=1

SiGe t=150 Nd=1e17 dy=1

s-Si t=100 Nd=1e17 dy=1

SiGe t=1000 Nd=1e17 dy=1

SiGe t=1um dy=10

substrate

fullyionized

v1 0.25 -2.25 -.25

temp=0.1K

B.3 Symmetric Si/SiGe Double Quantum Well Input File

$Si_{0.7}Ge_{0.3}$ = 27 nm
Si = 8 nm
$Si_{0.7}Ge_{0.3}$ = 4 nm
Si = 8 nm
$Si_{0.7}Ge_{0.3}$ = 27 nm
substrate

surface schottky=0 v1

SiGe t=150

SiGe t=20

SiGe t=100

s-Si t=80

SiGe t=40

s-Si t=80

SiGe t=100

SiGe t=20

SiGe t=150

substrate

fullyionized

v1 -1 0.2 0.1

dy=10

schrodingerstart=20

schrodingerstop=720

find quantized states

temp=4K

Appendix C

Publications and Presentations Resulting From This Thesis

C.1 Journal Articles and Conference Papers

1. K. Yao, M. Gaevski, J. C. Sturm, A. Chernyshov, L. P. Rokhinson, C. Mike, J-S. Park, J. G. Fiorenza, and A. Lochtefeld, “Effect of leakage in relaxed SiGe buffer layers on Si/SiGe quantum devices”, manuscript in preparation.

2. K. Yao, J. C. Sturm, and A. Lochtefeld, “Strained silicon two-dimensional electron gases on commercially available $Si_{1-x}Ge_x$ relaxed graded buffers”, in SiGe and Ge: Materials, Processing, and Devices, ECS Transactions, Volume 3, Issue 7, pp. 313-315 (2006).

3. K. Yao and J. C Sturm, “Nanopatterning of Si/SiGe two-dimensional hole gases by PFOTS-aided AFM lithography of carrier supply layer”, in Nanomanufacturing, Mater. Res. Soc. Symp. Proc. **921E**, 0921-T02-08 (2006).

C.2 Conference Presentations

4. K. Yao, M. Gaevski, J. C. Sturm, A. Chernyshov, L. P. Rokhinson, C. Mike, J-S. Park, J. G. Fiorenza, and A. Lochtefeld, "Effect of substrate doping in relaxed SiGe buffers on strained Si 2DEG quantum devices", American Physical Society March Meeting, Pittsburgh, USA (2009).

5. K. Yao, M. Gaevski, A. Chernyshov, L. P. Rokhinson, and J. C. Sturm, "Si/SiGe epitaxy for digital control of exchange interactions in a spin-based quantum computer", ARO/NSA/IARPA Quantum Computing & Quantum Algorithms Program Review, Buckhead, USA (2008).

6. K. Yao, M. Gaevski, A. Chernyshov, L. P. Rokhinson, and J. C. Sturm, "Epitaxially passivated strained silicon quantum dots", ARO/NSA/IARPA Quantum Computing & Quantum Algorithms Program Review, Minneapolis, USA (2007).

7. K. Yao, J. C. Sturm, and A. Lochtefeld, "Strained silicon two-dimensional electron gases on commercially available $Si_{1-x}Ge_x$ relaxed graded buffers", 210th Meeting of The Electrochemical Society (2nd International SiGe & Ge: Materials, Processing, and Device Symposium), Cancun, Mexico (2006).

8. K. Yao, L. P. Rokhinson, and J. C. Sturm, "Digital control of exchange interaction in a spin-based silicon quantum computer, – strained silicon two-dimensional electron gases and clean epitaxial regrowth", Quantum Computing & Quantum Algorithms Program Review, Buckhead, USA (2006).

9. K. Yao and J. C Sturm, "Nanopatterning of Si/SiGe two-dimensional hole gases by PFOTS-aided AFM lithography of carrier supply layer", Materials Research Society Spring Meeting, San Francisco, USA (2006).

C.3 NASA New Technology Report

10. E. M. Dons, G. S. Tompa, J. C. Sturm, and K. Yao, "Silicon germanium alloy photovoltaics for 1.06 Micron wireless power transmission", submitted and approved by NASA in 2006.