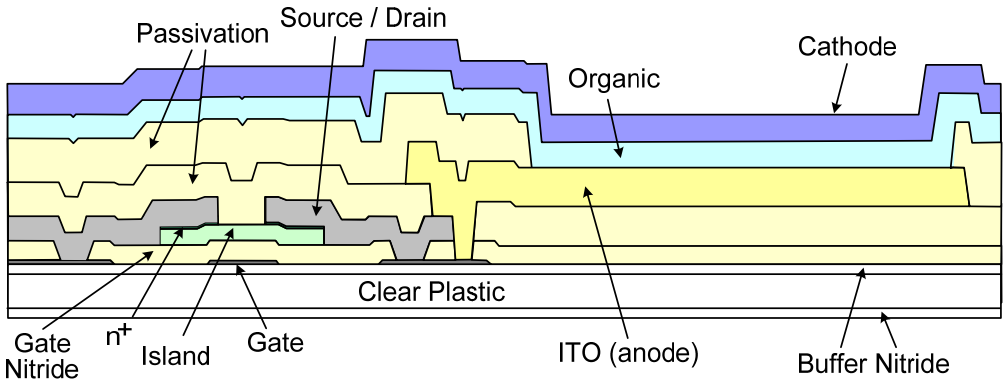
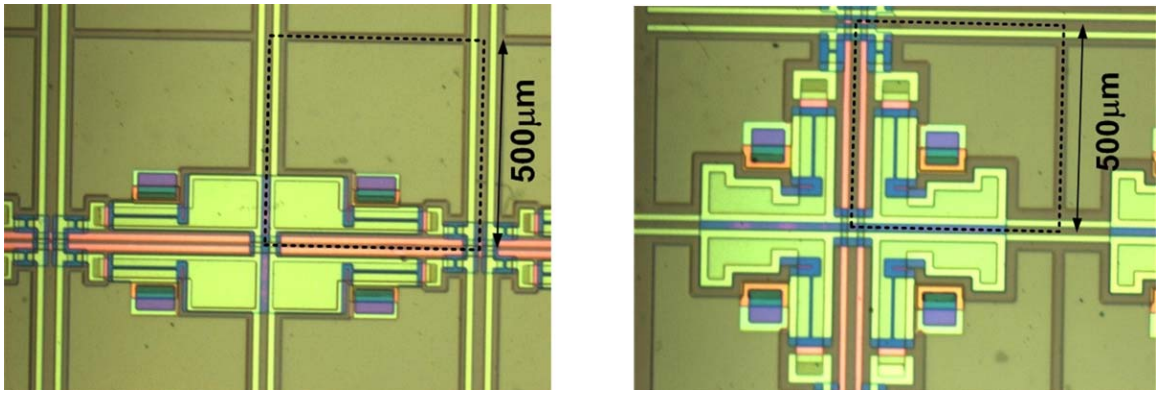


Fig. 4.3. Schematic cross-section of a 2-TFT AMOLED pixel fabricated in this work.

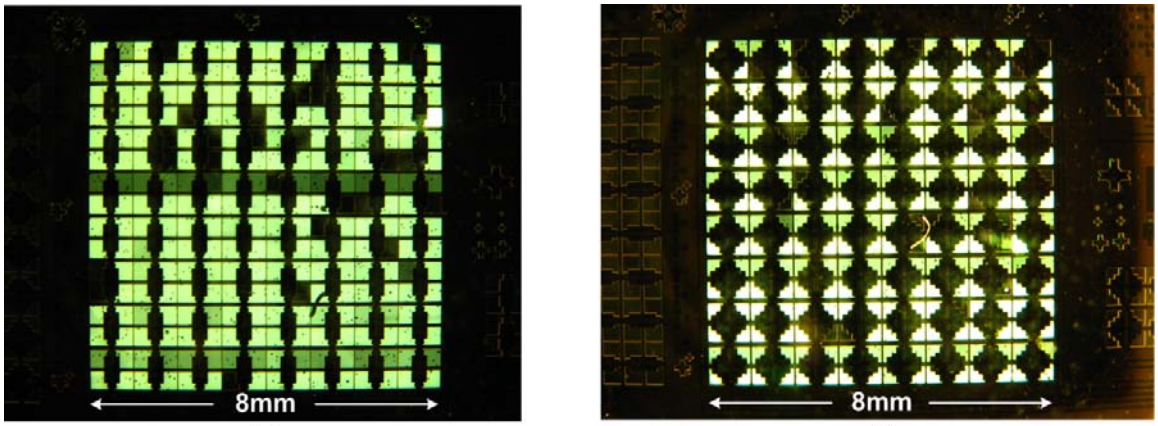
deposition has been optimized for best quality at 250°C for the 250°C and 285°C processes, and at 200°C for the 200°C process [12][13][14]. Dry etching is used next to pattern the *a*-Si:H islands and open contact vias to the bottom metal. The top metal (Cr/Al based) is then thermally evaporated and patterned by wet etching. The n^+ *a*-Si:H is then cut at the backside of the *a*-Si:H channel by dry etching, and the samples are annealed at 180°C for 1 hour to repair the dry etching damage to the channel. The backplane is then passivated by a 250nm-thick layer of *a*-SiN_x:H grown by PECVD at 125°C and dry-etching is used to open contact holes for ITO (OLED anode). Next, a 200nm-thick ITO layer is deposited at room temperature by DC-sputtering from an In_2O_3/SnO_2 target (with 90/10 weight ratio) in Ar/O_2 ambient and patterned by wet etching. A passivation layer is then deposited and patterned to cover the edges of ITO to avoid shorts between ITO and cathode in the OLED (evaporated subsequently). Dry etching is used next to open vias to the external pads in the passivation (not shown in the cross-section). Finally, the AMOLED structure is completed by the evaporation of small molecule green OLEDs through a pair of shadow masks for organic layers and cathode. The optical images of the arrays with 10μm and 20μm alignment tolerance prior to OLED evaporation are shown in Fig. 4.4 (a) and (b), respectively.

OLED evaporation was initially performed in Princeton University to develop the AMOLED fabrication process and conduct the primary characterization of the pixels. OLEDs used for this purpose were standard bi-layer small-molecule OLEDs with TPD (N,N'-Bis-(3-methylphenyl)-N,N'-diphenylbenzidine) hole transport layer (~3nm-thick) and Alq_3 (aluminum tris-(8-hydroxyquinoline)) electron transport/emissive layer (~3nm-



(a) (b)

Fig. 4.4. Optical micrographs of the arrays with (a) 10µm and (b) 20µm alignment tolerance prior to OLED evaporation. The dashed lines show the pixel boundaries.



(a) (b)

Fig. 4.5. Optical images of 16×16 AMOLED test arrays fabricated with (a) 10µm and (b) 20µm alignment tolerance on clear plastic using a TFT backplane process temperature of 250°C.

thick). Indium-tin-oxide (ITO) was used as the OLED anode (~80nm-thick) and Mg/Ag with 1/10 ratio (~10nm-thick) followed by 100nm-thick Ag layer as the cathode. After AMOLED process development with standard OLEDs, a high quality green phosphorescent OLED (PHOLED ™) [15][16] was used instead. The PHOLEDs were deposited at Universal Display Corporation (UDC) in collaboration with Dr. Kamala Rajan and Dr. Michael Hack.

Stress Engineering – Controlling the mechanical stress in the deposited layers is crucial in order to obtain a flat surface with crack-free layers, especially at high process temperatures (250°C and 285°C) where the dimensional change in the substrate becomes significant (even with the low coefficient of thermal expansion of the clear plastic

substrates). The mechanical stress in the PECVD-grown layers can be adjusted by the plasma power density as established by our group [17][18]. The buffer nitride layers on both sides of clear plastic are grown at a plasma power density of 200mW/cm^2 resulting in tensile films balancing out the stress levels in each other and laying out the passivated substrate flat. Both bottom and top metal layers are tri-layers of Cr/Al/Cr with thin and thus low-tensile-stress Cr layers (15nm) for adhesion and low-stress Al layers for sufficient conduction. The gate nitride and *a*-Si:H are deposited at plasma power densities of 22mW/cm^2 and 17mW/cm^2 respectively, resulting in compressive films. The n^+ *a*-Si:H layer grown at 17mW/cm^2 is tensile, similar to the top and bottom Cr layers, and balances out the stress from the compressive layers. The nitride passivation layer on the device side and the sputtered ITO are nearly stress-free. The overall result is a crack-free backplane with a flat surface, ready for OLED evaporation.

4.4 *Experimental Results*

The optical images of the 16×16 AMOLED test arrays fabricated with 10μm and 20μm alignment tolerance are shown in Fig. 4.5 (a) and (b), respectively. The TFT backplane process temperature for these arrays is 250°C. The process yields for the test arrays with 10μm and 20μm alignment tolerance shown here are about 75% and 85%, respectively. However, we found no overall correlation between the alignment tolerance and process yield for the two alignment tolerances tried experimentally. The yield loss does not reflect a fundamental issue and is mainly related to the typical limitations of laboratory scale processing equipment and environment. The inset in Fig. 4.8 shows a process yield of about 96% for an 8×8 AMOLED test array. We have characterized the AMOLED test arrays by measuring the DC and AC characteristics, as well as the reliability of light emission over time.

4.4.1 Pixel Characteristics

The pixel characteristics were investigated both prior and after the OLED evaporation. The backplane pixel was characterized by grounding the source of the driver TFT and measuring the pixel current while sweeping the data voltage at various select voltages (Fig. 4.6 (a)). The overlapping part of the curves shows the output characteristics of

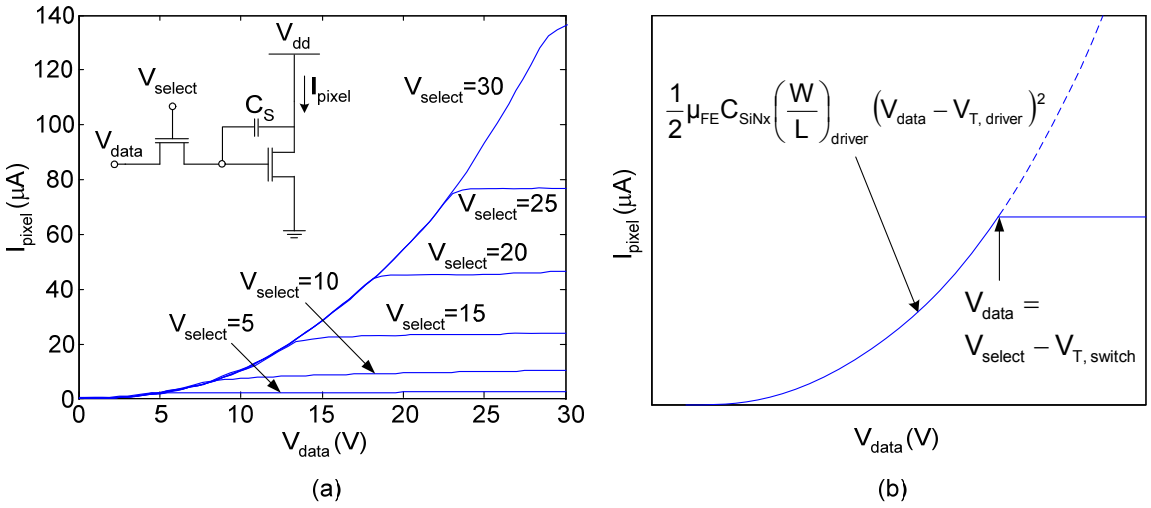


Fig. 4.6. (a) The DC output characteristics of the 2-TFT pixel backplane (prior to OLED evaporation) with the source of the driver TFT grounded as shown in the inset, and (b) the illustration of the ideal output characteristics of the 2-TFT pixel assuming the switching TFT is an ideal switch with no subthreshold as explained in the text.

driver TFT in saturation, while the non-overlapping parts reflect the subthreshold characteristics of the switching TFT. This can be most simply explained by assuming that the switching TFT is an ideal switch, i.e. if $V_{GS,\,switch} > V_{T,\,switch}$ the switching TFT is in the ON state, and if $V_{GS,\,switch} < V_{T,\,switch}$ it is in the OFF state (Fig. 4.6 (b)). Therefore if $V_{data} < V_{select} - V_{T,\,switch}$ the switching TFT is ON and the data voltage is transferred to the gate

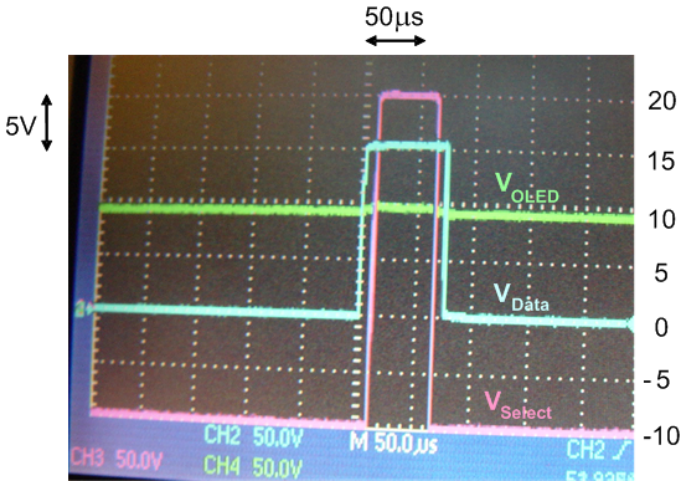


Fig. 4.7. AMOLED pixel QVGA leakage test prior to OLED evaporation with a 1MΩ resistor to simulate the OLED. The voltage drop across the resistor during a frame time is negligible confirming efficient charge storage.

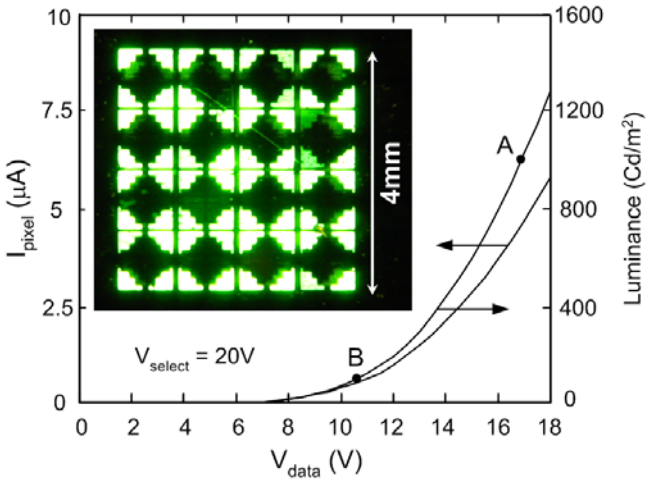


Fig. 4.8. DC output characteristics of an AMOLED pixel fabricated on clear plastic. The inset shows an image of an 8×8 AMOLED test array fabricated on clear plastic at 250°C.

of the driver TFT, i.e. $V_{GS,\ driver} = V_{data}$. But if $V_{data} \geq V_{select} - V_{T,\ switch}$ the switching TFT remains in the ON/OFF transition state and $V_{GS,\ driver} = V_{select} - V_{T,\ switch}$. In practice, the switching TFT is not an ideal switch and therefore in the latter case it operates in the subthreshold mode. As a result, the gate voltage of the driver TFT increases slightly with increasing the data voltage as seen in the experimental data.

The backplane pixels were also tested with the QVGA signals to evaluate their charge storage capability. A 1MΩ resistor was used to simulate the OLED. Negligible

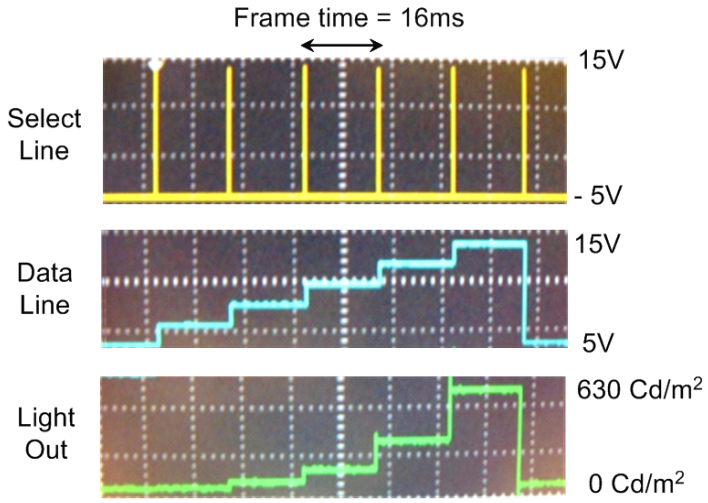


Fig. 4.9. QVGA timing of the pixel showing that the pixel brightness follows the program voltage on the data line, consistent with the DC output characteristics.

voltage drop on the resistor during a frame time indicates a low leakage current (primarily the off-current of the switching TFT) and efficient charge storage (Fig. 4.7).

The DC output characteristics of a finished AMOLED pixel are given in Fig. 4.8. A luminance intensity of 1000Cd/m^2 is obtained at a data voltage of 16.8V and corresponds to an OLED efficiency of 57Cd/A. The QVGA timing of the pixels shows sufficient voltage storage over the frame time (Fig. 4.9).

4.4.2 Electrical Reliability

The DC output characteristics of typical driving TFTs fabricated on clear plastic at 200°C and 285°C are plotted in Fig. 4.10. It is observed that the on-state drive current is not essentially affected by changing the process temperature. Both TFTs show an apparent (i.e. not corrected for contact resistance) effective mobility of 0.63cm^2/Vs and an apparent threshold voltage of 2.1V in the saturation regime. However, the lower gate leakage current for the 285°C process shows improvement in the quality of gate nitride at higher process temperatures. It should be noted that there are statistical variations in the mobilities and threshold voltages of the measured TFTs on all samples (Chapter 5). The two TFT characteristics plotted in Fig. 4.10 were intentionally chosen to have very close threshold voltages and mobilities to show that the on-state TFT characteristics are not particularly correlated with the process temperature provided that the growth conditions

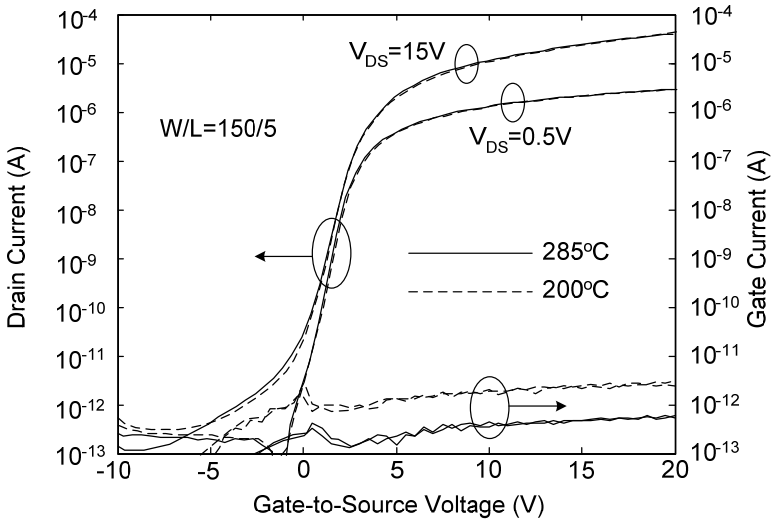


Fig. 4.10. DC output characteristics of the driver TFTs fabricated on clear plastic at 200°C and 285°C process temperatures.

for the TFT stack are optimized for each deposition condition.

The process temperature drastically affects the stability of AMOLED pixels. Each pixel was stressed at two different pixel currents corresponding to pixel luminance intensities of 1000Cd/m^2 and 100Cd/m^2 (points A and B marked on the luminance curve in Fig. 4.8). For each stress point, the bias voltages on the select line (20V) and data line (with values corresponding to the initial pixel luminance at points A and B) were kept constant and the pixel luminance was measured versus time. Fig. 4.11 (a) shows the luminance drop under the mentioned stress conditions for pixels processed at three process temperatures, 200°C, 250ºC and 285ºC. The luminance intensities are normalized to their initial values (100Cd/m^2 for stress point B and 1000Cd/m^2 for stress point A). In all curves, the pixel luminance drops over time. It is observed that for each process temperature, the luminance degradation is faster at stress point A than at stress point B, and more importantly degradation proceeds significantly faster at lower TFT process temperatures. Since the temperature is the only process variable, faster luminance degradation at lower TFT process temperatures may be attributed to a faster threshold voltage increase in the driver TFT, which reduces the pixel current accordingly. Note that

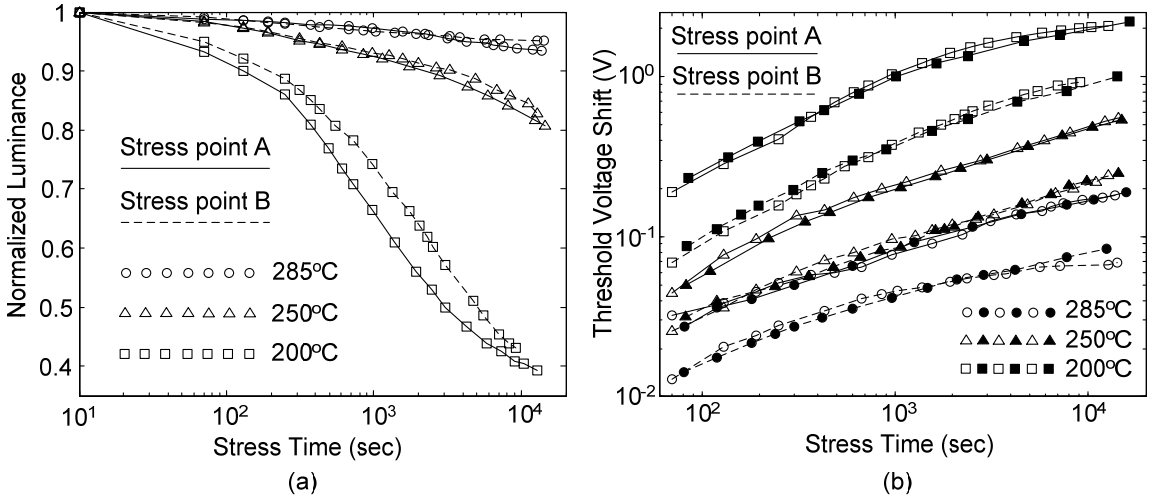


Fig. 4.11. (a) Luminance as a function of DC stress time for the AMOLED pixels fabricated at three process temperatures on clear plastic. The Stress points A and B correspond to the points marked on the luminance curve in Fig. 4.8 and (b) threshold voltage shift of the driver TFT as a function of DC stress time extracted from luminance data of part (a) assuming negligible OLED luminance degradation (empty symbols) and measured threshold voltage shift of individual test driver TFTs under the same DC bias stress (full symbols).

on this time scale, the effect of OLED luminance degradation is negligible due to the relatively long lifetime of the green phosphorescent OLED [15][16]. The faster drop at stress point A comparing to stress point B may be explained by the increased charge trapping in the gate nitride and defect creation in *a*-Si:H at higher gate voltages, resulting in a larger threshold voltage shift in the driving TFT. As observed in Fig. 4.11(a), the improvement in the pixel reliability at higher process temperatures is significant. After 4 hours of continuous stress, the pixel brightness drops to about 40% of its initial value for the 200°C process, while for the 285°C process the brightness drops to only about 95%. This result demonstrates the impact of increasing the process temperature on improving the reliability of AMOLED pixels. Such high process temperatures are not conventionally possible because of the thermal constraints of clear plastic substrates which limit the TFT process to low temperatures. Therefore new clear plastic substrates with thermal properties that allow processing at such high temperatures are essential to flexible bottom-emitting AMOLED displays based on *a*-Si:H.

To confirm that the luminance degradation of the fabricated AMOLED pixels is mainly due to the *a*-Si:H TFT threshold voltage shift, we compare the threshold voltage shift of the driver TFTs calculated from the AMOLED luminance data of Fig. 4.11(a) assuming no OLED degradation, with the directly measured threshold voltage shift of individual test driver TFTs under the same DC bias stress, in Fig. 4.11(b). The small differences between these data verify that the pixel luminance degradation is mainly a result of the threshold voltage shift of the driver TFTs.

Although the improvement achieved in AMOLED reliability by increasing the process temperature is significant, it is still not sufficient for commercial display products. The stability requirement of *a*-Si:H TFTs for driving OLEDs and improving the lifetime of *a*-Si:H TFTs to meet this requirement is presented in Chapter 5.

4.5 *Summary and Conclusion*

The design and fabrication of AMOLED pixel arrays on high-temperature flexible clear plastic substrates at temperatures close to 300°C was presented in this chapter. The process temperature of nearly 300°C is an improvement of about 150°C compared to previous demonstrations. The electrical stability measurements of the pixels show the

impact of high temperature processing on improving the pixel reliability. Controlling the mechanical stress of the deposited layers and adhesion of the layers was essential to the development of the plastic-compatible process by ensuring crack-free layers and a flat backplane prior to OLED evaporation.

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High Lifetime *a*-Si:H TFTs for Active-Matrix OLED Displays

As discussed in the previous chapter, increasing the process temperature improves the stability of *a*-Si:H TFTs significantly and enhances the reliability of light emission in AMOLED pixels. However, in the present chapter, it is shown that the improvement achieved in *a*-Si:H TFT lifetime by increasing the process temperature is not sufficient and further improvement in lifetime is necessary for sufficient AMOLED reliability. Also in this chapter, the mechanisms responsible for the degradation of lifetime in *a*-Si:H TFTs are discussed and it is demonstrated that the lifetime of *a*-Si:H TFTs can be significantly enhanced by improving the quality of the gate nitride and the quality of *a*-Si:H close to the *a*-Si:H/nitride interface. Comparison with the literature shows that at low gate electric fields required for driving high-efficiency OLEDs, the lifetimes of the improved *a*-Si:H TFTs developed in this work are far in excess of the lifetimes of the *a*-Si:H TFTs reported by other groups.

5.1 *Lifetime Requirements for Driving OLEDs*

Standard *a*-Si:H TFTs are in widespread production for manufacturing the backplane for active-matrix liquid crystal displays (AMLCDs). However, driving OLEDs is far more demanding than driving LCDs. This is because in AMLCDs (Fig. 5.1(a)), the LCD is a capacitive load, and the TFT just acts as a digital switch. This makes the circuit fairly insensitive to changes in the TFT threshold voltage. Further, the duty cycle of the TFT is as low as 0.1%, minimizing the time the TFT is in operation. However, in AMOLED pixels (Fig. 5.1 (b)), the OLED is driven in DC (i.e. 100% duty cycle) and the OLED current and thus brightness depends directly and continuously (in an analog fashion) on

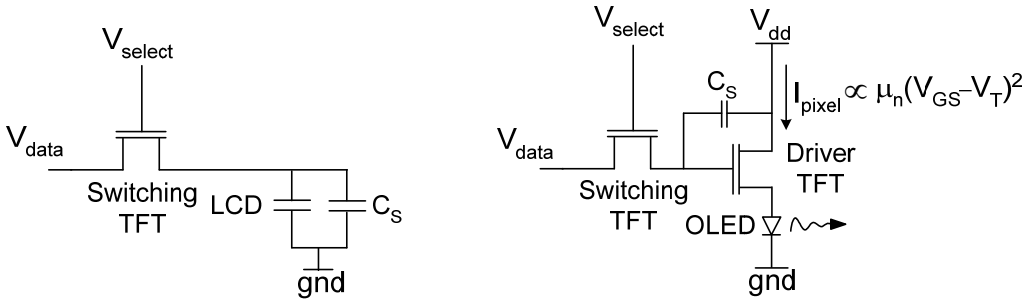


Fig. 5.1. The schematic pixel circuit of (a) an AMLCD and (b) an AMOLED display.

the TFT drive current which is lowered by the TFT threshold voltage rise.

The sensitivity of the human eye to the changes in the pixel brightness and the resulting distortion of color balance are also very high. For commercial applications, the maximum allowable distortion of color balance occurs when the brightness of one of the primary colors (red, green or blue) drops 5% with respect to the others [1]. This allows a maximum drop of 5% in the TFT drive current. For drive conditions corresponding to 1000Cd/m^2 OLED brightness discussed in Chapter 4, this 5% drop corresponds to about 100mV shift in the TFT threshold voltage.

Fig. 5.2 shows the threshold shift of a standard *a*-Si:H TFT typical of that used in the AMLCD industry, which is made on glass at a process temperature of 350°C [5] (The gate nitride deposition temperature, the highest temperature step in the a-Si:H TFT process, and similar to the previous chapter, hereafter we will refer to it as the "process temperature"). Also shown are data for what were (before this thesis) what we best know to be the most stable *a*-Si:H TFTs fabricated on clear plastic substrates for various process temperatures, as will be needed for future display technologies [6][7]. Previous work by our group shows that the stability of *a*-Si:H TFTs depends on the TFT process conditions (including the process temperature) but it is not affected by the type of the substrate [6][7]. Therefore, the TFT stability requirement investigated in this section, applies to both glass and clear plastic substrates, as well as other types of substrates. As seen in Fig. 5.2, a 100 mV shift, corresponding to the 5% current drop described in the previous paragraph, occurs at only about 10 minutes for industry standard TFTs processed at temperatures and the best TFTs on plastic (processed at 300°C). This indicates that the threshold voltage stability of standard *a*-Si:H TFTs is not sufficient for driving OLEDs.

Since the AMOLED pixel brightness depends directly and continuously on the current of the driver TFT, from an application point of view, it is helpful to investigate the TFT lifetime by measuring the degradation of TFT drive current (biased in saturation) over time. Since the OLEDs are characterized by their luminance half-life, defined as the time the OLED luminance drops by 50% at constant DC current, similarly, we define the

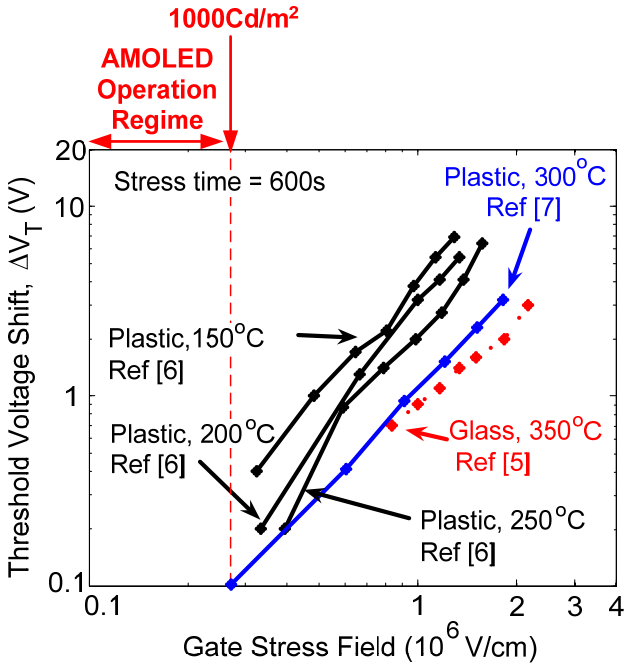


Fig. 5.2. Threshold voltage shifts of *a*-Si:H TFTs processed at various temperatures on clear plastic [6][7] along with a reference TFT on glass [5]. The TFTs were stressed for 10 minutes at various gate electric fields.

TFT current half-life as the time the TFT current drops to 50% under constant DC voltage bias in saturation. The extrapolated luminance half-life of high quality green phosphorescent OLEDs is as high as 30 years for an initial luminance of 1000Cd/m^2 [2]. Fig. 5.3 shows the degradation of the saturation current of standard *a*-Si:H TFTs over time at bias conditions required for driving OLEDs at a brightness of 1000Cd/m^2 (see Section 4.2) for various nitride deposition temperatures. As seen in the figure, the drive current half-lives of the TFTs are below 1 month, much shorter than the luminance half-life of the OLEDs. This indicates that the lifetime of standard *a*-Si:H TFTs is too short for driving OLEDs and therefore requires major improvement.

5.2 *Threshold Voltage Shift Mechanisms*

Improving the stability of *a*-Si:H TFTs requires knowledge of the TFT instability mechanisms. Conventionally, *a*-Si:H TFTs are stressed at high gate electric fields which are required for driving LCDs (typically larger than 10^6 V/cm). In addition, even for applications which require low gate electric fields such as driving OLEDs, stress measurements are conventionally performed at high gate electric fields to reduce the

measurement time (typically referred to as "accelerated testing"). This is because the TFT threshold voltage shift is higher at higher gate electric fields, allowing shorter stress times for measuring the TFT threshold voltage shift. In Fig. 5.4, the threshold voltage shifts of the driver TFTs at 1000Cd/m^2 OLED drive conditions extracted from AMOLED luminance degradation data (see Fig. 4.11) corresponding to low gate electric fields (labeled as "normal testing") is compared against TFT threshold voltage shifts measured directly at high gate electric fields (labeled as "accelerated testing"). Interestingly, as seen in the figure, the TFT threshold voltage shift at high fields cannot be extrapolated back to low gate electric fields needed for driving OLEDs. This indicates that different mechanisms are responsible for the TFT instability at low and high gate electric fields.

At high gate electric fields, the threshold voltage shift of *a*-Si:H TFTs is dominated by electron trapping in the gate nitride (Fig. 5.5 (a)), resulting in a logarithmic

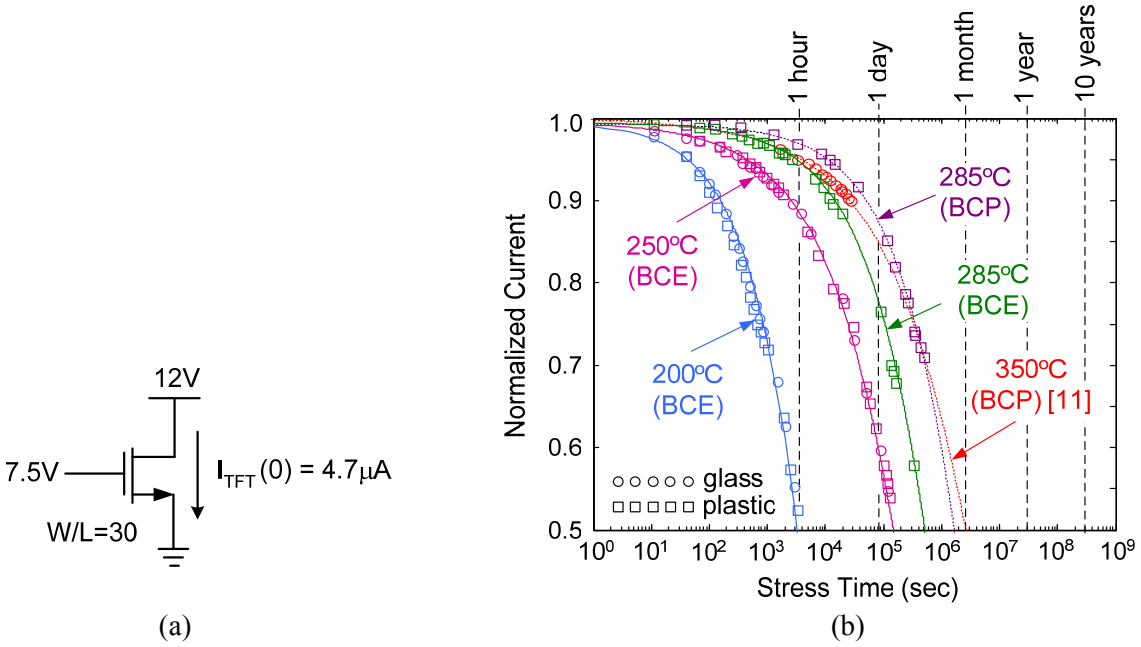


Fig. 5.3. (a) TFT drive condition for 1000Cd/m^2 OLED brightness corresponding to a gate voltage bias of 7.5V for a TFT with 300nm-thick gate nitride (see Section 4.2) and (b) the degradation of *a*-Si:H TFT saturation current over time at this drive condition (V_{GS} = 7.5V and V_{DS} = 12V) for various nitride deposition temperatures on glass and/or plastic. "BCE" and "BCP" refer to "back-channel etched" and "back-channel passivated" TFT structures, respectively (Section 3.1). The effect of the TFT structure on TFT lifetime is discussed in Section 5.3. The current drop from Ref. [11] was calculated from the published plot of threshold voltage shift vs. time which was measured at a gate bias stress of 8.0V, very close to our stress conditions.

time dependence of the TFT threshold voltage shift (ΔV_T)

$$\Delta V_T \propto (\log t)^{\lambda} \tag{5.1}$$

where λ is a constant close to 1 [3][8][5][8]. At low gate electric fields, the creation of defects in *a*-Si:H and capturing of electrons by these defects (Fig. 5.5 (b)) is the dominant instability mechanism, and as discussed in Section 2.7, this instability mechanism results in a stretched exponential time dependence which can be approximated by a power law relation at short stress times

$$\Delta V_T \propto t^{\beta} \tag{5.2}$$

with values of β in the range of 0.2-0.6 reported in the literature [5][8][9][10].

As seen in Fig. 5.6 (a), a value of 1.2 for λ extracted from fitting our experimental high-field threshold voltage shift data to Eq. (5.1) is close to the theoretical value of 1, indicating the dominance of electron trapping in the gate nitride at high gate electric fields. However, as seen in Fig. 5.6 (b), at low gate electric fields, the rate of the TFT threshold voltage shift is faster than could be predicted by the charge trapping model, as indicated by an extracted values of 4.8 for λ which is much larger than the theoretical value of 1. In contrast, a value of 0.44 extracted for β by fitting the low field threshold voltage shift data to Eq. (5.2) indicates that defect creation in *a*-Si:H is the dominant instability mechanism at low gate electric fields.

It is interesting to note that the low-field threshold voltage shift has a strong dependence on the gate nitride deposition temperature (Fig. 5.6 (b)). This is counter-intuitive, as the time dependence of the threshold voltage shift in this regime indicates the dominance of defect creation in the *a*-Si:H channel rather than charge trapping in the gate nitride. The dependence of low-field stability on the gate nitride indicates that the nitride quality affects the quality of *a*-Si:H close to the *a*-Si:H/nitride interface where defect formation in *a*-Si:H and then charge trapping occurs. As discussed in Section 3.2, since *a*-Si:H is deposited after the gate nitride, the quality and microstructure of *a*-Si:H can be affected by that of the nitride underneath it. Therefore, the quality of the gate nitride is important at both high and low gate electric fields. This will be further discussed in Section 5.4.

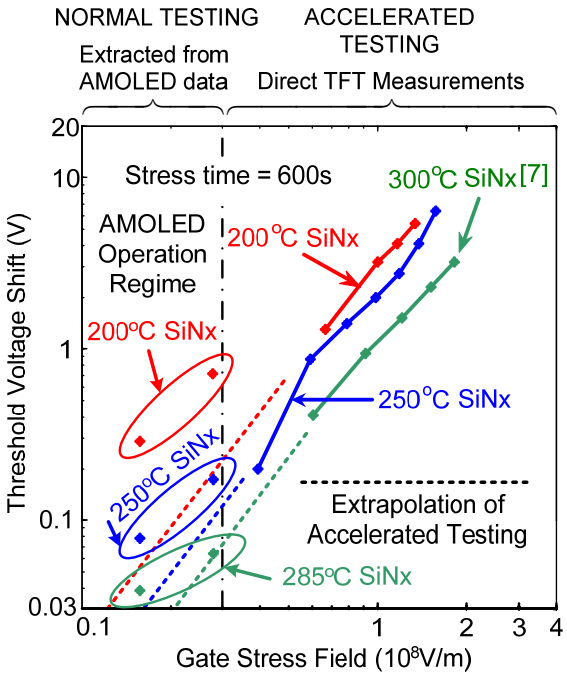
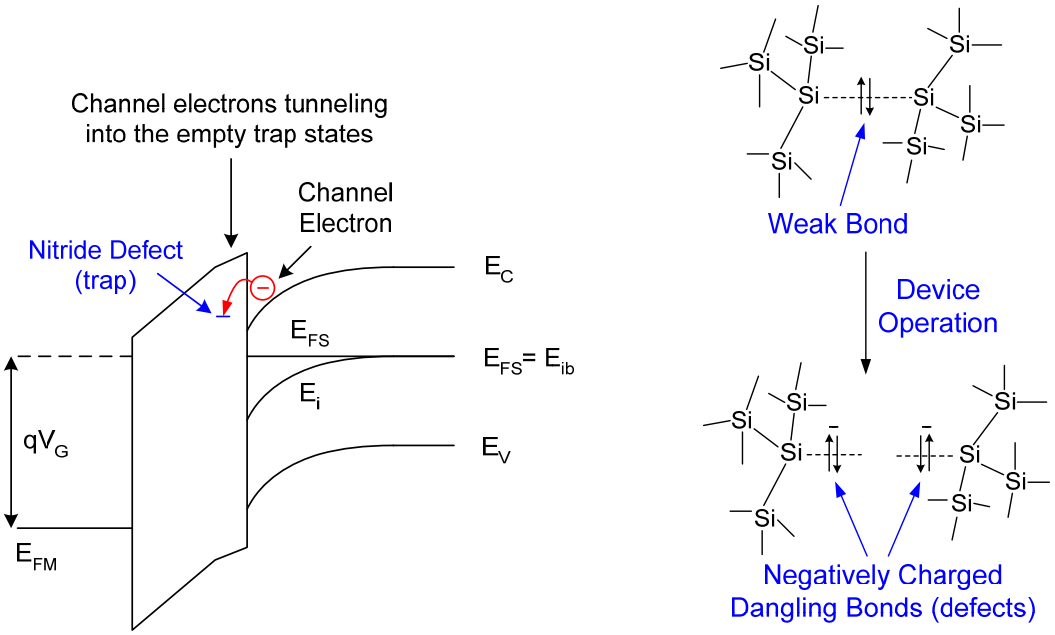


Fig. 5.4. Accelerated testing (direct TFT threshold voltage shift measurements and high gate electric fields) and normal testing (extraction of TFT threshold voltage shift from luminance drop in AMOLED pixel at normal drive conditions). Extrapolation of accelerated testing data underestimates the threshold voltage shift at low gate electric fields.



(a) $\Delta V_T \propto \log t$ (b) $\Delta V_T \propto t^{\beta}$

Fig. 5.5. Instability mechanisms responsible for threshold voltage shift in *a*-Si:H TFTs, (a) electron trapping in the gate nitride resulting in a logarithmic time dependence and (b) creation of defects in *a*-Si:H resulting in a power law relation at relatively short stress times.

5.3 *Improving the a-Si:H Channel with Hydrogen Dilution*

Since the low-field stability is dominated by the creation of defects in *a*-Si:H, improving the quality of *a*-Si:H is critical for improving the stability of *a*-Si:H TFTs. Our experiments show that this can be achieved by including hydrogen dilution in silane for growing the *a*-Si:H channel, both for *a*-Si:H TFTs on glass and plastic substrates.

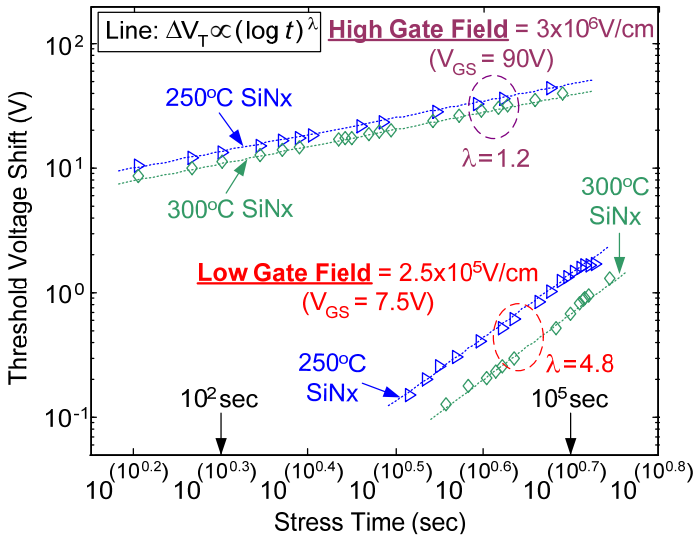
5.3.1 Experimental Structure

Inverted-staggered bottom-gate *a*-Si:H TFTs were fabricated with standard "back-channel etched" (BCE) or "back-channel passivated" (BCP) structures (Section 3.1) on clear plastic. Control samples were also prepared on glass substrates. In the back-channel etched structure, the n^+ *a*-Si:H layer is deposited in a single run with the gate nitride and undoped *a*-Si:H and subsequently removed from the back-side (top) of the channel after the deposition and patterning of the source/drain metal. In the back- channel passivated structure, the back-channel passivation (nitride) is deposited in a single run with the gate nitride and undoped *a*-Si:H and the n^+ *a*-Si:H layer is deposited after patterning the back-channel passivation which defines the channel length. The latter process seals the *a*-Si:H channel *in situ* with a nitride layer immediately after *a*-Si:H deposition at the cost of an extra mask step.

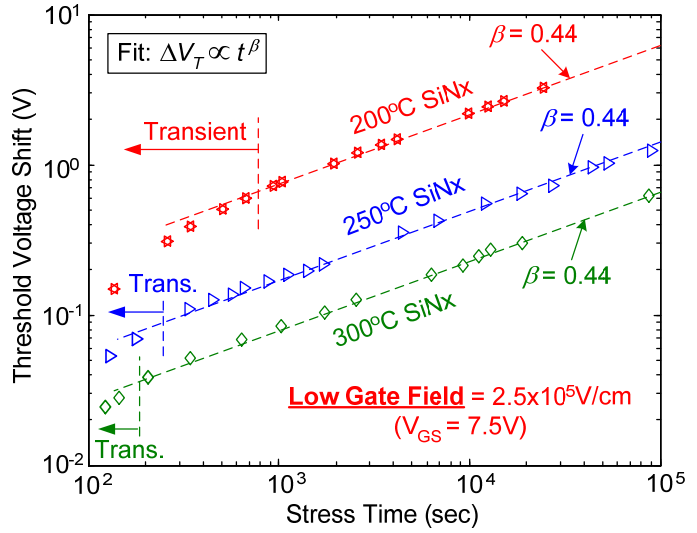
All TFTs were made with 300nm-thick gate nitride layers grown at a plasma power density of 22mW/cm^2 and a chamber pressure of 500mtorr. The 250-nm-thick *a*-Si:H layers were grown at a chamber pressure of 500 mtorr and at a plasma power density of 17 mW/cm^2. The 30-nm-thick n^+ *a*-Si:H layers were grown at 250°C, at 17mW/cm^2 and 500mtorr. All *a*-Si:H TFTs were annealed at 180°C in vacuum for one hour to repair plasma etch damage. The process parameters which were varied are listed in Table 5.1.

5.3.2 Stress Conditions and Extraction of Threshold Voltage

For all our low-field stress measurements, the TFTs were biased in saturation (with a constant drain voltage of 12V) and the threshold voltage shift (Fig. 5.7(a)) was calculated from the measured drop in the saturation current (Fig. 5.7(b)) using the model of a MOSFET in saturation (see Section 3.2)



(a)



(b)

Fig. 5.6. High-field and low-field threshold voltage shifts of back-channel etched (BCE) *a*-Si:H TFTs fabricated with different gate nitride deposition temperatures. (a) Plotting the TFT threshold voltage shifts in a semi-logarithmic plot shows that the high-field threshold voltage shifts match the nitride charge trapping model ($\lambda \approx 1$) while the low-field threshold voltage shift do not ($\lambda >> 1$). (b) Plotting the same low-field threshold voltage shifts in a logarithmic plot shows that the low-field threshold voltage shifts match the defect creation model in *a*-Si:H.

$$\Delta V_{T,sat} = (V_{GS} - V_{T0})\left(1 - \sqrt{I_{TFT,sat}(t)/I_{TFT,sat}(0)}\right) \tag{5.3}$$

where ΔV_T is the threshold voltage shift, V_{GS} the gate-source voltage, V_{T0} the initial threshold voltage, I_{TFT} the TFT drain current and the subscript "*sat*" refers to the saturation regime.

The measured change in mobility was negligible as expected from previous work [9][10][11]. We also found that mobility changed little – in transistors which had a threshold voltage shift of ~1.2V (corresponding to a 50% drop in current for a gate voltage of ~ 7.5V, standard linear region measurements to separate threshold and mobility showed a mobility change of less than 1%. Saturation measurements were done for two reasons, (i) saturation is the realistic operating condition in AMOLED pixels, and (ii) changes in saturation current allow more accurate measurement of small the threshold voltage shifts than linear measurements and do not require stopping the stress to estimate the threshold voltage shift. A gate stress field of ~2.5×10^5 V/cm corresponds to a gate voltage of ~7.5V. Due to the statistical variation of the TFT threshold voltages (Table 5. 1) the gate stress voltages were slightly adjusted for each TFT measurement to assure the same $V_{GS} - V_T$ of ~5.3V and thus the same initial saturation current of ~30nA per micrometer gate width.

Stress experiments were typically done for a period of several weeks to give the data in Fig. 5.7 (a). The threshold voltage shifts versus time in Fig. 5.7(a) were then extrapolated with a straight line in a log-log plot based on Eq. (5.2) to predict the shift for longer times. These extrapolated threshold voltages were then used to predict current vs. time in Fig. 5.7 (b) using the model of a MOSFET in saturation

$$I_{TFT,sat}(t) = I_{TFT,sat}(0)[1 - \Delta V_{T,sat}(t)/(V_{GS} - V_{T0})]^2 \qquad (5.4)$$

Sample/ Curve Label	TFT Back Channel	SiN_x Temp. (°C)	*a*-Si:H Deposition			Annealing Temp. (°C)	Mobility (cm^2/Vs)	Threshold voltage (V)
			Temp. (°C)	Pressure (Torr)	$[H_2]$ / $[SiH_4]$ Flow Ratio			
(a)	Etched	250	250	0.5	0	180	0.63±0.06	2.0±0.3
(b)	Etched	285	250	0.5	0	180	0.63±0.04	2.0±0.3
(c)	Passivated	285	250	0.5	0	180	0.64±0.04	2.3±0.1
(d)	Passivated	285	250	0.5	0	180+260	0.62±0.05	2.4±0.3
(e)	Passivated	285	250	0.8	10	180	0.66±0.05	2.2±0.1
(f)	Passivated	285	250	0.8	10	180+260	0.61±0.04	2.4±0.2

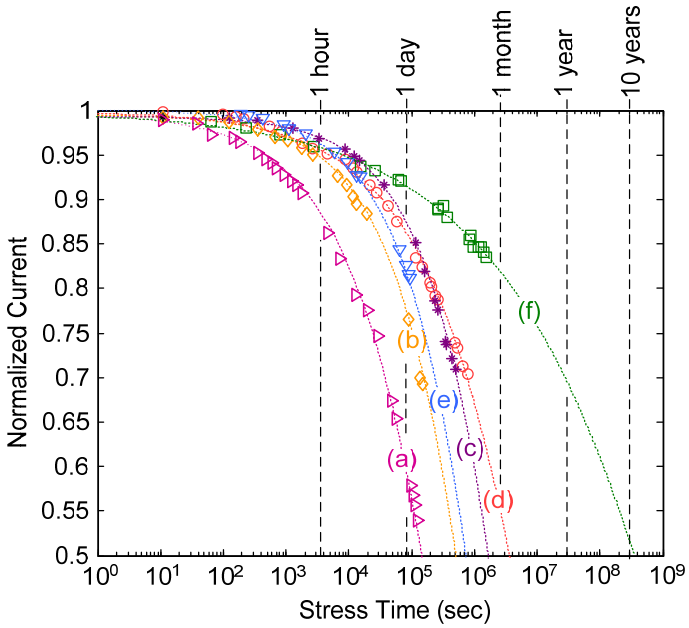
Table 5.1. Properties and process conditions that were varied and the saturation mobility and threshold voltage of the fabricated TFTs (with standard deviations). The parameters that were held constant are described in the text. The W/L ratio is 150μm/5μm for all the TFTs.

5.3.3 Effect of Hydrogen Dilution on TFT Stability

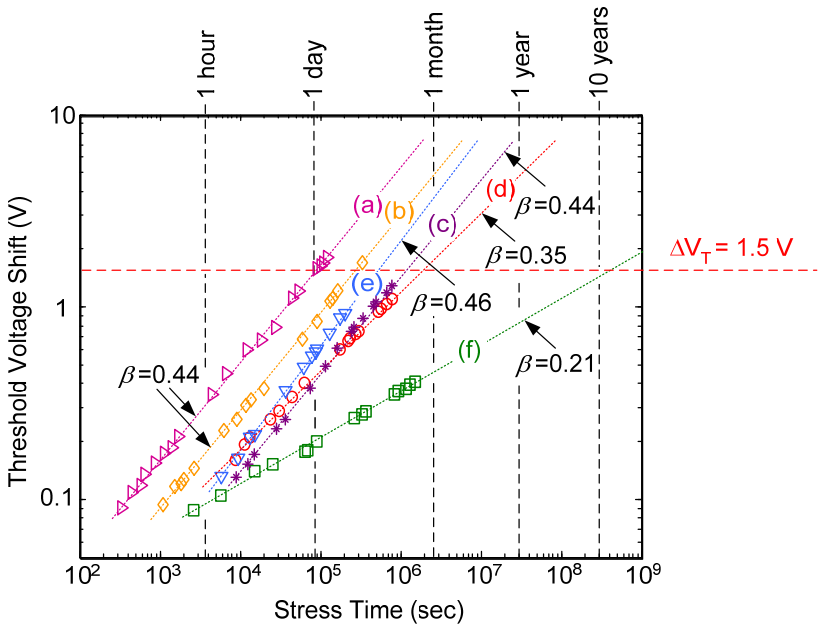
As discussed in 5.2, increasing the nitride deposition temperature improves the TFT stability at low fields by improving the quality of *a*-Si:H close to the *a*-Si:H/nitride interface. This improvement is observed in TFTs with gate nitride deposition temperature of 285°C (curve (b)) compared to TFTs with gate nitride deposition temperature of 250°C (curve (a)) which are included as a reference (both TFTs have "etched" structures). We now focus on comparing the TFTs with a fixed nitride deposition temperature of 285°C, i.e. curves (b) – (f). The TFTs with *a*-Si:H channel grown from pure silane and annealed at 180°C have a much lower threshold voltage shift in the "passivated" structure, curve (c), than in the "etched" structure, curve (b). An additional annealing of one hour in vacuum at 260°C slightly reduced threshold voltage shift in the "passivated" structure, curve (d), while this 260°C anneal degraded the DC characteristics of the "etched" TFTs so much that they were not measured further. This is consistent with the lasting damage created by plasma and process chemicals to the exposed back-channel. Varying the *a*-Si:H deposition temperature in the range of 230°C-280°C in both types of devices made no significant change. Hydrogen dilution slightly degraded the "passivated" devices, curve (e), compared to the "passivated" devices without hydrogen dilution, curve (c). The straight line fits to (a)-(e) have β in the range of 0.36-0.44 which is again consistent with defects in the *a*-Si:H close to the *a*-Si/nitride interface. Finally the 260°C anneal of the "passivated" sample (f) grown with hydrogen dilution dramatically reduces the threshold voltage shift, fitting a β of 0.20. Extrapolating the threshold voltage shift of this TFT gives ~1.2V after 10 years of continuous operation, curve (f), representing a 100-fold increase from the devices of curve (a). The TFT half-life of 10 years is now comparable with the OLED half-life of 30 years and indicates that the "improved" *a*-Si:H TFTs may qualify for driving OLEDs.

5.3.4 Physical Effect of Hydrogen Dilution

The role of hydrogen dilution in improving the lifetime of *a*-Si:H TFTs may be illustrated by the model of Fig. 5.9. Hydrogen radicals in plasma etch the weak Si-Si bonds *in situ* (i.e. at the growth surface, during growth) resulting in a material with fewer weak bonds.



(a)



(b)

Fig. 5.7. (a) Normalized TFT drain currents and (b) TFT threshold voltage shifts vs. time measured in saturation (V_{DS} = 12V) at a constant gate field of ~ 2.5×10^5 V/cm (symbols: data points, lines: extrapolations based on Eq. (5.1). The threshold voltage shift of 1.5V marked on plot (a) corresponds to approximately 50% drop in the TFT currents.

As explained in Section 2.7.2, the weak bonds in *a*-Si:H (weak or strained Si-Si bonds) have different energies. The bonds with lower energies convert to defects (by bond

breaking and capturing electrons) on a shorter time scale than those with higher energies. Therefore, reducing the density of weaker bonds (i.e. reducing the low-energy band tail of the density of weak bonds) reduces the rate of bond breaking during device operation and improves the device stability.

This concept that hydrogen radicals can remove weak Si-Si bonds during growth is well-known. Adding much more hydrogen than presented in this thesis can actually lead to the growth of "nanocrystalline" or "microcrystalline" silicon, in which nearly all amorphous silicon is removed [13][14][15][16]. Although carrier mobility is higher in the nano/microcrystalline Si TFTs compared to *a*-Si:H TFTs, these devices suffer from high off-current, high device-to-device threshold voltage variation compared to *a*-Si:H TFTs, and typically poor stability[17][18][19][20]. Our work is novel in that it uses hydrogen dilution to "improve" the *a*-Si:H channel, with a focus on reducing "weak bonds" to improve *a*-Si:H TFT stability, while avoiding nano/microcrystalline growth. Earlier groups have observed that low amounts of hydrogen dilution affect the plasma properties during *a*-Si:H growth with an affect on TFT stability, but no lifetimes in excess of ~1 month were observed [21][22].

5.3.5 Comparison with *a*-Si:H TFTs from the Literature

Nearly all of our measurements of TFT stability were done with the TFT operated continuously in saturation. In most other stability work in the literature, the TFT is operated with small drain voltages in the linear regime. Since defect creation in *a*-Si:H depends on the density of mobile channel electrons, for a fair comparison, the threshold voltage shifts measured by other groups at low gate electric fields can be scaled to our conditions by the ratio of the density of mobile channel electrons at our stress conditions in saturation ($Q_{ch,\,PU}$) to that of their stress conditions with small drain voltages (Q_{ch})

$$\Delta V_{T,\,scaled} = \Delta V_T \times \frac{Q_{ch,\,PU}}{Q_{ch}} = \Delta V_T \times \frac{(2/3) C_{ins,\,PU} (V_{GS,\,PU} - V_{T0,\,PU})}{C_{ins} (V_{GS} - V_{T0})} \qquad (5.5)$$

where C_{ins} is the gate dielectric capacitance per unit area of the channel, V_{T0} is the initial threshold voltage and the subscript PU refers to our TFTs. The 2/3 coefficient in this equation accounts for conducting our measurements in the saturation regime where the

density of mobile channel electrons is lower than that in the linear regime (used by other groups) by a factor of 2/3.

Fig. 5.10 compares the threshold shifts vs. time of *a*-Si:H TFTs compared to our work (curves (b), (c), and (f) repeated from Fig. 5.7 (b)). It is difficult to quantitatively compare the different sets of work because of different gate voltages and gate insulator thicknesses, meaning different electric fields in the gate insulator and different electron densities in the channel, both of which affect stability. However, all points are in the range where defect formation in *a*-Si:H is expected to dominate the shift in threshold. A visual comparison of the scaled threshold voltages (which physically means comparing the rate of electron trapping in the dangling bonds) shows clearly that the low-field stability of our improved *a*-Si:H TFTs with hydrogen dilution during *a*-Si:H deposition (curve (f)) is superior to that of standard *a*-Si:H TFTs reported in the literature (Fig. 5.10). In Chapter 6, we present a formal method for making a "fair comparison" of the stabilities of TFTs with different gate insulator materials and thicknesses measured under different gate voltages.

5.4 *Improving the a-Si:H Channel by Improving the Gate Nitride*

As discussed in Section 5.2, the quality of *a*-Si:H close to the *a*-Si:H/gate nitride interface can be improved by improving the quality of the gate nitride. In this section, we present experiments demonstrating that improving the quality of the gate nitride together with including hydrogen dilution for the growth of the *a*-Si:H channel can increase the TFT lifetime to over 1000 years. Improving the gate nitride quality has been pursued by

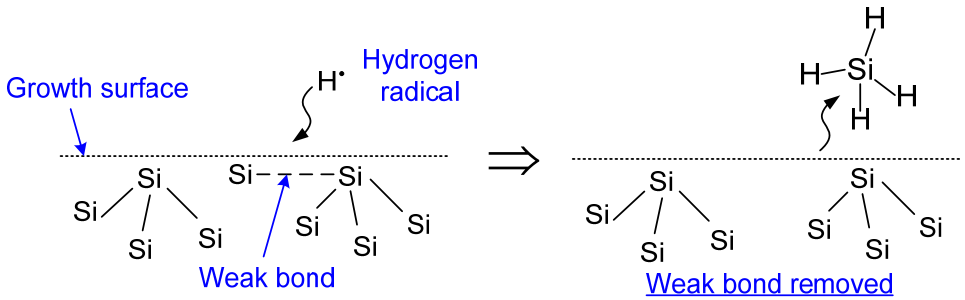


Fig. 5.9. Suggested mechanism for *in situ* removal of weak bonds by hydrogen radicals during *a*-Si:H growth. Silane is diluted with hydrogen during *a*-Si:H growth for this purpose.

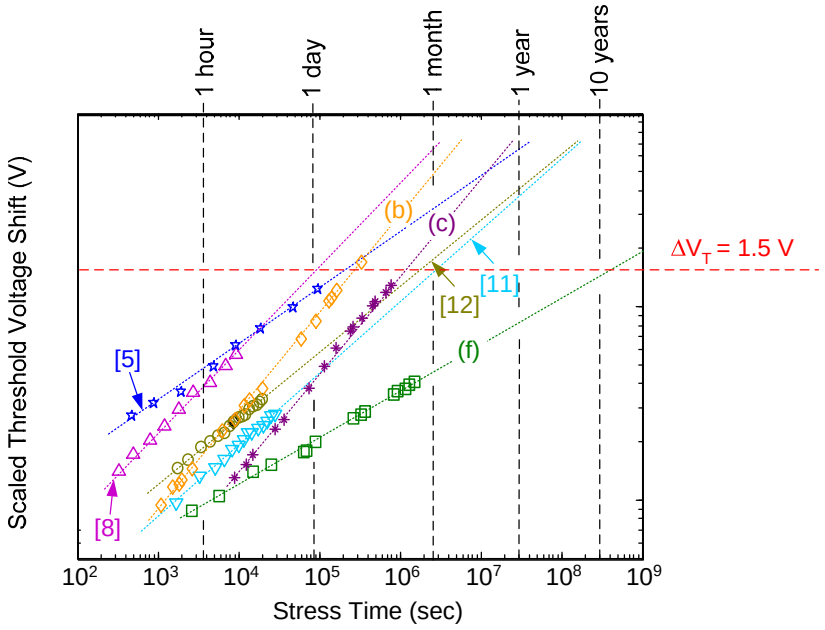


Fig. 5.10. ΔV_T vs. time (symbols: data points, lines: extrapolations) of the test TFTs (b), (c) and (f) (Table I) and the scaled ΔV_T of *a*-Si:H TFTs reported in literature [5][8][11][12] based on Eq. (5.2). The TFT parameters are, Ref. 5: "etched" TFTs, V_{GS} = 20V, V_{T0} =2.5V, insulator: SiN_x 500nm, Ref. 7: "passivated" TFT's, V_{GS} = 25V, V_{T0} =4.5V, insulator: SiO_x 300nm+SiN_x 50nm, Ref. 9: "passivated" TFTs, V_{GS} = 8V, V_{T0} =1.3V, insulator: SiN_x, 300nm, Ref. 10: "passivated" TFTs, V_{GS} = 15V, V_{T0} =2.7V, insulator: SiN_x, 200nm. A relative dielectric constant of 7.5 and 3.9 was assumed for all nitride and oxide insulators, respectively. The threshold voltage shift of 1.5V marked on the plot corresponds to approximately 50% drop in the TFT currents.

increasing the gate nitride deposition temperature, using hydrogen dilution during the growth of the gate nitride and eventually the combination of both. We show that hydrogen dilution during the growth of *a*-Si:H is necessary for achieving high TFT lifetimes at low gate electric fields and discuss it in terms of the substrate dependence of *a*-Si:H growth.

5.4.1 Experiments: Increased Nitride Growth Temperature

The experimental results of Section 4.4 suggest that the *a*-Si:H TFT lifetime is improved by increasing the gate nitride deposition temperature from ~200°C to ~300°C. This was further studied in Section 5.2 and the improvement of the low field stability of *a*-Si:H TFTs by increasing the gate nitride deposition temperature was attributed to the improvement of the *a*-Si:H channel quality close to the *a*-Si:H/nitride interface. Our experiments show that without hydrogen dilution for *a*-Si:H growth, increasing the gate

nitride deposition temperature from 300°C (sample (c), Table 5.2) to 350°C (sample (g), Table 5.2) has negligible effect on low-field TFT stability (Fig. 5.7.Fig. 5.11). However, when hydrogen dilution is used for the growth of *a*-Si:H, increasing the gate nitride deposition temperature from 300°C (sample (f), Table 5.2) to 350°C (sample (h), Table 5.2) improves the TFT lifetime from ~10 years to ~100 years (Fig. 5.7.Fig. 5.11). The physical effect of the gate nitride and the role of hydrogen dilution during *a*-Si:H growth in improving the low field stability in these experiments are discussed in Section 5.4.4.

The *a*-Si:H TFT drive current half-life of ~100 years exceeds the luminance half-life (~30 years) of high-quality OLEDs, suggesting that these TFTs may qualify for driving high-quality OLEDs in 2-TFT AMOLED pixels. However, due to the high nitride deposition temperature of 350°C, we have implemented this process only on glass. Plastic compatibility requires improving the nitride quality without further increasing the deposition temperature. This issue is addressed in the following section.

5.4.2 Experiments: Hydrogen Dilution for Nitride Growth

In the previous section, the deposition temperature of the gate nitride was increased to ~350°C to improve quality of *a*-Si:H close to the *a*-Si:H/nitride interface and achieve a TFT lifetime of ~100 years. However, a process temperature limit of 300°C is desired to improve the plastic compatibility. Our experiments show that hydrogen dilution can be used for the growth of the gate nitride to allow lower nitride deposition temperatures. As a result, a nitride deposition temperature of ~ 300°C can be used to achieve a high TFT lifetime of ~100 years (sample (i), Table 5.2).

As discussed in Section 3.3.2, the application of hydrogen dilution for improving the quality of nitride at low deposition temperatures (<200°C) has been reported [23][24][25]. Earlier groups have also observed that hydrogen dilution affect the plasma properties during nitride growth at higher depositions temperatures as well and affect TFT stability, but no significantly high lifetimes (higher than ~1 month) were achieved with the growth conditions under study [26][27]. Our work is novel in that hydrogen dilution is used at high nitride deposition temperatures (~300°C), not particularly to improve the quality of the nitride for high field properties but rather to improve the quality of *a*-Si:H close to the *a*-Si:H/nitride interface.

Sample/Curve Label	*a*-SiN_x:H Deposition		*a*-Si:H Deposition		Extrapolated Lifetime
	Temperature	H dilution	Temperature	H dilution	
(c)	~ 300°C	No	~ 250°C	No	~ 1 month
(f)	~ 300°C	No	~ 250°C	Yes	~ 10 years
(g)	~ 350°C	No	~ 250°C	No	~ 1 month
(h)	~ 350°C	No	~ 250°C	Yes	~ 100 years
(i)	~ 300°C	Yes	~ 250°C	Yes	~ 100 years
(j)	~ 350°C	Yes	~ 250°C	Yes	~ 1000 years

Table 5.2. Deposition conditions of the *a*-Si:H channel and the gate nitride for the test TFTs studied in this section. The extrapolated lifetimes of these TFTs are also listed in the table. Samples (c) and (f) are repeated from Table 5.1 for comparison. All test TFTs are back-channel passivated.

5.4.3 Experiments: Hydrogen Dilution and Increased Temperature for Nitride Growth

Our experiments show that further improvement in the TFT lifetime is possible by raising the nitride deposition temperature and using hydrogen dilution for the growth of both the *a*-Si:H channel and the gate nitride. With a process temperature of 350°C for the gate nitride (sample (j), Table 5.2), we have demonstrated a TFT lifetime of ~1000 years (Fig. 5.7.Fig. 5.11). The drive current half-life of ~1000 years is well above the luminance half-life of high-quality OLEDs (~30 years), showing the promise of these TFTs for driving high-quality OLEDs in 2-TFT AMOLED pixels.

5.4.4 Physical Effect of Gate Nitride on *a*-Si:H Channel

As discussed in Section 3.2, in the bottom-gate *a*-Si:H TFT structure, *a*-Si:H is deposited on top of the gate nitride. Therefore the quality and microstructure of *a*-Si:H can be affected by that of the nitride underneath it. Substrate dependence of *a*-Si:H growth is well-known especially when hydrogen dilution is included during PECVD growth typically intended for the growth of nanocrystalline Si (nc-Si) or microcrystalline Si (μc-Si) which are of interest for both TFT and solar cell applications [13][14][28].

In general, it is well-established that for amorphous substrates such as glass, metal or plastic, sufficiently high $[H_2]/[SiH_4]$ ratios (about 10 and above) lead to the growth of

nc/μc-Si after an *a*-Si:H transition layer (in which random nucleation takes place) is grown [13][14]. The thickness of the transition layer is substrate dependent and is reduced by increasing the hydrogen dilution ratio. For example, with $[H_2]/[SiH_4]=15$, the thickness of the *a*-Si:H transition layer was found to be ~100nm and ~300nm on silicon dioxide (SiO_2) and *a*-Si:H substrates, respectively. With $[H_2]/[SiH_4]=40$, nc/μc-Si was found to grow immediately on SiO_2 (i.e. with no initial *a*-Si:H transition layer growth), while an *a*-Si:H transition layer of 20nm was still observed on *a*-Si:H substrates at the same $[H_2]/[SiH_4]$ of 40. For immediate growth of nc/μc-Si:H on *a*-Si:H, the required $[H_2]/[SiH_4]$ is extrapolated to be as high as 1000 (which are not practical for film growth) [13][14]. These observations clearly indicate that an underlying substrate, even if of amorphous nature, can have a significant effect on the quality and microstructure of *a*-Si:H which is grown on that substrate. The substrate dependence of nc/μc-Si:H growth is also well-known [28]

The substrate dependence of growth is even more pronounced if a nano/micro-crystalline, polycrystalline or single crystalline substrate is used instead of an amorphous substrate. For example, in the case of a single-crystalline substrate such as a Si wafer, $[H_2]/[SiH_4]$ ratios of ~10 and higher result in immediate epitaxial growth of single-crystalline Si on the wafer [29][30]. However, eliminating or lowering the hydrogen dilution results in the growth of *a*-Si:H rather than single-crystalline Si, further highlighting the role of hydrogen dilution, which can be explained within the context of Fig. 5.9. Hydrogen radicals remove the weak Si-Si bonds (which would otherwise result in the growth of an amorphous film) in-situ from the growth surface, leaving only the strong Si-Si bonds, and therefore leading to the growth of a single-crystalline film following the crystalline structure of the Si substrate.

The improvement in the low-field lifetime of our test TFTs with improving the nitride quality when hydrogen dilution is used for growing the *a*-Si:H channel (samples (f), (h), (i) and (j), Table 5.2) from ~10 years to ~1000 years is a clear indication that the gate nitride quality affects the quality of the *a*-Si:H channel material grown on top of it. The role of hydrogen dilution is also evident as the lifetime of the test TFTs fabricated with no hydrogen dilution for the growth of the *a*-Si:H channel is lower than a month (samples (c) and (g), Table 5.2). Our work is novel in that we use an "amorphous"

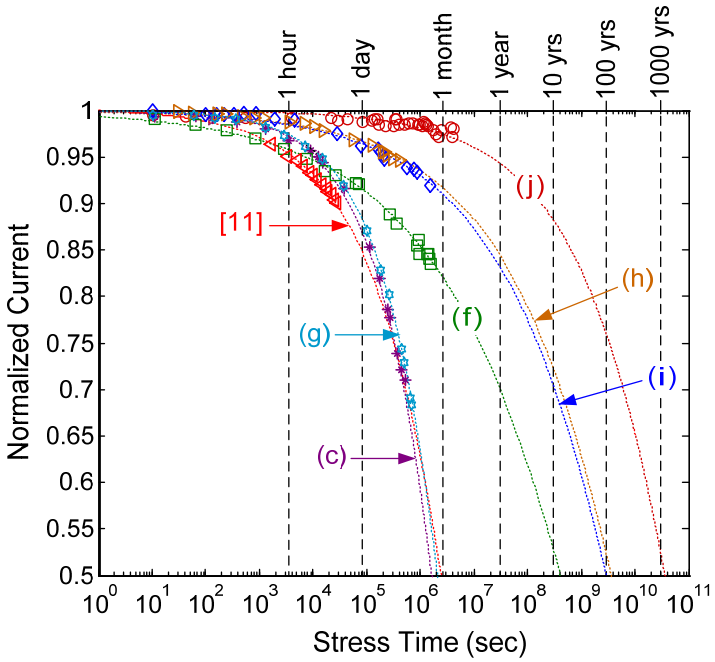


Fig. 5.11. Normalized TFT current vs. time for various *a*-Si:H TFTs grown at different conditions listed in Table 5.2. The stress conditions are the same as that illustrated in Fig. 5.3 (a). The current drop of a conventional *a*-Si:H TFT is also included from the literature as a reference [11].

material (nitride) as a growth template to improve the quality of another "amorphous" material (*a*-Si:H) grown on top of it (rather than growing nano/microcrystalline films). The extracted electron mobility of our test TFTs (of the order ~1cm^2/Vs for long-channel devices) confirms that the channel is still amorphous.

5.5 *Summary and Conclusion*

In this chapter, the stability requirement on *a*-Si:H TFTs for driving OLEDs was discussed and the stability of conventional *a*-Si:H TFTs was shown to be too short was driving OLEDs. To improve the stability of *a*-Si:H TFTs, the mechanisms responsible for the threshold voltage shift in these devices were studied. The instability mechanisms were identified by measuring the time-dependence and field dependence of the TFT threshold voltage shift. At low gate electric fields required for driving OLEDs, the creation of defects in *a*-Si:H and electron trapping into these defects was found to be the dominant instability mechanism. The quality of *a*-Si:H close to the *a*-Si:H/nitride interface which determines the rate of defect creation in *a*-Si:H was found to depend on both the *a*-Si:H channel and the gate nitride. Including hydrogen dilution during the

growth of *a*-Si:H and the gate nitride, and a high temperature for the growth of the gate nitride was demonstrated to improve the drive current half-life of standard *a*-Si:H TFTs from lower than a month to over 1000 years, well above the luminance half-life of high-quality OLEDs (~30 years). This suggests that the improved *a*-Si:H TFTs may qualify for driving OLEDs for commercial display applications.

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Trade-off Regimes of Lifetime in *a*-Si:H Thin-Film Transistors and a Universal Lifetime Comparison Framework

In the previous chapters, the *a*-Si:H TFT lifetime was studied in the context of the TFT current decay versus time or versus the gate electric field. Changing the TFT structural parameters such as the gate insulator thickness will change both the TFT current and the rate of degradation, making it difficult to compare different designs. However, comparing lifetime versus channel sheet resistances, as shown this chapter, is not affected by changes in TFT parameters. Studying the *a*-Si:H TFT lifetime versus channel sheet resistance identifies two modes of degradation which are explained in terms of their physical origins and modeled quantitatively in this chapter. These modes of degradation demonstrate that there is a trade-off between high TFT drive current and high-lifetime, both of which are desirable design parameters. Based on these studies, a universal lifetime comparison framework is presented for *a*-Si:H TFTs as well as other TFT technologies.

6.1 *Current Decay Modes and Lifetime Regimes*

The TFT current decay for the "standard" and "improved" *a*-Si:H TFTs and at drain-source voltages of 0.1V (for gate voltages up to 120V) in the linear regime and a drain-source voltage of 15V (for gate voltages up to 10V) in saturation are plotted in Fig. 6.1 ("Standard Process" refers to no hydrogen dilution for *a*-Si:H and gate nitride growth (process (c), Table 5.2), "Improved Process A" refers to hydrogen dilution only for *a*-Si:H growth (process (f), Table 5.2) and "Improved Process B" refers to hydrogen dilution for both *a*-Si:H and gate nitride growth (process (j), Table 5.2)). Because the current decays faster (lifetime is lower) at high gate voltages (low channel sheet resistance), from an application point of view, it is useful to examine the lifetime vs. channel sheet resistance. The channel sheet resistance (R_{sheet}) is defined as $(V_{DS} / I_{TFT,lin}) \cdot (L/W)$, where V_{DS} is the drain-source voltage, $I_{TFT,lin}$ the TFT current in the linear mode, L the channel length and W the channel width. The reason for choosing channel sheet resistance instead of gate voltage is that the drain current and circuit delay

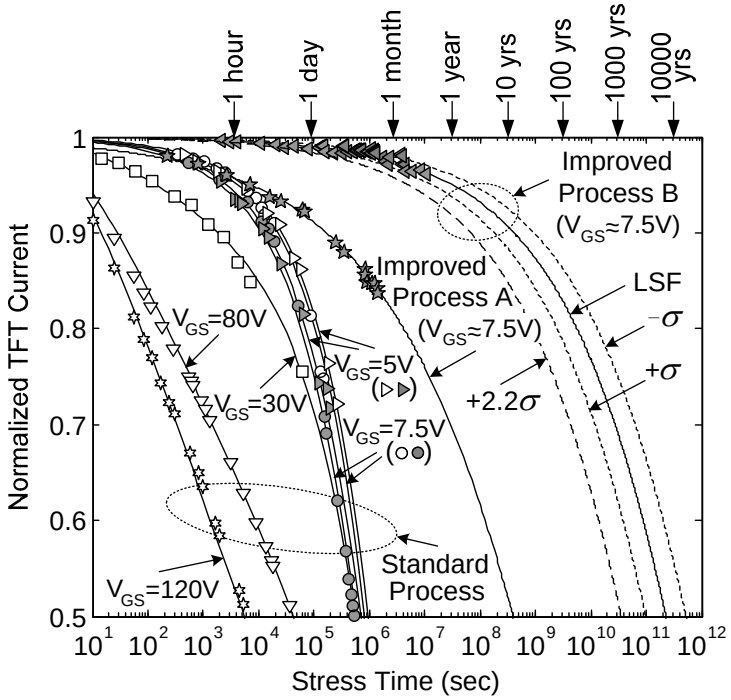

Fig. 6.1. Degradation of *a*-Si:H TFT current in the linear (empty symbols) and saturation mode (full symbols). The lines are predictions based on Eq. (6.3) and (6.5). The "Standard Process", "Improved Process A" and "Improved Process B" refer to processes (c), (f) and (j) in Table 5.2, respectively. The dashed lines show the error bounds for the least square fit (LSF) used for the improved process B.

can be determined directly from the channel sheet resistance without being affected by changes in the gate insulator capacitance, carrier mobility and initial threshold voltage.

The lifetime for a 10% decay of current (denoted as $\tau_{10\%}$ in Fig. 6.2) from the data of Fig. 6.1 (for the standard TFT process) shows two different regimes. At low channel sheet resistance there is a trade-off between high lifetime and low channel sheet resistance (both desirable device parameters). At high channel sheet resistance, the lifetime becomes independent of channel sheet resistance.

6.2 *Physical Origin of Lifetime Regimes*

To understand the physical origin of the two regimes, the TFT threshold voltage rise (ΔV_T) is extracted from the decay of current (Fig. 6.3), assuming negligible shift in mobility and other TFT parameters [4][5][6]. First-order TFT equations are assumed in the linear (with small V_{DS}) and saturation regimes (Section 3.2)

$$I_{TFT,lin}(t) = \mu_{FE} C_{ins} \frac{W}{L}\left(V_{GS} - V_{T0} - \Delta V_{T,lin}(t)\right) V_{DS} \qquad (6.1a)$$

$$I_{TFT,sat}(t) = \frac{1}{2}\mu_{FE} C_{ins} \frac{W}{L}\left(V_{GS} - V_{T0} - \Delta V_{T,sat}(t)\right)^2 \qquad (6.1b)$$

where V_{GS} is the gate-source voltage, V_{T0} the initial threshold voltage, μ_{FE} the field-effect mobility of carriers (electrons), and C_{ins} the gate dielectric capacitance per unit area, i.e. $\varepsilon_{ins}/t_{ins}$, where ε_{ins} and t_{ins} are the dielectric constant and thickness of the gate dielectric ($\varepsilon_{ins} = 7.4\varepsilon_0$ for nitride). The subscripts "*lin*" and "*sat*" refer to the linear and saturation modes, respectively. For our standard *a*-Si:H TFTs (L = 5μm), $\mu_{FE} = 0.64 \pm 0.05$ cm^2/Vs and $V_{T0} = 2.2 \pm 0.2$ V.

Qualitatively, the two regimes may be understood as follows. The TFT threshold voltage shift is caused by the channel electrons trapped into the gate nitride or the defects created in the *a*-Si:H channel [4][5]. In either case, channel sheet resistance increases with the drop in the number of mobile channel electrons, n_{chan} (note $n_{chan} = C_{ins}(V_{GS} - V_T) = C_{ins}(V_{GS} - V_{T0}) + Q_{trap}/q$, where V_T is the TFT threshold voltage, Q_{trap} the trapped charge ($Q_{trap} < 0$) and q the electron charge). Therefore the fractional

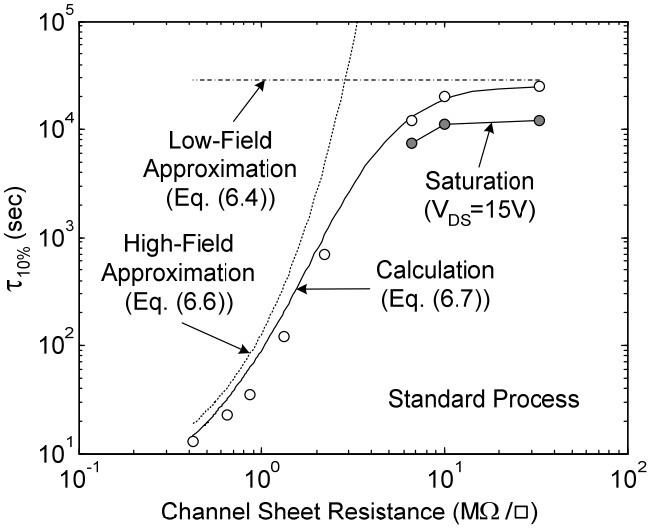

Fig. 6.2. The 10% current decay lifetime ($\tau_{10\%}$) vs. channel sheet resistance ($1/[\mu_{FE} C_{ins}(V_{GS} - V_{T0})]$) for our standard TFTs (process (c) in Table 5.2) along with the high and low field approximations and calculation for the linear mode. Empty and full symbols indicate the linear and saturation modes, respectively.

change in channel sheet resistance is

$$\frac{\Delta R_{sheet}}{R_{sheet}} \approx \frac{-\Delta n_{chan}}{n_{chan}} \propto \frac{-Q_{trap}/\varepsilon_{ins}}{n_{chan}} \propto \frac{-Q_{trap}/\varepsilon_{ins}}{E_{ins}} \qquad (6.2)$$

where E_{ins} is the gate electric field, defined as V_{GS}/t_{ins}. For the last term we assume the trapped charge is small compared to the channel charge (so n_{chan} is the dominant source of E_{ins}), as would be valid when the current decays is less than 10% of its initial value (implying the channel charge has been reduced by less than 10%). In writing Eq. (6.2), we assume the gate insulator is thick compared to the *a*-Si:H/nitride interface region where charge trapping occurs). At low gate electric fields (V_{GS} < ~7.5V for our nitride thickness), the threshold voltage shift is dominated by defect creation in *a*-Si:H and electron trapping in these defects. The rate of this process (and thus the trapped charge) and the shift of the channel sheet resistance are proportional to the number of mobile channel electrons [6]. Thus the fractional change in the channel sheet resistance (and thus the TFT lifetime) is independent of the channel sheet resistance in this regime, explaining the observation in Fig. 6.2. At high gate fields (V_{GS} > ~30V), the threshold voltage shift is dominated by charge trapping in the PECVD gate nitride, where Fowler-Nordheim tunneling is dominant at room temperature [1], resulting in an approximately quadratic dependence on the gate electric field, E_{ins} [8]. Therefore at high gate fields, $\Delta R_{sheet}/R_{sheet} \propto E_{ins}$. The TFT lifetime drops with increasing the gate electric field (lowering the channel sheet resistance), again consistent with Fig. 6.2.

6.3 *Quantitative Model of Lifetime Regimes*

The two regimes of lifetime may be quantitatively modeled as follows. In the low-field regime (referred to by the subscript "*low*-V_{GS}"), the threshold voltage shift may be approximated by a power law [4][5] (β and τ_0 are constants).

$$\Delta V_{T,lin,low-V_{GS}} = (V_{GS} - V_{T0}) \cdot (t/\tau_0)^{\beta} \qquad (6.3)$$

The saturation regime is important at low fields because it is the realistic operation regime for driving OLEDs. In this regime, $\Delta V_{T,sat,low-V_{GS}} = (2/3)\Delta V_{T,lin,low-V_{GS}}$ as the density of mobile channel electrons is lower by a factor of 2/3 compared to the linear mode [6].

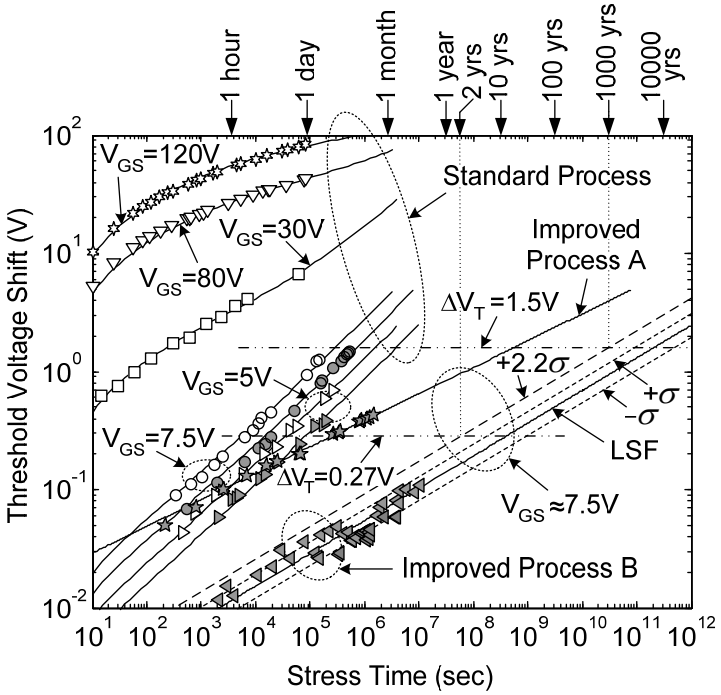

Fig. 6.3. Threshold voltage shifts of *a*-Si:H TFTs extracted from Fig. 6.1. The models (lines) are based on Eq. (6.3) and (6.5). Empty and full symbols refer to the linear and saturation modes, respectively. The 0.27V and 1.5V shifts correspond to 10% and 50% current drop at V_{GS} = ~7.5V in saturation. The dashed lines show the error bounds for the least square fit (LSF) used for the improved process B.

For our standard TFTs, $\beta = 0.45$ and $\tau_0 = 2.8\times10^6\,\text{sec}$. Using Eq. (6.3) and (6.1a), the low-field lifetime in the linear regime is found as

$$\tau_{10\%,\,lin,low-V_{GS}} = \tau_0\,(0.1)^{1/\beta} \qquad (6.4)$$

Using Eq. (6.1b) and Eq. (6.3) (including the 2/3 factor for the latter), the low-field lifetime in saturation is found to be lower than that in the linear regime by a factor of $[(2/3).(1+\sqrt{0.9})]^{1/\beta}$. This is because of a higher sensitivity of the TFT current to the TFT threshold voltage in saturation. In the high-field regime (referred to by the subscript "*high-*V_{GS}"), ΔV_T is logarithmic in time [1][3] (B and t_0 are constants).

$$\Delta V_{T,lin,high-V_{GS}} \approx B\cdot {V_{GS}}^2\cdot\ln(1+t/t_0) \qquad (6.5)$$

For our standard TFTs, $t_0 = 4.7\,\text{sec}$ and $B = 5.8\times10^{-4}\,\text{V}^{-1}$. Thus the high field lifetime can be found from Eq. (6.5) and (6.1a)

$$\tau_{10\%,\ lin,\ high-V_{GS}} \approx t_0 \exp(0.1/BV_{GS}) \qquad (6.6)$$

When both degradation mechanisms are important, $\tau_{10\%}$ may be calculated numerically

$$(V_{GS}-V_{T0})\cdot(\tau_{10\%,lin}/\tau_0)^{\beta} + B\cdot V_{GS}{}^2\cdot\ln(1+\tau_{10\%,lin}/t_0) = 0.1(V_{GS}-V_{T0}) \qquad (6.7)$$

This model fits the data quantitatively (Fig. 6.2).

6.4 *Process Dependence of Lifetime Regimes*

The two lifetime regimes are present for the improved *a*-Si:H TFTs as well. The quality of *a*-Si:H may be improved by "in situ" removal of weak Si-Si bonds by including hydrogen dilution during the PECVD of *a*-Si:H and using a back-channel passivated TFT structure. Replacing the standard *a*-Si:H with the improved *a*-Si:H (improved process A), improves the lifetime at high channel sheet resistance (red triangles in Fig. 6.4), as a result of a lower defect creation rate in the improved *a*-Si:H.

Improving the quality of the gate nitride in addition to improving the *a*-Si:H channel (improved process B) further improves the lifetime at both high and low channel

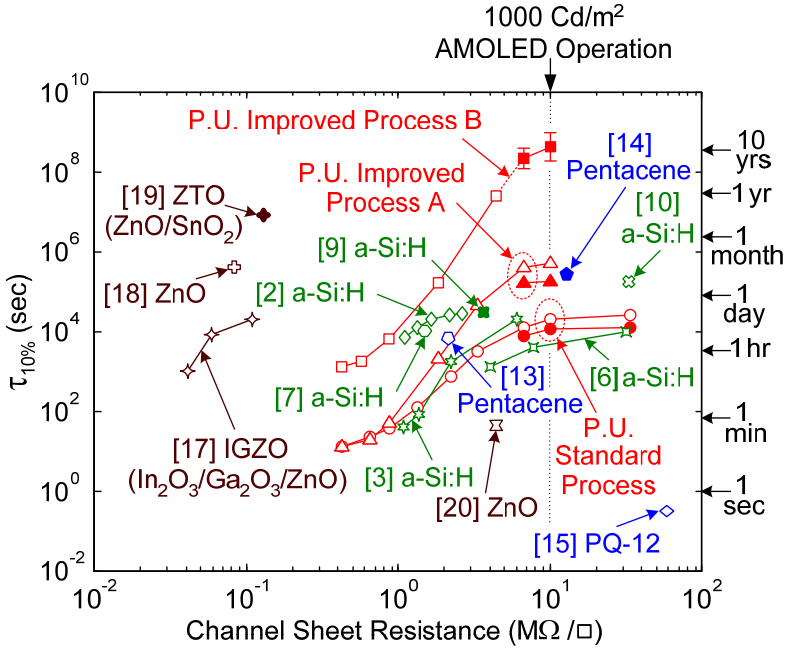

Fig. 6.4. The 10% current decay lifetime vs. channel sheet resistance for our *a*-Si:H TFTs (P.U. refers to "Princeton University" and the error bars indicate the standard deviations of fitting errors), along with those of *a*-Si:H TFTs and other TFT technologies from other groups. Empty and full symbols refer to the linear and saturation modes, respectively.

sheet resistance (red squares in Fig. 6.4). This was achieved by using a high deposition temperature (350°C) and including hydrogen dilution during the PECVD of the gate nitride for the "in situ" removal of weakly bonded Si atoms. The improvement at high fields is due to lower charge trapping in the improved nitride as a result of a lower density of nitride traps. The improvement at low-fields may be due to an improved *a*-Si:H quality close to the *a*-Si:H/nitride interface. Since *a*-Si:H is deposited after the gate nitride, the quality of *a*-Si:H may be affected by that of the nitride underneath it. For both improved processes, the two distinct lifetime regimes are clearly evident.

A low gate voltage of ~7.5V (corresponding to $V_{GS} - V_{T0} = 5.3$ V, $E_{ins} \approx 2.5\times10^5$ V/cm and R_{sheet} =10MΩ/□) is required for driving high quality OLEDs at a luminance of 1000Cd/m^2 in a typical AM-OLED design (see section 4. 2). The current degradation of the improved *a*-Si:H TFTs at these drive conditions in saturation are plotted in Fig. 6.1 ($V_{T0} = 2.4 \pm 0.2$ V and 2.6 ± 0.2 V for the improved processes A and B, respectively). The threshold voltage shifts are extracted from the current degradation and extrapolated based on Eq. (6.3) (including the 2/3 factor) using linear least square fits (Fig. 6.3). These fits are then used to extrapolate the current degradation in Fig. 6.1 using Eq. (6.1b). The upper and lower error bounds corresponding to the standard deviation of errors in the least square fit ($+\sigma$ and $-\sigma$) are also plotted for the improved process B. An upper error bound of 2.2 times the standard deviation ($+2.2\sigma$) corresponds to 2 years and 1000 years of lifetime for 10% and 50% current decay, respectively. Assuming a normal distribution of errors, the $+2.2\sigma$ bound indicates a confidence of ~ 99% (~ 1% error) in prediction.

6.5 *Universal Lifetime Comparison Framework*

The presence of the two lifetime regimes for different *a*-Si:H TFT processes developed in our lab suggests that plotting the current decay lifetime versus the TFT channel sheet resistance can be used as a framework for comparing the lifetime of *a*-Si:H TFTs fabricated with different structures, process technologies or growth conditions. In this section, this is verified by plotting the *a*-Si:H TFT data from the literature in the context of this comparison framework. Next, it is shown that this comparison framework can be used for other TFT technologies as well.

6.5.1 Comparison with other *a*-Si:H TFTs

Converting the published plots of threshold voltage shift vs. time to current decay for *a*-Si:H TFTs reported in the literature [3][6][2][7][9][10] shows that at low fields (high channel sheet resistances), the lifetimes of our standard *a*-Si:H TFTs (red circles in Fig. 6.4) and those reported in the literature (green symbols in Fig. 6.4) are comparable. Our improved *a*-Si:H TFTs have significantly higher lifetimes, especially in the high-channel resistance regime, which is the one appropriate for driving OLEDs. This improvement is due to low defect creation rates in *a*-Si:H (and therefore more stable threshold voltages) as indicated from both small values of β (0.22 and 0.26 for the improved processes A and B, respectively, vs. 0.45 for the standard process) and large values of τ_0 (1.1×10^{8} and 4×10^{10}, vs. 2.8×10^{6} sec) extracted from the fits in Fig. 6.3. The low β of the improved TFTs physically corresponds to a sharper low energy tail of the distribution of bond energies, i.e. a lower density of weak bonds and thus a more stable material [5][11]. The large τ_0 implies a lower attempt frequency for bond breaking [11][12], which can be explained by a larger localization length of the electron wave-function in the case of stronger Si-Si bonds [12].

6.5.2 Comparison with other TFT Technologies

This comparison framework of lifetime vs. channel sheet resistance is more general than *a*-Si:H TFTs and can be applied to other TFTs as well. In contrast to direct comparison of threshold voltage stability, this approach is not affected by the different values of mobility, gate insulator capacitance, initial threshold voltage as well as the different values of gate stress voltages used for the TFTs being compared. The lifetime of various TFTs reported in the literature including organic [13][14][15] and metal-oxide devices [16][17][18][19] are given in Fig. 6.4 above. These lifetimes were determined by inspecting the published plots of TFT current decay vs. time or converting the published plots of TFT threshold voltage shift vs. time to plots of current decay, using Eq. (6.1a) or (6.1b) based on the TFT operation mode. A first-order extrapolation in time was performed on the data when necessary. Organic devices generally fall to the right due to their low mobilities and in the best case have a lifetime of ~3 days at a channel sheet resistance of 12.8 MΩ/□, several orders of magnitude below high-lifetime *a*-Si:H TFTs.

Metal-oxide devices with mobilities of the order of 1 cm^2/Vs have channel sheet resistance values close to that of *a*-Si:H and those with higher mobilities (10-15cm^2/Vs) fall to the left with the highest lifetime of ~100 days at a channel sheet resistance of 130 KΩ/□. It might be expected that high mobility metal oxide TFTs at low gate voltages will also have high lifetimes similar to our TFTs, but to the best of our knowledge they have not yet been reported in the literature.

6.6 *Summary and Conclusion*

In summary, at low channel electron density, the lifetime of *a*-Si:H TFTs is independent of the channel sheet resistance and depends on defect formation in the *a*-Si:H. In contrast, at high channel electron density, the lifetime decays with decreasing the channel sheet resistance due to electron trapping in the gate dielectric. At high channel sheet resistance, the extrapolated TFT lifetime can be raised to over 2 years and 1000 years for 10% and 50% current decay, respectively. This was achieved by including hydrogen dilution during growth to improve the quality of *a*-Si:H and the gate nitride. This comparison framework of lifetime versus channel sheet resistance is more general than *a*-Si:H TFTs and can be applied to other TFTs as well.

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Inverted TFT/OLED Integration on Glass and Clear Plastic

In the conventional TFT/OLED integration process implemented in Chapter 4 (Fig. 7.1), the driver TFT is connected to the OLED anode. This is because of three process constraints: (i) OLEDs must be deposited after fabrication of the TFT backplane because the TFT process severely damages the OLEDs, (ii) the best OLEDs are deposited from anode to cathode (anode as the first layer, followed by organic layers and cathode), and (iii) patterning the organic layers is not possible by conventional photolithography without damaging the organic layers. Since practical *a*-Si:H TFT are *n*-channel devices (due to the very low mobility of holes), the TFT terminal connected to the OLED in the conventional structure is the TFT source rather than the TFT drain. Therefore, the data

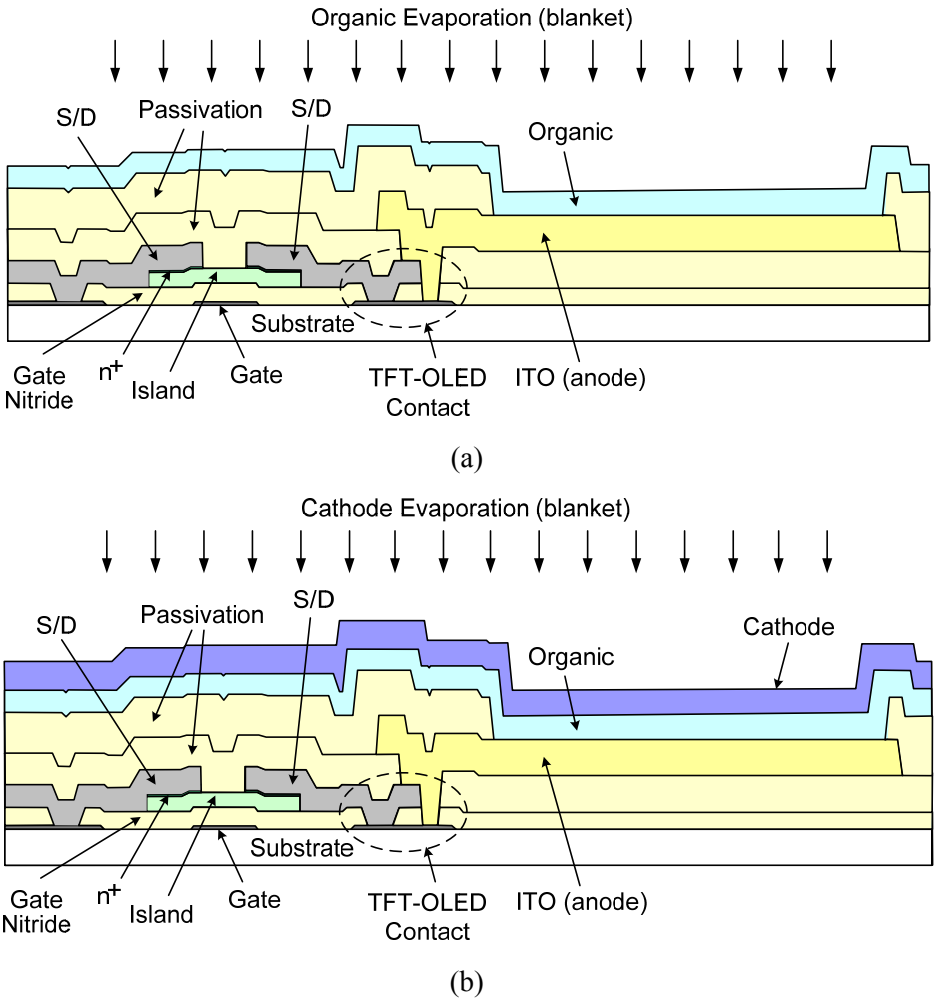


Fig. 7.1. Conventional AMOLED integration process. The substrate may be glass or clear plastic/nitride (a) organic evaporation and (b) cathode evaporation.

voltage is split across the gate-source of the driver TFT and the OLED (Fig. 7.2 (a)). As a result, high data voltages are required for driving the pixel and the pixel current depends on the OLED characteristics which change over time as a result of aging and may be different from device to device due to manufacturing issues [1][2]. The direct voltage programming of AMOLED pixels with *a*-Si:H TFTs requires a contact between the driving TFT and the OLED cathode (Fig. 7.2 (b)) which is conventionally not possible. Therefore either more expensive poly-Si technology must be used instead of *a*-Si:H (because p-channel TFTs are available in poly-Si technology) [3][4][5] or non-conventional OLEDs which can be deposited from cathode-to-anode are required [6][7].

In this chapter, a new "inverted" integration technique is presented which makes the direct programming possible by connecting the driver n-channel *a*-Si:H TFT to the OLED cathode, while still using conventional OLEDs with the anode as the lower electrode. As a result, the pixel drive current increases by an order of magnitude for the same data voltages and the pixel data voltage for turn-on drops by several volts. In addition, the pixel drive current becomes independent of the OLED characteristics so that OLED aging and device-to-device variations does not affect the pixel current. Furthermore, the new integration technique can be modified to allow substrate rotation during OLED evaporation which improves the pixel yield and uniformity. This new

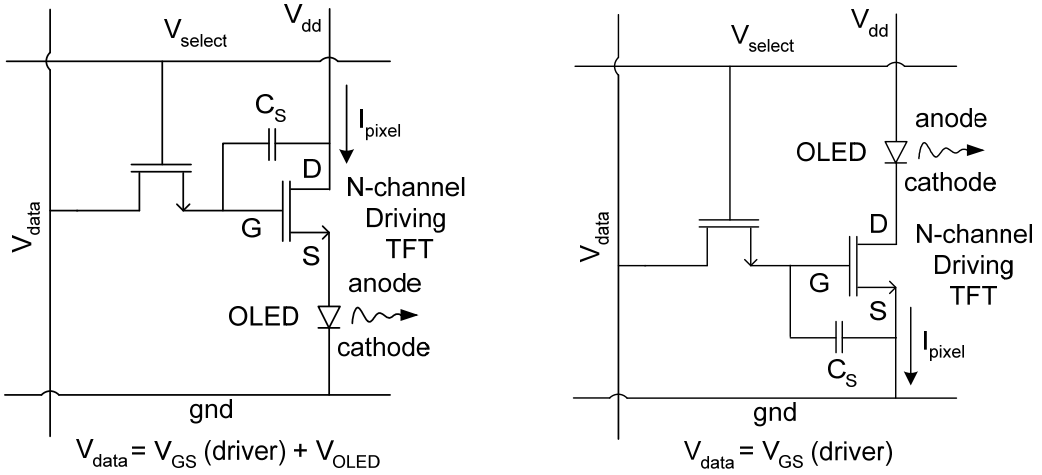


Fig. 7.2. Conventional and (b) Inverted AMOLED pixel. In the conventional pixel the driver TFT is connected to the OLED anode and the data voltage is split across the gate-source of the driver TFT and the OLED. In the inverted pixel the data voltage is transferred directly to the gate-source of the driver TFT.

integration technique is important for realizing active matrix OLED displays with *a*-Si:H technology and conventional bottom-anode OLEDs. Inverted AMOLED test arrays on both glass and plastic substrates will be presented in this chapter.

7.1 *Integration Process*

The schematic of the inverted AMOLED process is shown in Fig. 7.3. After processing the TFT backplane (including ITO as the OLED anode), insulating "separators" are formed by patterning a layer of positive photoresist using conventional photolithography. As shown in Fig. 7.3 (a), the organic layers are then evaporated at an angle in such a way that an interconnect extension connected to the driving TFT is not coated with the organic layers, taking advantage of the shadowing effect of the separator. 10μm-thick photoresist separators and standard TPD/ALQ_3 organic layers were used for this purpose. Then, as shown in Fig. 7.3 (b), the cathode (Mg-Ag/Ag) is evaporated at an angle opposite to the organic evaporation angle to form the OLED cathode and also to contact the interconnect extension. Therefore the electrical circuit of Fig. 7.2 (b) is realized.

7.2 *Electrical Characteristics*

The measured DC characteristics of *a*-Si:H AMOLED pixels integrated with the conventional and inverted processes are compared in Fig. 7.4. First, in the inverted structure, the pixel drive current, I_{pixel}, turns on at V_{data}=1.7V (corresponding to the threshold voltage of the driver TFT) which is considerably lower than the conventional design where I_{pixel} turns on at V_{data}=4.8V (corresponding to the threshold voltage of the driving TFT (1.7V) plus the turn-on voltage of the OLED (3.1V)). Second, in the inverted structure, at typical operation current levels of few microamperes, the pixel current is higher by an order of magnitude than the current in the conventional structure for the same data voltages. This is because in the conventional design the data voltage is split across the OLED and the gate-source of the driving TFT, but in the inverted design it is converted directly to the gate-source voltage of the driving TFT. SPICE simulations confirm the experimental behavior of the inverted pixels.

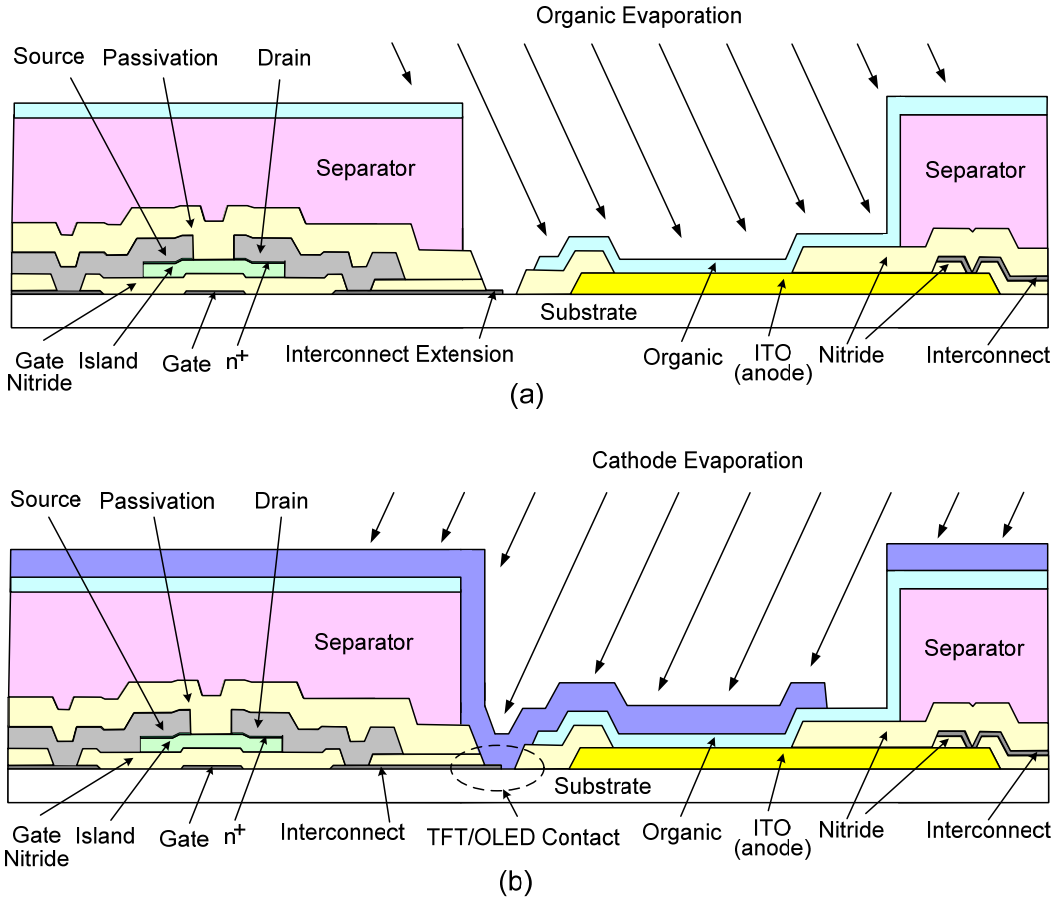


Fig. 7.3. Schematic cross-section of the fabricated new "inverted" AMOLED structure of Fig. 7.2 (c), during the evaporation of (a) the organic layers and (b) cathode.

To further verify the independence of the pixel driving current from the OLED characteristics, we compared the drift in the output characteristics of conventional and inverted AMOLED pixels after storing them in a non-ideal environment. The AMOLED arrays, which were *not* encapsulated, were stored in a nitrogen box with a relatively high oxygen content of about 100ppm, for six months. The storage condition will not alter *a*-Si TFT's, but the oxygen content and humidity lead to considerable OLED degradation. Fig. 7.5 (a) shows a large drop in I_{pixel} of conventional AMOLED pixels after storage. This is because the OLED degradation causes an increase in the voltage drop across the OLED for a given current, and thus a higher voltage is required to achieve the same V_{GS} (driver) and the same I_{pixel} in the driver TFT. In contrast, I_{pixel} of inverted AMOLED pixels (Fig. 7.5(b)) is not affected by OLED degradation, an observation verifying that I_{pixel} is independent of the OLED characteristics.

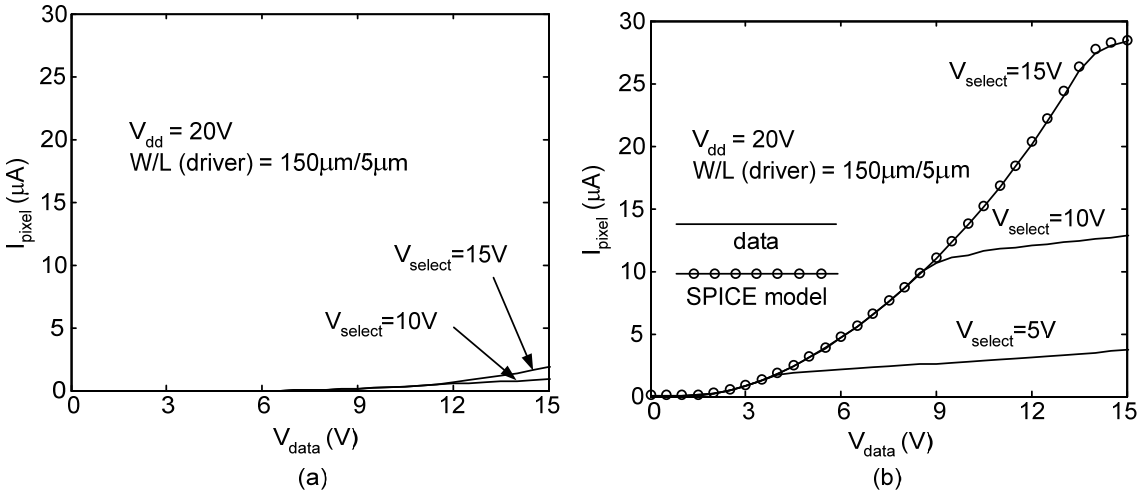


Fig. 7.4. Measured pixel current (I_{pixel}) as a function of the programmed data voltage (V_{data}) of (a) a conventional *a*-Si:H AMOLED pixel shown in the pixel circuit of Fig. 1(b), and (b) an inverted *a*-Si:H AMOLED pixel shown in the pixel circuit of Fig. 1(c). The SPICE simulation for V_{select}=15V is also plotted in (b).

7.3 *Modified Inverted Integration*

The inverted integration presented above is prone to pixel yield loss and non-uniformity since it does not allow substrate rotation during the evaporation of organic layers and cathode. Rotation of the substrate during the evaporation of the cathode is desired for good step coverage and thickness uniformity. To overcome this problem, we modified the integration process by using insulating separators with overhangs (Fig. 7.6) using a

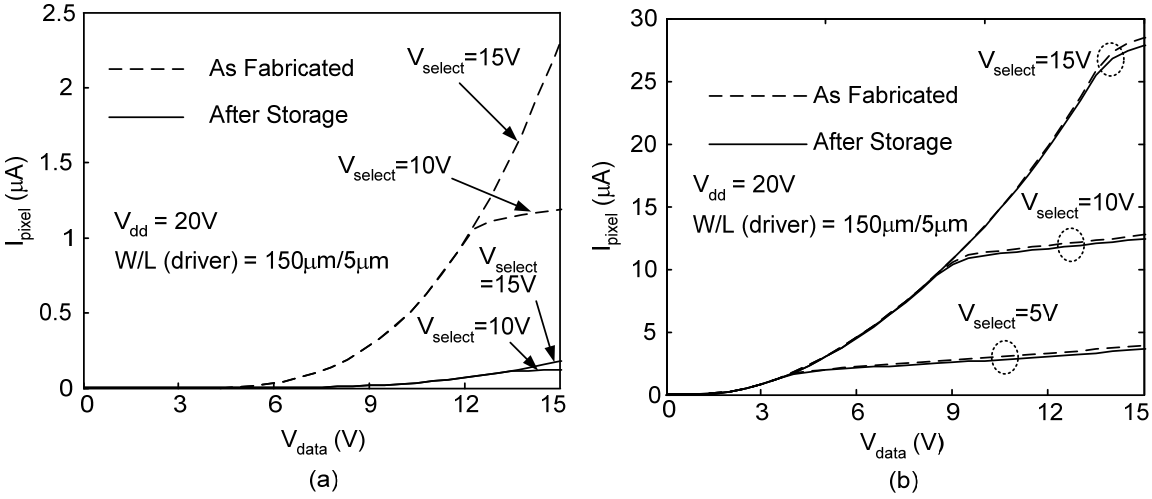


Fig. 7.5. The effect of the drift in OLED characteristics caused by storing un-encapsulated devices in an environment relatively high in oxygen and humidity, on the pixel driving current for (a) conventional and (b) inverted AMOLED pixels.

double-layer photoresist process. We used 10µm high separators with 5µm wide overhangs. The organic layers are then evaporated at normal incidence and the substrate is rotated during organic evaporation (Fig. 7.6(a)). The overhang shadows an exposed interconnect which is connected to the driver TFT. The cathode is evaporated next at an angle while the substrate is being rotated (Fig. 7.6(b)) and therefore the OLED cathode is connected to the exposed interconnect and the inverted structure of Fig. 1(c) is realized.

Fig. 7.7 shows an optical micrograph of a modified inverted pixel prior to organic and cathode evaporation. AMOLED test arrays fabricated using the inverted integration process shown in Fig. 7.3 and the modified inverted process shown in Fig. 7.6 are compared in Fig. 7.8 (a) and (b), respectively. It is observed that the modified inverted process results in a higher pixel yield and better uniformity. A quarter video graphics

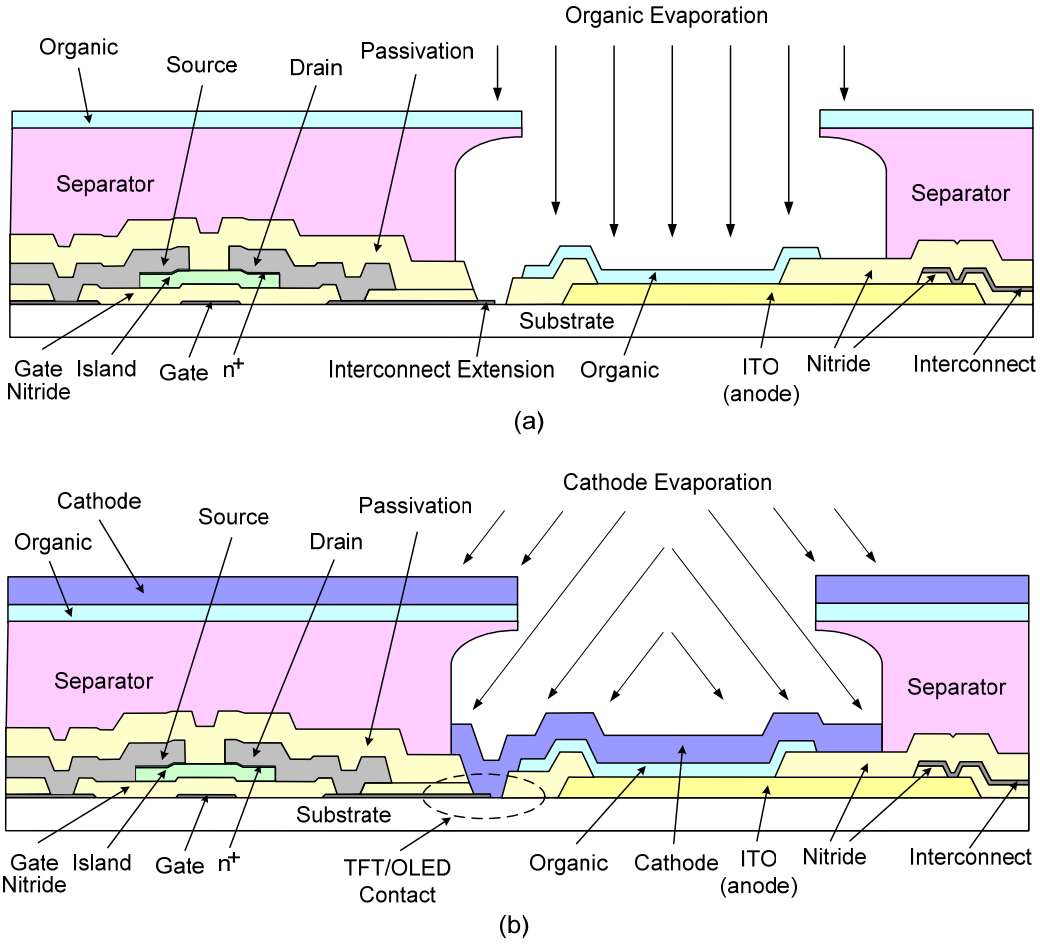


Fig. 7.6. Schematic cross-section of the "modified" inverted AMOLED pixel, during the evaporation of (a) the organic layers and (b) cathode.

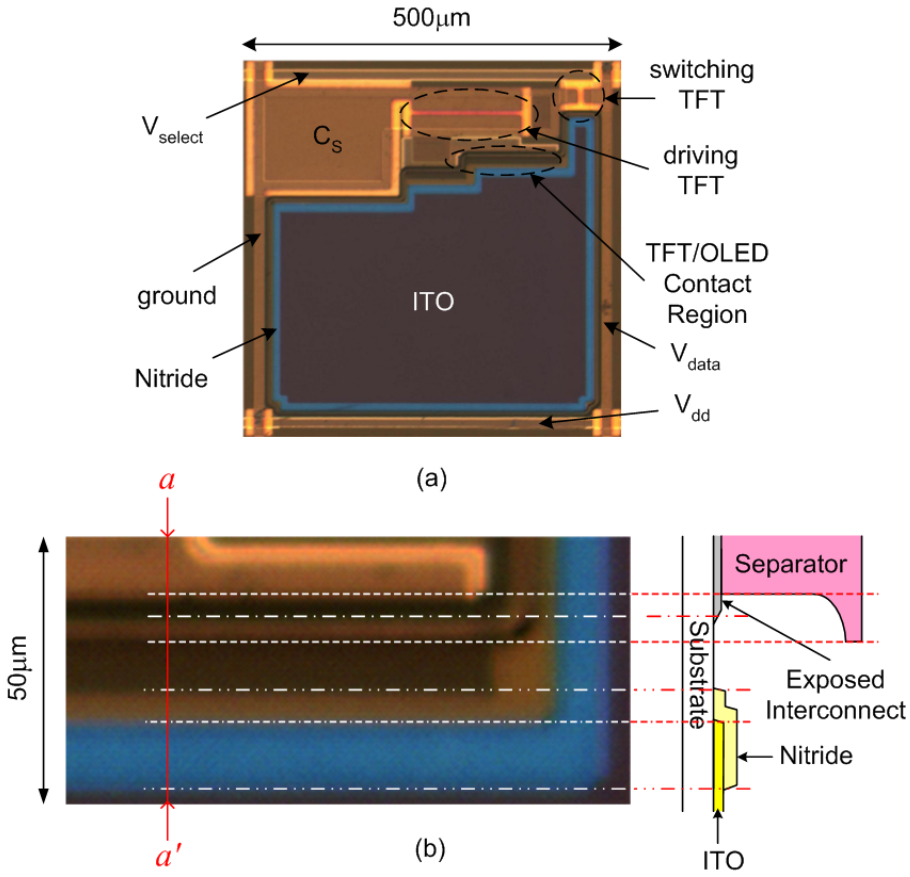


Fig. 7.7. (a) Optical micrograph of a modified inverted pixel (Fig. 7.6) prior to OLED evaporation and (b) higher magnification of the TFT/OLED contact region along with schematic cross-section along line $a - a'$. The non-modified inverted structure (Fig. 7.3) has the same geometry, except for the separator which lacks the overhang.

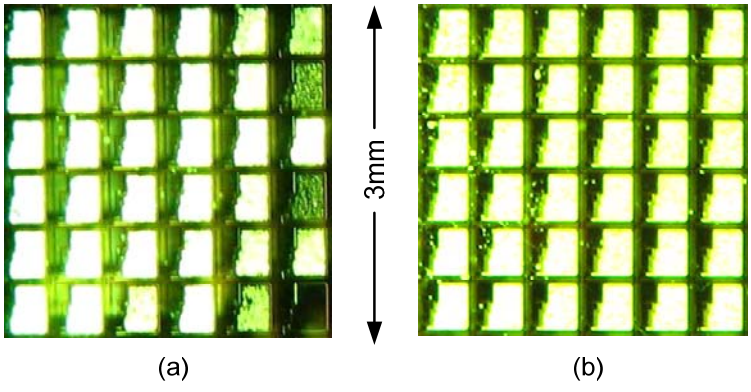


Fig. 7.8. Comparison of the AMOLED pixels fabricated by the inverted process of Fig. 7.3 (no rotation) and the modified inverted process of Fig. 7.6 (with rotation).

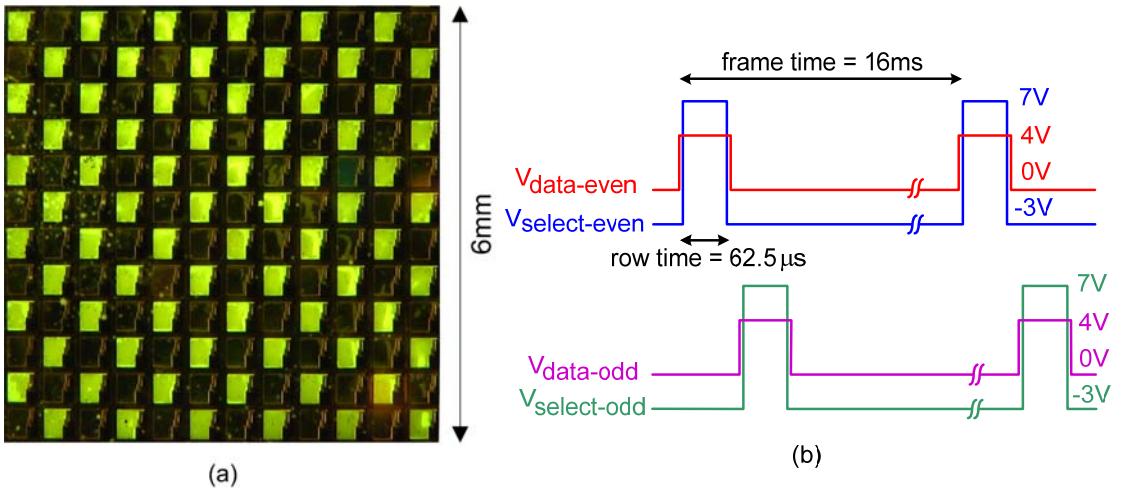


Fig. 7.9. QVGA checkerboard demonstration of the AMOLED pixels fabricated by the modified inverted process presented in Fig. 7.6 and (b) the QVGA drive signals.

array (QVGA) checkerboard demonstration of a 12×12 AMOLED test array fabricated using the modified inverted integration is presented in Fig. 7.9 (a) and (b) showing high pixel yield and uniformity. The checkerboard is a severe test of AMOLED performance, as it simultaneously verifies the successful programming of the driver TFT, sufficient storage of the data voltage over the frame time, low off-current of the switching the TFT, and low cross-talk between the adjacent rows and/or columns.

7.4 *Integration on Clear Plastic*

Apart from a different pixel layout to accommodate the interconnect extensions and overhangs, the integration on clear plastic is in principle the same as that on glass. However, a minor process modification in necessary. The inverted AMOLED process on glass is started with ITO-coated glass which is commercially available. However, in our AMOLED process on clear plastic, we deposit the ITO after the fabrication of the TFT backplane. This is to avoid exposing the ITO layer to the stress from TFT stack which may cause cracking in the ITO layer. Taking this into consideration gives preference to laying out the interconnect extension in the top metal level rather the bottom level. This requires a shorter step to be covered by the cathode during angle evaporation to connect the OLED to the interconnect extension. The schematic cross section of the modified inverted AMOLED process on clear plastic is shown in Fig. 7.11 and an optical micrograph of the fabricated backplanes is given in Fig. 7.12.

7.5 *Electrical Characteristics on Clear Plastic*

The electrical characteristics of an inverted pixel on clear plastic are compared to a conventional pixel on clear plastic in Fig. 7.12, showing a significant increase in the drive current and considerable reduction of the turn-on voltage as expected. As explained above in section 7.2 for a similar comparison on glass substrates, this is because in the conventional design, the data voltage is split across the gate-source of the driver TFT and the OLED, but in the inverted design, the data voltage is transferred directly to the gate source of the driver TFT. The optical micrograph of the finished inverted AMOLED test arrays on clear plastic with a 250°C backplane process is given in Fig. 7.13.

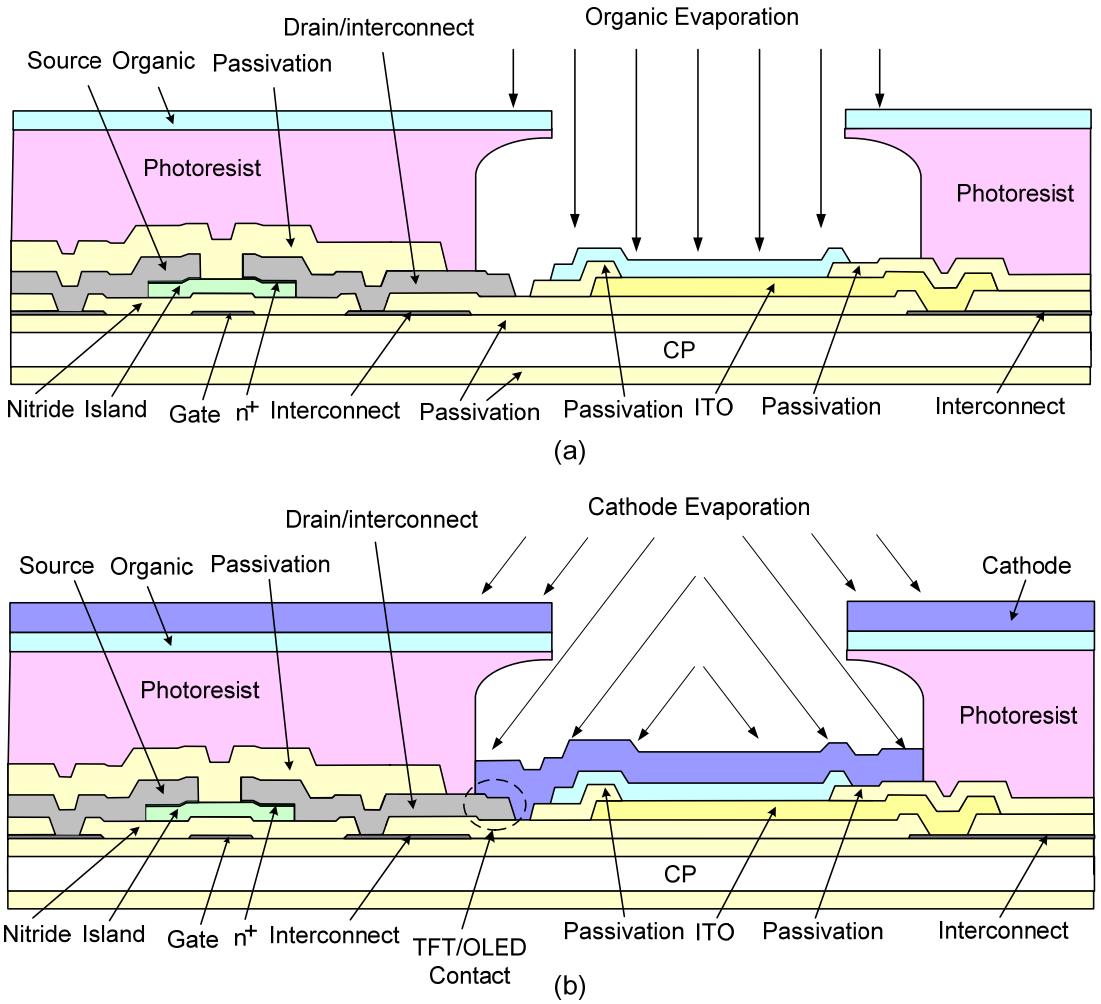


Fig. 7.10. Schematic cross-section of an inverted *a*-Si:H AMOLED pixel on clear plastic (a) during the evaporation of the organic layers and (b) during the evaporation of the cathode.

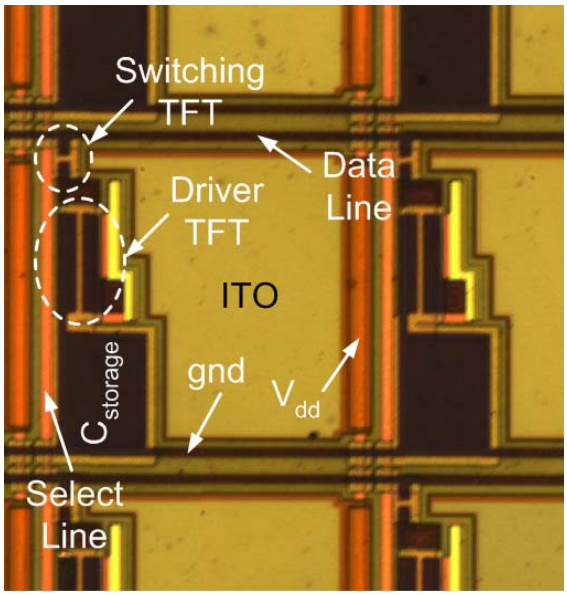


Fig. 7.11. Optical micrograph of inverted *a*-Si:H TFT AMOLED backplane array on clear plastic (prior to OLED evaporation).

7.6 *Electrical Reliability*

The electrical stability (operation lifetime) of the inverted and conventional AMOLED pixels fabricated on clear plastic is compared in Fig. 7.14. The pixels were stressed in DC, with constant V_{select} and V_{DD}, and various constant values of V_{data}. The pixel current and luminance were normalized by their initial values for each measurement. The predictions of the pixel current/luminance decay calculated based on the measured drift of the individual TFTs and OLEDs are also plotted in the figure and are in good agreement with the experimental data. These calculations are presented in the next section. As seen in the plots, the inverted pixels fabricated in this work have higher lifetimes than their conventional counterparts. This can be explained as follows.

In the inverted structure, the pixel current is independent of the OLED characteristics and the drop of the pixel current is due to the threshold voltage increase of the driver TFT. In the conventional structure, the threshold voltage rise of the driver TFT reduces the pixel current, but the presence of the OLED at the source of the driver TFT affect the drop of the pixel current as well. The presence of the OLED has two opposite effects on the drop of the pixel current. The first effect is the increase of the OLED turn on voltage over time (due to OLED degradation) which tends to increase the voltage across the OLED and therefore reduce the voltage across the gate-source of the driver

TFT, favoring the drop of the pixel current over time. The second effect is the lowering of the voltage across the OLED due to the pixel current drop over time (note the OLED current equals the pixel current) which tends to increase the gate-source voltage of the driver TFT and oppose the pixel current drop. In other words, the OLED creates a negative voltage feedback opposing the pixel current drop. Note that the first effect is due to the degradation of the OLED over time while the second effect is due to the DC characteristics of the OLED (purely because an OLED is a device whose voltage decreases by decreasing the current bias applied to it). If the first effect is dominant, inverted pixels have higher lifetimes than the conventional pixels and vice versa. The experimental data of Fig. 7.14 indicate that the first effect is dominant for the TFTs and OLEDs used in this work.

7.7 *Prediction of the Pixel Reliability*

As will be shown in this section, the electrical reliability of the AMOLED pixel can be predicted from the characteristics and the drift of the individual TFT and OLED components. This approach is based on measuring the drift of the individual TFTs and OLEDs at constant bias stress and applying the knowledge of the time dependence and bias dependence of the TFT and OLED degradation to the measurement results in order to predict the drift of the pixel characteristics where the bias conditions on the TFTs and

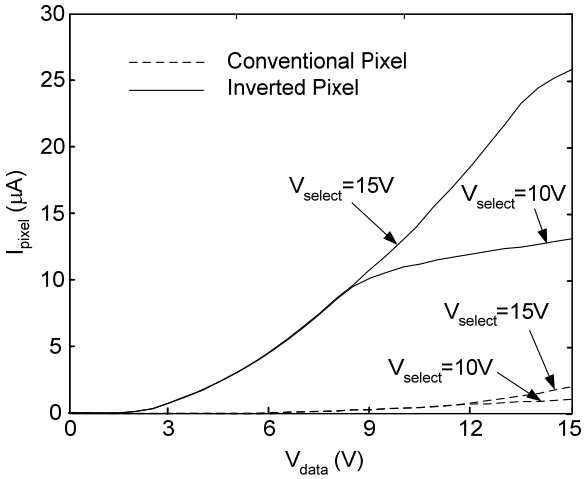


Fig. 7.12. Comparison of the DC output characteristics of the inverted and conventional AMOLED pixel arrays on clear plastic, showing a high drive current and low turn on voltage for the inverted pixels.

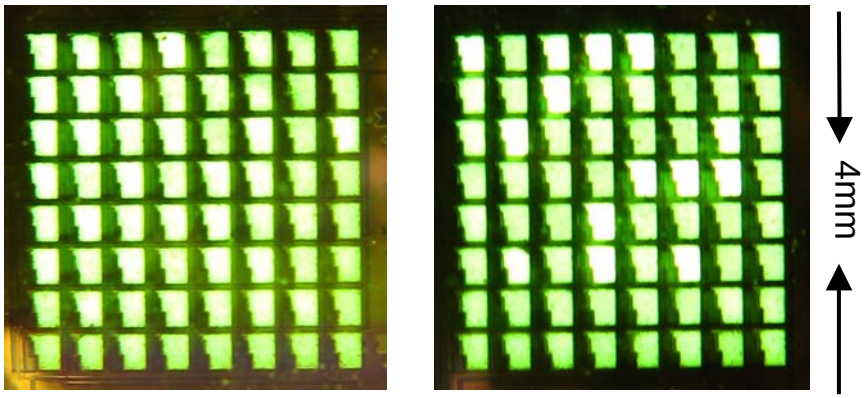


Fig. 7.13. Optical image of 8×8 inverted AMOLED arrays on clear plastic fabricated with a backplane process temperature of 250°C.

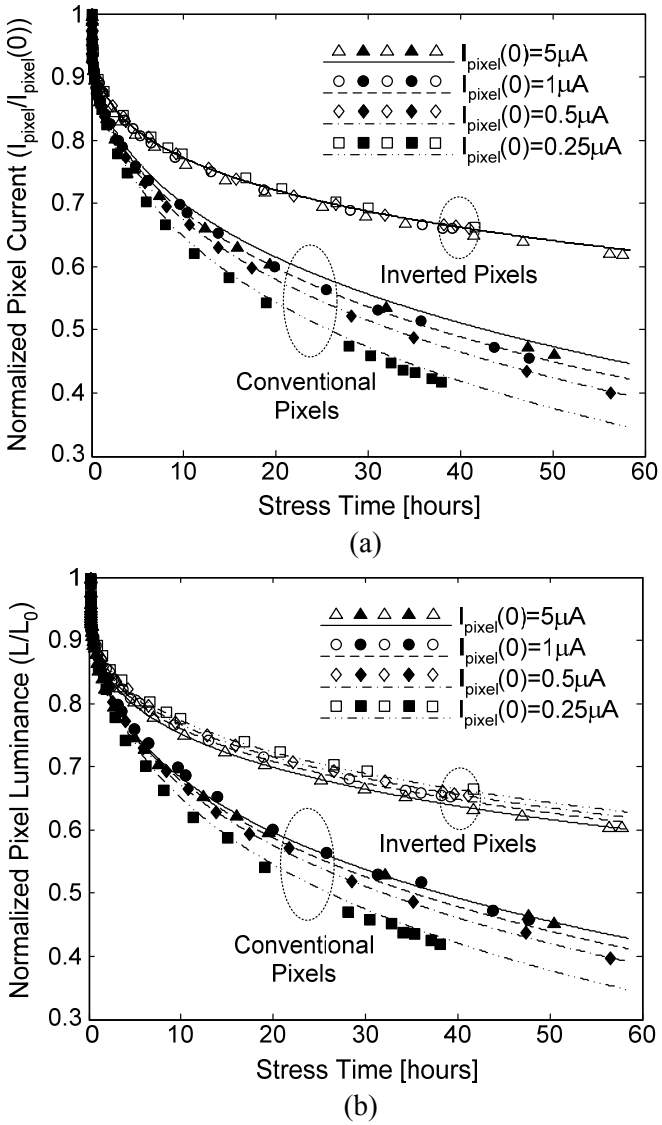


Fig. 7.14. (a) Normalized pixel current drop and (b) normalized pixel luminance decay for the conventional and inverted pixels for several initial pixel currents.

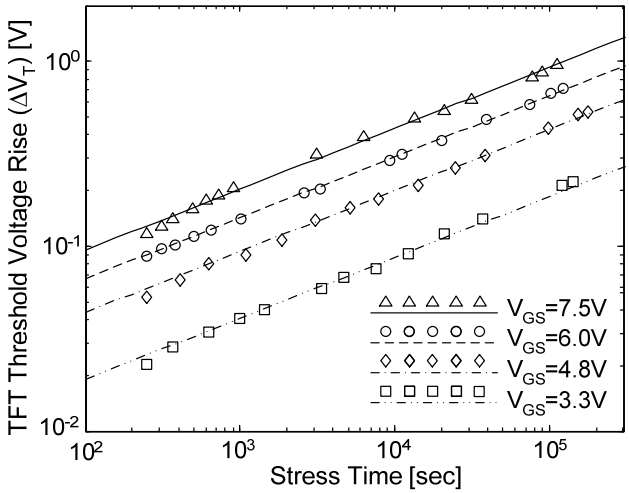


Fig. 7.15. Threshold voltage shift of the individual test TFTs vs. time at several DC gate stress voltages (symbols: data points, lines: model based on Eq. 7. 3). The extracted parameters are β = 0.33 and $A = 4.16\times10^{-3}$ $(\text{sec})^{-\beta}$.

OLEDs change over time during operation. The measurement of the electrical characteristics and the drift of the individual TFTs and OLEDs are covered in subsections 7.7.1 andFig. 7.15.7.7.2, respectively. The circuit equations and the prediction of the pixel current drop are covered in subsection Fig. 7.17.7.7.3.

7.7.1 TFT Characteristics and Drift

The TFT current is modeled with an MOS equation for simplicity (μ_n is the electron mobility, C_{SiNx} the gate nitride capacitance and W/L the channel width to length ratio. For our test TFTs, V_{T0} = 2.5V, μ_n = 0.65cm^2/Vs, W/L = 150µm/5µm and $C_{SiNx} = 2\times10^4$ pF/(µm)^2 corresponding to a 300nm-thick gate nitride with a relative dielectric constant of 7.5) (Section 3.2)

$$I_{TFT} = k(V_{GS} - V_T)^2,\ k = \frac{1}{2}\mu_n C_{SiNx}\frac{W}{L} \tag{7.1}$$

The degradation of *a*-Si:H TFTs at low gate electric fields typically used for driving OLEDs is dominated by creation of defects in *a*-Si:H near the *a*-Si:H/*a*-SiN_x:H interface resulting in a stretched exponential time dependence of the threshold voltage shift (ΔV_T) [8][9] (Section 5.2)

$$\Delta V_T(t) = \Delta V_T(\infty)\times(1-\exp[-(t/\tau_{TFT})^{\beta}]) \tag{7.2}$$

where $\Delta V_T(\infty) = (V_{GS} - V_{T0})$, V_{GS} is the constant gate-source voltage bias stress, V_{T0} the initial threshold voltage, and τ_{TFT} and β are constants (with negligible dependence on V_{GS}). This means that the TFT threshold voltage increases with time under bias until the TFT current drops to zero, considering the very large number of available weak Si-Si bonds that may break and convert into defects given sufficient time. As the time constant τ_{TFT} is large (typically of the order of 1 year), Eq. 7.2 may be approximated by a power law relation for relatively short stress times ($t << \tau_{TFT}$) [9][10]

$$\Delta V_T(t) = A(V_{GS} - V_T) \times t^{\beta} \tag{7.3}$$

where $A = (\tau_{TFT})^{-\beta}$ is a constant (with negligible dependence on V_{GS}). Our TFT measurement data closely fit Eq. 7.3, as shown in Fig. 7.15. The extracted parameters are listed in Table 7. 1. If V_{GS} varies with time rather than being constant (which may be the case in a pixel circuit), the rate of the drift in the threshold voltage varies with V_{GS}, with threshold voltage shift being faster at higher V_{GS}, as indicated by Eq. 7.2

$$\frac{dV_T}{dt} = \frac{d\Delta V_T}{dt} = A\beta\left(V_{GS}(t) - V_T\right)t^{\beta-1} \tag{7.4}$$

And the TFT current may be expressed as

$$I_{TFT}(t) = k\left(V_{GS}(t) - V_T(t)\right)^2 \tag{7.5}$$

7.7.2 OLED Characteristics and Drift

OLEDs used for this study were standard bi-layer small-molecule OLEDs with TPD (N,N'-Bis-(3-methylphenyl)-N,N'-diphenylbenzidine) hole transport layer and Alq_3 (aluminum tris-(8-hydroxyquinoline)) electron transport/emissive layer. Indium-tin-oxide (ITO) was used as the OLED anode and Mg/Ag as the cathode.

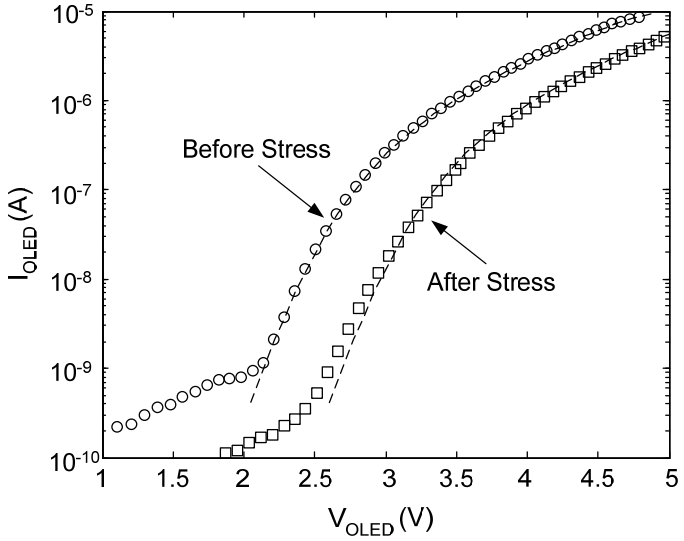
An OLED is typically modeled as a diode with a non-ideality factor, n, and a reverse saturation current, I_S (K is the Boltzmann constant, T the absolute temperature and q the electron charge) [11]

$$V_{OLED} = \frac{nKT}{q}\ln\left(1 + I_{OLED}/I_S\right) \tag{7.6}$$

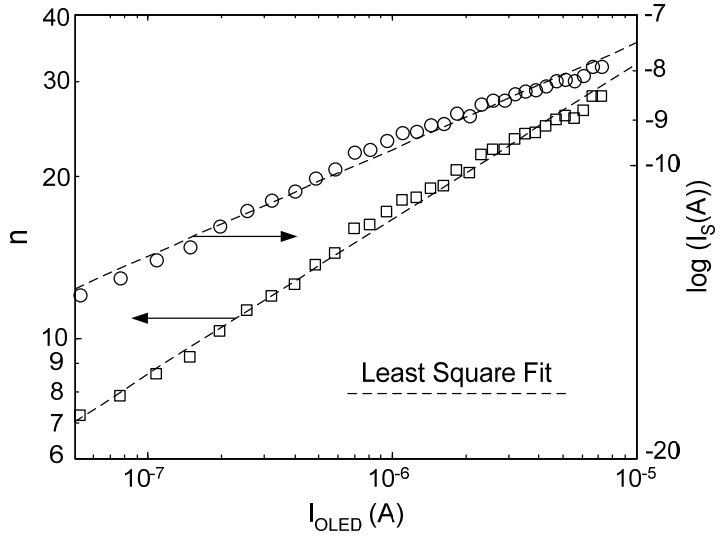
or equivalently

$$I_{OLED} = I_S\left(\exp\left(qV_{OLED}/nKT\right) - 1\right) \tag{7.7}$$

In this simple model, n and I_S are constants. However, as can be readily seen in Fig. 7.16 (a), the slope of the OLED I-V curve in a semi-logarithmic plot (and therefore n) is not rigorously constant. Therefore a more accurate OLED model requires variable n and I_S parameters. For a close fit to the experimental data, we extract n and I_S as functions of



(a)



(b)

Fig. 7.16. (a) The I-V curve of the individual test OLEDs before and after constant current stress (symbols: data points, lines: model). This shows that the effect of DC current stress may be modeled as a horizontal shift in the I-V characteristics, and (b) the extracted n and I_S based on Eq. 7.8 and Eq. 7.9.

OLED current, I_{OLED} (Fig. 7.16 (b)). First, n is extracted assuming small I_S ($I_S << I_{OLED}$)

$$n = \frac{q}{KT}\frac{\partial V_{OLED}}{\partial \ln\left(1 + I_{OLED}/I_S\right)} = \frac{q}{KT}\left(I_{OLED} + I_S\right)\frac{\partial V_{OLED}}{\partial I_{OLED}} \cong \frac{q}{KT} I_{OLED}\frac{\partial V_{OLED}}{\partial I_{OLED}} \qquad (7.8)$$

And second, knowing n as a function of I_{OLED}, I_S is extracted as well

$$I_S = \frac{\partial I_{OLED}}{\partial\left(\exp\left(qV_{OLED}/(nKT)\right) - 1\right)} = \frac{nKT}{q}\exp\left(-qV_{OLED}/(nKT)\right)\frac{\partial I_{OLED}}{\partial V_{OLED}} \qquad (7.9)$$

As seen from Fig. 7.16 (b), at any OLED current (I_{OLED}), the extracted $I_S << I_{OLED}$, so the approximation used in Eq. 7.8 is valid. The notion of modeling an OLED as a diode is purely phenomenological and does not reflect the physics of carrier transport in the OLED. This is evident from the extracted n values which are typically much larger than 2, in contrast with diodes where $1 \le n \le 2$.

OLEDs degrade in two generally independent ways. Under constant DC current bias stress, (i) the OLED operation voltage increases and (ii) the OLED luminance (or equivalently external quantum efficiency) drops.

The OLED operation voltage rise is attributed to migration of metal ions from the OLED anode into the organic material or degradation of OLED cathode [12][13]. Here it is assumed that stressing the OLED does not change n and I_S and results only in a

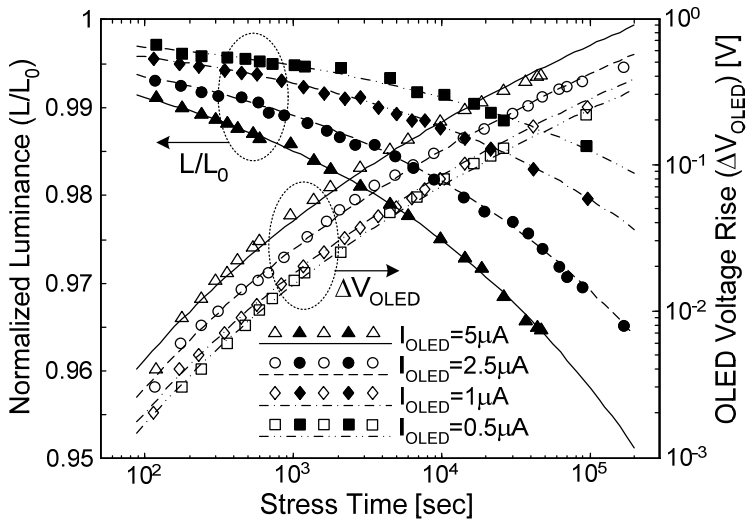


Fig. 7.17. Operation voltage rise and luminance degradation of the individual test OLEDs at several DC stress currents (symbols: data points, lines: model based on Eqs. 6.10, 6.13, 6.14 and 6.15. The extracted parameters are α = 0.28, C = 0.1 sec(μA)$^{-\delta}$, δ = –2, B = 54 μV(μA)$^{-\gamma}$ [log(sec)]$^{-\lambda}$, γ = 0.44 and λ = 5.4.

horizontal shift of the OLED I-V curve, denoted as $\Delta V_{ON}(t)$, which is a good assumption especially at typical OLED operation currents of the order of micro-amperes (OLED area = 500μm×500μm) (Fig. 7.16(a)). Under constant DC current bias, the following empirical relation results in a close fit with the data for the test OLEDs (Fig. 7.17)

$$\Delta V_{ON}(t) = B\left(I_{OLED}\right)^{\gamma}\left(\log t\right)^{\lambda} \tag{7.10}$$

where B, γ and λ are constants. The extracted parameters are listed in Table 7. 1. If I_{OLED} varies with time rather than being constant (which may be the case in a pixel circuit), the rate of the horizontal shift of the OLED IV curve varies with I_{OLED}, with the shift being faster at higher I_{OLED} as indicated by Eq. 7.5

$$\frac{d\Delta V_{ON}}{dt} = B\lambda\left(I_{OLED}(t)\right)^{\gamma}(\log e)t^{-1}\left(\log t\right)^{\lambda-1} \tag{7.11}$$

And, the voltage across the OLED may be expressed as

$$V_{OLED}(t) = \Delta V_{ON}(t) + \frac{nKT}{q}\ln\left(1 + I_{OLED}(t)/I_S\right) \tag{7.12}$$

The OLED luminance degradation is attributed to the formation of quenching centers in the organic material [12][13] and results in a stretched exponential time dependence of the OLED normalized luminance [14][15]:

$$\frac{L}{L_0}(t) = \exp[-\left(t/\tau_{OLED}\right)^{\alpha}] \tag{7.13}$$

where L is the OLED luminance measured under constant current bias, L_0 the initial luminance and τ_{OLED} and α are constant at a constant current. Unlike Eq. 7.2, Eq. 7.13 may not be approximated by a power law relation because the time constant τ_{OLED} is comparable to the typical stress times. In addition, while the dependence of α on the stress current is negligible, the dependence of τ_{OLED} on the stress current may not be neglected. For our test OLEDs we find the following empirical dependence on the stress current, fitting closely to the experimental data (Fig. 7.17)

$$\tau_{OLED} = C\left(I_{OLED}\right)^{\delta} \tag{7.14}$$

TFT Threshold Voltage Drift		**OLED Turn-ON Voltage Drift**			**OLED Efficiency Drift**		
A [(sec)$^{-\beta}$]	β	B [μV(μA)$^{-\gamma}$]	γ	λ	α	C [sec(μA)$^{-\delta}$]	δ
4.16×10^{-3}	0.43	54	0.44	5.4	0.28	0.1	-2

Table 7. 1. TFT and OLED drift parameters extracted from Fig. 7.15 and Fig. 7.17.

where C and δ are constants. The extracted parameters are again listed in Table 7. 1. If I_{OLED} varies with time, the rate of the normalized OLED luminance degradation is

$$\frac{d(L/L_0)}{dt} = -\alpha[\tau_{OLED}(t)]^{-\alpha} t^{\alpha-1} \exp[-(t/\tau_{OLED}(t))^{\alpha}] \tag{7.15}$$

where $\tau_{OLED}(t) = C[I_{OLED}(t)]^{\delta}$.

7.7.3 Circuit Equations

As seen from the pixel circuits of Fig. 7.2 (a) and Fig. 7.2 (b)

$$\begin{cases} V_{data} = V_{GS} & (Inverted\ Pixel) \\ V_{data} = V_{GS} + V_{OLED} & (Conventional\ Pixel) \end{cases} \tag{7.16}$$

$$I_{pixel} = I_{TFT} = I_{OLED} \quad (Both\ Pixels) \tag{7.17}$$

To compare the reliability of the two pixel structures by comparing their operation lifetime for the same initial pixel currents. Using Eq. 7.16 to obtain the same initial pixel currents, the data voltage must be higher for the conventional pixel than the inverted pixel by the initial OLED voltage in the conventional pixel (the subscripts "*inv*" and "*conv*" refer to the inverted and conventional pixels, respectively).

$$\begin{cases} I_{pixel,inv}(0) = I_{pixel,conv}(0) = I_0 \\ V_{data,conv} = V_{data,inv} + V_{OLED,conv}(0) \end{cases} \tag{7.18}$$

Using Eqs. 6.16, 6.17 and 6.18, the pixel current for the inverted and conventional structures are then given by

$$\begin{cases} I_{pixel,inv}(t) = k(V_{data,inv} - V_{T0} - \Delta V_{T,inv}(t))^2 \\ I_{pixel,conv}(t) = k(V_{data,conv} - V_{T0} - \Delta V_{T,conv}(t) - V_{OLED,conv}(0) - \Delta V_{OLED,conv}(t))^2 \end{cases} \tag{7.19}$$

The pixel current decay and luminance decay may be predicted by finding simultaneous solutions to the set of TFT/OLED drift differential equations (Eqs. 6.4, 6.11 and 6.15), given the circuit equations (Eqs. 6.16 and 6.17), and the device equations (Eqs. 6.1 and 6.12), which may be done numerically. These predictions are also plotted in Fig. 7.14 (a) and (b) and are consistent with the experiment. It is clear that this approach is not restricted to the particular TFT/OLED characteristics or the particular time dependence and bias dependence of the TFT/OLED drift rates measured and modeled for our test devices. This approach may be used for any given TFT/OLED characteristics and TFT/OLED decay rates (known as functions of time and bias).

7.8 *Summary and Conclusion*

In summary, a new integration technique was presented for the direct programming of AMOLED pixels with *a*-Si:H TFTs and standard bottom-emission OLEDs. This technique is based on connecting the OLED top contact (cathode) to the underlying TFT. As a result, the drive current of the fabricated pixels becomes independent of the OLED characteristics and therefore is not affected by OLED aging. Furthermore, as a result of direct programming, the data voltages required for typical pixel operation currents (of the order of $1mA/cm^2$) drop from about 15V to about 5V. This integration approach to the direct programming of *a*-Si:H AMOLED pixels is important for the realization of AMOLED displays with *a*-Si:H TFT backplanes as it allows the use of conventional bottom-emission OLEDs. Finally, an approach was presented to predict the degradation of the AMOLED pixel current and luminance based on the electrical characteristics and stability of the individual TFTs and OLEDs.

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Summary and Future Work

This chapter summarizes the work presented in thesis, and provides suggestions for future work.

8.1 *Summary and Conclusion*

As discussed in the previous chapters, *a*-Si:H TFTs are currently in widespread production of backplanes for active-matrix LCD displays. However, driving OLEDs is far more demanding in terms of the required TFT lifetime. Therefore the conventional thinking has been that the lifetime of *a*-Si:H TFTs is too short for driving OLEDs for commercial display products. This thesis shows that the conventional thinking is most probably not true. As demonstrated in this thesis, *a*-Si:H TFTs may qualify for driving OLEDs provided that special considerations are taken into account at the materials growth level, device fabrication level and integration level. Most critical are modifications that found to be necessary to the materials growth conditions. The main conclusions of this work may be summarized as follows:

(i) High process temperatures are critical for high *a*-Si:H TFT lifetimes, underscoring the importance of the new high-temperature clear plastic substrates for the realization of flexible AMOLED displays. Controlling the mechanical stress and adhesion of the layers to avoid cracking and delamination at high process temperatures on clear plastic is also of critical importance.

(ii) Appropriate hydrogen dilution during the PECVD growth of the *a*-Si:H channel and the gate nitride combined with high process temperatures for the growth of the gate nitride can raise the drive-current half-life of the standard *a*-Si:H TFTs from lower than a month to over 1000 years. The 1000-year half-life of the improved a-Si:H TFTs is well above the 30-year half-life of most stable high-efficiency OLEDs suggesting that the improved *a*-Si:H TFTs may qualify for the production of AMOLED display backplanes.

(iii) Comparison with the literature shows that the drive-current lifetime of the improved *a*-Si:H TFTs is far in excess of those of other TFT technologies. In conjunction with the advantage of the existing industrial infrastructure for the production of *a*-Si:H TFTs, the high lifetime of the improved a-Si:H TFTs gives

them a clear edge over other TFT technologies which are currently under research and development rather than in large-scale production.

(iv) An "inverted" integration technique may be used to allow for the direct programming of AMOLED displays based on *a*-Si:H TFTs and standard bottom-emission OLEDs. Direct programming enhances the drive current of the pixel significantly for the same programming voltages and reduces the turn-on voltage of the pixel. In addition, it makes the pixel current independent of the OLED characteristics which may change over time or vary from device to device in manufacturing.

Based on these findings, this thesis suggests that *a*-Si:H TFTs may be seriously considered for the commercial production of AMOLED display backplanes both on rigid and flexible substrates.

8.2 *Future Work*

Future work is suggested in the follows areas:

(i) The high lifetime of the improved *a*-Si:H TFTs suggests that the quality of *a*-Si:H is improved close to the *a*-Si:H/*a*-SiN_x:H interface. This improvement was attributed to a lower density of weak Si-Si bonds as inferred from the stretched exponential time dependence of the TFT threshold voltage shift. Within the weak bond model, a lower density of weak Si-Si bonds corresponds to a lower valence band-tail density of states at low binding energies. Measuring this low-energy tail can therefore verify or rule out the link between the stretched exponential relaxation and the weak bond model which is still controversial. Such a measurement is however not straightforward and a specially designed spectroscopy technique which is surface sensitive is required.

(ii) The electrical characteristics of *a*-Si:H TFTs such as threshold voltage and mobility are closely related to the conduction band tail density of states. There is significant evidence that the conduction band tail density of states is affected by the quality of the *a*-Si:H/*a*-SiN_x:H interface, as discussed in Chapter 3. However, further study is required to explore how and to what extent the quality of the interface can be tuned to improve the TFT characteristics such as mobility, and whether or not the TFT stability is affected by such tuning.

(iii) The effect of tension or compression on the TFT characteristics such as threshold voltage and mobility as well as that on the degradation of drive current over time is important for the realization of reliable AMOLED displays on flexible substrates. The effect of an improved *a*-Si:H TFT channel on the TFT stability under mechanical stress is therefore worth investigating.

(iv) In this thesis, the stability measurements were performed at room temperature. To the first order, the "β" parameter of the stretched exponential relaxation is linearly proportional to the absolute temperature. Therefore higher temperatures may be used for accelerated testing in the low gate electric field regime.

(v) The high lifetime *a*-Si:H TFTs presented in this thesis are back-channel passivated mainly to avoid plasma etch damage to the channel during fabrication. To save an extra mask step while avoiding plasma etch damage, the development of a fully wet-etch process for back-channel etched TFTs may be investigated.

(vi) As shown in this thesis, high temperature processing is critical for high TFT lifetimes. However, the advantage of lowering the process temperature may outweigh a certain degree of compromise on TFT lifetime. Therefore optimizing the TFT lifetime at lower process temperatures is worth investigating. For example, since the coefficient of thermal expansion in polymer substrates may increase drastically at a threshold temperature, a slight decrease in the process temperature (~ 25°C) may considerably increase the process yield on clear plastic especially at industrial scales. However, the drop of the TFT lifetime at the lower process temperature may be relatively low provided that the growth conditions at the lower temperature are optimized for the best interface quality.

(vii) The device-to-device threshold voltage variation of *a*-Si:H TFTs is significantly lower than that of poly-Si TFT. However, with the very high lifetimes achieved in this work for *a*-Si:H TFTs, the contribution of threshold voltage variation to brightness non-uniformity starts to become comparable with that of differential aging among pixels due to threshold voltage shift. Therefore, reducing the threshold voltage variation on plastic (for example by optimizing the buffer layer) may be investigated.

Publications and Presentations Resulting from this Thesis

Chapter 4:

- B. Hekmatshoar, A. Z. Kattamis, K. H. Cherenack, K. Long, J-Z. Chen, S. Wagner, J. C. Sturm, K. Rajan and M. Hack, "Reliability of Active-Matrix Organic Light-Emitting-Diode Arrays with Amorphous Silicon Thin-Film Transistor Backplanes on Clear Plastic", *IEEE Electron Device Letters*, vol. 29, no. 1, pp. 63-66, January 2008
- [invited] J. C. Sturm, B. Hekmatshoar, K. Cherenack, A. Z. Kattamis and S. Wagner, "Active Matrix OLED's with High Life-time Amorphous Silicon Transistors on Clear Plastic Substrates", *Materials Research Society Fall Meeting*, Boston, MA, November 2007
- B. Hekmatshoar, K. Long, S. Wagner and J. C. Sturm, "Analytical Model of Apparent Threshold Voltage Lowering Induced by Contact Resistance in Amorphous Silicon Thin Film Transistors", *65th Annual Device Research Conference*, South Bend, IN, June 2007

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- B. Hekmatshoar, K. Cherenack, A. Z. Kattamis, S. Wagner and J. C. Sturm, "Dependence of stability of a-Si TFT's fabricated on clear plastic at 285°C on gate stress voltage", *Materials Research Society 2007 Spring Meeting*, San Francisco, CA, April 2007
- B. Hekmatshoar, A. Z. Kattamis, K. Cherenack, S. Wagner and J. C. Sturm, "Statistics of Amorphous Silicon TFT backplanes for AMOLED Displays Fabricated at 250°C on a Clear Plastic Substrate", *6th Annual Flexible Display & Microelectronics Conference*, Phoenix, AZ, February 2007

Chapter 5:

- B. Hekmatshoar, S. Wagner and J. C. Sturm, "Optimum Low-Gate-Field and High-Gate-Field Stability of Amorphous Silicon Thin-Film Transistors with a Single Plastic-Compatible Gate Nitride Deposition Process", *67th Annual Device Research Conference*, University Park, PA, June 2009

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- B. Hekmatshoar, K. Cherenack, S. Wagner and J. C. Sturm, "Amorphous Silicon Thin-Film Transistors with DC Saturation Current Half-Life of More than 100 Years", *International Electron Devices Meeting*, San Francisco, CA, December 2008

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- B. Hekmatshoar, K. Cherenack, A. Z. Kattamis, K. Long, S. Wagner and J. C. Sturm, "Highly Stable Amorphous-Silicon Thin-Film Transistors on Clear Plastic", *Applied Physics Letters*, vol. 93, no. 3, pp. 032103-1-3, July 2008
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Chapter 6:

- B. Hekmatshoar, S. Wagner and J. C. Sturm, "Trade-off Regimes of Lifetime in Amorphous Silicon Thin-Film Transistors and a Universal Lifetime Comparison Framework", *Applied Physics Letters*, vol. 95, no. 14, pp. 143504-1-3, October 2009
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Chapter 7:

- B. Hekmatshoar, K. Cherenack, K. Long, A. Kattamis, S. Wagner and J. C. Sturm, "AMOLED Reliability with a-Si TFT's in Normal vs. Inverted TFT/OLED Integration Scheme", *66th Annual Device Research Conference*, Santa Barbara, CA, June 2008

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- B. Hekmatshoar, A. Z. Kattamis, K. Cherenack, S. Wagner and J. C. Sturm, "A Novel TFT-OLED Integration for OLED-Independent Pixel Programming in Amorphous-Si AMOLED Pixels", *Journal of the Society for Information Display*, vol. 16, no. 1, pp. 183-188, January 2008

Appendix: *Publications and Presentations Resulting from this Thesis*

- B. Hekmatshoar, K. Cherenack, A. Z. Kattamis, S. Wagner and J. C. Sturm, "Inverted Integration of Amorphous Si Active Matrix OLED pixels on Clear Plastic", *7th Annual Flexible Display & Microelectronics Conference*, Phoenix, AZ, January 2008
- B. Hekmatshoar, A. Z. Kattamis, K. Cherenack, S. Wagner and J. C. Sturm, "Novel Amorphous-Si AMOLED Pixels with OLED-independent Turn-on Voltage and Driving Current", *65th Annual Device Research Conference*, South Bend, IN, June 2007

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