Highly Stable Amorphous Silicon Thin Film Transistors and Integration Approaches for Reliable Organic Light Emitting Diode Displays on Clear Plastic

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A Dissertation
Presented to the Faculty
of Princeton University
in Candidacy for the Degree
of Doctor of Philosophy

Recommended for Acceptance
by the Department of
Electrical Engineering

Advisor: James C. Sturm

September 2010

Abstract

Hydrogenated amorphous silicon (*a*-Si:H) thin-film transistors (TFTs) are currently in widespread production for integration with liquid crystals as driver devices. Liquid crystal displays are driven in AC with very low duty cycles and therefore fairly insensitive to the TFT threshold voltage rise which is well-known in *a*-Si:H devices. Organic light-emitting diodes (OLEDs) are a future technology choice for flexible displays with several advantages over liquid crystals. In contrast to liquid crystal displays, however, OLEDs are driven in DC and thus far more demanding in terms of the TFT stability requirements. Therefore the conventional thinking has been that *a*-Si:H TFTs are too unstable for driving OLEDs and the more expensive poly-Si or alternative TFT technologies are required.

This thesis defies the conventional thinking by demonstrating that the knowledge of the degradation mechanisms in *a*-Si:H TFTs may be used to enhance the drive current half-life of *a*-Si:H TFTs from lower than a month to over 1000 years by modifying the growth conditions of the channel and the gate dielectric. Such high lifetimes suggest that the improved *a*-Si:H TFTs may qualify for driving OLEDs in commercial products. Taking advantage of industry-standard growth techniques, the improved *a*-Si:H TFTs offer a low barrier for industry insertion, in stark contrast with alternative technologies which require new infrastructure development. Further support for the practical advantages of *a*-Si:H TFTs for driving OLEDs is provided by a universal lifetime comparison framework proposed in this work, showing that the lifetime of the improved *a*-Si:H TFTs is well above those of other TFT technologies reported in the literature.

Manufacturing of electronic devices on flexible plastic substrates is highly desirable for reducing the weight of the finished products as well as increasing their ruggedness. In addition, the flexibility of the substrate allows manufacturing bendable, foldable or rollable electronic systems which is not possible with conventional rigid substrates. The most reliable TFTs require a temperature higher than that possible with existing clear flexible plastic substrates. Successful integration of *a*-Si:H TFTs with OLEDs on new high temperature flexible clear plastic substrates, capable of being processed at 300^{o}C, is presented in this thesis. Controlling the mechanical stress and adhesion of the layers is found to be critical at high process temperatures to avoid cracking and delamination on clear plastic, and TFTs with a lifetime of 100 years on clear plastic have been achieved. In addition, a new “inverted” integration technique is demonstrated both on glass and clear plastic to allow the programming of standard bottom-emission OLEDs with *a*-Si:H TFTs independent of the OLED characteristics which may change over time and vary from device to device in manufacturing. This technique also enhances the pixel drive current by nearly an order of magnitude for the same programming voltage. Finally, an approach for the design of reliable pixels is presented. Based on the individual TFT and OLED device stability, a guideline to the overall circuit configuration that will provide the most stable light emission is provided.

Acknowledgement

First of all, I would like to thank my advisor, Prof. Jim Sturm, for his constant guidance, critical advice and invaluable support which was essential for the all the achievements presented in this thesis. His approach to advising graduate students is not just to guide them to learn the right technical issues, but also, in his words, “to develop the right approach and the right confidence in their abilities to be independent researchers”. Not to mention other reasons, and to say the least, I can hardly imagine a better advisor.

I would also like to thank Prof. Sigurd Wagner for the numerous discussions and the invaluable advice and help that I received from him throughout my studies at Princeton University, for which I will be always grateful.

Also, I greatly appreciate the time spent by Prof. Sigurd Wagner and Prof. Andrew Houck for reading this thesis and their valuable comments. I would also like to thank Prof. Stephan Chou, Prof. Craig Arnold and Prof. Gerard Wysocki for taking time to serve on my FPO committee.

I would like to thank the present and former members of Prof. Sturm’s and Prof. Wagner’s labs particularly those involved in the large-area projects for their help and cooperation: Ke Long, Troy Graves-Abe, Hongzheng Jin, I-Chun Cheng, Jian-Zhang Chen, Alex Kattamis, Kuni Cherenack, Prashant Mandlik, Yifei Huang, Lin Han, Ting Liu and Noah Jafferis. I am also grateful to the other lab members for their help along the way: Rebecca Peterson, David Inglis, John Davis, Kun Yao, Keith Chung, Weiwei Zheng, Sushobhan Avasthi, Jiun-yun Li, Oliver Graudejus, Jane Leisure, Wenzhe Cao and many others. Special thanks to Yifei Huang, Lin Han, Ting Liu and Bhadri Lalgudi for their help with the lingering repair and maintenance work on the PECVD tool.

I would also like to thank the staff members of PRISM cleanroom, Helena Gleskova, Joe Palmer, Pat Watson and Mike Gaevski for their great efforts to keep the cleanroom up and running. I also appreciate all the help from PRISM and ELE staff, Sheila Gunning, Carolyn Arnesen, Sarah Braude, Roelie Abdi and many others.

Finally, I want to thank my family for their love, encouragement and support throughout all the years that I have been away from home.

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Motivation and Organization of this Thesis

This chapter is devoted to the motivation behind the work presented in this thesis and the organization of the thesis chapters. This includes a brief overview of large-area and flexible electronics and in particular the advantage of reliable amorphous silicon (*a*-Si:H) thin-film transistor (TFT) backplanes for flexible organic light-emitting diodes (AMOLED) displays.

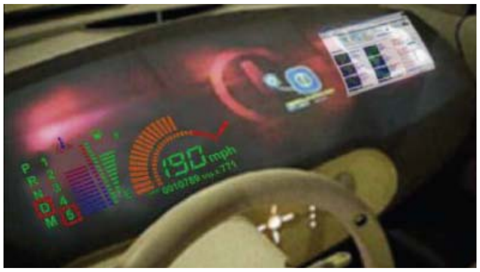
1.1 *Large-Area and Flexible Electronics and Displays*

Large-area electronics is a developing field of research widely expected to impact energy, health and the environment in a highly beneficial way. Examples of large-area applications are flat-panel displays, thin-film solar cells, medical imagers, electronic paper, radio frequency identifiers, electronic signage, smart labels and large-area sensors. In contrast to conventional VLSI where small device dimensions and high-quality materials are essential to high-performance devices and systems performing complex functions at high speed and low power consumption, key to the success of large-area electronics is low-cost material growth and fabrication of devices over large areas to perform simple low-speed electronic functions that bring intelligence to a variety of applications at low costs not possible by VLSI devices. This requires the use of polycrystalline and amorphous materials instead of single crystalline semiconductors, and substrate materials and process technologies which are very different from VLSI. These materials and processes also enable the use of flexible substrates leading to several new applications in electronics, including bendable and flexible displays, wearable electronics and smart textiles, flexible bio-electronic and bio-optical sensors, smart skins and artificial muscles.

Flexible displays, which are the main focus of this thesis, are widely expected to revolutionize the display of information in various electronic products with high-end military and medical applications, as well as regular and low-end consumer products. Some of these applications are illustrated in Fig. 1.1.

The market for flexible electronics and displays is expected to be growing exponentially in the next decade. According to DisplaySearch Incorporation, the global revenue of the flexible display market alone is expected to increase from \$800M in 2008

Retractable/Rollable Laptop (Polymer Vision)

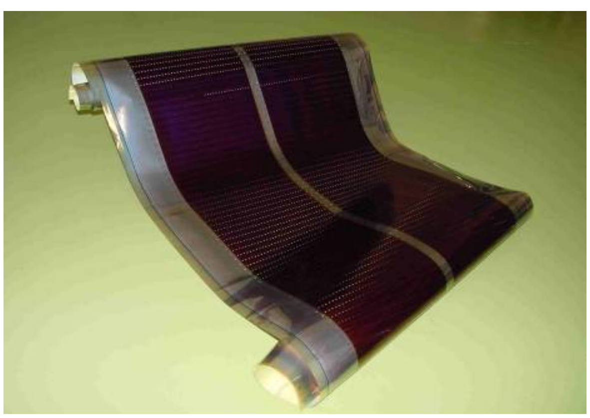


Digital Dashboard (DisplaySearch)

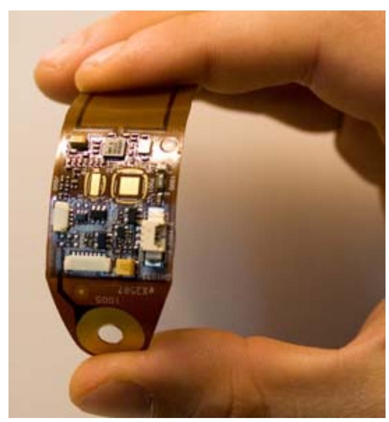
Flexible GPS (US Army)

Flexible Cell Phone (Nokia)

Flexible PDA (Universal Display Co.)



Flexible Solar Module (Fuji Electrics)



Flexible Cardiac Monitoring Patch (IMEC)

Fig. 1.1. Design concepts or prototypes of various flexible electronics applications, including flexible, bendable and/or rollable displays, solar cells and medical devices.

to $4.1B in 2015, i.e. from 0.8% to 2.8% of the total display market revenue. This is a reflection of the fact that the transition to flexible substrates is on the industry roadmap for replacing rigid substrates with low-cost light-weight flexible substrates, as well as for developing new applications which are not possible with rigid substrates. Following this roadmap will require addressing several fundamental issues, further underscoring the need for research and development in this area.

1.2 *Flexible Active Matrix OLED Displays*

Active Matrix Organic Light Emitting Diode (AMOLED) displays have all the necessary features to become the dominant technology for the next generation of flat-panel and flexible displays. Compared to liquid crystals displays (LCDs), OLEDs offer superior properties such as high speed response, wide viewing angle and simple structure (Fig. 1.2), offering the potential of low manufacturing costs. In addition, OLEDs are emissive devices and do not need backlight illumination and color filters, resulting in low power consumption [1][2]. Integrating OLEDs with TFTs in the form of active matrices (Fig. 1.3) is required for achieving very low power consumptions in mid-sized and large-sized displays [3][4]. The "backplane" refers to an array of TFTs used for addressing and programming. Since the introduction of AMOLED displays, low-temperature poly-Si (LTPS) has been the material of choice for making the TFT backplanes due to the relatively high mobility and stability of poly-Si TFTs [4][5]. However, with the improvement of OLED efficiency and especially the introduction of phosphorescent OLEDs with efficiencies superior to conventional fluorescent OLEDs, which allow the use of *a*-Si:H TFTs instead of poly-Si devices, *a*-Si:H TFTs have become very appealing

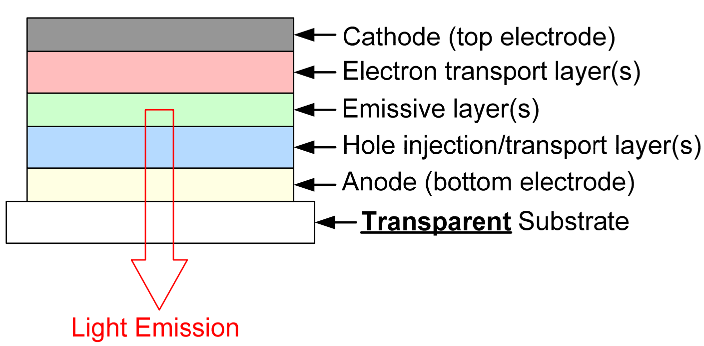


Fig. 1.2. Schematic cross-section of a typical organic light-emitting diode (OLED) device

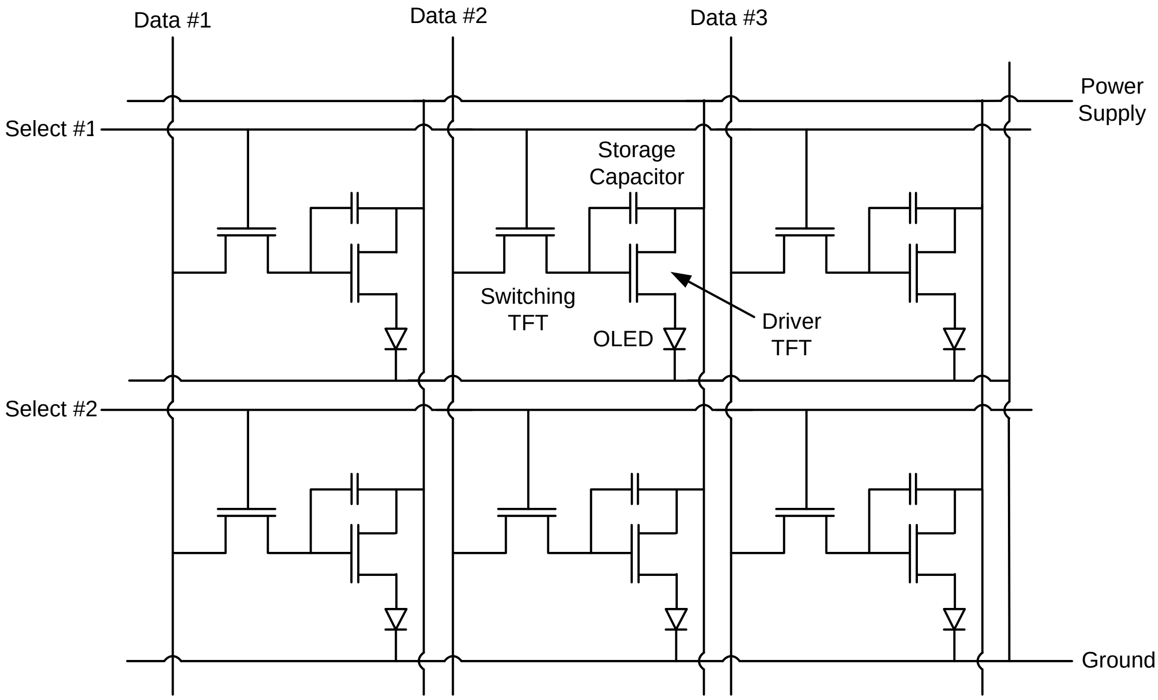


Fig. 1.3. Circuit schematic of a 2-TFT active-matrix OLED (AMOLED) array. Two rows and three columns are depicted for illustration. Each pixel is comprised of a switching TFT, a driver TFT, a storage capacitor, an OLED, a select line, and a data line. The pixels share a common ground line and a power supply line. The operation of AMOLED pixels is covered in Chapter 4.

for AMOLED applications [3][6][7]. The reason is that *a*-Si:H technology is a mature low-cost technology widespread in production and is very suitable for large-area deposition especially on flexible plastic substrates [8]. Flexibility is a requirement for economical mass production by roll-to-roll processing.

1.3 *Stability of a-Si:H TFTs for Driving OLEDs*

A critical technical issue associated with employing *a*-Si:H TFT backplanes on clear plastic substrates for AMOLED displays is the stability of *a*-Si:H TFTs. The threshold voltage of *a*-Si:H TFTs increases with time due to charge trapping in the gate nitride and defect creation in the *a*-Si:H [9]. This problem becomes serious when the TFTs are made at the low process temperatures compatible with existing clear plastic substrates (<< 300°C) [10][11][12]. Unlike AMLCDs, AMOLED pixels operate in DC and the OLED current depends directly and continuously on the TFT threshold voltage. Therefore as the threshold voltage increases, the OLED current supplied by the TFT and thus the pixel brightness drop. This leads to various issues including the distortion of color balance in the pixel, which is a serious problem (Fig. 1.4). Therefore, the stability issue of *a*-Si:H TFTs needs to be resolved before they can be used for the manufacturing of AMOLED display backplanes. Improving the stability of *a*-Si:H TFTs could enable the mainstream *a*-Si:H TFT production infrastructure to be used for the emerging applications instead of requiring a new infrastructure for employing new materials. This subject is the main focus of this thesis. A number of other issues associated with the application of *a*-Si:H TFTs for AMOLED displays, particularly on flexible clear plastic substrates, are also addressed in this thesis.

1.4 *Organization of this Thesis*

The basic properties of *a*-Si:H are reviewed in Chapter 2. These properties include the atomic and electronic structure, electronic transport, structural defects, doping, thermal equilibrium and metastability. Knowledge of the basic materials properties of *a*-Si:H is essential to understanding the operation of *a*-Si:H TFTs.

The device operation and fabrication process of *a*-Si:H TFTs are covered in Chapter 3. The standard *a*-Si:H TFT structures, the basic operation of these devices and materials growth for the channel and gate dielectric of *a*-Si:H TFTs are reviewed in this chapter, followed by the standard *a*-Si:H TFT process in our lab.

Chapter 4 is focused on the design, fabrication and reliability of AMOLED pixel arrays with *a*-Si:H TFT backplanes on high temperature clear plastic substrates. A significant improvement in the reliability of light emission over time is demonstrated in this chapter thanks to the high temperature process compatibility of new clear plastic

2% Red Drop	5% Red Drop	10% Red Drop	20% Red Drop
2% Green Drop	5% Green Drop	10% Green Drop	20% Green Drop
2% Blue Drop	5% Blue Drop	10% Blue Drop	20% Blue Drop

Fig. 1.4. The degradation of white color as a result of the drop of one of the blue, red and green components with respect to the others.

substrates developed by DuPont in collaboration with Princeton, as well as the proper stress engineering of the backplane layers.

Record high lifetime *a*-Si:H TFTs for driving OLEDs on glass and clear plastic substrates are demonstrated in Chapter 5. In this chapter, the instability mechanisms responsible for threshold voltage shift in *a*-Si:H TFTs are studied, and the knowledge of these mechanisms is applied to enhancing the lifetime of these devices by more than three orders of magnitude. This improvement is achieved by modifying the growth conditions of the *a*-Si:H channel and the gate nitride to improve the quality of *a*-Si:H close to the *a*-Si:H/nitride interface.

In Chapter 6, a formal method for making a “fair comparison” of the stabilities of TFTs with different gate insulator materials and thicknesses measured under different gate voltages is presented. Comparison with the literature shows that the lifetime of the improved *a*-Si:H TFTs achieved in this work is far in excess of standard *a*-Si:H TFTs reported by other groups as well as other TFT technologies.

In Chapter 7, a new “inverted” TFT/OLED integration technique is demonstrated on glass and clear plastic for direct programming of the pixel current which is conventionally not possible with *a*-Si:H TFTs and standard bottom-emission OLEDs. This integration method significantly improves the drive current and reduces the turn on voltage of the pixel and the makes the pixel current independent of the OLED characteristics. In addition, predicting the degradation of the AMOLED pixel current based on the measured characteristics and the drift of the individual TFTs and OLEDs at constant bias-stress conditions is presented in this chapter.

Finally, a summary and conclusion of this thesis and suggestion for future work is given in Chapter 8. Publications and presentation resulting from this thesis are listed in the Appendix.

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Basic Properties of Hydrogenated Amorphous Silicon

Hydrogenated amorphous silicon (*a*-Si:H) is the mainstream semiconductor in the commercial production of thin-film-transistor (TFT) backplanes for active-matrix liquid crystal displays (AMLCDs), thin-film solar cells and x-ray imagers. A brief review of the basic properties of this material and the electrical characteristics resulting from these properties is presented in this chapter. The growth of *a*-Si:H and hydrogenated amorphous silicon nitride (*a*-SiN_x:H) (the main dielectric material for *a*-Si:H TFTs) are covered in the next chapter. Further detail about the properties and characteristics of *a*-Si:H material and devices may be found in [1][2].

2.1 *Atomic Structure*

The atomic structure of *a*-Si:H is shown schematically in Fig. 2.1. The presence of hydrogen in the lattice is crucial. Hydrogen passivates most of the Si dangling bonds so that most of the Si atoms are 4-fold coordinated (with 4 bonds per atom), the same as single-crystalline Si (*c*-Si). Without hydrogen, amorphous Si would have a very high density of defects (unpassivated dangling bonds) preventing doping, photoconductivity and other desirable characteristics of a useful semiconductor.

As an amorphous material, *a*-Si:H is not completely disordered and has a short-range order. This is because the deviations of the Si-Si bonding lengths and angles from their equilibrium values (determined by covalent bonding rules for *c*-Si) are sufficiently small to maintain order in a short range (the average bonding angle and length disorder

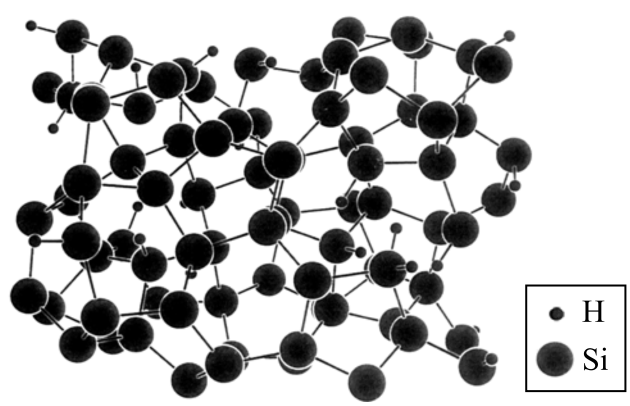

Fig. 2.1. The atomic structure of hydrogenated amorphous silicon (*a*-Si:H) [1].

are less than 10% and 1%, respectively [1]). In a single-crystalline material, knowing the positions of atoms in a reference unit cell and the lattice constants provide accurate information about the positions of all the other atoms in the lattice. In an amorphous material, however, the accuracy of such information is reduced and eventually lost with increasing the distance from the reference unit cell. The lack of long-range order in *a*-Si:H has important consequences that determine the electrical and optical properties. Bonding disorder results in band tails, localization and scattering; structural defects result in electronic states in the bandgap; and alternative bonding configurations result in metastable electronic states. These effects will be reviewed in the following sections.

2.2 *Electronic Structure*

The electronic structure of single-crystalline semiconductors is described by band diagrams (electron energy, E, vs. crystal momentum, k), all common in having a bandgap and extended states above the minimum of the conduction band (E_c) and below the maximum of the valence band (E_v). The standard treatment in solid-state physics for the calculation of E-k diagrams, which involves the application of Bloch's Theorem, may create a wrong impression that the presence of a bandgap is a consequence of the periodicity of the lattice. While the periodicity of the lattice is necessary to ensure that k is a good quantum number and therefore E-k diagrams are meaningful, the presence of a bandgap (as well as extended states above E_c and below E_v) is a direct consequence of the assumption that the linear combination of atomic orbitals (LCAO) is a valid principle, irrespective of the presence or the lack of periodicity in the long range. The splitting of the bonding and anti-bonding orbitals of the covalent bonds (sp^3 hybridized orbitals in the case of Si) which determines the bandgap is strongly affected by short-range order which is the same for amorphous and semiconductor materials and the lack of long-range periodicity in amorphous materials in only a small perturbation. This is because the nearest neighboring atoms have the highest contribution to the LCAO.

Since long-range order is absent in amorphous materials, the scattering length (ℓ_0) is small and of the order of interatomic spacing (a_0). Therefore the uncertainty in determining k is of the order of k itself ($\Delta\mathrm{k} = \hbar / \ell_0 \approx \hbar / a_0 \approx \mathrm{k}$) and k is not a good quantum number. The electronic structure of amorphous materials is thus represented by

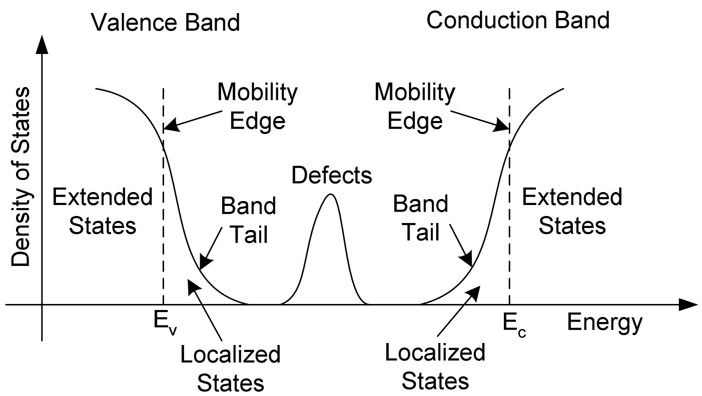

Fig. 2.2. The schematic density of electronic states in an amorphous semiconductor.

the density of states vs. energy ($N(E)$ vs. E) rather than E-k diagrams. The schematic density of states for an amorphous semiconductor is shown in Fig. 2.2. The defects states are the consequence of coordination disorder (dangling bonds) while the band tails are due to bonding disorder in the amorphous material. In *a*-Si:H the density of defects is low ($<10^{16}$ cm^{-3}) due to hydrogen passivation and therefore carrier transport and optical properties are mainly determined by the band tails. The remaining (unpassivated) defects are responsible for metastability and have a major role in substitutional doping.

Localization and the Mobility Edge – In a single-crystalline solid, an electron experiences a periodic potential. This is represented in its simplest one-dimensional form with an array of atomic potential wells and a corresponding band broadening B due to atomic interactions (Fig. 2.3 (a)). Bloch's theorem states that electrons are not scattered by such a periodic potential. The electronic states are therefore "extended" states as the electron wavefunction expands all over the crystal, i.e. the position of an electron with a given momentum k can be anywhere in the crystal, which is a direct consequence of the uncertainty principle. A disordered solid can be modeled by superimposing a disorder potential V_0 on the periodic potential (Fig. 2.3 (b)). Anderson's theory of localization [3] predicts that there is a critical value of disorder potential ($V_0 \approx 3B$) above which *all* of the electronic states are "localized", i.e. electrons have zero probability to diffuse away from a particular site. However, this level of disorder is very high (~15 eV) and is not met in amorphous materials as the existing short range order prevents high levels of distortion.

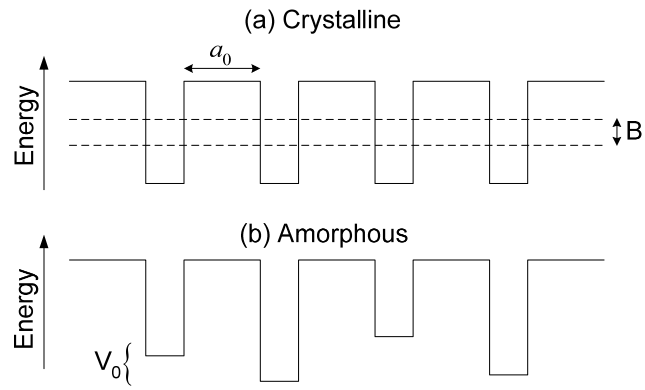

Fig. 2.3. The Anderson Model of potential wells for (a) crystalline and (b) amorphous networks.

Mott showed that for disorder levels lower than the Anderson criterion, both localized and extended states are present and localization is stronger for higher binding energies [4]. In Mott's model, which is widely accepted as the standard model of amorphous materials, localized and extended states are separated by a "mobility edge" (Fig. 2.2). We denote the mobility edge at the conduction band with the same symbol E_c as the bottom of the conduction band in single crystalline semiconductors because of their analogy in marking the lowest allowed energy of an "unbound" electron, i.e. the lowest extended state energy level which is unoccupied at zero temperature. Similarly, we denote the valence band edge by E_v. The band tails are generally assumed to be exponential in energy, especially because of the correlation of the conduction band tail with the Urbach edge [5][6] (the exponential tail of the optical absorption coefficient in the vicinity of the bandgap energy in amorphous materials). Detailed measurements of the density of states show that the band tails are not strictly exponential [7][8]. However, the departure from exponential dependence is small and negligible to the first order.

2.3 *Electronic Transport*

Electrical conduction in *a*-Si:H takes place by trap-limited transport in the extended states as well as hopping between the localized states in the band tails and the midgap states. At room temperature and higher temperatures, extended-state transport is dominant while hopping conduction becomes important at lower temperatures. Conduction in the extended states above E_c can be expressed with the relation

$$\sigma_{ext} = \sigma_{oe} \exp[-(E_c - E_f)/kT] \tag{2.1}$$

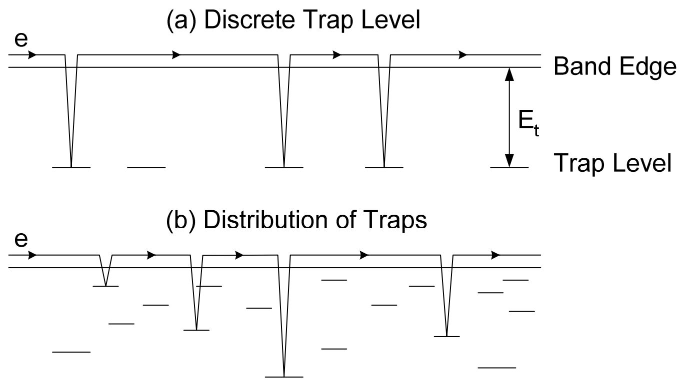

Fig. 2.4. Illustration of trap-limited transport for (a) a discrete level and (b) a distribution of traps.

where σ_{oe} is the average conductivity above E_c (about 100 $\Omega^{-1}\text{cm}^{-1}$). The activation energy is the separation of E_c from E_f and varies from nearly 1eV in undoped *a*-Si:H to 0.1eV in n-type material [1]. Raising E_f closer to E_c is not possible by increasing the doping concentration or raising the electric potential (for example by increasing the gate voltage in *a*-Si:H TFTs). This is because of the low efficiency of dopants (see section 2.6) and the high density of band tail states that pin the Fermi level at ~ 0.1eV below E_c.

2.3.1 Trap-Limited Conduction

Transport in *a*-Si:H is trap-limited. Electrons and holes are frequently trapped in the tail states, followed by thermal excitation to the extended states. The effective mobility of carriers, referred to as the drift mobility (μ_d), is therefore lower than the actual mobility of the extended states, referred to as the band mobility (μ_0). Because of the thermal excitation of carriers from traps to the extended states, the trap-limited mobility is thermally activated.

The drift mobility is the band mobility reduced by the fraction of time that the carrier spends in the trap [1]:

$$\mu_d = \mu_0 \tau_{free} / (\tau_{free} + \tau_{trap}) \qquad (2.2)$$

Statistically, this is equivalent to the band mobility reduced by the fraction of carriers captured in the traps at any given time

$$\mu_d = \mu_0 n_{free} / (n_{free} + n_{trap}) \qquad (2.3)$$

Therefore for a single trap level at a depth E_t below the mobility edge (Fig. 2.4 (a))

$$\mu_d = \mu_0 N_c / [N_t \exp(E_t / kT) + N_c] \approx \mu_0 (N_c / N_t) \exp(-E_t / kT) \qquad (2.4)$$

where N_t is the trap density and N_c is the effective density of states at the mobility edge. Note that in writing Eq. (2.4), the Fermi level E_f is assumed to be below E_t, which is the case in *a*-Si:H if N_t represents an "effective" density of traps at E_t (Section 3. 2). This is because of the high density of tail states close to the mobility edge (Section 2.5). When there is a distribution of traps $N(E)$ (Fig. 2.4 (b)), the drift mobility reflects the average release time of the carriers, given by (N_T is the total density of traps and ω_0 is approximately the frequency of optical phonons ($\sim 10^{13}\,s^{-1}$))

$$\tau_{avg} = \frac{1}{N_T}\int_0^{\infty} N(E)\omega_0^{-1}\exp(E/kT)\,dE \tag{2.5}$$

Assuming an exponential distribution of traps of slope kT_c and a prefactor N_0, i.e. $N(E) = N_0\exp(-E/kT_c)$, for $T > T_c$, Eq. (2. 5) yields

$$\tau_{avg} = \omega_0^{-1} N_0\, k\,T\,T_c/(T - T_c) \tag{2.6}$$

For $T < T_c$, however, the integral in Eq. (2. 5) diverges and the average release time becomes infinite. Physically, this means that increasing the transport time allows the electrons to get captured by/released from traps at deeper energy levels, i.e. the measured drift mobility decreases with increasing the measurement time, as traps at deeper energy levels get involved in the trapping/releasing process. Such an apparent time dependence of drift mobility is experimentally observed in time of flight measurements and transport under this condition is referred to as "dispersive transport" [7][9].

Dispersive transport provides a powerful tool for measuring the band tail slope. In time of flight measurements on a trap-free sample with thickness d and applied voltage F, the transit time $\tau_{tr} = \mathrm{d}/\mu_d F$ and the drift mobility have no field dependence. In the case of dispersive transport, however, there is a large increase in the drift mobility by increasing the electric field and the drift mobility is proportional to $(F/d)^{1/\alpha-1}$ where $\alpha = T/T_c$ [10]. For the conduction and valence band tails, the measured values of T_c and T_v for *a*-Si:H are in the range of 250-300K and 450-500K, respectively [11]. Therefore hole transport in *a*-Si:H is dispersive at room temperature, while electron transport is not.

2.3.2 Hopping Conduction

Hopping conduction in the tail states takes place by tunneling between neighboring localized states allowed by the spatial overlap of their wavefunctions (Fig. 2.5). The tunneling transition rates between two states of spatial separation R and energy difference E_{12} are [1]

$$T_{12} = \omega_0 \exp(-2R/R_0)\exp(-E_{12}/kT) \tag{2.7}$$

$$T_{21} = \omega_0 \exp(-2R/R_0) \tag{2.8}$$

where R_0 (E) is the localization length, roughly equal to $\hbar/[m_e(E_c - E)]^{1/2}$ for electrons. Hopping conduction in the tail states needs a lower thermal activation energy than conduction in the extended states; however, the density of the tail states is much lower than that of the extended states. As a result, conduction in the extended states is the dominant mechanism at room temperature and hopping conduction becomes important at lower temperatures. Hopping conduction is also possible in the midgap states by a similar mechanism and becomes important only at very low temperatures.

2.4 *Structural Defects*

In single crystalline materials, any small deviation from the periodic structure creates a defect and generates states within the energy gap. As a result there are more than 50 types of defects in single crystalline materials [1]. Structural defects are meaningless in a completely disordered material. However, in amorphous materials such as *a*-Si:H, the presence of short range order gives meaning to a structural defect as a deviation from the short range order. Deviations in the bonding length and angle generate long range disorder, and account for band broadening and the presence of band tails. Such deviations are intrinsic to amorphous materials and as such are not considered structural defects. In fact, the only possible structural defects in amorphous materials are coordination defects, i.e. missing or extra bonds. These defects generate short range disorder and therefore create electronic states within the bands.

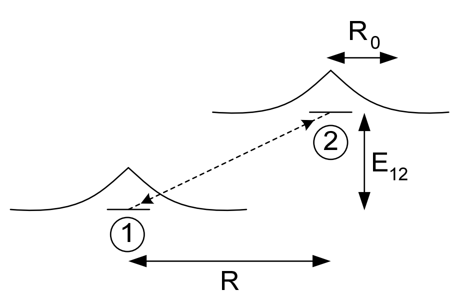

Fig. 2.5. Model of tunneling between two neighboring localized states.

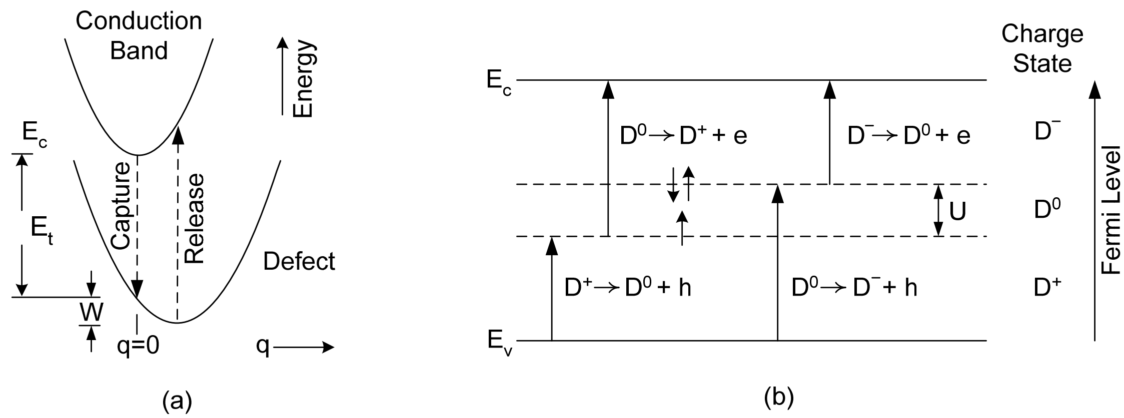

Fig. 2.6. (a) Configuration coordinate diagram describing the capture and release of carriers between the conduction band and the defects and (b) the illustration of the one-electron and two-electron energy levels of defects (with positive U), possible transitions to the conduction and valence bands and the charge states of the defects as a function of the Fermi level position.

Trapping of an electron in a defect, for example, results in a structural change and reduces the energy of the defect state. This can be explained by a semi-classical configuration diagram shown Fig. 2.6 (a) [1]. Considering a configuration coordinate q, an electron in the conduction band creates a vibrational mode with a potential energy which is the sum of the electron potential energy at the bottom of the conduction band (mobility edge) and the vibrational energy of the lattice, $E(q) = E_c + Aq^2$. The coefficient A reflects the strength of lattice vibrations. With no electron-phonon coupling, the trapping of this electron into a defect state at depth E_t below E_c would result in a defect state with an energy lower than $E(q)$ by E_t (i.e. $E_{defect}(q) = E_c - E_t + Aq^2$). Electron-phonon coupling, however, lowers the energy of the defect by a deformation energy equal to Bq (to the first order), i.e. $E_{defect}(q) = E_c - E_t + Aq^2 - Bq$. The equilibrium energy of the network is therefore lowered by $W = B^2/4A$ as a result of lattice relaxation.

A coordination defect in *a*-Si:H (also called dangling bond defect) can exist in three charge states depending on the position of the Fermi level. A dangling bond defect can be occupied by up to two electrons (based on Pauli Exclusion Principle). The dangling bond is positively charged when not occupied (D^+), neutral when singly occupied (D^0) and negative when doubly occupied (D^-) and there are four possible transitions to and from the conduction and valence bands (Fig. 2.6 (b)). The correlation energy separating the singly occupied and doubly occupied levels is $U = e^2/4\pi\varepsilon\varepsilon_0 R - W$

where the first term is the electron-electron repulsion (R is roughly the localization length of the defect wavefunction) and the second term is the lattice relaxation energy due electron-phonon coupling. The presence of D^0 defects indicates a positive correlation energy, which is the case in *a*-Si:H; however, negative correlation energies exist in other amorphous materials such as chalcogenide glasses [12][13] and their presence results in Fermi level pinning. This is because as the doubly occupied state lies below the singly occupied state (at a separation equal to U) the Fermi level, by definition, has to lie between the two states, i.e. above the filled and below the unfilled state.

2.5 *Measurement of the Density of Electronic States*

The conduction and valence band density of states are measured by photoemission spectroscopy. A photon with energy $\hbar\omega$ can excite an electron from a valence band state with a binding energy E_{VB} (with respect to the Fermi energy) and eject it from the surface (assuming a workfunction ϕ) with a kinetic energy of $\hbar\omega - \phi - E_{VB}$. Measuring the kinetic energies of the ejected electrons can therefore determine the distribution of valence band states. A combination of x-ray photoemission spectroscopy (XPS) and UV photoemission spectroscopy (UPS) are commonly used for this purpose [14][15]. The inverse of the photoemission process (using an incident electron beam and measuring the energy of emitted photons) is used for measuring the density of conduction band states.

The density of tail states is usually determined using a combination of time of flight measurements under dispersive transport condition (see Section2.3) and photoemission spectroscopy. The measured density of conduction and valence band states for good quality *a*-Si:H is shown in Fig. 2.7 (a) [1].

The measurement of the density of states of defects is more complicated and usually a combination of different techniques is required for an accurate interpretation of the results. Here we will review some of these techniques briefly.

The D^0 defects are paramagnetic and their total density (over all energies) can be measured by electron spin resonance (ESR) [16]. This is because the two quantum states of D^0 defects (positive and negative spin states) are degenerate, and can be split by applying a magnetic field (due to Zeeman Effect). This method provides a good measure of defect density in undoped *a*-Si:H as D^0 is the equilibrium charge state. However, in n-type and p-type *a*-Si:H, the equilibrium charge states (D^- and D^+, respectively) are not paramagnetic.

Standard capacitance-voltage (C-V) measurements cannot be used for measuring the density of defects in *a*-Si:H, because the defect energies are continuous rather than discrete, and their energy distribution is unknown, but the C-V data can be fitted to an assumed energy distribution [17].

Deep level transient spectroscopy (DLTS) which is commonly used for measuring the density of deep traps in single-crystalline semiconductors can be used for measuring the defect density in doped or undoped *a*-Si:H. In this method, a forward bias is applied to a Schottky junction (metal/*a*-Si:H) to fill all the traps, followed by applying a reverse bias to bring the junction into deep depletion. As the carriers are released from the traps, the width of the depletion region is decreased until the steady state is reached. Since the release time of carriers from traps τ_R is related to the trap depth E_t (measured with respect to the mobility edge), $\tau_R = \omega_0^{-1} \exp(E_t / kT)$, measuring the time dependence of the depletion region width (by measuring the junction capacitance over time) provides information about the energy distribution of traps (Fig. 2.7 (b)) [18][19].

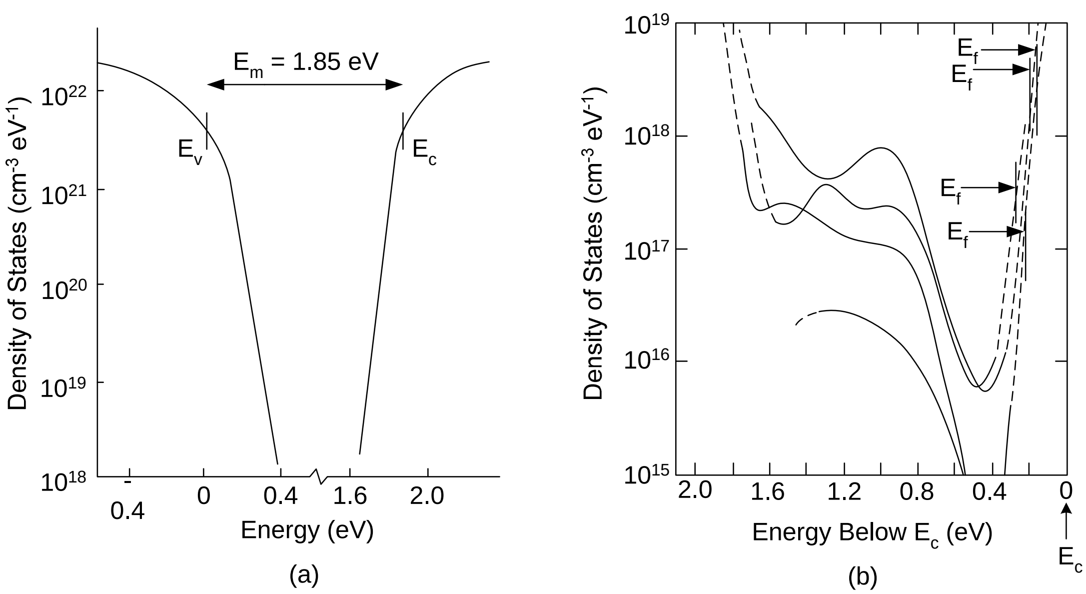

Fig. 2.7. (a) Conduction and valence band density of states determined from a combination of photoemission spectroscopy and time of flight measurements [1] and (b) density of states of defects in n-type *a*-Si:H measured by DLTS for different phosphorus doping levels [18].

Other techniques for measuring the density of states of defects include space charge limited current (SCLC) measurements [20], photo-thermal deflection spectroscopy (PDS) [21], constant photo-current method (CPM) [22] and field-effect measurements [23]. Field-effect measurements are important in that unlike the other techniques, they measure the density of states in *a*-Si:H close to the *a*-Si:H/dielectric interface rather than in the bulk. As explained in the next chapter, this is important because the density of states close to the interface (which determines the characteristics of field-effect devices such as *a*-Si:H TFTs) can differ (and normally does differ) from that in the bulk. Field-effect measurements are covered in the next chapter.

2.6 *Substitutional Doping*

The "$8 - N$" rule in chemistry states that an atom from group N of the periodic table, in its lowest-energy bonding configuration, has N bonding electrons (i.e. valence electrons in the outer shell) for $N < 4$, and $8 - N$ bonding electrons for $N > 4$. Therefore in the ground state, boron (group III) has three bonding electrons and phosphorus (group V) has three bonding electrons and a lone pair (two non-bonding electrons). Therefore based on the "$8 - N$" rule, both boron and phosphorus atoms should be 3-fold coordinated (and therefore non-ionized) both in *c*-Si and *a*-Si:H. This is not the case as boron and phosphorous act as dopants in *c*-Si and *a*-Si:H.

The reason for doping (ionization of the impurity atom) in *c*-Si is the periodicity of the lattice which constrains the impurity atom to conform to the lattice coordination. This is because a non-ionized impurity (which is 3-fold coordinated) creates a dangling bond (coordination defect) in the lattice and the combined energy of a non-ionized (neutral) impurity and a dangling bond defect is higher than that of an ionized impurity (which is 4-fold coordinated and therefore does not create a dangling bond) and therefore doping is energetically favorable. This difference of the two energies is high and therefore provided that the temperature is high enough for ionization (higher than few milli-Kelvins), the doping efficiency is high in *c*-Si.

In *a*-Si:H, the lattice periodicity is absent and therefore the neutral 3-fold coordination of an impurity has the lowest energy. However, doping is possible because of the "defect compensation" of dopants [24]. The combined energy of a dangling bond

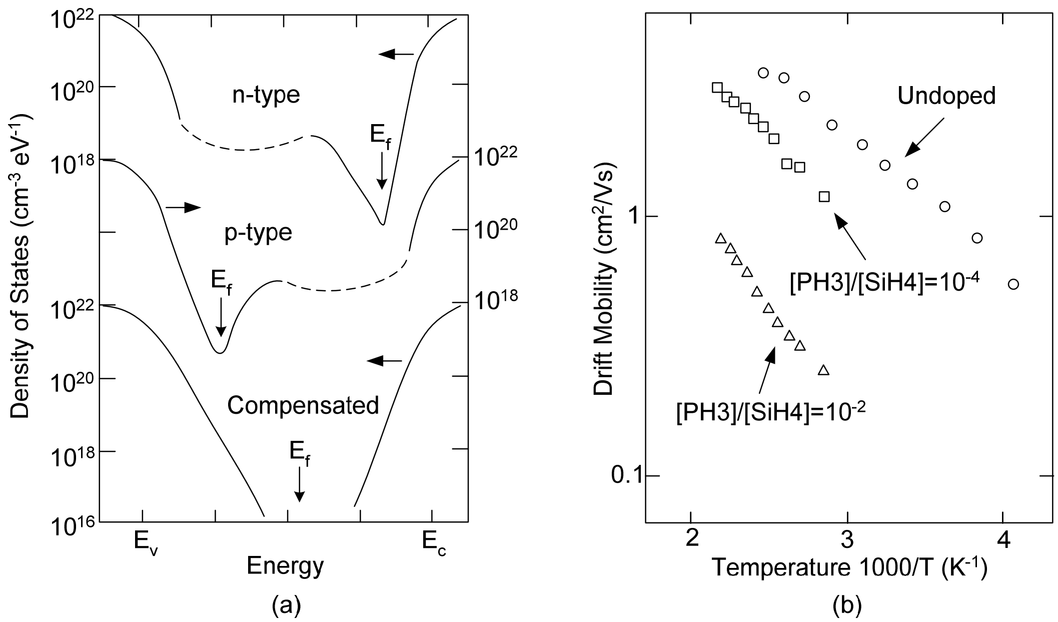

Fig. 2.8. (a) The doping dependence of the density of states expected from chemical bonding arguments [25] and (b) the dependence of the drift mobility on phosphorus doping determined from time-of-flight measurements [26].

defect and an ionized 4-fold coordinated impurity (a dopant-defect pair) is lower than the energy of a 4-fold coordinated impurity (dopant) alone, but still higher than that of a neutral 3-fold coordinated impurity. However, the energy difference between a dopant-defect pair and a neutral 3-fold coordinated impurity is small, allowing a considerable number of ionized impurities (paired with defects) to exist. Therefore doping is possible in *a*-Si:H but with a low efficiency. Also, doping causes a large increase in the concentration of defects roughly equal to the doping density. The doping dependence of the density of states is illustrated in Fig. 2.8 (a).

The defect compensation may be expressed in the form of the following chemical reactions for phosphorous and boron:

$$Si_4^0 + P_3^0 \rightleftarrows P_4^+ + D^- \qquad (2.9)$$

$$Si_4^0 + B_3^0 \rightleftarrows B_4^- + D^+ \qquad (2.10)$$

In equilibrium, $[Si_4^0][P_3^0] = K_1[P_4^+][D^-]$ and $[Si_4^0][B_3^0] = K_2[B_4^-][D^+]$ (K_1 and K_2 are the reaction constants). This model predicts that the doping density increases with the square root of the impurity atom concentration (note that $[P_4^+] = [D^-]$ and $[B_4^-] = [D^+]$). This is consistent with the experimental data for *a*-Si:H and *a*-Ge:H [25].

Adding small ratios of phosphine or diborane to the deposition gas during growth of *a*-Si:H (see section 3.3.3) shifts the Fermi level up to 0.15eV below E_c or down to 0.3eV above E_v, respectively, and modulates conductivity by a factor of more than 10^8. The concentration of ionized impurities (and therefore conductivity) increases proportional to roughly the square root of the doping concentration for doping concentrations lower than 1% and saturates at higher concentrations. Therefore, there is no metallic conduction (degeneracy) in *a*-Si:H in contrast to highly doped single crystalline semiconductors. This is because of a high density of band tail states close to the mobility edge and also because of low doping efficiencies.

In addition to the creation of defects to allow substitutional doping, impurity atoms affect the bonding angle distribution and create electronic states in the band tails, resulting in a wider Urbach edge and a lower carrier mobility compared to the intrinsic material. A phosphine ratio of 1% in silane ($[PH_3]/[SiH_4] = 0.01$) during PECVD reduces the drift mobility by a factor of about 10 (Fig. 2.8(b)) [26].

2.7 *Structural Equilibration: Thermal Equilibrium and Metastability*

Structural equilibration in *a*-Si:H is a widely accepted concept and is supported by strong experimental evidence. However, the underlying microscopic mechanisms such as the defect reactions leading to structural equilibration are still controversial and the subject of active research. In this section, we review the general concept of structural equilibration and discuss some of the most widely accepted models.

2.7.1 Thermal Equilibrium

Thermal equilibrium in *a*-Si:H may be expressed by a chemical reaction of the form [1]

$$A + B \rightleftarrows C + D \qquad (2.11)$$

where A, B, C and D refer to different configurations of defects, dopants, weak bonds, electronic charges, etc. This may be explained by a configuration diagram with a low-energy (ground) state and a high-energy state (Fig. 2.9). The equilibrium density of the high-energy states depends on their formation energies (U) and the equilibration time (time required to reach equilibrium) depends on the barrier height E_B.

$$\tau_R = \omega_0^{-1} \exp(E_B / kT) \qquad (2.12)$$

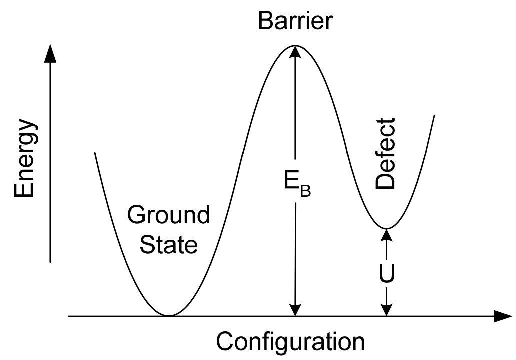

Fig. 2.9. Configuration coordinate diagram of equilibration between two states.

In the case of defect creation and annihilation (annealing) in undoped *a*-Si:H, the ground and the high-energy states correspond to the energies of the weak bonds and dangling bonds (defects), respectively. In doped *a*-Si:H, the pairing of dopants and defects must be taken into consideration to explain the thermal equilibrium. In this thesis, we mainly focus on undoped *a*-Si:H (which is the material of interest for thin-film transistor channels) and neglect the effect of ionized impurities.

Evidence for thermal equilibrium in *a*-Si:H comes from the dependence of the electrical characteristics on thermal history. For example, the conductivity of a doped *a*-Si:H sample annealed at about 200°C and then cooled down to a lower temperature at a fast cooling rate (few °C per minute) is higher than that of a sample cooled down slowly to the same temperature [26]. The reason is that the equilibrium doping efficiency (i.e. the equilibrium density of ionized impurities and their defect pairs) is higher at 200°C compared to lower temperatures and slow cooling provides sufficient time for the density of ionized impurities (and thus the density of band-tail electrons) to reduce to its equilibrium value at the lower temperature, but a fast cooling rate freezes in a non-equilibrium density which is higher than the equilibrium value at the lower temperature. The non-equilibrium density will however gradually relax to its equilibrium value. The relaxation time is of the order of 1 year at room temperature but only about a few minutes at 120°C (Fig. 2.10 (a)) [27][28]. Thermal equilibrium effects are also present in undoped *a*-Si:H [29]. ESR measurements show that annealing undoped *a*-Si:H at 400°C, creates a large density of neutral defects which are relaxed by subsequent annealing at lower temperatures (Fig. 2.10 (b)) [30].

2.7.2 Equilibrium Model

Thermal equilibrium models are based on determining the thermodynamic equilibrium distribution of formation energies, for example those of defects or dopants [1]. The thermodynamic equilibrium corresponds to a minimum of the Gibbs free energy

$$G = H - TS \tag{2.13}$$

where $H = U - PV$ is the enthalpy, U the formation energy, P the pressure, V the volume (PV may be assumed constant for a solid) and S the entropy. The number of configurations for N_D defects on a network of N_0 sites is $W = N_0!/N_\mathrm{D}!(N_0 - N_\mathrm{D})!$ and using Stirling's approximation ($\ln N_\mathrm{D}! \approx N_\mathrm{D}\ln N_\mathrm{D} - N_\mathrm{D}$) the entropy $S = k\ln W$ is evaluated as

$$S = k\left[N_0 \ln\left(\frac{N_0}{N_0 - N_\mathrm{D}}\right) - N_\mathrm{D}\ln\left(\frac{N_\mathrm{D}}{N_0 - N_\mathrm{D}}\right)\right] \tag{2.14}$$

Minimizing the free energy with respect to N_D gives

$$N_\mathrm{D} = \frac{N_0}{1 + \exp(U/kT)} \approx N_0 \exp(-U/kT) \quad \text{when} \quad U >> kT \tag{2.15}$$

When there is a distribution of defect formation energies, it is straightforward to show

$$N_\mathrm{D} = \int \frac{N_0(U)}{1 + \exp(U/kT)}\, dU \tag{2.16}$$

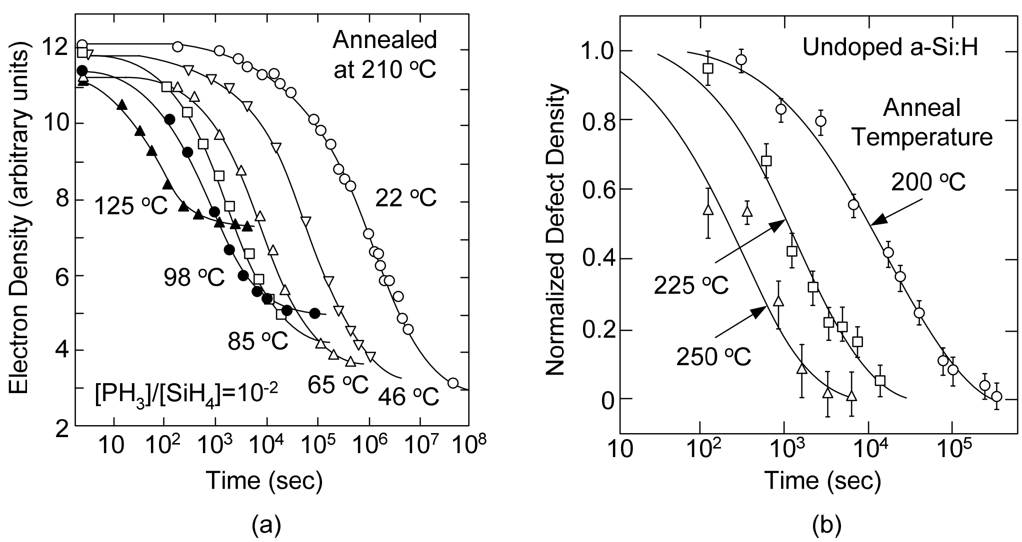

Fig. 2.10. (a) Decay of band-tail carrier concentration in n-type *a*-Si:H at different temperatures, following an anneal at 210°C and rapid cooling [27], and (b) decay of the neutral defect density in undoped *a*-Si:H at different temperatures after annealing at 400°C and rapid cooling [30].

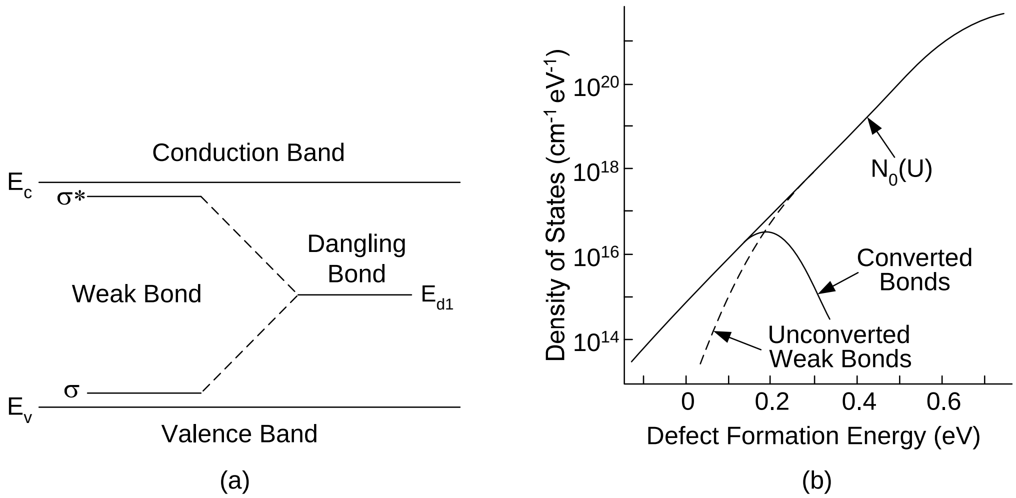

Fig. 2.11. (a) Energy diagram showing the conversion of a weak Si–Si bond into a dangling bond [40][41], and (b) the distribution of the formation energies according to the weak bond model. The shape of the distribution follows the valence band density of states. The density of defects is calculated based on Eq. (2.16) [1].

The distribution of the defect formation energies in thermal equilibrium is related to the energy distribution of weak bonds in *a*-Si:H.

The weak bond model – In *a*-Si:H, dangling bonds (defects) are created from weak Si–Si bonds in a reversible process which can be expressed as [40][41]

$$\textit{weak bond} \rightleftarrows \textit{dangling bond} \tag{2.17}$$

The formation energy of a neutral defect is the energy required for the structural change associated with converting a weak bond to a dangling bond (Fig. 2.11(a))

$$U_{d0} = E_{d1} - E_{\mathrm{WB}} + \sum_{VB \neq \mathrm{WB}} \left[(E'_{VB} - E_{VB}) + \Delta E_{ion} \right] \tag{2.18}$$

where E_{d1} is the one-electron energy level of the neutral defect state, E_{WB} the energy of the valence band tail state associated with the weak bond, E'_{VB} and E_{VB} the energies of the valence band tail states before and after bond breaking, and ΔE_{ion} the change in the ion-core interaction energy during bond breaking. The first two terms in Eq. (2.18) represent the energy difference of a non-bonding electron (of a dangling bond) in the gap with that of a bonding electron (of a weak bond) in the valence band tail. The weak bond model assumes that breaking a weak bond does not induce any structural change in the other weak bonds and therefore does not change the energies of the valence band tail states other than that of the weak bond which is broken. The formation energy of the neutral defects may thus be approximated by

$$U_{d0} \approx E_{d1} - E_{\mathrm{WB}} \qquad (2.19)$$

Based on this assumption, the distribution of the formation energies follows the valence band tail density of states which is exponential in energy (Fig. 2.11(b)).

The formation energy of a negatively charged defect is equal to that of a neutral defect minus the energy released from (or plus the energy required for) transferring an electron from the Fermi level E_f to the two-electron defect energy level E_{d2}

$$U_{d-} \approx U_{d0} - (E_f - E_{d2}) \qquad (2.20)$$

Similarly, the formation energy of a positively charged defect is equal to that of a neutral defect minus the energy released from (or plus the energy required for) transferring an electron from the one-electron defect energy level E_{d1} to the Fermi level E_f

$$U_{d+} \approx U_{d0} - (E_{d1} - E_f) \qquad (2.21)$$

The weak bond model does not specify the mechanism of bond-breaking (in particular whether hydrogen is involved in the bond breaking process or not) and whether the created dangling bond pairs remain coupled or diffuse apart. For example, a model in which hydrogen is released from a Si–H bond and breaks a weak Si–Si bond by attaching to one of the Si atoms can be described by the reaction (Fig. 2.12)

$$\text{Si–H} + \textit{weak bond} \rightleftarrows D_{\mathrm{H}} + D_{\mathrm{W}} \qquad (2.22)$$

Another model can be constructed by assuming hydrogen release from a second Si–H bond and the saturation of the weak bond with two hydrogen atoms. Other models of the same general type can be constructed as well [30]. Whether or not hydrogen is involved

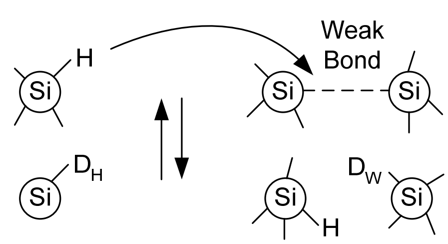

Fig. 2.12. Illustration of the hydrogen-mediated weak-bond model [30]. A hydrogen atom moves from a Si–H bond and breaks a weak Si–Si bond, leaving two defects D_{H} and D_{W}.

in structural equilibration is controversial and the subject of active research. This is further discussed in section 2.7.4.

2.7.3 Metastability

An external excitation that shifts the position of the Fermi level alters the distribution of the formation energies of charged defects. As a result, the density of charged defects is driven to a new steady-steady value which is different from that in thermal equilibrium. This is referred to as "metastability" and accounts for the drift of the electrical characteristics of *a*-Si:H devices during operation. The most widely-studied metastable phenomena are light-induced defect generation, particularly for *a*-Si:H solar cell applications [31][32][33][34] and bias-induced defect generation, which is important in *a*-Si:H thin-film transistors [35][36]. Other metastable phenomena include defect generation induced by space-charge limited currents [37] and metastable changes in doping efficiency [38][39].

The most important characteristic of metastable phenomena is their reversibility. If the external excitation is removed, the equilibrium densities relax to their thermal equilibrium values. The relaxation is thermally activated (the barrier height for the reverse reaction is $E_B - U$). Irreversible structural changes in *a*-Si:H are not referred to as metastability. Annealing *a*-Si:H at high temperatures (> 400°C), for instance, removes most of the hydrogen and results in an irreversible change in materials properties (unless hydrogen is incorporated back into *a*-Si:H through a different process).

The barrier height (activation energy) for the forward reaction (defect creation) (E_B in Fig. 2.9) is lowered by E_X in the presence of an external excitation. The forward reaction remains thermally activated (with an activation energy $E_B - E_X$) if $E_X < E_B$, and becomes athermal if $E_X > E_B$. Bias-induced defect generation in *a*-Si:H TFTs is an example of a thermally activated process while light-induced defect generation in *a*-Si:H solar cells is generally athermal (within a wide temperature range). In the case of solar cells, the energy required for lowering the barrier height is provided by the recombination of light-induced carriers while in *a*-Si:H TFTs this energy is provided by the trapping of bias-induced carriers in dangling bonds [1].

2.7.4 Kinetics of Equilibration

The relaxation data of Fig. 2.10 (a) and (b) follow a "stretched exponential" time dependence, expressed as (for a function of time such as $f(t)$)

$$f(t) = f(\infty) + [f(0) - f(\infty)]\exp[-(t/\tau)^{\beta}] \qquad (2.23)$$

where τ is the relaxation time and $0 < \beta < 1$. Defining $\Delta f(t) = f(t) - f(0)$ and hence $\Delta f(\infty) = f(\infty) - f(0)$, Eq. (2.23) may be rewritten as

$$\Delta f(t) = \Delta f(\infty)(1 - \exp[-(t/\tau)^{\beta}]) \qquad (2.24)$$

For short stress times ($t << \tau$) the stretched exponential can be approximated by a power law relation

$$\Delta f(t) = \Delta f(\infty)[t/\tau]^{\beta} \qquad (2.25)$$

The stretched exponential time dependence is consistent with a distribution of barrier heights in the configuration diagram of Fig. 2.9 and can be interpreted as a distribution of time constants, rather than a single time constant corresponding to a simple exponential ($\beta = 1$) (indicating a single barrier height for all defects, which is not the case). There are two classes of models for explaining the kinetics of stretched exponential relaxation which differ on the assumption of the rate-limiting mechanism.

Defect-controlled models – these models have been applied to other amorphous materials such as naphthalene and anthracene as well and can be explained based on the configuration coordinate diagram of Fig. 2.9 [43][44][45][46]. Assuming the density of species in the ground state (e.g. that of weak bonds) and in the high energy state (e.g. that of dangling bonds) at energy E_i are $n_1(E_i)$ and $n_2(E_i)$, respectively, and assuming a transition probability W_F from the ground state to the high energy state (e.g. for defect creation) and W_R from the high energy state to the ground state (e.g. for defect annealing), the rate of change in $n_1(E_i)$ and $n_2(E_i)$ is

$$\frac{\mathrm{d}n_1(E_i)}{\mathrm{d}t} = -\frac{\mathrm{d}n_2(E_i)}{\mathrm{d}t} = -n_1(E_i)W_F(E_i) + n_2(E_i)W_R(E_i) \qquad (2.26)$$

Assuming exponential (and continuous rather than discrete) distributions of states based on thermodynamic arguments [47]

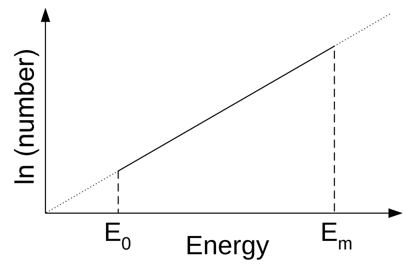

Fig. 2.13. Exponential distribution of states assumed for weak bonds and defects in the defect controlled model, based on thermodynamic arguments.

$$\frac{dn_1(E)}{dE} = \kappa_1\, \mathrm{e}^{E/kT^*} \quad \text{and} \quad \frac{dn_2(E)}{dE} = \kappa_2\, \mathrm{e}^{E/kT^*} \tag{2.27}$$

where T^* is a characteristic temperature (commonly referred to as the *freeze-in* temperature, above which the defects are in thermal equilibrium but below which thermal equilibrium cannot be maintained) and κ_1 and κ_2 are normalization constants given by $\kappa_1 = [N_1(t)/kT^*]\exp(-E_{m1}/kT^*)$ and $\kappa_2 = [N_2(t)/kT^*]\exp(-E_{m2}/kT^*)$, where $N_1(t) = \int_{E_0}^{E_{m1}} n_1(E)\mathrm{d}E$ and $N_2(t) = \int_{E_0}^{E_{m2}} n_2(E)\mathrm{d}E$ are the total densities, and E_{m1} and E_{m2} are the upper energy ranges in the distributions (Fig. 2.13) for the ground state and high energy state, respectively. With this assumption, Eq. (2.27) gives

$$\begin{aligned}\frac{\mathrm{d}N_1(t)}{\mathrm{d}t} = {} & -N_1(t)\int_{E_0}^{E_{m1}} \frac{\mathrm{d}E}{kT^*} W_F(E) e^{-(E-E_{m1})/kT^*} \\ & + N_2(t)\int_{E_0}^{E_{m2}} \frac{\mathrm{d}E}{kT^*} W_R(E) e^{-(E-E_{m2})/kT^*}\end{aligned} \tag{2.28}$$

For a thermally activated process, $W_F = k_F \exp(-E/kT)$ and $W_R = k_R \exp(-E/kT)$ where k_F and k_R are the transition rate constants. A solution to Eq. (2.28) can be thus found as ($N_0 = N_1$(t) + N_2(t) is the total number of states which is constant) [46]

$$N_2(t) = \frac{N_0}{1+\gamma} + C_1 \exp[-(t/\tau)^\beta] \tag{2.29}$$

where $\gamma = (k_R/k_F)\exp[(E_{m2} - E_{m1})/kT^*]$, C_1 is a constant determined from the initial condition, $\beta = T/T^*$ and $\tau = \nu^{-1}\exp(E_{act}/kT)$ with $E_{act} = kT^*\ln(\nu) + E_{MN}$ and $E_{MN} = kT^*\ln\beta - kT^*\ln[k_F\exp(-E_{m2}/kT^*) + k_R\exp(-E_{m1}/kT^*)]$. The parameter ν can be interpreted as an "attempt to reconfigure" frequency, which shows the ease of reconfiguration.

In the presence of an external excitation (e.g. illumination of *a*-Si:H solar cells or applying a gate voltage in *a*-Si:H TFTs), the reaction expressed by Eq. (2.17) is driven to the right and $k_F >> k_R$, therefore $\gamma << 1$ and (note that within the weak-bond model, $N_D(t) = N_2(t)$ and $N_{WB}(t) = N_1(t)$)

$$N_2(t) = N_2(\infty) + [N_2(0) - N_2(\infty)]\exp[-(t/\tau)^{\beta}] \qquad (2.30)$$

In the case of defect annealing, the reaction is driven to the left, $k_R >> k_F$ and γ is large, and therefore

$$N_2(t) = N_2(0) + [N_2(0) - N_2(\infty)]\exp[-(t/\tau)^{\beta}] \qquad (2.31)$$

In both cases, the time dependence is stretched exponential.

Diffusion-controlled models – These models are based on a link between the dispersive diffusion of hydrogen and the structural equilibration [42][48][49]. Diffusion of hydrogen in *a*-Si:H has been studied extensively by annealing *a*-Si:H films at different temperatures and for different annealing times, and measuring the change in the hydrogen distribution profile using techniques such as secondary ion mass spectroscopy (SIMS) [50][51][52]. For example, high temperature annealing can change a uniform distribution of hydrogen to a complementary error function as a result of hydrogen diffusion to the surface of the film followed by hydrogen desorption (out of the film) at the surface [52]. These experiments show a dispersive diffusion coefficient for hydrogen which can be expressed as [49]

$$D_{\mathrm{H}} = D_{\mathrm{H0}}(\omega_0 t)^{-\alpha} \qquad (2.32)$$

where ω_0 is an attempt frequency, D_{H0} is the temperature dependent diffusion coefficient and α = 0.2–0.25 at 200°C.

A time-independent rate constant for a structural change, for example defect creation or annealing, results in a simple exponential but the experimental observation of a stretched exponential indicates a time-dependent rate constant $v_E(t)$

$$\frac{d}{dt}\Delta N_D(t) = -v_E(t)\Delta N_D(t) \qquad (2.33)$$

Assuming that hydrogen diffusion is the rate limiting mechanism, the rate constant $\nu_E(t)$ can be assumed to be equal to the hydrogen hopping rate, D_H/a^2, where a is the characteristic hopping distance that hydrogen moves in a single diffusion step (which is time-independent). Using the expression for D_H from Eq. (2.32) to solve Eq. (2.33) results in the exponential time dependence

$$\Delta N_D(t) = N_{D0}\exp[-(t/\tau)^\beta] \tag{2.34}$$

where $\beta = 1-\alpha$. Assuming the dispersion in D_H arises from an exponential distribution of sites, i.e. $\exp(-E/kT_0)$, results in $\beta = T/T_0$ [48].

Within the weak bond model, the defect-controlled model predicts an exponential distribution of weak Si–Si bond energies, while the diffusion-controlled model predicts an exponential distribution of bond energies for the release of hydrogen from Si–H bonds. Despite the quite different physics, both models explain the experimental data equally well using analogous parameters. The reason that both models give the same annealing and production kinetics is that the underlying disorder in the amorphous silicon is the main determinant of the form of the relaxation in each model [46]. The strength of the second model is that unlike the first model, it links the stretched exponential relaxation to a phenomenon (dispersive diffusion of hydrogen) that can be characterized through direct measurements. However, since both models fit the experimental data, the equilibration kinetics alone cannot be used as proof that hydrogen is involved in metastable defect relaxation. There are also experimental studies that suggest hydrogen may be involved in the bond breaking process but not as the rate-limiting step [53].

In this thesis, the weak bond model is adopted in its general form, Eq. (2.17), and the experimental results are explained in terms of the energy distribution of weak Si–Si bonds. However, no attempt has been made to rule out the possibility of hydrogen involvement. Investigating the role of hydrogen in structural equilibration is beyond the scope of this thesis.

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Amorphous Silicon Thin-Film Transistors: Fabrication Process and Device Operation

Hydrogenated amorphous silicon thin-film transistors (*a*-Si:H TFTs) were first demonstrated in 1979 [1] and soon became the dominant active devices used in the commercial production of active-matrix liquid crystal displays (AM-LCDs), optical scanners and radiation imagers. In this chapter, the device structure and operation of *a*-Si:H TFTs is reviewed, followed by a brief survey of material growth techniques for the fabrication of these devices. At the end, the standard process for the fabrication of *a*-Si:H TFTs in our lab is presented.

3.1 *Device Structures*

In contrast to VLSI field-effect devices where the channel is lightly doped to adjust the threshold voltage, the channel of *a*-Si:H TFTs are undoped. This is because of the significant reduction of mobility in doped *a*-Si:H (Section 2.6). In addition, since the mobility of holes is too low in *a*-Si:H due to a high density of valence-band tail states (Section 2.3.1), all practical *a*-Si:H TFTs are n-channel devices (with n^+ source/drain contacts for electron injection).

The standard *a*-Si:H TFTs are fabricated with "inverted-staggered" structures which may be either back-channel etched (BCE) (Fig. 3.1 (a)) or back-channel passivated (BCP) (Fig. 3.1 (b)). The term "inverted" refers to the bottom-gate configuration and "staggered" indicates that the source/drain contacts and the gate are located on the different sides of the device (source/drain on the top for a bottom-gate structure and on the bottom for a top-gate structure). In the BCE structure, the TFT channel length is

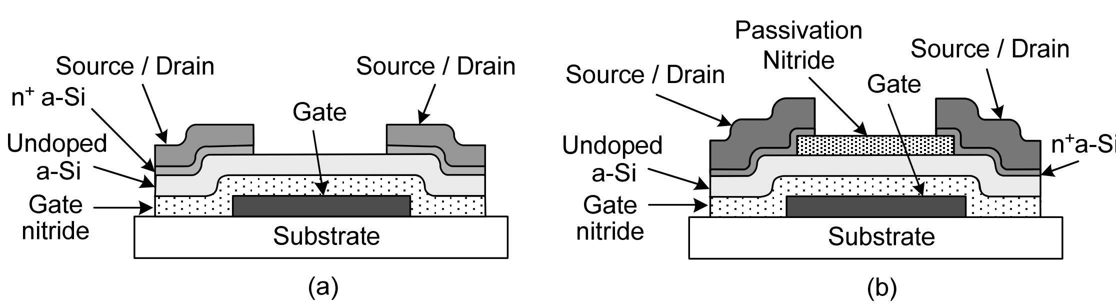

Fig. 3.1. Schematic cross-section of (a) back-channel etched (BCE) and (b) back-channel passivated (BCP) standard *a*-Si:H TFT structures.

determined by the separation between the source and drain contacts, whereas in the BCE structure, the length of the top nitride passivation layer determines the channel length. The overlap between the gate and the source/drain contacts in necessary to assure sufficiently low source/drain contact resistance [2].

Hydrogenated amorphous silicon nitride (*a*-SiN_x:H) grown by plasma-enhanced chemical vapor deposition (PECVD) provides the best channel/dielectric interface quality and the best TFT characteristics among the other candidates. PECVD-grown silicon oxide in particular results in a poor interface quality and TFTs with high subthreshold slopes [3]. For reasons which are still not clearly understood, the top-gate structure grown with PECVD *a*-SiN_x:H results in a poor channel/dielectric interface quality compared to the bottom gate structure [4]. The reason is thought to be the ion bombardment of *a*-Si:H surface from the nitride deposition plasma when nitride is deposited on top of *a*-Si:H.

In the BCE structure, the TFT stack (the gate nitride, the undoped *a*-Si:H channel and the n^+ *a*-Si:H for the source-drain contacts) are deposited within one vacuum pump-down (without exposure to the ambient between the depositions) for best gate nitride/*a*-Si:H interface quality. After patterning the source/drain contacts, the n^+ layer is removed from the top of the channel (typically by dry etching) using the source/drain contacts as the mask. Since the etchant for n^+ can also etch undoped *a*-Si:H, the etching for removing the n^+ layer has to be carefully timed to assure the complete removal of the n^+ layer, while avoiding the complete removal of the undoped *a*-Si:H channel. To allow sufficient tolerance, a relatively thick undoped *a*-Si:H layer must be used.

In the BCP structure, the TFT stack (the gate nitride, the undoped *a*-Si:H channel and the passivation nitride) are deposited again within one pump-down for best gate nitride/*a*-Si:H interface quality and also to avoid the exposure of the *a*-Si:H channel to the ambient. The n^+ layer is deposited and patterned after the patterning of the passivation nitride. Since the etchant for the nitride is fairly selective to *a*-Si:H, relatively thin *a*-Si:H channel layers can be used in contrast to the BCE structure.

The main advantage of the BCE structure compared to the BCP structure is avoiding an extra mask step for pattering the passivation nitride. Reducing the number of mask steps can significantly reduce the manufacturing costs especially for large-area

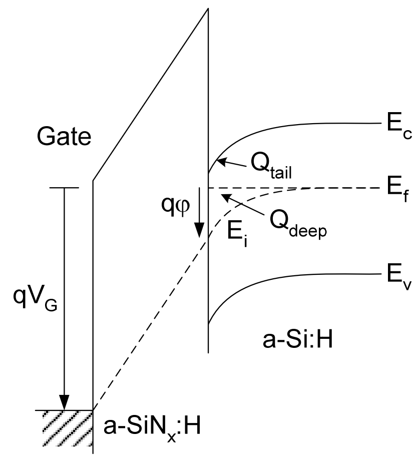

Fig. 3.2. Band diagram showing the operation of *a*-Si:H TFTs under positive gate voltage bias. The charge induced by the gate in *a*-Si:H is divided between the tail states and the deep states.

display applications [5]. The absence of the passivation nitride in the BCE structure, however, exposes the channel to the ambient and plasma-etch damage during the fabrication process, which can have an adverse effect on the device stability. In addition, the thick *a*-Si:H layer used for the BCE structure increases the light sensitivity of the TFT, which is not desirable for most applications. The application requirements and the economical considerations therefore determine the type of the TFT structure suitable for a particular application.

Alternative *a*-Si:H TFT structures with specific advantages have been proposed and demonstrated but have not been used in commercial production yet. Some examples are double-gate TFT structures for increasing the drive currents [6], vertical TFTs for reducing the TFT area on the chip [7][8] and top-gate self-aligned TFTs for increasing the TFT switching speed [9].

The fabrication process for the standard BCE and BCP *a*-Si:H TFTs in our lab is presented in Section 3.4.

3.2 *Device Operation*

The operation of *a*-Si:H TFTs can be generally described by a band diagram similar to that of field-effect VLSI devices with single-crystalline channels (Fig. 3.2). The main difference is however the presence of gap states in *a*-Si:H. To discuss the flat-band condition, we neglect the work-function difference between the gate electrode and the *a*-

Si:H channel, and assume negligible charges trapped in the nitride or at the *a*-Si:H/nitride interface, so that the flat-band voltage corresponds to zero bias on the gate. At flat band, the Fermi level is close to the mid-gap. Neglecting the effect of thermal activation for simplifying the argument, the states below the Fermi level (acceptor levels) are full (and thus neutral) and the states above the Fermi level (donor levels) are empty (and thus neutral) and therefore no charged states exist (Due to thermal excitation at finite temperatures, some of the states above the Fermi level are full and thus negatively charged, and some of the states below the Fermi level are empty and therefore positively charged; however, the net charge is zero due to charge neutrality). As the gate voltage is increased, the Fermi level moves up in the band, creating negatively charged states (donor levels with trapped electrons) which are in charge neutrality with the positive charges accumulated in the gate. At finite temperatures, a small fraction of the induced electrons are thermally excited to the extended states, but their number is small and less than 10% (even in the strong electron accumulation regime), which is the ratio of the effective mobility to the band mobility as explained in section 2.3.1. Therefore a reasonably accurate analysis can be performed by assuming that the majority of the field-induced electrons are trapped in the gap states and solving the Poisson equation accordingly [2]

$$\frac{\mathrm{d}^2\varphi(x)}{\mathrm{d}x^2} = \frac{q}{\varepsilon_{Si}}\int N(E)\big(f[E+q\varphi(x)] - f(E)\big)\mathrm{d}E \tag{3.1}$$

where $\varphi(x)$ is the band bending (electric potential, defined at zero in the "bulk" *a*-Si:H), q the electron charge, ε_{Si} the dielectric permittivity of *a*-Si:H (close to that of single crystalline Si, i.e. $11.7\varepsilon_0$, under DC operation), $N(E)$ the density of states, and $f(E)$ the Fermi level. Various *a*-Si:H TFT models that consider the gap state distribution of *a*-Si:H have been developed, some of which are particularly useful for circuit simulation [10][11][12].

A less accurate but a very useful approach (particularly from the circuit analysis point of view) is to model the *a*-Si:H TFT as a field-effect VLSI device with an effective (or apparent) field-effect mobility and threshold voltage that fit the TFT characteristics over an operation regime of interest. Using first-order MOS equations for the saturation and linear operation regimes, the TFT current can thus be described by

$$I_{DS,\,sat} = \frac{1}{2}\mu_{FE} C_{SiNx} \frac{W}{L}(V_{GS} - V_T)^2 \tag{3.2}$$

$$I_{DS,\,lin} = \mu_{FE} C_{SiNx} \frac{W}{L} V_{DS}(V_{GS} - V_T - V_{DS}/2) \tag{3.3}$$

where μ_{FE} is the effective (or apparent) field-effect mobility, V_T the effective (or apparent) threshold voltage, $C_{SiNx} = \varepsilon_{SiNx}/t_{SiNx}$ the gate dielectric capacitance of the nitride per unit area (ε_{SiNx} is the dielectric constant of the gate nitride close to $7.5\varepsilon_0$ and t_{SiNx} is the thickness of the gate nitride), W the channel width, L the channel length and V_{DS} the drain-source voltage. Because of the sharp slope of the conduction band tail, practically all electrons reside at the bottom of the band tail (with a small fraction thermally excited to upper levels) with an effective density of N_t at $E_c - E_t$. Therefore (see Section 2.3.1)

$$\mu_{FE} \approx \mu_0 (N_c / N_t) \exp(-E_t / kT) \tag{3.4}$$

where μ_0 is the band mobility, E_c the conduction band mobility edge and N_c the effective density of states at E_c. The activation energy E_t is found to be about 0.17eV from temperature-dependent measurements of the field-effect mobility [13]. As the gate voltage is increased, the Fermi level gets past the midgap defect states and enters the band tail. Assuming negligible thermal excitation, V_T is the gate voltage corresponding to the Fermi level position at the onset of the tail states. In practice, V_T is smaller because of thermal excitation of carriers above the Fermi level which allows the majority of the electrons to reside in the band-tail before the Fermi level enters the band-tail.

Note that the effect of two-dimensional confinement, vertical gate electric-field and source/drain contact resistance in lowering the mobility is not included in Eq. (3.4). However, similar to VLSI devices, these effects are included in the effective mobility extracted by fitting the device characteristics to Eq. (3.2) or Eq. (3.3). Also it should be noted that the extracted values of μ_{FE} and V_T for an *a*-Si:H TFT are generally different in the saturation and linear regimes. However, the extracted values are close and the difference can be neglected for a first-order analysis.

Field-Effect Measurement of the Density of States – Eq. (3.1) describes the effect of gap states on the operation of *a*-Si:H TFTs. This equation can be also used to

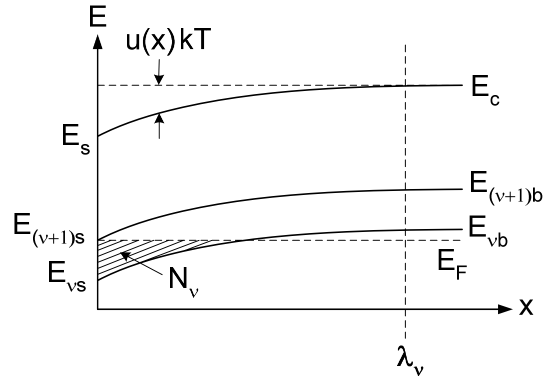

Fig. 3.3. Band diagram illustrating the field-effect analysis. Localized states of volume N_v, which lie between E_{vb} and $E_{(v+1)b}$ in the bulk, cross the Fermi level at the surface and change their electron occupation.

extract the density of gap states from the measured electrical TFT characteristics. This method was first proposed in 1972 and is known as the field-effect measurement [14]. In fact, the original reason to construct the *a*-Si:H TFT structure was to measure the density of states in *a*-Si:H rather than developing a useful field-effect device. However, these measurements eventually led to the development of the *a*-Si:H transistor devices by the same group [1].

This method can be explained using the band diagram of 0. Assume the gate voltage V_G is increased from the flat-band voltage V_{FB} to $V_{FB} + v\Delta V_G$ (v is an integer) in v steps each equal to ΔV_G. When V_G is increased from $v\Delta V_G$ to $(v+1)\Delta V_G$, localized states lying between E_{vb} and $E_{(v+1)b}$ cross E_f at the surface ($x = 0$), and change their electron occupation from empty to full. After the v-th step, the space charge density in the localized states is $v\Delta N_s/\lambda_v$, where λ_v is the depth of the accumulation layer and ΔN_s is the change in the accumulated charge per each voltage step, equal to $C_{SiNx}\Delta V_G$. The Poisson equation in the accumulation after the v-th step is:

$$E_v(x) = E_c - \frac{A_v}{\lambda_v}(x - \lambda_v)^2 \qquad (3.5)$$

where $A_v = (q/2\varepsilon_{Si})\,\Delta N_s\, v$. Introducing the dimensionless variable $u(x) = (E_c - E(x))/kT$ and at the surface $u_s = (E_c - E_s)/kT$, the electron density in the extended states between $x = 0$ and $x = \lambda_v$ is given by $n(x) = n_b \exp u(x)$, where n_b is the electron density in the bulk ($x > \lambda_v$). The ratio of the TFT current at the v-th step (i_v) to that of the flat-band (i_0) is equal to the ratio of the carrier densities at these two points

$$\frac{i_v}{i_0} = \frac{n_v}{n_b} = 1 - \frac{\lambda_v}{d} + \frac{1}{d}\int_0^{\lambda_v} \exp[u(x)]\mathrm{d}x \tag{3.6}$$

where d is the thickness of the a-Si:H layer. This can be rewritten as

$$\frac{A_v}{kT} d\left(i_v / i_0 - 1\right) = \sqrt{u_s} \int_0^{\sqrt{u_s}} \exp(t^2)\,\mathrm{d}t \tag{3.7}$$

Also from Eq. (3.5)

$$\lambda_v = u_{vs} kT / A_v \tag{3.8}$$

And knowing the initial position of the Fermi level E_i, the position of E_{vb} relative to E_c is given by $E_c - E_{vb} = E_c - E_i - u_{vs}kT$. Finally, the density of localized states N_v corresponding to the v-th step is found by equating the total density of electrons in the space charge region to the sum of the contributions from each step

$$\frac{v\Delta N_s}{\lambda_v} = \sum_{i=0}^{v-1} N_i \Delta E_i + N_v \Delta E_v \tag{3.9}$$

giving

$$N_v = \frac{v\Delta N_s}{\Delta E_v \lambda_v} - \frac{1}{\Delta E_v}\sum_0^{v-1} N_i \Delta E_i \tag{3.10}$$

It should be noted that mathematically, the voltage steps must be infinitesimally small rather than discrete step voltages and such a mathematically accurate analysis will lead to integral equations rather than summations. However, for the sake of numerical calculation, and given that the voltage steps are chosen small enough for sufficient accuracy, the analysis reviewed here is the most useful mathematical form.

An example of the distribution of states in a-Si:H TFTs with thermal oxide and PECVD nitride gate dielectrics extracted by field-effect measurements is plotted in Fig. 3.4 [15]. The dependence of the density of states on the type of the gate dielectric material is an indication that the gate dielectric material can affect the quality of a-Si:H close to the interface. Further evidence may be that the TFT properties (such as mobility) which are closely related to a-Si:H can be influenced by the growth conditions of the gate insulator [16][17]. The density of states measured by field-effect measurements is normally higher than that in the bulk indicating that the gate dielectric induces additional electronic states at the interface which are typically referred to as surface or interface

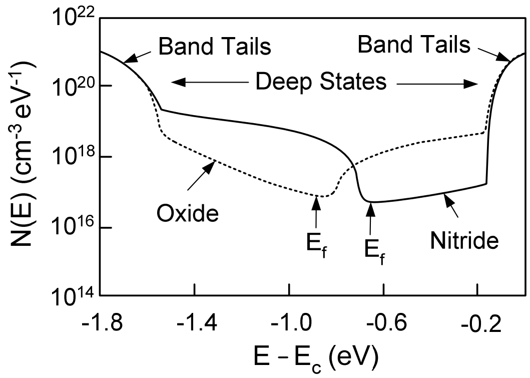

Fig. 3.4. The density of gap states in a-Si:H close to the channel/dielectric interface extracted using the field-effect method from a-Si:H TFTs with nitride or oxide gate dielectrics [15]. E_f is the Fermi level at flat-band.

states [18][19]. Recent work with a new hybrid gate dielectric and field-effect mobilities nearly twice as high as that in the bulk suggests that the density of states close to the interface may be actually lower than that in the bulk [20][21]. In this thesis, the dependence of the TFT stability on the gate nitride at low gate electric fields (where the TFT stability is related to the quality of *a*-Si:H rather than the gate nitride) is presented as further evidence that the quality and microstructure of *a*-Si:H close to the interface can be affected by that of the gate nitride (Chapter 5).

3.3 *Material Growth*

In this section, the growth of *a*-Si:H TFT stack materials is reviewed. This includes the growth of undoped *a*-Si:H for the TFT channel, the growth of *a*-SiN$_x$:H for the gate dielectric (as well as the top passivation layer) and the growth of doped *a*-Si:H for source and drain contacts.

3.3.1 Growth of Undoped *a*-Si:H

The most widely-used method for the growth of *a*-Si:H is plasma-enhanced chemical vapor deposition (PECVD). Hydrogenated *a*-Si was grown for the first time in 1969 using this technique [22]. This development was a major breakthrough because of the capability to contain hydrogen in the *a*-Si film, in contrast to other techniques such as sputtering or thermal evaporation. Standard *a*-Si:H TFTs which are in the commercial production of large-area displays today are grown by PECVD using pure silane (SiH_4) at temperatures close to 250°C [23]. The role of the plasma is to provide sufficient energy to crack the silane molecules at low temperatures. In the absence of a plasma, temperatures higher than 450°C are required to decompose silane. At such high deposition temperatures, hydrogen is not retained in the film, resulting in a poor film quality. Temperatures higher than 550°C are typically used for the growth of polycrystalline or epitaxial silicon films.

An alternative technique for growing *a*-Si:H is hot-wire chemical vapor deposition (HWCVD) which has been reported both for TFT and solar cell applications [24][25][26]. An advantage of HWCVD as an alternative is the elimination of in-situ plasma damage to the film during growth. However, it is difficult to scale up the HWCVD technique for large areas. In addition, since the industrial infrastructure is based on highly-established PECVD equipment, alternative growth techniques such as HWCVD that require new infrastructure development are generally not economical.

Growth Mechanism – Several silane dissociation reactions are possible during the PECVD of *a*-Si:H. Silane molecules may also react with the radicals produced from the dissociation of other silane molecules and form larger molecules such as Si_2H_6 and Si_3H_8. These larger molecules may in turn decompose and form new radicals [27]. Since the mean free path of the gas molecules and radicals (in the range of 10–100μm at typical deposition pressures) is much smaller than the reactor dimensions, the possibility of secondary collisions and intermolecular reactions is very high and therefore understanding the deposition mechanism is very difficult [23][28]. Some of the silane dissociation reactions that require the lowest energies are [29]

$$SiH_4 \rightarrow SiH_2 + H_2 \qquad 2.2\ \text{eV} \tag{3.11}$$

$$SiH_4 \rightarrow SiH_3 + H \qquad 4.0\ \text{eV} \tag{3.12}$$

$$SiH_4 \rightarrow Si + 2H_2 \qquad 4.2\ \text{eV} \tag{3.13}$$

The growth mechanism of *a*-Si:H and particularly the question of which species cause the deposition are controversial, but the common view is that at least for the low plasma powers typically used for the growth of *a*-Si:H from pure silane, SiH_3 radicals are the dominant species [30][31]. With this assumption, some of the processes which may occur at the surface of *a*-Si:H during growth are illustrated in Fig. 3.5[32]. A hydrogen-

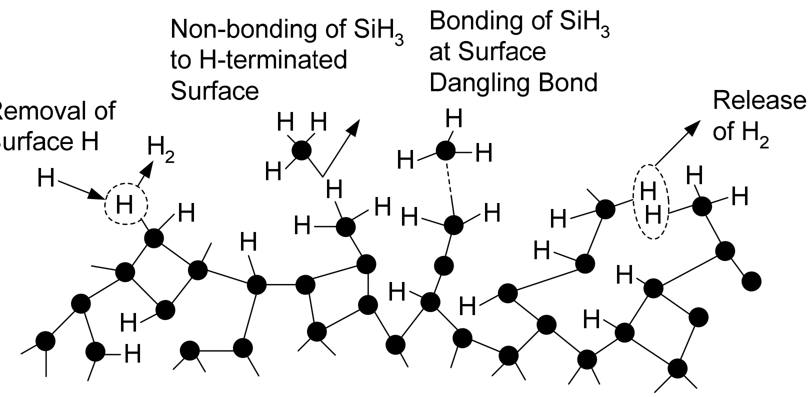

Fig. 3.5. Illustration of some of the possible reactions at the growth surface of *a*-Si:H [32].

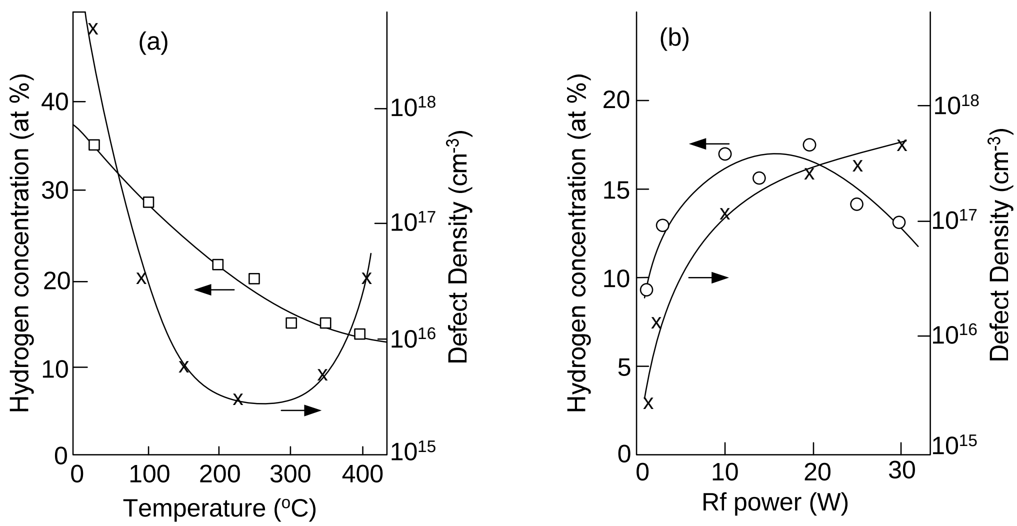

Fig. 3.6. Effect of substrate temperature and RF plasma power on defect density and hydrogen concentration of PECVD *a*-Si:H [33].

terminated silicon atom cannot pick up SiH_3, therefore hydrogen release from the surface is a necessary reaction in this growth model.

Growth Parameters – The PECVD growth conditions have a direct impact on the quality of the *a*-Si:H film. The optimum chamber pressure is in the range of 0.1–1Torr. Striking and maintaining the plasma may not be possible at low pressures, while at high pressures, the low mean free path of the gas molecules may result in most of the chemical reactions occurring away from the substrate surface. The optimum deposition temperature is in the range of 200–300°C [33]. High and low deposition temperatures both result in high defect densities in the film. At low temperatures, the high sticking coefficient and low diffusivity of the gas species at the growth surface results in a large number of dangling bonds. The main reason for a high defect density at high temperatures is insufficient hydrogen retention. The defect density in the film increases with increasing the RF power density. This is generally believed to be due to the ion bombardment of the growth surface from the plasma. Reducing the plasma power reduces the growth rate of the *a*-Si:H film and increases the cost of the film growth. Therefore there is often a trade-off between the quality and the cost of *a*-Si:H films. In addition, striking and maintaining the plasma may not be possible at low RF powers. A common way to reduce the plasma damage is to keep the plasma away from the growth surface by inserting a metal grid between the plasma plate and the substrate holder, which is known as a "triode" structure (versus the conventional "diode" structure with only two parallel electrodes). The gas flow rates determine the residence time of the gas species inside the chamber. Low gas flow rates (especially if combined with high plasma powers) may result in the complete consumption of silane in reactions away from the growth surface. The dependence of the *a*-Si:H material properties on the deposition conditions is shown in Fig. 3.6 [23][33][34].

Effect of Diluents – Silane may be diluted with another gas for the growth of *a*-Si:H. The most widely-used diluent gas is hydrogen which is commonly used for the growth of *a*-Si:H for solar cell applications [35]. High hydrogen dilution ratios result in the growth of nanocrystalline silicon rather than *a*-Si:H; however, for reasons which are still controversial, most stable solar cells are grown at the amorphous/nanocrystalline transition regime [36][37]. As for *a*-Si:H TFT applications, using hydrogen dilution in silane has been reported mainly for low-temperature (<200°C) *a*-Si:H growth, which is of interest for plastic substrates with low working temperatures [38][39][40]. The issue of plastic compatibility is discussed in Chapter 4. Hydrogen dilution in silane at standard *a*-Si:H deposition temperatures (~250°C) can be used as a technique to improve the lifetime of *a*-Si:H TFTs. This technique is presented in Chapter 5.

Inert gases such as argon are commonly used to dilute silane for the growth of polycrystalline or epitaxial silicon at high temperatures. Argon dilution does not affect the growth of high-temperature polycrystalline or epitaxial silicon; however, it has a detrimental effect on the PECVD growth of *a*-Si:H. Argon dilution averts the growth of *a*-Si:H from a CVD to a PVD (physical vapor deposition) process. In a CVD process, gas species have low sticking coefficients and therefore are continually absorbed and released from the growth surface before eventual reacting and being absorbed to the growth surface. Therefore the rate of the chemical reactions at the growth surface determines the growth rate rather than the flux of species striking the surface [41]. In contrast, in a PVD process, the gas species have high sticking coefficients and therefore the growth rate depends on the flux of the species striking the surface. The presence of highly reactive gas species favors a CVD process, while nonreactive species such as argon favor a PVD process. Under PVD conditions, *a*-Si:H films grow in a columnar structure rather than conforming to the growth surface and have high defect densities not suitable for device applications [42].

3.3.2 Growth of *a*-SiN_x:H

The standard method of nitride growth for *a*-Si:H TFT applications is PECVD. Other growth methods such as HWCVD exist but not used in production [43][44]. The typical PECVD nitride films are grown from a mixture of silane and ammonia or a mixture of silane and nitrogen. Films with nitrogen to silicon atomic ratios close to the stoichiometric value of 4/3 are typically referred to as nitrogen-rich, while those with smaller ratios are typically referred to as silicon-rich. The gas flow ratios are normally adjusted for the growth of nitrogen-rich films. Nitrogen-rich films are known to result in steeper TFT subthreshold slopes and higher electrical stability [45][46].

Growth Mechanism – Studying the growth mechanisms of *a*-SiN_x:H is more complicated than that of *a*-Si:H as two types of atoms (silicon and nitrogen) are involved in the plasma reactions. Direct mass spectroscopy inside the reaction chamber shows the presence of several species including $(SiH_3)_2$ (disilane) and $Si(NH_2)_3$ (triaminosilane) [47]. The ratio of triaminosilane to disilane radicals increases with increasing the plasma power. The growth rate of nitride also increases with increasing plasma power suggesting that triaminosilane is directly involved in the film growth. Based on these studies and other experiments, a growth model constructed upon triaminosilane absorption at the growth surface and condensation of the film by ammonia (NH_3) release has been proposed (Fig. 3.7) [47]. Based on this model, the overall chemistry of the growth reactions can be summarized in the form of the following reactions

$$SiH_4 + 4NH_3 \rightarrow Si(NH_2)_4 + 4H_2 \qquad (3.14)$$

$$3Si(NH_2)_4 \rightarrow Si_3N_4 + 8NH_3 \qquad (3.15)$$

The first reaction represents the formation of the gas phase precursor driven by the plasma power and the second reaction represents the surface condensation reaction driven by the substrate temperature. It should be noted that this model applies to amino-saturated conditions (nitrogen rich growth conditions and relatively high plasma powers) which are typically used for the growth of the TFT gate nitride, rather than high disilane density conditions (silicon rich growth conditions and/or relatively low plasma powers).

***Growth Temperature* –** The growth temperature of the gate nitride has a direct impact on the TFT stability, and sufficiently high growth process temperatures are required for reasonably stable TFTs [40][48][49][50]. For standard *a*-Si:H TFTs, the gate nitride is grown at temperatures close to 300°C on glass. Lower process temperatures are desired for low-cost plastic substrates; however, the nitride quality is poor at low temperatures (<200°C). Hydrogen dilution may be used to improve the nitride quality grown at low temperatures [39][40][52]. However, in terms of TFT electrical stability, the quality of the gate nitride grown at low temperatures is not satisfactory for demanding applications such as driving organic light emitting diodes. The issue of *a*-Si:H TFT stability, growth temperature and plastic compatibility is discussed in Chapter 4.

3.3.3 Growth of Doped *a*-Si:H

Adding a small flow of phosphine or diborane to silane is used for the PECVD of n-type or p-type *a*-Si:H. The typical flow ratios of the dopant gases for n^+ or p^+ *a*-Si:H are in the few 100ppm range. Since the hole mobility is very low in *a*-Si:H (Section 2.3), *a*-Si:H TFTs are normally fabricated as n-channel devices with n^+ *a*-Si:H source and drain contacts. However, p-channel *a*-Si:H TFTs with p^+ contacts have been recently reported [20]. Both types of dopings are routinely used for the fabrication of *a*-Si:H solar cells with p/i/n structures.

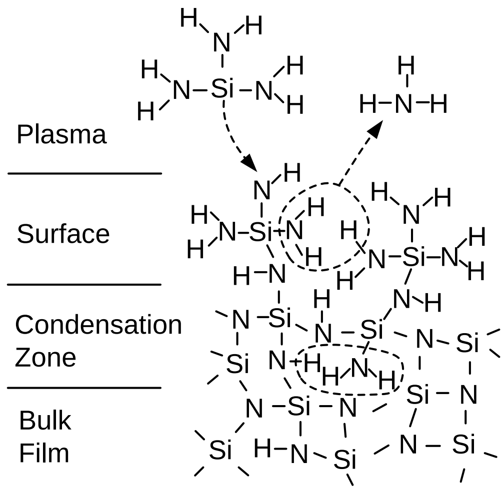

Fig. 3.7. Cross-sectional structure model of the PECVD growth of a-SiN_x:H [47].

3.4 *Standard TFT Process in Our Lab*

The standard process for the fabrication of back-channel etched (BCE) and back-channel passivated (BCP) TFT structures on glass and plastic substrates in our lab is covered in this section. The plastic compatibility of this process is contingent upon considerations discussed in Chapter 4.

***Our PECVD tool* –** The PECVD machine used in our lab for the growth of the TFT stack is a four-chamber machine with a load-lock and three deposition chambers for the growth of a-SiN_x:H, undoped a-Si:H and n^+ a-Si:H. To avoid cross-contamination, each chamber is allocated to the deposition of a single material. The adjacent chambers are separated from each other with high vacuum slit valves to allow the transfer of the samples between the chambers without exposure to the ambient. The samples are loaded through the load-lock for outgasing and then transferred to the deposition chambers.

***Back-channel Etched TFTs* –** The gate metal is deposited by thermal evaporation and patterned by standard photolithography and wet etching. We use a 15nm/50nm/15nm Cr/Al/Cr tri-layer as the gate metal to ensure high-temperature plastic compatibility for reasons discussed in Chapter 4. For glass substrates or low-temperature processes on plastic, an 80nm thick Cr layer may be used to reduce the process steps. The TFT stack (gate nitride/undoped a-Si:H channel/n^+ a-Si:H) is then deposited by PECVD in a single pumpdown (without exposure to the ambient between the depositions). The 300nm-thick gate nitride is deposited from a mixture of ammonia and silane ([SiH_4]/[NH_3] = 14 sccm/130 sccm) at 300°C and a plasma power density of 21 mW/cm^2. We define the plasma power density as the total power fed into the chamber by the RF generator, devided by the area of the plasma plate, which is 6"×6" (232.3 cm^2). The 250nm-thick undoped *a*-Si:H is deposited from pure silane ([SiH_4] = 50 sccm) at 250°C and 17 mW/cm^2. The 30nm-thick n$^+$ layer is deposited from a mixture of silane and premixed 1% phosphine – 99% hydrogen gas ([PH_3 –H_2]/[SiH_4] = 8 sccm/44 sccm) at 230°C and 17 mW/cm^2. The deposition pressure is 500 mtorr and the plasma frequency is 13.56 MHz for all the three depositions. After the TFT stack deposition, the undoped/n$^+$ *a*-Si:H layers are patterned by photolithography and dry etching to form the TFT active regions (islands). Via holes for the gate contacts are then opened in the gate nitride using photolithography and dry etching. Following a hydrofluoric acid (HF) dip step to remove the native oxide from the top of the n$^+$ layer, the source/drain metal is thermally evaporated and patterned by wet etching. We use a 15nm/250nm/15nm Cr/Al/Cr tri-layer for the source and drain contacts to ensure plastic compatibility for reasons discussed in Chapter 4. For glass substrates, a single Cr layer may be used instead of the Cr/Al/Cr tri-layer to reduce the process steps. In the Cr/Al/Cr tri-layer, the purpose of the top Cr layer is to assure a good contact with indium-tin-oxide (ITO) in case the TFTs are integrated with organic light-emitting diodes (OLEDs) for active-matrix OLED display applications. The source/drain metal is then used as a mask to remove the n$^+$ layer from the backside (top) of the channel by dry-etching. The finished TFTs are annealed at 180°C for 1 hour to repair the damage from the dry etch steps.

Back-channel Passivated TFTs – The deposition and patterning of the gate metal is the same as that for the BCE structure. After the PECVD growth of the gate nitride and undoped *a*-Si:H (with the same conditions as that of the BCE structure), a 200-nm thick passivation nitride is deposited at 230°C in the PECVD machine without exposing the sample to the ambient. The growth conditions of the passivation nitride (other than the growth temperature) are the same as that of the gate nitride. The passivation nitride is then patterned by photolithography and dry etching. Following an HF-dip step to remove the native oxide from the top of the *a*-Si:H layer, the n$^+$ layer is deposited with the same conditions as described for the BCE structure. The TFT active regions (islands) are then formed by patterning the undoped/n$^+$ *a*-Si:H layers using photolithography and dry etching. The remaining steps (opening the via holes in the gate nitride, removing the native oxide from the top of the n$^+$ layer, the deposition and patterning of the source and drain metal and thermal annealing) are the same as those described for the BCE structure.

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Active Matrix OLED Arrays with *a*-Si:H TFT backplanes on High-Temperature Clear Plastic: Design, Fabrication and Reliability

Active Matrix Organic Light Emitting Diode (AMOLED) displays are widely expected to dominate the future display market. In addition to the potential replacement of the current flat-panel cathode ray tube (CRT) and active-matrix liquid crystal displays (AMLCDs) with AMOLED displays in various conventional products, novel flexible display applications are expected to provide a critical market opportunity for AMOLED displays in the future. The low-cost and large-area deposition capability, as well as compatibility with flexible substrates, makes *a*-Si:H TFT technology very promising for manufacturing the TFT backplanes in AMOLED displays.

This chapter is focused on the design and fabrication of AMOLED test arrays with *a*-Si:H TFT backplanes on high temperature clear plastic substrates in our lab and studying the effect of the process temperature on the reliability of light emission in AMOLED displays. The issue of the plastic compatibility of the *a*-Si:H TFT process is also discussed.

4.1 *High-Temperature Clear Plastic*

As discussed in Chapter 3, standard *a*-Si:H TFTs are fabricated on glass with gate nitride growth temperatures close to 300°C. Replacing the glass substrates with plastic for the fabrication of AMOLED displays poses important requirements on the plastic substrates, which may be listed as follows (i) high glass transition temperature (>300°C), (ii) low coefficient of thermal expansion (<10ppm/°C), (iii) optical transparency, and (iv) process compatibility (vacuum and chemicals).

The high nitride growth temperatures are needed to assure acceptable device characteristics and in particular sufficient electrical stability. In this chapter, the effect of increasing the gate nitride growth temperature on improving the stability of *a*-Si:H TFTs and therefore increasing the reliability of light emission in AMOLED displays with *a*-Si:H TFT backplanes is verified experimentally (section 4.4) and further discussed in Chapter 5. The low coefficient of thermal expansion accompanied by the proper control of the mechanical stress and adhesion of the deposited layers is needed to avoid cracking and delamination of the layers (section 4.3). Optical transparency is required to allow the

Plastic Type	Optical Transmission (λ=700nm)/Thickness	T_g (°C)	CTE (ppm/°C)	Maximum Working Temperature (°C)
Polyethylene Terephthalate (PET)	88% / 125µm	70 – 110	15	< 120
Polyethylene Naphthalate (PEN)	82% / 125µm	120	13	130
Poly-Carbonate	90% / 125µm	130	60 – 70	120
New Clear Plastic	85% / 100 µm	> 300	< 10	300

Table 4.1. Comparison of the thermal and optical properties of the commercially available clear plastic substrates and the new clear plastic used in this work [5].

application of standard bottom-emission OLEDs. The compatibility of the plastic substrates with the standard micro-fabrication technology is also an important requirement. It is worth mentioning that Kapton® is a commercially available high-temperature plastic substrate which has been used extensively for the fabrication of *a*-Si:H TFTs [1][2][3][4]. However, Kapton® is not optically clear and therefore not suitable for AMOLED displays with standard bottom-emission OLEDs.

The commercially available clear plastic substrates which are compatible with the standard process technology do not meet the requirements of high working temperatures and low coefficients of thermal expansion. Therefore a novel clear plastic substrate that met these requirements was developed and provided by an industrial collaborator (the DuPont Company) for this purpose. The properties of the new clear plastic substrate are compared with those of the existing clear plastic substrates in Table 4.1 [5]. Because of the limitations of the conventional clear plastic substrates, the process temperature of the AMOLED displays reported on clear plastic substrates prior to this work has been limited to 150°C [6][7]. More detail regarding the optical and thermal properties of the new clear plastic substrate and the implication of these properties in the development of a high-temperature plastic-compatible *a*-Si:H TFT process is available in [8].

4.2 *Pixel Circuit*

The circuit schematic of a 2-TFT AMOLED pixel and the driving signals are illustrated in Fig. 4.1. The pixel is composed of a switching TFT, a driver TFT, an OLED, a select line, a data line, a power supply line and a storage capacitor. When the select voltage

(V_{select}) is high, the data voltage (V_{data}) is transferred through the switching TFT to the gate of the driver TFT, determining the pixel current and thus brightness. The storage capacitance is used to maintain the voltage of the storage node (the gate voltage of the driver TFT) until the next time the pixel is refreshed (i.e. during the frame time). The addressing scheme with a frame time of 16 msec and 256 rows (resulting in a row time of 62.5 μsec) is referred to as "quarter video graphics array" (QVGA) timing.

The 2-TFT pixel is the simplest AMOLED pixel structure in terms of having the smallest number of TFTs, capacitors and control signals. AMOLED pixel structures with more circuit elements and control signals have been proposed to improve the reliability of light emission by compensating for the drift of the *a*-Si:H TFT and/or OLED characteristics over time [9][10]. However, increasing the number of circuit elements reduces the process yield and limits the light-emitting area of the pixel (the percentage of the light-emitting area of a pixel is typically referred to as "fill-factor" or "aperture ratio"), as *a*-Si:H TFTs and capacitors both occupy considerable areas on the pixel. This limits both the resolution (the number of pixels per unit area, typically stated in the units of pixel per inch or "ppi") and lifetime of the display. The lifetime of the display is reduced by reducing the aperture ratio because a higher OLED current density would be required to achieve a desired pixel brightness (OLED brightness reduced by the ratio of the OLED area to the total pixel area). A larger number of control signal lines also reduces the aperture ratio but more importantly increases the complexity and therefore the cost of the control circuitry. Therefore, we believe the practical path to realizing commercially viable AMOLED displays is choosing a simple 2-TFT pixel structure and improving the stability of the individual TFTs and OLEDs. In this thesis we will mainly focus on improving the stability of the *a*-Si:H TFTs (Chapter 5). Highly stable OLEDs are provided by an industrial collaborator (Universal Display Corporation).

Pixel design – The ideal pixel operation during the frame time can be explained by the following equations

$$V_{data} = V_{GS,\,driver} + V_{OLED} \tag{4. 1}$$

$$I_{pixel} = I_{OLED} = I_{TFT,\,driver} = \frac{1}{2}\mu_{FE} C_{SiNx} \left(\frac{W}{L}\right)_{driver} (V_{GS,\,driver} - V_{T,\,driver})^2 \tag{4. 2}$$

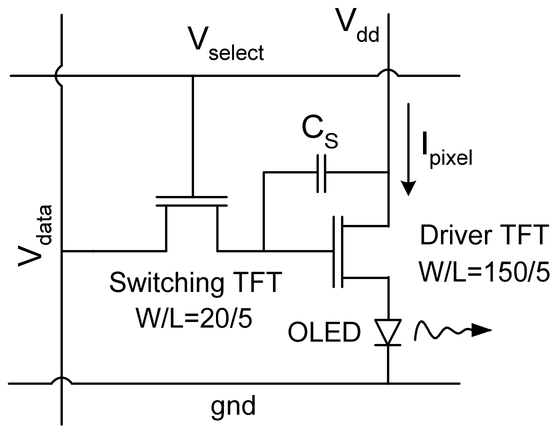

Fig. 4.1. Circuit schematic of the 2-TFT AMOLED pixel used in this work.

where μ_{FE} is the effective field-effect mobility of the electrons, C_{SiNx} the gate dielectric capacitance, W/L the channel width to length ratio, V_T the threshold voltage and the subscript "*driver*" refers to the driver TFT (see Section 3.2 for a description of the *a*-Si:H TFT equation). The power supply voltage (V_{dd}) is chosen high enough to ensure the driver TFT is operated in the saturation regime ($V_{dd} > V_{GS,\,driver} - V_{T,\,driver}$).

For a pixel size of 500µm×500µm and an OLED efficiency of 57Cd/A, a pixel brightness of 1000Cd/m^2 requires a pixel current of 4.7µA. With a mobility of 0.63cm^2/Vs and a threshold voltage of 2.1V, and choosing a W/L ratio of 150µm/5µm for the driver TFT, a gate-source voltage of 7.5V is required on the driver TFT to provide this current. Note that a fractional reduction in the current in the driver TFT of 0.1% corresponds to about a 3mV drop of the gate-source ($\Delta I_{TFT} / I_{TFT} = [1 - \Delta V_{GS} / (V_{GS} - V_T)]^2$). For an off-current of $I_{off} \approx$ 1pA for the switch TFT, a storage capacitance of $C_{st} \approx 4.8$ pF is required to assure such a small voltage drop over a frame time of t_{frame} = 16 msec (note $I_{off} = C_{st} \times \Delta V_{GS} / t_{frame}$). A V_{dd} of 20V was used to assure the driver TFT is biased in saturation.

Design Layout – The layouts of the 2-TFT pixels designed with two different alignment tolerances (10µm and 20µm) are shown in Fig. 4. 2 (a) and (b), respectively. The purpose of the alignment tolerance is to allow overlay registration when the substrate dimension changes from one mask step to the other. It can be readily observed that increasing the alignment tolerance considerably reduces the pixel aperture ratio. The

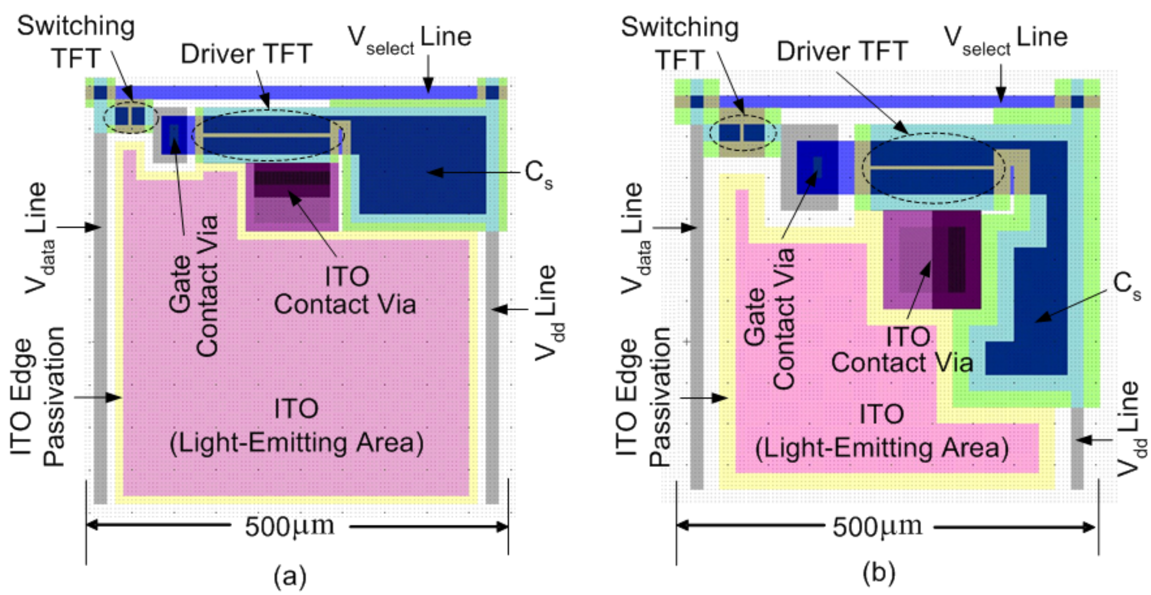

Fig. 4.2. Design layout of the 2-TFT AMOLED pixels used in this work with (a) 10 μm and (b) 20 μm alignment tolerance.

experimental results (Section 4.4) show that an alignment tolerance of 10μm is more than sufficient for active substrate area (the area with *a*-Si:H TFT backplanes) of 2 inch ×2 inch. For large array sizes, however, the issue of the substrate dimensional change and overlay registration needs to be addressed. A practical solution is using a self-aligned *a*-Si:H TFT process which has been developed by our group [8][11].

4.3 *Fabrication Process*

The cross-section of the AMOLED pixel structure is given in Fig. 4.3. The fabrication process starts by coating both sides of the clear plastic substrate with 200nm-thick nitride buffer layers grown by plasma-enhanced chemical vapor deposition (PECVD) for protection against the chemicals during the fabrication process. The bottom metal (Cr/Al based) is then evaporated thermally and patterned by wet-etching. Next a 300nm/200nm/30nm TFT stack of *a*-SiN_x:H / *a*-Si:H (undoped) / n^+ *a*-Si:H (gate dielectric / channel / drain and source contacts) is deposited by PECVD. For comparison, AMOLED arrays were fabricated at three different gate nitride deposition temperatures of 285°C, 250°C and 200°C. The gate nitride deposition temperature is the highest temperature used in processing and we refer to it as the process temperature. The *a*-Si:H