TOWARDS FLEXIBLE FULL-COLOR ACTIVE MATRIX ORGANIC LIGHT-EMITTING DISPLAYS: DRY DYE PRINTING FOR OLED INTEGRATION AND 280°C AMORPHOUS-SILICON THIN-FILM TRANSISTORS ON CLEAR PLASTIC SUBSTRATES

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ABSTRACT

The goal of this thesis is to achieve flexible full color AMOLED displays on clear plastic substrates using high temperature amorphous-silicon TFT's. Dry dye-printing and solvent-enhanced dye diffusion were used to fabricate side-by-side red, green and blue organic light emitting device (OLED) pixels. The technique was then used to make combined polymer/small molecule devices, in which the printability of polymer for color integration was combined with the superior transport properties and thin layer capabilities of small molecules for high efficiency and low leakage current. A three-color passive-matrix test array with 300μm x 1mm RGB subpixels was demonstrated with this structure.

The mechanical interaction of the TFT stack and the plastic substrate is modeled to develop design guidelines to avoid cracking due to the thermal expansion mismatch between the plastic substrate and the TFT films. The guidelines are then used to successfully fabricate a-Si TFT's on novel clear plastic substrates at a maximum process temperature of up to 280°C. The TFT's made at high temperatures have higher mobility and lower leakage current, and higher stability compared to TFT's made on conventional low-T_g clear plastic substrates. Active matrix pixel circuits for organic LEDs on both glass and clear plastic substrates were fabricated with these TFT's. The leakage current in the switching TFT is low enough to allow data storage for video graphics array (VGA) timings. The pixels provide suitable drive current for bright displays at a modest drive voltage. A small AMOLED array was successfully demonstrated with very high brightness (1500 nits) at a relatively low data voltage of 15V with only ~9V of this across the TFT itself. These results show that amorphous silicon TFT's on clear plastic are an attractive route to AMOLED displays on clear flexible plastic substrates.

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CONTENTS

CHAPTER 1

INTRODUCTION

1.1 Motivation

There is a growing interest in flexible electronics because products based on this technology will be light-weight, unbreakable, rollable, foldable, and flexible, for many new generation large-area electronic products. Applications include artificial sensor skin, rugged sensor arrays, wearable electronic-textiles, and flexible displays. Research on flexible displays is now very active both in industry and in academia. It is driven by the need for foldable display screens for computers and cell phones, electronic books, newspapers and maps, display wallpaper and wearable displays, etc. Basic prerequisites for flexible displays include a flexible transistor backplane and a flexible display front plane. The backplane provides power and electrical control signals to the front plane. It consists of thin-film transistors (TFT's) fabricated on flexible substrates.

The flexible electronics products closest to reality are organic light-emitting displays (OLED's). They have many potential advantages over the current dominant liquid-crystal displays (LCD's), such as self-emission, video response, wide viewing angle, very thin form factor, and the compatibility with flexible plastic substrates to enable flexible displays. They can be made with organic "small molecules" or with polymers. Commercial display products based on polymer OLED's have been in the market for several years on rigid glass substrates. Polymers are attractive emission materials for OLED displays because they can be deposited by low-cost and high-throughput methods such as spin-coating. However, spin-coating creates blanket layers which can generally emit only one color. For efficient full-color displays, pixels emitting red, green and blue (RGB) colors should be fabricated side by side on the same substrate with high resolution. Therefore patterning the polymer layer to achieve RGB colors is an important problem.

Research for this thesis addressed two issues:

- Integration of three-color OLED's using a dry-printing process;
- Fabrication of amorphous-silicon (a-Si) TFT's on clear plastic substrates for flexible backplanes.

1.2 Organic Light-Emitting Devices

In 1987, C. W. Tang and S. A. VanSlyke fabricated an organic light-emitting device with promising characteristics based on small molecules [1]. Since then, the field of organic electronics has attracted a tremendous amount of attention both from industry and

academia. In 1990, Burroughes et al. fabricated devices based on the polymer poly(p-phenylene vinylene) (PPV), which is still one of the most often used polymers [2]. Devices based on polymers now have efficiencies in excess of 20 lm/W and lifetimes of more than 10,000 hours at 200 cd/m^2 have been reported [3][4].

The device structure of an OLED is surprisingly simple: sandwiched between two electrodes is a thin film of organic material (Fig. 1-1). If an electric field is applied across the electrodes, electrons and holes are injected into states of the lowest unoccupied molecular orbital (LUMO) and the highest occupied molecular orbital (HOMO), respectively. Light emission from the organic material occurs when a molecule relaxes from the excited state to the ground state and emits a photon.

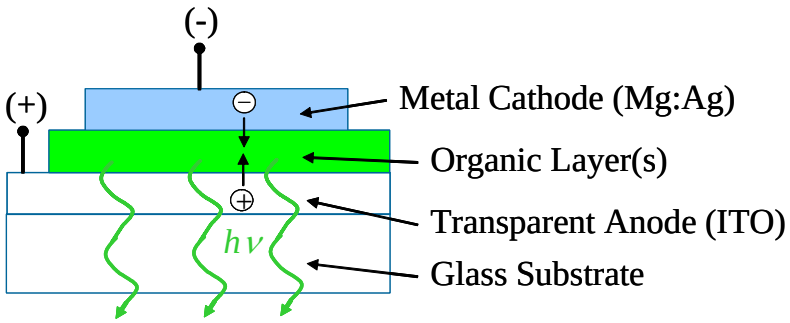

Figure 1-1. Schematic cross-section of an OLED

Commonly used as the transparent and hole injecting electrode (anode) is indium-tin-oxide (ITO). The material is transparent, conductive and has a reasonably high work function (4.5 to 5 eV) [5]. When depositing ITO films, In_2O_3 and SnO_2 are usually simultaneously sputtered onto transparent substrates such as glass. Because ITO is non-stoichiometric, the electronic properties depend on the preparation and cleaning process

used. An oxygen plasma treatment can increase the work function by as much as 0.5eV and thus increase the efficiency of the device [6] [7].

The material used as a cathode should have a low work function, like alkali metals, for good electron-injecting properties. However, all of these metals are also more likely to react with either the emissive materials or with the surrounding atmosphere leading to device degradation. The device stability can be enhanced by using alloys containing these metals in a mixture of more stable metals like silver or aluminum. In this thesis, a magnesium and silver mixture of Mg:Ag = 10:1 is used as the cathode metal unless otherwise stated.

Two kinds of polymer-based organic systems for OLED's were used in this work. In the dry-dye printing work described in Chapter 2, poly(9-vinylcarbazole) (PVK) based polymer blends were used. The chemical structure of PVK is shown in Fig. 1-2(a). The PVK we used has a molecular weight of 1,100,000 g/mole. PVK has a high hole mobility but a low electron affinity and is a good hole-transport material. To compensate for the lack of electron-transport in PVK, a small molecule with electron transport properties, 2-(4-biphenylyl)-5-(4-tert-butyl-phenyl)-1,3,4,-oxidiazole (PBD), was added to the polymer solution. The concentration of PBD in PVK for optimum EL efficiency was established to be 29% by weight in the final film [8]. The PVK/PBD blend is doped using dyes with high fluorescence efficiencies to enhance the performance of the device as well as tune the emissive color. We used the blue dye Coumarin 47 (C47, 0.3% by weight, emission peak at 440nm) as the blue emission material, the green dye Coumarin 6 (C6, emission peak at 500nm) and red dye Nile red (NR, emission peak at 590nm) as the green and red emission materials, respectively (Fig. 1-2 (c), (d), (e)). The HOMO and

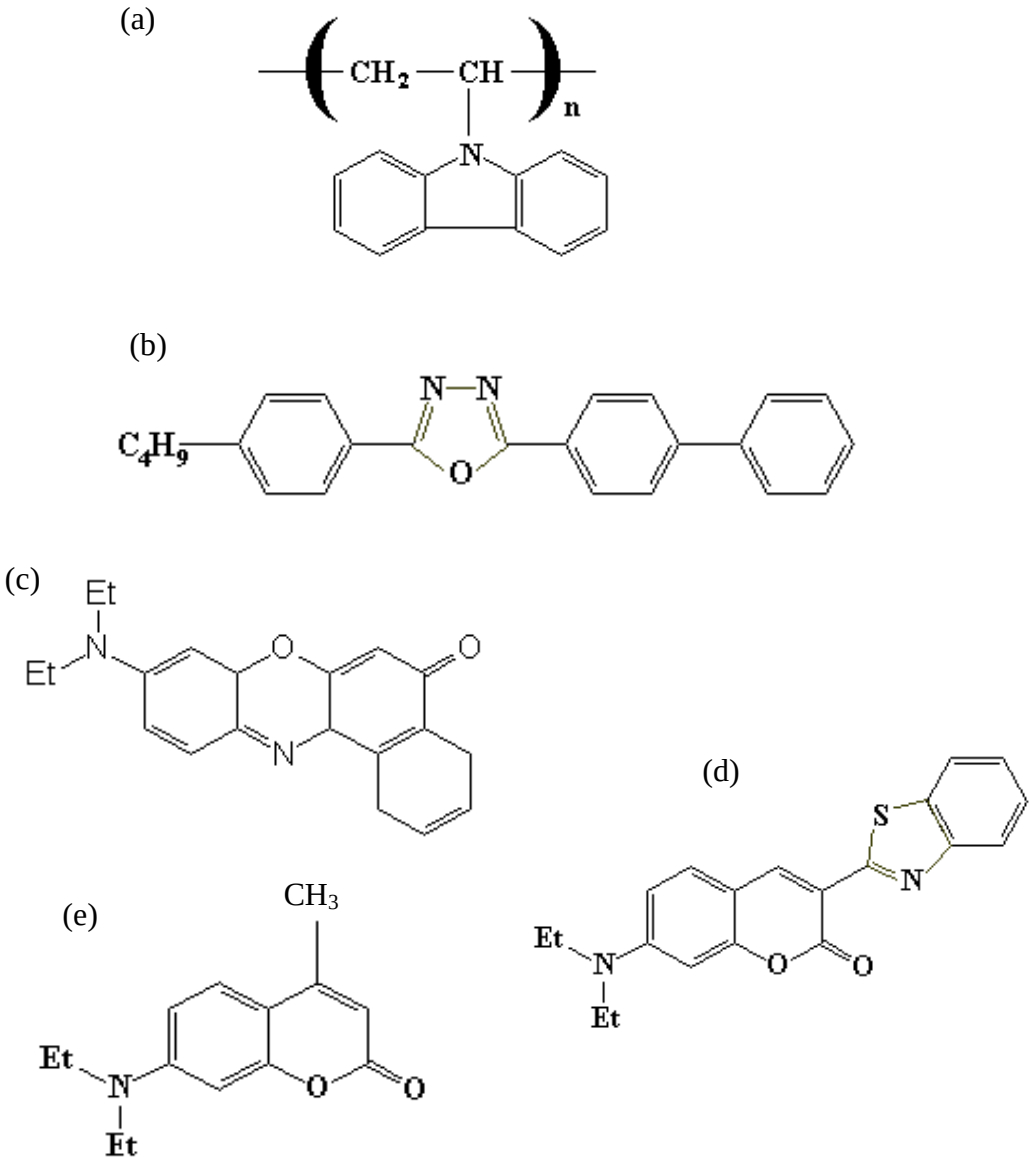

Figure 1-2. Chemical structure of (a) poly(9-vinylcarbazole) (PVK); (b) 2-(4-biphenylyl)-5-(4-tert-butyl-phenyl)-1,3,4,-oxidiazole (PBD); (c) Nile red; (d) Coumarin 6; (e) Coumarin 47.

Table 1-1. HOMO, LUMO levels and wavelength of the peak emission of organic materials used in experiments (described in Chapter 2).

	HOMO (eV)	LUMO (eV)	Peak emission (nm)	Reference
PVK	5.54	2.04	380	[9]
PBD	6.6	2.7	390	[10]
C47	5.37	2.5	420	[9]
C6	5.39	2.9	495	[9]
Nile red	5.3	3.5	600	[9]

LUMO levels (below vacuum level) along with the peak of the emission spectrum of the materials are listed in Table 1-1. The device efficiency depends strongly on the dye concentration [11]. The following weight ratios of PVK:PBD:dye for optimal device performance were established: for C47: 100:40:0.3; for C6: 100:40:0.3; for nile red: 100:40:0.2 [9][12].

For the active matrix OLED test arrays described in Chapter 5, a PPV-based polymer “Super-yellow” was used [13]. The integration of OLED onto the backplane was done at DuPont Displays, in Santa Barbara, CA.

1.3 Flexible Amorphous-Silicon Thin-film Transistor Backplanes

There are many active materials available for transistor backplane applications, such as hydrogenated amorphous silicon (a-Si:H), nanocrystalline silicon (nc-Si:H), polycrystalline silicon (poly-Si), or organics. Among them, a-Si:H is the current

industrial standard, widely used in active matrix liquid crystal displays (AMLCD's) as a pixel switch. a-Si:H can be uniformly deposited using plasma-enhanced chemical vapor deposition (PECVD) over a large area at a relatively low temperature of 300-350°C [14]. In this thesis, our work is focused on a-Si:H thin-film transistors.

One of the advantages of a-Si is that it can be deposited on a wide range of substrates. Table 1-2 lists the substrates being used for a-Si fabrication. Glass is the standard substrate being used in the AMLCD industry. It is transparent with a low coefficient of thermal expansion (CTE) and a relatively high glass transition temperature (T_g), ideal for a-Si TFT fabrication. While thin foils of glass are flexible, they have not been adopted for flexible electronics because they are fragile. Metal and organic polymer (plastic) foils both satisfy the criteria for flexible substrates. Stainless steel foils have high dimensional stability compared to plastic foils and tolerates process temperature over 1000°C, so the standard a-Si process on glass substrate can be used on stainless

Table 1-2. Existing thin-film transistor substrate choices.

Substrate	color	CTE (10^{-6}/ °C)	T_g (°C)	$T_{process}$(°C)	comment
glass	clear	2.1	650	300-360	Industry standard, not flexible
Stainless steel foil[14]	opaque	18-20	>1000	350	Top emitting /reflecting displays
Kapton® Polyimide[15]	orange	16.7	360	150-250	Most common plastic substrate
poly(ethylenenaphthalate)(PEN)[16]	clear	17-20	120	130	Poor TFT properties
Clear Polyimide[19]	clear	?	high	250	Very thin (20μm), not free standing
New clear plastic (DuPont proprietary)	clear	10-50	320	280	Our work

steel foil for optimal device performances [15]. Kapton® polyimide foil produced by DuPont Company is a widely used flexible substrate. It has a T_g of about 350°C and a relatively low CTE which allowed TFT fabrication at process temperatures of 150-250°C [16][18]. But Kapton has an orange-brown color thus is not clear.

The substrates for the TFT backplane must be optically clear for active-matrix liquid-crystal displays (AMLCD's) or conventional bottom-emitting active-matrix organic light-emitting displays (AMOLED's), which require the light to pass through the substrates (Fig. 1-1). So stainless steel foil and Kapton polyimide foil are not suitable for AMLCD or AMOLED applications. Optically clear flexible substrates are desired. A popular clear plastic substrate is poly(ethylene naphthalate) (PEN). It has a T_g of 120°C. a-Si TFT's have been fabricated on it in our lab at a maximum process temperature of 130°C. But TFT's deposited at temperatures below 140°C have low electron mobility, high leakage current, and show pronounced drift due to charge trapping [17]. This is a common problem for a-Si TFT fabrication on clear plastic substrates[18][19], because most clear plastics have glass transition temperature (T_g) of 120°C or less. Some research has been performed with a-Si TFT's fabricated on a clear polyimide foil at 250°C [20]. But the substrate used was very thin (20μm) and was bonded to a rigid carrier, so the plastic itself can not serve as a reliable rugged substrate. In this thesis, new clear plastic substrates with high T_g were used to fabricated a-Si TFT's at high process temperatures (250-280°C) for backplanes to drive AMOLED arrays. This is important because it shows a path for the a-Si TFT industry on glass to migrate their product processes to plastic without having to make major changes in their transistor growth and fabrication processes.

1.4 Overview of the Thesis

Chapter 2 describes low dry dye-printing and solvent-enhanced dye diffusion were used to fabricate side-by-side red, green and blue organic light emitting device (OLED) pixels. The technique was then used to make combined polymer/small molecule devices, in which the printability of polymers for color integration was combined with the superior transport properties and thin layer capabilities of small molecules for high efficiency and low leakage current. The electroluminescence (EL) efficiency of the devices was optimized by varying the dye concentration of the printing plate. A three-color passive-matrix test array with 300μm × 1mm RGB subpixels was demonstrated with this structure.

In Chapter 3, more detailed information on a-Si materials, a-Si TFT device structures, the deposition of a-Si and SiN_x thin films, and the a-Si TFT operation and characterization will be discussed.

In Chapter 4, the mechanical interaction of the TFT stack and the plastic substrate is modeled to develop design guidelines to avoid cracking of the inorganic device stack on plastic substrates. This methodology was then used to successfully fabricate a-Si TFT's on novel clear plastic substrates with a maximum process temperature of up to 280°C. To the best of our knowledge, this is the highest fabrication temperature achieved to date for a-Si TFT's on clear plastic – i.e. our results are the process closest to the current industry standard on glass. The TFT's made at high temperatures have higher

mobility and lower leakage current, and higher stability than TFT's made on conventional low-T_g clear plastic substrates.

Chapter 5 describes the fabrication of active matrix pixel circuits for OLED's on both glass and clear plastic substrates with a-Si TFT's. The pixels provide adequate drive current for bright displays at a modest drive voltage and have the low leakage required for data storage through a display frame time. Test active matrices with integrated polymer LED's on glass showed good pixel uniformity, and were as bright as 1500cd/m^2.

Chapter 6 summarizes the results of this thesis and provides an outlook for future work on realizing full-color active matrix organic light-emitting displays on flexible substrates.

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CHAPTER 2

FULL COLOR ORGANIC LIGHT-EMITTING DIVICES INTEGRATED BY DRY DYE PRINTING

This chapter investigates a dry dye printing approach for integrating red, green and blue polymer LED's. The work in this chapter was done in collaboration with Florian Peschenitzka and Troy Gravis-Abe. Florian Peschenitzka's main contributions were developing the dry-dye printing and solvent-enhanced dye diffusion technique [20][21][23][25]. Troy Gravis-Abe developed model of the solvent-enhanced diffusion [24]. My contributions were using this technique to fabricate a three-color passive matrix array, invented a tri-layer OLED structure to reduce leakage and increase efficiency, and optimizing the printed OLED devices. In this chapter, section 2.1 reviews different approach for full-color OLED integration, section 2.2 introduces the dry dye printing process for large area full-color polymer OLED integration, section 2.3 describes the characteristics and optimization of the printed devices, sections 2.4 and 2.5 are the discussion and summary of this chapter.

2.1 Patterning Techniques for Full-Color OLED Integration

2.1.1 Direct deposition of red, green and blue emitters

The most straightforward approach to obtain emission from red, green and blue subpixels is the direct deposition of material emitting the respective color. The efficiency of this method is optimal because no external filtering is necessary.

Ink-jet printing

Ink-jet printing has been demonstrated to be a viable technology to locally deposit different polymer materials [1]. In this case, a small drop of solution with the proper polymer is deposited onto the substrate. The drying properties of the solution with the

drop are of major concern because an uneven morphology leads to an non-uniform emission pattern and ultimately to early degradation of the device [2][3]. The use of a substrate pre-patterned with “banks” helps confine the solution to form a polymer film with more uniform thickness [4][5] (Fig. 2-1).

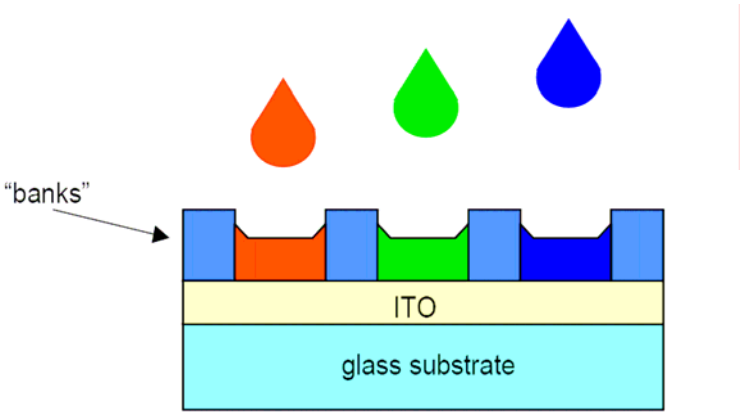


Figure 2-1. Ink-jet printing of red, green and blue polymer droplets onto a pre-patterned substrate with “banks” to form a more uniform polymer film.

Screen printing

Analogous to the conventional screen printing technology used in the printing industry, this method has the potential of low fabrication cost. The polymer solution is applied through a screen (stencil) onto the substrate by squeezing the solution through the openings of the screen [6][7]. For a full-color display, three successive steps have to be carried out. This process bears the risk of mechanically damaging the already deposited polymer features during the following printing steps, resulting in short circuited devices.

Dry etching

Using oxygen plasma to locally etch away the organic layer after deposition has been utilized [8]. After the first deposition of a polymer solution by spin-coating, the

cathode was evaporated at places where devices with the respective emission color were desired (Fig. 2-2(a)). The subsequent dry etching step removed the polymer layer where it was not protected by the cathode metal layer (Fig. 2-2(b)). Then the existing devices were completely encapsulated to avoid damaging by the spinning –on of the second polymer layer (Fig. 2-2(c)). The procedure was repeated until a three-color device was fabricated (Fig. 2-2(d)). This method has the drawback of requiring multiple cathode deposition and patterning steps.

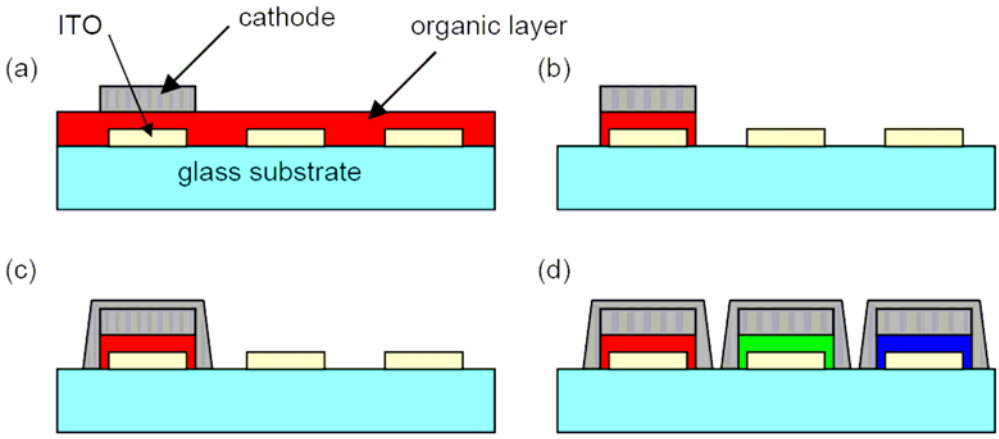


Figure 2-2. Fabrication of three colors by dry etching of organic layers.

2.1.2 Emission of RGB with a uniform emissive material

White OLED and color filters

Conventional liquid crystal displays (LCD) operate by locally blocking white light from a back light with red, green and blue color filters. The back light can be replaced by white-emitting OLED's [9][10] (Fig. 2-3). The advantage of this method is

the use of very reliable color filter technology. However, the efficiency of the device is lower than that of direct emitting devices.

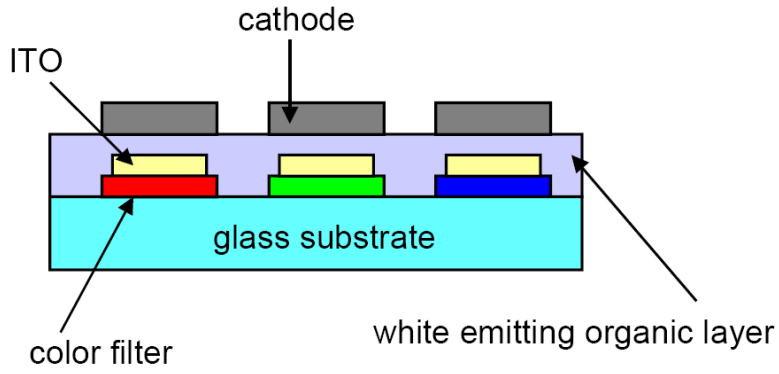


Figure 2-3. Red, green and blue emissions using white-emitting OLED and color filters.

Blue OLED with color conversion

By converting light of a short wavelength to light of a longer wavelength [11], the blue photon can be changed to red and green by color converting materials (CCM) (Fig. 2-4). The blue emission is converted into green and red emission by converting phosphors in front of the emitting subpixels [12][13].

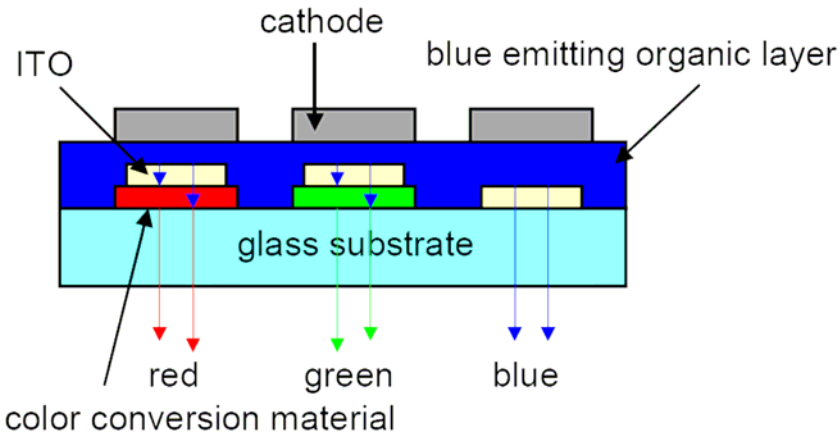


Figure 2-4. RGB emission using blue OLED and color conversion materials.

2.1.3 Direct emission of RGB by local dye doping

The emission colors of polymers can be controlled by adding small amounts of fluorescent dyes into the polymer films (less than 1% by weight) [14][15]. There are several methods to achieve full color based on this principle.

Ink-jet printing of dye solution

To avoid the problem of non-uniformities in film thickness caused by the drying of ink-jet printed droplets of polymer solution, a dye solution is ink-jet printed onto a previously spin-coated polymer film, and diffused into the polymer layer, thereby changing the emissive color of the polymer film (Fig. 2-5). The emission of the dye has to be of longer wavelength than the host material to allow for energy transfer from the host to the dye [16]. However, due to the drying properties of the solvent droplet and mass transport within the droplet, the lateral distribution of the dye still needs to be optimized [17].

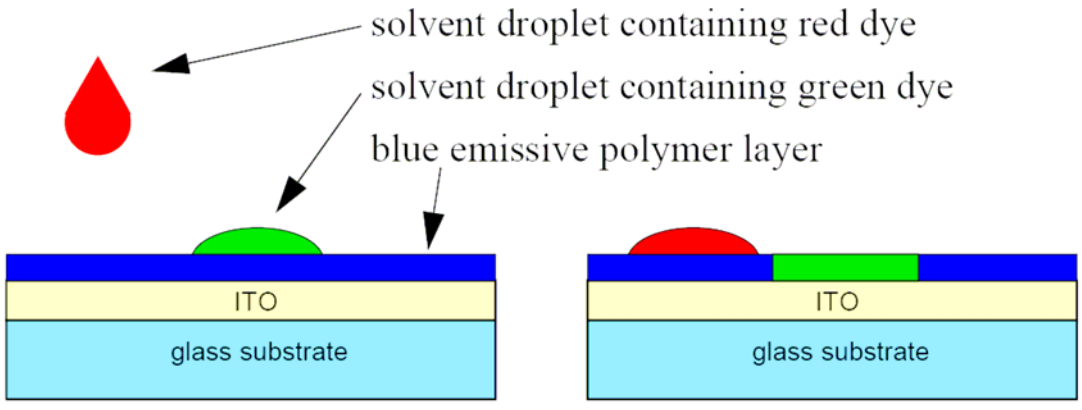


Figure 2-5. Patterning of the emission color by local ink-jet printing of dye solution.

Photobleaching

A photosensitive dye is mixed into the spin-on polymer solution. Then the dye was locally and selectively deactivated by UV radiation using a conventional photo mask to define the pattern. Therefore, the dye emits in its respective color where it was not irradiated with UV, and the emission occurs from the host where the dye has been bleached [18]. So far, the stability of such dyes has been insufficient.

Dye transfer method

This is another method to introduce a small amount of dye into a previously deposited polymer layer. In this case, the dye is locally transferred into the polymer film over a large area and thus changes the emission color of the device. This can be done by patterned dye transfer by local heating [19], thermal transfer through a mask [20], or using a patterned soft printing plate [21].

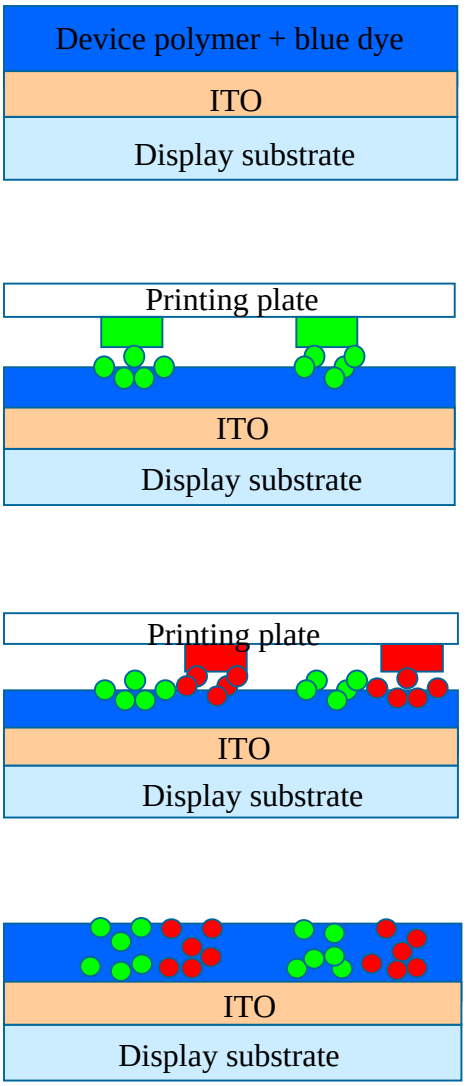
Dry printing is in principle attractive compared to wet printing (such as ink-jet) since issues associated with the lateral redistribution during the solvent drying process can be avoided [1][17][22]. A large-area highly parallel printing process is also attractive from a throughput point of view compared to a serial process such as ink-jet printing. This Chapter described extending the local dye transfer process to pattern polymer films over a large area and demonstrating the operation of a three-color pixel. Both technology problems associated with the dye patterning process (section 2.2) as well as device efficiency and optimization (section 2.3) are addressed.

2.2 Large-Area Dye Printing into Polymers

2.2.1 Process Overview

The solvent-enhanced dry dye-printing method is shown schematically in Fig. 2-6. The OLED device structure consists of a substrate with patterned ITO lines, onto which the polymer is uniformly deposited by spin-coating from a chlorobenzene solution to form a 90-nm thick film. In all of the work in this chapter, the solution contained poly(9-vinylcarbazole) (PVK; M_w ca. 1,100,000 g/mole; 71% by weight in the final film) as the host polymer and the hole transport material, 2-(4-biphenylyl)-5-(4-tert-butyl-phenyl)-1,3,4,-oxidiazole (PBD; 28.7% by weight) as the electron transport molecule and the blue dye Coumarin 47 (C47, 0.3% by weight, emission peak at 440nm) as the blue emission material [15], unless otherwise noted. The chemical structures of these organic materials were shown in Fig. 1-2.

The printing plate consists of a pre-patterned dye source layer on a glass substrate. The dye source layer consist of a polymer matrix of Vylon 103®, to which the green dye Coumarin 6 (C6, emission peak at 500nm) or red dye Nile red (NR, emission peak at 590nm) were added. The fabrication of this printing plate is discussed below. The printing plate was aligned to and brought into contact with the device plate and then annealed in vacuum at 70°C for one hour to transfer the dyes from the dye source onto the surface of the device polymer. This initial dye transfer step was done once for the green dye and once for the red dye. Then the device sample was put into an acetone vapor ambient to diffuse the dyes throughout the thickness of the polymer film. A uniform dye distribution throughout the polymer film was achieved after a treatment in acetone vapor



(a) Uniform spin-coat of device polymer with blue dye

(b) Transfer of green dye from pre-patterned dye source (at 70ºC for 1 hour);

(c) Repeat the transfer step for red dye;

(d) Solvent-enhanced diffusion of dye throughout the polymer film

Figure 2-6. Schematic process flow of dry-dye printing from pre-patterned dye sources and subsequent solvent-enhanced dye diffusion for red, green, and blue patterns. Vertical dimensions are exaggerated vs. lateral dimensions.

for 150 seconds at room temperature, in a nitrogen atmosphere with 130 ml acetone vapor per liter of N_2 gas [21]. The device structure and subsequent processing are discussed in a later section of the chapter (see section 2.3).

2.2.2 Printing plate fabrication

The printing plates (Fig. 2-6) consist of a glass substrate and a dye-doped polymer layer as the dye source. First a uniform dye source layer is formed by spin-coating from a solution containing polymer Vylon 103® (obtained from Toyoba, M_w 20,000-25,000 g/mol; glass transition temperature T_g = 47°C) and the green dye C6 or the red dye NR to be diffused into the device polymer layer. The dye concentration was varied from 2% to 8% by weight in Vylon. Vylon is used because of its low glass transition temperature, allowing dye to diffuse out easily, and its "anti-stick" properties, causing it not to stick to the device polymer during the printing process.

To form the patterned dye source of Fig. 2-6, a conventional spun-on photoresist could not be directly applied to the doped Vylon dye source because the photoresist processing will damage the dye source. Therefore a dry transferable photoresist film RISTON® (obtained from DuPont) is used to pattern the dye source layer. A schematic process flow of the dye source patterning is shown in Fig. 2-8. RISTON is designed to be used as a thick film photoresist on printed circuit boards (PCB). Normally, it is used by first removing a capping layer and then laminating it onto a PCB, followed by photolithography while it is attached to the PCB. In our case, the lithography was done first and the patterned RISTON was transferred. The RISTON was exposed by UV light,

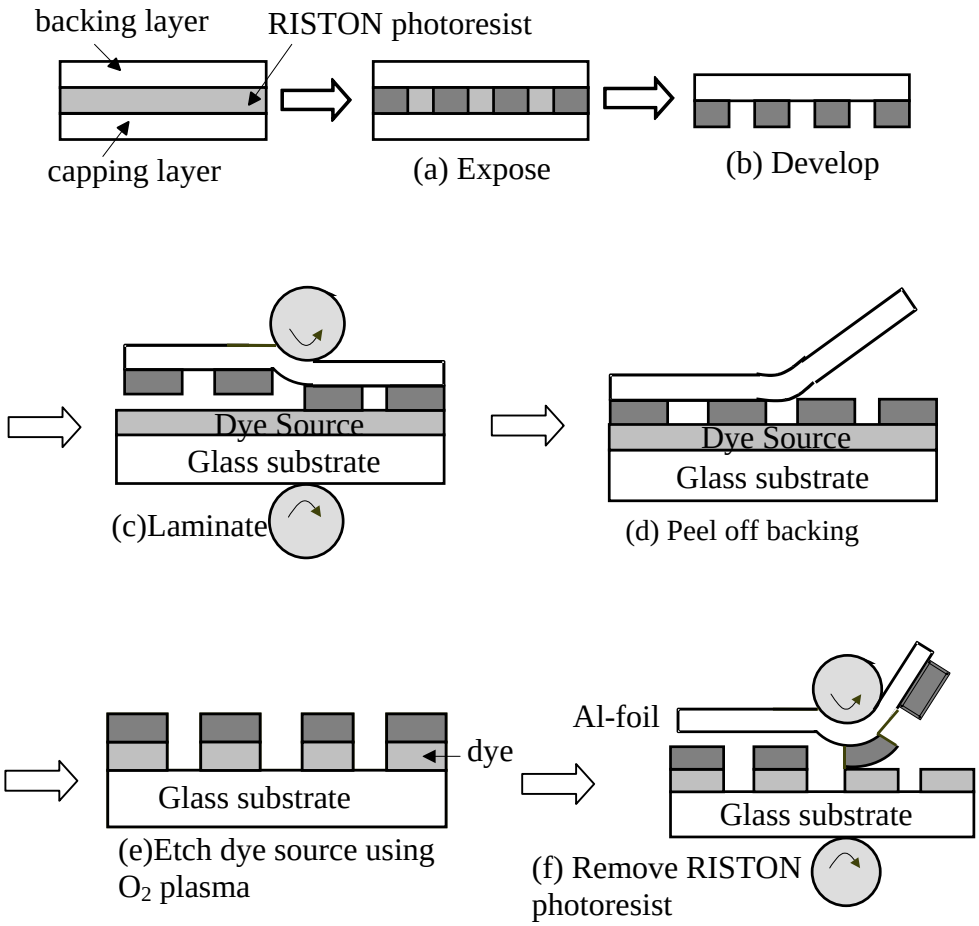


Figure 2-8. Fabrication of the printing plate. (a) pattern RISTON dry photoresist with backing layer remaining as support; (b) laminate patterned RISTON dry photoresist onto the surface of the dye-doped polymer layer (together with backing layer); (c) peel off the backing layer to expose the pattern on the dry photoresist; (d) etch dye-doped polymer using oxygen plasma; (e) remove the dry photoresist by laminating to and peeling off with an aluminum foil. [21]

the capping layer was peeled off, and the resist was developed (Fig. 2-8 (a)). The patterned RISTON was laminated onto the dye source at ~ 120°C, and the backing layer was peeled off to leave a layer of patterned dry photoresist on the dye source plate (Fig. 2-8(b), (c)). Then the dye source layer was dry-etched by oxygen plasma using the patterned RISTON film as the mask (Fig 2-8(d)). Finally an aluminum foil was laminated on top of the RISTON, and then peeled off. Since the RISTON film sticks to aluminum much better than to Vylon, the dry photoresist was peeled off together with the aluminum foil, leaving behind the patterned dye source on the glass substrate (Fig. 2-8(e)).

In a different approach, we also tried using the RISTON film on top of the dye as a local diffusion barrier, with the dye source itself not being etched. However, it was found that the photoluminescence (PL) in the host polymer was quenched where it was in contact with the RISTON at elevated temperature during the dye transfer step. This may be due to a contamination in the RISTON entering the host polymer where the films were in contact. As a result, this route was not further pursued.

2.2.3 Dye Printing and Diffusion

To print the dye onto the OLED device polymer, the dye source plate and the polymer device plate were aligned and brought into contact in a contact mask aligner, with a thin magnetic steel plate under the device plate. The dye plate was used in place of a photo mask. The dye plate was released from the mask holder and secured to the device plate by putting magnets on top of it (Fig. 2-9). The stack of the magnets, the dye

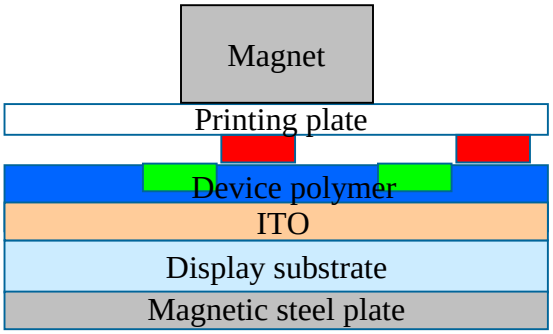


Figure 2-9. Schematic cross section of the aligned magnetic steel plate, device plate, dye source plate and magnet stack ready for putting in the oven for dye transfer. Vertical dimensions are exaggerated over lateral dimensions.

plate, the device plate and the steel plate was then transferred to an oven (70°C in vacuum) for the dye printing. At elevated temperature, dye diffuses from the dye source onto the surface of the device polymer. Since the surface roughness of the dye source and the device polymer is about ±3nm (Fig. 2-10), the two layers are in intimate contact at some points where the dye diffuses directly from one film to another, and in other areas, where there is a gap between the plates, the dye evaporates from the source plate, travels a short distance (maximum 6 nm) in the gas phase and re-deposited onto the surface of the device polymer.

The above printing step left the dye only on the surface of the device polymer, presumably due to the device polymer's high glass transition temperature T_g (~120°C for PVK and PBD mixture) and the low diffusion coefficient of dye in the polymer matrix [23][24]. Then the device plate was put into acetone vapor for annealing, to soften the device polymer to increase the diffusion coefficient [23]. This is because acetone vapor

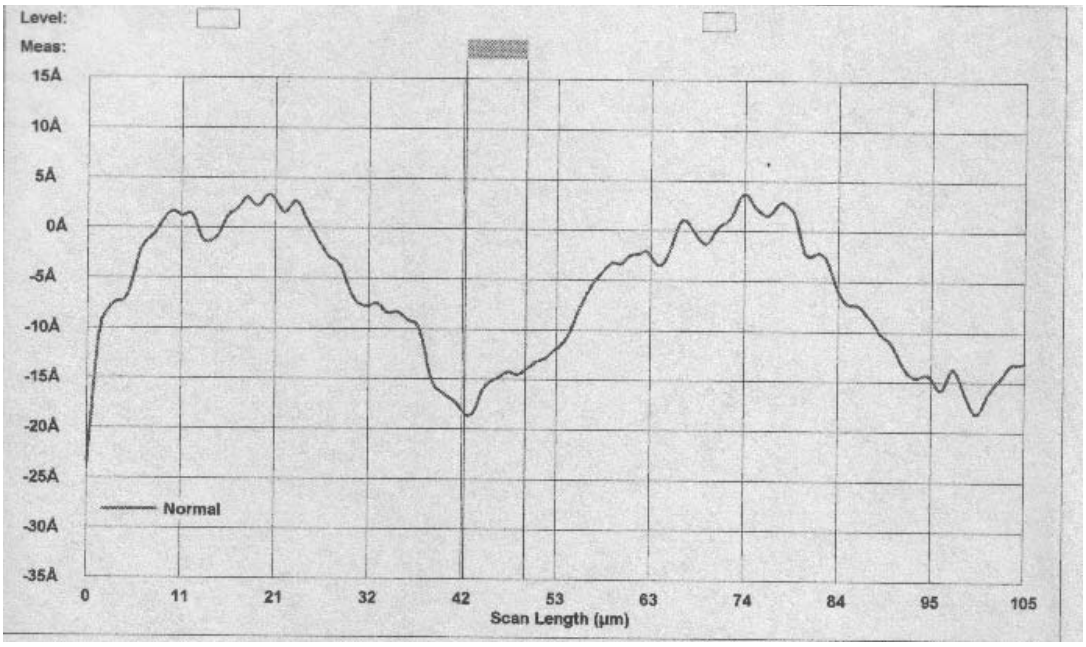


Figure 2-10. Surface profile of the OLED polymer. The peak-to-peak surface roughness is about 3nm.

is absorbed by the polymer and causes it to expand. The glass transition temperature T_g of the polymer is thus greatly reduced, resulting in an increase of the dye diffusion coefficient by many orders of magnitude. The increase is so large that during the acetone vapor "annealing", the dye can diffuse throughout the bulk of the polymer film very quickly even at room temperature.

Fig 2-11 shows the electroluminescence (EL) spectra of the PVK/PBD/C47 (70.1%/28.7% /0.3% by weight) devices with C6 transferred from a dye source of Vylon layer doped with C6 (4% by weight). The insert plot shows the device cross section. C47 is a blue dye with peak emission at 440nm and C6 is a green dye with peak emission at 500nm. For the device made with only the initial printing step (in vacuum at 70°C for 1

hour) only blue emission from C47 present from the initial spin-coated host film was obtained. This is because the printed C6 is accumulated at the surface of the polymer film and is not active in the emission process. Conventional annealing to diffuse C6 into the bulk of the device polymer is not desirable because it is too slow: after four hours at 92°C, the penetration of C6 into the polymer bulk is still clearly limited, with the C6 concentration at a depth of 100nm only 9% of that at the surface [23]. Therefore we chose to employ the solvent-enhanced diffusion process described above. After 60 seconds of acetone-vapor annealing in a nitrogen-acetone ambient (total pressure = 1 atm, acetone partial pressure = 90 torr), the EL emission has shifted predominantly to green, indicating that C6 is moving into the polymer film. However, a small C47 peak is still observed in the EL spectrum, which maybe due to insufficient C6 in the recombination zone of the device. After a 150-sec anneal, the emission is now entirely from C6, the devices are transferred from blue-emitting devices to green-emitting devices by this solvent-enhanced dye diffusion process. Note that when two dyes are present, photoluminescence from both dyes is observed but electroluminescence from only the lower energy dye is obtained. Details of this mechanism can be found in reference [1] and [25]. This is fortuitous because it allows us to put a blue dye in the emissive device film by the initial spin-coating, and then achieve patterned RGB electroluminescence with only two printing steps for green and red dyes. The process of dye printing and the solvent vapor annealing does not measurably change the device film thickness. Although the film can swell in thickness by 20-30% during the solvent vapor treatment, it shrinks back within minutes after the vapor is removed.

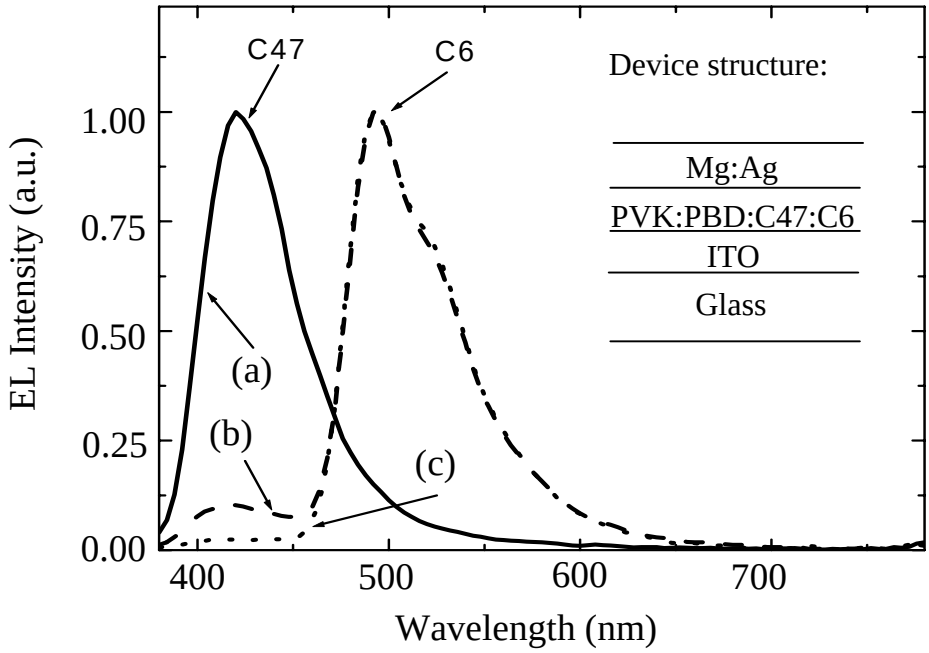


Figure 2-11. Electro-luminescence spectra of PVK/PBD/C47 OLED devices with C6 transferred from a dye source of Vylon layer doped with C6 (4% by weight) (a) with only the initial printing step (at 70°C for 1 hour); (b) after 60 sec of acetone-vapor annealing; and (c) after 150 sec of acetone-vapor annealing at acetone vapor pressure of 92 torr at room temperature. The inset shows the device structure [25].

2.2.4 Large-area patterned three-color polymer film

Fig. 2-12 shows a photoluminescence image of a PVK/PBD/dye polymer film with blue, green and red patterns. The blue dye C47 was spin-coated together with the polymer, and the green and red dyes C6 and NR were introduced by two printing steps followed by a single solvent-enhanced dye diffusion step. Each printing step was done in an oven at 70°C for one hour in vacuum. The solvent-enhanced dye diffusion is done at

room temperature for 150 seconds, in an acetone-nitrogen-mixture with a total pressure of 1atm, acetone partial pressure of 90 torr. 350μm-wide red, green and blue color stripes over a 3.5 cm x 2.5 cm area with excellent color uniformity were achieved. There are ITO stripes underneath the polymer layer along with the color stripes. A full-color passive-matrix display can be made by evaporating cathode stripes perpendicular to the ITO stripes on top of the polymer layer. However, as shown in the next section, the reverse-bias leakage current of these dye-diffused polymer LED's made with a single layer of 90nm PVK/PBD/dye is too high to make devices suitable for passive-matrix application.

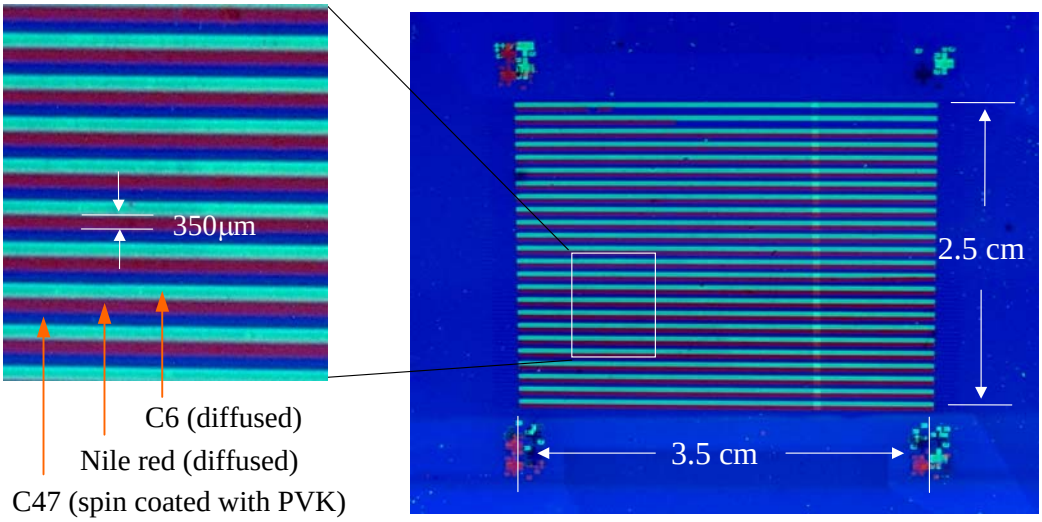


Figure 2-12. Photoluminescence image of a PVK/PBD/dye polymer film with 350μm-wide blue, green and red stripes. The blue dye C47 was spin-coated together with the polymer, and the green and red dyes C6 and NR were introduced by two printing steps and a single solvent-enhanced dye diffusion step [26].

2.3 Device Characteristics and Optimization

2.3.1 Single-layer device I-V characteristic after acetone vapor annealing

Organic LED's were fabricated by evaporating Mg:Ag (10:1)/Ag cathodes through a shadow mask to create large-area test devices (2 mm^2 circles on un-patterned ITO) onto the doped polymer film. Fig. 2-13(a) shows the I-V characteristics of the PVK/PBD/C47 devices with C6 transferred from a uniform dye source of Vylon layer doped with C6 (4% by weight in the final film). The photocurrent produced by a photodiode collecting the light emitted from the OLED is also shown. Based on previous calibration, the external quantum efficiency of the OLED's can be estimated from this photocurrent. A device with only the initial thermal printing step (in vacuum at 70°C for 1 hour) shows a very low photocurrent and thus a low quantum efficiency (0.04%) because the printed dye is accumulated at the surface of the polymer film and is not active in the emission process. After annealing in acetone vapor for 60-sec in a nitrogen-solvent-mixture, the external quantum efficiency increases a bit to 0.06%. After annealing for 240 seconds, the external quantum efficiency improved by nearly an order of magnitude to 0.35%. Secondary ion mass spectroscopy (SIMS) study shows that now the dye is homogeneously distributed throughout the polymer film [23][24]. The homogeneous distribution of the dye throughout the polymer film is similar to the case of the spin-on polymer with dye contained in the solution, which produced the best device efficiency.

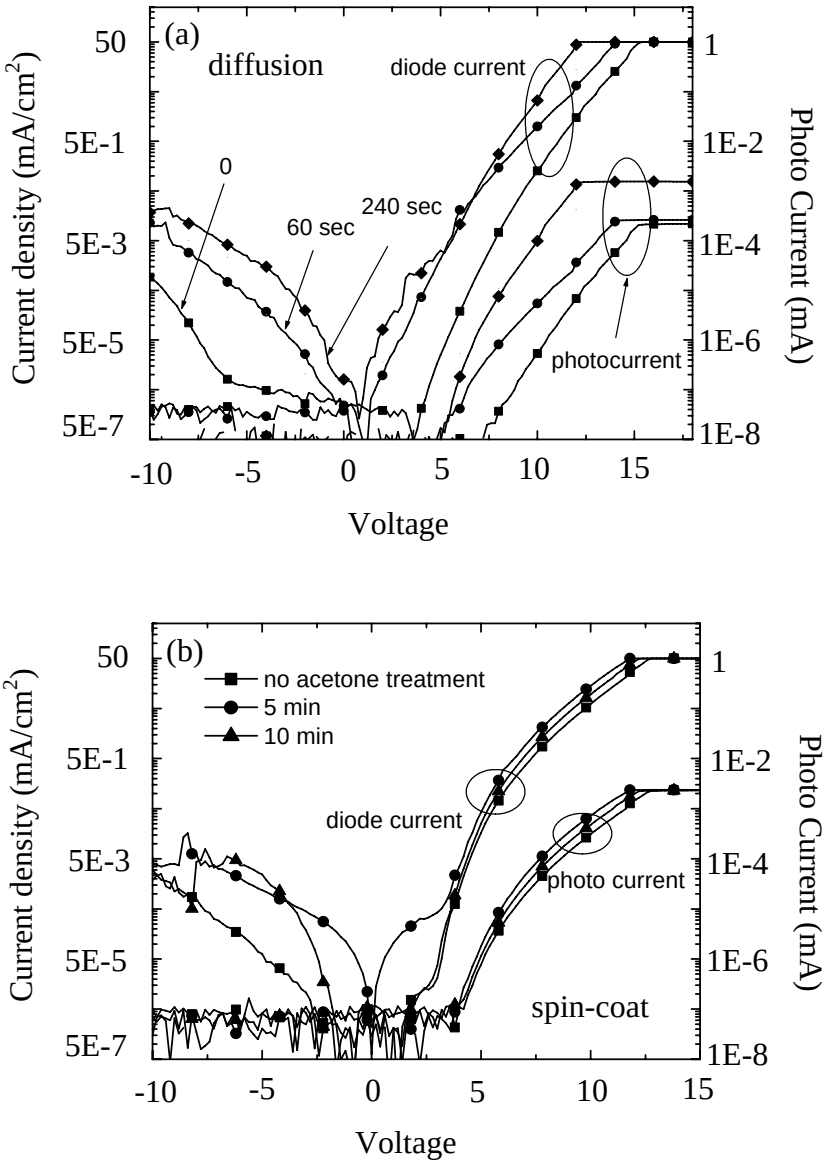


Figure 2-13. I-V characteristics of the PVK/PBD/C6 devices annealed in acetone-vapor (partial pressure 92 torr) for different times: (a) devices with C6 transferred from a uniform dye source of Vylon layer doped with C6 (4% by weight in the final film); and (b) control devices with C6 contained in the spin-on solution and not added by printing. [23]

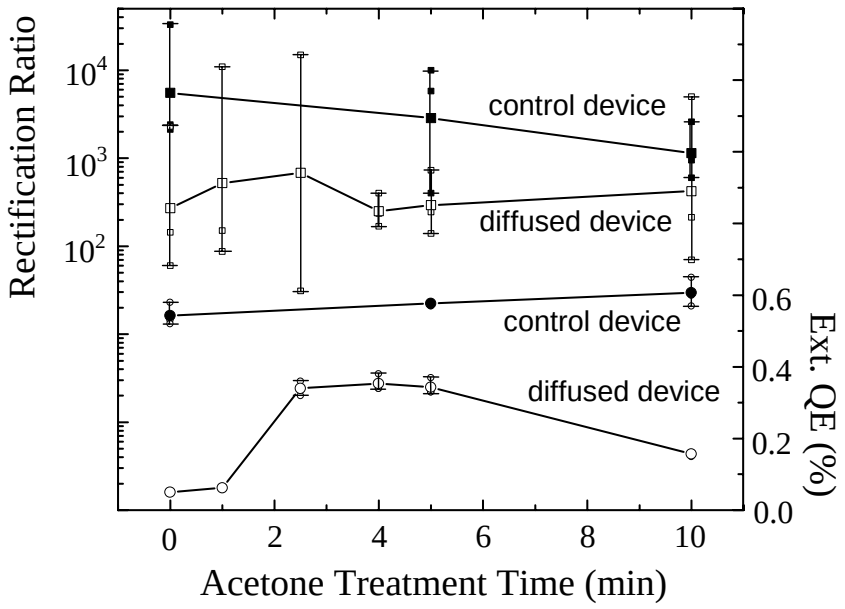


Figure 2-14. External quantum efficiency (circles) and the rectification ratio (squares) as a function of exposure time to acetone-vapor (partial pressure 92 torr at room temperature). Control devices (solid symbols) are devices with C6 in the spun-on solution, and diffusion devices (open symbols) are devices with transferred C6. [23]

The external quantum efficiency of these devices is comparable to those of devices with dye contained in the spin-on solution, instead of printed, as shown in Fig. 2-14.

However, Fig. 2-13(a) also shows that the reverse-bias current of the devices treated with acetone vapor increases drastically with the exposure time to the acetone vapor. This is also true for control devices with dye contained in the spin-on solution instead of printed, as shown in Fig. 2-13(b). The rectification ratio γ, defined as the ratio of the forward-biased current at 10V over the reverse-bias current at –10V, shows this trend in Fig. 2-14. In any case, an increased leakage current is especially harmful for passive-

matrix display applications because of the resulting inability to individually address single devices [27].

2.3.2 Bi-layer devices

To reduce the reverse-biased leakage current of the single-layer doped polymer LED's, an electron transport layer (ETL) was added on top of the polymer layer after the introduction of the dyes into the polymer matrix. Tris-8-hydroxyquinoline aluminum (Alq_3) was chosen for this ETL because it has good electron conductivity and a low highest occupied molecular orbital (HOMO) thus resulting in an increased barrier for hole injection [28]. The band diagram of a single-layer PVK-based OLED under reverse-bias is shown in Fig. 2-15(a). Because the hole injection barrier (1.8eV) is lower than the electron injection barrier (2.5eV) [15][28], the dominant leakage current comes from the

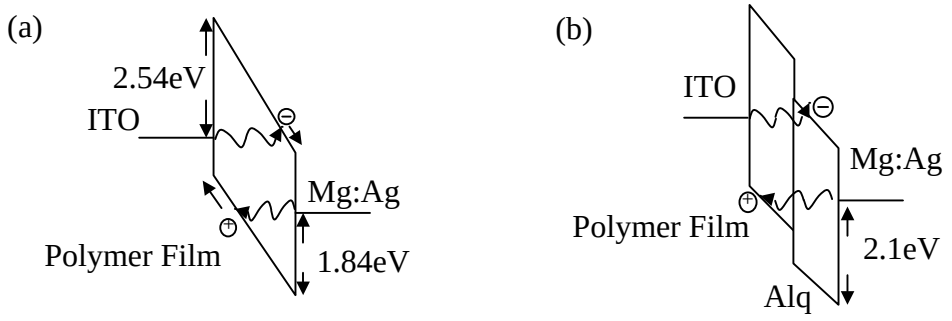


Figure 2-15. Reverse-biased band diagrams of the (a) single-layer (90nm PVK/PBD/Dye) and (b) bi-layer (90nm PVK/PBD/Dye + 40nm Alq_3) OLED's. The diagram shows tunneling. Reduction in current would also be expected for emission over a barrier. [26]

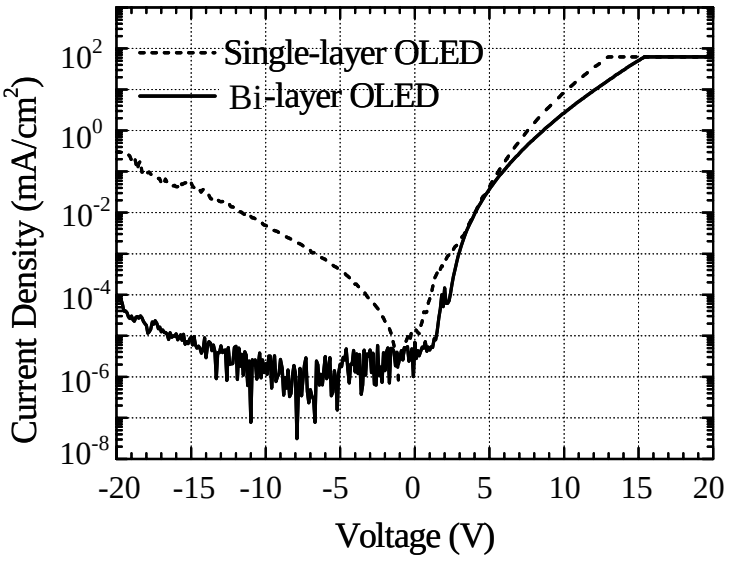


Figure 2-16. Typical I-V characteristics of the single-layer (dashed line) and bi-layer (solid line) devices doped with green dye C6, where the PVK/PBD/C6 layer is made by spin-coating. [29]

hole current. Alq_3 has a HOMO level 0.3eV lower than that of PVK. Adding an Alq_3 layer increases the thickness of the device structure thus decreases the electrical field under the same bias. Therefore adding an Alq_3 layer can suppress hole injection under reverse-bias, and reduce the reverse leakage current (Fig. 2-14(b)). In addition, the Alq_3 layer is expected to increases the efficiency of the OLED devices because it moves the cathode away from the emissive dyes. This reduces cathode-quenching of the excitons via dipole-metal interaction [30], balances electron and hole transport, and raises efficiency.

Bi-layer devices were made by first locally doping the PVK-based film as described earlier. A blanket Alq_3 film was then evaporated on top of the PVK-based layer,

followed by the cathode deposition. Fig. 2-16 shows the typical I-V characteristics of the single-layer and bi-layer devices, doped with C6. The leakage at 20V reverse bias is decreased by almost four orders of magnitude, and the forward current at a given bias increases by a factor of two, which greatly increases the rectification ratio at ± 10V to ~ $1x\ 10^6$.

2.3.3 Hole/exciton blocking layer

While the electrical properties of the bi-layer devices are attractive, the optical emission properties are not. Single-layer devices doped with C47 emit blue light (peak emission at 440nm) (Fig. 2-17(a)). Bi-layer devices doped with C47 in the polymer emit predominantly at 530nm (green) with only a small peak at 440nm (Fig. 2-17(b)). This undesired green peak is thought to be due to emission from the Alq_3. A device made with undoped PVK as a hole transport layer (HTL) and evaporated Alq_3 as an electron transport layer (ETL) and emitting layer emits in this same range (Fig. 2-17 (c)).
The following two processes can cause this undesired green Alq_3 emission in devices in which the PVK is doped with only C47: a) due to the lower energy gap of the Alq_3, excitons formed in the polymer layer will migrate into the Alq_3 layer and recombined there, or, b) holes can be injected from the PVK layer into the Alq_3 layer and form excitons directly in Alq_3. Therefore the dye in the polymer does not control the emission color (Fig. 2-18).

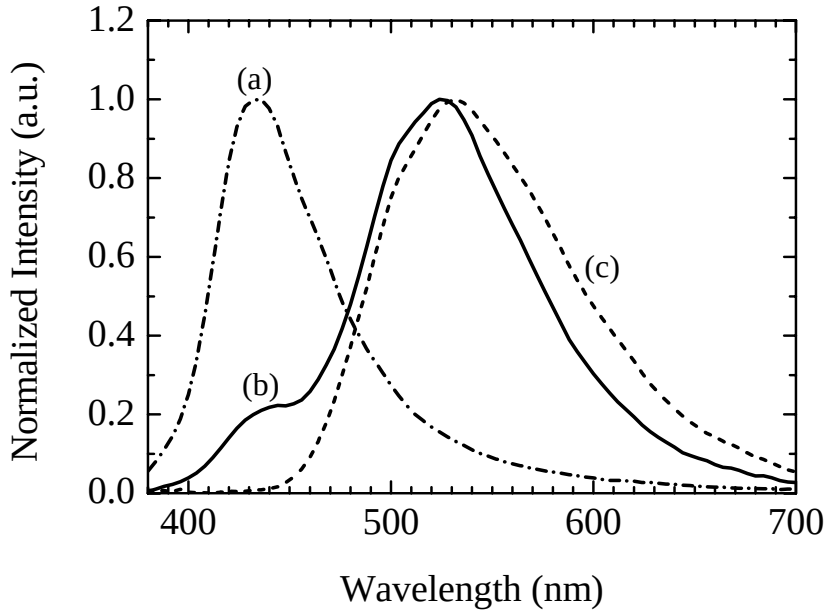


Figure 2-17. Normalized electro-luminescence spectra of (a) single-layer device of 90nm PVK/PBD/C47 (dash-dotted line); (b) bi-layer device of 90nm PVK/PBD/C47 + 40nm Alq_3 (solid line); and (c) Alq3 emission reference (dashed line). [26]

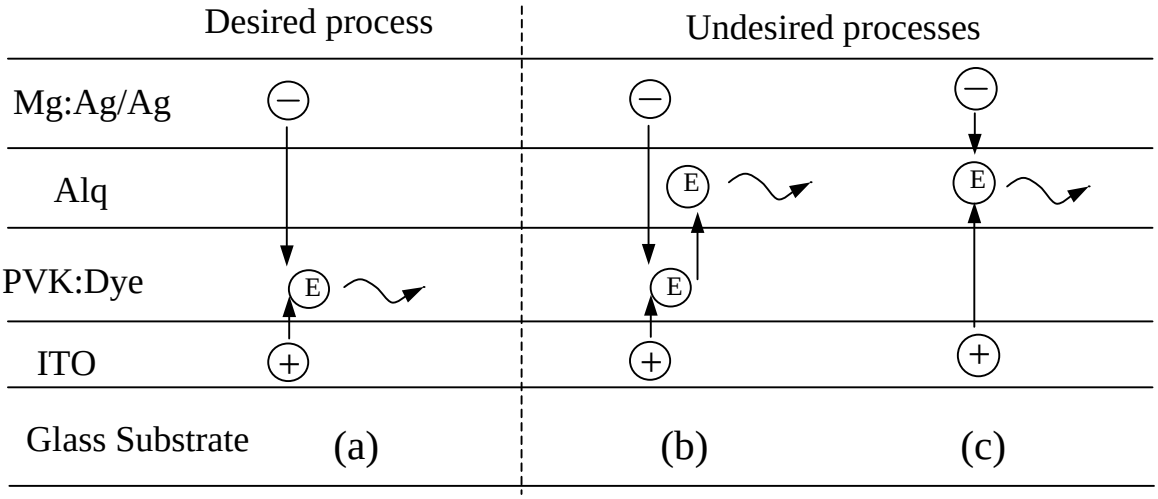


Figure 2-18. Emission processes in a bi-layer device. (a) Excitons formation and emission in PVK; (b) Excitons diffusion to and emit from Alq; (c) Excitons formation and emission in Alq. Motion of the electrons, holes and excitons is shown. [26]

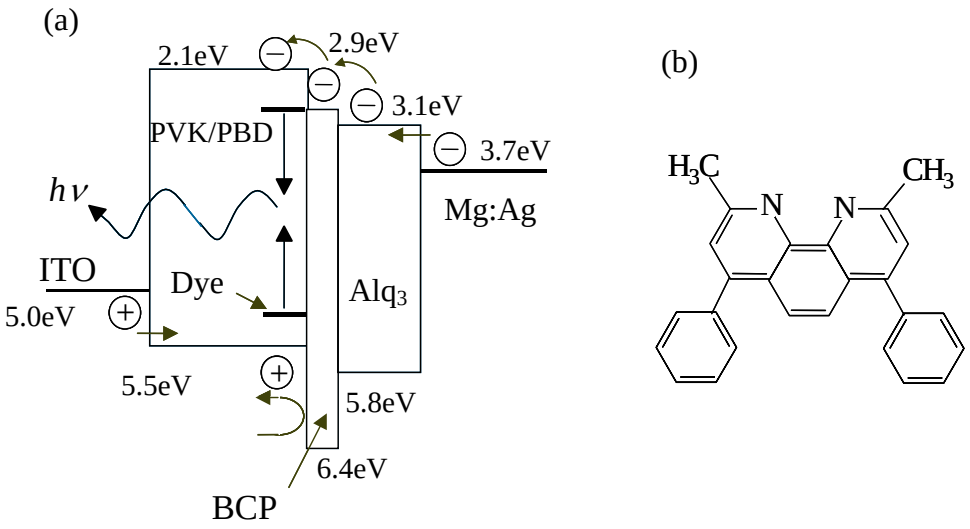


Figure 2-19. (a) Schematic band diagram of the tri-layer OLED structure with PVK:PBD:Dye/BCP/Alq_3. The electric fields are omitted (i.e. the bands are drawn flat) to show more clearly the relative energy levels in the different materials and how the HOMO in the BCP blocks holes from reaching the Alq_3. (b) Chemical structure of 2,9-dimethyl-4,7-diphenyl-1,10-phenanthroline (BCP). [29]

To eliminate the OLED color problem from Alq_3 emission, and to confine the light emission within the dye-doped polymer layer, holes and excitons must be prevented from entering the Alq_3 layer. For this purpose, we placed a thin hole/exciton blocking layer (HBL/EBL) between the doped-polymer layer and the Alq_3 layer. 2,9-dimethyl-4,7-diphenyl-1,10-phenanthroline (BCP) was used for this blocking layer because it satisfies the bandgap requirement for this hole/exciton blocking layer [28][31]. As shown in Fig. 2-19, BCP has a low HOMO to block the holes from entering the Alq_3 layer. The barrier from PVK to BCP is 0.9 eV, vs. only 0.3 eV from PVK directly into Alq_3. Furthermore, the high bandgap of BCP confines the excitons within the polymer layer (3.6 eV in BCP

vs. 2.7 eV in Alq_3). BCP also has a low enough electron barrier to allow electrons to pass through and enter the polymer layer, for the LUMO of BCP (2.9 eV) is between the LUMO of the Alq3 (3.1 eV) and the LUMO of the PBD (2.1 eV) doped in the PVK for electron transport[15][28].

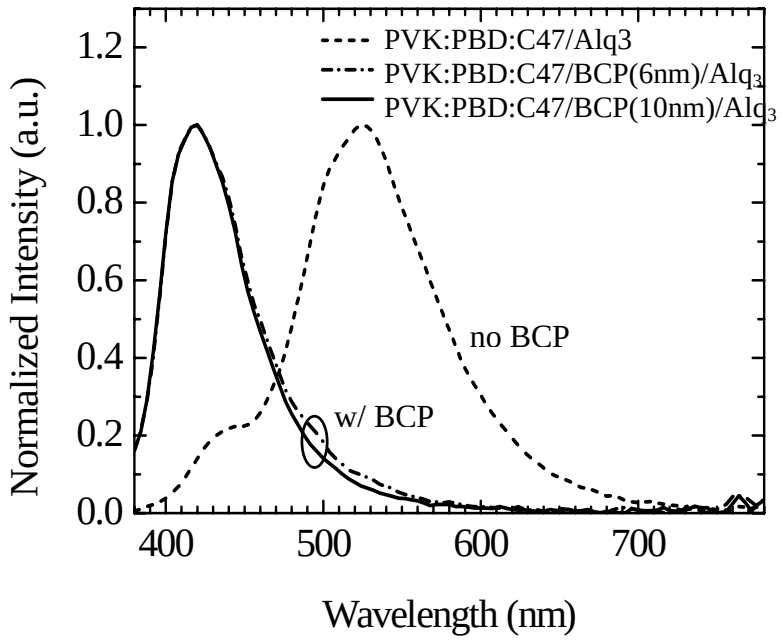


Figure 2-20. Electro-luminescence spectra of the blue dye-doped OLED devices with or without BCP hole/exciton blocking layer. [29]

Fig. 2-20 shows the spectra of the blue dye-doped devices with a BCP hole/exciton blocking layer with different thicknesses. The dominant emission is green without the BCP layer, and with a thin layer of BCP of 6nm or 10nm, the emission is all from the blue dye. No green Alq_3 emission is observed as desired. Furthermore, the addition of this thin blocking layer does not increase the operation voltage of the OLEDs (Fig. 2-21).

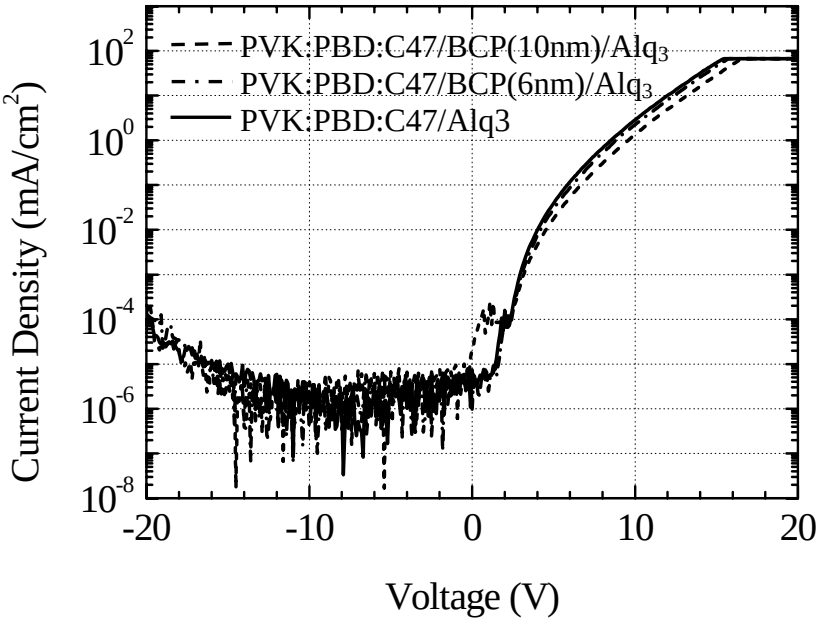


Figure 2-21. I-V characteristics of the blue dye-doped OLED devices with or without BCP hole/exciton blocking layer. [26]

Individual red, green and blue polymer LED's have been fabricated with this tri-layer structure. The devices begin with a 90-nm thick polymer blend layer of PVK/PBD and a fluorescent dye (Nile red for red devices, Coumarin 6 for green devices, Coumarin 47 for blue devices), which is deposited on top of the ITO layer by spin coating. The typical dye concentration was 0.3% by weight. Then a thin (6-nm) BCP layer as a hole/exciton blocking layer and a 40-nm thick Alq_3 layer as an electron transport layer are deposited sequentially by thermal evaporation. A 150-nm thick Mg:Ag (10:1)/Ag layer is deposited as the OLED cathode. Fig. 2-22 shows the electro-luminescence spectra of the fabricated blue, green, and red tri-layer devices, with peak wavelengths of

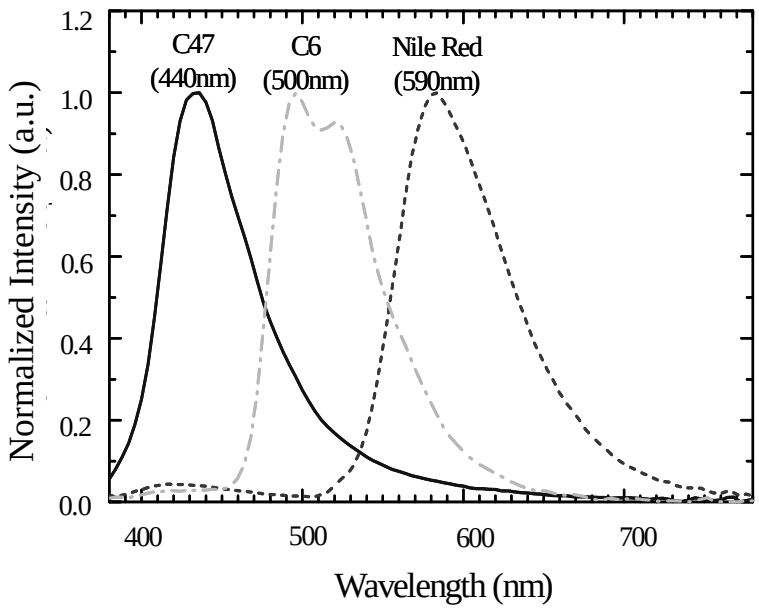


Figure 2-22. Electro-luminescence spectra of the red, green and blue tri-layer devices with a structure of PVK:PBD:dye (90nm)/BCP (6nm)/Alq_3 (40nm), with peak wavelength of 590nm, 500nm, 440nm, respectively. [29]

Table 2-1. Comparison of the EL efficiencies and the current rectification ratio at +/- 10V of the single-layer and tri-layer devices with red, green and blue dye dopants, respectively. [29]

		Blue (C47)	Green (C6)	Red (Nile red)
η_{ext} (%)	Single-layer Tri-layer	0.13% 0.34%	0.70% 1.1%	0.61% 0.95%
Rectification ratio @ ±10V	Single-layer Tri-layer	1.5e4 2.4e6	1.3e3 1.3e6	7.4e3 8.7e5

440 nm, 500 nm and 590 nm, respectively. Compared with the devices without the BCP layer in Figure 2-20, the peaks of the red, green, blue devices are well-defined and do not show the contamination of color from the Alq_3 emission. These tri-layer devices have very high rectification ratio (> 10^6 for green devices) and a higher external quantum efficiency than the single-layer devices (1.1% vs. 0.7% for green devices) (Table 2-1).

2.3.4 Optimization of device efficiency

It was initially observed that devices made from printing plates with 2% dye in spin-coated Vylon, which had been patterned, had lower quantum efficiencies than devices made from a printing plate with the same amount of 2% dye in Vylon, which was not patterned (0.22% vs. 0.51%, Fig. 2-24). This was found to be due to the loss of a large amount of dye (presumably by diffusion) from the Vylon to the RISTON during the lamination of the patterned RISTON to the dye source plate (Fig. 2-8(c)). For adhesion the lamination was done at ~120°C for ~5min. This step depleted the dye source, so less dye was available for subsequent transfer to devices. Secondary ion mass spectroscopy (SIMS) of the green dye C6 doped Vylon films show that about 70% of dye in the dye source plate was lost due to the patterning process (Fig. 2-23).

The OLED electro-luminescence efficiency is strongly dependent on the dye concentration in the polymer film [32]. The EL efficiency increases with dye concentration initially because more excitons can be formed on the dye due to an increased number of dye molecules. But at a certain dye concentration, the OLED EL efficiency reaches its peak. An excess dye concentration leads to dye quenching and thus a lower EL

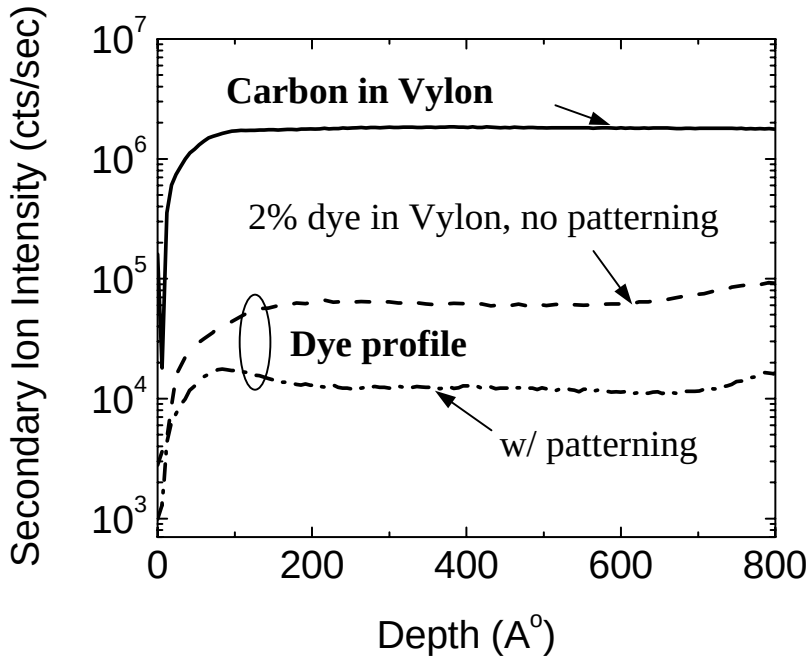


Figure 2-23. SIMS profiles before and after patterning of the green dye C6 doped Vylon films. [29]

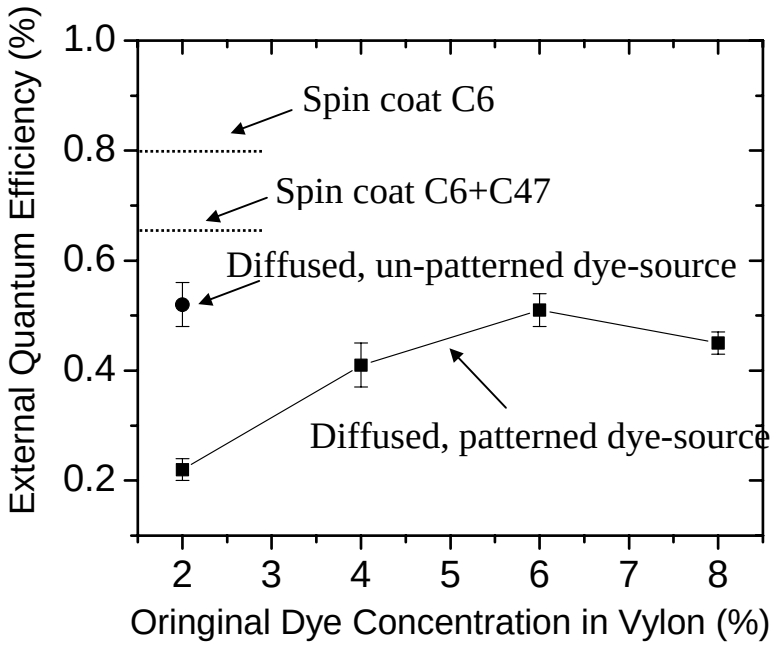


Figure 2-24. EL quantum efficiencies of green devices fabricated with different dye doping methods. [29]

efficiency [25]. In the tri-layer devices, 0.3% dye in PVK by weight yielded the highest EL external quantum efficiency of the devices, which was 1.1% for green devices. To achieve this optimum final device concentration, we determined experimentally the optimum dye source concentration in the un-patterned spin-coated printing stamp to be 2% dye in Vylon by weight for dye transfer at 70°C for 60 min.

Since there is dye loss due to the patterning process, the initial dye concentration in Vylon needed to be increased when making a patterned printing plate. We then made diffused C6 devices with patterned dye sources from 2%, 4%, 6%, and 8% initial dye in Vylon, and measured the EL external quantum efficiencies of these devices (with tri-layer structures as in Fig. 2-19). The devices made using dye source with 6% initial C6 in Vylon yielded the highest EL efficiency (0.51%), which is the same as that of devices made using unpatterned dye source with the optimum 2% C6 in Vylon (Fig. 2-24).

2.3.5 Full-color passive matrix test array

Using the steps of this dye-printing, solvent-enhanced diffusion, and the tri-layer device structure, a full-color passive-matrix test array was fabricated with integrated red, green and blue emitting devices. First ITO was patterned by wet etching into 320μm-wide stripes for column electrodes. A blue-doped (C47) PVK layer was spin-coated, followed by C6 (green) and Nile red (red) dry printing and a solvent assisted diffusion step. The red, green and blue color stripes were aligned with the ITO stripes. Then a thin 6-nm BCP layer and a 40-nm-thick Alq_3 layer were deposited by thermal evaporation on

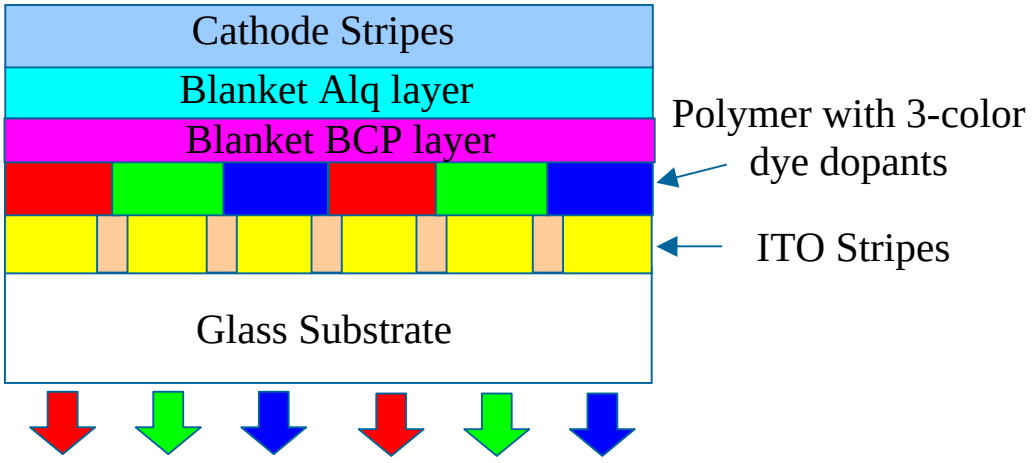


Figure 2-25. Schematic cross-section of the full-color passive-matrix OLED test array.

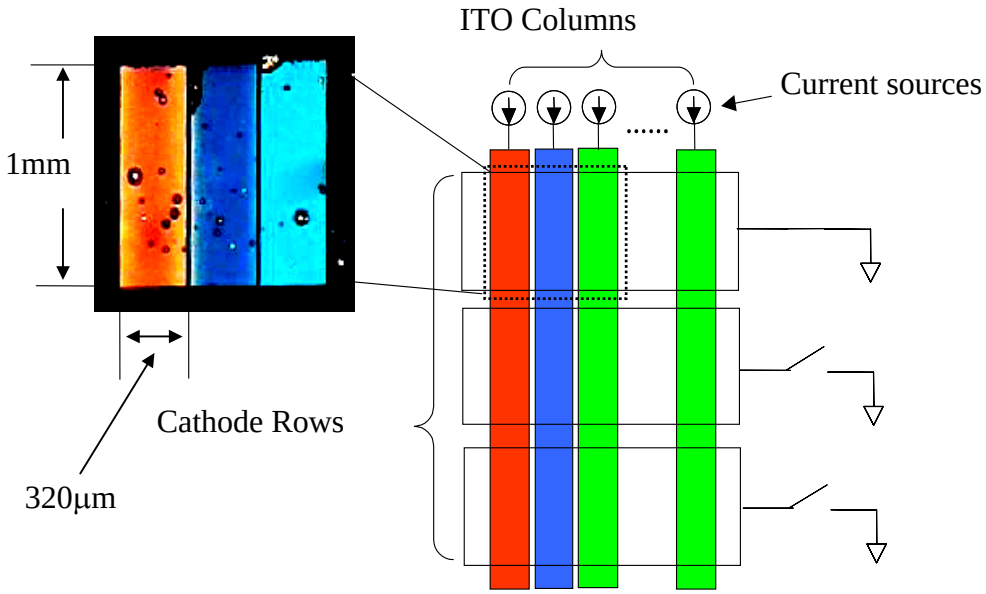


Figure 2-26. Electro-luminescence micrograph of a RGB pixel from a small passive matrix test array fabricated using dry-dye printing and tri-layer structure. [26]

top of the dye-doped PVK layer. Finally a 150-nm thick Mg:Ag (10:1)/Ag layer was deposited as the OLED cathode, with a shadow mask to pattern the cathode into stripes perpendicular to the ITO stripes as row electrodes (Figure 2-25). A 3-row by 15-column three-color passive-matrix test array was fabricated with 100% pixel yield. Fig. 2-26 shows a schematic diagram of the test array and an optical micrograph of one pixel. Although the cathode contains dark spot defects, the color of each sub-pixel is well-defined, and the brightness of the individual pixels could be well controlled.

Appendix 2 documents the passive matrix test system I designed and constructed for providing programmable row and column voltages for up to 72 row and 72 column display.

2.4 Discussion

Our final device structure is unusual for a patterned device. It is not uncommon to find a small molecule ETL on top of polymer HTL [33][34]. However, in our case, it is the hole transport layer that is patterned as the color emitter, and the electron transport layer is uniform. This is the opposite of the usual approach in three-color structures based on small molecules [14]. Our structure results from the fact that for several reasons printing steps are more amenable to polymers than small molecules, and that the polymer layer was deposited before the small molecules because of concerns that the polymer processing and printing would damage underlying small molecules. (We tried at length to adopt the printing process shown in this paper to dope Alq_3, but the solvent vapor step caused re-crystallization of the Alq_3.) While polymers are amenable to printing, small

molecules are more easily used to control transport properties and the thickness of the layers. Thus our general approach represents a novel combination to exploit the best properties of both small molecule films (for transport and band diagram considerations) and polymer films (for printability) for organic LED's.

2.5 Summary

Dry dye printing from a pre-patterned printing stamp followed by solvent-enhanced dye diffusion was used to locally dope a previously spin-coated polymer film with different dyes to fabricate side-by-side RGB OLED sub-pixels for a full color display. To reduce reverse leakage current and improve efficiency, a novel tri-layer OLED structure, which consists of an additional Alq_3 ETL layer and a BCP hole/exciton blocking layer was developed. The BCP layer confines the light emission to the doped polymer layer. The EL efficiency of the devices was optimized by the dye concentration in the printing plate. Devices with this tri-layer structure and the optimized dye source demonstrate high external quantum efficiencies (~1%) and an extremely low reverse leakage current (rectification ratio of 10^6 at +/- 10V). This device architecture demonstrates a new approach to combine the printability of polymer with the optimum transport capability of small organic molecules to achieve high performance organic LED's.

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CHAPTER 3

HYDROGENATED AMORPHOUS-SILICON THIN-FILM TRANSISTORS

Active matrix OLED displays (AMOLED's) have wider applications than passive matrices because AMOLED's can more easily achieve high resolution, large size, and lower power consumption. In this thesis, amorphous silicon (a-Si) thin-film transistors (TFT's) are used to make the AMOLED backplane. This chapter reviews the materials and characteristics of a-Si TFT's.

3.1 Basic Properties of Amorphous Silicon

Unlike crystalline silicon (c-Si), whose atoms are arranged neatly in a periodic lattice, the silicon atoms in an a-Si:H film are bonded to each other with variation in the bond angles and the bond lengths, thus forming an amorphous network (Fig. 3-1).

Although a-Si is disordered at the atomic scale, it retains the same local chemical bonding as in crystalline silicon, with four bonds on most silicon atoms. As shown in Fig. 3-2, a-Si retains the short-range order while the long-range order is missing. When a silicon atom is missing one or more of its silicon bonds, hydrogen can be bonded to the

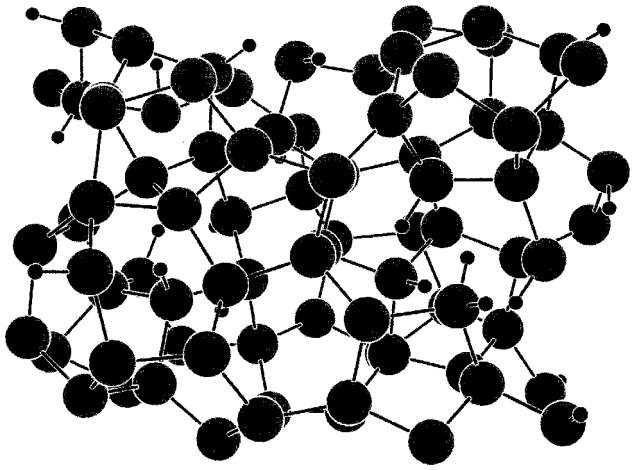

Figure 3-1. Model of the atomic structure of a-Si:H showing the random covalent network and the Si-H bonds. [6]

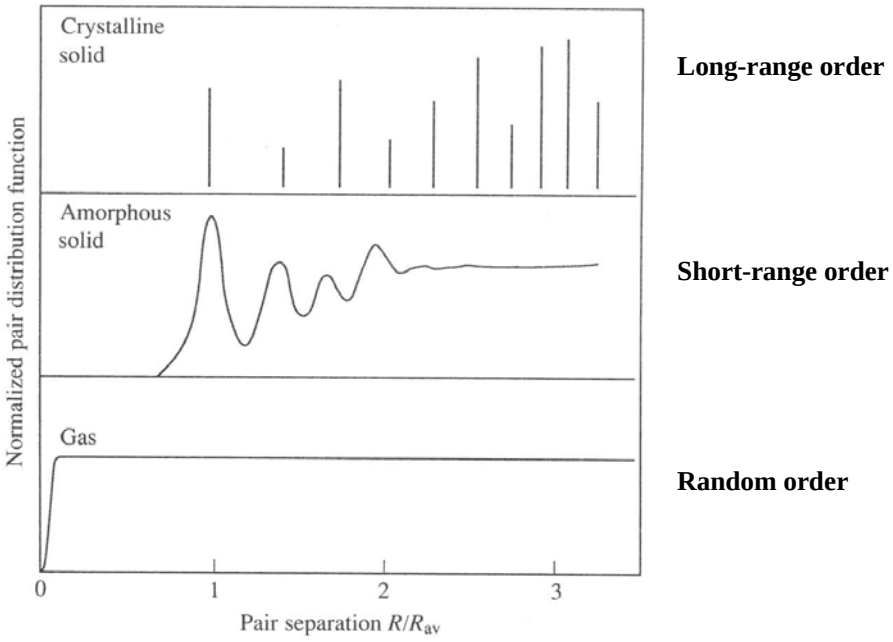

Figure 3-2. Normalized pair distribution as a function of separation distance [1].

silicon atoms in the form of Si-H bonds, either isolated or on the surface of small voids. This Si-H bond passivates what otherwise would be a dangling bond and defect level. The bonding disorder determines most of the electronic properties of a-Si:H and strongly influences the design of the devices. Free electrons and holes in a-Si:H have a scattering length of only an inter-atomic spacing, and consequently a free carrier mobility of only about 10-20 cm^2/Vs, compared to about 500 cm^2/Vs in crystalline silicon. More significantly, the disorder causes an exponentially decaying density localized states at the band edges extending into the forbidden gap (Fig. 3-3). The energy dividing the extended

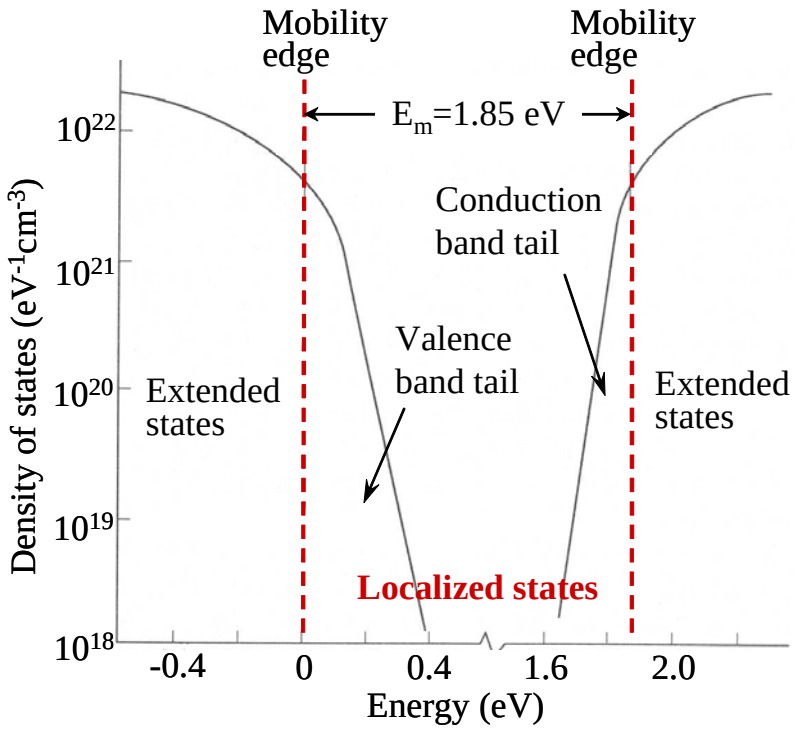

Figure 3-3. a-Si:H density of state as a function of energy [1]. The onset of tail states marks the edges of the mobility gap E_m.

and localized states is known as the mobility edge. Conduction of both electrons and holes occurs near the mobility edges, but involves frequent trapping and release from the localized states and consequently, the effective carrier mobility is further reduced. The conduction band tail is narrower than the valence band tail, so that electrons have a higher mobility than holes. Some of the key electronic parameters are listed in table 3-1.

Table 3-1. Typical material parameters for good electronic quality a-Si:H [1]. The exact values depend on the details of the deposition conditions.

Electron drift mobility	1 cm^2/Vs
Hole drift mobility	0.003cm^2/Vs
Optical band gap	1.7eV
300K conductivity (undoped)	10^{-11} Ω^{-1} cm^{-1}
300K conductivity (n^+)	10^{-2} Ω^{-1} cm^{-1}
300K conductivity (p^+)	10^{-3} Ω^{-1} cm^{-1}
Defect density	$10^{15}cm^{-1}$
Diffusion length	300 nm
Hydrogen concentration	10 at.%

Despite the large amount of bonded hydrogen, undoped a-Si:H retains about $10^{15}cm^{-3}$ dangling bond defects which form electronic states near the middle of the band gap (Fig. 3-4). These defects control the trapping and recombination of carriers, and hence determine the carrier lifetimes, photoconductivity and depletion layer width of Schottky barriers and p-i-n junctions. Many years of experimenting with plasma deposition conditions have not succeeded in further reducing either the defect density or the band tail widths, which suggests that fundamental limits may have been reached. In doped material the defect density increases by 2-3 orders of magnitude, which greatly reduces the minority carrier lifetimes. For this reason, doped layers are primarily used to set the Fermi levels in junctions rather than active layers. Hence, the channel of the TFT is undoped.

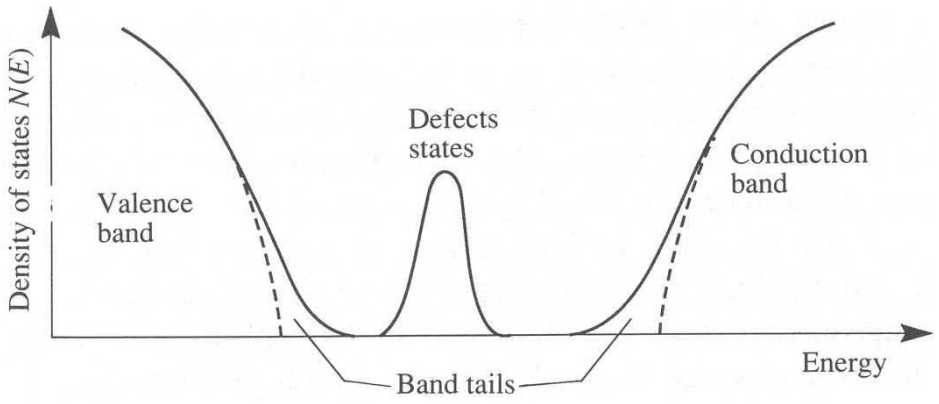

Figure 3-4. Schematic density of states of a-Si:H showing the localized band tails and defect states [2].

3.2 Structures of amorphous silicon thin-film transistors

Amorphous silicon thin-film transistors are metal-insulator-semiconductor field-effect transistors (MISFET's) which require three materials to function: a gate metal, a gate dielectric or insulator, and a semiconductor active layer. Conventional MISFET devices such as MOSFET's use thermally-grown silicon dioxide (SiO_2) as the gate insulator and c-Si as the semiconductor layer. Amorphous silicon TFT's, on the other hand, typically use deposited films of silicon nitride (SiN_x) as the gate insulator and undoped a-Si as the active semiconductor layer. A phosphorus-doped n+ a-Si layer provides ohmic contact between the active layer and the source-drain metal. The gate metal and source-drain metal are depend on the choice of TFT structure. For metal layers

exposed to the deposition environment, refractory metals or alloys such as chromium (Cr) or Mo/Ta must be used.

An inverted-staggered structure with bottom gate and top source/drain is the standard a-Si TFT structure widely used in the industry due to its superior electronic properties and ease of fabrication. Since the gate insulator SiN_x film and the active layer undoped a-Si film can be grown continuously without a patterning step in between, the nitride-silicon interface can be less contaminated, thus having less defects. This inverted-staggered structure can be built as back-channel etch structures or as etch-stop structures, as illustrated in Fig. 3-5(a) and (b). To ensure complete removal of the n+ layer from the channel, the back-channel etch structure requires a slight over-etch into the undoped a-Si layer. This forces the undoped channel layer to be rather thick. The etch-stop structure, on the other hand, can have a very thin undoped layer. This is possible because a second insulator layer, deposited on top of the intrinsic layer, serves as an etch-stop during removal of the n^+ layer from above the channel. Thus, there is no over-etch into the intrinsic layer, which can therefore be made very thin.

The advantage of the back-channel etch structure is its ease of fabrication. There is one less mask step and one less layer to grow than for the etch-stop structure. The drawbacks, however, are the need for a relatively thick intrinsic layer, which leads to higher OFF currents and greater photo sensitivity. The etch-stop structure requires more steps to fabricate, but avoids the problems encountered by the back-channel etch structure. For this thesis, the back-channel etch structure is used for its simplicity.

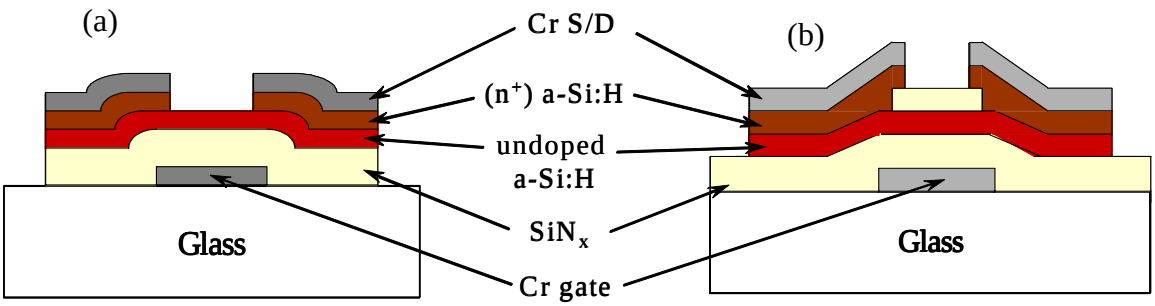

Figure 3-5. Schematic cross section of a-Si TFT structures: (a) back-channel etch structure; (b) etch-stop structure.

3.3 Growth of amorphous silicon and silicon nitride

Growth of a-Si and silicon nitride thin films typically involves the reaction and absorption of chemical vapors and their reactive species on a substrate surface. This process, known as chemical vapor deposition (CVD), is well suited to the fabrication of large-area electronics. When the growth reaction is activated by a plasma excited by rf power, the process is know as plasma-enhanced chemical vapor deposition (PECVD). PECVD is the most common technique for growing of amorphous silicon and silicon nitride thin films. Assisted by plasma power, the CVD reaction can then be activated at low temperatures (< 400°C). This is very important for obtaining good quality a-Si:H films with hydrogen incorporated into the amorphous network. If the substrate temperature is higher than 450°C, hydrogen will not be retained in the film. Silane gas (SiH_4) is used for a-Si growth. Fig. 3-6 shows the defect density and hydrogen concentration in a-Si film as a function of substrate temperature (a) and rf power (b)

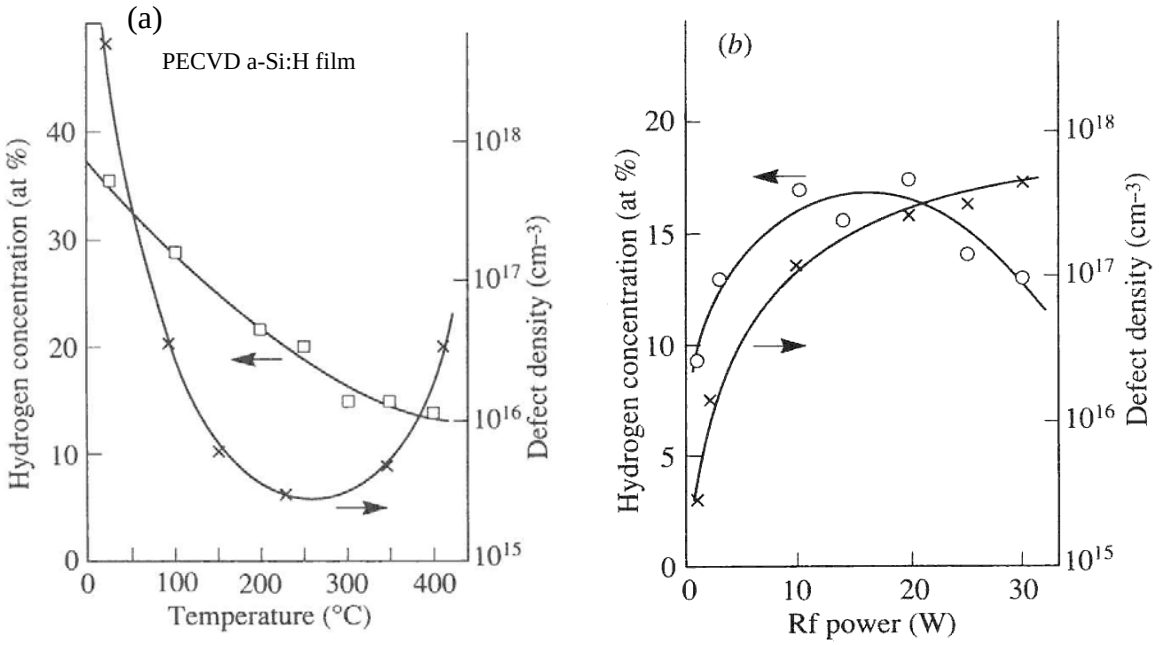

Figure 3-6. Defect density and hydrogen concentration in a-Si film as a function of (a) substrate temperature and (b) rf power during PECVD process [1].

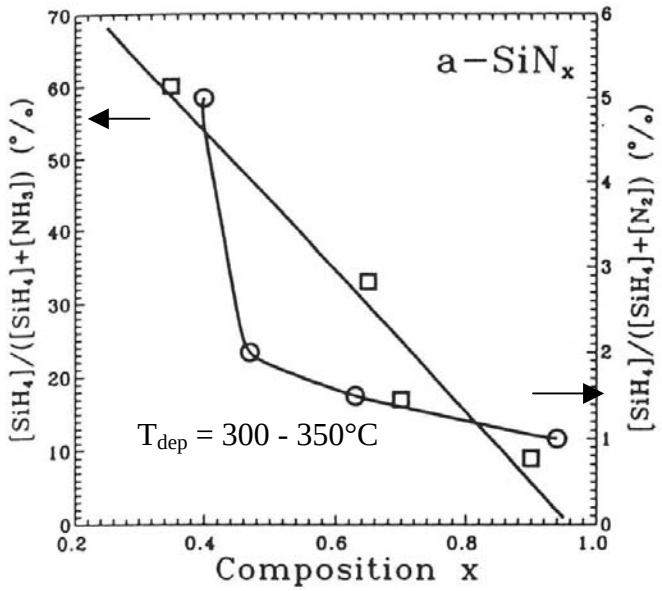

Figure 3-7. Dependence of SiN_x composition on the degree of NH_3 or N_2 dilution in the gas mixture. X=1.33 is the stochiometric composition for the best film quality [3].

during the PECVD process. A-Si deposited by PECVD contains a large amount of hydrogen. The H-content decreases with increasing substrate temperature. The defect density reaches a minimum at the substrate temperature of 250°C, and low rf power produces the best films.

Silane and ammonium mixtures ($SiH_4 + NH_3$) or silane and nitrogen mixtures ($SiH_4 + N_2$) are used for SiN_x growth. Silicon nitride film deposited by PECVD is non-stochiometric. From Fig. 3-7 shows high NH_3 (N_2) dilution of SiH_4 is needed for SiN_x composition close to the stochiometric one.

Studies of the dependence of the SiN_x film composition on the substrate temperature show that higher deposition temperature provides films close to the stochiometric composition and low H content. The optimum deposition temperature is 300 – 350ºC (Fig. 3-8).

In summary, to get high quality a-Si:H films, the optimum substrate temperature is 250ºC. Highly NH_3 or N_2 diluted SiH_4 is preferred for SiN_x deposition, and 300 – 350ºC substrate temperature produces the best SiN_x film. In this thesis, we increased the process temperature on clear plastic substrates from below 140ºC on conventional clear plastics to up to 280ºC on a novel high temperature clear plastic substrate. This high temperature process produces high quality a-Si and SiN_x films and a-Si TFT's with high mobility, low leakage current and high device stability [7], and will be investigated in Chapter 4.

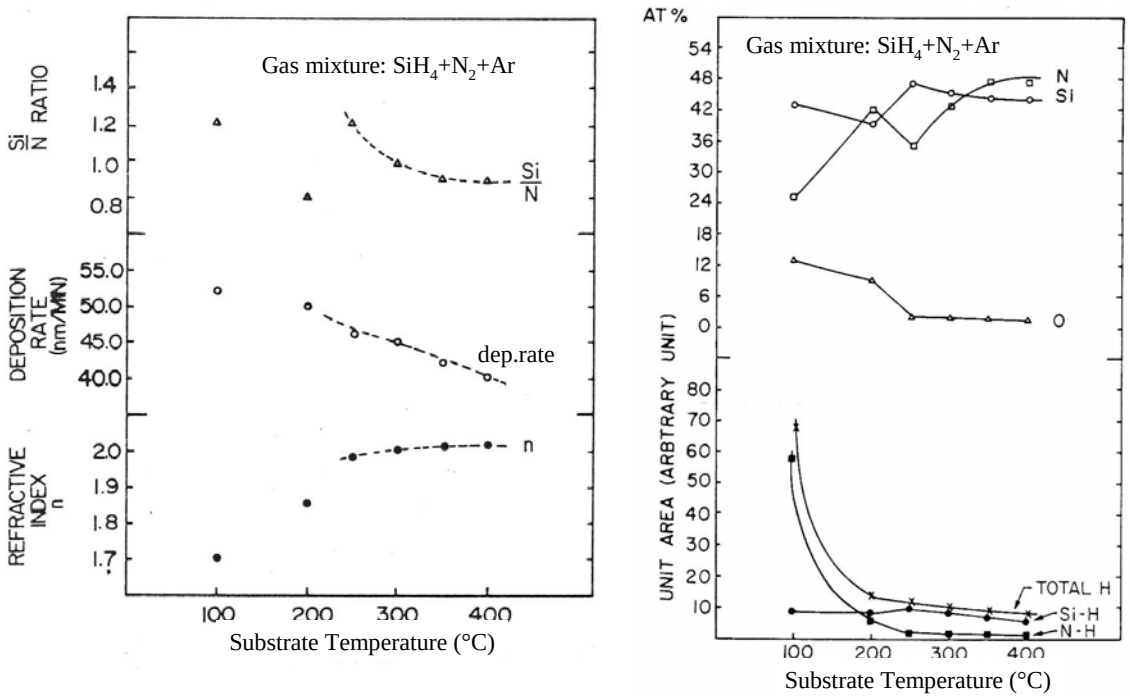

Figure 3-8. Dependence of SiN_x properties on substrate temperature [8].

3.4 a-Si TFT Operation and Its Characteristics

3.4.1 Operation of a-Si TFT's

Because the hole mobility in undoped a-Si is quite poor, nearly three orders of magnitude lower than the electron mobility (Table 3-1), a-Si TFT's are operated only as n-channel devices. Depletion devices in doped p-type a-Si are not used for p-channel devices because of this low hole mobility and because doping amorphous silicon results in more defective material, leading to poorer transport properties [4]. Because of the defects in doped material, the n-type devices in practice are "accumulation mode" in

undoped a-Si. A positive voltage on the gate, will attract electrons to the interface between the gate dielectric (SiN_x) and the active layer (undoped a-Si), forming a highly conductive "accumulation" layer. When a voltage is then applied across the source-drain contacts, electrons, assisted by the electric field, enter the accumulation layer and drift through the channel. This behavior characterizes the ON state of an a-Si TFT. The magnitude of the ON current depends largely on the geometry of the devices, but also on the quality of the i-layer and its interface with the gate dielectric.

In the OFF state, there is no accumulation of electrons between the source ad drain, so the channel resistance is high and drain current per unit channel width is very low (~ 1pA/μm). This drain OFF current is determined primarily by device geometry and material quality. When the drain OFF current is too high, it is sometimes referred to as leakage current, of which there are two types: source-drain leakage and gate leakage. Source-drain leakage in a TFT is strongly affected by the thickness of the intrinsic a-Si layer and by exposure of the channel region to light. Gate leakage refers to any current which flows through the gate contact. It is primarily determined by the quality of the gate insulator. Optimization of the silicon nitride film is therefore critical in the fabrication of TFT's.

3.4.2 Device characterization

The current-voltage characteristics of a TFT can be analyzed in essentially the same way as those of crystalline silicon MOSFET's [5]. In order to formulate the I-V characteristics, the following assumptions are made: 1. The carrier mobility in the

channel is constant; 2. The gate capacitance is constant and independent of the gate voltage; 3. The source and drain electrodes have ohmic contacts to a-Si:H; 4. The initial charge density in a-S:H is n_0; 5. The gradual channel approximation developed for conventional c-Si MOSFET's can also be applied to a-Si TFT devices. The last assumption means that the longitudinal electric field (E_z) is greater than the transverse electric field (E_x) in the channel.

From these assumptions, we can calculate that when $0 < V_{ds} < V_{gs} - V_t$, the drain current increases with gate voltage:

$$I_d = \frac{W}{L}\mu_n C_i \left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right] \qquad (3\text{-}1)$$

We say the device is working in the linear region. I_d is the drain current measured between the drain and source electrodes, V_{gs} is the voltage applied across the gate and source electrodes, V_{ds} is the voltage applied across the drain and source electrodes. The width-to-length ratio (W/L) is determined from the geometry of the device. The field-effect mobility μ_n and the threshold voltage V_t are determined experimentally. C_i is the capacitance per unit area of the silicon nitride gate dielectric.

When $V_{ds} > V_{gs} - V_t$, the drain current is saturated and it does not increase with increasing V_{ds}, the conducting channel is pinched-off in the neighborhood of the drain. The saturated drain current is:

$$I_d = \frac{W}{2L}\mu_n C_i (V_{gs} - V_t)^2 \qquad (3\text{-}2)$$

Now the TFT is working in the saturation region.

The two most common measurements used to describe TFT performance are the output characteristics (I_{DS} vs. V_{DS}) and the transfer characteristics (log I_D vs. V_{GS}). The

output characteristics are obtained by measuring drain current as a function of drain voltage for several different gate voltages. This produces a "family of curves" as shown in Fig. 3.9 (b) [6]. The transfer characteristics, however, are displayed on a semi-log plot

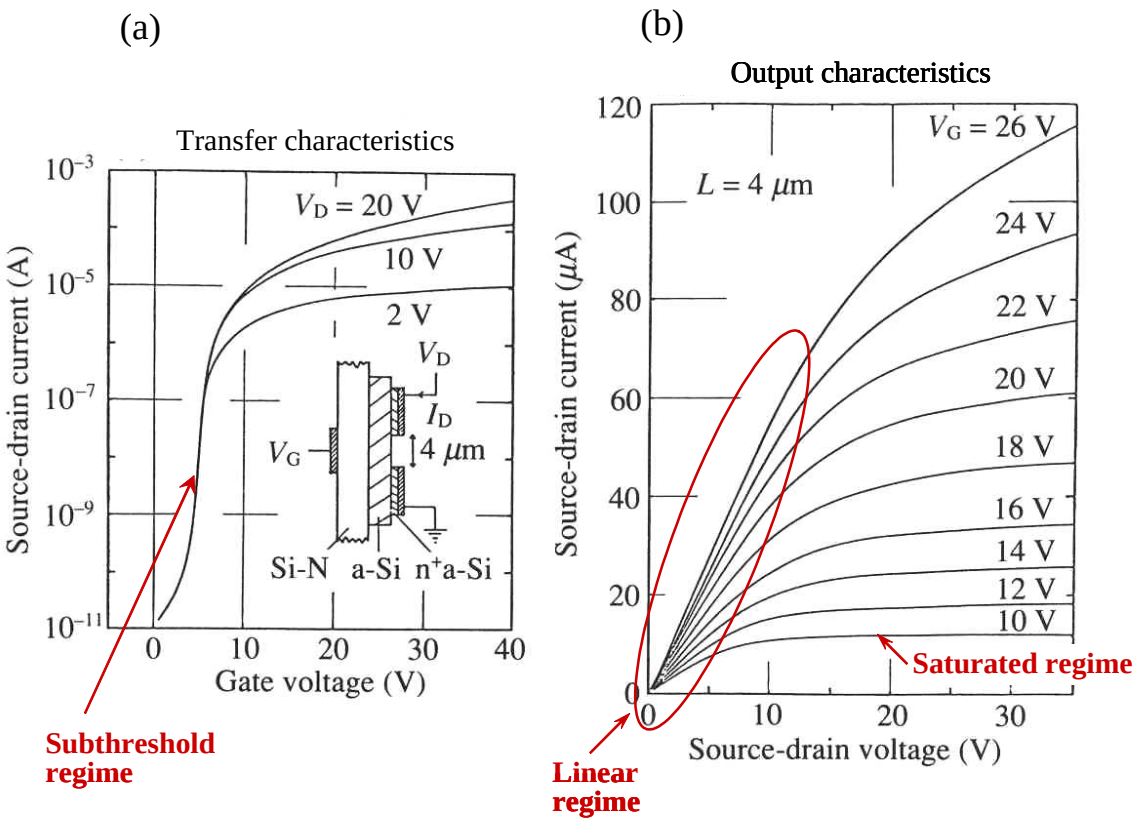

Figure 3-9. (a) Transfer and (b) output characteristics of an a-Si:H TFT.

and obtained by measuring drain current as a function of gate voltage. As illustrated in Fig.3-9 (a), they are typically evaluated at several different drain voltages. This measurement generally provides more useful data than the output characteristics. Many TFT parameters can be obtained from the transfer characteristics, specifically the field-

effect mobility, threshold voltage, ON/OFF ratio, and subthreshold slope. So it is used extensively throughout this thesis.

Field-Effect Mobility and Threshold Voltage. One measure of the ease with which electrons flow between source and drain when the channel is biased into accumulation is the electron field-effect mobility, μ_n. Specifically, it is the velocity of electrons per unit (source-drain) electric field, with units [cm^2/Vs]. There are, in fact, two field-effect mobilities evaluated, a linear-region mobility and a saturation-region mobility, which have similar but usually not identical values.

The linear-region mobility can be obtained from the equation of the linear-region drain-to-source current Eqn. (3-1):

$$I_d = \frac{W}{L}\mu_n C_i\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \qquad (3\text{-}3)$$

Assuming V_{gs} is varied and V_{ds} is fixed:

$$I_d = \frac{W}{L}\mu_n C_i(V_{gs} - V_t - \frac{V_{ds}}{2})V_{ds} = \frac{W}{L}\mu_n C_i V_{gs} V_{ds} + constant \qquad (3\text{-}4)$$

The drain current I_d is linear with gate voltage. Plotting I_d on a linear scale against V_{gs} in this regime will reveal this linear region as illustrated in Fig. 3-10. By extrapolation down to zero drain current, the threshold voltage can be determined. As one can see from Eqn. (3-4) above, the x-intercept of such a plot corresponds to a value of $V_{gs} = V_t + V_{ds}/2$. For the case where $V_{ds} << (V_{gs} - V_t)$, $V_{gs} = V_t$ for the x-intercept. This gate voltage marks the "threshold" where the transistor changes from the OFF state to the ON state.

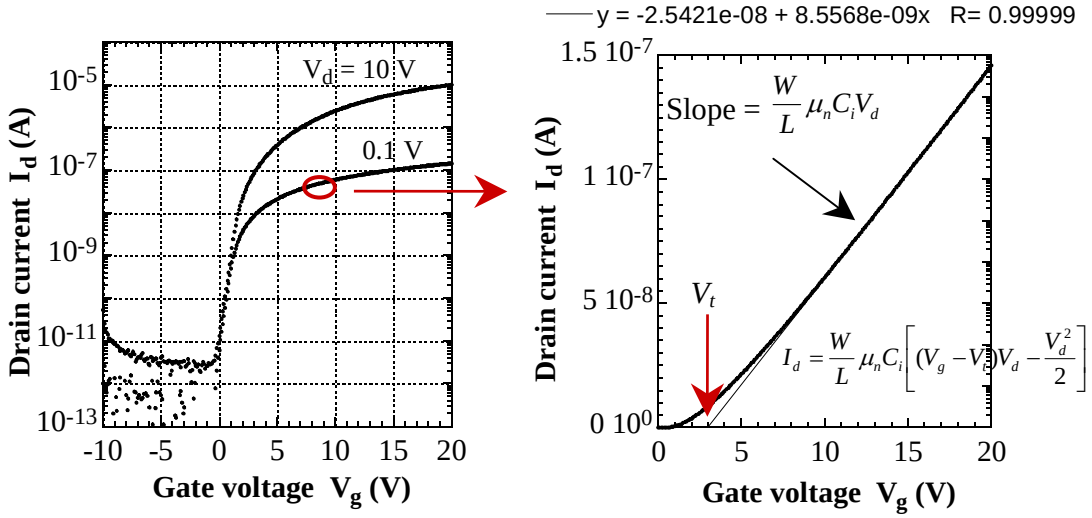

Figure 3-10. Drain current is plotted against gate voltage for the low drain voltage condition, V_d = 0.1V. Threshold voltage (V_t) and linear mobility (μ_n) can be extracted from such a plot.

The linear-region mobility can be determined by measuring the slope in Fig. 3-10:

$$\mu_{n,linear} = \frac{slope}{C_i (W/L) V_{ds}} \tag{3-5}$$

To determine the saturation-region mobility, consider the drain-to-source current in saturation region when $V_{ds} > V_{gs} - V_t$ (Eqn. (3-2)):

$$I_{d,sat} = \frac{W}{2L} \mu_{n,sat} C_i (V_{gs} - V_t)^2 \tag{3-6}$$

Taking the square-root of I_d, we obtain:

$$\sqrt{I_{d,sat}} = \sqrt{\frac{\mu_{n,sat} C_i W}{2L}} (V_{gs} - V_t) \tag{3-7}$$

Eqn. (3-7) reveals that $\sqrt{I_{d,sat}}$ is linear with respect to V_{gs}, with the x-intercept corresponding to the threshold voltage, V_t. Plotting $\sqrt{I_{d,sat}}$ vs. V_{gs} from the actual experimental data will reveal a linear region (Fig. 3-11). The threshold voltage can be determined by extrapolating down to the x-intercept. The slope of this plot can be determined analytically:

$$slope = \frac{\partial \sqrt{I_{d,sat}}}{\partial V_g} = \sqrt{\frac{W \mu_{n,sat} C_i}{2L}} \qquad (3\text{-}8)$$

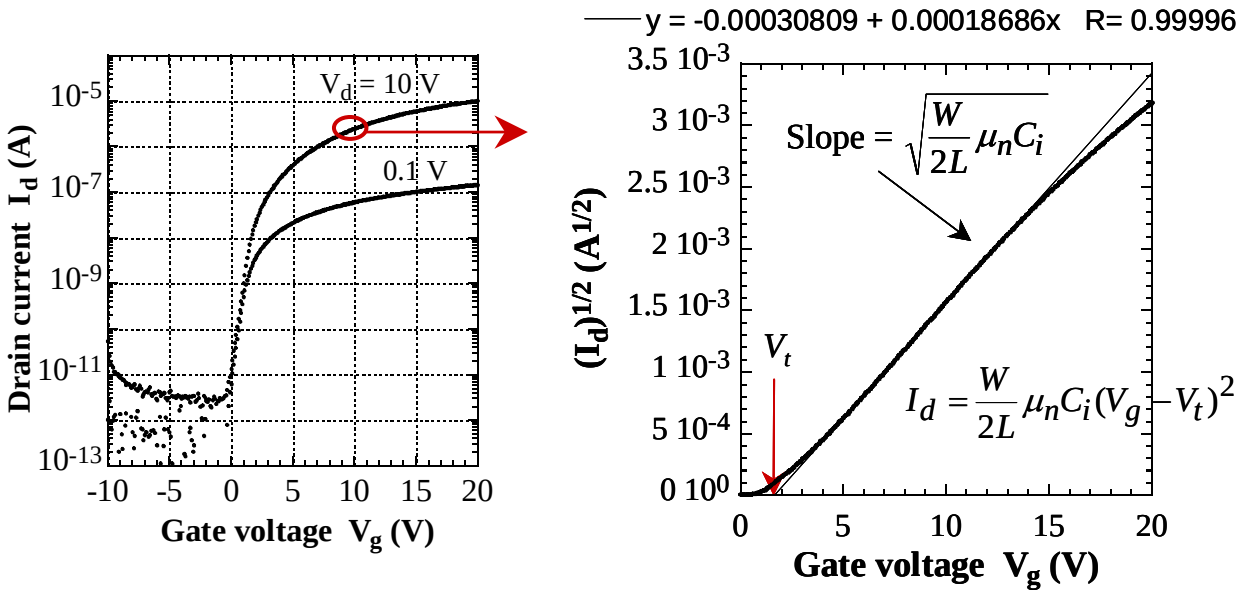

Figure 3-11. Drain current is plotted against gate voltage for the high drain voltage condition, V_d = 10V. Threshold voltage (V_t) and saturation mobility ($\mu_{n,sat}$) can be extracted from such a plot.

The saturation mobility is:

$$\mu_{n,sat} = slope^2 \left(\frac{2L}{WC_i} \right) \qquad (3\text{-}9)$$

The saturation mobility can be calculated from the slope.

ON/OFF Ratio and Sub-threshold Slope. One measurement of the TFT performance is the ratio between the highest ON current measured (I_{on}) and the minimum leakage current measured when the TFT is OFF (I_{off}). As shown in Fig. 3-12, typical ON/OFF ratio are between 10^5 and 10^7 for a-Si TFT's. In this plot of TFT transfer characteristics, there is a slope that provides a measure of the increase in gate voltage required to switch the transistor from OFF to ON. This gate voltage swing must be capable of increasing the

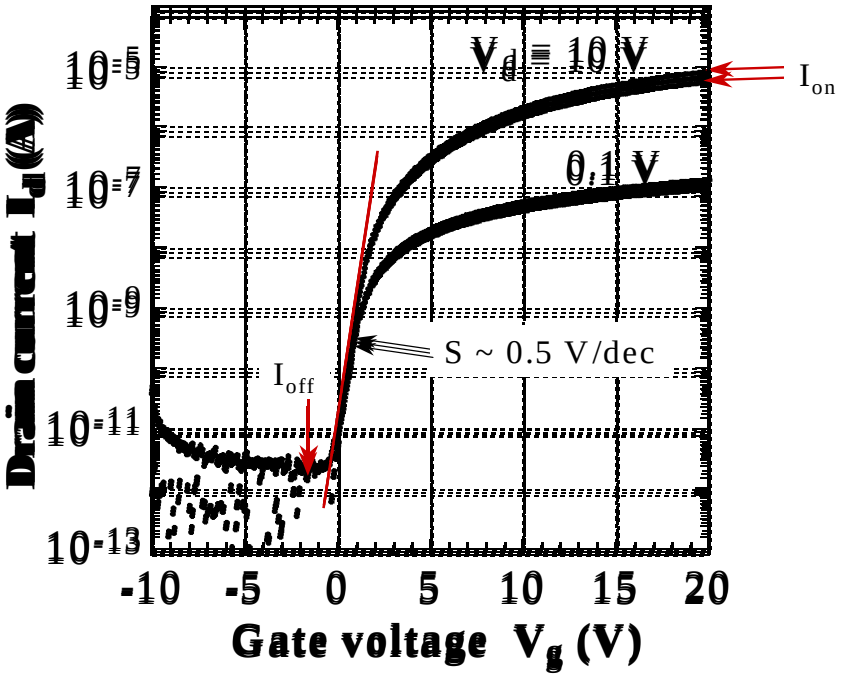

Figure 3-12. TFT transfer characteristics. ON current, OFF current, and sub-threshold slope are obtained form this plot.

current by as much as seven orders of magnitude, yet should be kept small in order to minimize switching time and power consumption. Rather than measuring the transition region slope, the sub-threshold slope actually reports its inverse, with units [V/decade]. Smaller numbers correspond to faster switching and better TFT's.

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CHAPTER 4

AMORPHOUS-SILICON THIN-FILM TRANSISTORS ON CLEAR PLASTIC SUBSTRATES

4.1 Introduction

Amorphous-silicon (a-Si) thin-film transistors (TFT's) on plastic substrates are attractive for driving flexible displays because they provide thin, light-weight, rugged, rollable and foldable backplanes. The plastic substrates for the TFT backplane must be optically clear for active-matrix liquid-crystal displays (AMLCD's) and for bottom-emitting active-matrix organic light-emitting displays (AMOLED's) which require the light to pass through the substrates.

In the AMLCD industry, a-Si TFT's are fabricated on glass at a maximum plasma-enhanced chemical vapor deposition (PECVD) process temperature of 300-350°C. This high temperature results in the best a-Si TFT performance, in particular because ~ 350°C is required for obtaining silicon nitride (SiN_x) gate insulator of high quality and good TFT reliability [1]. High-temperature plastics, such as the polyimide Kapton® E, have glass transition temperatures T_g of ~350°C and allow TFT fabrication at process temperatures of 150-250°C [2][3][4]. However, Kapton is not optically clear. The optical transmission of a 50-μm thick Kapton 200E substrate cuts off at a wavelength of about 500nm (Fig. 4-1), which gives it an orange-brown color.

The properties of the clear plastic substrates available to date have restricted the a-Si TFT fabrication process to temperatures below 140°C, since most clear plastics have glass transition temperature (T_g) of 120°C or less [5][6][7]. A widely used clear plastic substrate is poly (ethylene terephthalate) (PET) [8]. Its glass transition temperature (T_g) of 70-110°C is too low for fabricating high quality a-Si:H TFT's (Table 4-1). Another popular clear plastic substrate is poly(ethylene naphthalate) (PEN). It has a T_g of 120°C.

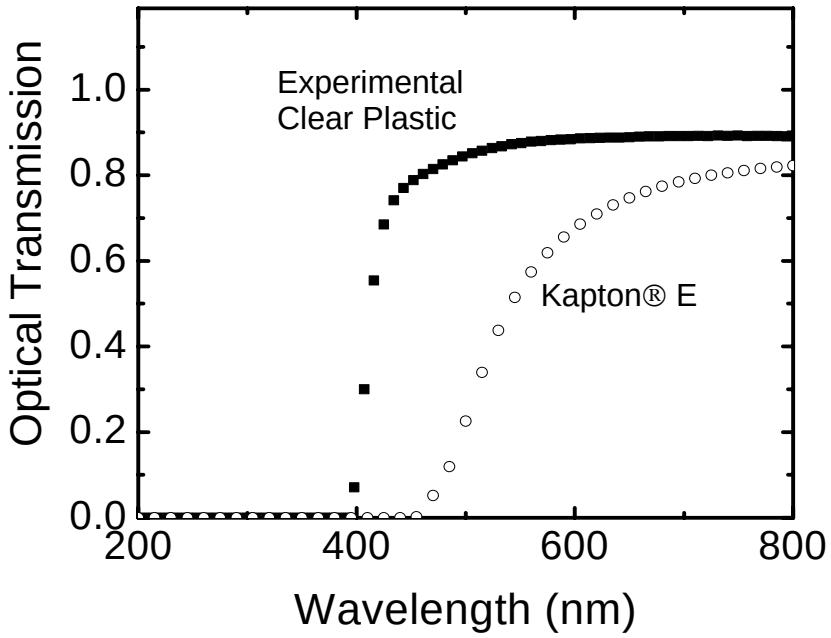


Figure 4-1. . Optical transmission spectra of a 50μm-thick foil of Kapton® 200E and of a 75μm-thick clear plastic substrate A .

Table 4-1. Clear plastic substrates for TFT fabrication. Optical transmission at λ=700nm, glass transition temperature (T_g), coefficient of thermal expansion (CTE), and maximum a-Si TFT fabrication temperatures are listed. Experimental substrates A and B were used in this work and were supplied by DuPont.

Substrate	**Optical Transmission (λ=700nm) / Thickness**	**T_g (°C)**	**CTE (10^{-6}/ °C)**	**Max. Process Temperature (°C)**
Polyethylene Terephthalate (PET)	88% / 125μm	70-110	15	<120 [15]
Poly(ethylene naphthalate) (PEN)	82% / 125μm	120	13	130 [16]
Poly-Carbonate	90% / 125μm	130	60-70	120 [17]
Experimental clear plastic substrate A	90% / 100μm	326	45	180 (this work)
Experimental clear plastic substrate B	85% / 100μm	315	≤10	Up to 280 (this work)

We have fabricated a-Si TFT's on it at a maximum process temperature of 130°C (Fig. 4-2). However, their electron mobility is only 0.3 cm^2/Vs, in contrast to ~0.8 cm^2/Vs for the TFT's fabricated at 150°C on Kapton E [3], which demonstrates the loss in device quality as the process temperature is reduced. In addition, the TFT's on PEN have high source-to-gate leakage current (up to 200 pA/μm of gate width). A low mobility may lead to low refresh rate and low brightness of the displays. More critically, a high leakage current would produce flicker over a display frame time. The TFT results are consistent with earlier results that show that TFT's deposited at temperatures below 140°C have low electron mobility, high leakage current, and show pronounced drift due to charge trapping [5][7].

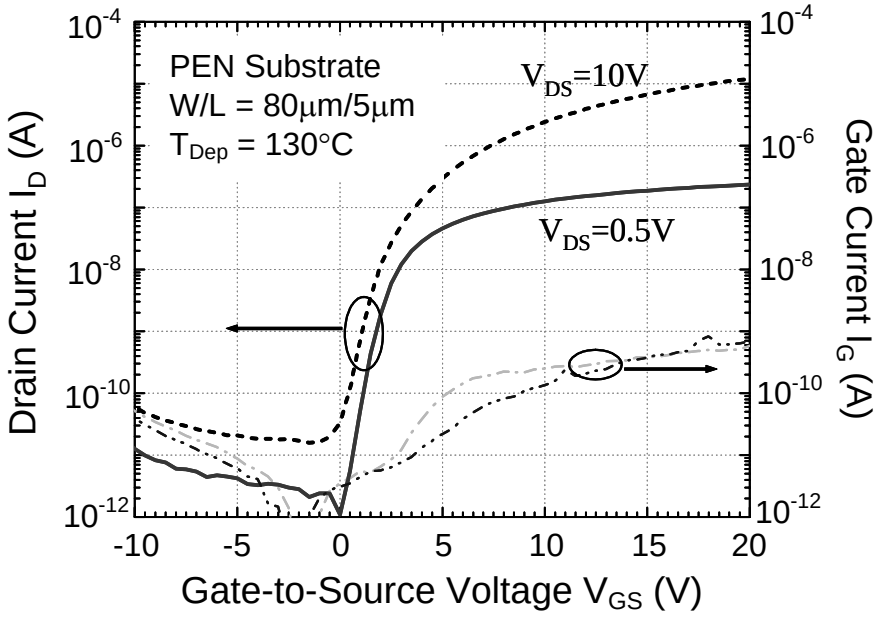


Figure 4-2. Transfer characteristics of a TFT processed at 130°C on PEN.

Thus clear plastic substrates with a glass transition temperature (T_g) in excess of 300°C are desired to allow process temperatures close to those used on glass substrates. However, clear plastics with a high T_g typically have a coefficient of thermal expansion (CTE) far larger than that of the silicon nitride and a-Si layers used in the TFT's [9][10]. This difference easily makes the device films crack, and may set a process temperature ceiling well below the plastic glass transition temperature.

In this chapter, we discuss the mechanical interaction of the TFT stack and the plastic substrate to develop mechanical design guidelines to avoid cracking. This model is then used to successfully fabricate a-Si TFT's on experimental clear plastic substrates at a maximum process temperature of up to 280°C. The TFT's made at high temperatures have higher mobility, lower leakage current, and high stability than TFT's made on conventional low-T_g clear plastic substrates.

Section 4.2 describes the engineering of the strain which develops at the interface between a plastic substrate with a high CTE and low Young's modulus and a device layer with a low CTE and high Young's modulus. The failure limit of the structure is experimentally quantified and design guidelines for the fabrication of crack-free TFT's are developed. Section 4.3 then describes the properties of such TFT's fabricated on clear substrates at maximum process temperatures of 180°C (on a plastic substrate with relatively high CTE) and at 250-280°C (on a plastic substrate with a low CTE). Section 4.4 discusses the increased device stability with high process temperatures.

4.2 Mechanical Behavior of Device Films on Plastic Substrates

To obtain crack-free device films, the SiN_x-on-plastic structure was studied in order to develop design guidelines to avoid cracking. SiN_x was chosen because in our typical process on plastic, a relatively thick nitride layer (~0.5μm) is deposited on both sides of the substrate to seal it against chemical attack during processing. As a first-order approximation, we assume the entire TFT stack (SiN_x, a-Si, Cr (Fig. 4-8)) has the same properties as SiN_x for mechanical modeling, since at least half of the total thickness (including the buffer) is SiN_x.

4.2.1 Mechanical Behavior of Film-on-Substrate Structures

A film-on-substrate structure has a mismatch strain in the device films after they are deposited at high temperature and then cooled down to room temperature. The total mismatch strain ε_M can be described by the following equation:

$$\varepsilon_M = \varepsilon_0 + \varepsilon_{th} + \varepsilon_{ch} , \qquad (4\text{-}1)$$

where ε_0 is the built-in strain, ε_{th} is the thermal mismatch strain and ε_{ch} is the moisture mismatch strain.

The built-in strain ε_0 is produced by built-in stress, which arises from atoms deposited in out-of-equilibrium positions. It is a function of the material system and the deposition conditions. The built-in stress tends to be tensile in chromium (Cr) and compressive in a-Si, and can be varied from tensile to compressive in SiN_x by increasing the PECVD deposition power [11].

The thermal mismatch strain ε_{th} is introduced by the coefficient of thermal expansion mismatch between the film and the substrate. During a-Si TFT fabrication, the films are typically deposited at elevated temperature. The thermal mismatch strain produced by cooling down to room temperature is given by:

$$\varepsilon_{th} = \Delta CTE \times \Delta T, \qquad (4\text{-}2)$$

where $\Delta CTE = CTE_{device\ film} - CTE_{substrate}$ is the CTE difference between the device film and the substrate, ΔT is the process temperature excursion (defined >0).

The moisture mismatch strain ε_{ch} is observed in samples deposited after vacuum bake that have been brought into moist air after deposition. It is described by

$$\varepsilon_{ch} = \Delta CHE \times \%RH \qquad (4\text{-}3)$$

where ΔCHE is the difference in coefficient of humidity expansion (CHE) and $\%RH$ is the percent of relative humidity. From Table 4-2 we can see the CHE of the device films is zero while the clear plastic substrate has a CHE of ~10 *ppm*/*%RH*.

Table 4-2. Mechanical properties of the experimental clear plastic substrates and the device films. The properties of SiN_x, a-Si and Cr are taken from reference [13].

		Clear Plastic A	**Clear Plastic B**	**SiN_x**	**i a-Si**	**n^+ a-Si**	**Cr**
Thickness (μm)	t	60-100	60-100	0.3	0.2	0.05	0.1
Coeff. thermal exp. (10^{-6}/K)	α	45	≤10	2.7	3 (2.2 - 4.5)		3 (1-5)
Young's modulus (GPa)	Y	2.9	2.9	210	170		140
Poisson's ratio	ν	0.34	0.34	0.25	0.22		0.21
Biaxial modulus* (GPa)	Y*	4.4	4.4	280	218		180
Plane strain modulus** (GPa)	Y'	3.3	3.3	224	180		146
Built-in stress in film (GPa)	σ_{BI}	--	--	Power dependent	Compressive –0.16		Tensile 0.54

*Biaxial modulus: $Y^* = Y / (1 - \nu)$
** Plane strain modulus: $Y' = Y / (1-\nu^2)$

In our experiments, the plastic substrate was coated on each side with a layer of SiN_x buffer, which acts as a very good moisture barrier. Therefore we assumed that the moisture mismatch strain ε_{ch} in our experiments is zero, and consider only the built-in strain ε_0 and thermal mismatch strain ε_{th}:

$$\varepsilon_M = \varepsilon_0 + \varepsilon_{th} = \varepsilon_0 + \Delta CTE \times \Delta T \qquad (4\text{-}4)$$

When a film is deposited on a compliant substrate, deformation occurs in both the film and the substrate. During deposition, our substrates are free-standing and not rigidly bonded to a glass or wafer carrier. Bonding will limit lateral thermal expansion, but removal of the bonding agent after processing without damaging the optically clear property of the back of the plastic can be problematic. In our work, during PECVD deposition, the substrate is held in a frame, so that the substrate is constrained to be flat, although it can expand and contract laterally. Under this flat condition, the stress in the film after returning to room temperature is given by [3]

$$\sigma_f = \frac{\varepsilon_M Y_f^*}{1 + (Y_f^* d_f)/(Y_s^* d_s)} \qquad (4\text{-}5)$$

$Y_f^* = Y_f/(1-\nu_f)$ is the biaxial elastic modulus of the film, with Y_f being Young's modulus and ν_f Poisson's ratio. Y_s^* is the biaxial elastic modulus of the substrate, d_f is the film thickness and d_s is the substrate thickness. The stress in the substrate is given by

$$\sigma_s = -\sigma_f d_f / d_s \qquad (4\text{-}6)$$

In most cases, $d_s >> d_f$, so the stress in the substrate is quite small compared to the stress in the film.

After deposition of the film, if the structure is released from the frame, the substrate bends into a roll [12]. Elementary beam theory can be used to model the structure as a bimetallic strip. The radius of curvature is given by [2]

$$R = \frac{(Y_s' d_s^2 - Y_f' d_f^2)^2 + 4Y_f' Y_s' d_f d_s (d_f + d_s)^2}{6\varepsilon_M Y_f' Y_s' d_f d_s (d_f + d_s)} \qquad (4\text{-}7)$$

Here $Y' = Y/(1-\nu^2)$ is the plane strain elastic modulus. This radius of curvature can be used to quantify the strain levels in the films [13].

If the inorganic device films are under tensile strain, the films fail by crack propagation from pre-existing defects. Under compressive strain, device films fail by delamination from the substrate coupled with buckling and fracture. The films may crack during or after deposition. The main strain component during deposition is built-in strain, and both built-in strain and thermal mismatch strain make up the total strain after deposition. Once the substrate and the process temperature have been selected, the thermal mismatch strain is fixed. The total mismatch strain can be reduced by controlling the built-in strain, i.e. by adjusting the deposition conditions of the device films. Typical brittle inorganic films for a-Si TFT's can be strained more in compression than in tension [14]. Good adhesion between the device films and the substrate can suppress the compressive strain failure, since we will show in the next section that interfacial effects appear to control the onset of failure.

4.2.2 Effect of Deposition Conditions on Built-in Strain

Our goal was to fabricate a-Si TFT's at as high a temperature as possible on two new types of experimental clear plastic substrates supplied by DuPont, substrate A and

substrate B, each with high T_g > 315°C (Table 4-1). They are transparent down to λ=400nm. The optical transmission spectrum of substrate A is shown in Fig. 4-1. Substrate A is more transparent at λ=700nm than substrate B (90% vs. 85% at 100μm thickness), but it also has a much higher CTE (45 ppm/°C) than substrate B (<10 ppm/°C) (see Table 4-1).

SiN_x films of various thicknesses were deposited on clear plastic substrates A or B under different deposition conditions. The SiN_x was deposited in a multi-chamber RF powered PECVD system with electrode area of 6" × 6" in a triode configuration. The typical deposition pressure is 500 mTorr, and the source gases are SiH_4 for a-Si, NH_3 and SiH_4 for SiN_x, with H_2 dilution for depositions at temperatures below 200°C.

The total strain in the device films can be reduced by choosing the appropriate deposition condition and by employing the built-in strain to compensate for the thermal mismatch strain. Because the CTE of substrate A (45 ppm/°C) is much higher than that of the SiN_x film (2.7 ppm/°C) (Table 4-2), the thermal strain in the SiN_x film is compressive when the SiN_x is cooled down to room temperature from the elevated deposition temperature. Therefore we want the built-in strain of the SiN_x film to be tensile to compensate for the thermal mismatch strain.

The built-in strain in the SiN_x can be controlled by adjusting radio-frequency (RF) power during the PECVD process. To measure the built-in strain ε_0 of SiN_x films vs. RF power, SiN_x films were deposited on one side of 50-μm-thick Kapton 200E substrates. The substrates were held in a frame during the nitride film deposition to keep it flat. After the deposition, the samples were cooled down to room temperature in the frame. When

they were released after the cooling, the samples bent into a roll because of the mismatch strain. Eqn. (4-7) allows the calculation of the total mismatch strain ε_M in the nitride film from the radius of curvature. From ε_M we can calculate the built-in strain ε_0 in the SiN_x film using Eqn. (4-4). For SiN_x films deposited at 150°C, the built-in strain changes from tensile to compressive as the deposition power increases (Fig. 4-3), from 0.26% at 5W deposition power to –0.1% at 25W deposition power. Tensile strain in the film is defined as positive. The crossover point lies at about 21W (90mW/cm^2) [13]. Because a deposition power below 5W can not maintain a stable deposition rate, the deposition power of 5W produces the most tensile built-in strain we can obtain in SiN_x. This condition was used for all later device work unless stated otherwise.

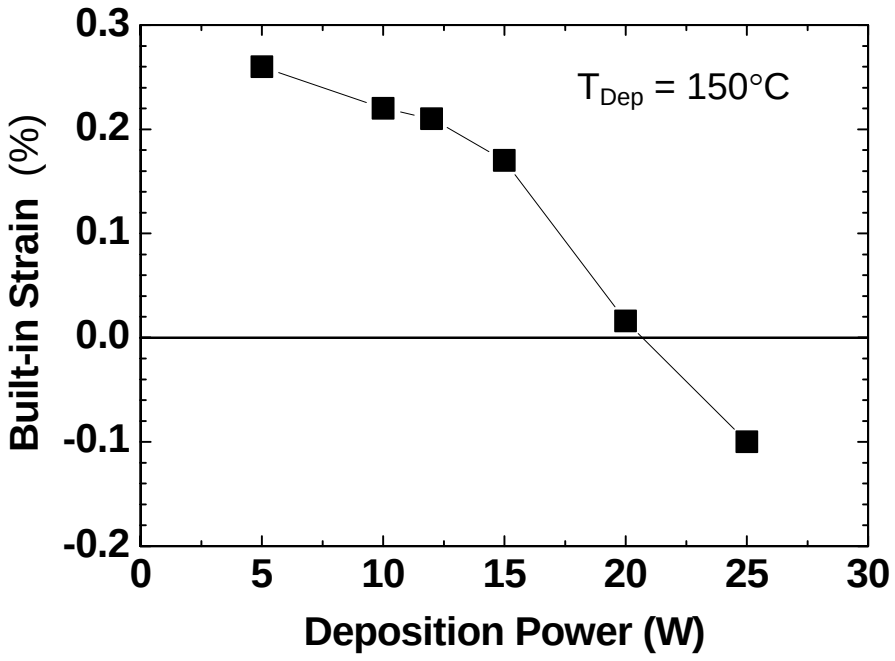


Figure 4-3. Built-in strain of SiN_x films deposited at 150°C by PECVD over a range of RF power. Low power grows films in tension (positive strain) and high power in compression (negative strain). [13]

We then deposited SiN_x on substrate A (75 μm thick) at the temperatures of 120°C, 150°C, 180°C, and 250°C, respectively, with the deposition power fixed at 5W. Again the built-in strain in the nitride films was calculated from Eqn. (4-7) and Eqn. (4-4). Table 4-3 lists the thickness of the nitride films we deposited, the deposition temperatures, radius of curvature of the structures at room temperature, and the built-in strain of the nitride films. The built-in strain increases slightly with rising deposition temperature, from 0.28% at 120°C to 0.42% at 250°C (Fig. 4-4). The built-in strain of SiN_x deposited at 150°C on clear plastic substrate A is calculated to be slightly higher than that on Kapton 200E (0.32% vs. 0.26%). This difference may result from uncertainties in the thickness, elastic modulus, or CTE between the two substrates.

For SiN_x on substrate A, $\Delta CTE = (45\text{-}2.7)\times10^{-6}/℃ = 42.3\times10^{-6}/℃$. From Eqn. (4-4) one finds that even the most tensile built-in strain of SiN_x, deposited at an RF power of 5W, for any deposition temperatures above 100°C, will leave the SiN_x film in compression after cooling to room temperature. The deposition power of 5W will result in the lowest total strain, however.

Table 4-3. Built-in strain of SiN_x films deposited at different temperatures with 5W rf power on Substrate A.

Deposition temperature T_{dep} (°C)	120	150	180	250
Silicon nitride thickness d_{SiNx} (μm)	0.3	0.6	0.5	0.2
Radius of curvature R_f (cm)	7.8	4.5	3.6	2.1
Built-in strain in SiN_x (%)	0.28	0.32	0.37	0.42

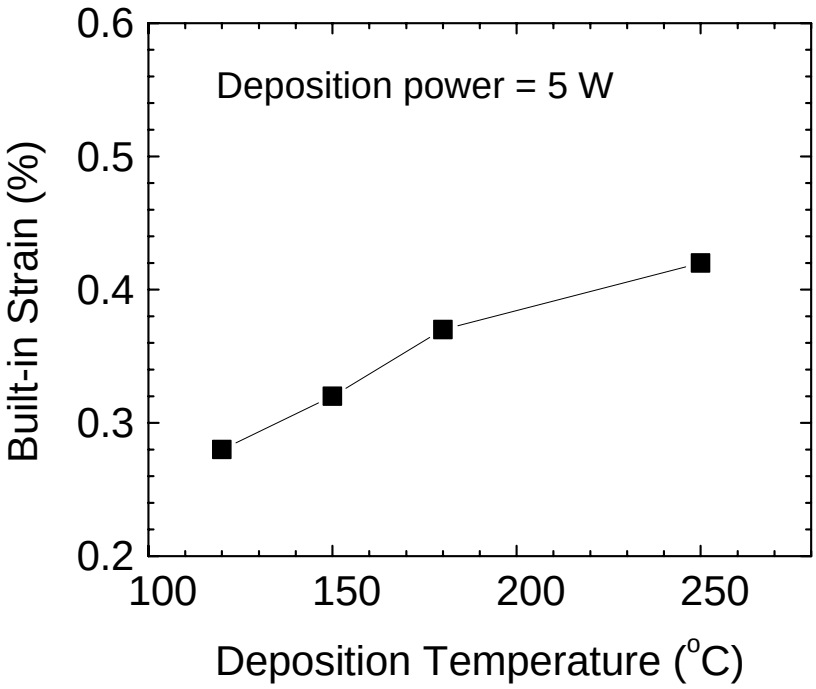


Figure 4-4. Built-in strain of SiN_x films deposited over a range of temperatures at 5W RF power. [25]

4.2.3 Interfacial Adhesion

We then studied the effect of adhesion of the SiN_x film on substrate A. The mismatch strain between the device films and the substrate must be supported by an interfacial force. Good adhesion between the device films and the substrate can help increase the critical value of the interfacial force the system can sustain and suppress the film failure. Right before the SiN_x deposition, we usually perform an Ar-plasma treatment step on the bare substrate. This step further cleans the substrate surface, and

activates the polymer substrate surface to create dangling bonds. Thus the SiN_x layer deposited immediately after the Ar-plasma treatment adheres to the substrate better.

4.2.4 Film Fracture and Critical Interfacial Force

At all PECVD temperatures (120°C, 150°C, 180°C, 250°C), the SiN_x films still cracked above a certain thickness. Fig. 4-5(a) shows the film thickness vs. deposition temperature. The filled symbols represent crack-free films, and the open symbols represent cracked films. The maximum nitride film thickness before cracking decreases as the temperature increases. When the temperature increased to 250°C, only a 200-nm-thick SiN_x film could be deposited without cracking. Since the strain in the nitride is essentially independent of thickness (Eqn. (4-4)), these experiments show that the critical factor leading to film failure and thus limiting TFT fabrication is not a fixed strain level in the film.

Any stress in the device film must be supported by an interfacial force between the device films and the substrate. From Eqn. (4-5), the interfacial force per unit width is:

$$\frac{F}{L} = \sigma_f \cdot d_f = \frac{\varepsilon_M Y_f^* d_f}{1 + (Y_f^* d_f)/(Y_s^* d_s)} \qquad (4\text{-}8)$$

where $\varepsilon_M = \varepsilon_0 + \varepsilon_{th} = \varepsilon_0 + \Delta CTE \times \Delta T$.

This interfacial force increases as the film thickness increases. We then re-plotted the data of Fig. 4-5(a) with absolute value of the interfacial force required to support all the stress in the device film as the ordinate (Fig. 4-5(b)). From the data it is clear that the

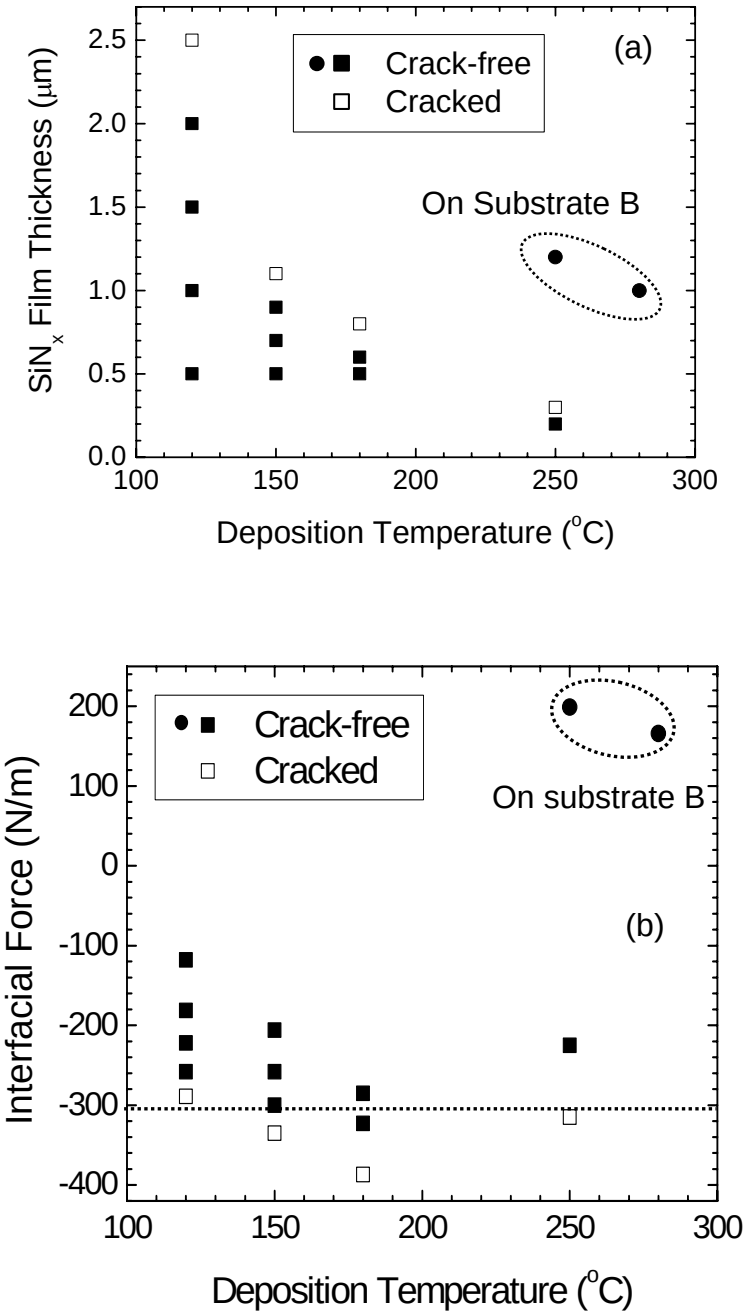


Figure 4-5. (a) Thickness and (b) Interfacial force of cracked (open symbols) and crack-free (filled symbols) SiN_x films deposited over a range of temperatures. The two films on substrate B (with low CTE) are labeled separately.

critical condition for the onset of mechanical failure is a critical interfacial force, which is independent of temperature. This critical interfacial force is ~ -300 N/m (the minus sign means compressive stress). SiN_x films with higher interfacial force cracked, while SiN_x films with lower interfacial force could be deposited without cracking.

Assuming a critical interfacial force of the SiN_x-on-plastic system, we can now engineer structures to remain below this critical force. Eqn. (4-8) indicates that decreasing the substrate thickness can raise the maximum film thickness allowed for a fixed critical interfacial force. When the nitride (or TFT stack) is made thicker, it forces the substrate to comply more with the nitride, which in turn lowers the interfacial force. Thin substrates and those with low Young's modulus comply more easily than thick and stiff substrates. For SiN_x of the present series of experiments deposited at 180°C with 5W RF power on substrate A with CTE = 45 ppm/°C and Young's modulus = 2.9 GPa, the interfacial force is shown as a function of substrate thickness in Fig. 4-6(a) for a range of nitride thicknesses. For a nitride thickness of 0.2μm and 0.5μm, the predicted interfacial force will not exceed the critical value on any substrate up to 100μm thick. However, for a 1-μm-thick nitride, the substrate must be thinner than 40μm to keep the interfacial force below the cracking point.

Because the deposition temperature determines the differential thermal contraction, it also affects the interfacial force. For a nitride layer of 1-μm thickness, Fig. 4-6(b) shows the interfacial force vs. substrate A thickness, with deposition temperatures ranging over 120°C, 150°C, 180°C, and 250°C. With a 120°C process, 1 μm of

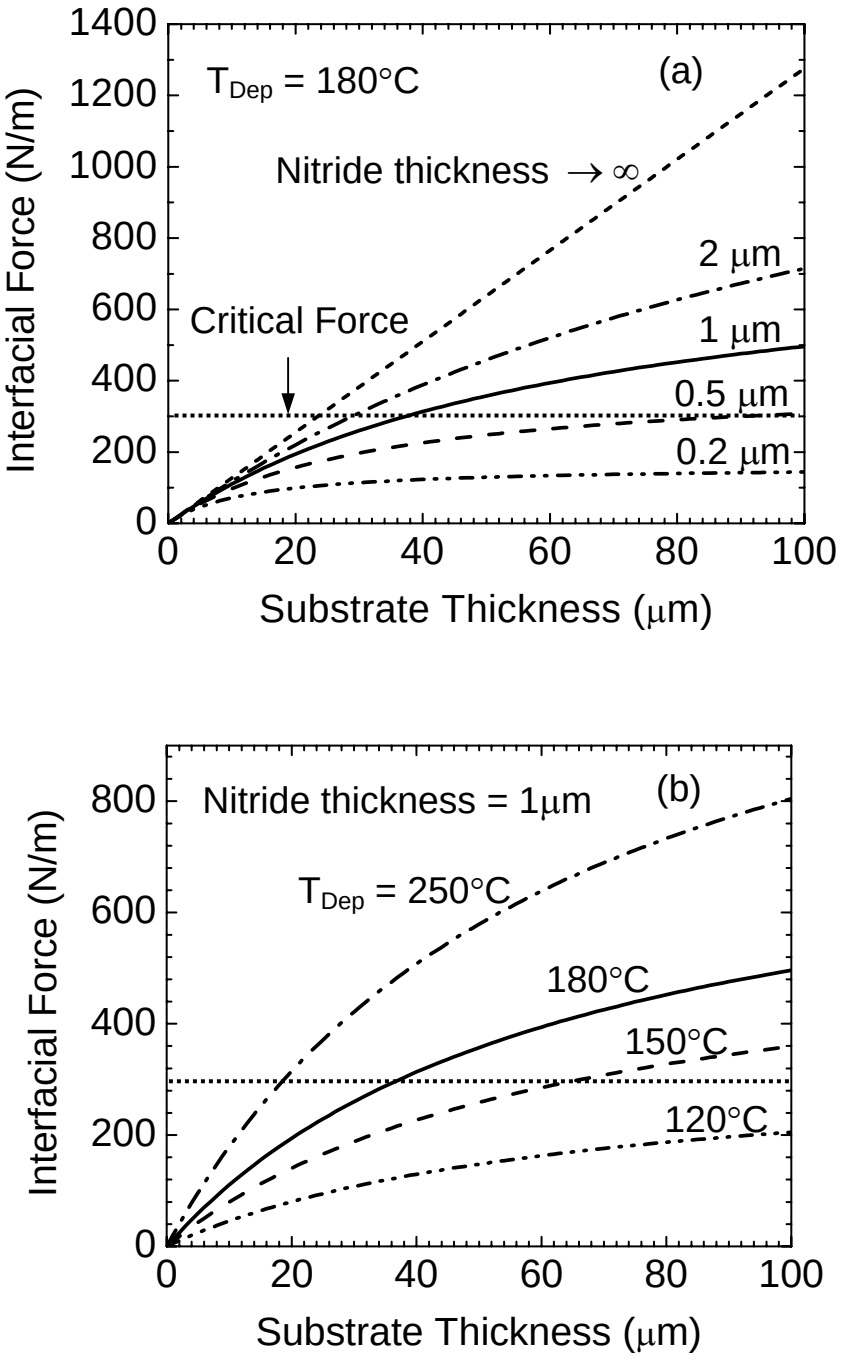


Figure 4-6. Calculated interfacial force as a function of substrate thickness for SiN_x-on-plastic substrate A (high CTE). (a) SiN_x with a range of thicknesses deposited at 180°C; (b) 1-μm-thick SiN_x deposited over a range of temperatures.

nitride can be deposited without cracking for a substrate thickness up to 100 μm. The maximum substrate thickness decreases to 70 microns when process temperature is raised to 150°C. For the even higher temperature of 250°C the substrate thickness must be less than 20μm, which may be too thin for practical use as a free-standing substrate. Given the results shown in Fig. 4-6(b), we fabricated TFT's on 60-μm-thick substrate A at 180°C, as described in a later section.

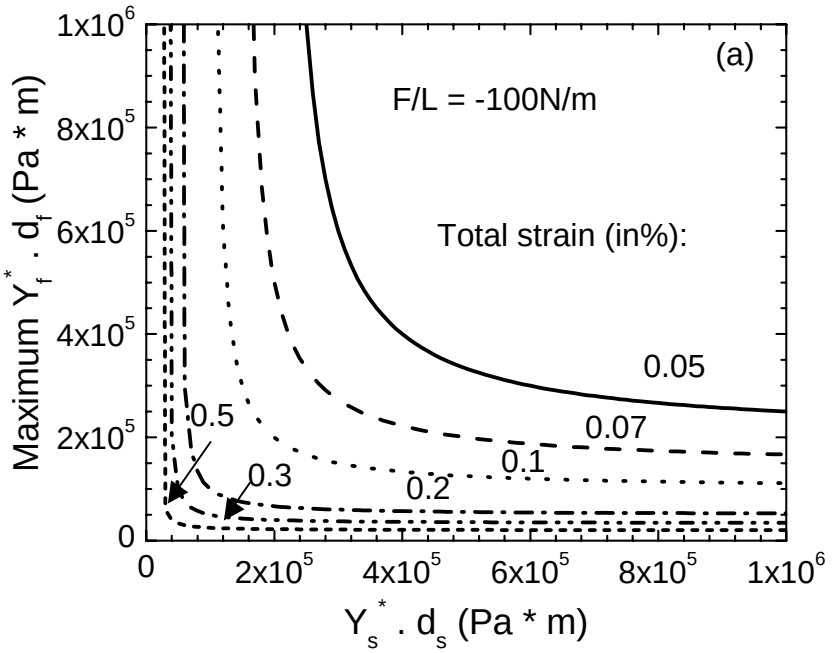
With a CTE less than 10 ppm/°C, substrate B is a better candidate to achieve one-micron crack-free device layers at a deposition temperature of 250°C, than substrate A (CTE = 45 ppm/°C). To test this conclusion, we deposited SiN_x films on Substrate B at 250 and 280°C, also with the RF power of 5W. Crack-free 1.2-μm-thick and 1-μm-thick SiN_x films were deposited on substrate B at 250°C and 280°C, respectively (Fig. 4-5(a)). The calculated interfacial force in these two films is also plotted in Fig 4-5(b). The total stress in these SiN_x films is tensile, with absolute values much smaller than those of SiN_x films deposited on substrate A.

The guidelines of Fig. 4-6(a) and (b) apply only to the substrates, device film (nitride) and parameters we used. A more generally useful relationship can be realized by plotting the maximum allowed product of the layer thickness times its biaxial Young's modulus ($d_f \cdot Y_f^*$) vs. the product of the substrate thickness times its biaxial Young's modulus ($d_s \cdot Y_s^*$), for different values of the total mismatch strain between the film and the substrate. From Eqn. (4-8), one finds:

$$Y_f^* \cdot d_f = \frac{F/L}{\varepsilon_M - (F/L)/(Y_s^* d_s)} \qquad (4\text{-}9)$$

where the total strain ε_M is calculated from Eqn. (4-4). Such relationships are shown in Fig. 4-7(a), (b) and (c) for a critical interfacial force of -100 N/m, -300N/m, and -1000N/m, respectively. In each case the allowable film thickness is reduced as the film becomes stiffer, or as the substrate thickness and/or stiffness increases. Note that for a suitably thin and soft substrate (denoted by $Y_s^* \cdot d_s^*$), there is no limit to the device film thickness. This maximum $Y_s^* \cdot d_s^*$ product increases as the allowed interfacial force increases:

$$Y_s^* \cdot d_s^* = (F/L)/\varepsilon_M \qquad (4\text{-}10)$$



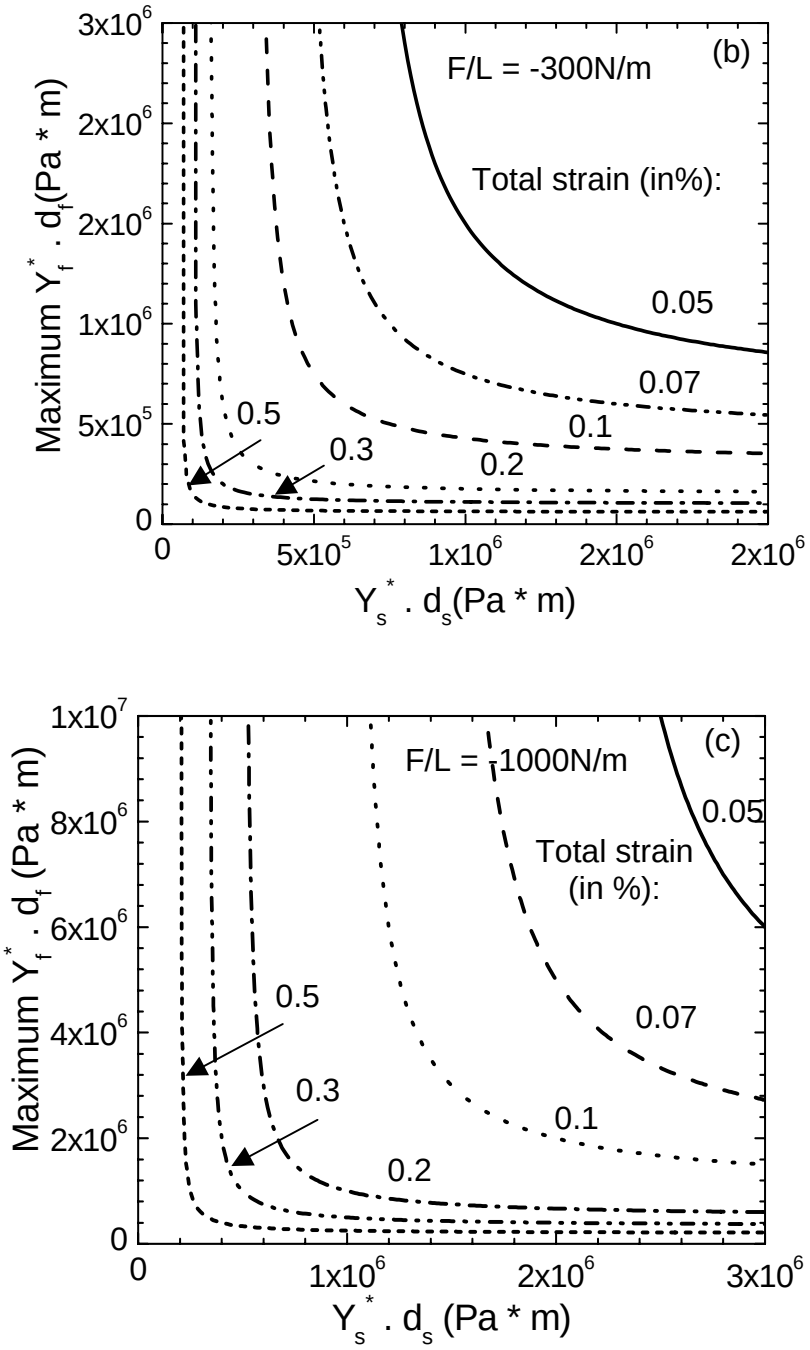


Figure 4-7. Calculated maximum allowed products of device layer thickness times its Young's modulus ($d_f \cdot Y_f^*$) vs. the substrate thickness times its Young's modulus ($d_s \cdot Y_s^*$), for a range of values of the total strain level in the film. The critical interfacial force is assumed to be (a) -100N/m (on previous page); (b) -300N/m; (c) -1000N/m.

4.3 Fabrication of Amorphous-Silicon Thin-Film Transistors at High Temperature on Clear Plastic Substrates

Fig. 4-8 shows the cross-section of the TFT structure we made on plastic substrates A and B. A thick silicon-nitride (SiN_x) buffer layer on each side of the substrate planarizes the substrate, passivates it against process chemicals and moisture, and makes the device layers adhere to the organic polymer. The TFT structure is the standard inverted-staggered structure with a bottom gate and top source/drain contacts. The TFT channel is defined by back-channel-etch. In contrast to previous work with high temperature plastic substrates that were mounted to rigid carriers for TFT fabrication [4], we kept our substrates free-standing to keep the back surface optically clean and clear. During PECVD deposition, the substrates were held in a frame which forced them to remain flat and not curl through the deposition and cool-down process. First, a 100-nm-thick chromium layer was deposited by sputtering and was wet-etched as the bottom gate electrode. A silicon nitride (SiN_x) layer, an undoped amorphous-silicon layer, and a thin highly-doped n^+ a-Si layer were deposited as the gate insulator, the active channel layer and the source/drain contact layer, respectively. They were deposited in a multi-chamber PECVD system in one run, without breaking the vacuum. Before any patterning, another 80-nm-thick chromium layer was deposited using thermal evaporation. This chromium layer was wet-etched to form the source/drain electrodes, and the n^+ a-Si layer was dry-etched with the same pattern. Then the undoped a-Si was dry-etched to define the transistor island. The TFT fabrication was finished by dry-etching windows into the

gate nitride to open access to the gate contact pads. Appendix 4 lists the PECVD recipes for the SiN_x, undoped a-Si, and n^+ a-Si deposition at different deposition temperatures.

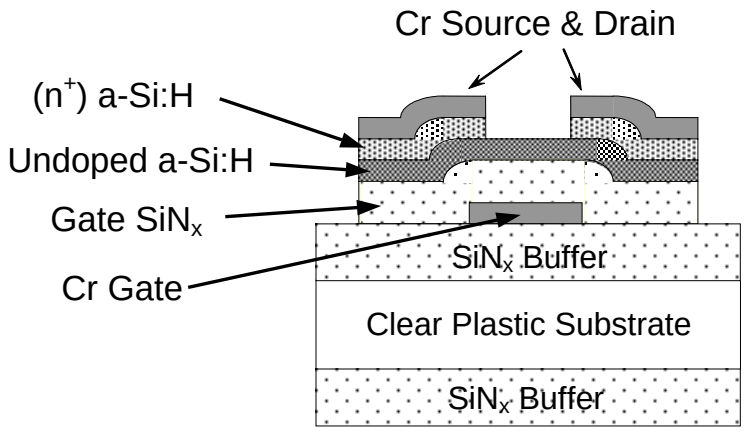


Figure 4-8. Schematic cross-section of the amorphous-silicon thin-film transistor structure on clear plastic substrates.[3]

4.3.1 A-Si TFT's on Clear Plastic Substrate A with High Coefficient of Thermal Expansion

We first experimented with clear plastic substrate A, which has the high coefficient of thermal expansion (CTE) of 45 ppm/°C. When we attempted a 250°C process on substrate A (75 μm thick), the large CTE mismatch ΔCTE produced a large stress in the device layers and cracked them (Fig. 4-9). Cracking is expected from the data and modeling presented in Section 4.2.

To prevent cracking in the device films, we followed the guidelines developed in our earlier discussion. We reduced the process temperature to 180°C, used the thinnest

substrates available (60-μm-thick) and modified the TFT device structure to decrease the total thickness of the device stack. We reduced the thickness of the front nitride buffer layer from the 500nm of the standard structure on Kapton 200E [3] to 200nm, while keeping the buffer layer on the back side 500nm thick. The thickness of the TFT layers was reduced from the standard design as follows: gate chromium from 100nm to 80nm, gate nitride from 350nm to 300nm, intrinsic a-Si from 200nm to 150nm, n^+ a-Si from 50nm to 30nm.

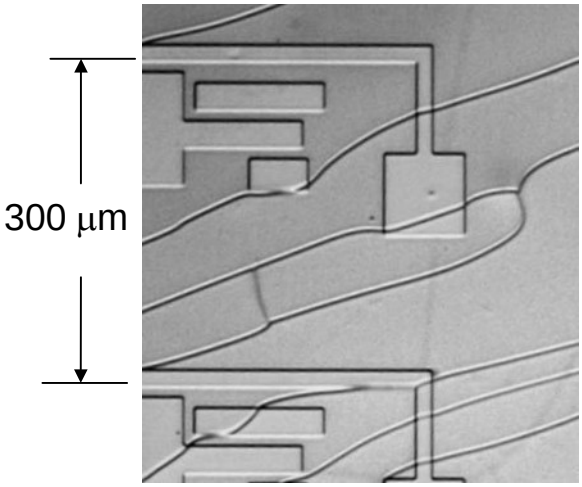


Figure 4-9. Cracks in device films deposited at 250°C on substrate A. Film thicknesses were: buffer nitride, 500nm; gate chromium, 100nm; gate nitride, 350nm; intrinsic a-Si, 200nm; n^+ a-Si, 50nm. [25]

After these modifications we successfully fabricated TFT's with very good performance on substrate A at 180°C (Fig. 4-10). For a TFT with channel width/length of W/L = 80μm/40μm, the threshold voltage is 3.2 V, the ON/OFF ratio is ~10^6 with gate

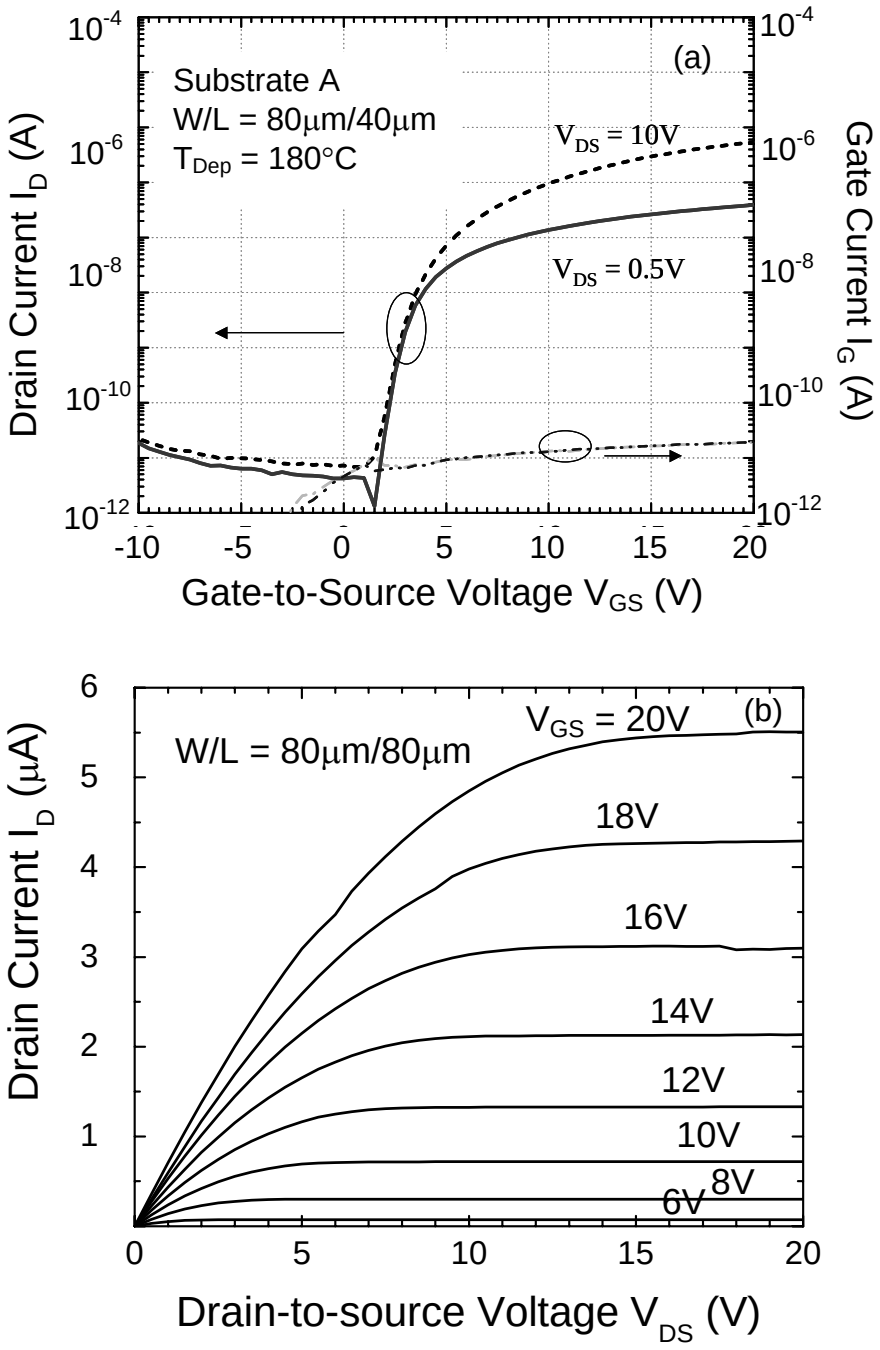


Figure 4-10. (a) Transfer and (b) output characteristics of TFT's processed at 180°C on clear plastic substrate A.

voltages varied from –10V to 20V, the linear mobility is 0.67cm^2/Vs and the saturation mobility is 0.55 cm^2/Vs. The source-gate leakage current is smaller than 20 pA, and is dominated by instrumentation. The mobilities were calculated from Eqn. (3-5) and (3-9), and not corrected for series resistance. The mobility increases at longer channel length, presumably due to series resistance adversely affecting the short channel devices (Fig. 4-11).

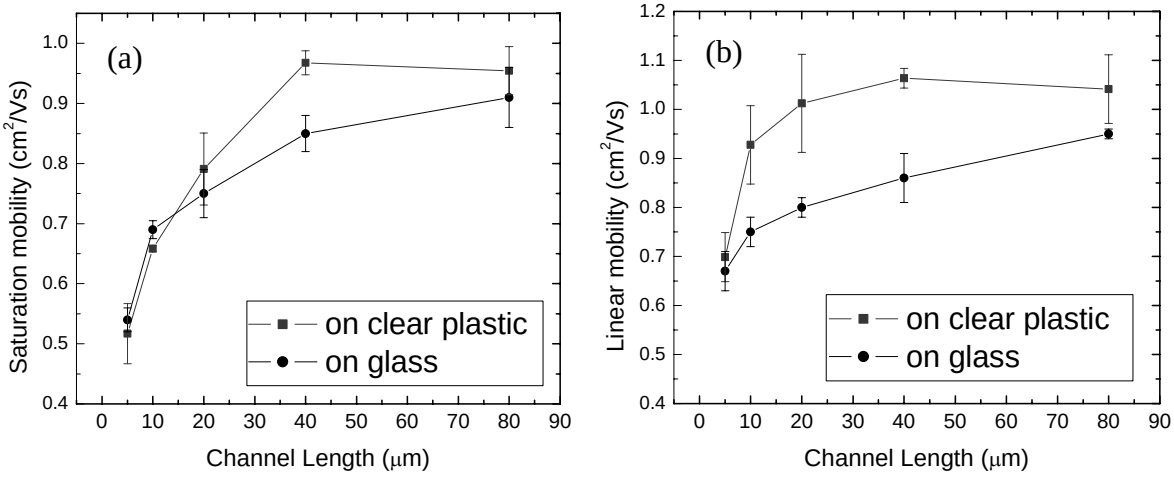


Figure 4-11. Mobility vs. channel length for a-Si:H TFT's fabricated at 180°C on clear plastic substrate and on glass, for devices with a width of 80μm. (a) Saturation region; (b) Linear region.

Control samples were also made on glass (Corning 1737) substrates with the same deposition temperature of 180°C. The TFT structure and fabrication process on glass were the same as those on plastic except that there were no buffer layers needed on the

glass substrate. For an 80μm/5μm TFT on glass, the threshold voltage is 2.0 V, the linear mobility is 0.70 cm^2/Vs and the saturation mobility is 0.67 cm^2/Vs (Fig. 4-12). These are similar to those on the plastic substrates, as were the other device parameters. As was the case for the TFT's on plastic, both the linear and saturation mobilities (uncorrected for series resistance) increase with channel length. Both the linear and saturation mobilities of TFT's made on clear plastic substrate tend to be higher than those made on glass substrates at the same process temperature of 180°C (Fig. 4-11). The reason for this difference is not known. It might be a lower series resistance in devices on clear substrates than on glass. The mobility extracted from I-V data increases for long channels, presumably because series resistance reduces the extracted mobility value more strongly for short channel devices (the mobilities of Fig. 4-11 are not corrected for series resistance).

At a process temperature of 250°C, the device films still cracked seriously with the modified structure. This is not surprising given that Fig. 4-5 reveals that only 0.2μm of SiN_x can be deposited without cracking, which is too thin for TFT fabrication. This is an instance where the maximum process temperature is not limited by the glass transition temperature (T_g) of the substrate, but by the CTE mismatch between the substrate and the device layers.

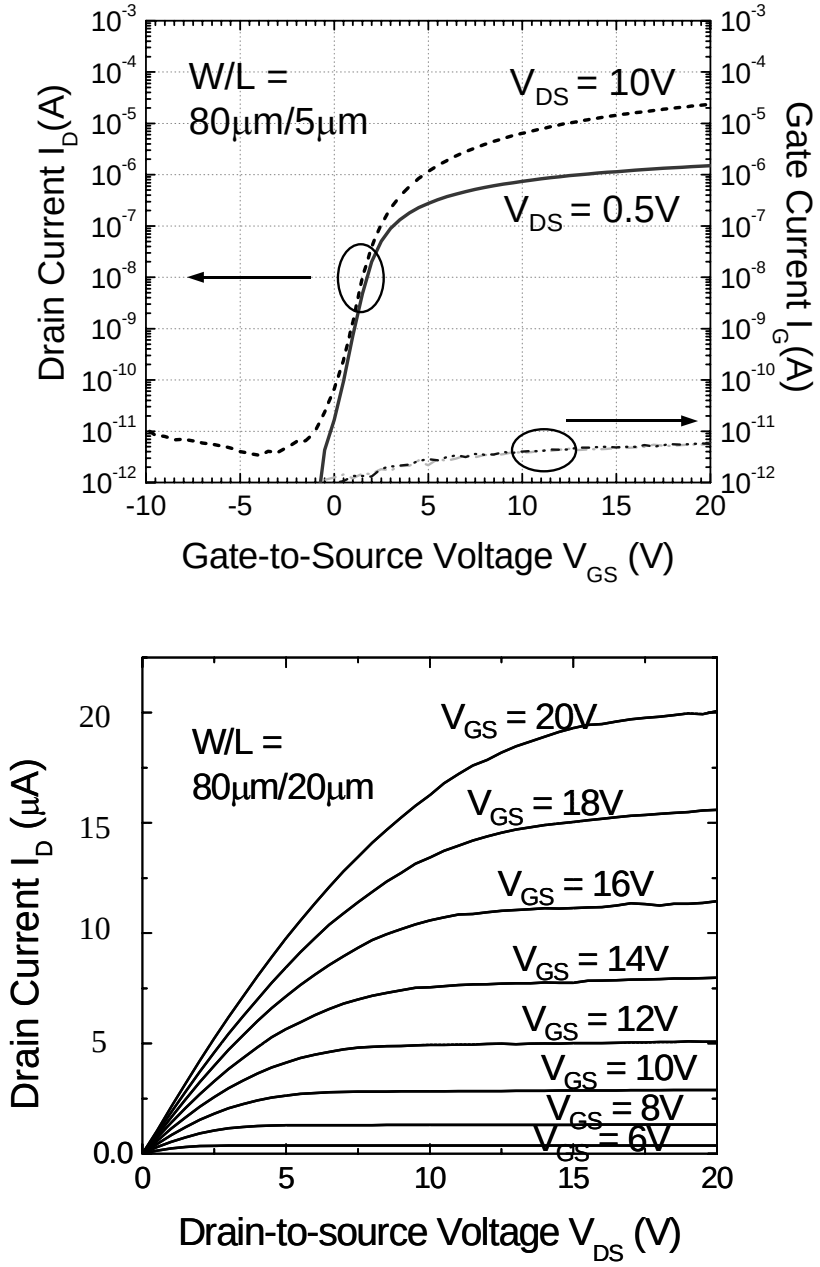


Figure 4-12. Transfer (a) and output (b) characterizations of a-Si TFT's made on glass with a maximum process temperature at 180°C.

4.3.2 A-Si TFT's on Clear Plastic Substrate Fabricated at Temperatures up to 280℃

To increase the TFT process temperature, we used the second experimental clear plastic substrate B. Because substrate B has a coefficient of thermal expansion of ≤ 10 ppm/°C, it allowed thick SiN_x films (>1μm) to be deposited without cracking at 250°C and 280°C (Fig. 4-5).

We successfully fabricated TFT's on substrate B at these maximum process temperatures of 250°C and 280°C. These deposition temperatures are desirable, because they lie close to the standard industrial process temperatures of 300-350°C. A 200nm SiN_x buffer layer was used on each side of the plastic substrate. The device layer thicknesses were: gate chromium 80nm, gate nitride 250nm, intrinsic a-Si 200nm, n^+ a-Si 30nm.

For TFT's made at 250°C and 280°C, the threshold voltages range from 2.0V to 3.8V, the ON/OFF ratios are ~10^6 for a gate voltage swing from –10V to 20V, the subthreshold slopes are about 500mV/dec, the source-gate leakage is 4 to 10 pA at V_{GS} = 20V (which is limited by the instrumentation). The electron mobilities in TFT's made at 280°C are slightly higher than those made at 250°C. In TFT's with gate width/length of W/L = 80μm/40μm, the average saturation mobility is 1.1 cm^2/Vs for 280°C TFT's vs. 0.8 cm^2/Vs for 250°C TFT's. The transfer and output characteristics of a-Si TFT's made on substrate B at 280°C are shown in Fig. 4-13. It is evident that the process temperatures of 250°C and 280°C on substrate B produce TFT's with higher mobility and lower threshold voltage than the 180°C process on substrate A.

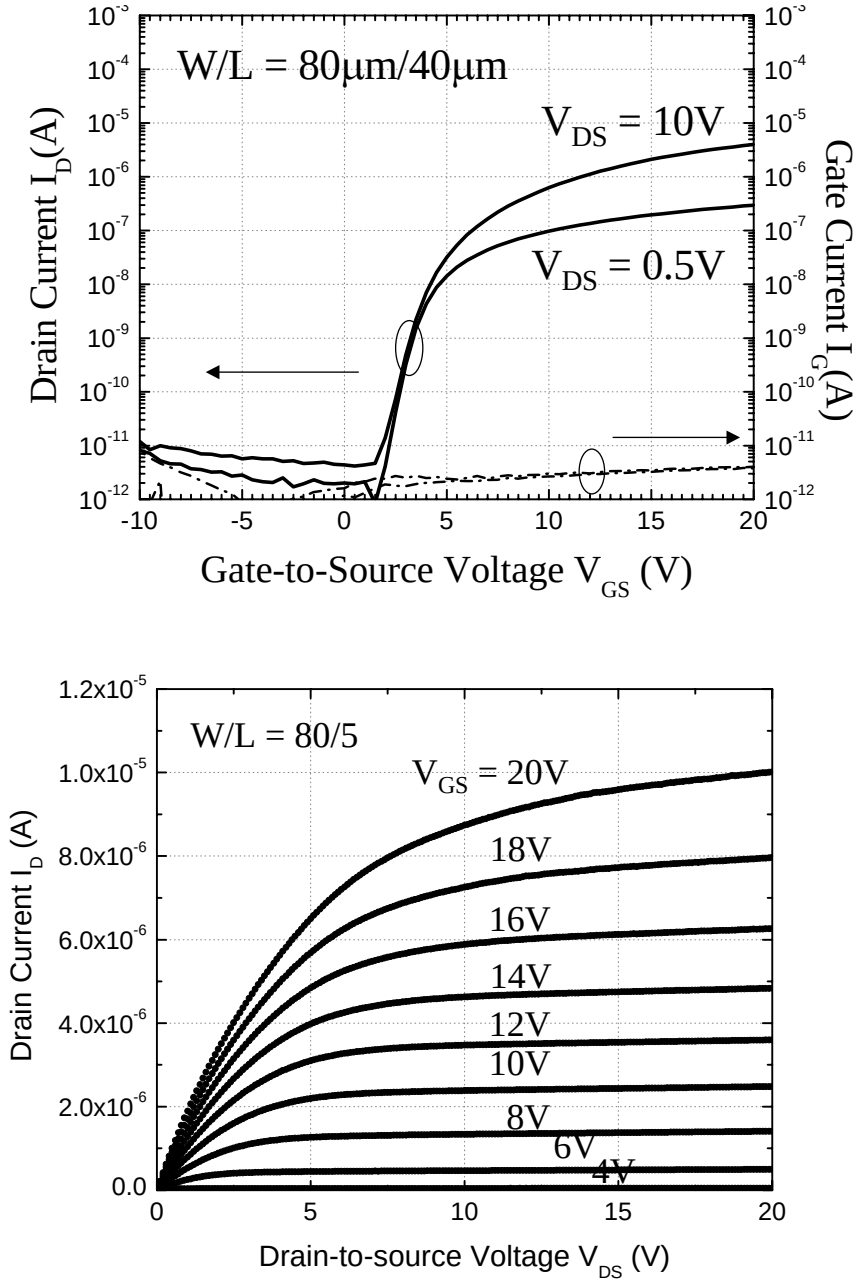


Figure 4-13. (a) transfer and (b) output characteristics of TFT's on free-standing clear plastic substrates, made at a maximum process temperature of 280°C.

Fig. 4-14 compares the mobilities and leakage current of TFT's fabricated over the range of maximum process temperatures from 130°C to 280°C. Evidently, raising the process temperature raises the field effect mobility and reduces the leakage current. Increasing the process temperature from 130°C on PEN (Fig. 4-2) to 280°C on the clear plastic substrate B increased the mobility from 0.3 cm^2/Vs to 1 cm^2/Vs, and reduced the leakage current by at least 2 orders of magnitude. Moving from a maximum process temperature of 150°C to 250°C also greatly increased the device stability, which will be discussed in next section.

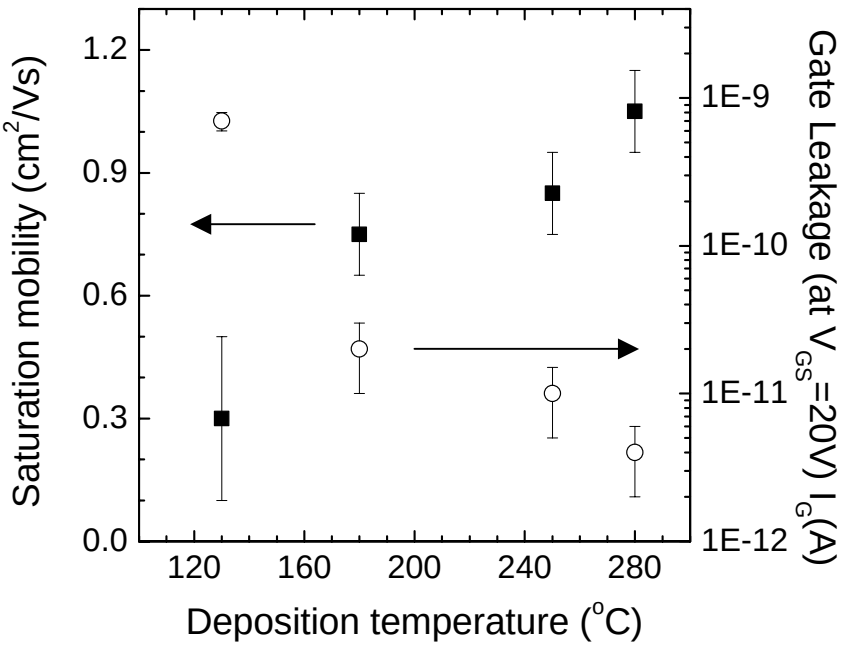


Figure 4-14. Saturation mobilities and gate leakage currents of TFT's made at different maximum process temperatures. Size of the TFT's are W/L = 80μm/40μm. [25]

4.4 Increased TFT Stability on Clear Plastic Substrates with High Process Temperatures

TFT stability is a key issue for active matrix displays, especially for active matrix OLED displays that require current driving with TFT's operating in DC mode. The threshold voltage of a-Si TFT's changes with the application of the gate bias voltage, because of carrier trapping in the silicon nitride gate insulator and the creation of new dangling bonds in the a-Si channel [18][19]. The experimental formulation of this threshold voltage shift, ΔV_T, as a function of temperature T, stress time t, and stress gate voltage V_g, is given by

$$\Delta V_T = \pm C\left|V_g\right|^{\beta} t^{\gamma} \exp(-E_a / kT) \qquad (4\text{-}11)$$

where the sign on the right hand side corresponds to that of the gate bias. E_a is the activation energy, C is a constant, and β and γ are exponents that describe the voltage and tie dependence. β is in the range of 1-2 for a positive gate bias and 3-4 for a negative gate bias. γ varies from 0.3 to 0.5 depending on the device parameters and bias polarity. The activation energy E_a lies in the range of 0.20-0.35 eV [20][21].

We performed gate voltage stress tests on the 250°C TFT's fabricated on clear plastic substrate B described in the previous section, with drain and source grounded. For comparison, control devices made at 150°C on clear plastic substrate A and at 150°C and 250°C on glass were also tested. To the best of our knowledge, this is the first time te reliability of a-Si TFT's on clear plastic have been reported. The transfer characteristics of a TFT made on clear plastic at 150°C before and after gate stress at 20V for 600 sec is

shown in Fig. 4-15. The threshold voltage shift of the TFT is calculated from this change of transfer characteristics.

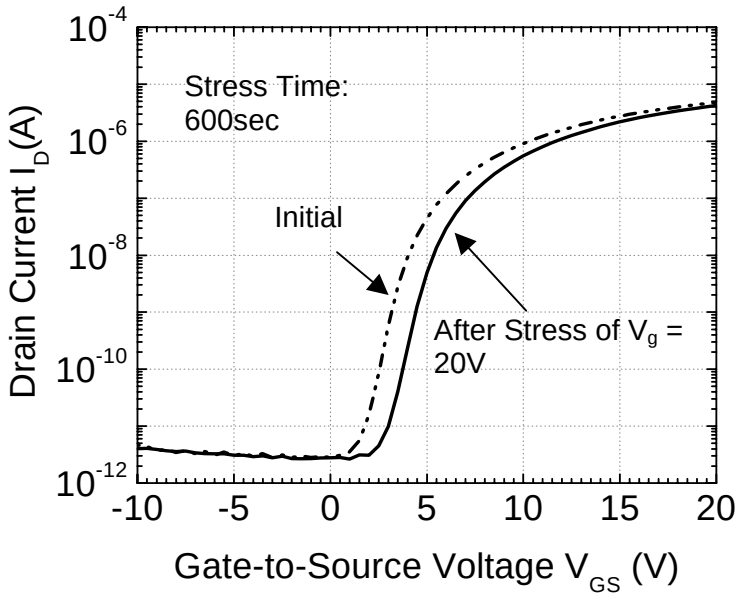


Figure 4-15. Transfer characteristics of a-Si TFT made at 150°C on clear plastic before (dotted line) and after (solid line) gate bias stressing at 20V for 600sec at room temperature. Size of the TFT is W/L = 80μm/20μm.

We first stressed the TFT's at different gate voltages for a fixed period of 600sec. The transfer characteristics of the TFT's were measured after each stress test to obtain the threshold voltage shift. With the same stress condition, the threshold voltage shift ΔV_T is smaller in TFT's made at 250°C than those made at 150°C. That the TFT stability is a function only of process temperature and practically not of substrate type is clearly evident from Fig. 4-16. The stressing does not substantially alter the mobility and leakage current of the TFT's (Fig. 4-17). The thicknesses of the gate nitride are different in the TFT's made at the two different temperatures, so the stress electric field instead of

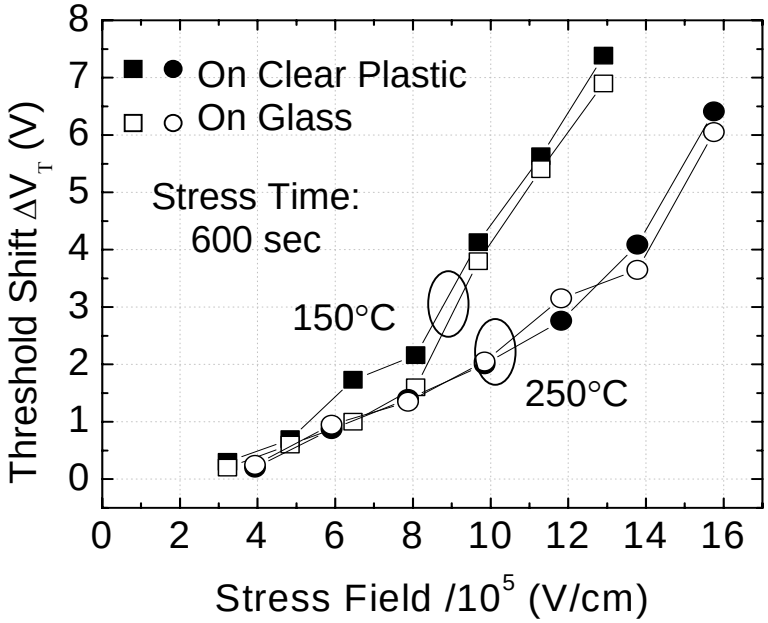


Figure 4-16. TFT threshold voltage shift after gate stressing at room temperature for 600 seconds, as a function of gate stress field, for clear plastic (closed symbols) and glass (open symbols) substrates. Circles are for 250°C process, squares are for 150°C process.

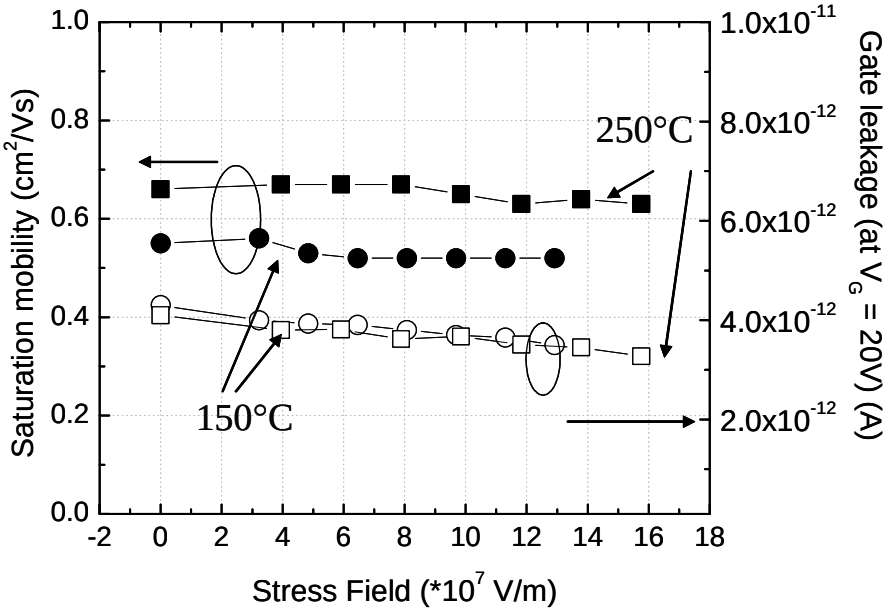


Figure 4-17. TFT saturation mobility (closed symbols) and gate leakage current (open symbols) after gate stressing at room temperature for 600 seconds, as a function of gate stress field. Circles are for 150°C process, squares are for 250°C process. Size of the TFT's are W/L = 80μm/20μm.

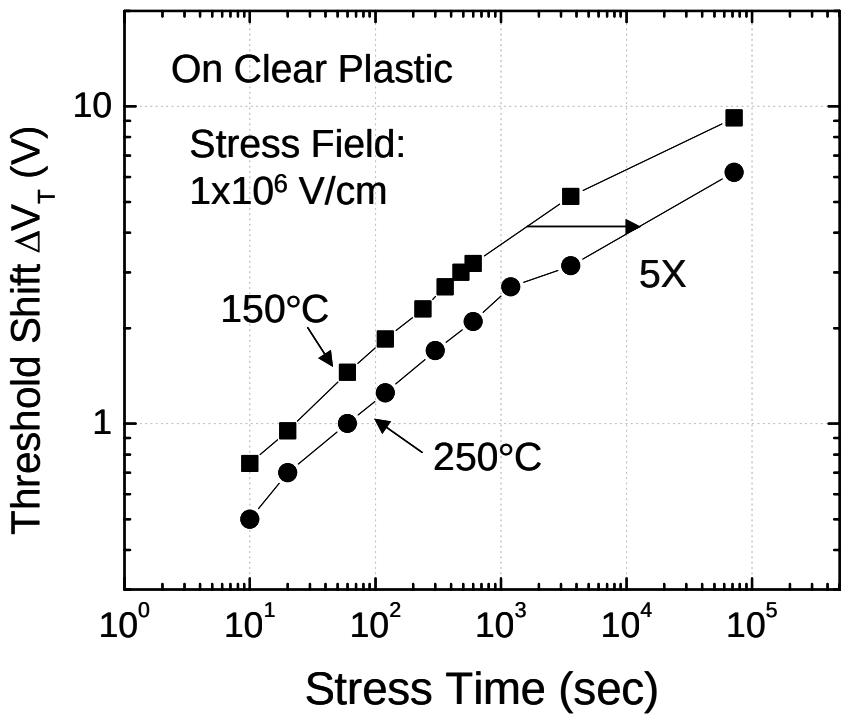


Figure 4-18. TFT threshold voltage shift vs. stress time at constant gate bias for TFT's made at 150°C and 250°C on clear plastic. [26]

voltage is used as the x-axis. The thickness of the gate nitride is determined by measuring the capacitance of the test capacitor: $t_{SiNx} = C/A\varepsilon_0\varepsilon_{SiNx}$, where A is the area of the test capacitor. The gate nitride thickness is 300nm for the 150°C process and 250nm for the 250°C process. The stress field can then be calculated from the stress voltage as: $E = (V_G - V_S) / t_{SiNx}$.

Separately, TFT's made on clear plastic substrates at 150°C and 250°C were stressed for up to 24 hours at the same gate bias electric field of 10^6 V/cm. The log-log plot of threshold voltage shift vs. stress time is shown in Fig. 4-18. According to Eqn. 4-11, the linear fitting of these 2 curves gives γ of 0.29 and 0.28 for 150°C and 250°C

TFT's, respectively. The nearly uniform lateral shift of the ΔV_T data of shows that the lifetime in 250°C devices is a factor of about five longer than in 150°C devices.

We now compare our stability results to literature data for a-Si TFT's processed at higher temperatures on glass (300-360°C). Fig. 4-19 shows the threshold voltage shift after 600 sec of stress as a function of stress field for our 150°C and 250°C TFT's on clear plastic, for TFT's on Kapton® 200E polyimide from our lab made at 150°C [21], and TFT's made at temperatures of 300-360°C on glass [19][23][24]. All data closely follow straight lines on a log-log plot, with slopes of ~2 [18][19]. TFT's made on Kapton® E at 150°C in our lab [22] about 5 years ago give results almost identical to our 150°C TFT's on clear plastic, suggesting a stable fabrication process. The 250°C devices on clear plastic

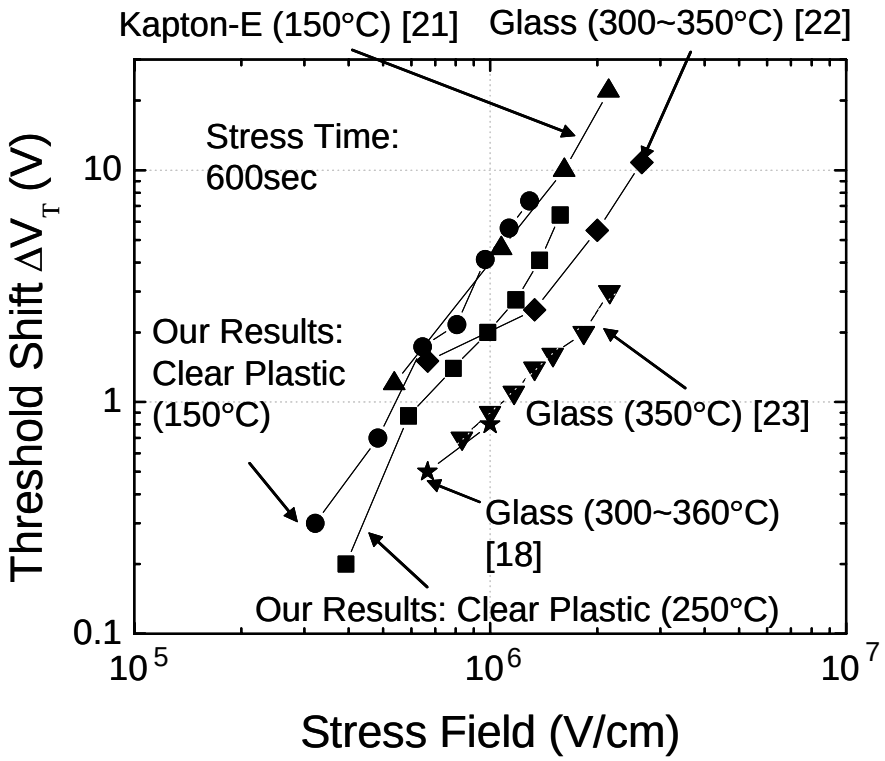


Figure 4-19. TFT threshold voltage shift as a function of gate electric field, held constant for 600sec. Various substrates and process temperatures are labeled. [26]

are superior to the 150°C devices as discussed above. It is evident that ΔV_T is reduced when the process temperature increased because of the higher quality of SiN_x and a-Si film. The 250°C results on plastic begin to approach the 300-350°C results on glass. Further improvement is expected for TFT's fabricated on clear plastic at 300°C.

4.5 Conclusion

The mechanical interaction of a silicon nitride layer (which represents the TFT stack), and a plastic substrate is studied to develop design guidelines that avoid cracking during TFT fabrication. Experiments show that the TFT films crack when the film stress per unit length exceeds a critical interfacial force. The film stress developed in the device stack can be reduced by controlling the built-in strain of the PECVD nitride into tension, by reducing the thickness of the device stack, using thin substrates, and by using a substrate with a small coefficient of thermal expansion. The PECVD deposition power can be used to control the built-in strain in the SiN_x film, and compensate for the thermal mismatch strain. This method was then used to successfully fabricated a-Si TFT's on experimental clear plastic substrates with a maximum process temperature of up to 280°C. The TFT's made at high temperatures have higher mobility and lower leakage current, and are more stable than TFT's made at low temperatures on conventional low-T_g clear plastic substrates.

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CHAPTER 5

A-SI TFT BACKPLANES ON CLEAR PLASTIC AND GLASS SUBSTRATES FOR AMOLED

Active matrix OLED displays (AMOLED's) have wider applications than passive matrices because AMOLED's can more easily achieve high resolution, large size, and low power consumption. To date, several groups have demonstrated AMOLED's on glass substrates driven by amorphous-silicon transistor backplanes with very good performance [1,2].

AMOLED on flexible plastic substrates are very attractive because of potential thin, light-weight, rugged, rollable and foldable properties. In this chapter, using the a-Si:H TFT's with a 180°C maximum process temperature developed on clear plastic substrate described in Chapter 4, we present initial pixel performance on clear plastic and on glass substrates and integrated polymer LED's on glass. Compared to previous work on

TFT-OLED on clear plastic at low temperature(120°C) [3], our results show that 180°C a-Si TFT's on plastic or glass substrates can provide adequate drive current for bright light emission at low driving voltages and have the necessary low leakage current. To the best of our knowledge, these are the best a-Si TFT OLED pixels demonstrated on clear plastic substrates.

5.1 AMOLED Backplanes with 180°C a-Si TFT's

5.1.1 *Design of 180℃ a-Si TFT AMOLED backplane*

The AMOLED pixel circuit design (Fig. 5-1) is the simple 2-TFT scheme. T1 is the switching TFT, whose function is similar to the one in an AMLCD pixel, and controls writing and holding of the data signal (V_{DATA}) to the storage capacitor (V_{STORE}). T2 is the driving TFT, which provides current to drive the OLED to the desired brightness according to the data voltage on its gate. The data voltage (V_{DATA}) is stored on the capacitor (V_{STORE}) to drive T2.

We now estimate the W/L ratio required of the driving transistor for a desired pixel brightness. Note that the source of T2 is connected to the OLED anode (V_{OLED}), so the applied data voltage (V_{DATA}) is split between the OLED and T2. For a transistor under saturation, the drain current I_{DS} is:

$$I_{DS} = (W/2L)\mu_{SAT}(\varepsilon_{SiNx}\varepsilon_0/t)(V_{GS}-V_T)^2 \qquad (5\text{-}1)$$

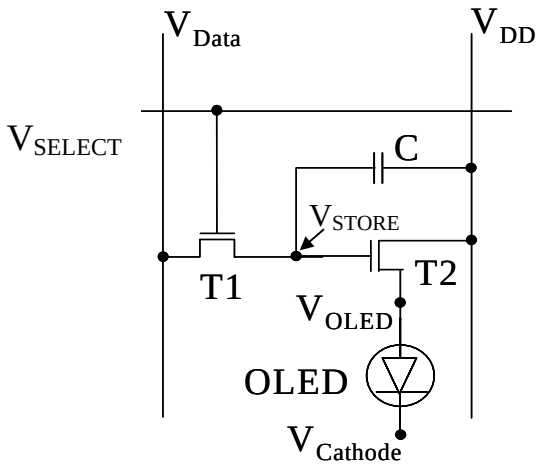


Figure 5-1. Schematic circuit of the 2-TFT pixel used in this work. T1 is the switching transistor, T2 the drive transistor, and C is the storage capacitor. The OLED anode is connected to source of T2.

where W and L are the channel width and length, μ_{SAT} is the field effective mobility in saturation, ε_{SiNx} and t are the dielectric constant and thickness of the gate nitride, V_{GS} is the gate voltage (V_{STORE}-V_{OLED}), and V_T is the threshold voltage. The relationship between the OLED drive current I and the OLED luminance L is:

$$L = \eta_0 I \qquad (5\text{-}2)$$

where η_0 is the OLED luminance efficiency.

The required gate voltage for a brightness B with a pixel of area A and polarizer efficiency η_p is then:

$$V_{GS}\text{-}V_T = (A\,B/(\eta_p(W/2L)\mu_{SAT}(\varepsilon_{SiNx}\varepsilon_0/t)))^{1/2} \qquad (5\text{-}3)$$

This is shown in Fig. 5-2, as a function of W/L of T2, for a display brightness B (luminance over area) of 100 cd/m^2 (nits), a pixel size A of 300μm x 300μm, a polarizer

efficiency η_p of 50%, an a-Si TFT mobility μ_{SAT} of 0.5cm^2/Vs, and a gate SiN_x thickness of 250nm, and assuming OLED efficiencies of 5, 10 and 15 cd/A. Our design point assumed the above parameters, an OLED efficiency of 10 cd/A, and a maximum difference of the data voltage from the OLED anode voltage (V_{DATA}-V_{OLED}) of 5V, resulting in a required W/L of T2 of 16. At this point the pixel current would be 2 μA.

5.1.2 *Fabrication of 180℃ a-Si TFT AMOLED backplane*

A 3" x 3" test sample, with several small AMOLED arrays and test structures in the center 1" x 1", was fabricated (Fig. 5-3). The area around this center was for interconnecting lines, for external connection to driver electronics and environmental sealing. Fig. 5-4 (a) is the schematic cross-section of the a-Si TFT AMOLED backplane on plastic. The a-Si TFTs were fabricated using the same structure and process as mentioned in Chapter 4. After the TFT fabrication, aluminum was deposited and patterned by lift-off as the interconnect metal. The aluminum connects different TFT's to form AMOLED circuits and forms interconnect lines and contact pads for making contact to external drivers. To avoid contact resistance from oxidation of Al by ITO, the ITO and aluminum were connected through the chromium gate metal. A thick SiN_x (500nm) layer was deposited as the passivation layer to cover the whole backplane before OLED integration. ITO was then deposited by sputtering at room temperature, and patterned by wet-etching. Another SiN_x layer was deposited on top of the patterned ITO to passivate the edge of the ITO to avoid short circuit between the ITO anode and the OLED cathode. A window was opened on top of the ITO through the SiN_x by dry-etching, to expose the

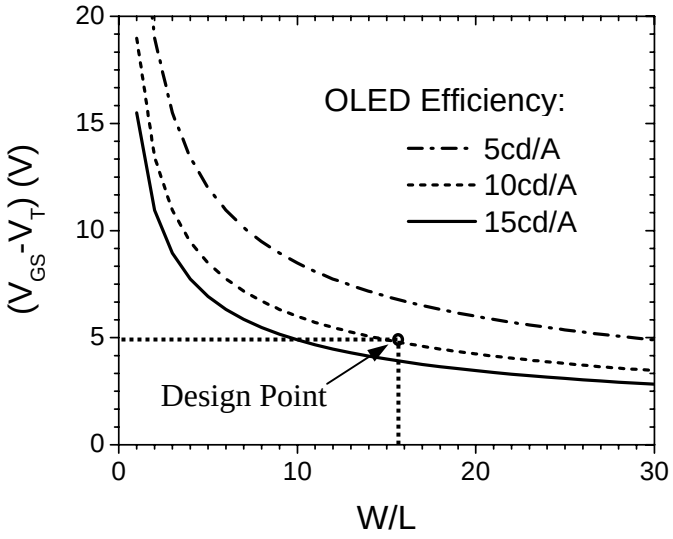


Figure 5-2. Required V_{GS}-V_T on drive transistor as a function of W/L, for various OLED efficiencies, assuming a pixel size of 300μm x 300μm, a polarizer efficiency of 50%, an a-Si TFT mobility of 0.5cm^2/Vs, and a gate SiN_x thickness of 250nm. Our design point is W/L=16, with OLED efficiency of ~10cd/A.

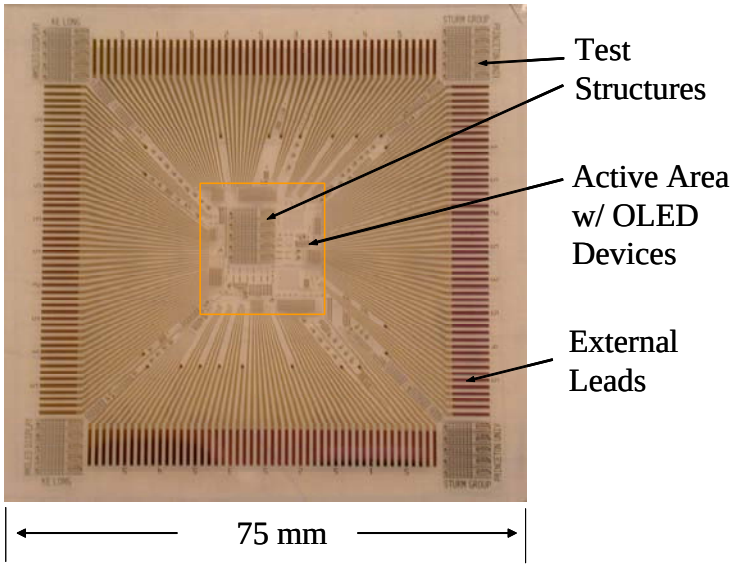


Figure 5-3. Photograph of a test sample. The TFT driving circuits are fabricated, waiting for OLED integration.

ITO for the OLED integration. Blanket organic layer deposition, and a cathode (limited by a shadow mask to the central area) completed the structure.

On glass substrates, the process was similar except we started with ITO-coated glass from an external supplier. After the ITO was patterned by wet-etching, a 100-nm thick SiN_x was deposited using PECVD to protect the ITO from the TFT process. After that the TFT structure and interconnect metal were fabricated and covered by thick SiN_x. Then the ITO was exposed and the OLED was integrated (Fig. 5-4(b)). Fig. 5-5 is a micrograph of a pixel in the array before OLED integration. The size of one pixel is 300μm x 300μm. T1 was implemented as two TFT's with width/length of 20μm/5μm in series for insuring a low leakage current [4]. T2 had width/length of 80μm/5μm, and its source connected to the anode of the OLED. The storage capacitance was about 2pF. The capacitor was formed between the gate matel and the interconnect metal with a dielectric of the gate nitride and the intrinsic silicon. The fill factor of the pixel is about 46%. It was limited by the minimum linewidth of our design, which is 5μm.

5.2 Testing of the AMOLED backplane before OLED integration

5.2.1 *Current Drivability*

Before the OLED was deposited, we tested the drive current generated by a pixel by applying DC control voltages to pixels on both plastic and glass substrates. A fixed V_{DD} of 20V was applied to the drain of the driving transistor T2. The source of T2 (future OLED anode) was connected to ground. We scanned the data voltage (V_{DATA}) from

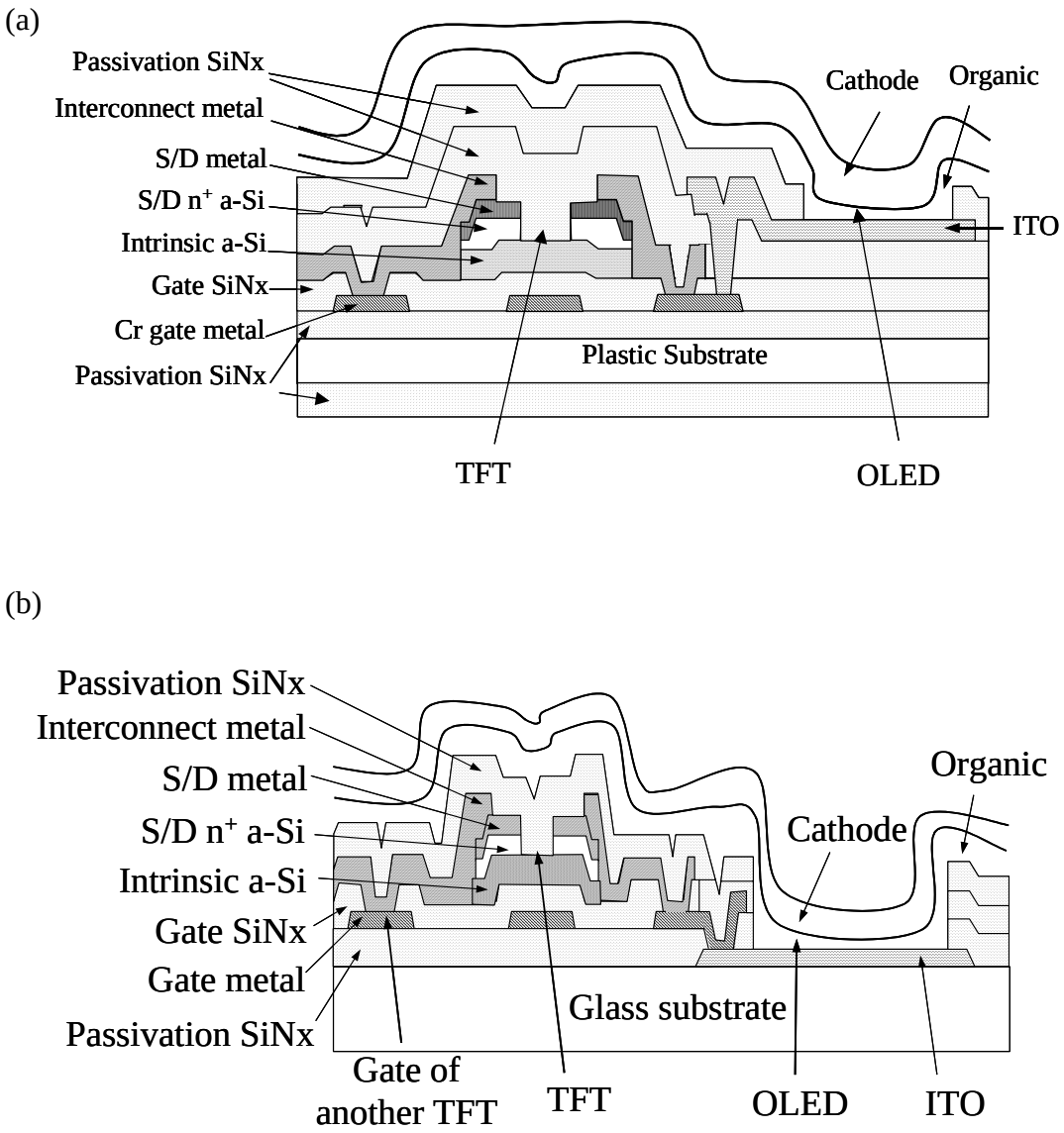


Figure 5-4. Schematic cross-section of the TFT-OLED integration (a) on clear plastic substrate and (b) on glass substrate.

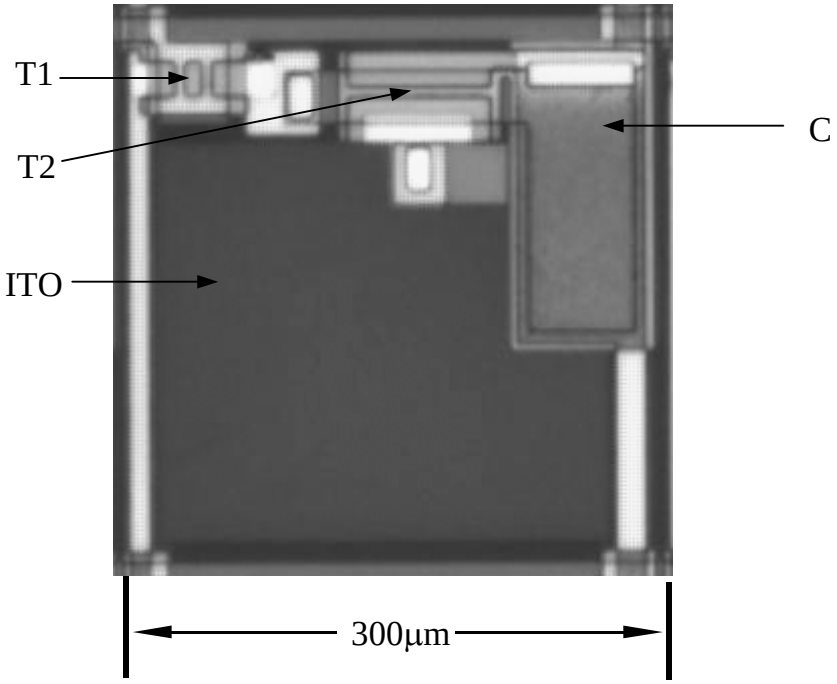


Figure 5-5. Micrograph of a pixel in a 2-TFT AMOLED array before OLED integration. T1 is the switching transistor, T2 the drive transistor, and C is the storage capacitor. The patterned ITO will become the anode of the OLED.

0 to 20 volts, and stepped the voltage on the gate of T1 (V_{SELECT}) as 5V, 10V, and 15V. The current flowing through T2 is measured as the pixel current (Fig. 5-6(a) for pixel on plastic). As V_{DATA}-V_{OLED} is increased, the pixel current increases as expected, with T2 in saturation. In this region Equation (5-1) describes the pixel current. For large V_{DATA}-V_{OLED}, the current saturates, because T1 limits the charging of the storage capacitor (controlled by V_{SELECT}). The open circles are the circuit simulation results using H-SPICE and an a-Si TFT model. In the simulation, threshold voltage V_T = 3.5V, mobility

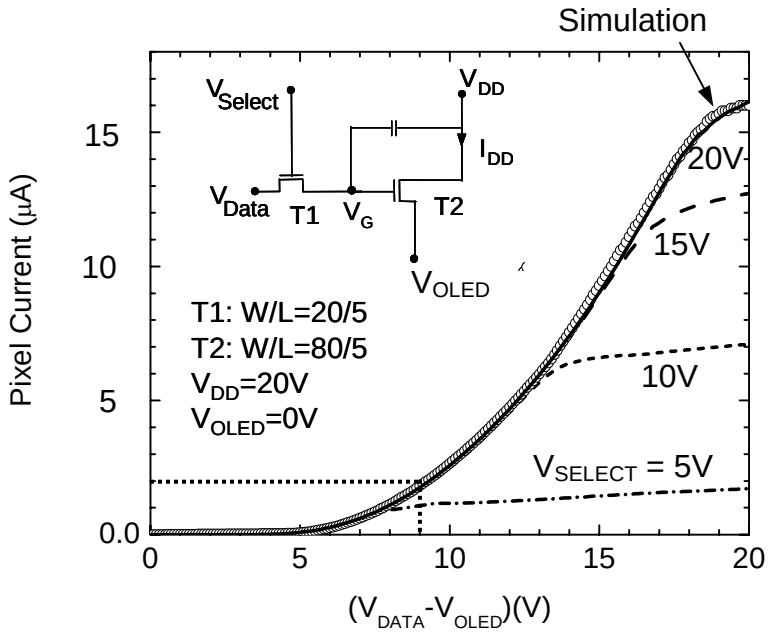
$\mu = 0.80 cm^2/Vs$ for T1 and $V_T = 4.5V$, $\mu = 0.65 cm^2/Vs$ for T2 were assumed, which are consistent with the measured TFT results in Chapter 4. And the gate dielectric is 300nm thick silicon nitride with dielectric constant as $\varepsilon_{SiNx} = 7.4$. The simulation results agree well with the measured data. For the desired pixel current of 2 μA for 100 cd/m^2 display brightness (assuming an OLED efficiency of 10 cd/A), a V_{DATA}-V_{OLED} of only 9V is required, corresponding to V_{GS}-V_T = 4.5V on T2. This result is close to the design point of the previous section ($V_{GS} - V_T = 5V$), showing that the 180°C a-Si TFT's backplane on clear plastic substrates provides sufficient drive current for AMOLED application.

Similar results were found on glass substrates (Fig. 5-6(b)). In this case modeling parameters of $V_T = 2.0V$, $\mu = 0.7 cm^2/Vs$ for both T1 and T2 were used to fit the data. On the glass substrate, the V_{DATA} - V_{OLED} needed to get 100 nits brightness (~2μA of drive current) is only 6V, corresponded to $V_{GS} - V_T = 4V$ on T2. This is lower than the design goal of 5V (Fig. 5-2) due to the higher experimental mobility of 0.7 cm^2/Vs vs. the earlier conservative assumption of 0.5 cm^2/Vs.

5.2.2 *Data storage and leakage current*

An important property of an AMOLED pixel is its ability to hold the data signal programmed into it through a frame time. To test this storage ability of the a-Si TFT backplane, before OLED integration, we connected a 1MΩ resistor in place of the OLED in a test pixel on a glass substrate, so we could use the voltage drop across it as a measure

(a)



(b)

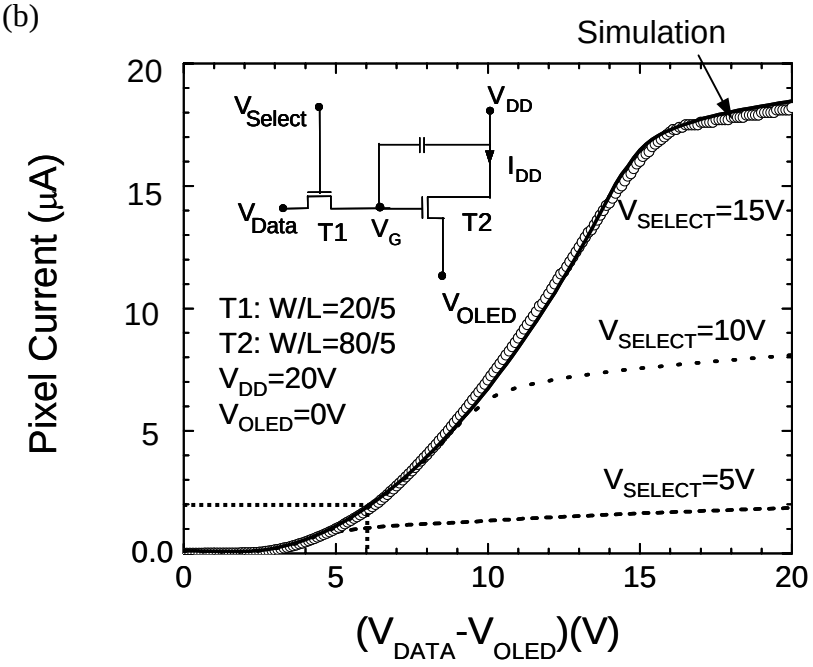


Figure 5-6. DC drive current as a function of data voltage tested a 2-TFT pixel before OLED integration on (a) clear plastic and (b) glass substrates for different select voltages. The open circles are simulation results using H-SPICE. The data voltage needed for 100nits display brightness (2 μA pixel current) is also labeled with dotted line.

of the drive current (Fig. 5-7). With V_{DD} (drain of T2) of 24V, pulse signals as V_{DATA} and V_{SELECT} were applied with different frame times to test the data storage of the pixel. During one frame time, the programmed V_{DATA} should be stored as V_G. If there is a leak in T1, or if the gate nitride is leaky, the gate voltage will decrease, which can be observed as a drop in the voltage over the resistor due to decreased current in T2. Fig. 5-8 shows the waveform of V_{DATA}, and V_{SELECT} applied to the pixel and the measured voltage drop on V_{OLED} on a multi-channel oscilloscope. The SELECT signal went from –10V (OFF) to 20V (ON), with a pulse width of 20μs. The DATA signal went from 0 (OFF) to V_{DATA} (ON), with a pulse width of 40μs. Fig. 5-9 shows the time-averaged V_{OLED} (proportional to drain current) as a function of V_{DATA} with different frame times. On a scale of volts, no difference of V_{OLED} could be detected with different frame times of 4ms, 8ms and 16ms, showing that any loss of data voltage during a frame time is very small. (A 16ms frame time and ~60μs row time are characteristics of QVGA display timing.) Directly observed on an oscilloscope, there is a slight voltage drop on V_{OLED} during a frame time (Fig 5-8). Voltage drops of V_{OLED} as 80mV, 120mV and 160mV were observed for frame times of 4ms, 8ms, and 16ms. With the storage capacitor of 2 pF, this places an upper limit on the leakage current through T1 of 2×10^{-11}A. This is in agreement with the TFT leakage current under reverse gate bias of –10V, which is ~10^{-11}A as shown in Fig. 4-10(a). While the exact voltage decay allowed in an application depends on the number of bits of gray scale, the observed decay shows that the 180°C process provides leakage currents low enough for most applications. This low leakage current is a crucial advantage of those 180°C TFT's on clear plastic over those shown earlier on other substrates with lower process temperatures [5][6].

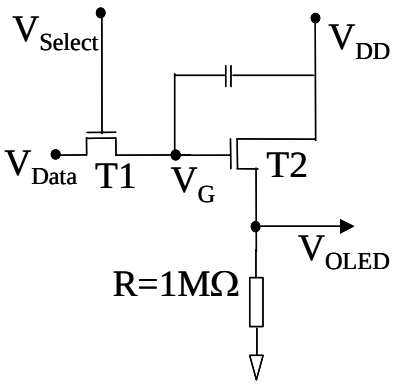


Figure 5-7. Schematic circuit for dynamic testing of pixels before OLED integration, with OLED replaced by a 1MΩ resistor for current monitoring.

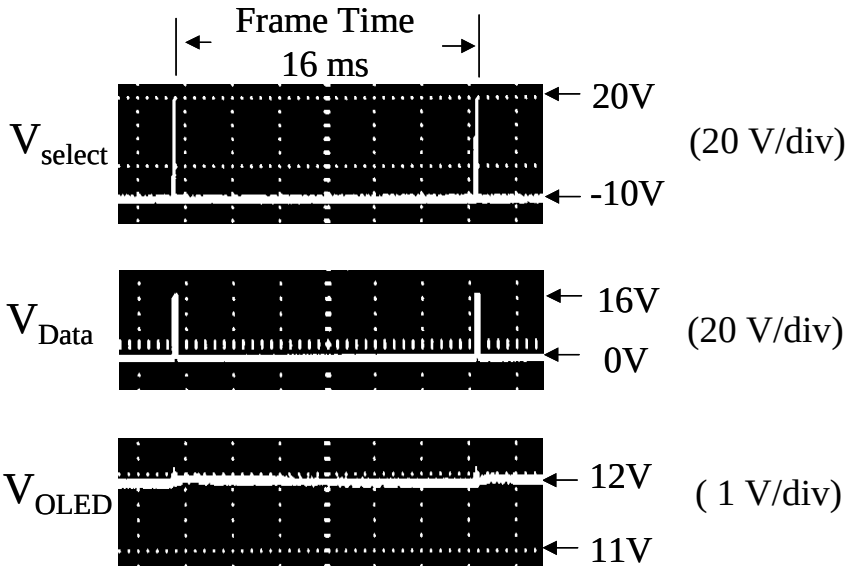


Figure 5-8. Applied data signal, applied select signal and V_{OLED} (proportional to drive current) vs. time shown on a multi-channel oscilloscope. The scale of each signal on the oscilloscope is also shown.

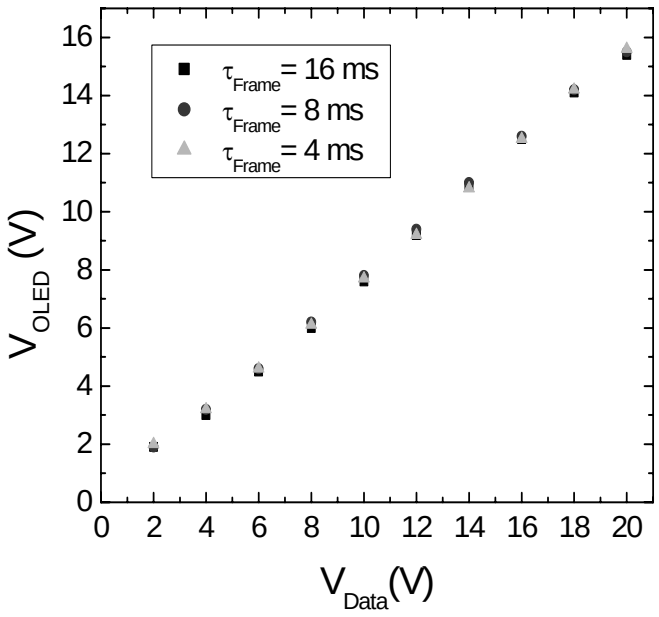


Figure 5-9. Stored voltage at the OLED node as a function of input data voltage for different frame times of 4ms, 8ms and 16ms.

5.3 AMOLED Test Array

We integrated the a-Si TFT backplane on glass with polymer OLED's to make AMOLED test arrays. The OLED integration on the two clear plastic substrates was limited by practical yield problems during the interconnect metal patterning step. After the TFT fabrication, the backplane was covered by a thick SiN_x passivation layer, which prevents the OLED cathode metal from connecting with the TFT circuits (Fig. 5-4(b)). The polymer layer and the cathode layer were un-patterned within the active region. After windows were opened in the SiNx passivation down to the ITO, a poly(3,4-ethylenedioxythiophene) (PEDOT) layer was spun on as the hole injection layer. After the drying of the PEDOT layer, a "Super-Yellow" emissive polymer (a poly(phenelene

vinylene)-type polymer from Merck) was deposited by spin-coating and dried. Finally the cathode was deposited. The organic layer and cathode were limited to the central active region, and the active area was sealed with a glass cap and epoxy for environmental stability. The contact pads at the edges of the display sample were then connected to the external driver electronics using flex cables and TAB bonding (Fig. 5-10). The TFT backplane was fabricated at Princeton University. The sample was then sent to DuPont Displays in Santa Babara, CA for OLED integration and sealing. This was done by Matt Stevenson, Gang Yu and Marie at DuPont Displays. The sample was then returned to Princeton University for testing. Appendix 5 and 6 document all the process steps of the AMOLED test array fabrication both on glass and on clear plastic substrates.

Fig. 5-11 shows a 5 x 5 AMOLED array being driven with QVGA timing with 16ms frame time and 50μs row time, at different data voltages V_{DATA}. V_{DD}, V_{SELECT} and the cathode voltage were set at 24V, 20V, and 0V, respectively. Because of the limitation of our driver electronics, all pixels were driven to the same brightness. One row contact failed, so only 4 rows are visible. The uniformity of the brightness of the pixels is visibly good. The I-V characteristics of a 250μm x 250μm test OLED, close to the area of the OLED's in these pixels, are shown in Fig. 5-12. For the target current density of 2 mA/cm^2 for a pixel brightness of 200nits before any polarizer, an OLED voltage of 5.5V is required, which adds to the data voltages in the previous section where the OLED anode contact was grounded.

A large-area photodiode was used to collect the light emitted from the array. The detected photo-current was then converted to the total luminance of the array, knowing

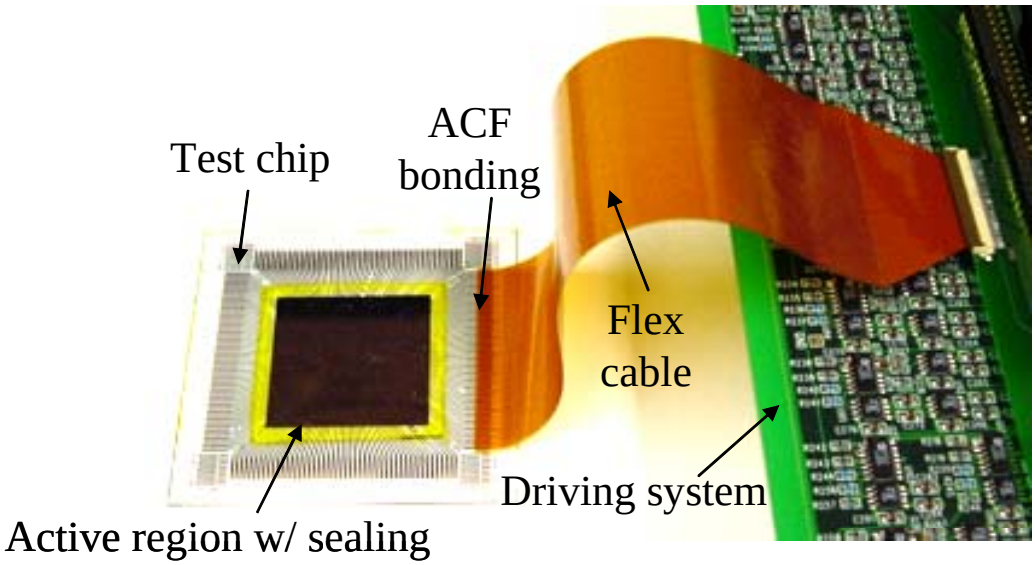


Figure 5-10. Picture of the finished test sample connected to driving system.

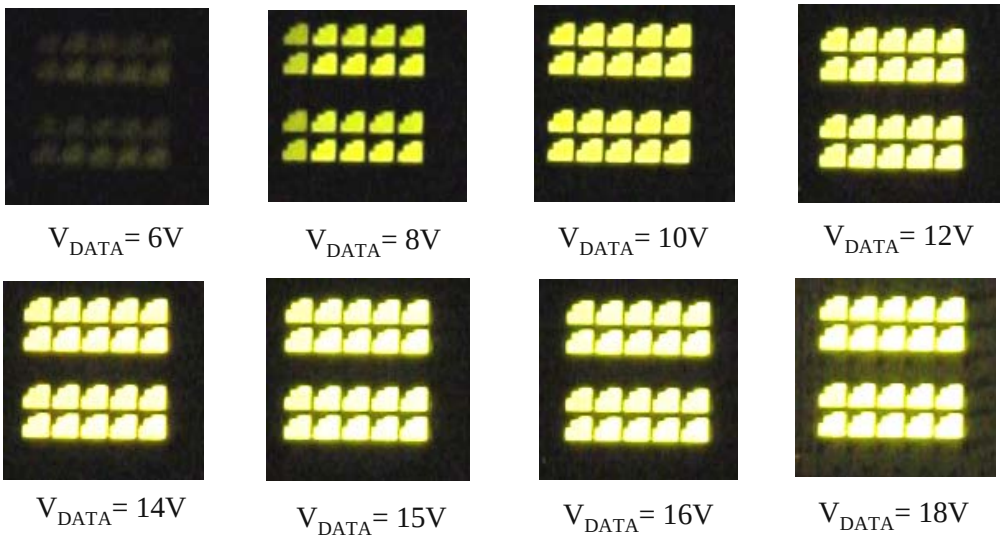


Figure 5-11. Images of a 5x5 AMOLED array (one row contact is missing) under QVGA driving with different data voltages.

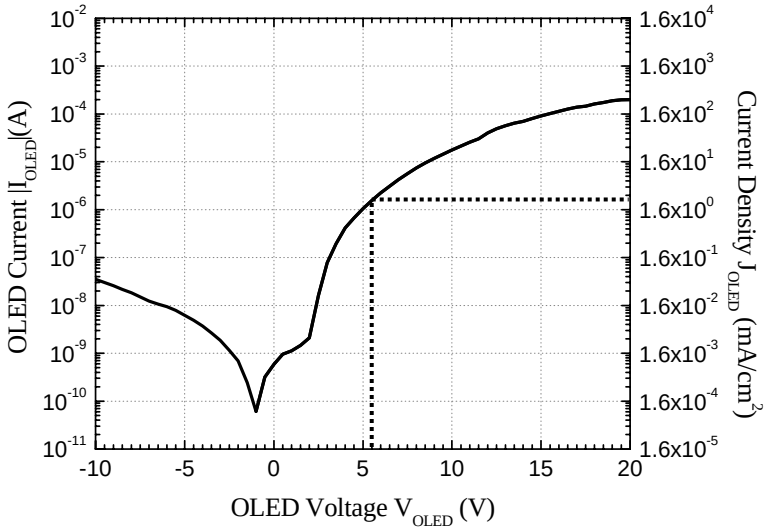


Figure 5-12. I-V characteristics of a test OLED with an area of 250μm x 250μm. Dotted lines show current density needed for 200 cd/m^2 OLED brightness.

the efficiency of the photo diode and the collection efficiency. Then the average brightness of the array was calculated using the area of the 20 working pixels. The average pixel current as well as the display brightness as a function of the data voltage are shown in Fig. 5-13. Including the ~4V OLED turn on voltage, the display starts to turn on at V_{DATA}=6V, implying a TFT threshold voltage of ~2V. From the slope of the pixel luminance vs. pixel current graph (Fig. 5-14), the luminance efficiency of the OLED is deduced as 14cd/A, which was typical of that expected for polymer LED's made of the "Super-Yellow" polymer [7]. For a display brightness of 100nits (pixel brightness of 200nits), V_{DATA} of 11V is required, corresponding to V_{OLED} of ~5.5V and a gate-to-source voltage (V_{DATA}-V_{OLED}) on T2 of 5.5V. This number is slightly lower than the required 6V estimated by DC electrical testing before the OLED integration. The

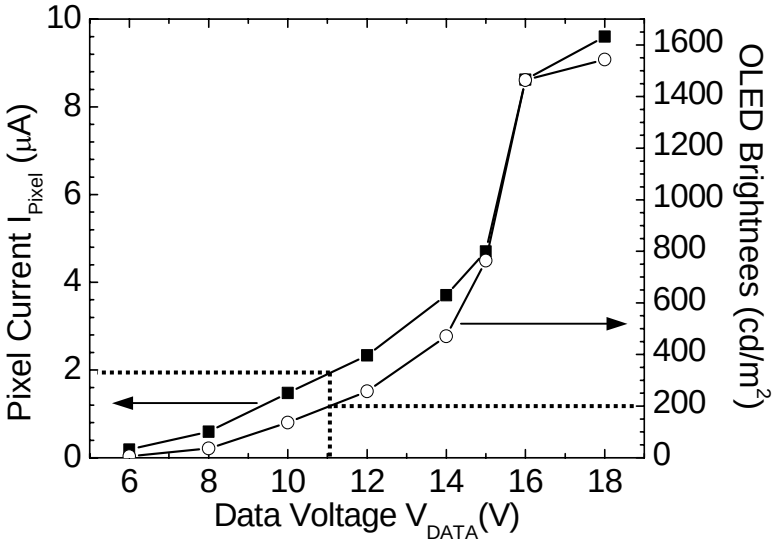


Figure 5-13. Measured pixel current and pixel brightness as a function of data voltage. The dotted lines indicate 11V data voltage is needed for 100 nits display brightness (assume 50% polarizer loss).

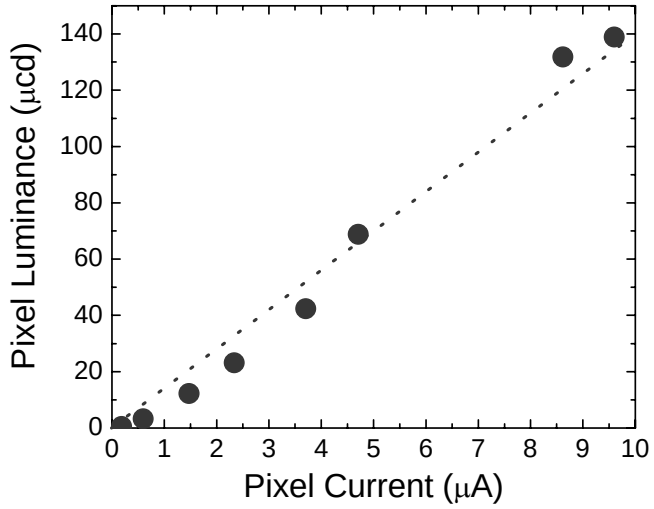


Figure 5-14. Pixel brightness as a function of pixel current.

primary reason for the lower drive requirement is that the actual OLED luminance efficiency of 14cd/A is higher than that used in the estimation (10cd/A).

5.4 Conclusion

Amorphous-Si TFT's with excellent performance have been fabricated at a process temperature of 180°C both on clear plastic and glass substrates. Active matrix backplane pixel circuits made for polymer LED's can provide sufficient drive current at low data voltage for bright displays and have sufficiently low leakage current for active matrix operation. Pulsed operation under various timings shows that the leakage in the access transistor is very small, so that data is accurately latched in the pixel for the entire frame time. A small AMOLED array was successfully demonstrated with very high brightness (>1000 nits) at a relatively low data voltage (15V) with only ~9V of this across the TFT itself. These results show that amorphous silicon TFT's on clear plastic are an attractive route to AMOLED displays on clear flexible plastic substrates.

ACKNOWLEDGEMENT

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CHAPTER 6

SUMMARY AND FUTURE WORK

6.1 Summary

The goal for our work has been to develop fundamental elements necessary to achieve flexible full color AMOLED displays on clear plastic substrates using high temperature amorphous-silicon TFT's. For this purpose, dry dye printing from a pre-patterned printing stamp followed by solvent-enhanced dye diffusion was used to locally dope a previously spin-coated polymer film with different dyes to fabricate side-by-side RGB OLED sub-pixels for a full color display. To reduce reverse leakage current and improve efficiency, a novel tri-layer OLED structure, which consists of an additional Alq_3 ETL layer and a BCP hole/exciton blocking layer was developed. The BCP layer confines the light emission to the doped polymer layer. The EL efficiency of the devices was optimized by the dye concentration in the printing plate. Devices with this tri-layer structure and the optimized dye source demonstrate high external quantum efficiencies (~1%) and an extremely low reverse leakage current (rectification ratio of 10^6 at +/- 10V). This device architecture demonstrates a new approach for combining the printability of polymer with the optimum transport capability of small organic molecules to achieve high performance organic LED's.

A high process temperature (~300°C) is required for optimum a-Si TFT properties and minimum electron trapping in the gate dielectric for long-term stability. However, clear plastics with a glass transition temperature (T_g) in excess of 300°C have a

coefficient of thermal expansion (CTE) larger than that of the silicon nitride and a-Si in the TFT's. This can lead to cracking of the device films that limits the process temperature to well below that of the plastic glass transition temperature. In chapter 4, the mechanical interaction of the TFT stack and the plastic substrate is modeled to develop design guidelines to avoid cracking. A critical interfacial stress determines the fracture point. This methodology was then used to successfully fabricate a-Si TFT's on novel clear plastic substrates supplied by DuPont at a maximum process temperature of up to 280°C. The TFT's made at high temperatures have higher mobility and lower leakage current, and higher stability compared to TFT's made on conventional low-T_g clear plastic substrates.

Active matrix pixel circuits for organic LEDs on both glass and clear plastic substrates were fabricated with these TFT's. The leakage current in the switching TFT is low enough to allow data storage for video graphics array (VGA) timing. The pixels provide suitable drive current for bright displays at a modest drive voltage. A small AMOLED array was successfully demonstrated with very high brightness (1500 nits) at a relatively low data voltage of 15V with only ~9V of this across the TFT itself. These results show that amorphous silicon TFT's on clear plastic are an attractive route to AMOLED displays on clear flexible plastic substrates.

6.2 Future work

There is a growing interest in flexible electronics. Industry is seeking to keep the TFT process on flexible substrates in the temperature range of 300-350°C developed for

a-Si TFTs on glass. This high temperature results in the best a-Si TFT performance, particularly because temperatures of at least 300 ^{o}C are required for high quality SiN_x gate insulators. Therefore, one of our future projects is to further increase the a-Si TFT process temperature on clear plastic substrate to be identical to that on glass substrates, i.e., at least 300°C.

Although we have fabricated a TFT back plane for AMOLED application, the integration of OLED's with the TFT backplane on a clear plastic substrates still hasn't been achieved. Integrating OLED's onto the TFT backplane to demonstrate a true flexible AMOLED display on clear plastic substrate using high temperature a-Si TFT's is another of our future projects.

We have demonstrated a three color passive matrix OLED array using dry-dye printing technique for the three color patterning. To combine this three color OLED with the TFT back plane on clear plastic substrate to realize a full color flexible AMOLED display is also very attractive.

APPENDICES

A.1 List of Patent Disclosures and Publications

Patent and Inventions

1. “Organic Light-Emitting Devices with Blocking and Transport Layers”, K. Long, M. H. Lu, J. C. Sturm, US patent # 6784016, issued Aug. 2004
2. “Active matrix organic LED display pixel with OLED efficiency monitoring”, J. C. Sturm, K. Long, patent disclosure filed Dec. 2002
3. “Conductive layer planarization with self-aligned insulator”, K. Long, F. Pschenitzka, J. C. Sturm, patent disclosure filed Mar. 2002

List of Publications

1. Ke Long, I-Chun Cheng, Alexis Kattamis, Helena Gleskova, Sigurd Wagner, and J. C. Sturm, “Amorphous-Silicon Thin Film Transistors Made at 280°C on Clear Plastic Substrates by Interfacial Stress Engineering”, to be submitted
2. K. Long, A. Z. Kattamis, I-C. Cheng, H. Gleskova, S. Wagner, and J. C. Sturm, "Stability of amorphous-silicon thin-film transistors deposited on clear plastic substrates at 250°C to 280° C", accepted to be published in IEEE Electron Device Letters, Feb. 2006.
3. K. Long, A. Z. Kattamis, I-C. Cheng, H. Gleskova, S. Wagner, and J. C. Sturm, "Active-Matrix Amorphous Silicon Thin-Film Transistors Arrays at 180°C on Clear Plastic and Glass Substrates for Organic Light-Emitting Displays", submitted to IEEE Transactions on Electron Devices.
4. K. Long, I.-C. Cheng, A. Kattamis, H. Gleskova, S. Wagner, J. C. Sturm, “Increased reliability of a-Si TFT's deposited on clear plastic substrates at high temperatures”, Dig. 63rd Device Research Conf. pp. 141-142 (2005)
5. K. Long, F. Pschenitzka, M.H. Lu, and J. C. Sturm, “Full-color OLED’s integrated by dry dye printing”, submitted to IEEE Trans. on Elec. Dev.

6. K. Long, A. Kattamis, I.-C. Cheng, Y. C. Gao, H. Gleskova, S. Wagner, J. C. Sturm, "High Temperature (250°C) amorphous-silicon TFT's on clear plastic substrates", SID'05 Tech. Dig., vol 36, pp. 313-315 (2005)
7. I.-C. Cheng, A. Kattamis, K. Long, J. C. Sturm, and S. Wagner, "Stress Control for Overlay Registration in a-Si:H TFTs on Flexible Organic Polymer Foil Substrates", Journal of the SID, vol. 13, no. 7, pp563-568 (2005)
8. S. Wagner, I.-C. Cheng, K. Long, A. Kattamis, and J. C. Sturm, "Managing Mechanical Stress in Flexible Active-Matrix Backplanes", Proc. International Display Manufacturing Conference, pp. 415-418 (2005)
9. I-C. Cheng, A. Kattamis, K. Long, J. C. Sturm and S. Wagner, "SiN_x stress control for overlay registration in a-Si:H TFTs on flexible foil substrates", accepted to be published on Mat. Res. Soc. Symp. Proc. (2005)
10. S. Wagner, R. Bhattacharya, I.-C. Cheng, H. Gleskova, J. Jones, A. Kattamis, S. P. Lacour, K. Long, J. C. Sturm, C. Tsay, T. Li and Z. Suo, "Flexible, Conformal, and Elastic Electronic Surfaces", accepted to be published on Mat. Res. Soc. Symp. Proc. (2005)
11. A. Kattamis, I.-C. Cheng, K. Long, J. C. Sturm, S. Wagner, "nc-Si Thin Film Transistors on Optically Clear Polymer Foil Substrates", accepted to be published on Mat. Res. Soc. Symp. Proc. (2005)
12. K. Long, H. Gleskova, S. Wagner, and J. C. Sturm, "Short Channel Amorphous-Silicon TFT's on High-Temperature Clear Plastic Substrates", Dig. 62nd Device Research Conf. pp. 89-90 (2004)
13. K. Long, H. Gleskova, S. Wagner, J.C. Sturm, K.R. Sarma, C. Chanley, S. Dodd, J. Roush, J. Schmidt, G. Srdanov, M. Stevenson, R. Wessel, J. Innocenzo, G. Yu, M. O'Regan, W.A. MacDonald, R. Eveson, "Active matrix OLED using 150°C a-Si TFT backplane built on flexible plastic substrate," SPIE Proc. Vol. 5080, Cockpit Displays vol. X, pp. 180-191 (2003)
14. F. Pschenitzka, K. Long, and J. C. Sturm, " Solvent vapor-enhanced dye diffusion for full-color OLED fabrication", Mat. Res. Soc. Symp. Proc. 665, pp. C9.5.1-C9.5.7 (2001)

15. K. Long, F. Pschenitzka, and J. C. Sturm, “Three-color passive-matrix pixel array with dye-diffusion-patterned thin-film and a novel tri-layer structure”, Mat. Res. Soc. Symp. Proc. 708, pp. BB6.8.1-BB6.8.6 (2001)
16. K. Long, M.H. Lu, F. Pschenitzka, and J. C. Sturm, “Novel three-color polymer light-emitting devices for passive-matrix flat panel displays”, Dig. 59th Device Research Conf. pp. 179-180 (2001)

Conference Presentations

1. “Increased reliability of a-Si TFT's deposited on clear plastic substrates at high temperatures”
   K. Long, I.-C. Cheng, A. Kattamis, H. Gleskova, S. Wagner, J. C. Sturm, 63rd Device Research Conference, Santa Barbara, CA, June 2005
2. “High Temperature (250°C) amorphous-silicon TFT’s on clear plastic substrates”
   K. Long, A. Kattamis, I. C. Cheng, Y. C. Gao, H. Gleskova, S. Wagner, J. C. Sturm, SID’05, Boston, MA, May 2005
3. Invited Talk: “Flexible, Conformal, and Elastic Electronic Surfaces”
   S. Wagner, R. Bhattacharya, I.-C. Cheng, H. Gleskova, J. Jones, A. Kattamis, S. P. Lacour, K. Long, J. C. Sturm, C. Tsay, T. Li and Z. Suo, Materials Research Society Spring Meeting, San Francisco, CA, Mar. 2005
4. “SiN_x stress control for overlay registration in a-Si:H TFTs on flexible foil substrates”
   I.-C. Cheng, A. Kattamis, K. Long, J. C. Sturm and S. Wagner, Materials Research Society Spring Meeting, San Francisco, CA, Mar. 2005
5. “nc-Si Thin Film Transistors on Optically Clear Polymer Foil Substrates”,
   A. Kattamis, I.-C. Cheng, K. Long, J. C. Sturm, S. Wagner, Materials Research Society Spring Meeting, San Francisco, CA, Mar. 2005
6. Invited Talk: “Managing Mechanical Stress in Flexible Active-Matrix Backplanes”,
   S. Wagner, I.-C. Cheng, K. Long, A. Kattamis, and J. C. Sturm, International Display Manufacturing Conference, Taipei, Taiwan, Feb. 2005
7. “Stress Compensation for Overlay Registration in the Fabrication of a-Si:H TFTs on Organic Polymer Foil Substrates”

I.-C Cheng, A. Kattamis, K. Long, J. C. Sturm and S. Wagner, Flexible Displays & Microelectronics Conference, Feb. 2005

8. "Short Channel Amorphous-Silicon TFT's on High-Temperature Clear Plastic Substrates"
   K. Long, H. Gleskova, S. Wagner, and J. C. Sturm, 62nd Device Research Conference, Norte Dame, IN, June 2004
9. "Dye Source Optimization for 3-Color OLED Using Dry Dye Printing"
   K. Long, F. Pschenitzka, and James C. Sturm, Materials Research Society Spring Meeting, San Francisco, CA, Apr. 2004
10. "Feasibility study of 150°C a-Si TFT backplanes for AMPLED"
    K. Long, H. Gleskova, S. Wagner, J. C. Sturm, 2nd SID/MAC OLED Research and Technology Conference, Park Ridge, NJ, Oct. 2003
11. Invited talk: "Physics and Technology of Patterned Dry Dye Printing for Full Color OLED Integration"
    J.C. Sturm, K. Long, Troy Abe, and F. Pschenitzka, 1st SID/MAC OLED Research and Technology Conference, Princeton, NJ, Oct. 2002
12. "Three-color passive-matrix pixel array with dye-diffusion-patterned thin-film and a novel tri-layer structure"
    K. Long, F. Pschenitzka, and J. C. Sturm, Materials Research Society Fall Meeting, Boston, MA, Nov. 2001
13. "Solvent vapor-enhanced dye diffusion for full-color OLED fabrication"
    F. Pschenitzka, K. Long, and J. C. Sturm, Materials Research Society Spring Meeting, San Francisco, CA, Apr. 2001
14. "Novel three-color polymer light-emitting devices for passive-matrix flat panel displays"
    K. Long, M.H. Lu, F. Pschenitzka, and J. C. Sturm, 59th Device Research Conference, Norte Dame, IN, June 2001

A.2 OLED Passive Matrix Test System

In a passive matrix display, the row drivers provide select signal which scan through each row one at a time. In each frame, one row of pixels are turned on for a duration of t_{frame}/N, where t_{frame} is the frame time and N is the number of rows. In passive matrix scheme, we have to drive OLED N times brighter than the desired display brightness, but it doesn't need TFT's, so the system is simpler than active matrix.

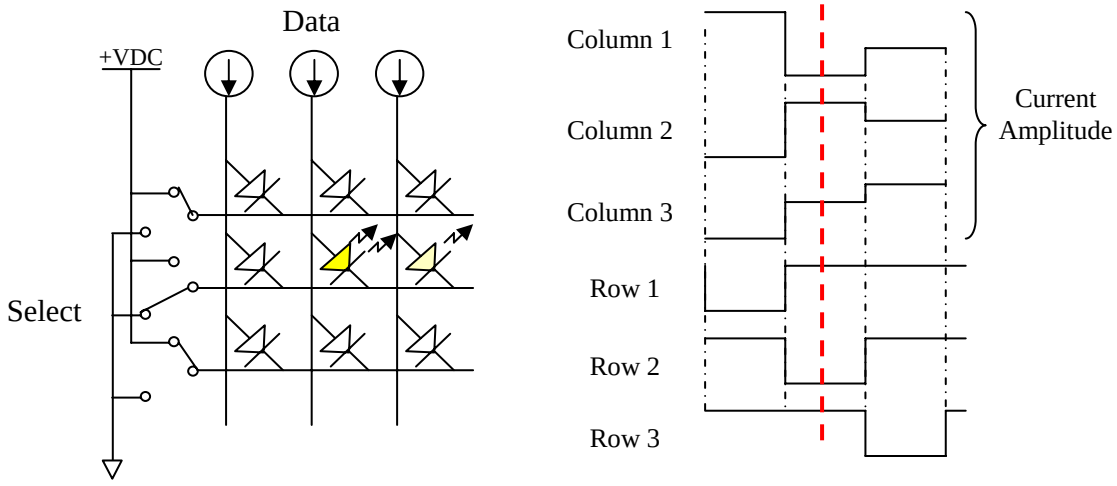


Figure A-1. Passive matrix circuit and driving waveforms.

Fig. A-1 shows the schematic circuitry of an OLED passive matrix and the driving waveforms. Two kinds of driver is needed for driving a passive matrix: row drivers and column drivers. The row drivers provide select signal to scan through row electrodes, turning on one row at a time. The column drivers apply data signals to column electrodes individually using current sources, driving the OLED to the desired brightness. The row lines not selected are reverse-biased.

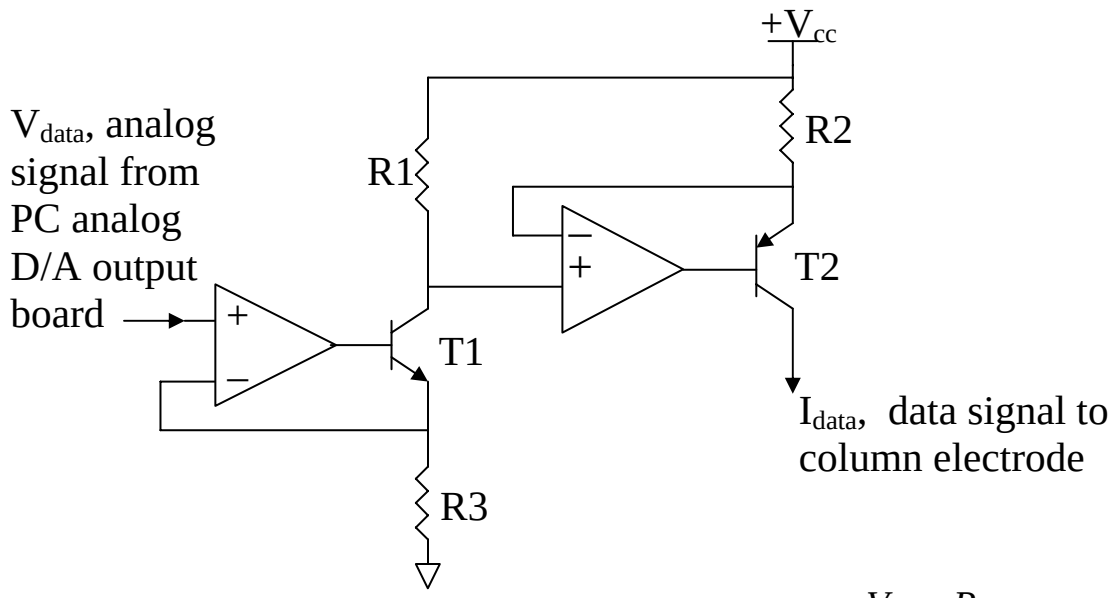


Figure A-2. Column driver: voltage controlled current source, $I_{data} = \frac{V_{data}}{R_3} \frac{R_1}{R_2}$

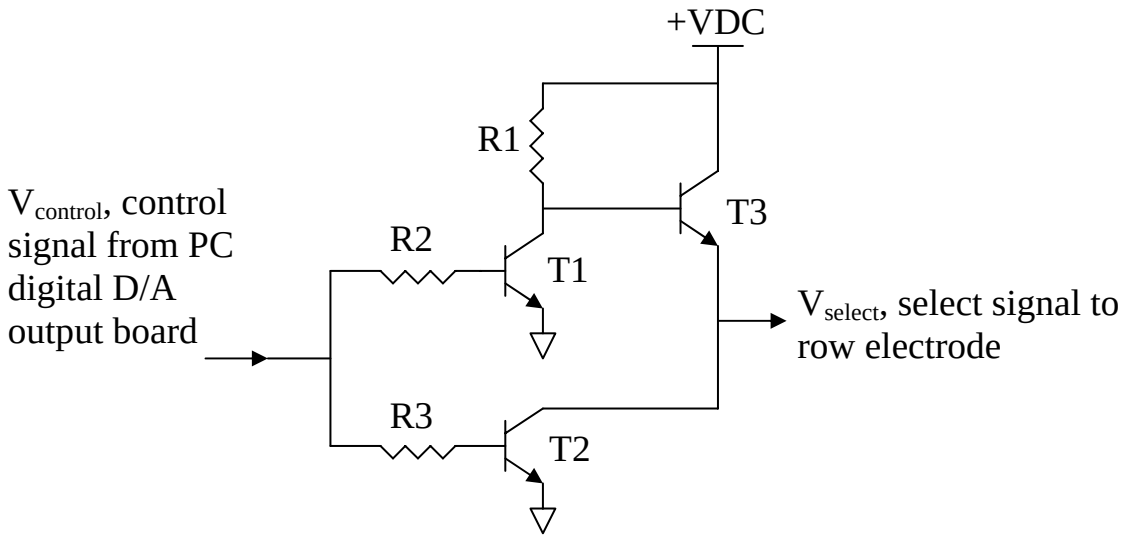


Figure A-3. Row driver: digital switch,

$V_{control}$	High	Low
V_{select}	0	+VDC
Row	ON	OFF

Row Drivers Column Drivers

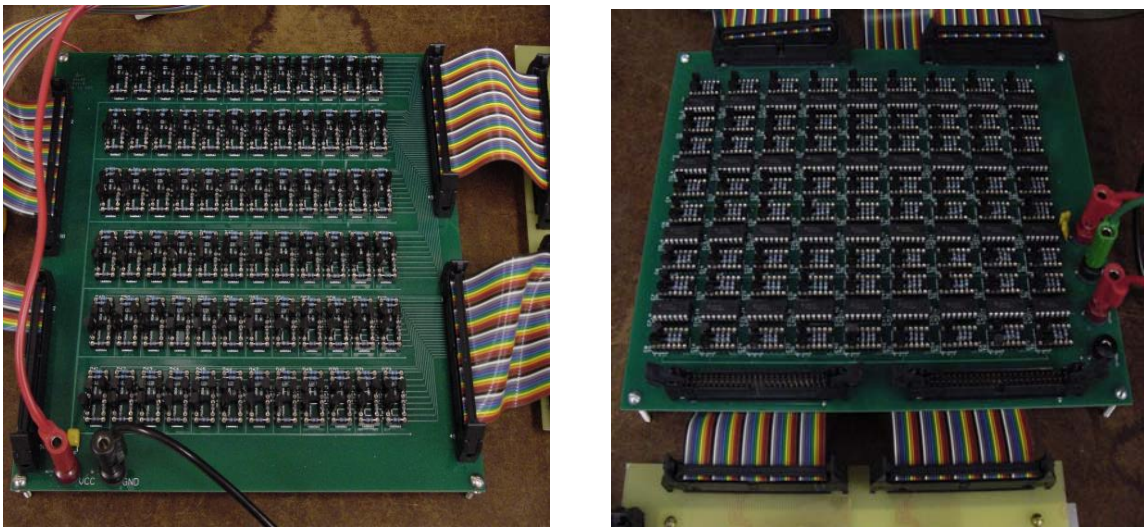


Figure A-4. Pictures of the row driver and column driver PCB.

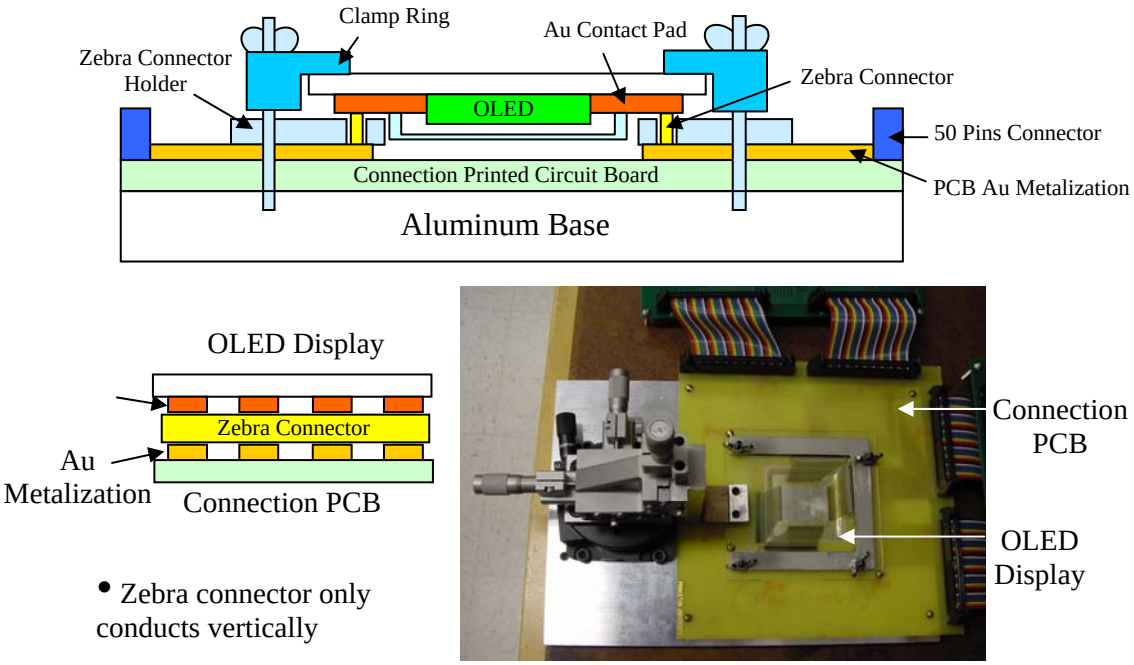


Figure A-5. Integration of the PMOLED display sample and the drivers.

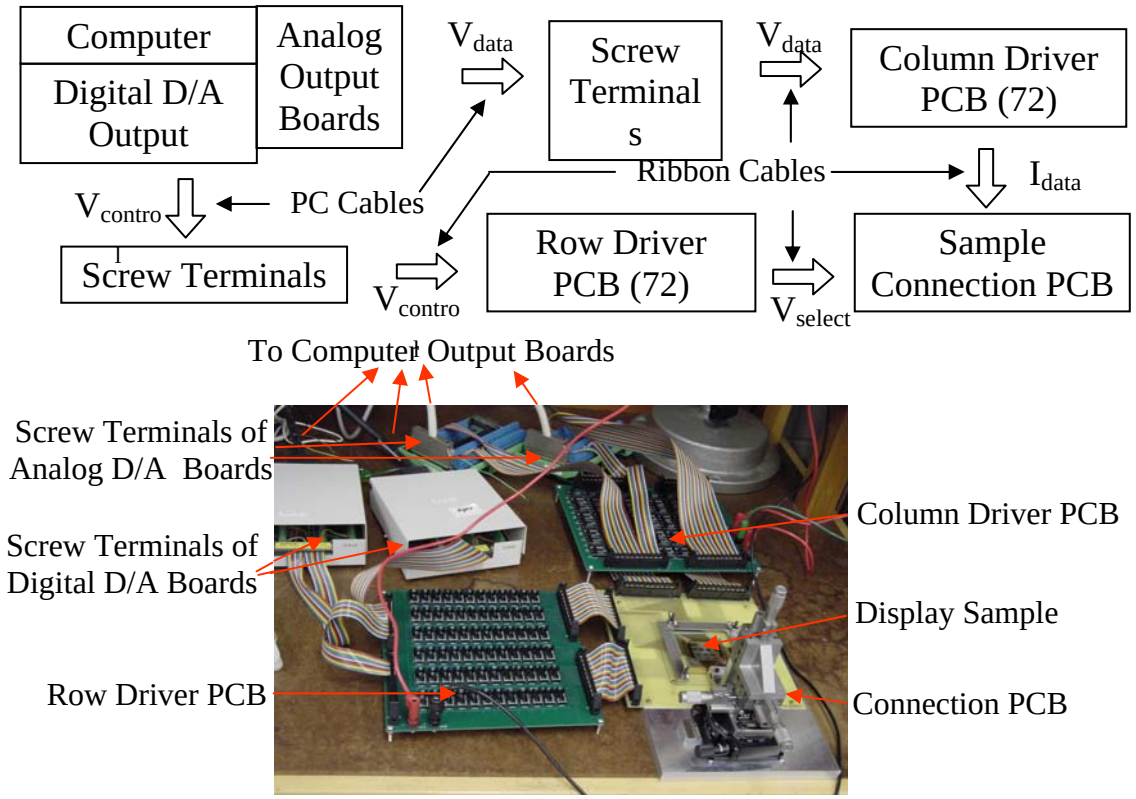


Figure A-6. Schematic of the driving setup.

A.3 PECVD Deposition Conditions for the Device Films: SiN_x, Un-doped a-Si, n^+ a-Si

1. 180°C Process

	LL	N (SiNx)	I (i-Si)	P (n^+-Si)
Heater settings	200, 200, 200	200, 200, 200	200, 200, 200	200, 200, 200
Est. Subs. T	200	150	180	150

Gases	--	SiH_4 = 5 sccm, NH_3 = 50 sccm, H_2 = 220 sccm	SiH_4 = 20 sccm,, H_2 = 20 sccm	SiH_4 = 44 sccm,, PH3 = 6 sccm
Pressure	Vacuum	500 mTorr	500 mTorr	500 mTorr
Plasma Power	--	5W-15W	6W	4W
Deposition rate	--	1Å/sec – 1.7Å/sec	1.6Å/sec	1.2Å/sec

2. 250°C Process

Chamber	LL	N (SiNx)	I (i-Si)	P (n^+-Si)
Heater settings	200, 200, 200	300, 300, 300	250, 250, 230	260, 270, 200
Est. Subs. T	200	250	220	220
Gases	--	SiH_4 = 15 sccm, NH_3 = 130 sccm,	SiH_4 = 50 sccm	SiH_4 = 44 sccm,, PH3 = 6 sccm
Pressure	Vacuum	500 mTorr	500 mTorr	500 mTorr
Plasma Power	--	5W	4W	4W
Deposition rate	--	1.5Å/sec	1.4Å/sec	1.2Å/sec

3. 280°C Process

Chamber	LL	N (SiNx)	I (i-Si)	P (n^+-Si)
Heater settings	250, 250, 250	350, 350, 320	250, 250, 230	260, 270, 200
Est. Subs. T	230	280	220	220
Gases	--	SiH_4 = 15 sccm, NH_3 = 130 sccm,	SiH_4 = 50 sccm	SiH_4 = 44 sccm,, PH3 = 6 sccm
Pressure	Vacuum	500 mTorr	500 mTorr	500 mTorr
Plasma Power	--	5W	4W	4W
Deposition rate	--	1.7Å/sec	1.4Å/sec	1.2Å/sec

A.4 Fabrication Processes for the AMOLED Arrays

1. On ITO/glass substrates

Step #	Process	Mask #	Mask name
1	ITO etch	1	Poly / 46
2	ITO passivation SiN_X deposition		
3	Open contact hole for ITO-gate metal*	2	N Select / 45
4	Gate metal deposition and etch	3	Metal1/ 49
5	Gate SiN_X, a-Si, n^+ a-Si deposition		
6	Source/Drain Metal deposition and etch	4	Poly2 / 56
7	Si Island definition	5	Active / 43
8	n^+ Channel etch (S/D metal as the mask)		
9	Open contact hole for interconnect-gate metal	6	Via / 50
10	Interconnect metal deposition and pattern	7	Metal2 / 51
11	TFT passivation SiN_X deposition		
12	Open windows on top of ITO for OLED's**	8	N Well / 42
13	Spin on polymer		
14	Remove organic at edge for cathode-interconnect contact		
15	Cathode evaporation with shadow mask	9 (shadow mask)	P Select / 44

* Interconnect metal (Al) and ITO connected through gate metal (Cr) to avoid Al-ITO interaction

** Here also open contact holes for cathode-ITO connection (outside of organic area) and for external connection to external bond pads.

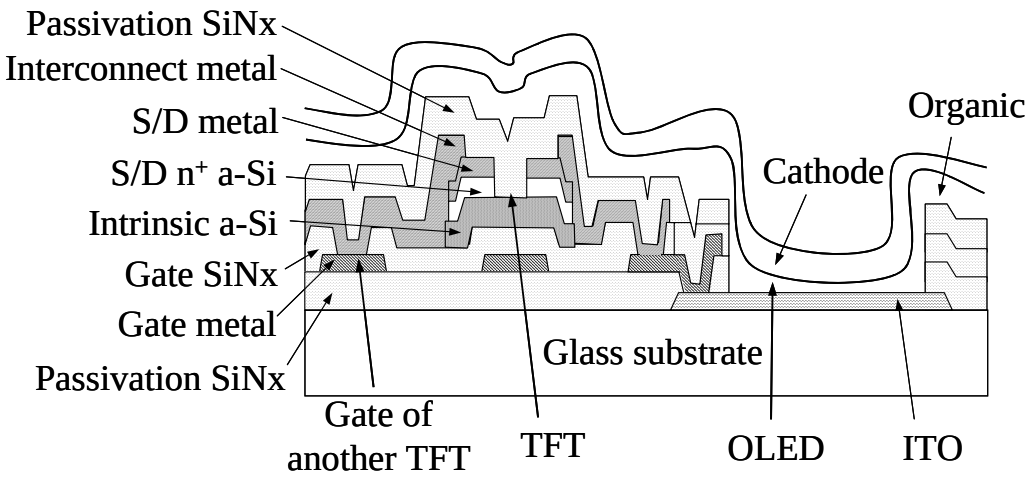


Figure A-1. Schematic cross-section of the TFT-OLED integration on ITO/glass substrate.

2. On clear plastic substrates

Step #	Process	Mask #	Mask name
1	SiN_X buffer deposition (top & bottom)		
2	Gate metal deposition and etch	1	Metal1/ 49

3	Gate SiN_X, a-Si, n^+ a-Si deposition		
4	Source/Drain Metal deposition and etch	2	Poly2 / 56
5	Si Island definition	3	Active / 43
6	n^+ Channel etch (S/D metal as the mask)		
7	Open contact hole for interconnect-gate metal	4	Via / 50
8	Interconnect metal deposition and pattern	5	Metal2 / 51
9	TFT passivation SiN_X deposition (passivation I)		
10	Open contact hole for ITO-gate metal*	6	N Select / 45
11	ITO deposition and etch	7	Poly / 46
12	ITO edge passivation SiN_X deposition(passivation II)		
13	Open windows on top of ITO for OLED's**	8	N Well / 42
14	Spin on polymer		
15	Remove organic at edge for cathode-interconnect contact		
16	Cathode evaporation with shadow mask	9 (shadow mask)	P Select / 44

* Interconnect metal (Al) and ITO connected through gate metal (Cr) to avoid Al-ITO interaction

** Here also open contact holes for cathode-ITO connection (outside of organic area) and for external connection to external bond pads.

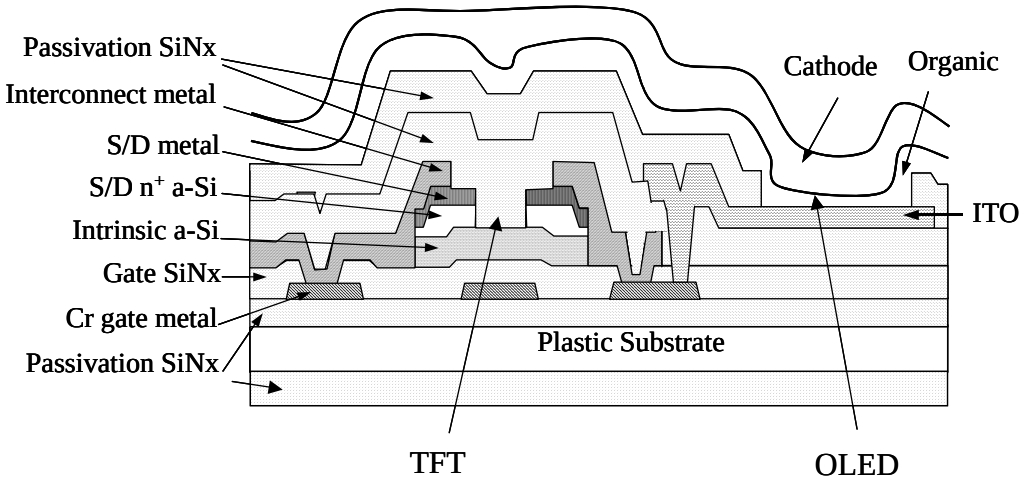
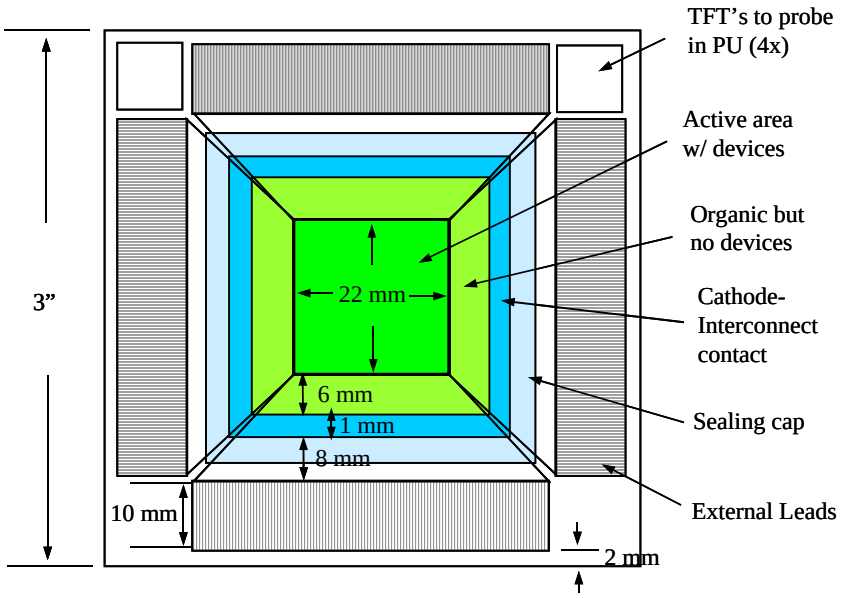


Figure A-2. Schematic cross-section of the TFT-OLED integration on clear plastic substrate.

3. Overview of the test AMOLED sample

3.1 Top view of the test sample



3.2 Test features on the test sample

3.2.1 Electronic test structures (probe before deposition of organic)

- TFT's:
  - Single-gate: W/L = 5/5, 10/5, 20/10, 20/20, 40/5, 60/5, 80/5, 80/10, 80/20, 80/40, 80/80
  - Double-gate: W/L = 5/5, 10/5, 20/10, 20/20
- Capacitors:
  - Area: 50 x 50 μm2 Capacitance: ~ 0.5 pF

    100 x 100 μm2 ~ 2 pF

    200 x 200 μm2 ~ 8 pF

    300 x 300 μm2 ~ 16 pF
- Sheet resistance:

  Stripes with W/L = 1500/15 of gate metal, interconnect metal, source/drain metal and ITO
- Connection via chain (chains with 20 contacts through 10 μm x 10 μm contact holes)
  - Gate-ITO
  - Gate-Interconnect metal
  - Gate-ITO-Interconnect metal
  - S/D metal-n+ a-Si: NOT possible since S/D metal serves as the mask to etch n+ a-Si

Connection through direct contact

- S/D metal to Interconnect metal: contact resistance test
- Cathode-Interconnect metal: short test (area = 2mm x 2mm)

3.2.2 Features connected to external leads (200 leads, with 50 at each side, pitch of the leads = 1mm)

- 2-TFT pixel (300μm x 300μm)
  - 2 single pixels
  - 6 x 18 array
  - 6 x 6 array
  - Fill factor = 0.46
- 3-TFT pixel (300μm x 300μm)
  - single pixels
  - 6 x 18 array
  - 6 x 6 array
  - Fill factor = 0.37
- 4-TFT pixel (300μm x 300μm)
  - 2 single pixels
  - 6 x 9 array
  - 3 x 9 array
  - Fill factor = 0.32
- 5-TFT pixel (300μm x 300μm)
  - single pixels
  - 6 x 6 array
  - x 6 array

  - Fill factor = 0.30

- TFT-OLED: one TFT driving one OLED
  - TFT's with W/L = 80 μm /5 μm, 60/5, 80/10
  - OLED's: about the same size as those in the pixels: ~ 250 μm x 200 μm
- Single OLED's:
  - 2 of 250 μm x 250 μm
  - 2 of 3 mm x 3 mm
- Single TFT's: W/L = 80 μm /10 μm, 60/5, 20/20, 20/5

A.5 External Pin Assignments of the AMOLED Test Sample

Top starting at left

PIN #	Name	DESCRIPTION
	New Pixel 6x6	2-TFT pixel plus a third TFT for OLED voltage monitoring, every 3rd rows share select signal
T1		N/A
T2		V_{OLED} 1
T3		V_{OLED} 2
T4		V_{OLED} 3
T5		V_{OLED} 4
T6		V_{OLED} 5
T7		V_{OLED} 6
T8		Select 1
T9		Select 2
T10		Select 3
T11		Data 1
T12		Data 2
T13		Data 3
T14		Data 4
T15		Data 5
T16		Data 6
T17		VDD

T18		Cathode
	2-TFT 6x18	6 row x 18 column array, every 3rd rows share select signal, every 6th columns share data signal
T19		Select 1
T20		Select 2
T21		Select 3
T22		Data 1
T23		Data 2
T24		Data 3
T25		Data 4
T26		Data 5
T27		Data 6
T28		VDD
T29		Cathode
	2-TFT	Single test pixel
T30		Cathode
T31		Select
T32		Date
T33		VDD
	TFT_OLED	3 TFT's drive 3 OLED's, with drain and gate connected, W/L = 80/10, 60/5, 80/5; OLED's with area ~ 250μm x 250μm
T34		Cathode
T35		Source, W/L = 80/10
T36		Drain & Gate, W/L = 80/10
T37		Source, W/L = 60/5
T38		Drain & Gate, W/L = 60/5
T39		Source, W/ L = 80/5
T40		Drain & Gate, W/L = 80/5
	4-TFT	Single test pixel
T41		Cathode
T42		Select
T43		I_Data
T44		VDD
T45		Select Enable
	3-TFT	Single test pixel
T46		Cathode
T47		Select
T48		Data
T49		VDD
	Large_OLED	Single test OLED with area = 9 mm^2
T50		Anode

Right starting at top

R1		Cathode

	4-TFT 3x9	3 row x 9 column array
R2		Cathode
R3		Select Enable 1
R4		Select Enable 2
R5		Select Enable 3
R6		Select 1
R7		Select 2
R8		Select 3
R9		I_Data 1
R10		I_Data 2
R11		I_Data 3
R12		I_Data 4
R13		I_Data 5
R14		I_Data 6
R15		I_Data 7
R16		I_Data 8
R17		I_Data 9
R18		VDD
	5-TFT 6x6	6 row x 6 column array
R19		Select Enable 1
R20		Select Enable 2
R21		Select Enable 3
R22		Select 1
R23		Select 2
R24		Select 3
R25		IO 1
R26		DD 1
R27		IO 2
R28		DD 2
R29		IO 3
R30		DD 3
R31		IO 4
R32		DD 4
R33		IO 5
R34		DD 5
R35		IO 6
R36		DD 6
R37		Select 4
R38		Select 5
R39		Select 6
R40		Select Enable 4
R41		Select Enable 5
R42		Select Enable 6
R43		VDD
R44		Cathode

	5-TFT	Single test pixel
R45		Select
R46		IO
R47		DD
R48		VDD
R49		Select Enable
R50		Cathode

Bottom starting at right

	TFT 20/5D	Single test TFT, W/L = 20/5, double-gate
B1		Source
B2		Gate
B3		Drain
	Large_OLED	Single test OLED with area = 3 mm x 3 mm
B4		Anode
B5		Cathode
	Small_OLED	Single test OLED with area = 250μm x 250μm
B6		Anode
B7		Cathode
	3-TFT 6x18	6 row x 18 column array
B8		Select 1
B9		Select 2
B10		Select 3
B11		Data 1
B12		Data 2
B13		Data 3
B14		Data 4
B15		Data 5
B16		Data 6
B17		VDD
B18		Cathode
	2-TFT 6x6	6 row x 6 column array
B19		Select 1
B20		Select 2
B21		Select 3
B22		Data 1
B23		Data 2
B24		Data 3
B25		Data 4
B26		Data 5
B27		Data 6
B28		VDD
B29		Cathode
	4-TFT	Single test pixel
B30		Select

B31		I_Data
B32		VDD
B33		Select Enable
B34		Cathode
	3-TFT	Single test pixel
B35		Select
B36		Data
B37		VDD
B38		Cathode
	2-TFT	Single test pixel
B39		Select
B40		Data
B41		VDD
B42		Cathode
	TFTs	4 test TFT's sharing drain, every 2 sharing gate, each has own source
B43		Gate, W/L = 20/5 & 60/5
B44		Source, W/L = 20/5
B45		Source, W/L = 60/5
B46		Source, W/L = 80/10
B47		Source, W/ L = 20/20
B48		Gate, W/L = 80/10 & 20/20
B49		Drain
	Small_OLED	Single test OLED with area = 250μm x 250μm
B50		Cathode

Left starting at bottom

L1		Anode
	4-TFT 6x9	6 row x 9 column array
L2		Cathode
L3		Select Enable 1
L4		Select Enable 2
L5		Select Enable 3
L6		Select 1
L7		Select 2
L8		Select 3
L9		I_Data 1
L10		I_Data 2
L11		I_Data 3
L12		I_Data 4
L13		I_Data 5
L14		I_Data 6
L15		I_Data 7
L16		I_Data 8
L17		I_Data 9

L18		Select 4
L19		Select 5
L20		Select 6
L21		Select Enable 4
L22		Select Enable 5
L23		Select Enable 6
L24		VDD
	5-TFT 6x6	6 row x 6 column array
L25		Select Enable 1
L26		Select Enable 2
L27		Select Enable 3
L28		Select 1
L29		Select 2
L30		Select 3
L31		IO 1
L32		DD 1
L33		IO 2
L34		DD 2
L35		IO 3
L36		DD 3
L37		IO 4
L38		DD 4
L39		IO 5
L40		DD 5
L41		IO 6
L42		DD 6
L43		VDD
L44		Cathode
	5-TFT	Single test pixel
L45		Select
L46		IO
L47		DD
L48		VDD
L49		Select Enable
L50		Cathode