Chapter 5

PEDOT/Si/TiO_2 Heterojunction Solar Cells

5.1 Introduction

The work presented thus far has discussed the properties of two heterojunctions on n-type silicon; PEDOT/Si and Si/TiO_2. The data presented in Chapter 3 have shown the PEDOT/Si heterojunction acts as an electron-blocking, hole-selective contact that can be used in place of a p-n junction. The dark current in the PEDOT/Si device is observed to be dominated by hole injection into the n-type silicon, which leads to the need of a back-surface field for further J_0 reduction. In Chapter 4, the band alignments and surface passivation of the Si/TiO_2 heterojunction were shown to fit the requirements of a hole-blocking, electron selective contact which can potentially act as a BSF for an n-type solar cell. The symmetry of these heterojunctions is valuable in that they present two complementary contacts, which can combine to increase the efficiency of a photovoltaic device. Furthermore, both heterojunctions were fabricated without the use of any high-temperature diffusion steps as are typically required in forming a p-n junction or n^+-n BSF. Therefore, the use of a Si/TiO_2 heterojunction

as a back surface field for a PEDOT/Si device to form a PEDOT/Si/TiO_2 (PST) solar cell represents the logical continuation of the work presented in the preceding chapters.

The PST solar cell can be considered analogous to the HIT solar cell discussed in Chapter 2. Figure 5.1 shows the band offsets of the PEDOT/Si and Si/TiO_2 heterojunctions to the conduction and valence bands of silicon. Both rely on heterojunctions to a lightly doped, high-quality wafer (rather than diffusing a conventional p-n junction), however the HIT solar cell requires a plasma deposition process to form amorphous-silicon heterojunctions. The growth of these amorphous silicon heterojunctions must be done carefully to avoid the formation of a heavily doped crystalline layer [144]. Therefore, the PST not only represents a heterojunction solar cell fabricated without a p-n junction, but also without any plasma deposition processes. In addition, all processing temperatures used were below 250 °C. In this chapter, the dark current characteristics, photovoltaic performance, external quantum efficiency, and charge storage behavior of the PST cell are presented and compared to those of the single-sided PEDOT/Si device.

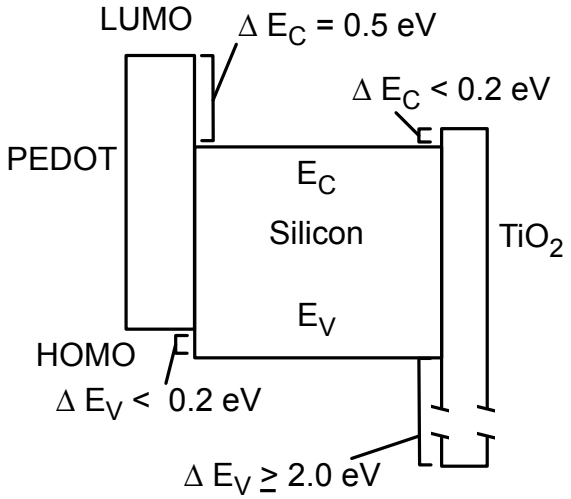


Figure 5.1: Band offsets of PEDOT:PSS and Titanium dioxide to crystalline silicon as measured by photoemission spectroscopy.

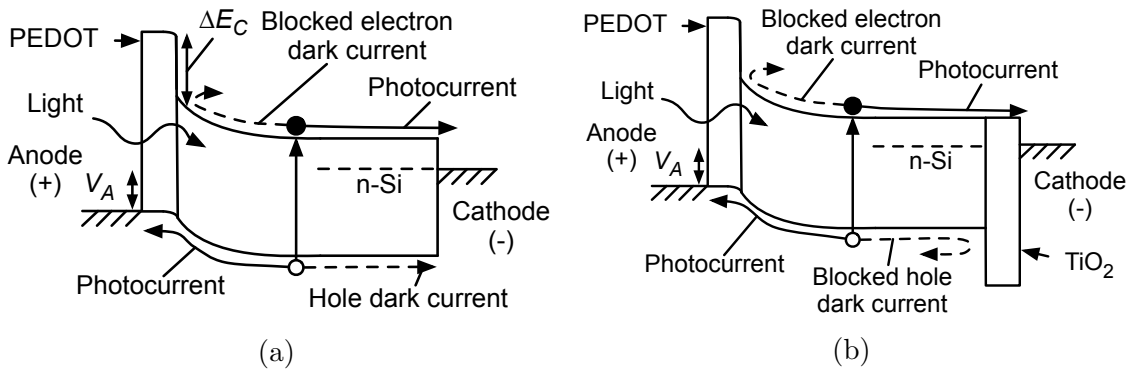


Figure 5.2: Band diagrams of (A) single-sided PEDOT/Si photovoltaic device under illumination with small forward bias compared to a (B) PST device under similar conditions.

The introduction of a titanium dioxide hole blocker serves to reduce the dark current in a PEDOT/Si device. As shown in Chapter 3, the current in a PEDOT/Si device is dominated by hole current injected into the body of the n-type silicon from the PEDOT:PSS. These injected holes can then recombine due to bulk recombination or diffuse to the back at the back interface and recombine at the metal cathode. For the high-lifetime silicon substrates used for the PST devices, the bulk recombination time is long ($\geq$1.0 ms) and the hole diffusion length $L_{p,N}$ is much longer than the width of the n-type quasi-neutral region W ($L_{p,N}/W > 3$). As a result, the device can be considered to be in the short-base regime, and the majority of the injected holes from the PEDOT:PSS will reach the cathode and recombine. The carrier paths within such a device are presented in the band diagram of Figure 5.2a. By incorporating a TiO_2 hole-blocking layer at the cathode, these injected holes are presented with an energetic barrier due to the valence band offset of the TiO_2. Therefore, the dark current flow due to these injected holes is reduced, as illustrated in Figure 5.2b.

In this chapter the effects of using TiO_2 as a BSF to complement the PEDOT/Si solar cell are presented. Section 5.2 discusses the fabrication of the PST solar cell. Section 5.3 presents experimental data from the PST solar cells compared to PEDOT/Si devices, including dark current-voltage measurements (section 5.3.1), illu-

minated current-voltage measurements (section 5.3.2), external quantum efficiency (section 5.3.3), and minority carrier storage (section 5.3.4). Section 5.4 shows the effect that the thickness of the TiO_2 has on the PST devices, and section 5.5 draws conclusions form the experimental data presented.

5.2 Fabrication

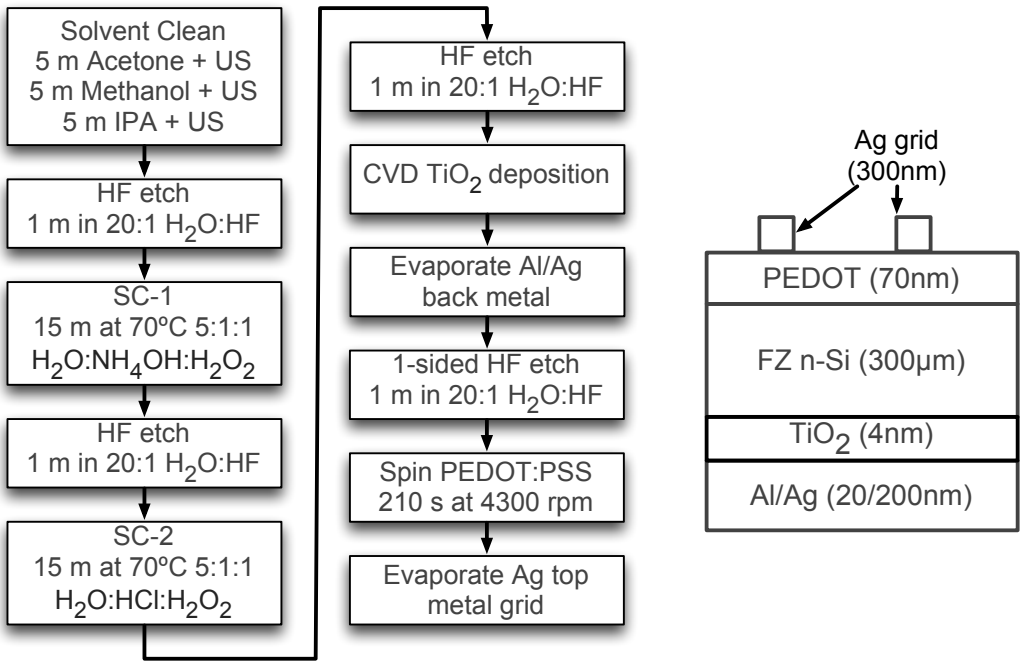


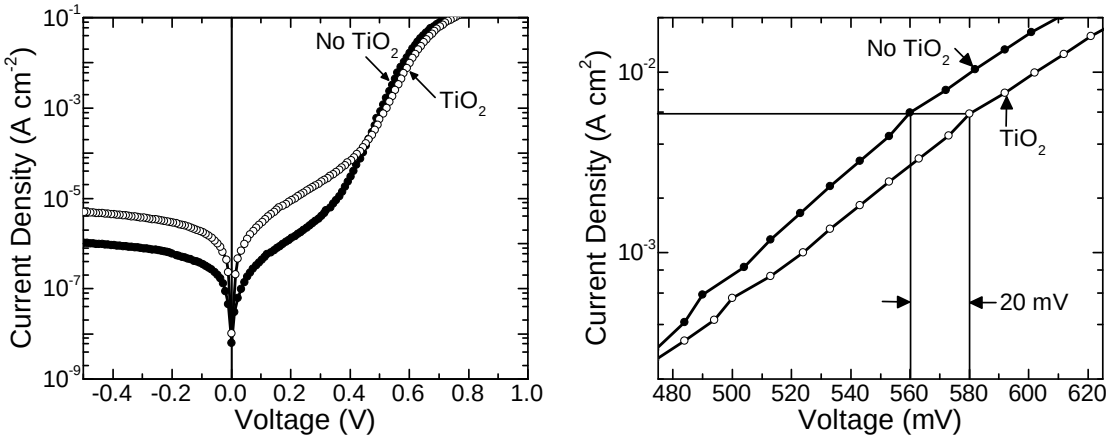
Figure 5.3: Fabrication process and structure of PST solar cell.

The fabrication process of the PEDOT/Si/TiO_2 Solar Cell is shown in Figure 5.3. For the double-sided heterojunction solar cells, in order to reduce losses due to bulk recombination, float-zone wafers with high bulk-lifetime were used, which had a phosphorus doping concentration of $10^{15}\,\mathrm{cm}^{-3}$. These wafers had a thickness of 300 µm and were double-side polished. The initial dicing and cleaning procedure of a solvent clean with ultrasonic (US) agitation and RCA clean is identical to that of the single sided PEDOT/Si device described in Section 3.2.

Immediately following the final HF dip of the cleaning procedure, the 16 mm×16 mm silicon samples are placed into the TiO_2 deposition chamber. The thin films are deposited using the cycled growth method described in Section 4.2. For the devices fabricated and discussed within this chapter a standard deposition of 3 cycles was used (unless specified otherwise, as in section 5.4). Following the deposition of TiO_2 the samples received evaporation of aluminum and silver metal to form the contact on the cathode side of the device.

As described in Chapter 4, TiO_2 is deposited on both sides (anode and cathode) of the silicon samples during the low-temperature CVD process. The TiO_2 on the anode side of the sample is etched away with the use of a PDMS mold, which allows the application of 20:1 H_2O:HF acid to only one side of a 16 mm×16 mm sample (shown schematically in Figure 5.4). This allows the TiO_2 on the cathode side to remain while the anode side is etched. Immediately following the HF acid etch, the sample is rinsed with deionized water, blown dry using N_2, and the anode side of the device is spin-coated with PEDOT:PSS at 4300 rpm. After PEDOT:PSS coating the samples are then placed under vacuum for thermal evaporation of the front side metal grid. Three grid designs were used that covered 5.4 %, 9.7 %, and 16.2 % of the top surface area of the device. The grid layouts are shown in section A.1.

Figure 5.4: Schematic of PDMS mold used to etch TiO_2 from only one side of the silicon sample.



(a) (b)

Figure 5.5: (A) Current-density vs voltage characteristics of single-sided and PST solar cell in the dark. (B) Close-up of ideal (n=1) exponential region showing ∼20 mV shift

5.3 Performance of TiO_2 Hole Blocker as a Back-Surface-Field

The following sections seek to experimentally demonstrate the performance of TiO_2 as an effective hole blocker in photovoltaic devices. To that end, the double-sided heterojunction device (PEDOT/Si/TiO_2) is compared to a single-sided heterojunction device (PEDOT/Si). Section 5.3.1 looks at the effect that TiO_2 has on the current-voltage characteristics of solar cells in the dark, while Section 5.3.2 presents the data obtained under AM1.5G illumination. Section 5.3.3 shows the effect of TiO_2 on external quantum efficiency (EQE) measurements. Section 5.3.4 presents the effect that TiO_2 has on the stored charge within the device as measured by reverse recovery.

5.3.1 Dark Current-Voltage Characteristics

The current density-voltage (J-V) characteristics of a PEDOT/Si and PEDOT/Si/TiO_2 (PST) device as measured in the dark are presented in Figure 5.5a. Both devices show some non-ideal (n>1) current in reverse and low forward bias (<0.4 V). The

source of this non-ideal current may be caused by the differences in the fabrication process needed to make the PST solar cells (compared to the PEDOT/Si devices presented in Chapter 3). However, in the ideal portion of the log(J)-V characteristics where n≈1, the current in the double-sided device is reduced substantially compared to the single-sided one. A closer view of the ideal exponential portion of the log(J)-V curves in forward bias is shown in Figure 5.5b. Here it becomes easier to quantify the amount of current reduction. For a fixed bias voltage, the hole-blocking layer causes a 1.8-fold reduction in the dark current-density that flows in the double-sided device compared to the single-sided device. Equivalently, to reach the same current-density a 20 mV greater bias voltage is required for the double-sided heterojunction device.

The J-V measurements in the dark show a reduction in the dark current that can be used to calculate an estimate of the SRV at the Si/TiO_2 interface. Using Equation 2.4 and values of $D_{p,N} = 11\,\mathrm{cm/\,sec}$ and $W = 300\,\mu\mathrm{m}$, a blocking factor of 1.8 gives an estimated S_{Si/TiO_2} of $\sim$460 cm/ sec. The blocking factor taken from the dark J-V is one method for estimating the SRV of the Si/TiO_2 interface in an actual device. This is important, as the TiO_2 films within the PST solar cell receive metal, whereas those used to measure SRV via the Quasi-Steady-State Photoconductance Decay (QSSPCD) method presented in Chapter 4 do not. Therefore several measurements of the PST solar cell are employed to make estimates of the SRV of the Si/TiO_2 interface.

5.3.2 Illuminated Current-Voltage Characteristics

The J-V characteristics of the single-sided and double-sided devices under AM1.5G illumination are shown in Figure 5.6, and the solar cell performance parameters are shown in Table 5.1. AM1.5G measurements were made using an OAI systems AAA Tri-sol solar simulator, and a 4 mm×4 mm aperture was used to ensure accurate estimation of photocurrent. Solar simulator output was measured using a silicon reference

cell (PV Measurements Inc.) that was calibrated using Newport Corporations PV Cell Lab. All calculations use total device area (4 mm×4 mm), including the metalized grid, which covered about 16 % of the device surface for the data shown Figure 5.6 and Table 5.1. The double-sided device shown exhibits a significant improvement over the single-sided device of over 30 mV in V_{OC}. This is further evidence that the dark current is reduced at the Si/TiO_2 interface due to the hole-blocker, as this increase in V_{OC} agrees to first order with the shift observed in the dark current characteristics.

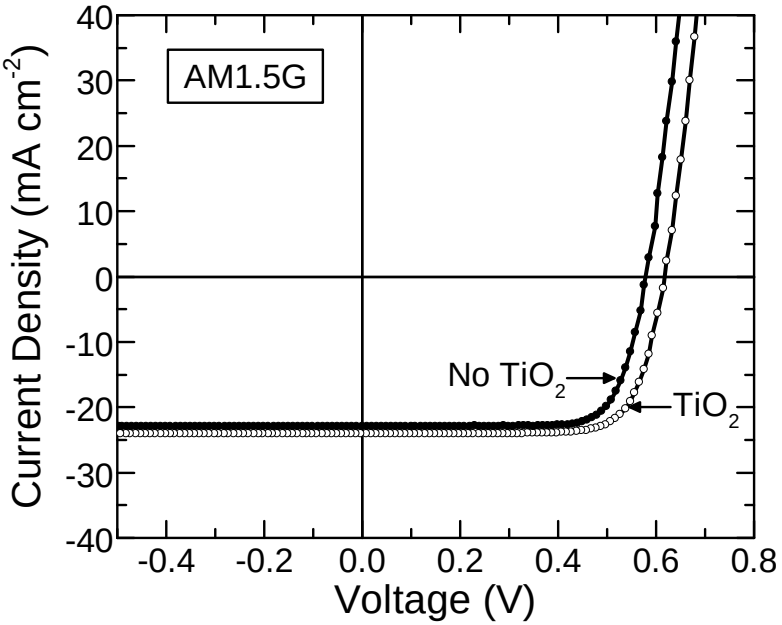


Figure 5.6: Current-voltage characteristic of a PEDOT/Si solar cell with and without TiO_2 hole blocker under AM1.5G illumination.

Table 5.1: Performance parameters of PEDOT/Si and PEDOT/Si/TiO_2 solar cells

Device	V_{OC}(mV)	J_{SC}(mA cm^{-2})	FF(%)	η(%)
No TiO_2	583	22.9	77.1	10.3
With TiO_2	614	24	76.2	11.2
Δ	+31	+1.1	-0.9	+0.9

The measured improvement in open-circuit voltage ΔV_{OC} can also provide an estimate of the SRV at the Si/TiO_2 interface. Using the observed open-circuit voltages of the devices presented in Table 5.1 and Equation 2.7, the SRV at the Si/TiO_2 interface can be estimated to be $\sim$170 cm s^{-1}. However, this contrasts to the value estimated from dark J-V measurements of $\sim$460 cm/ sec for the Si/TiO_2 interface.

It is useful to also consider the average values of V_{OC} of the devices. The average and standard deviation of V_{OC} for eighteen PEDOT/Si devices and eighteen PST devices are (588 ± 4) mV and (613 ± 5) mV, respectively, which provides an average value of ΔV_{OC} of (25 ± 7) mV. This leads to an estimate of SRV between 150 cm s^{-1} to 360 cm s^{-1}, a range which is closer to the value estimated from the dark J-V measurement.

It is also possible that the disagreement in the SRV estimation may be due in part to the control device suffering from a parasitic barrier at the back contact. The parasitic back contact and the backside scribing used to mitigate its effect are discussed in Section A.2. However, it is possible that even with the backside scribing, there is a finite parasitic barrier still present at the back contact. This would artificially lower the V_{OC} of the single sided device, increasing ΔV_{OC} and decreasing the calculated value of the SRV. This is further discussed within the experimental conclusions presented in section 5.5.

The hole-blocking TiO_2 layer also improves the short-circuit current density in the PST device. The single-sided device exhibits a short-circuit current of 22.9 mA cm^{-2}, while the double-sided device achieved a J_{SC} of 24.0 mA cm^{-2}, an increase of 1.1 mA cm^{-2}. On average (for 16 % coverage of the top metal grid), the J_{SC} of single-sided devices was (22.8 ± 0.5) mA cm^{-2} and of double-sided devices was (23.6 ± 0.4) mA cm^{-2}, a difference of 0.8 mA cm^{-2}. The increase in short-circuit current density can be attributed to reduced recombination at the rear interface of

the solar cell due to the TiO_2 hole blocker, which will be discussed in the following section.

Overall, the PST device shows an absolute improvement of 0.9 % (8.7 % relative) in power conversion efficiency over the device without any TiO_2 hole blocker. The small decrease in FF observed is a relative change of just -1.2 %, and while this may be due to the incorporation of the TiO_2 layer, it does not significantly hamper the performance of the PST device.

5.3.3 External Quantum Efficiency

The external quantum efficiency measurements also demonstrate the ability of the TiO_2 to reduce hole recombination at the back interface. The EQE spectra for a single-sided device and double-sided device are shown in Figure 5.7. It is clear from the optical modeling presented in Section 3.6 that PEDOT:PSS does not serve as an ideal anti-reflective coating. There is loss in the EQE spectra due to both surface reflection and absorption in the PEDOT:PSS, as predicted by the modeling performed in section 3.6. However, of the most interest is the difference in the spectra of the PST device and the single-sided device towards longer wavelengths (from 700 nm to 1050 nm).

Lower energy photons – those with longer wavelengths– are absorbed poorly in silicon. Figure 5.8 shows the absorption depth vs wavelength for silicon [145]. As the wavelength of light increases, so does the absorption depth, meaning that the profile of absorbed carriers in silicon extends further into the silicon. Since optical absorption directly leads to carrier generation in the silicon, for a given intensity, longer wavelength light is more likely to generate carriers at the back of the solar cell, near the Si/TiO_2 interface. The optical generation in the silicon can be written as in Equation 5.1, where G_0 is the generation rate at the surface of the absorber material, and α_{abs} is the inverse of the absorption depth, also known as the absorption

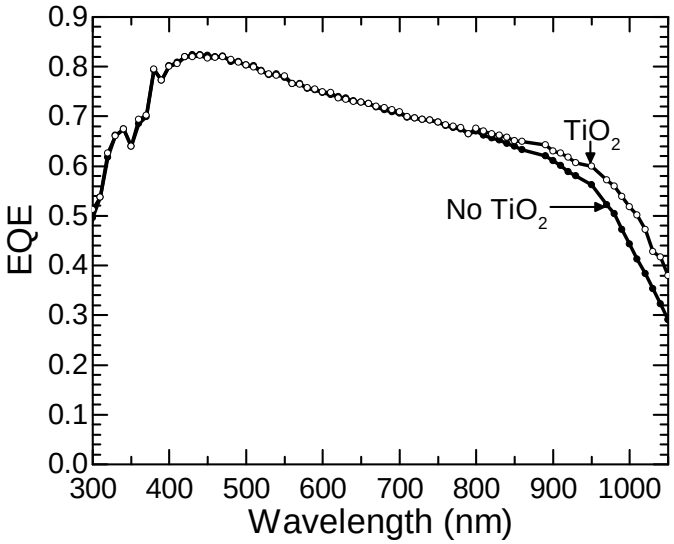


Figure 5.7: External quantum efficiency spectra of double sided and single-sided devices.

coefficient.

$$G_{light}(x) = G_0 \exp(-x\alpha_{abs}) \tag{5.1}$$

The normalized generation rate is plotted as a function of depth in the silicon for several wavelengths in Figure 5.9, and illustrates how longer wavelength light

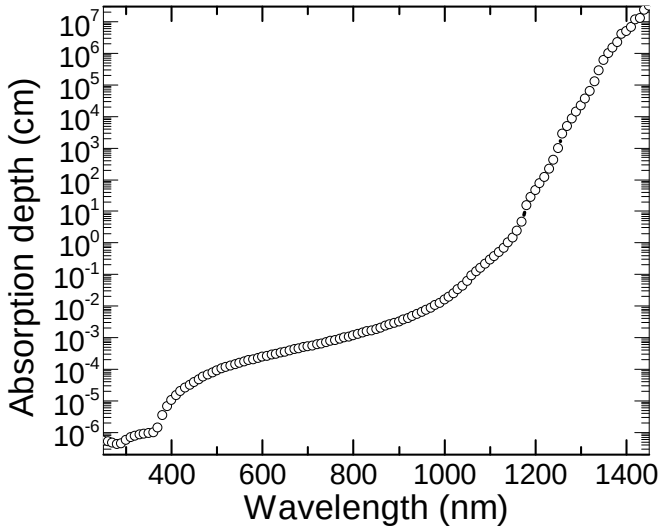


Figure 5.8: Absorption depth versus wavelength for crystalline silicon [145]

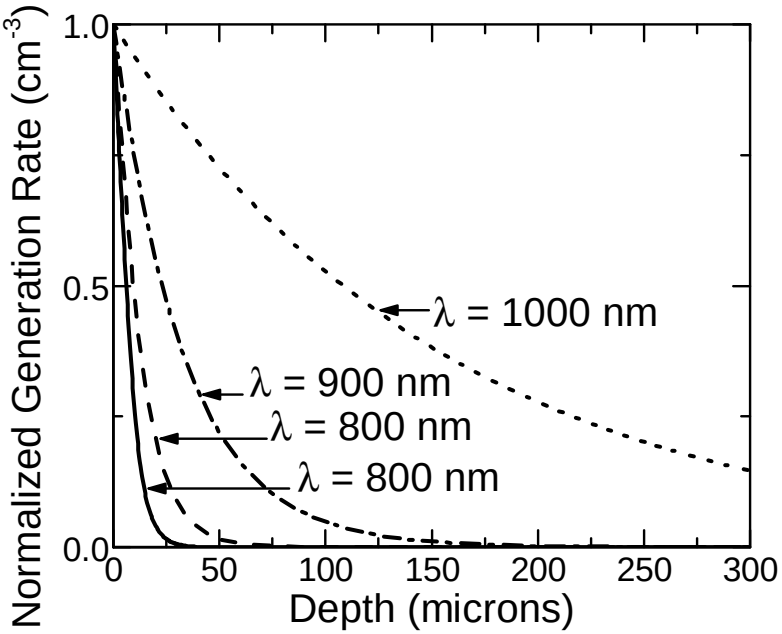


Figure 5.9: Normalized generation rate as a function of depth in silicon for several wavelengths

generates more carriers deeper in the silicon. Thus, these wavelengths will be more sensitive to reduced recombination due to the TiO_2 hole-blocker.

The EQE of the double-sided device is shown normalized to the EQE of the single-sided device in Figure 5.10. It is clear that for wavelengths >800 nm, the EQE of the double-sided device is higher than that of the single-sided device. The improvement in the EQE of the double sided device increases as the wavelength increases, as is made apparent by the normalized EQE. The normalized EQE can also be used to calculate the difference in J_{SC} for the two devices, or ΔJ_{SC}. The calculation is performed by using Equation 5.2, where $\Delta EQE(\lambda)$ is the difference in EQE between the single sided and double sided devices and $S(\lambda)$ is the spectral irradiance, in this case the AM1.5G spectrum. The spectral irradiance represents the energy per square meter per wavelength which is incident on the solar cell. This is divided by the energy per photon at each wavelength to give the number of photons absorbed per wavelength. The $\Delta EQE(\lambda)$ represents the percentage of these photons which generate carriers

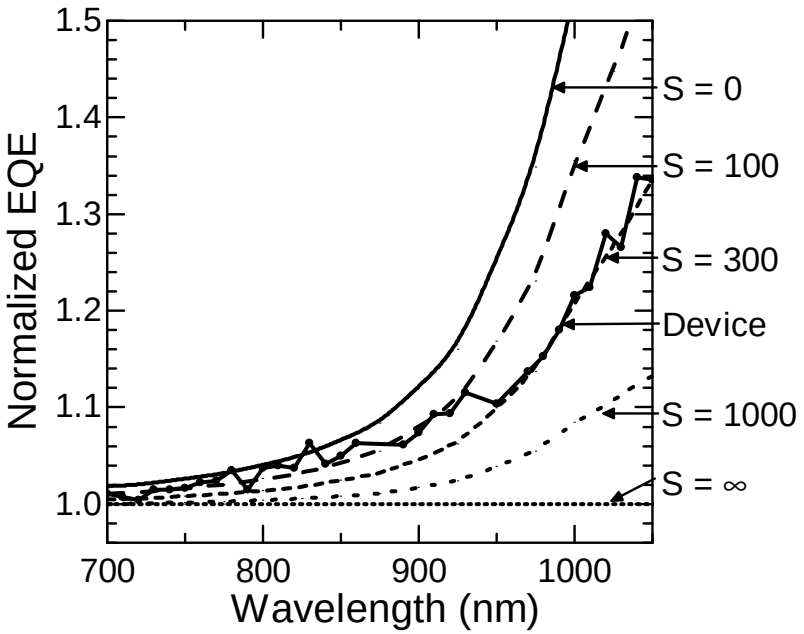


Figure 5.10: EQE of double-sided device normalized to the single-sided device. Data is compared to modeled spectra with various SRV or S values for the Si/TiO_2 interface.

which are collected and contribute to photocurrent in the double sided device which are not collected by the single sided. Therefore, integrating over all wavelengths yields a ΔJ_{SC} of $1.1\,\mathrm{mA\,cm^{-2}}$, in agreement with the observed increase in photocurrent measured in Figure 5.6.

$$\Delta J_{SC} = \frac{q}{hc} \int \Delta EQE(\lambda) S(\lambda) \lambda \partial \lambda \tag{5.2}$$

The improvement in the EQE, ΔEQE, depends on the SRV or S at the Si/TiO_2 interface. The optical generation profile can be used along with the continuity equation to calculate how many carriers will be collected at the front junction in the EQE measurement. For the single-sided device, recombination at the rear interface is essentially infinite. Therefore the boundary condition here is that the recombination current is limited by how fast the carriers can diffuse to the interface. For the double-sided device, the boundary condition is determined by the surface recombination at that interface. This is modeled numerically for several values of SRV of the Si/TiO_2

interface in figure 5.10. As Figure 5.10 shows, the data agree best with a modeled SRV of $300\,\mathrm{cm\,s^{-1}}$.

5.3.4 Stored Minority Carrier Charge

The effectiveness of the TiO_2 hole-blocking layer can also be determined by measuring the stored minority hole charge Q_{stored} in the neutral n-type silicon of the device under forward bias. For the same current in forward bias, and thus the same slope of the hole concentration profile, the double-sided device will contain a greater Q_{stored} as indicated by the crosshatched area in Figure 2.3b. The reverse recovery method [78–85] was used to estimate Q_{stored} in the PST and single-sided devices. As described in Chapter 3, the reverse recovery measurement is performed by alternately forward biasing and reverse biasing the device. Under reverse bias, a transient reverse current I_R can be observed.

The reverse current is due to the holes leaving the silicon back to the PEDOT and will continue to flow up to a time t_{store}, at which point the hole concentration at the edge of the depletion region reaches equilibrium value, and I_R begins to fall. Q_{stored} is approximated by the product of I_R and t_{store}.

Figure 5.11 shows I_R as a function of time for a single-sided and a double-sided device. The double-sided device maintains a flow of I_R for a three-fold longer t_{store}, and therefore contains approximately a three-fold greater initial Q_{stored} compared to the single-sided device without TiO_2.

The stored charge measurement can also provide an estimate of the surface recombination velocity. Assuming minimal bulk recombination, the stored charge of the single sided device $Q_{store,SS}$ is represented by the area under the minority carrier profile shown in Figure 2.3b and is given by Equation 5.3

$$Q_{store,SS} = \frac{p'_{SS}(0)W}{2} \tag{5.3}$$

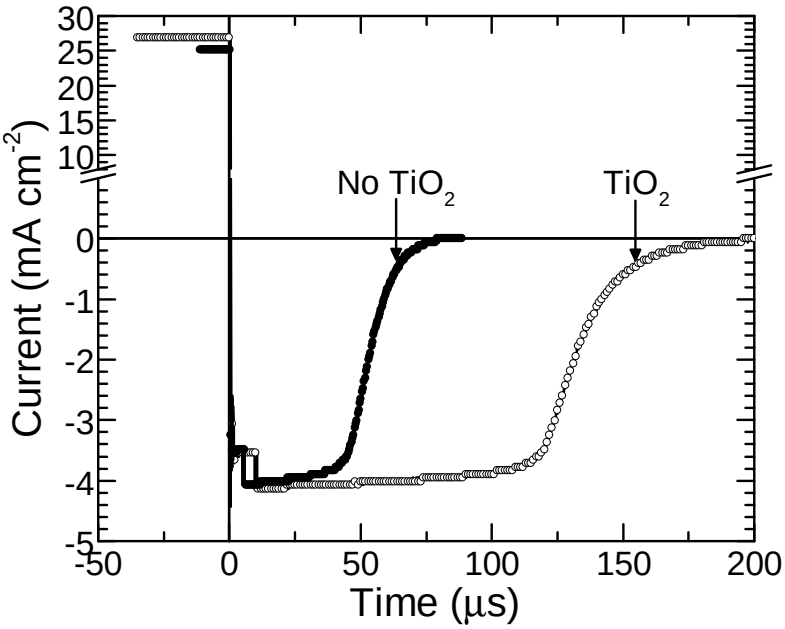


Figure 5.11: Reverse current as a function of time for the PST and single-sided solar cell in the reverse recovery experiment

Similarly, the stored charge within the double-sided device $Q_{store,DS}$ is given by Equation 5.4.

$$Q_{store,DS} = Wp'_{DS}(W) + \frac{p'_{SS}(0)W}{2} \tag{5.4}$$

Taking the ratio of the stored charge yields Equation 5.5.

$$\frac{Q_{store,DS}}{Q_{store,SS}} = 2\frac{p'_{DS}(W)}{p'_{SS}(0)} + 1 \tag{5.5}$$

The forward current in the single sided device is dependent on the diffusion profile of holes in Equation 2.2 must equal the current due to holes recombining at the Si/TiO_2 interface given by Equation 2.3. Combining Equation 2.2 and Equation 2.3 yields an expression for $p'_{DS}(W)/p'_{SS}(0)$, and substituting this into Equation 5.5 yields Equation 5.6, in which the ratio of stored charge depends directly on the SRV of the TiO_2 hole-blocker.

$$S_{Si/TiO_2} = \frac{D_{p,N}}{2W}\left(\frac{Q_{store,DS}}{Q_{store,SS}} - 1\right) \tag{5.6}$$

Using the data from Figure 5.11, the ratio of the stored charge is 2.72 and the estimated SRV from the charge storage measurement is $345\,\mathrm{cm\,s^{-1}}$. It should be noted that this is only a first order estimate, as it neglects the effect of recombination at the back and front interfaces during both the forward bias and reverse bias phase. More precise modeling incorporating recombination during the reverse bias phase is being carried out by Alexander Berg in our lab and will be reported elsewhere.

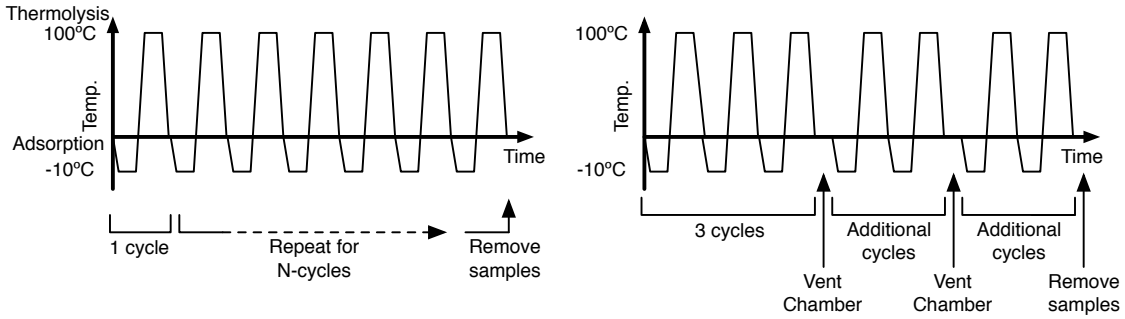
5.4 Thickness effects of TiO_2 films

Thus far, the discussion of PST solar cells has not considered the effect of the TiO_2 thickness. As this section will show, the thickness of the TiO_2 film can have a significant impact on performance of the PST solar cells. Initial attempts at fabricating PST solar cells with thin ($< 2.5\,\mathrm{nm}$) films of TiO_2 were observed to be insufficient to provide good hole-blocking properties. The poor performance of thin TiO_2 films motivated the growth thicker films of TiO_2. However, the TiO_2 thickness obtained from the method introduced in Chapter 4 was observed to saturate with multiple deposition cycles around 4 nm. Modified deposition methods were therefore developed for obtaining thicker ($> 4\,\mathrm{nm}$) TiO_2 films, and these films were incorporated into PST devices.

The modification of the growth process in order to achieve thicker TiO_2 layers is presented in section 5.4.1. The mechanisms underlying the poor performance of thin TiO_2 films in PST solar cells are presented in section 5.4.2. The mechanisms underlying the performance of thick ($> 4\,\mathrm{nm}$) TiO_2 films are presented in section 5.4.3.

5.4.1 Modified Growth Process for Thick TiO_2

The first approach to grow thicker layers was to simply increase the number of adsorption and thermolysis cycles used in the low-temperature CVD process described in



(a) (b)

Figure 5.12: (A) standard TiO_2 deposition process using multiple cycles and (B) modified process with chamber vent between additional cycles. All adsorption and thermolysis times were kept constant at 10 min, and the chamber vent was typically 1 min to 5 min

Chapter 4. The hypothesis was that more of the titanium alkoxide precursor would adsorb and thermolyze with each subsequent cycle, increasing the thickness of the overall film. This process is shown schematically in Figure 5.12a. In this approach, samples are placed into the chamber and undergo a set amount of repeated cycles before removal.

However, the thickness of TiO_2 layers obtained by simply increasing the number of cycles was observed to saturate, as shown by Figure 5.13. These data points represent samples that underwent multiple cycles (with the exception of the 1-cycle data point) before removal from the chamber. It is hypothesized that the presence of unreacted organic groups left from incomplete decomposition of the titanium(IV) tetra-(*tert*-butoxide) precursor on the surface of the TiO_2 film can prevent the adsorption of more precursor. If no precursor molecules adsorb to the surface of the film, then there is no TiO_2 created during the thermolysis step and the thickness of the film does not increase with further cycling. As a result, the growth of the TiO_2 films is observed to saturate at $\sim$3 nm to 4 nm, as shown.

To facilitate decomposition of the organic groups that may be present on the surface of the TiO_2 film, the introduction of oxygen and water vapor from laboratory ambient was investigated. Since the titanium(IV) tetra-(*tert*-butoxide) precursor is

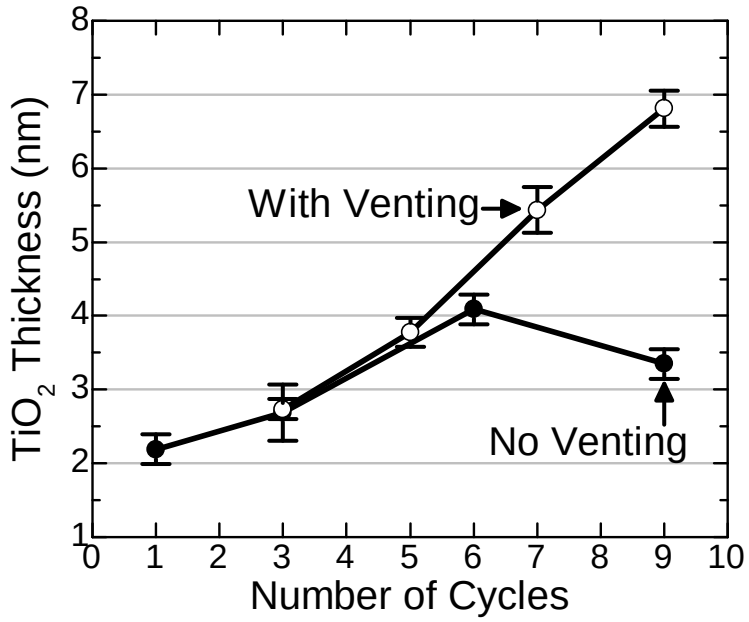


Figure 5.13: Thickness of TiO_2 films versus number of cycles using venting process (hollow circles) and without venting (filled circles).

quickly broken down upon exposure to oxygen and water vapor, it was hypothesized that exposure to laboratory ambient would allow unreacted organic groups on the surface of the TiO_2 film to decompose. By reacting the surface organic groups, the titanium alkoxide should then able to adsorb to the TiO_2 surface, resulting in more TiO_2 deposition upon further cycling.

Laboratory ambient was introduced by venting the deposition chamber between cycles, as shown schematically in Figure 5.12b. After a number of cycles (typically 3), the chamber is vented and exposed to laboratory ambient for 1 min to 5 min. Then the chamber is pumped back down and additional cycles are run to add thickness to the TiO_2 film. Venting the chamber was observed to prevent the saturation of TiO_2 thickness with additional cycles, as shown in Figure 5.13. For the data shown, 3 cycles were run for the inital TiO_2 film, which resulted in $\sim$2.7 nm thickness. By venting the chamber and then running an additional 2 cycles, the thickness was increased to $\sim$3.8 nm, then $\sim$5.5 nm, and finally a $\sim$6.8 nm film was achieved.

Another growth method (which was developed by Gabriel Man) was investigated which uses a controlled pulse of vapor pressure from the precursor vial to obtain thicker TiO_2 growth. The process nominally follows the same procedure as the standard method described in Chapter 4, yet with a precursor valve that can be carefully controlled (The chamber used also has a slightly different geometry, however this is not anticipated to cause a difference). This method controls the opening speed of the precursor bulb in order to obtain a spike in the chamber base pressure. It is hypothesized that the spike in pressure is due to a burst of precursor vapor entering the chamber, which results in a thick coating of adsorbed precursor onto the samples. As a result, this method is observed to obtain TiO_2 films that are 5 nm to 12 nm thick, depending on location within the chamber.

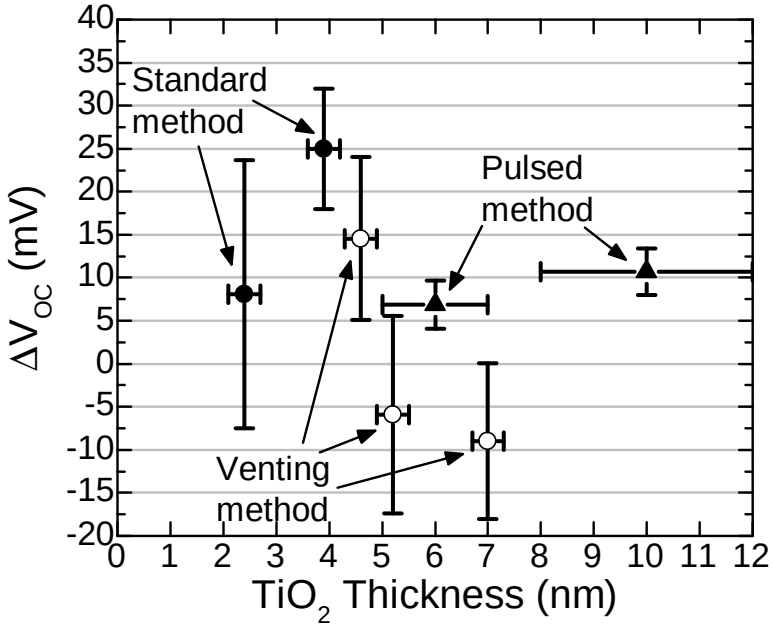


Figure 5.14: ΔV_{OC} as a function of the thickness of the TiO_2 hole blocking film in PST solar cells for various growth methods. Error bars represent the standard deviation of a batch of nine devices

The various growth methods discussed were used to deposit TiO_2 films for incorporation into PST solar cells, and the improvement in V_{OC} over the PEDOT/Si

control devices is shown in Figure 5.14. For TiO_2 films deposited using the standard growth procedure, a problem is observed in which TiO_2 films that are too thin do not demonstrate improvement in V_{OC}. Another issue is observed for TiO_2 films obtained using the venting growth process, in which the improvement in V_{OC} is observed to decrease with thicker films. Finally, experiments with the pulsed vapor deposition method show encouraging results for thick TiO_2 films, in contrast to the venting method. The mechanisms behind these observations are discussed in the following sections.

5.4.2 'Thin' TiO_2 and Aluminum Interaction

The requirements of a hole-blocking heterojunction, as outlined in Chapter 2, are having the correct band alignments and providing good surface passivation of crystalline silicon. The photoemission spectroscopy (PES) and Quasi-Steady State Photoconductance Decay (QSSPCD) measurements presented in Chapter 4 show that TiO_2 satisfies both of these requirements. Therefore, one would predict good performance from these films when incorporated into PST solar cells as BSFs. However, the fabrication process of a PST solar cell differs from that of a PES or QSSPCD measurement sample in that the TiO_2 is metalized. Metal deposition on top the TiO_2 film is required in order to form the cathode contact of the PST solar cell, whereas for PES or QSSPCD measurements the sample is comprised of a bare TiO_2 film on silicon.

The metalization process can have a significant effect on the performance of the PST solar cells. This is not surprising considering the impact that metalization had on the performance of the p-type Si/TiO_2 diodes discussed in Chapter 4. As is the case with the p-type diodes, in the PST devcies, the metal used to contact the TiO_2 is aluminum and is deposited via thermal evaporation. The evaporator used to deposit the aluminum for all devices presented in this chapter was the Edwards 306 system, which was shown to provide good p-type diodes. However, in a PST solar cell there

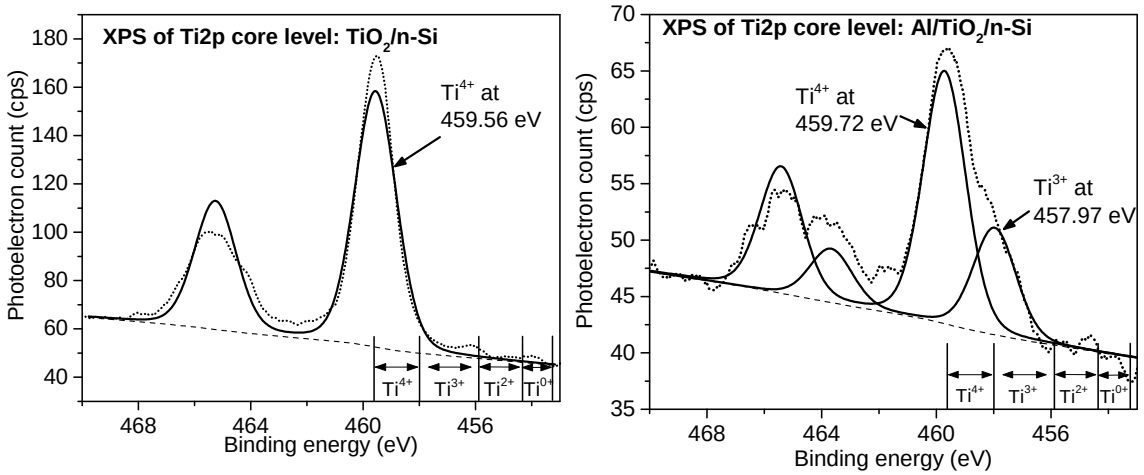


Figure 5.15: XPS scan of the titanium 2p core levels in a TiO_2 films on silicon substrate (A) without metal and (B) with thin (1 nm to 2 nm) film of Al. Dotted lines indicate measured spectra, solid lines indicate fitted Gaussian-Lorentz peaks, and thin dashed line indicated background noise. A range of binding energies is shown for the Ti2p3/2 level for Ti in the Ti^{4+}, Ti^{3+}, Ti^{2+}, and Ti^{0+} oxidation states, from the NIST database (Such reported values are useful only as a rough guide, as they are taken from measurements of bulk films, the binding energies of which can differ significantly from those of thin films, such as in this work). Measurement courtesy of Gabriel Man.

is no band-bending at the Si/TiO_2 interface as in the p-type diode, and therefore this interface is more sensitive to recombination.

X-Ray Photoemission Spectroscopy measurements revealed the effects of aluminum metalization on the TiO_2 films. The thermal evaporation process facilitates an interaction between the aluminum film and the TiO_2 in which the Al is oxidized and a mixed oxide is formed. Evidence for this reaction can be seen by scanning the titanium 2p core levels. A typical TiO_2 film deposited via low-temperature CVD only shows titanium in the Ti^{4+} state, as shown in Figure 5.15a. This is indicative of a stoichiometric TiO_2 film, as discussed in Chapter 4 and in previous work [39].

However, Figure 5.15b shows that after aluminum evaporation, the composition of the TiO_2 film changes. In addition to the Ti^{4+} peaks, an additional peak is observable at lower binding energy. The peak is located at $\sim$2 eV lower binding energy (a very

significant shift in the binding energy), and therefore indicates that this peak arises from titanium in the Ti^{3+} oxidation state. Therefore the XPS data provides evidence that the stoichiometric TiO_2 film changes chemically into a mixed $Al_xTi_yO_z$ oxide. In the formation of such a mixed oxide, if the aluminum reacts with the TiO_2 film it may also consumes a portion of it. It is speculated that the consumption of the TiO_2 film results in a thinner film, which leads to degraded hole-blocking of the heterojunction due to tunneling, and poorer PST devices.

5.4.3 Properties of 'Thick' TiO_2

The achievement of thicker TiO_2 films using the venting growth process was envisioned to enhance the open-circuit voltage achieved by the double-sided heterojunction devices. However, as Figure 5.14 shows, as the thickness of the TiO_2 films is increased with the venting method, the open-circuit voltage gain of the PST devices decreases to the point of becoming negative. The fact that V_{OC} begins to decrease *below* that of the control devices suggests that there is a parasitic effect happening due to the thicker films. One hypothesis is that the films may contain some form of trapped charge which causes a parasitic barrier, similar to that discussed in Section A.2. In this hypothesis, negative charges in the TiO_2 film would cause a shift downward in the Fermi level and upwards in the conduction band. Therefore, while there is no barrier to electrons in the silicon conduction band normally, negative charges in the TiO_2 may cause band-bending that results in a barrier. When excess electrons are generated due to photocurrent, they would normally simply diffuse to the cathode. However if a barrier is present in the conduction band of the TiO_2, a voltage drop would form in order to lower the barrier presented by the electric field of the conduction band, as is illustrated in Figur 5.16. This voltage would lower the open-circuit voltage achieved by the device just as in the case of the parasitic Schottky barrier contact discussed in Section A.2.

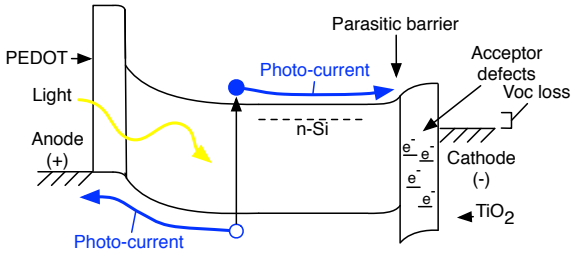
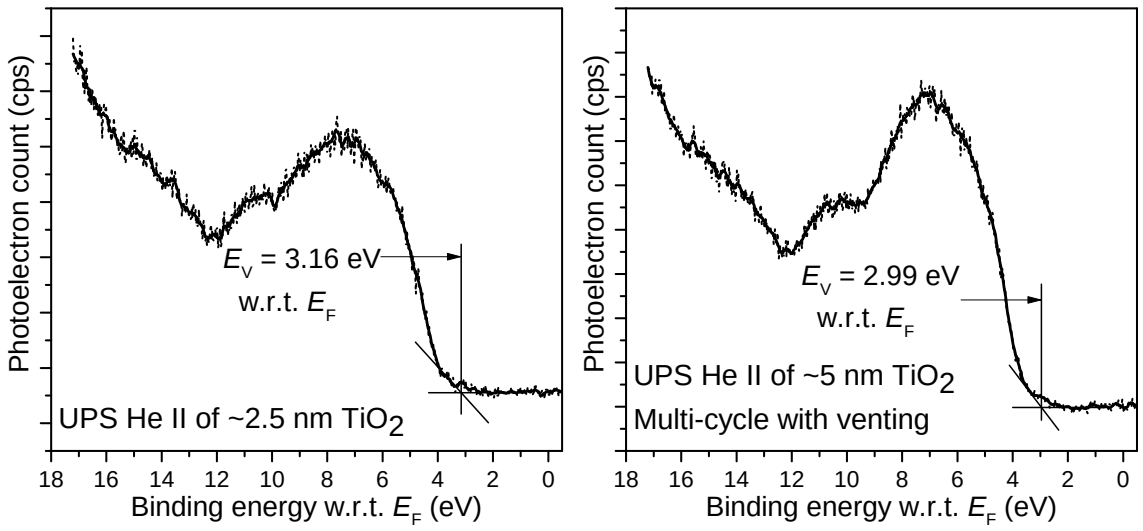


Figure 5.16: Band diagram illustration of a PEDOT/Si/TiO_2 solar cell showing negative charges causing a barrier for electrons at the cathode contact.



(a) (b)

Figure 5.17: UPS HeII scans showing valence band of (A) ∼2.5 nm TiO_2 and (B) ∼5 nm TiO_2 grown by venting process.

To study the mechanism behind the open-circuit voltage loss, photoemission spectroscopy was used to compare thick (5.2 nm) TiO_2 and thin (2.4 nm) TiO_2 films. UPS measurements showed that the valence band edge in the case of the thick TiO_2 films were shifted by 0.17 eV closer to the Fermi level than the case of the thin TiO_2, as shown by the HeII spectra shown in Figure 5.17. This ∼0.2 eV shift was mirrored in the IPES spectra of the conduction band states, the XPS spectra of the titanium 2p levels, and the oxygen 1s levels. This spectroscopy data show that the band alignments have not changed, rather the band bending in the silicon has changed.

The band bending of the silicon upwards at the Si/TiO_2 interface increases as a result of the thick TiO_2 film by $\sim$0.1 eV. A comparison of the band bending resulting from the different films is illustrated in Figure 5.18. These measurements support the stated hypothesis that there is a detrimental barrier being formed in the silicon conduction band due to thicker films of TiO_2.

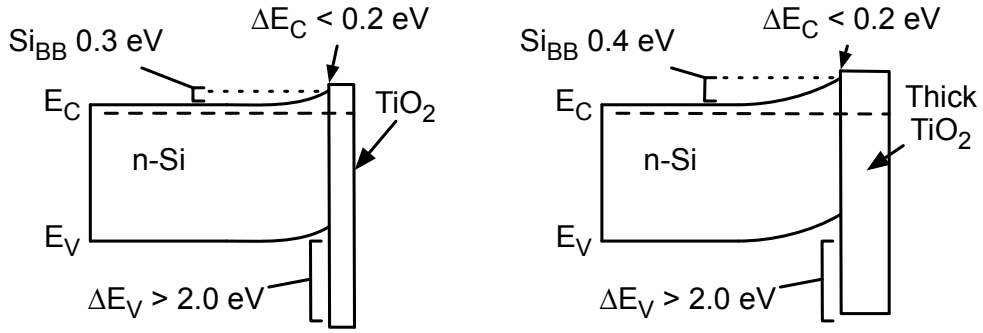


Figure 5.18: Comparison of band alignment for thin and thick TiO_2 films on n^+ silicon as measured by PES techniques by Gabriel Man. The band alignment of the Thick TiO_2 films show an increase the bending of the conduction band upwards, which supports the theory of thick TiO_2 films leading to a parasitic barrier at the back contact.

While the PST device data and photoemission spectroscopy data both support the hypothesis regarding negative charge, the source of these negative charges is not clear. One possibility is that the venting process introduces contaminants to the surface of the TiO_2 that become trapped as subsequent layers are grown. This hypothesis is also supported when considering the data from the PST solar cells which are fabricated using the pulsed vapor method. This method also achieves thick layers of TiO_2, however, improvement in the V_{OC} of PST devices which use these thick films is also observed and is shown in Figure 5.14. This shows that the ΔV_{OC} loss is not inherently due to thick TiO_2, but rather the method in which the thick layers are deposited. This therefore supports the possibility that the laboratory ambient is introducing contamination into the venting method.

5.5 PEDOT/Si/TiO_2 Solar Cell Conclusions

5.5.1 Summary of SRV Estimates

The data from the four measurements presented in Sections 5.3.1 through 5.3.4 show that the TiO_2 hole-blocker at the cathode serves to reduce recombination and dark current. The J-V characteristics in the dark and under illumination, the EQE, and the stored charge measurements all indicate that TiO_2 serves as a BSF to improve the PEDOT/Si solar cell. However, there is some disagreement between the magnitude of the effect between measurements. The estimated SRV values from the various measurements are summarized in Table 5.2.

Table 5.2: Summary of Si/TiO_2 SRV estimates

Measurement	Estimated SRV$\mathrm{cm\,s^{-1}}$
Dark J-V	460
Light J-V	150-360
EQE	400
Stored Charge	345

The value of SRV obtained from ΔV_{OC} stands out as the lowest estimate obtained, and merits further discussion. Due to the float zone silicon being double-side polished, the evaporation of aluminum onto the n-type silicon can form a electron Schottky barrier rather than an ohmic contact. Under illumination the parasitic Schottky barrier becomes forward biased and results in a voltage loss, reducing the open-circuit voltage observed. As discussed in section A.2, scribing of the silicon backside was employed to mitigate this effect at the back contact of the PEDOT/Si control device, however, it is possible that a small barrier still exists. If this is the case, the V_{OC} of the single-sided PEDOT/Si control device would be artificially lowered and

ΔV_{OC} would be artificially raised, resulting in an underestimation of the SRV at the Si/TiO_2 interface.

Effect of a Parasitic Barrier at the Cathode

To better illustrate the effect that a parasitic barrier can have, a PEDOT/Si device with a *large* parasitic barrier (no backside scribing at all) is presented and compared to a PST device with a ∼4 nm. Equation A.1 shows that the V_{OC} loss due to a parasitic Schottky barrier increases linearly with the photocurrent. Therefore, the effect of the back contact becomes apparent by comparing the dark current characteristics to a plot of V_{OC} for various levels of illumination. Ideally, the open-circuit voltage should be exactly where a given short-circuit current intersects with the dark J-V plot. Thus, when comparing a single-sided PEDOT/Si device to a PST device, the ΔV_{OC} should ideally agree exactly with the observed shift in the dark current. However, due to the presence of a parasitic Schottky barrier in the control device, the measured V_{OC} can deviate from this ideal behavior.

Figure 5.19 presents the dark current-voltage characteristics (solid lines and circles) of a PEDOT/Si solar cell with a large parasitic barrier, compared to those of a PST device in Figure 5.19. Also plotted in Figure 5.19 are the V_{OC} and J_{SC} obtained from measuring the same devices under various levels of illumination (filled and hollow diamonds represent the PEDOT/Si and PST devices, respectively). The PST device exhibits a lower dark current than the PEDOT/Si device, as expected, due to the inclusion of the TiO_2 back-surface field (section 5.3.1). The V_{OC} and J_{SC} data at lower illumination intensity (1/160 and 1/40 suns) show good agreement with the dark current-voltage curves. However, as the illumination level increases to 1-sun, the measured V_{OC} deviates from that which would be predicted by the dark current-voltage measurement for the PEDOT/Si unscribed device. This large V_{OC} loss is observed for the PEDOT/Si device with no backside scribing, but not for the

PST device. This suggests that the TiO_2 passivation de-pins the silicon surface at the cathode and thereby eliminates any parasitic Schottky barrier.

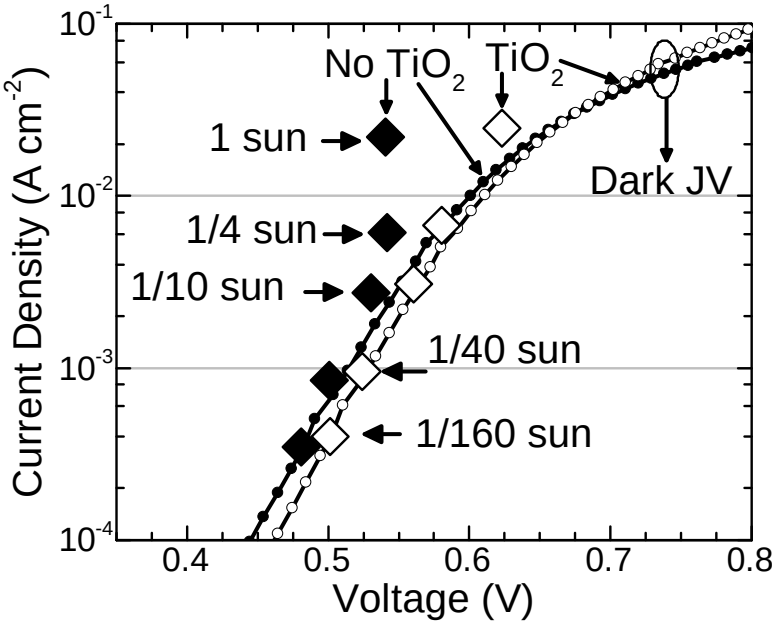


Figure 5.19: Dark current characteristics for a PEDOT/Si (solid line with filled circles) and PST solar cell (solid line with hollow circles), compared to the V_{OC} measured at various levels of illumination (filled diamonds for PEDOT/Si device and hollow diamonds for PST device).

The devices shown in Figure 5.19 represent an extreme case in which the observed ΔV_{OC} can be overestimated due to a large parasitic barrier at rear contact of the control PEDOT/Si device. The large ΔV_{OC} in this case is on the order of $\sim$80 mV, much larger than the $\sim$10 mV discrepancy in the dark and illuminated current-voltage measurements of Sections 5.3.1 and 5.3.2. However, this discussion serves to maintain the hypothesis that a smaller parasitic barrier may be present even after backside scribing of the PEDOT/Si devices and accounts for a small yet significant $\sim$10 mV loss in V_{OC} of these devices.

Recombination at PEDOT/Si Interface

The estimation of SRV also makes assumptions regarding the front interface that may benefit from refinement. In the case of the dark current reduction, the estimation of SRV is made with the assumption that all of the dark current is comprised of holes injected from the PEDOT into the n-type silicon ($\alpha = 1$). This is also assumed when calculating the SRV based on the open-circuit voltage under illumination. However, if a significant component of the dark-current is due to recombination at the front interface ($\alpha < 1$), then the effect of the hole-blocking TiO_2 will be reduced, and the calculation of SRV from dark and illuminated measurements and may be an overestimate.

This can be seen by modifying Equation 2.7 to account for an $\alpha < 1$. An $\alpha < 1$ means that there is an electron component of the dark current at the PEDOT/Si junction. Since the total current is simply the sum of the electron and hole components, the electron current component can be expressed as a function of alpha and $J_{0,holes}$, and is shown in Equation 3.7.

$$J_{0,electron} = J_{0,total} - J_{0,holes} = \frac{J_{0,holes}}{\alpha} - J_{0,holes} = J_{0,holes}\frac{1-\alpha}{\alpha} \tag{5.7}$$

The total current for single-sided PEDOT/Si device can then be written as shown in Equation 5.8.

$$J_{0,total,SS} = J_{0,holes} + J_{0,electrons} = J_{0,holes} + J_{0,holes}\frac{1-\alpha}{\alpha} \tag{5.8}$$

In a PST device, however, the blocking factor of the rear heterojunction will reduce the hole current, and the total current is given by Equation 5.9.

$$J_{0,total,SS} = J_{0,holes} + J_{0,electrons} = J_{0,holes}BF + J_{0,holes}\frac{1-\alpha}{\alpha} \tag{5.9}$$

Substituting Equations 5.8 and 5.9 into Equation 2.6 (assuming that $\frac{J_{SC}}{J_0} \gg 1$ for both the single and double-sided devices, $J_{SC,DS} \approx J_{SC,SS}$) and simplifying, a new expression for ΔV_{OC} is obtained, as shown by Equation 5.10. Figure 5.20 shows that for $\alpha < 1$, the improvement in V_{OC} expected from the hole-blocker is substantially reduced.

$$\Delta V_{OC} = \frac{nkT}{q} \ln\left(\frac{1}{\alpha(BF-1)+1}\right) \tag{5.10}$$

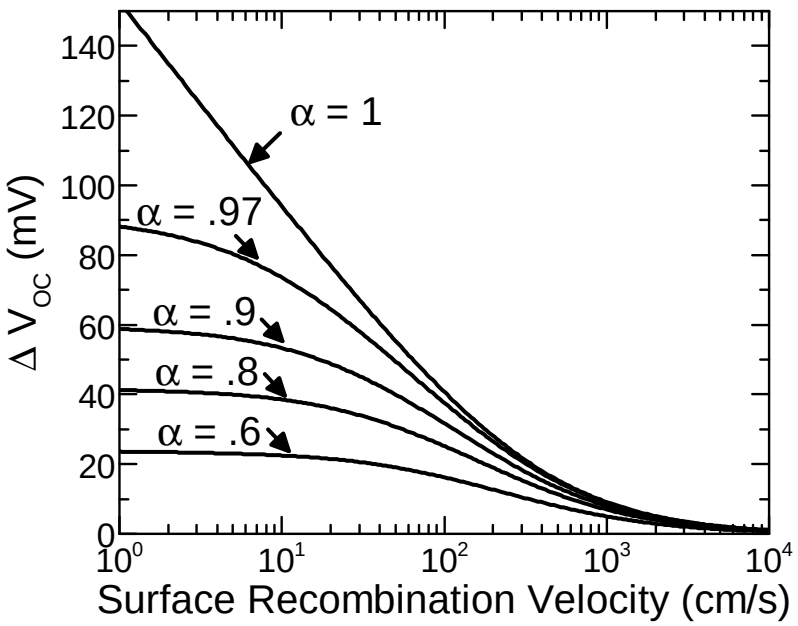


Figure 5.20: Dependence of ΔV_{OC} on the SRV of the rear BSF, for various values of α of the front junction.

The assumption that all dark current in the PEDOT/Si solar cell is due to injected holes ($\alpha = 1$) is supported by the reverse recovery measurements in Chapter 3. However, the modeling as presented assumes no recombination at the PEDOT/Si interface during the reverse current phase of the measurement. The analysis of reverse recovery measurements of stored charge in the single-sided and PST devices presented in section 5.3.4 also makes this assumption. In both analyses, including the effect of recombination at the PEDOT/Si interface during the reverse phase will provide a

clearer picture of α of the PEDOT/Si heterojunction and the SRV of the Si/TiO_2 interface in a PST device.

5.5.2 Conclusions

Overall, however, the experimental observations from the dark J-V, illuminated J-V, EQE, and stored charge measurements all indicate that the TiO_2 serves as an effective hole-blocking heterojunction. The dark J-V, EQE, and stored charge measurements all suggest that the SRV obtained at the rear interface is on the order of $150\,\mathrm{cm\,s^{-1}}$ to $460\,\mathrm{cm\,s^{-1}}$. While acknowledging that these analyses could be refined, the agreement is good to first-order. The successful demonstration of a low-temperature, plasma-free heterojunction solar cell was accomplished and represents promise for future devices.

The thickness of the TiO_2 layer has a significant effect on the performance of the PST solar cell. It was observed that if the TiO_2 film is too thin, metalization can render the film ineffective at preventing hole recombination at the cathode. It was also observed that the manner of depositing thicker TiO_2 films can influence whether the TiO_2 acts in a beneficial manner as a BSF or causes a parasitic barrier at the cathode contact. Two modifications from the standard method for growing TiO_2 presented in Chapter 4 were compared. Further investigation of the thick TiO_2 films obtained from these methods via photoemission spectroscopy will likely be very useful.

In summary, the data presented in this chapter represents the first demonstration of the use of TiO_2 as a selective heterojunction to form a BSF on a crystalline silicon solar cell. The use of a PEDOT/Si heterojunction as the front junction of the device makes the entire solar cell follow a low-temperature process which does not require any thermal diffusion or plasma processing steps. The PST solar cell therefore represents a promising architecture for future heterojunction solar cells.

Chapter 6

Silver Nanowire Networks on PEDOT/Si Solar Cells

6.1 Introduction

One approach to solving the issue of the limited conductivity of PEDOT:PSS films is to make use of another transparent conductor. While the standard for transparent conductors has been Indium Tin Oxide (ITO), deposition of ITO films requires a plasma deposition process. Because the motivation of the low-temperature heterojunction solar cell is to minimize processing complexity, this is not ideal. Additionally, the ITO plasma would likely result in damage or modification of the PEDOT:PSS film. As an alternative to ITO, silver nanowire (AgNW) networks are gaining interest due to their conductive and transparent properties. In comparison to ITO, the AgNW networks offer better mechanical robustness [146] as well as compatibility with facile deposition methods such a spray coating and spin-coating [147, 148]. Because of this, AgNW networks are promising for application in large-scale, roll-to-roll manufacturing processes [149] and are well suited to complement the low-temperature heterojunction solar cells developed in this work.

Much of the current work on AgNW networks is focused on post-processing methods that enhance their conductivity. This is accomplished by reducing contact resistance between the individual nanowires that comprise the network. The contact area between individual nanowires is generally small, so the contact resistance can be reduced by simply increasing this area. Other approaches seek to remove residues which may remain on the surface of the nanowires as a byproduct of synthesis [150].

Several methods of post-processing AgNW networks have been demonstrated that are effective at enhancing conductivity, yet are unsuitable for application to a PEDOT/Si solar cell. One common method is a furnace anneal of 100 °C to 200 °C for about an hour [151, 152]. This is not ideal as the PEDOT/Si interface would likely degrade in such conditions. Another simple approach is to use mechanical stress in order to fuse the nanowires in the network together [153, 154]. While these methods are both simple and effective, they are either time consuming or may be too aggressive for delicate substrates and films.

For these reasons, optical post-processing methods are attractive for application on PEDOT/Si devices. Optical methods are both fast and scalable, and can be very effective at welding nanowire junctions. The sources used can range from broadband halogen lamps [155], high-intensity lamps [156–158], and pulsed lasers [159]. However, the use of broadband lamps will result in heating of the entire sample, which may be non-ideal. Laser processing is particularly attractive due to the highly efficient coupling of 355 −nm light directly into a plasmon resonance of the nanowire junctions [159]. Because of this coupling, the energy from the laser is concentrated at the junctions and not along the length of the nanowires or transferred to the bottom substrate.

The work in this chapter was done in collaboration with Joshua Spechler, and presents the use of laser annealing to reduce the resistance of silver nanowire networks deposited on PEDOT/Si solar cells. Section 6.2 presents the fabrication process of

the AgNW/PEDOT electrodes and the lasering process. Sections 6.3 and 6.4 discuss effect of laser sintering on the conductivity and transparency of the AgNW/PEDOT films. Section 6.5.3 presents the results of using such laser-processed AgNW networks on PEDOT/Si solar cells.

6.2 Fabrication and Processing of AgNW Networks

For measurements of optical transparency and sheet resistance, AgNW/PEDOT:PSS filsm were fabricated on 1 inch×1 inch glass slides. The glass slides were cleaned using a solvent clean, which involved a baths of acetone, methanol, and isopropanol with ultrasonic agitation for 5 minutes each before drying using nitrogen gun. PEDOT:PSS films were spin-coated onto the glass slides at 4000 rpm for 210 s. PEDOT:PSS was purchased as 1.4 % dispersion by weight in water (Clevios PH1000) and 10 % w/w dimethyl sulfoxide (DMSO) was added to enhance the conductivity of the film and 0.25 % Zonyl FS-300 surfactant was added to facilitate adhesion [55–57].

The AgNWs used in this work have a mean length of 15 µm and a mean diameter of 90 nm. They were purchased from Blue Nano Inc. and dispersed in methanol at a concentration of 2 mg/mL. Coating is performed by mounting the glass slides on a motorized stage that was heated to 65 °C. The stage is scanned underneath a spray nozzle that uses 35 psi nitrogen to spray the AgNW/methanol solution at a rate of ∼2 mL/min. Eight passes of the spray resulted in the ∼10 % area coverage AgNW films. Thermally evaporated silver contact pads spaced 8 mm apart are deposited to form 4-point test structures.

The PEDOT/Si solar cells were fabricated in the manner described in Chapter 3 up to and including the spin-coating of the PEDOT:PSS. After coating of the PEDOT:PSS, the solar cells received AgNW deposition via the same method used to

fabricate samples for optical transparency and sheet-resistance measurements. To complete fabrication of the solar cell a thermally-evaporated silver busbar with a small contact pad for probing was deposited on top of the AgNW/PEDOT:PSS layers. The busbar was used was 100 µm wide and 3 mm long, with a contact pad 200 µm by 200 µm located in the center of the device. The area of the busbar was 2 % of the total device area of 4 mm×4 mm. On average, current has to flow laterally about 1 mm in the AgNW/PEDOT network. The fabrication process is shown in Figure 6.1.

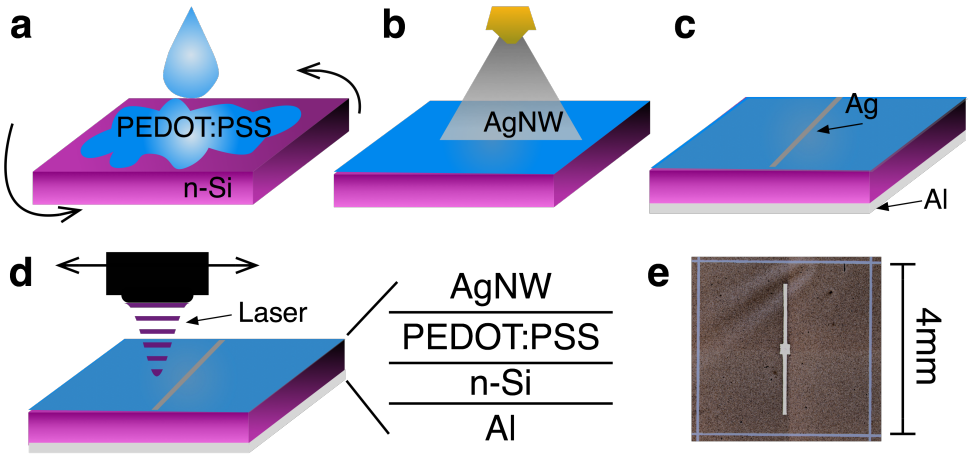


Figure 6.1: Schematic of the fabrication process for the hybrid organic PEDOT:PSS/n-Si heterojunction cell. A) PEDOT:PSS is deposited onto n-Si via spin coating. B) A coating of AgNW is spray coated on top of the PEDOT:PSS to serve as the transparent electrode. C) A front contact busbar and back electrode are added via evaporation. D) The AgNW network is laser processed in a raster fashion. E) A photograph of the top side of a completed cell, showing the shape of the contact busbar.

The post-processing of the AgNW networks is performed using a Coherent AVIA: 355-nm diode-pumped solid-state Nd:YVO_4 laser, with 27-ns pulses. The laser is focused through a 5× objective (NA = 0.13) and spot size is kept constant at a diameter of 500 µm. Each area of the sample received 625 pulses, and the laser is rastered using an XY translation stage at a speed of 1200 mm/ min. For all experiments except where otherwise noted, a fluence of 23.5 mJ cm^{-2} was used. When optimizing for fluence we change the laser energy via active Q-switching while leaving the spot size

unchanged. The post-processing of both AgNW/PEDOT/Si solar cells and optical transparency/sheet resistance samples occurred at room temperature in laboratory ambient.

6.3 Conductivity of AgNW/PEDOT:PSS Films

The conductivity of the AgNW networks depends on the density of the network and contact resistance between individual nanowires. By density, we refer to how many nanowires are present in a given area, as more nanowires per area will result in parallel conduction pathways and a better conductivity. The amount of surface area that is covered by the AgNW network is roughly quantified by using scanning electron microscopy imaging. The sheet resistances of various coverage AgNW networks are shown compared to a thin PEDOT:PSS film on glass in Figure 6.2. The AgNW films as deposited offer a significant reduction in sheet resistance in comparison to the PEDOT:PSS film. As the AgNW coverage increases, so does the number of conductive current paths in the network increases and therefore the sheet resistance decreases.

The sheet resistance of the films after laser processing is also shown in Figure 6.2. While the sheet resistance of the PEDOT:PSS is not observed to change because of the laser treatment, the contact resistance is observed to decrease significantly. The fractional change in sheet resistance is greater for less dense networks of AgNW, and this is attributed to the number of contact points in the network. For sparse networks, there are few overlaps between individual nanowires, so the contact resistance at these points influences the resistance of the network greatly. As more AgNWs are added to the network the number of contact points increases and act in parallel, so a reduction in the contact resistance has a smaller effect on the resistance of the overall network.

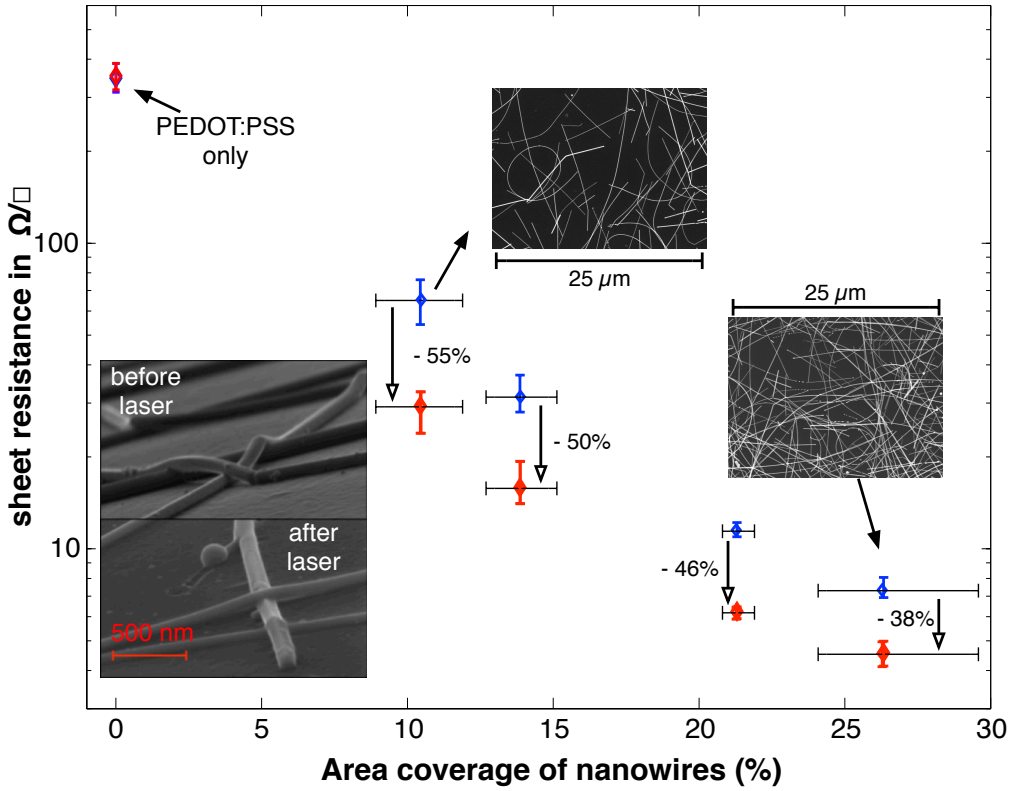


Figure 6.2: Sheet resistance before and after laser processing of various area coverages of AgNWs, as measured via 4-point measurements and SEM image thresholding. Insets show (clockwise from top) SEM image of low (10 %) and high (26 %) AgNW networks, and close up SEM image of AgNWs before and after laser processing showing junction fusing.

6.4 Transparency of AgNW/PEDOT:PSS

Increasing the conductivity of AgNW films comes with the familiar tradeoff of decreasing the transmission through the film. The transmittance (averaged from 400 nm to 700 nm) for AgNW films of various densities are presented in Figure 6.3. The data for specularly transmitted light are shown compared to the total (specular + diffuse) transmitted light as measured using a Hitachi U-3410 recording spectrophotometer with an integrating sphere. As expected, denser AgNW networks result in more shading and less light transmission. However, such nanometer scale nanowires also serve to scatter the transmitted light, resulting in more diffuse transmission.

Table 6.1: Effect of lasering on sheet resistance of AgNW networks ($23.5\,\mathrm{mJ\,cm^{-2}}$ laser fluence)

Film	$\Delta R_S\Omega/^2$ %
PEDOT:PSS only	<1 %
AgNW (11 ± 2) %/PEDOT:PSS	−55 %
AgNW (14 ± 2) %/PEDOT:PSS	−50 %
AgNW (22 ± 1) %/PEDOT:PSS	−46 %
AgNW (26 ± 3) %/PEDOT:PSS	−38 %

While decreased light transmission is obviously detrimental for solar cell performance, diffuse transmission can serve to benefit light absorption in the absorber material. By increasing the angle of transmission into the absorber, the scattering of light effectively increases the path length of transmitted light, allowing more light to be absorbed. The amount of diffuse or scattered light in Figure 6.3 also increases along with the nanowire density, as is expected.

6.5 Lasered AgNWs on PEDOT/Si Solar Cells

In this work, AgNW networks were applied directly onto a SOH solar cell and sintered via laser processing. Laser processing is shown not to detrimentally affect the SOH device, and helps to improve the sheet resistance of the AgNW network serving as the top transparent conductor. All devices were measured after deposition of the nanowire networks, and then remeasured after laser treatment. This method was employed to eliminate batch-to-batch variation in the nanowire coatings. Therefore the changes due to laser treatment represent a measurement on the same device before and after laser treatment. This section presents the effect of laser power and AgNW density on the PEDOT/Si solar cells.

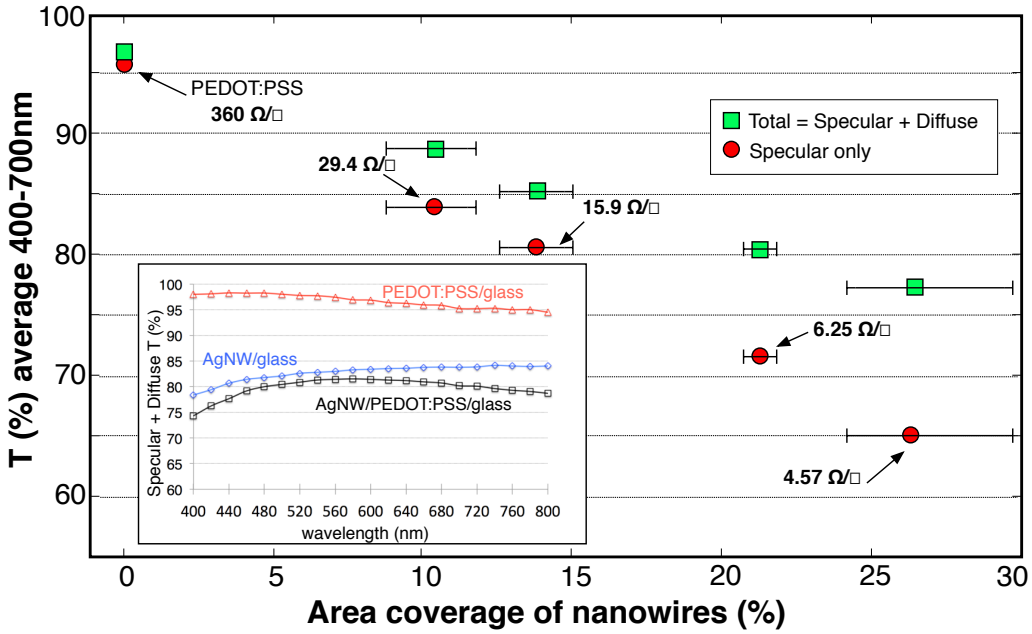


Figure 6.3: Optical properties of the AgNW/PEDOT:PSS/glass electrodes as a function of the nanowire area coverage in average transmission from 400nm-700nm (roughly the visible spectrum) after laser processing. The horizontal error bars, as well as the sheet resistance numbers (after laser sintering with fluence of 23.5 mJ cm^{-2}), are those from Figure 6.2. Inset is a sample spectrum through the visible (400-800nm) comparing the PEDOT:PSS/glass, AgNW/glass, and AgNW/PEDOT:PSS/glass electrodes for 26 % nanowire coverage. All the values have the glass substrate subtracted.

6.5.1 Laser power effects

An initial study was conducted on SOH devices to find the optimal power for the laser treatment. For this optimization, low density ((6 ± 1) %) AgNW films were utilized in order to maximize the observed affect of the laser treatment on performance. A range of laser fluence from ~5 mJ cm^{-2} to 34 mJ cm^{-2} was used. The absolute values of solar cell performance from these devices are poor due to the low density AgNW films used. However, this provides a large change in the parameters that is easily observed to peak for laser fluences of 20 mJ cm^{-2} to 25 mJ cm^{-2}, as shown in Figure 6.4.

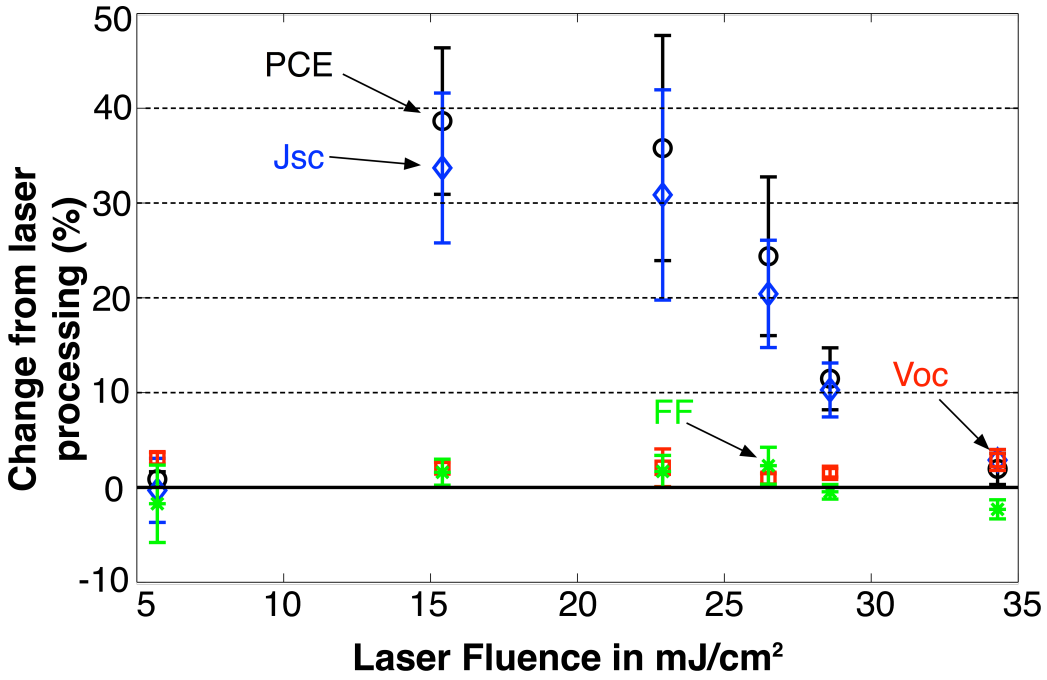


Figure 6.4: Relative change in solar cell parameters (V_{OC}, J_{SC}, FF, η) versus laser fluence for a AgNW/PEDOT/Si device with a low ($(6 \pm 1)\,\%$) coverage AgNW electrode.

6.5.2 AgNW density effects

Solar cells were fabricated with top electrodes of low, medium, and high densities of nanowires, corresponding to $(6 \pm 1)\,\%$, $(16 \pm 2)\,\%$, and $(25 \pm 3)\,\%$ area coverages. The metal busbar (dimensions specified in Section 6.2) was located in the middle of the device as shown in Figure 6.1. All devices were measured before and after treatment of the optimal laser fluence. It is important to note here that the substrate used in the case of the high density coverage was a $0.5-\Omega$cm phosphorus-doped ($1 \times 10^{16}\,\mathrm{cm}^{-3}$) silicon wafer, while the medium and low devices were made on $2-\Omega$cm phosphorus doped ($1 \times 10^{15}\,\mathrm{cm}^{-3}$) substrates. While this affects the open-circuit voltage of the devices, the relative changes observed in fill factor and short-circuit current are attributed to the laser processing. The solar cell parameters are summarized in Table 6.2 and the J-V characteristics under illumination are presented in Figure 6.5

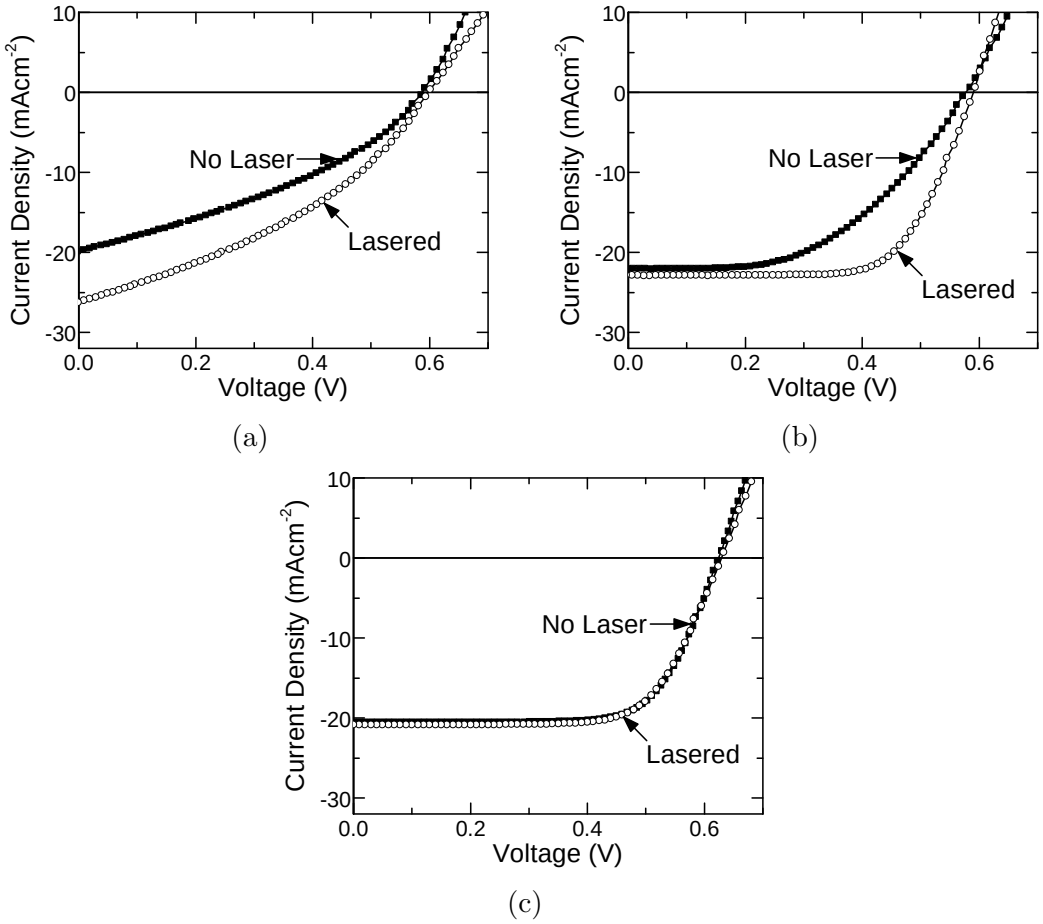


Figure 6.5: Current-Voltage characteristics of AgNW/PEDOT/Si solar cells with (A) 6 % (low), (B) 16 % (medium), and (C) 25 % (high) nanowire coating density. Filled circles and hollow circles show device data before and after laser processing, respectively.

The high coverage devices exhibit minimal changes as a result of the laser processing. This observation suggests that since the AgNW coating is so dense, the limiting factor of series resistance in this device is not the sheet resistance of top electrode. The sheet resistance of a high coverage AgNW coating is shown in Figure 6.2 to reduce from $\sim 7\,\Omega/\square$ to $4\,\Omega/\square$. Since high coverage AgNW coatings have a very low sheet resistance to start with, the change due to lasering therefore does not reduce the overall resistance of the device very significantly. The medium coverage devices, in contrast, are observed to benefit significantly from the laser processing. The improvement in the FF from 56 % to 66 % contributes to a gain of 1.9 % in absolute

Table 6.2: Performance parameters for PEDOT/Si solar cells with laser processed AgNW films

AgNW coverage and treatment	V_{OC}(mV)	J_{SC}(mA cm^{-2})	FF(%)	η(%)
25 % before laser	620 ± 1	20.4 ± 0.1	76 ± 1	9.0 ± 0.1
25 % after laser	630 ± 5	20.8 ± 0.1	69 ± 1	9.0 ± 0.1
16 % before laser	580 ± 4	22.4 ± 0.7	56 ± 3	7.3 ± 0.4
16 % after laser	590 ± 5	23.7 ± 1.1	66 ± 3	9.2 ± 0.2
6 % before laser	584 ± 1	17.8 ± 3.6	34 ± 2	3.6 ± 0.9
6 % after laser	590 ± 3	23.5 ± 3.7	35 ± 3	5.0 ± 1.1

PCE. The other solar cell parameters are not observed to change significantly, as is expected. Finally, the low coverage devices also showed significant improvement. However these devices benefited primarily through an increase in the short-circuit current, which is expected for devices with very high series resistance.

The effect of high series resistance on the short-circuit current density of low-coverage nanowire devices can be understood via the non-ideal solar cell model presented in Chapter 1. The non-ideal solar cell model in Figure 1.8 can be considered with an infinite shunt resistance. Therefore the only elements considered here are the series resistance R_S, the diode I_0, and the photocurrent I_{photo}. We can normalize the series resistance to the 'natural' resistance as given by equation 6.1. In this manner the series resistance effect can be compared regardless of the absolute parameters of the device.

$$R_{norm} = R_S \frac{I_{photo}}{V_{OC}} \tag{6.1}$$

Figure 6.6 shows the change in the normalized solar cell parameters as a function of changing the normalized series resistance. In the regime where $R_{norm} < 0.8$, the main effect of increased series resistance is to decrease the fill factor of the solar cell. This is the expected effect of losing power due to the generation of a voltage across

R_S, and the medium coverage devices are operating within this regime. As the series resistance continues increasing past$R_{norm} < 0.8$, the effect on the fill factor begins to diminish and the short-circuit current begins to suffer. This explains the J_{SC} effect that is observed with the low coverage density nanowire networks.

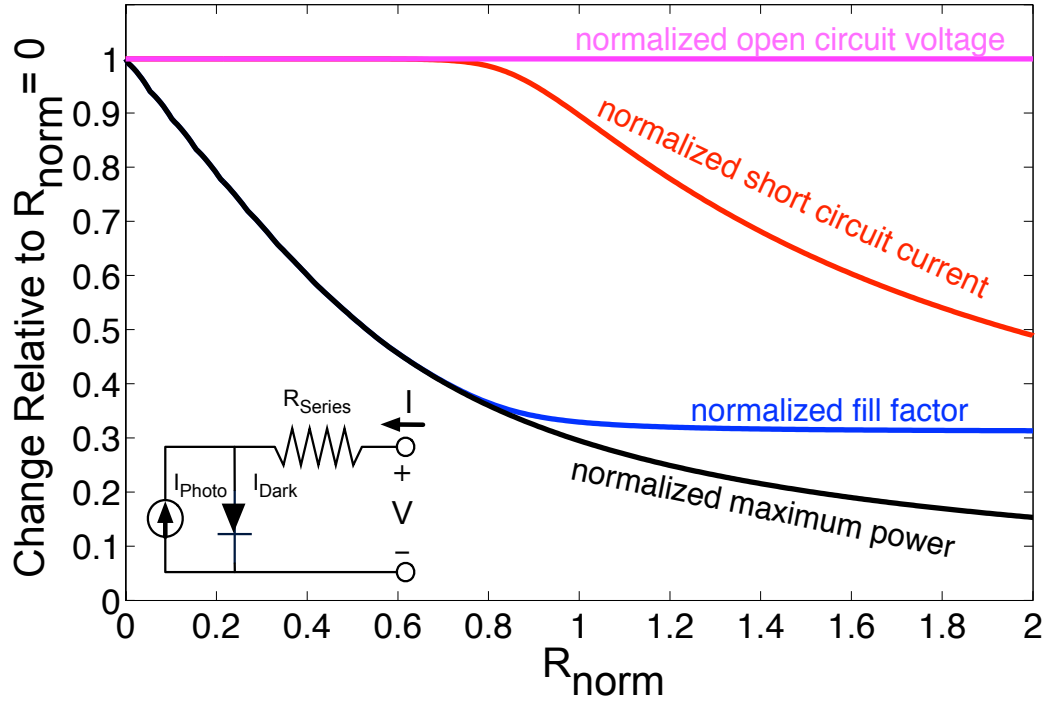


Figure 6.6: Relative change in solar cell parameters (V_{OC}, J_{SC}, FF, η) versus normalized series resistance.

Overall, it can be seen that AgNWs can be laser processed on top of a SOH solar cell to improve the conductivity of the network without adverse effects. The laser processing did not affect the open-circuit voltage of the devices, and therefore did not damage the blocking PEDOT/Si interface. However, sintering did achieve the desired effect of reducing sheet resistance of the AgNW networks and thereby increased the performance of the solar cells. Therefore, solution processed AgNW networks are promising as a complementary transparent conductor for use with PEDOT/Si and PST solar cells.

6.5.3 AgNW/PEDOT:PSS solar cells on textured silicon

Silver nanowire networks have also been of interest as a transparent conductor on top of textured PEDOT/Si devices [58]. As the optical modeling in Section 3.6.2 shows, the PEDOT:PSS absorption in textured/Si devices can be minimized by making the PEDOT:PSS layer thin. By employing a transparent conductor such as AgNW on top of the PEDOT:PSS layer, the distance that current must travel laterally in the PEDOT:PSS is greatly reduced (depending on the AgNW density). Therefore, the thickness of the PEDOT:PSS layers can be reduced to increase short-circuit current without sacrificing fill factor.

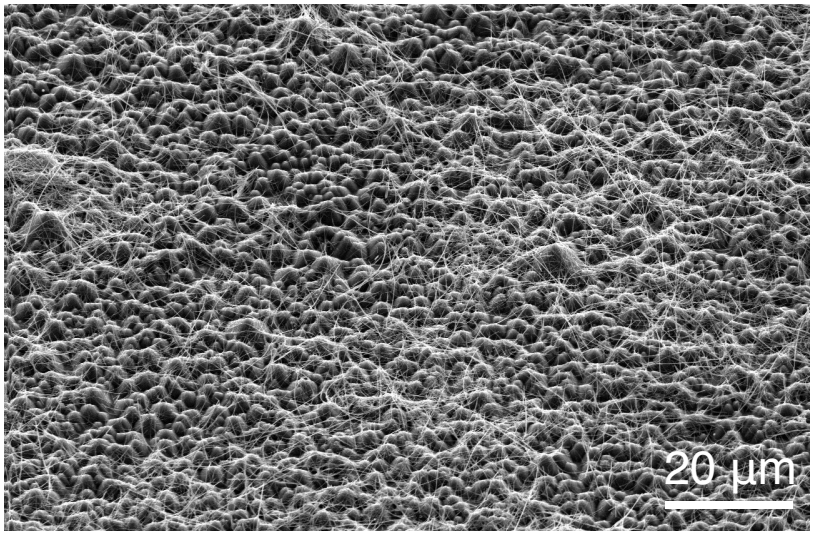
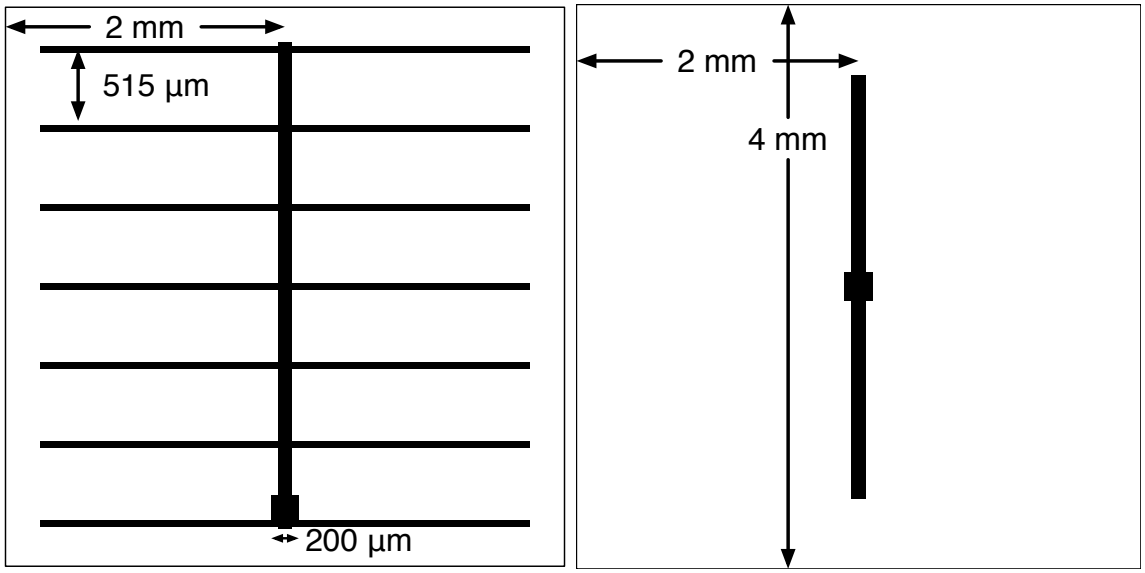


Figure 6.7: Scanning electron microscope image of randomly pyramidal textured Si coated with PEDOT:PSS and AgNW network.

Figure 6.9 shows the current-voltage characteristics of two PEDOT/Si solar cells made with textured silicon. One of the devices employs a typical finger and busbar pattern for the top metallization. The metal grid uses seven parallel $50-\mu m$ by $3.5-mm$ fingers spaced $515-\mu m$ apart, which are joined using a central $100-\mu m$ by $3.5-mm$ busbar which terminates in a $200-\mu m$ by $200-\mu m$ contact pad. The total metal grid results in a total coverage area of $9.7\,\%$, and is shown in Figure 6.8a.



(a) (b)

Figure 6.8: The (A) metal grid with 515 µm finger spacing compared to the (B) busbar used on the AgNW devices.

In contrast, the AgNW devices use a single 100 µm by 3 mm busbar with a central 200 µm by 200 µm contact pad for current collection. This results in a total coverage area of 2 %, and is shown in Figure 6.8b. The photocurrent collected by the PEDOT/Si solar cell with AgNWs must travel through the AgNW network on average ∼1 mm before being collected by the central busbar. The current in the device without AgNW travels on average ∼129 µm laterally through the PEDOT:PSS.

The solar cell parameters of the two devices is summarized in Table 6.3 The data show that the textured device with a conventional metal grid achieves a very good short-circuit current of 28.7 mA cm^{-2}. The device which makes use of a AgNW top electrode achieves an even higher J_{SC} of 29.9 mA cm^{-2}. On top of that, the AgNW solar cell also achieves a better fill factor. These data suggest that AgNW networks can clearly outperform a conventional grid approach and may be promising for furthering the efficiency of SOH solar cells.

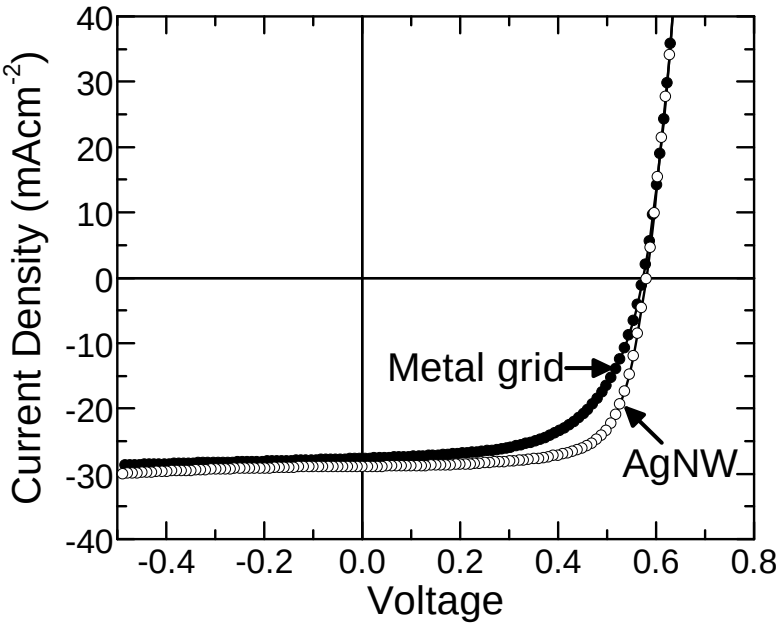


Figure 6.9: Illuminated AM1.5G current-voltage characteristics of PEDOT/Si solar cells on randomly pyramidal textured silicon comparing conventional 9.7 % metal grid and AgNW top electrode.

Table 6.3: Performance parameters for textured PEDOT/Si solar cells with grid versus AgNW contact

Top electrode	V_{OC}(mV)	J_{SC}(mA cm^{-2})	FF(%)	η(%)
9.7 % grid	561 ± 13	29.0 ± 0.5	56.0 ± 2.0	9.1 ± 0.4
AgNW	576 ± 4	29.5 ± 0.4	66.8 ± 1.6	11.3 ± 0.4

6.6 Conclusions

In conclusion, the deposition and laser-processing of percolating networks of AgNW films on PEDOT/SI solar cells has been successfully demonstrated. As discussed in Chapter 3, the non-ideal optical properties of PEDOT:PSS lead to reflection and absorption losses and limit the maximum attainable J_{SC} using PEDOT:PSS as a top electrode. The use of solution processed AgNW networks may offer an alternative transparent conductor to use in conjunction with PEDOT:PSS as a top electrode for SOH devices. Such AgNW films may benefit the overall efficiency and usefulness of

PEDOT/Si/TiO_2 devices as well. However, the absorption issues of PEDOT:PSS that have been discussed are not trivial, and solving them may require significant engineering. The solutions may require innovative changes to the device structure, surface treatments, thermal treatments, or even new materials development. Some possible avenues for improvements to the double heterojunction solar cell will be outlined in the following chapter.

Chapter 7

Conclusions and Future Work

7.1 Summary of Results

The key findings from the experimental results presented in Chapters 3, 4, 5 and 6 are summarized here. In Chapter 3, spectroscopic measurements showed that PEDOT:PSS had the necessary band alignments and work-function to form a hole-selective contact to silicon. The spectroscopic data suggested that the PEDOT/Si heterojunction could be used as a replacement for a diffused p^+-n junction in order to make an n-type silicon solar cell, and this was successfully demonstrated. The PEDOT/Si heterojunction was found to be similar to the p^+-n junction in that the dark current flow was dominated by minority carrier injection into the n-type silicon base. This was an important result, as it showed that further improvement of the device V_{OC} would require a back surface field to reduce the hole dark current. Additionally, the limitations of the PEDOT/Si solar cell were discussed. PEDOT is not an ideal transparent conductor or anti-reflection coating, and this leads to optical losses in the PEDOT/Si solar cell. These limitations motivate a search for a better low-temperature, hole-selective contact material for crystalline silicon.

In Chapter 4 we reviewed a new method for depositing TiO_2 with a maximum temperature of 100 °C, with a single precursor, and without any plasma enhancement. The properties of Si/TiO_2 heterojunctions formed using this low-temperature method were found to be suitable for a BSF to n-type silicon. The band alignments of the Si/TiO_2 heterojunction were shown to be suitable for blocking holes, and the TiO_2 was also shown to offer excellent surface passivation of crystalline silicon (surface recombination velocity as low as $20\,\mathrm{cm\,s^{-1}}$). These properties show that Si/TiO_2 heterojunctions hold great potential for use in crystalline silicon photovoltaic devices.

Chapter 5 presented the first time that TiO_2 was utilized as a selective contact in a crystalline silicon-based solar cell (either with a p-n junction or in a double heterostructure implementation). The addition of a TiO_2 BSF to the PEDOT/Si solar cell successfully reduced the dark current, raised the open-circuit voltage, raised the external quantum efficiency, and thereby improved the overall efficiency of the device. The dark current-voltage, V_{OC}, EQE, and charge storage measurements offered an estimation of the SRV at the Si/TiO_2 heterojunction in a fully fabricated device. The effects that TiO_2 thickness has on the PST solar cell were presented, along hypotheses of the underlying physical mechanisms and some supporting spectroscopic data. These mechanisms must be understood and addressed if the PST device is to be improved further.

Chapter 6 presented the performance of silver nanowire networks used as transparent conductors. The resistivity of these AgNW networks is lowered by laser post-processing, and laser-processed AgNWs are demonstrated as a top electrode on a PEDOT/Si device. This served as a route towards higher efficiency PEDOT/Si devices, as well demonstrating the versatility of laser-processed AgNW networks.

The demonstration of the PST solar cell is encouraging as it represents an alternative to the HIT cell. Since the HIT solar cell holds the record for power conversion efficiency of a silicon solar cell at 25.6 %, the performance ceiling for such silicon

heterojunction solar cells is very high. Low-temperature heterojunctions such as PEDOT/Si and Si/TiO_2 may even hold an advantage over amorphous silicon by not relying on plasma deposition processes, thereby potentially lowering manufacturing costs. However, in order to reach the same levels of performance as the HIT solar cell, significantly more work is needed.

7.2 Future work

To advance low-temperature silicon heterojunction solar cells will involve a variety of different innovations. The long-term solution for the PST solar cell will require improvements and innovations in three areas: interface passivation; device architecture; and development of alternative materials. Alternative methods of surface passivation can be incorporated to enhance the performance of both the PEDOT:PSS and TiO_2 interfaces. Section 7.2.1 discusses the possibility of using tunneling oxides for enhanced passivation at the PEDOT/Si and Si/TiO_2 interfaces. As the optical modeling in Sections 3.6.1 and 3.6.2 shows, using PEDOT:PSS as a top contact is not ideal. Section 7.2.2 presents alternative device architectures for the PST solar cell that offer higher performance. Finally, Section 7.2.3 discusses some other materials for use as selective contacts to crystalline silicon which may offer better performance than PEDOT:PSS or TiO_2.

7.2.1 Tunneling oxides

Section 3.6.3 discussed the use of native silicon oxide as a tunneling passivation layer situated between the PEDOT and silicon. While this has been shown to improve the V_{OC} of PEDOT/Si solar cells [95], the data presented in this work suggested that it is difficult to obtain a native oxide thin enough to maintain a good fill factor. Investigation of growth process parameters, such as time, temperature, and ambient

humidity, is likely worthwhile to controllably achieve a native oxide layer that is thin enough to facilitate tunneling.

There are a few other methods for obtaining tunneling oxides on silicon that have recently been demonstrated. One method, developed at the National Renewal Energy Laboratory, involves a conventional thermal oxidation followed by a dilute hydrofluoric acid etch to thin the oxide [160] to form passivated contacts on crystalline silicon. Such a process, while allowing for reproducible oxide properties and good surface passivation, still requires high-temperature processing. Another interesting method involves the use of HNO_3 to form an oxide [161]. In contrast to the previously mentioned thermal process, this method forms a tunnel oxide at temperatures as low as 20 °C. These methods for growing tunnel oxides should prove interesting for incorporation into a low-temperature heterojunction solar cell, and is a good avenue for future research.

7.2.2 Inverted Double-Heterojunction Solar Cells

One approach to mitigate the trade-offs among absorption, resistive and reflective losses of a PEDOT:PSS top contact is to use PEDOT:PSS as a back contact instead. This approach requires a high-quality top passivation at the top surface to ensure low recombination, since the built-in electric field produced by the PEDOT will be at the bottom surface. A PEDOT/Si rear junction solar cell has been demonstrated using a diffused n^+ junction as a front surface field [162]. This device employed a Si/SiO_x/PEDOT:PSS heterojunction at the rear of the solar cell combined with a diffused n^+ front-surface-field, which achieved a V_{OC} of 663 mV [162]. More recently a Si/PEDOT:PSS device with such diffused front surface fields was demonstrated with over 20 % PCE [163]. While moving the Si/PEDOT:PSS heterojunction to the rear of the solar cell can offer significant advantages in short-circuit current, ideally the top junction would be formed by a low-temperature process as well.

A more forward-thinking option is to use a low-temperature TiO_2 film to form the front surface field. TiO_2 is a much better choice for a top ARC than PEDOT:PSS, due to a higher refractive index and low optical absorption. Furthermore TiO_2 has already been shown to provide excellent surface passivation, which is critical for inverted devices. While the TiO_2 is not nearly as conductive as the PEDOT:PSS, it is also not needed to carry current laterally. As illustrated in Figure 7.1a, the structure of the inverted PST would require the photogenerated current to flow laterally in the silicon until reaching the metalized contact areas on the TiO_2. This approach is very similar to that of the passivated emitter and rear cell (PERC) [164] and passivated emitter rear locally diffused (PERL) solar cell [165]. One advantage of the inverted PST solar cell is that the TiO_2 may replace both the thermally diffused FSF (typically an n^+ diffusion) and the top passivation layer (typically thermally grown silicon dioxide or silicon nitride by PECVD). Even higher efficiencies could possibly come from an integrated-back contact approach [166]. In this structure, the top surface of the solar cell is coated only by a passivating ARC material (this could also be TiO_2). All electrical contacts to the cell are made on the rear of the device, which would have interwoven electron and hole selective contacts. This architecture would eliminate any short-circuit current losses due to shading from a top metal grid.

Optical Modeling

Titanium dioxide has exceptional optical characteristics for use as a top layer for an inverted PST solar cell. Due to its relatively high refractive index and very low optical absorption, TiO_2 functions well as an anti-reflective coating on silicon substrates [167]. Figure 7.3 shows the short-circuit current as a function of the thickness of a TiO_2 ARC on a planar substrates, as modeled by the OPAL2 simulation software [88–94]. The modeled J_{SC} values peak at $38\,\mathrm{mA\,cm^{-2}}$ for TiO_2 thicknesses around 60 nm on planar

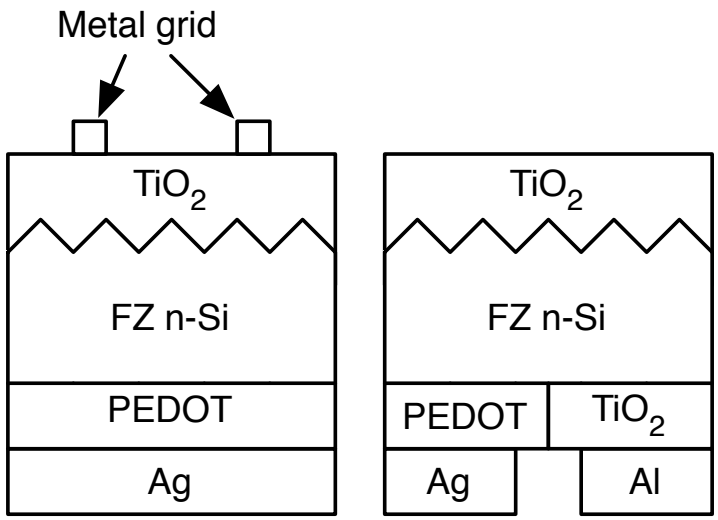


Figure 7.1: Proposed structures for (A) inverted and (B) all-back contact PEDOT/Si/TiO_2 solar cells with surface texturing.

substrates. This is much higher than the maximum attainable J_{SC} of 28 mA cm^{-2} using PEDOT:PSS as a top ARC on planar silicon, as shown in Chapter 3.

Figure 7.5 shows the modeling of a randomly pyramidal textured silicon substrate with TiO_2 as the top ARC. The optical losses due to reflection in the planar case are reduced, bringing the potential J_{SC} of the textured device up to 42.9 mA cm^{-2} for a TiO_2 thickness of about 60 nm. Therefore for a device architecture with no top metal shading losses, such as Figure 7.1b, the model predicts a J_{SC} that is very close to the highest values demonstrated for crystalline silicon (42.7 mA cm^{-2} [12]). It should be noted that for an architecture with top metal contacts is used (as in Figure 7.1a),the thickness used for an optimal ARC coating need not be the same thickness as the electrical contact underneath the top metal grid. As discussed in Chapter 5, thicker (>5 nm) TiO_2 layers at the anode contact may cause an open-circuit voltage loss. However this can be avoided by simply depositing the cathode metalization when the TiO_2 is at optimal thickness for cathode contact formation and depositing thicker TiO_2 layers afterwards for ARC purposes.

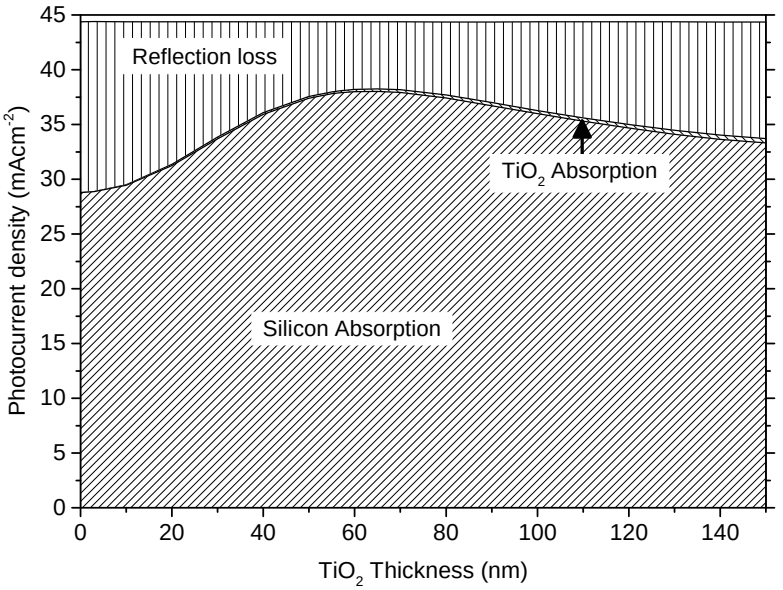


Figure 7.2

Figure 7.3: Optical modeling of TiO_2 as a top ARC on planar silicon substrate showing reflection loss, absorption in the TiO_2, and silicon absorption.

Surface Passivation for inverted devices

Due to the majority of incoming light being absorbed at the top surface of the silicon (as described in Chapter 5), surface passivation for the inverted PST solar cell is extremely important. In the standard PST structure, a high recombination velocity at the Si/TiO_2 interface reduces the hole-blocking effectiveness of the heterojunction. As a result, the improvement in V_{OC} expected from the TiO_2 layer is reduced substantially. For an inverted device structure, however, the SRV of the Si/TiO_2 interface not only affects the V_{OC} of the device, but can reduce the J_{SC}.

Figure 7.6 shows simulated J-V curves of an inverted PST solar cell with various values of SRV at the Si/TiO_2 interface. The simulation is performed for a 300 µm-thick substrate which is illuminated at normal incidence by a AM1.5G spectrum and all light is assumed to be absorbed in the substrate. As expected, with increasing SRV the open-circuit voltage decreases due to the hole-blocking layer functioning less effectively. The short-circuit current of the device is also observed to decrease sub-

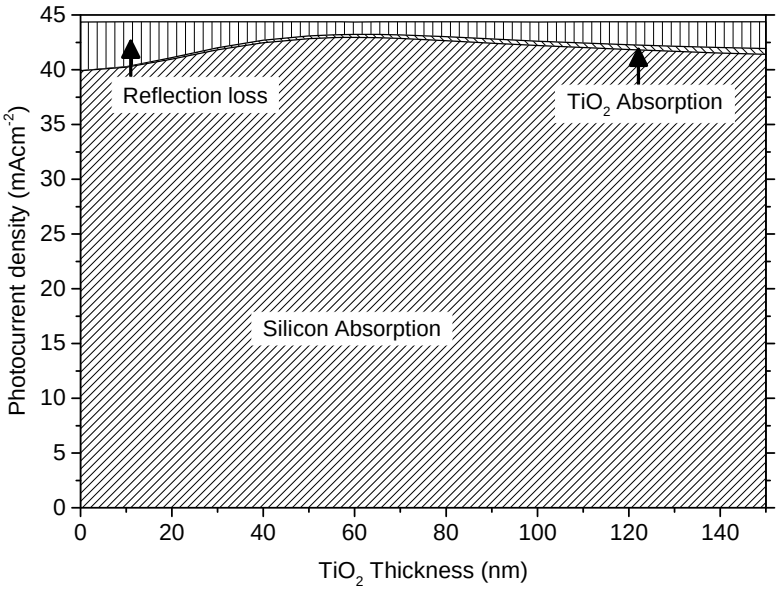


Figure 7.4

Figure 7.5: Optical modeling of TiO_2 as a top ARC on textured silicon substrate showing reflection loss, absorption in the TiO_2, and silicon absorption.

stantially with the increase of the SRV. Due to the large amount of carrier generation near the Si/TiO_2 interface of the inverted device, surface recombination here has a drastic effect on both the V_{OC} and J_{SC} of the devices. However, the modeling shows that an SRV of <50 cm/s will give near-optimal performance. Our lab has achieved SRV of 20 cm/s using TiO_2 on n-type silicon, and other labs have achieved SRV values as low as 2.8 cm/ sec [117].

In order to achieve the inverted DSH structures illustrated in Figures 7.1a and 7.1b, the passivating material must work on textured silicon surfaces. As the optical modeling of Figure 7.5 shows, the amount of light absorption in the silicon is much greater with a textured surface than with a planar silicon surface. Therefore the TiO_2 must also be able to passivate $< 111 >$ surfaces, which are the exposed crystal orientations which remain after the texturing process.

Figure 7.7 shows the minority carrier lifetime of an n-type float-zone silicon sample after 17 repeated TiO_2 deposition cycles with venting (expected thickness is $\sim$13 nm

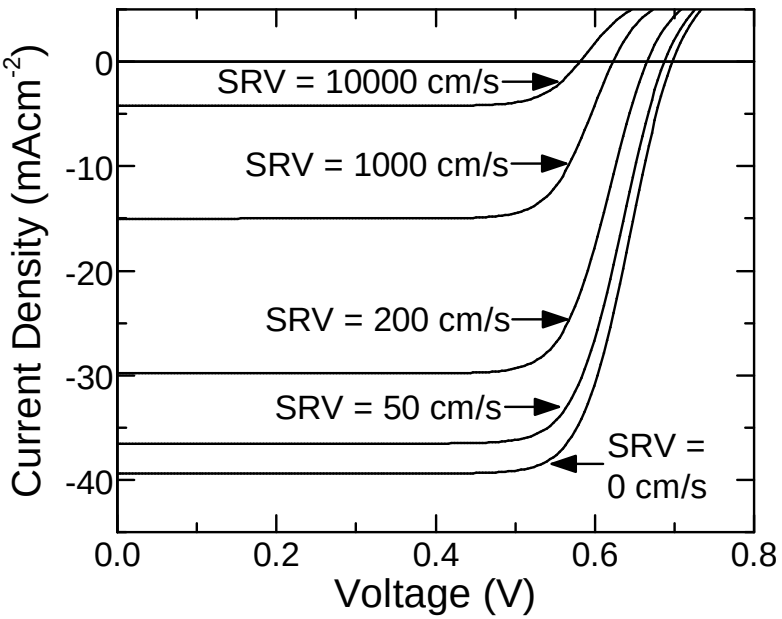


Figure 7.6: Simulated current-voltage characteristics of inverted PST solar cells under illumination, with various SRV values for the top Si/TiO_2 interface. Modeling performed in Sentaurus.

to 15 nm). This shows that for repeated depositions using the venting process, a textured Si/TiO_2 interface can achieve very good passivation of less than 50 cm/ sec. These results are very promising for the use of TiO_2 as a passivating ARC, as it shows that thicker TiO_2 layers can be deposited on textured $< 111 >$ silicon surfaces and maintain high-quality passivation. Further work is necessary to investigate the stability of the TiO_2 passivation of these textured silicon surfaces.

7.2.3 Alternative Materials for Silicon Heterojunctions

As discussed in Chapter 3, PEDOT:PSS has significant limitations as a hole-selective contact to silicon. This motivates the search for alternative materials which can form hole-selective heterojunctions to silicon which can offer improved performance as a transparent conductor, anti-reflection coating, or passivation layer.

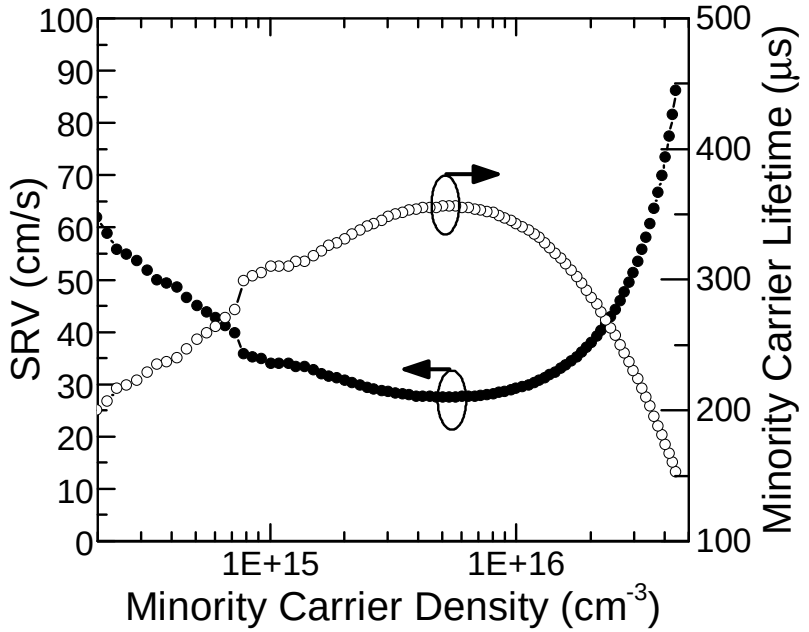


Figure 7.7: Surface recombination velocity (filled circles, left axis) and minority carrier lifetime (hollow circles, right axis) vs minority carrier density for a textured float zone silicon wafer with thick TiO_2 deposition.

To this end, some interest has been directed at finding metal oxides which can form hole-contacts to silicon. Nickel oxide may be suitable, due to the location of its valence and conduction band relative to those of silicon [52, 168, 169], however no such heterojunction has been demonstrated to date. MoO_3 has received significant interest as a high-work-function contact for silicon photovoltaics [170]. MoO_3 contacts with amorphous silicon passivation layers and heterojunction contacts (deposited by PECVD) have been demonstrated to achieve very high conversion efficiencies [171], most recently reaching 22.5 % [172]. While these results are promising, ideally such devices would not require PECVD to deposit the passivation layer. Recent work has demonstrated the transition metal oxides MoO_3, WO_3, and V_2O_5 as hole contacts directly on n-type silicon [173]. In summary, there are several promising metal oxide candidates for replacing PEDOT:PSS as a hole selective contact to silicon. Further

research regarding these materials on crystalline silicon promises to be an exciting avenue for future work in this field.

Appendix A

Processing Notes

A.1 Top Metal Grid Designs

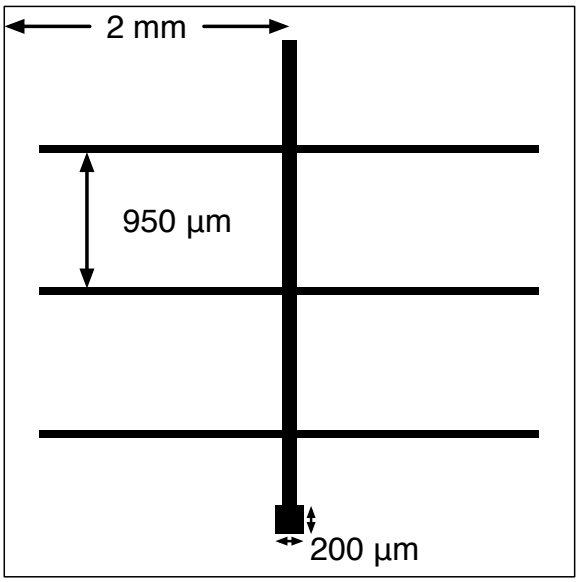


Figure A.1: 5.4 % area coverage design for top metal grid.

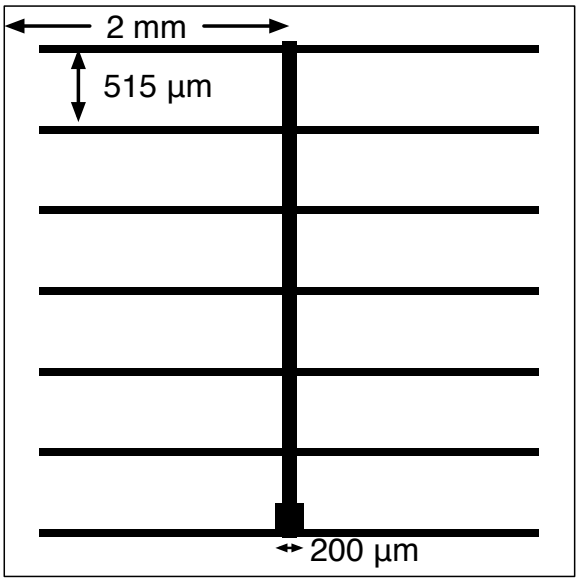


Figure A.2: 9.7 % area coverage design for top metal grid.

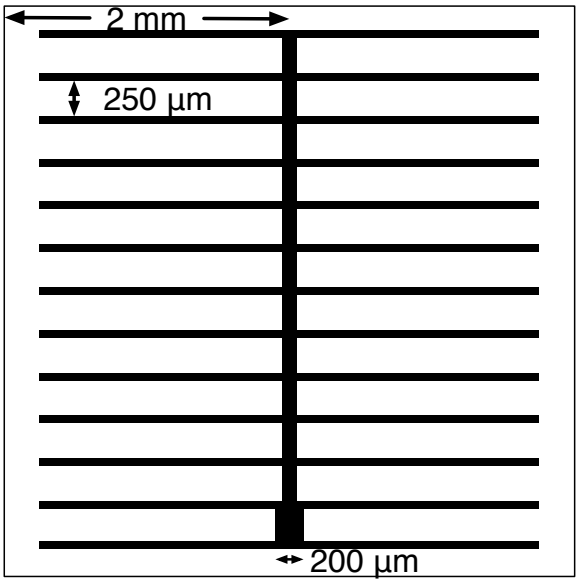


Figure A.3: 16.2 % area coverage design for top metal grid.

A.2 Parasitic Back Contacts

In conventional silicon solar cells, ohmic contacts are formed by heavily doping the contact regions by diffusion. However, part of the motivation for low-temperature heterojunction solar cells is to eliminate such high-temperature processing steps. There-

fore, in fabricating Si/PEDOT:PSS solar cells, care must be taken in order to avoid the formation of parasitic Schottky barriers at metal-silicon contact regions. The parasitic barrier forms due to Fermi-level pinning at the silicon-cathode interface (despite the choice of a nominally low work-function metal such as aluminum). The effect of a parasitic Schottky barrier at the rear interface of a solar cell can be described by a modified Ebers-Moll model as described by Green et. al and others [174–176]. An circuit diagram of the model (adapted for an n-type base region) is shown in Figure A.4.

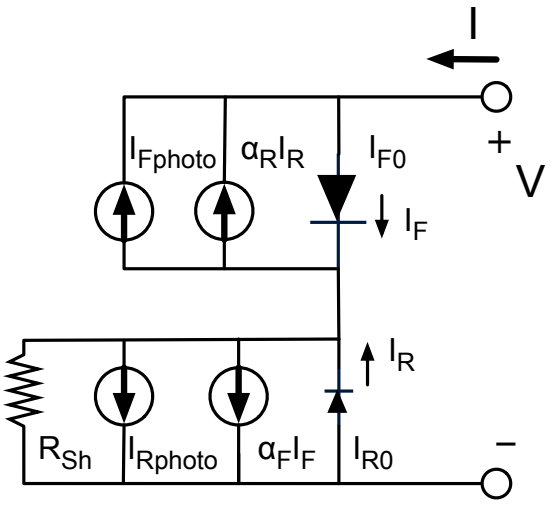


Figure A.4: Modified Ebers-Moll equivalent circuit for a SOH solar cell [174].

In Figure A.4, there are two diodes which represent the front (Si/PEDOT:PSS) and rear (parasitic Schottky) junctions formed in the device. I_{F0} and I_{R0} represent the saturation current of the forward and rear junctions, respectively, with the other junction shorted. α_F represents the injection efficiency of the front junction, and I_F is the current flowing through the front junction. Therefore, the current source at the rear junction $\alpha_F I_F$ represents the current due to injected holes that reach the rear junction (and vice versa for $\alpha_R I_R$). This represents the current that will flow as a result of injected holes reaching the rear junction. Also shown are current sources

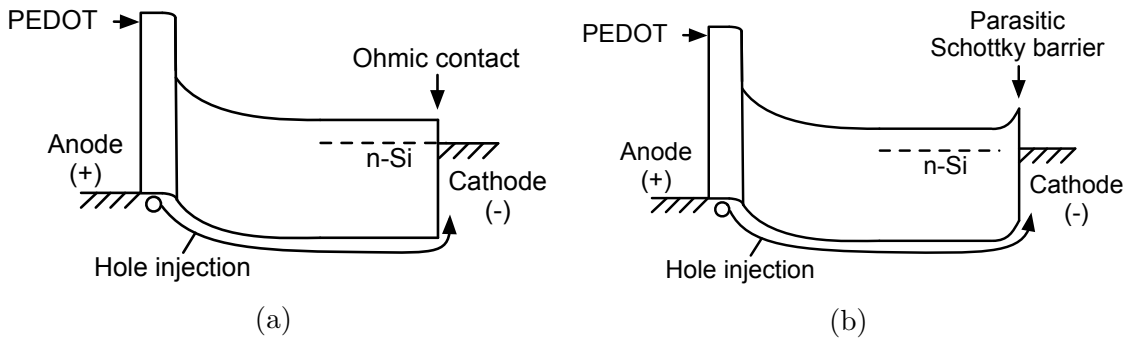


Figure A.5: Band diagrams of Si/PEDOT:PSS devices with (A) ohmic contact at the cathode and (B) parasitic Schottky back contact in forward bias in the dark.

which represent the photo-generated current collected by each junction. Finally, R_{SH} represents the shunt resistance associated with the rear junction (The shunt resistance for the front junction is assumed to be sufficiently high to neglect).

First, the effect of the rear junction in the dark is considered, in which the two current sources representing photo-current in Figure A.4 are off. If the injection efficiency of the front junction α_F is high (as is the case high quality silicon solar cells), the current from the front junction I_F flows through the current source $\alpha_F I_F$, and no voltage drop occurs across the rear junction. The physical interpretation of the high injection efficiency means that the majority of the current from the front junction is from injected holes that reach the back interface and subsequently recombine. Whether there is an ohmic or parasitic Schottky contact does not matter, as in either case the holes are able to recombine at the cathode (Figure A.5a and Figure A.5b).

Under illumination, however, the parasitic barrier can have a effect on the V_{OC} of the device. The open-circuit voltage generated across the device represented in Figure A.5b is given by Equation A.1.

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{I_{F,photo}}{I_{F,0}} + 1\right) - (\alpha_F I_{F,photo} + I_{R,photo}) R_{SH} \tag{A.1}$$

The first term is the expected open-circuit voltage and the second represents the V_{OC} loss due to the rear junction. Clearly, if the shunt resistance is reduced to zero (as

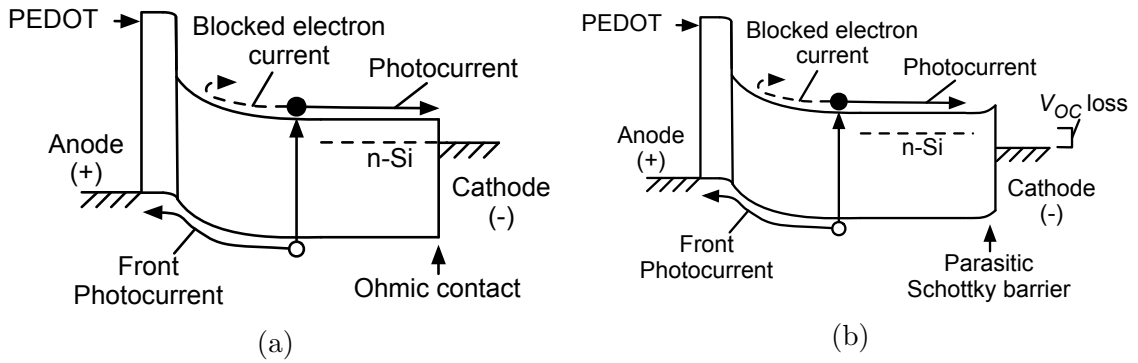


Figure A.6: Band diagrams of Si/PEDOT:PSS devices with (A) ohmic contact at the cathode and (B) parasitic Schottky back contact in forward bias and under illumination, showing V_{OC} loss.

in a good ohmic contact), then the loss of V_{OC} will reduced to zero as well. However if R_{SH} is non-negligible, then the loss of V_{OC} will scale with the photocurrent. The V_{OC} loss depends on the front junction photocurrent $I_{F,photo}$ and injection efficiency α_F because as the front junction collects a photogenerated hole, the n-type substrate becomes negatively charged. Similarly, the rear Schottky junction will collect some amount of photogenerated holes which causes the substrate to become negatively charged. However, electrons are prevented from leaving via the front of the device due to the electron blocker (or the p^+-n junction of a conventional device), and therefore must leave via the rear junction. If the rear contact is ohmic, the electrons are free to reach the cathode, but if a Schottky barrier exists here, then it must be forward biased in order to allow the electrons to escape. This results in a voltage drop between the n-Si substrate and the cathode, and a lower V_{OC} as measured measured between the anode and cathode of the device. This is illustrated in Figure A.6a for a device with an ohmic contact and Figure A.6b for a device with a parasitic Schottky contact.

The effect of the parasitic backside contact was observed primarily for double-side polished n-type substrates. Evaporating the aluminum cathode directly onto a polished n-type silicon surface resulted in a parasitic back contact. This effect was

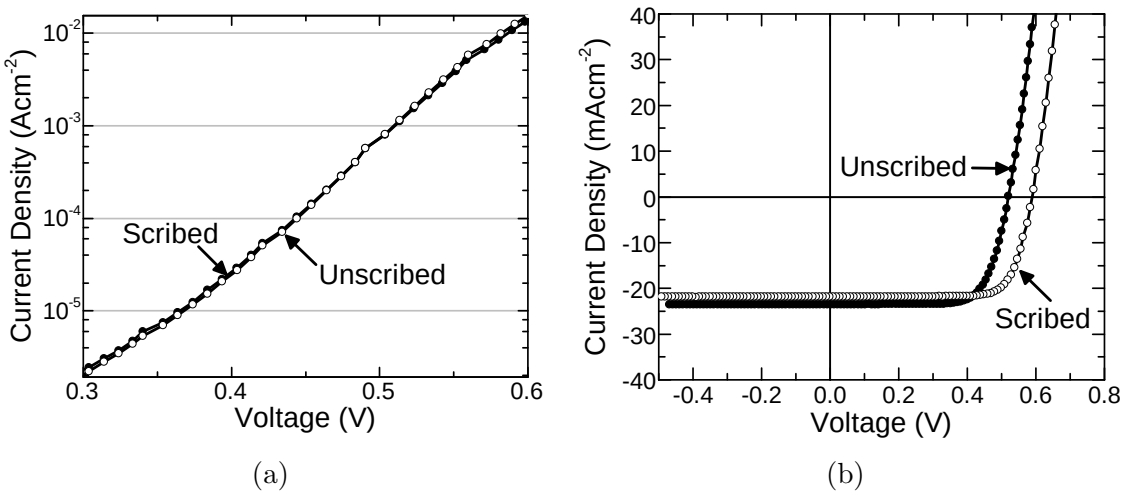


Figure A.7: Current-density vs voltage characteristics of PEDOT/Si devices with (filled circles) and without (hollow circles) backside scribing. (A) A semi-log plot in the dark and (B) a linear plot under AM1.5G illumination.

observed to be mitigated by roughening the back (cathode side) surface of the silicon by diamond scribing prior to aluminum evaporation.

Figure A.7a shows the zoomed in view of the dark current of two Si/PEDOT:PSS devices, with and without scribing of the silicon before aluminum cathode evaporation. There is no distinguishable difference between the dark current J-V characteristics of the two devices. This is consistent with the physical picture presented in Figures A.5a and A.5b which show that the parasitic Schottky barrier will not have an effect on the dark current compared to a device with an ohmic contact.

Figure A.7b shows the current-voltage characteristics of the same two devices under illumination. The device without backside scribing exhibits a low V_{OC} of , in contrast to the achieved by the scribed device. The loss of V_{OC} in the unscribed device is attributed to formation of a parasitic Schottky barrier as discussed. Introducing damage intentionally via scribing of the backside helps produce shunt paths [177] at the aluminum silicon interface, which allow electron current to bypass the Schottky barrier.

Appendix B

List of Publications

B.1 Journal publications

1. "A 12 % efficient silicon/PEDOT: PSS heterojunction solar cell fabricated at 100 °C." Ken A. Nagamatsu, Sushobhan Avasthi, Janam Jhaveri, and James C. Sturm, Photovoltaics, IEEE Journal of 4.1 (2014): 260-264.

2. "Titanium dioxide/silicon hole-blocking selective contact to enable double-heterojunction crystalline silicon-based solar cell." Ken A. Nagamatsu, Sushobhan Avasthi, Girija Sahasrabudhe, Gabriel Man, Janam Jhaveri, Alexander H. Berg, Jeffrey Schwartz, Antoine Kahn, Sigurd Wagner, James C. Sturm, Applied Physics Letters 106.12 (2015): 123906.

3. "Improved efficiency of hybrid organic photovoltaics by pulsed laser sintering of silver nanowire network transparent electrode." Joshua A. Spechler, Ken A. Nagamatsu, James C. Sturm, Craig B. Arnold, ACS applied materials & interfaces (2015).

B.2 Conference Proceedings, Presentations, and Posters

1. "Current Mechanisms in Silicon-organic Heterojunction Solar Cells with Transfer Printed Metalization" Ken A. Nagamatsu, Joshua Spechler, Sushobhan Avasthi, Craig Arnold, James C. Sturm, presented at 2012 Materials Research Society Fall Meeting November 25-30, 2012 Boston, MA

2. "High-Conductivity, High-Transparency PEDOT Films by Direct Application of Silver Nanowires on 10.6 % Low Temperature Hybrid Photovoltaic Device." Ken A. Nagamatsu, Joshua Spechler, Sushobhan Avasthi, Craig Arnold, and James C. Sturm, poster presented at 2013 Materials Research Society Spring Meeting April 1-5, (2013) San Francisco, CA

3. "Integrated laser processed silver nanowire transparent electrodes with organic electronic devices." Joshua Spechler, Ken A. Nagamatsu, James C. Sturm, and Craig B. Arnold, CLEO: Science and Innovations. Optical Society of America, (2013).

4. "Hole-blocking crystalline-silicon/titanium-oxide heterojunction with very low interface recombination velocity." Janam Jhaveri, Sushobhan Avasthi, Gabriel Man, William E. McClain, Ken A. Nagamatsu, Antoine Kahn, Jeffrey Schwartz, and James C. Sturm. In Photovoltaic Specialists Conference (PVSC), 2013 IEEE 39th, pp. 3292-3296. IEEE, (2013).

5. "Wide bandgap HBT on crystalline silicon using electron-blocking PEDOT: PSS emitter." Janam Jhaveri, Sushobhan Avasthi, Ken A. Nagamatsu, and James C. Sturm, In Device Research Conference (DRC), 2013 71st Annual, pp. 77-78. IEEE, (2013).

6. "Wide Bandgap Heterojunctions on Crystalline Silicon." James C. Sturm, Sushobhan Avasthi, Ken A. Nagamatsu, Janam Jhaveri, William E. McClain, Gabriel Man, Antoine Kahn, Jeffrey Schwartz, and Sigurd Wagner ECS Transactions 58, no. 9 (2013): 97-105. Invited

7. "Hole-Blocking Metal-Oxide/Crystalline-Silicon Heterojunctions with Recombination Velocity of <100 cm/s." Sushobhan Avasthi, William E. McClain, Yasmin Afsar, Gabriel Man, Janam Jhaveri, Ken A. Nagamatsu, Antoine Kahn, Jeffrey Schwartz, Sigurd Wagner, and James C. Sturm, presented at 2014 Materials Research Society Spring Meeting April 21-25, 2014 San Francisco, CA. Invited

8. "Growth Mechanism and Carrier Transport in Hole-Blocking TiO2/Silicon Heterojunctions" Sushobhan Avasthi, William E. McClain, Gabriel Man, Janam Jhaveri, Ken A. Nagamatsu, Antoine Kahn, Jeffrey Schwartz, and James C. Sturm, poster presented at 2013 Materials Research Society Spring Meeting April 21-25, 2013 San Francisco, CA

9. "Silicon/Organic Heterojunction Photovoltaic Cell with 12.7 % Efficiency by Use of Spray-Coated Nanowire Transparent Conductor" Ken A. Nagamatsu, Joshua Spechler, Sushobhan Avasthi, Craig Arnold, James C. Sturm, presented at 2013 Materials Research Society Spring Meeting April 21-25, 2013 San Francisco, CA

10. "Stable low-recombination n-Si/TiO 2 hole-blocking interface and its effect on silicon heterojunction photovoltaics." Janam Jhaveri, Sushobhan Avasthi, Ken A. Nagamatsu, and James C. Sturm, In Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th, pp. 1525-1528. IEEE, (2014).

11. "Double-heterojunction crystalline silicon solar cell fabricated at 250 °C with 12.9 % efficiency." Sushobhan Avasthi, Ken A. Nagamatsu, Janam Jhaveri, William E. McClain, Gabriel Man, Antoine Kahn, Jeffrey Schwartz, Sigurd Wagner, and James C. Sturm, In Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th, pp. 0949-0952. IEEE, (2014).

12. "Effect of Annealing on Stability of Low Interface Recombination Velocity at TiO2/p-Silicon Interface." Janam Jhaveri, Sushobhan Avasthi, Gabriel Man, Ken A. Nagamatsu, William E. McClain, Jeffrey Schwartz, Antoine Kahn, and James C. Sturm, presented at 2013 Materials Research Society Spring Meeting April 21-25, 2014 San Francisco, CA

13. "Double-heterojunction crystalline silicon solar cell with electron-selective TiO_2 cathode contact fabricated at 100C with open-circuit voltage of 640 mV."Janam Jhaveri, Ken A. Nagamatsu, Alexander H. Berg, Gabriel Man, Girija Sahasrabudhe, Sigurd Wagner, Jeffrey Schwartz, Antoine Kahn, and James C. Sturm, In Photovoltaic Specialist Conference (PVSC), 2015 IEEE 42nd IEEE, (2015).

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