Crystalline Silicon Photovoltaics via Low-Temperature TiO_2/Si and PEDOT/Si Heterojunctions

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Abstract

The most important goals in developing solar cell technology are to achieve high power conversion efficiencies and lower costs of manufacturing. Solar cells based on crystalline silicon currently dominate the market because they can achieve high efficiency. However, conventional p-n junction solar cells require high-temperature diffusions of dopants, and conventional heterojunction cells based on amorphous silicon require plasma-enhanced deposition, both of which can add manufacturing costs.

This dissertation investigates an alternative approach, which is to form crystalline-silicon-based solar cells using heterojunctions with materials that are easily deposited at low temperatures and without plasma enhancement, such as organic semiconductors and metal oxides. We demonstrate a heterojunction between the organic polymer, poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT), and crystalline silicon, which acts as a hole-selective contact and an alternative to a diffused p-n junction. We also present the use of a heterojunction between titanium dioxide and crystalline silicon as a passivating electron-selective contact. The Si/TiO_2 heterojunction is demonstrated for the first time as a back-surface field in a crystalline silicon solar cell, and is incorporated into a PEDOT/Si device. The resulting PEDOT/Si/TiO_2 solar cell represents an alternative to conventional silicon solar cells that rely on thermally-diffused junctions or plasma-deposited heterojunctions. Finally, we investigate the merits of using conductive networks of silver nanowires to enhance the photovoltaic performance of PEDOT/Si solar cells. The investigation of these materials and devices contributes to the growing body of work regarding crystalline silicon solar cells made with selective contacts.

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Chapter 1

Introduction

This dissertation explores an emerging approach to solar cell technology which is to form heterojunction solar cells at temperatures of ∼200 °C or less on crystalline silicon. The goal is to lower the cost and raise the efficiency of crystalline silicon-based solar cells, which is the dominant technology used in photovoltaics today. Section 1.1 describes the motivation for developing solar cell technologies. Section 1.2 reviews the classic p-n junction solar cell. Section 1.3 describes the state-of-the art silicon p-n junction solar cell, and presents some limitations of this approach. Finally, Section 1.4 presents a brief outline of the rest of the dissertation.

1.1 Motivation

> *"Warming of the climate system is unequivocal, and since the 1950s, many of the observed changes are unprecedented over decades to millennia. The atmosphere and ocean have warmed, the amounts of snow and ice have diminished, and sea level has risen."*

"Anthropogenic greenhouse gas emissions... are extremely likely to have been the dominant cause of the observed warming since the mid-20th century"

-Intergovernmental Panel on Climate Change Fifth Assessment Report

The above quote, from the Summary for Policymakers of the Synthesis Report of the fifth assessment report of the IPCC [1], is a powerful piece of language that summarizes in unambiguous fashion the overwhelming scientific consensus that climate change is real and observable via the effects on several elements of the global climate system. The report also states that the main driver of climate change is anthropogenic greenhouse gas emissions, with the largest contributor to warming being the increase in atmospheric carbon dioxide since the late 18^{th} century. The summary essentially makes three key points: Climate warming is happening; it is being driven by greenhouse gases emission; and it is *"extremely likely"* that humans are the cause.

1.1.1 Global Energy Demands

Global population is predicted to continue to grow well into the 21st century. In 2015, the world population was estimated at 7.3 billion people [2], as shown in Figure 1.1. Also shown are three projections of world population through the end of the century (based on different fertility rates and life expectancy). Even by the conservative estimates provided, the world population is expected to surpass 8 billion by 2030. As global population continues to grow, so will global energy demand.

Not only will global energy demand increase along with global population, but as the economies of the world continue to develop, their per capita energy consumption is bound to increase as well. In David MacKay's book, *Sustainable Energy: Without the Hot air* (an excellent resource provided free online [3]), he illustrates this by plotting per capita power consumption versus Gross Domestic Product (GDP), as

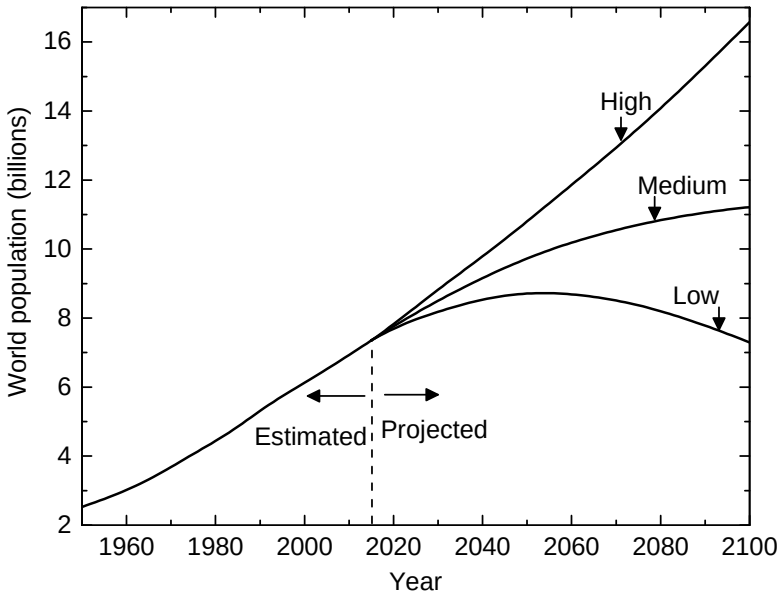


Figure 1.1: World population estimate from 1950 to 2015 in billions of people. Also shown are projections of population growth based on 'High', 'Medium', and 'Low' variant models for fertility [2].

shown in Figure 1.2. We can see that there is a positive correlation between power consumption and GDP per capita, and therefore as economies grow they will demand more energy. However, if the increase in energy demand is met with fossil-fuel sources such as coal and natural gas, then the development of any country's economy will stand in stark opposition to the pressing need to curb greenhouse gas emissions.

1.1.2 Solar Energy Resources

In this context, the need for sources of renewable and so-called 'clean' energy sources becomes very clear. The technical potential of a renewable energy system is defined as the achievable energy generation of a particular technology, given system performance, topographic limitations, environmental, and land-use constraints. While hydroelectric, wind, geothermal, and ocean energy sources represent promising energy solutions, their technical potential is limited due to these various constraints. Solar energy, however, offers a very large amount of technical potential of over 1000 EJ [1]. To put this

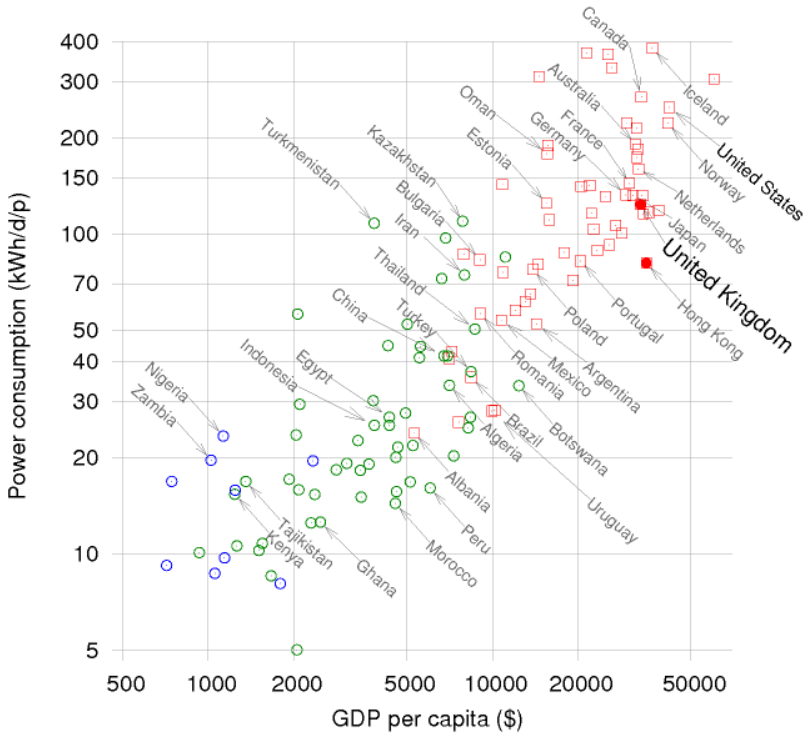


Figure 1.2: Power consumption per capita versus Gross Domestic Product (GDP) per capita for in US Dollars. Squares represent countries with 'high human development' and circles those with 'medium' or 'low' ratings according to the 2007 UNDP Human Development Report. Reproduced with permission [3]

quantity in perspective, the 2010 global primary energy supply was 510 EJ [1]. With the energy from the sun being so plentiful, the challenge then lies on scientists and engineers to harness this energy using efficient and cost-effective solar cells.

1.2 Solar Cell Operation

A solar cell is defined as a device that converts energy in the form of light into usable electricity. This happens via the photovoltaic effect, in which photons absorbed in a material creates a voltage or current. A solar cell harnesses the current that is generated into electrical power that can be delivered to a load. The amount of power that a solar cell can provide is expressed as a percentage of the total amount of power from the illumination source, and is referred to as the power conversion efficiency

(PCE or η). In this section, the physics behind the operation of a solar cell will be discussed in the context of the silicon p-n junction.

1.2.1 Ideal P-N Junction Solar Cell

The absorption of a photon in a semiconductor like silicon results in the excitation of an electron from the valence band, E_V, up to the conduction band, E_C. The excitation of the electron is a conversion of the photon's energy into potential energy of the electron. This is accompanied by the creation of an empty energy state in the valence band, and this missing electron is known as a hole. Because electrons and holes are charged particles, there is a coulombic attraction between them; a bound electron-hole pair is an exciton. In inorganic semi-conductors like silicon, the binding energy of the exciton is typically quite low and is easily overcome from thermal energy at room temperature.

Electrons in the conduction band and holes in the valence band that are not part of a bound pair are considered 'free' charge carriers, because the electron/hole sees many available states to move to in the conduction/valence band and can therefore move freely through the semiconductor crystal lattice. The photogenerated carriers may be lost to recombination, a process in which an electron falls from the conduction band (losing its potential energy) into a hole (an empty state in the valence band). Alternatively, free charge carriers can be collected by an electric field, which is commonly provided by a p-n junction.

The p-n junction is formed when a region of n-type semiconductor material is joined with a region of p-type semiconductor. A semiconductor becomes either n-type or p-type as a result of doping, in which a dopant atom becomes ionized and either donates or accepts an electron from the semiconductor lattice. A semiconductor is considered n-type if the majority of free carriers in the material are electrons, and p-type if the majority of free carriers are holes (undoped material, with equal numbers

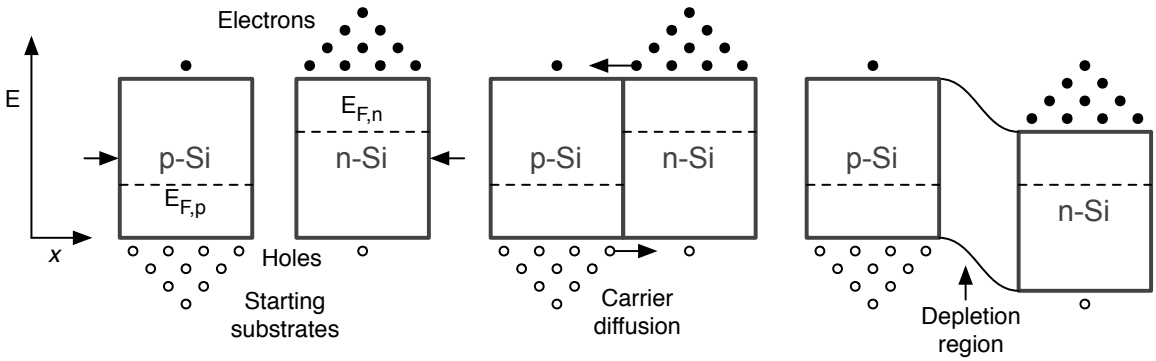


Figure 1.3: Formation of p-n junction showing starting p and n-type semiconductors with thermal carrier distribution, diffusion of free carriers, and formation of depletion region.

of electrons and holes, is considered intrinsic). Silicon, as a group IV element, can be doped n-type by group V elements such as phosphorus and arsenic, which have one more valence electron. When these dopants replace a silicon atom in the crystal lattice they are easily ionized by thermal energy, and the extra electron is donated to the lattice (phosphorus and arsenic are thus referred to as donor impurities). Boron acts in a reverse fashion; as a group III element it has one less valence electron than silicon and therefore acts as an acceptor impurity, creating holes in the semiconductor.

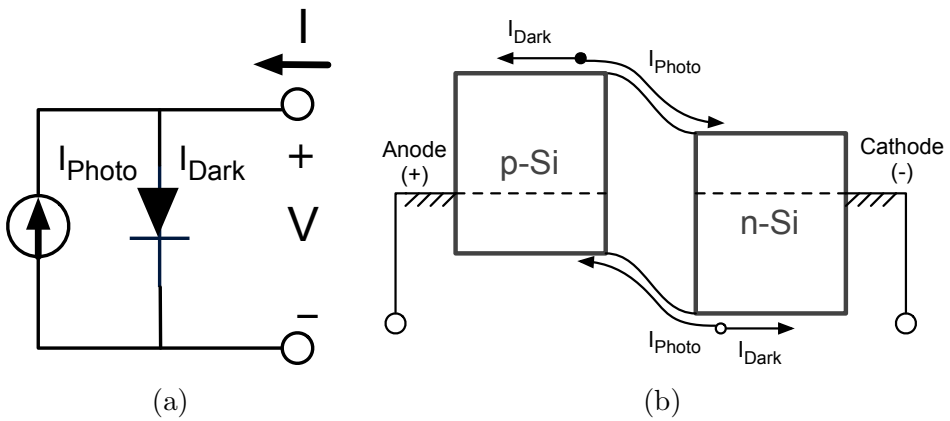
When a p-type and n-type semiconductor are joined together, a charge transfer occurs due to the difference in free electron density (diffusion current), as illustrated in Figure 1.3. Free electrons move from the n-type material to the p-type material (and holes flow from the p-side to the n-side), leaving behind the immobile, ionized dopant atoms. A space-charge, or depletion, region is formed, so-called due to the depleted number of free carriers in the region. The depletion region contains positively charged ionized donors on the n-type side and negatively charged ionized acceptors on the p-type side. An electric field is formed as a result, pointing from n-side to the p-side. Electrons, being negatively charged, move opposite the direction of an electric field (drift current), and thus the diffusion of electrons is halted by the energetic barrier provided by the electric field in the depletion region.

By making contacts to the n-type and p-type regions and applying a voltage, rectifying, or diode-like, behavior is observed from a p-n junction. Applying a positive bias to the p-type region (with respect to the n-side) reduces the electric field barrier in the depletion region, allowing current to flow due to the diffusion of electrons from the n-type region to the p-type region, where they are considered minority carriers (and likewise for holes in the opposite direction). Conversely, applying a negative bias to the anode of a p-n junction increases the electric field barrier, and limited current is observed to flow. The equation for current-density in an ideal diode is given by Equation 1.1, in which V is the applied voltage, n is the ideality factor, T is temperature, q is elementary charge, k is the Boltzmann constant, and I_0 is the leakage or saturation current.

$$I_{diode} = I_0 \left(\exp\left(\frac{qV}{nkT} \right) - 1 \right) \tag{1.1}$$

For semiconductors with a low defect density, relatively few carriers will recombine within the space-charge region, and therefore recombination in the neutral regions of the diode dominates. If the number of minority carriers is less than the equilibrium majority carrier concentration in the neutral region of a device, the device is considered to be in low-level injection, and $n = 1$. If the minority carriers generated in a semiconductor are equal to or greater than the equilibrium majority carrier concentration (which may be the case under solar illumination, or under high forward bias), then the device is considered to be in high-level injection and $n = 2$.

The equivalent circuit model of an ideal solar cell is represented by a diode in parallel with a current source, as shown in Figure 1.4a. The ideal current source represents the photocurrent (I_{photo}) created when the solar cell is illuminated, while the ideal diode represents the so-called 'dark current' flowing through the p-n junction. The band diagram in Figure 1.4b shows the direction of dark current flow, as well as



(a) (b)

Figure 1.4: (A) Equivalent circuit model and (B) Band diagram for an ideal solar cell.

the collection of photocurrent by the electric field in the p-n junction. The ideal solar cell equation can then be written as shown in Equation 1.2.

$$I(V) = I_0 \left(\exp\left(\frac{qV}{nkT} \right) - 1 \right) - I_{photo} \tag{1.2}$$

If the electrodes of the solar cell are left unconnected (such that no current flows out of the device), then a voltage build-up occurs; this is known as the open-circuit voltage, or V_{OC}. Setting $I = 0$ in Equation 1.2 and rearranging to find the voltage across the device provides an expression for the open-circuit voltage, as shown by Equation 1.3.

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{I_{photo}}{I_0} + 1 \right) \tag{1.3}$$

Similarly, the current that flows when the electrodes of the solar cell are shorted together is known as the short-circuit current, I_{SC}. Shorting the solar cell ensures that there is no voltage across the device ($V = 0$), so Equation 1.2 reduces to show that the short-circuit current is equal to the photocurrent in the ideal case, as shown by Equation 1.4.

$$I(0) = I_{SC} = I_{photo} \tag{1.4}$$

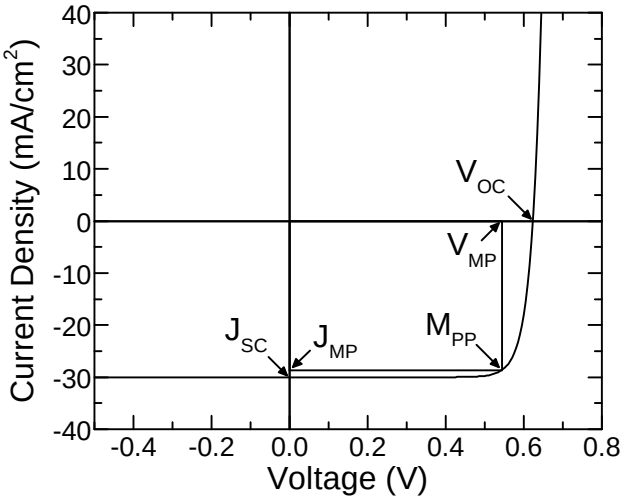


Figure 1.5: Plot of current-density versus voltage for an example solar cell. Performance parameters V_{OC} and J_{SC} are indicated, as well as operating points J_{MP}, V_{MP}, and the maximum power point M_{PP}.

The short-circuit current and open-circuit voltage represent two important parameters of the solar cell that must be maximized in order to maximize PCE. However, no useful power is extracted at either of these operating points. The power dissipated within or extracted from a solar cell is given by the product of the voltage and current, as given by Equation 1.5.

$$P(V) = V \times \left[I_0 \left(\exp\left(\frac{qV}{nkT} \right) - 1 \right) - I_{photo} \right] \tag{1.5}$$

It is useful to indicate these parameters on a plot of current-density versus voltage; an example J-V characteristic of a solar cell under illumination is shown in Figure 1.5. The V_{OC} and J_{SC} points are identified as the intersection points with the x and y axes, respectively. In quadrant IV of the plot, the voltage is positive yet the current flowing through the device is negative. According to Equation 1.5, the power in the device is therefore also negative, indicating that power is being produced, rather than dissipated in the device. The point at which the most amount of power is generated is referred to as the maximum power point (MPP). This is where the solar cell should

be operated, and the current (J_{MP}) and voltage (V_{MP}) at this bias point are also indicated in Figure 1.5.

Another important solar cell parameter is the fill-factor (FF), which relates the MPP to the V_{OC} and J_{SC} and is defined in Equation 1.6.

$$FF = \frac{V_{MP}J_{MP}}{V_{OC}J_{SC}} \tag{1.6}$$

The location of the V_{MP}, J_{MP}, and MPP points (along with the origin) outline a rectangle whose area represents the useful power extracted from the solar cell. A similar rectangle can be drawn from the V_{OC} and J_{SC} points, and the fill factor can be visualized as the ratio of the inner to the outer rectangle.

The overall efficiency of a solar cell depends on these three parameters and is defined by Equation 1.7.

$$\eta = \frac{V_{OC}J_{SC}FF}{P_{in}} \tag{1.7}$$

Here P_{in} is the total incident power provided by the illumination source. Terrestrial solar cell efficiencies are typically reported under illumination from the AM1.5G spectrum, which has an integrated power density of $1000\,\mathrm{W/m^2}$ and is shown in Figure 1.6. The AM1.5G spectrum represents the spectral irradiance that reaches the earth's surface at a solar zenith angle of 48.2°. The spectrum is intended to accurately represent the spectral irradiance after atmospheric effects like absorption and scattering that occur due to water vapor and other elements.

1.2.2 Open-Circuit Voltage

As Equation 1.3 shows, the open-circuit voltage of a solar cell depends on two main parameters: the amount of photogenerated current, and the dark saturation current J_0. Increasing the photogenerated current ties directly into the short-circuit current and will be discussed in section 1.2.4. The dark current (J_0) is caused by recom-

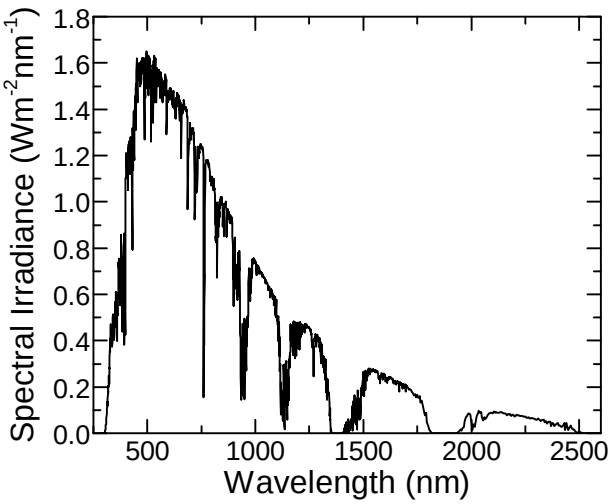


Figure 1.6: Spectral irradiance versus wavelength of the AM1.5G spectrum. Specified by the ASTM Terrestrial Reference Spectra for Photovoltaic Performance Evaluation.

bination within a solar cell. Simply put, reducing recombination of any kind in a solar cell will reduce J_0 and raise the open-circuit voltage. This section will serve to discuss the different types of recombination processes, and how those recombination processes relate to the dark current J_0.

Bulk Minority Carrier Lifetime and Recombination

The average rate of carrier recombination U within a semiconductor is given by Equation 1.8, where Δp is the number of excess minority carriers that are generated, and τ is the average lifetime of a minority carrier. As previously stated, many types of recombination can occur and affect the minority carrier lifetime τ.

$$U = \frac{\Delta p}{\tau} \tag{1.8}$$

Recombination that occurs inside the body of the semiconductor material is referred to as bulk recombination. Likewise, the average amount of time before a recombination event in the bulk is referred to as the bulk lifetime, τ_{bulk}, and is comprised

of three types of recombination as given by Equation 1.9.

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{radiative}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} \tag{1.9}$$

The first term on the right side of Equation 1.9, $1/\tau_{radiative}$, is due to radiative recombination, where $\tau_{radiative}$ is the average time before an electron and hole recombine by giving off energy as a photon. The rate of radiative recombination $U_{radiative}$ therefore depends on the product of the electron n and hole p concentration as shown in Equation 1.10, in which B is the bimolecular recombination constant, n is the electron concentration, p is the hole concentration, and n_i is the intrinsic carrier concentration.

$$U_{radiative} = B(np - n_i^2) \tag{1.10}$$

Radiative recombination is very important in direct-bandgap semiconductors such as GaAs, but is so slow that it is typically neglected for indirect-bandgap semiconductors such as silicon.

The second term in Equation 1.9, $1/\tau_{Auger}$, is due to Auger recombination, a process in which a minority carrier may recombine by transferring energy to another minority carrier. The rate of Auger recombination U_{Auger} is given by Equation 1.11, in which C_n and C_p are the Auger coefficients for electrons and holes, respectively.

$$U_{Auger} = C_n n(np - n_i^2) + C_p p(np - n_i^2) \tag{1.11}$$

Due to this process being dependent on three carriers being present (the electron and hole recombining and the extra minority carrier), Auger recombination becomes important when high carrier concentrations are present. For example, Kerr at al. showed for n-type samples with $N_D = 3.2 \times 10^{15}\,\mathrm{cm}^{-3}$, Auger recombination was not observed to begin reducing τ_{eff} until the excess carrier density was near $1 \times 10^{15}\,\mathrm{cm}^{-3}$

(close to high-level-injection) [4]. At this point, the auger-limited lifetime was ∼50 ms, which is a very high lifetime. The highest quality wafers used in this work had bulk lifetimes of ∼1 ms at an excess carrier density of $1 \times 10^{15}\,\mathrm{cm}^{-3}$, suggesting that other types of recombination were dominant.

The third term in Equation 1.9, $1/\tau_{SRH}$, represents recombination via defect or trap states and is referred to as Shockley-Read-Hall recombination (named after William Shockley, William Thorton Read Jr. and Robert Hall [5, 6]). The presence of contaminants such as metal ions can cause such energy states within the bandgap of the semiconductor, and such states are referred to as defect or trap states. The energy of carriers recombining via these trap states is given off by low energy photons or multiple phonon emission. The rate of SRH recombination U_{SRH} is given by Equation 1.12, in which v_{th} is the carrier thermal velocity, N_t and E_t are the concentration and energy level of the traps, σ is the capture cross section of the traps, and E_i is the intrinsic energy level.

$$U_{SRH} = v_{th} N_t \sigma \frac{np - n_i^2}{p + n + 2n_i \cosh\left(\frac{E_i - E_t}{kT}\right)} \tag{1.12}$$

Surface Recombination

Of course, a piece of semiconductor cannot be infinitely large, and therefore recombination at the surfaces of a semiconductor must be considered in addition to bulk recombination. At the surface of a semiconductor the crystal structure ends, and this disruption can lead to atoms at the surface having an unpaired electron, also called a 'dangling bond'. These dangling bonds provide energy states within the normally forbidden bandgap of the semiconductor, and thus facilitate SRH recombination of carriers. The rate of SRH recombination at the interface of a semiconductor and another material is given by Equation 1.13; in which N_{it}, σ_{it}, and E_{it}, are the concentration, capture cross-section, and energy level of traps at the interface, respectively.

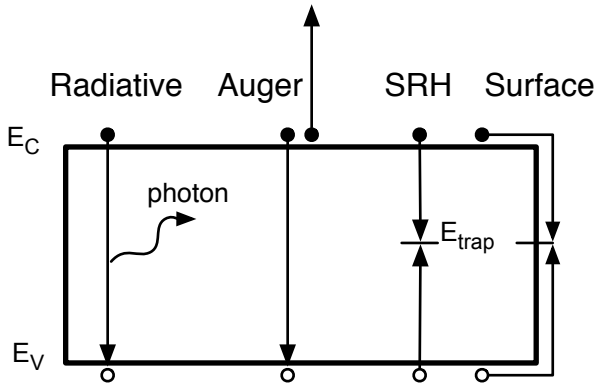


Figure 1.7: Illustration of bulk recombination via band-to-band radiative, Auger, and SRH processes.

$$U_{surface,SRH} = v_{th} N_{it} \sigma_{it} \frac{np - n_i^2}{p + n + 2n_i \cosh\left(\frac{E_i - E_{it}}{kT}\right)} \tag{1.13}$$

Since N_{it} is two-dimensional, the quantity $v_{th} N_{it} \sigma_{it}$ has units of velocity. This quantity is referred to as the surface recombination velocity (SRV or S). A low SRV indicates a low density of trap states from dangling bonds at the surface of a semiconductor. This can be accomplished by forming a bond with the unpaired electron of the dangling bond. Good surface passivation is indicated by a low SRV, and conversely a high SRV indicates a high density of dangling bonds and poor surface passivation.

Effective Minority Carrier Lifetime

The bulk and surface recombination processes presented are illustrated in Figure 1.7. The combined effects of bulk and surface recombination within a semiconductor, averaged over the substrate width W, result in an effective bulk lifetime, τ_{eff}, as shown in Equation 1.14.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} \tag{1.14}$$

The contribution of the surface lifetime, $\tau_{surface}$, to the effective lifetime, τ_{eff}, depends both on the geometry of the sample and the passivation level of the interface. Since SRV is a property of the interface that is independent of the geometry of the sample it is preferred for discussing the quality of surface passivation. Consider a one-dimensional semiconductor sample of uniform doping with two surfaces having SRV values of S_1 and S_2. The relation between $\tau_{surface}$ and S for identical surfaces ($S_1 = S_2$) can be closely approximated by Equation 1.15 [7], where W is the width of the sample, D is the minority carrier diffusion coefficient, and S is the surface recombination velocity.

$$\tau_{surface} \cong \frac{W}{2S} + \frac{1}{D}\left(\frac{W}{\pi}\right)^2 \tag{1.15}$$

Similarly for a one-dimensional sample with zero recombination at one surface ($S_2 = 0$), $\tau_{surface}$ can be approximated by Equation 1.16.

$$\tau_{surface} \cong \frac{W}{S_1} + \frac{4}{D}\left(\frac{W}{\pi}\right)^2 \tag{1.16}$$

The surface recombination velocity can be visualized by picturing a cloud of minority carriers generated in a semiconductor moving towards a surface to recombine. The velocity at which they move towards the surface to recombine is the surface recombination velocity. Achieving low surface recombination by passivating the dangling bonds at the surface of the silicon is crucial to achieving a high open-circuit voltage of a solar cell. The following section will relate recombination to dark current and therefore V_{OC}.

Dark Current and Recombination

Thus far, various recombination processes that can affect the minority carrier lifetime have been discussed, yet how these processes relate to the dark current J_0 is not yet apparent. As an example, let us consider a 1-dimensional p-n junction with metal

contacts (with infinite recombination) to the p and n type quasi-neutral regions, which have arbitrary widths. Dark current J_0 is carried by carriers that diffuse into the quasi-neutral regions under forward bias. This is described by Equation 1.17, where $D_{p,N}$, $L_{p,N}$, $N_{D,N}$, are the hole diffusivity, the hole diffusion length, and the donor density within the n-type quasi-neutral region of width W_N (Similarly, $D_{n,P}$, $L_{n,P}$, refer to the properties of electrons on the p-type side of doping $N_{A,P}$ and width W_P).

$$J_{0,PN} = qn_i^2 \left(\frac{D_{p,N}}{L_{p,N} N_{D,N}} \coth\left(\frac{W_N}{L_{p,N}}\right) + \frac{D_{n,P}}{L_{n,P} N_{A,P}} \coth\left(\frac{W_P}{L_{n,P}}\right) \right) \tag{1.17}$$

The minority carrier diffusion lengths $L_{p,N}$ and $L_{n,P}$ represent how far on average a minority carrier can diffuse in the bulk of a semiconductor before recombining. The diffusion length therefore must depend on the bulk lifetime, and this is given for holes in Equation 1.18, where $\tau_{p,N}$ is the bulk lifetime of holes in the n-type quasi-neutral region ($L_{n,P}$ can be similarly defined).

$$L_{p,N} = \sqrt{D_{p,N} \tau_{p,N}} \tag{1.18}$$

If the width of the quasi-neutral regions is semi-infinite, such that $W_N \gg L_{p,N}$ and $W_P \gg L_{n,P}$, the device is considered to be a 'long-base' diode. Equation 1.17 can then be reduced to Equation 1.19.

$$J_{0,PN} = qn_i^2 \left(\frac{1}{N_{D,N}} \sqrt{\frac{D_{p,N}}{\tau_{p,N}}} + \frac{1}{N_{A,P}} \sqrt{\frac{D_{n,P}}{\tau_{n,P}}} \right) \tag{1.19}$$

Equation 1.19 shows that the dark current in a long-base diode case depends upon the inverse of the minority carrier bulk lifetime. The longer the minority carrier lifetime (less recombination), the smaller J_0 becomes.

On the other hand, if the widths of the quasi-neutral regions are small, such that $W_N \ll L_{p,N}$ and $W_P \ll L_{n,P}$, then the device is considered to be a 'short-base' diode. Equation 1.17 can, in this case, be reduced to Equation 1.20.

$$J_{0,PN} = qn_i^2 \left(\frac{D_{p,N}}{W_N N_{D,N}} + \frac{D_{n,P}}{W_P N_{A,P}} \right) \tag{1.20}$$

Equation 1.20 shows that in the short-base diode, the dark current does not depend upon the bulk lifetime of the material. This is because the injected minority carriers will all reach the metal contacts and recombine there. Thus, the dark current depends only on how fast the carriers can diffuse to the contact $D_{p,N}/W_N$. Therefore, to reduce the dark current of a short-base diode, the recombination at the rear interface must be reduced.

For high-quality solar cells, substrates with low densities of bulk defects are preferred in order to provide high bulk lifetimes (and therefore long diffusion lengths). As a result, these will be short-base devices, and recombination at the interfaces must be reduced. This is accomplished in conventional p-n junction solar cells by the use of back-surface fields, a concept that is discussed at the end of this Chapter. Alternatively, a heterojunction may be used to prevent carriers from recombining at the contact, and this concept discussed in Chapter 2. The use of a heterojunction between titanium dioxide (TiO_2) and crystalline silicon as a back-surface field to reduce contact recombination is a major contribution of this thesis, and is discussed in Chapters 4 and 5.

In conclusion, the importance of reducing all kinds of recombination, and therefore dark current, within the solar cell has been shown. The mantra of reducing recombination in order to reduce dark current and therefore increase open-circuit voltage is one that will be a central theme of this dissertation.

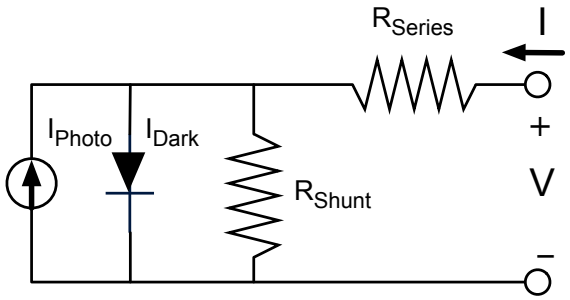


Figure 1.8: Equivalent circuit model for non-ideal solar cell with series and shunt resistances.

1.2.3 Fill Factor

The fill factor of a solar cell is greatly dependent on the series resistance and shunt resistance of the device. These resistances are shown incorporated into the solar cell model in Figure 1.8. The effect of these parasitic resistances will be discussed in turn, beginning with the series resistance R_S, and assuming that the shunt resistance R_{SH} is infinite. As current flows through the solar cell, there will be power dissipated in the series resistance. As a result, series resistance reduces the FF and η of a solar cell. This is shown by Equation 1.21

$$I(V) = I_0 \left(\exp\left(\frac{qV - IR_S}{nkT} \right) - 1 \right) - I_{photo} \tag{1.21}$$

The fractional power loss can be approximated by the calculating the power generated at the maximum power point minus the power dissipated in the resistor, as shown by Equation 1.22.

$$P_{loss,RS} = \left(1 - \frac{I_{MP} R_S}{V_{MP}} \right) \tag{1.22}$$

For series resistances that are not too large, I_{MP} and V_{MP} are close to I_{SC} and V_{OC}. Assuming that the I_{SC} and V_{OC} are unaffected by the R_S yields an expression for the

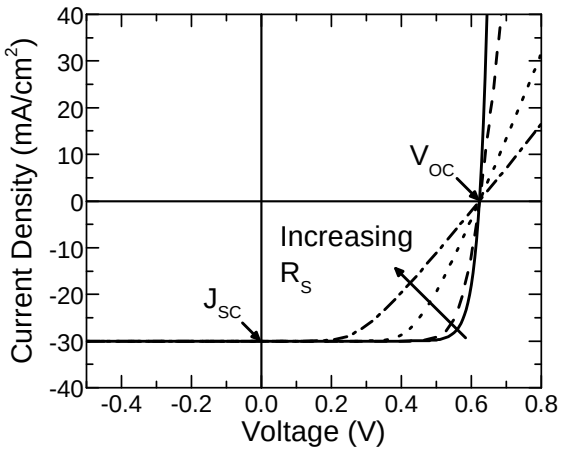


Figure 1.9: Effect of non-zero series resistance on the current-voltage characteristics of a solar cell.

fractional change in FF due to series resistance, shown in Equation 1.23.

$$FF_{loss,R_S} \approx \left(1 - \frac{I_{SC}R_S}{V_{OC}}\right) \tag{1.23}$$

This is easily visualised by plotting Equation 1.21 for several values of R_S, as shown in Figure 1.9. As the series resistance increases, the FF is decreased, and therefore the maximum power is also diminished. It is also clear that the moderate values of R_S do not affect the J_{SC} and V_{OC}, though it will be shown in later chapters that this is not always the case.

The effect of the shunt resistor will now be discussed. The shunt resistance provides an extra dark current path in the device in parallel with the diode, and therefore decreases the power output of the solar cell. Assuming no series resistance, the solar cell equation with finite shunt resistance is given by Equation 1.24.

$$I(V) = \frac{V}{R_{SH}} + I_0\left(\exp\left(\frac{qV}{nkT}\right) - 1\right) - I_{photo} \tag{1.24}$$

The same assumptions and approach used to reach Equation 1.23 can be applied here to obtain the fractional power loss due to a non-infinite shunt resistor, shown

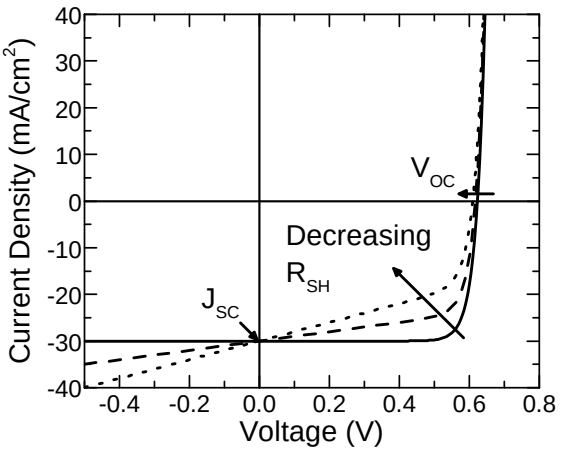


Figure 1.10: Effect of non-infinite shunt resistance on the current-voltage characteristics of a solar cell.

in Equation 1.25. Note that this is approximate because in reality a finite shunt resistance will affect the open-circuit voltage of the solar cell, while Equation 1.25 assumes it does not.

$$FF_{loss,R_{SH}} \approx P_{loss,RS} \approx \left(1 - \frac{V_{OC}}{I_{SC}R_{SH}}\right) \tag{1.25}$$

The effect that a shunt resistor has on the the fill factor and open-circuit voltage is shown in the current-voltage characteristic of Figure 1.10, which is calculated using Equation 1.24.

1.2.4 Short-Circuit Current

The short-circuit current is increased by improving the light absorption in a solar cell. This can be accomplished through the use of top anti-reflection coatings (ARCs) or by surface texturing techniques. Surface texturing increases the amount of light that enters the solar cell by deflecting incoming light that is reflected (and otherwise lost) to be incident on the semiconductor a second time. Once the light is in the absorber, it may be lost due to transmission from the rear of the solar cell, or by reflection at the

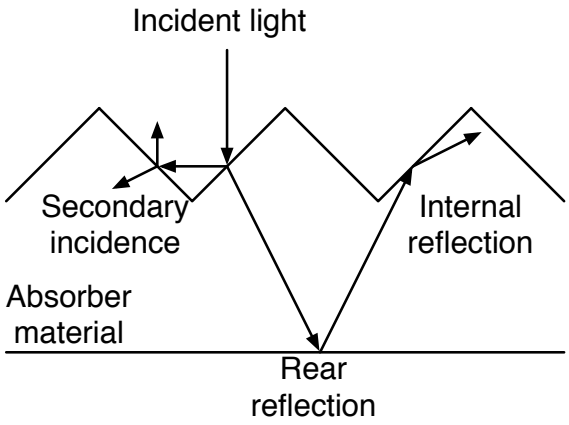
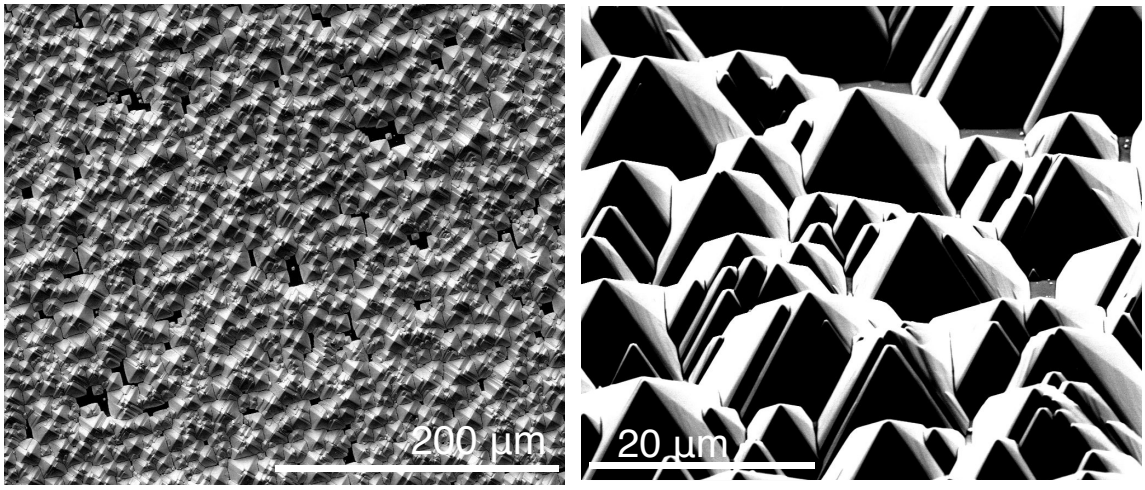


Figure 1.11: Schematic diagram of surface texturing contribution to reduced surface reflectance and increased light-trapping.

rear interface and transmission back out the front. Surface texturing can also serve to help trap this rear reflected light by increasing the angle of incidence at the top surface, such that the light is internally reflected within the semiconductor. These processes within a surface textured substrate are illustrated in Figure 1.11.

While many methods of texturing silicon surfaces can be employed, one of the most common is anisotropic etching in wet-chemical solutions [8]. Alkaline solutions such as potassium hydroxide or sodium hydroxide have been shown to etch preferentially along silicon $< 111 >$ crystal planes [9]. Tetramethylammonium hydroxide (TMAH) has also shown to be an effective, metal-ion free anisotropic etching solution [10]. These wet chemical etches provide a simple process that will transform a $< 100 >$ silicon surface into a randomly pyramidal-textured surface (with no patterning) or an ordered pyramidal textured surface (with lithographic patterns).

Figure 1.12 shows random pyramids that result from using a TMAH wet etch solution on a $< 100 >$ silicon wafer. The solution comprised 8 % isopropyl alcohol and 2 % TMAH in de-ionized water which was heated to 80 °C. Silicon samples were cleaned using the RCA cleaning procedure described in Chapter 3 and etched in



(a) (b)

Figure 1.12: SEM images of random pyramids as a result of TMAH etching on a silicon < 100 > wafer from (A) top and (B) side.

20:1 water to hydroflouric acid solution immediately prior to immersion in TMAH solution. Samples were immersed in TMAH solution for 2 h to 3 h.

1.3 Advanced p-n Junction Silicon Solar Cells and Limitations

Silicon is an element whose monocrystalline form has served as the backbone of the microelectronics industry. As a result, electronic-grade silicon is one of the purest materials readily available, as well as one of the most studied and well-understood. In addition to these advantages, silicon also has an almost ideal bandgap for a single-absorber solar cell. For these reasons silicon has become the material of choice for the vast majority of solar cell production and development.

The best crystalline silicon p-n junction based solar cells have reached 25 % efficiency under AM1.5 illumination [11]. The passivated emitter rear locally-diffused (PERL) cell developed at the University of New South Wales has reached efficiencies of (25.0 ± 0.5) % [12], and the all back-contact cell made by SunPower Corporation

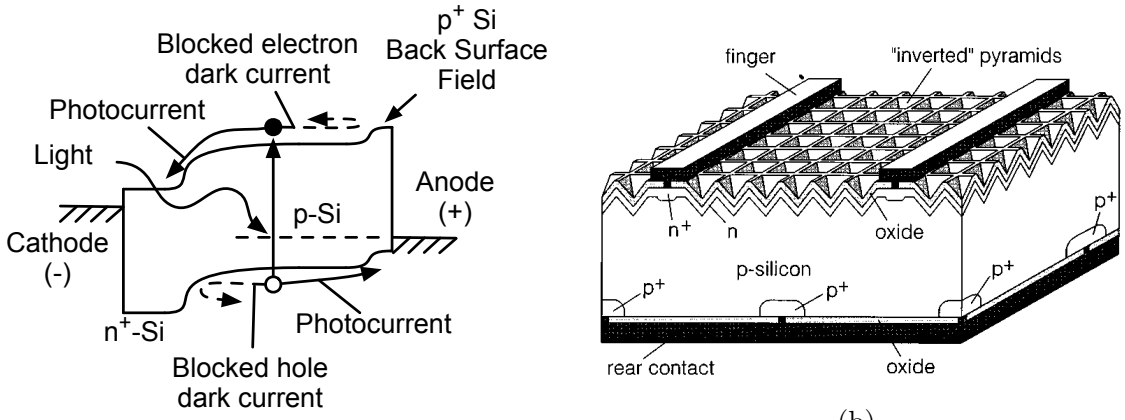


Figure 1.13: (A) Band diagram and (B) structure of PERL cell [14] (reprinted with permission).

has achieved an efficiency of $(25.0 \pm 0.7)\,\%$ [13]. A representative band diagram and structure of the PERL cell are shown in Figure 1.13.

The PERL cell achieves such high efficiencies due to several key features which are illustrated in Figure 1.13:

1. A high-temperature diffusion of phosphorus atoms is used to form an n-p junction at the top of the PERL cell. This provides the electric field that is needed to collect photogenerated current and prevents holes from recombining at the surface of the device (Figure 1.13a).

2. At the rear of the cell, optical lithography is used to define local anode contacts. By reducing the area of the p-type base which comes into contact with the metal anode, recombination is reduced (Figure 1.13b).

3. A high-temperature diffusion of boron atoms is used to form a p^+-p junction that serves as a 'back surface field' (BSF) at the localized anode contact points. The BSF reduces the contact resistance at the anode contact and reduces dark current from electron recombination at the metal anode. Minority carrier electrons are prevented from recombining at the anode because of the energy barrier

formed by the high-low doping of the p^+p junction (Figure 1.13a). A localized phosphorus diffusion is utilized to form an n^+ front surface field (FSF) for the same reasons.

4. Optical lithography and anisotropic etching techniques are used to form inverted pyramids on the surface of the solar cell. This surface texturing and the MgF_2/ZnS ARC deposited on top of it both serve to reduce reflection loss and improve light trapping (Figure 1.13b).

5. High-quality, thermally grown silicon dioxide is used over the majority of the solar cell geometry (openings are made only for emitter and base contacts) to provide excellent surface passivation.

While these features are exceptionally effective at preventing recombination, ohmic, and optical losses in the PERL cell, the processing required can be somewhat complicated. In order to form the n-type emitter, n^+ FSF, and p^+ BSF, high-temperatures (>800 °C) are required to diffuse the dopants into the silicon [15, 16]. The growth of the thermal oxide used for surface passivation also requires a high-temperature processing step. Additionally, the fabrication of the localized front and rear contact schemes, and the inverted pyramidal surface texturing require the use of optical lithography. While these processing techniques are reliable and effective, if simpler, lower-temperature processing methods are developed, this may present an opportunity to make high-efficiency crystalline silicon solar cells with lower manufacturing costs.

Goodrich et al. published a useful study showing the current (for 2011) cost structure for monocrystalline silicon-based solar cells as well as projections for future costs [17]. In that work, the costs of manufacturing several monocrystalline silicon solar cell architectures, including one similar to the PERL technology, were assessed. Goodrich et al. assumed suitably scalable manufacturing processes in or-

der to estimate the cost of such a solar cell, as the PERL process as presented is not commercially viable. For example, random surface texturing is assumed rather than lithographically defined inverted pyramid structures, silicon nitride from Plasma-Enhanced Chemical Vapor Deposition (PECVD) is assumed rather than thermally grown silicon dioxide for surface passivation and ARC, and the front localized n^+ FSF is assumed to be formed using a laser induced local-diffusion rather than a masked furnace diffusion. Assuming these scalable techniques, the solar cell based on the PERL architecture has a total cost of \$0.51 /W (peak direct-current power, assuming 22 % power conversion efficiency). The 160 µm-thick silicon wafer accounts for \$0.25 /W and manufacturing costs account for \$0.21 /W (the remaining cost is the 'required margin' for debt and equity investors).

In the supplemental material of the study, the manufacturing costs were further broken down into the costs (materials, labor, energy, equipment depreciation and maintenance) of the individual processing steps. Here it can be seen that even for this estimate of a low-cost PERL derivative cell, the cost of emitter formation using thermal diffusion (tube furnace, removal of phosphosilicate glass, and laser ablation steps), and of PECVD SiN for front and rear surface passivation account for ∼\$0.09 /W, or about 44 % of the manufacturing cost of the cell and about 18 % of the total cost of the cell. Therefore, Goodrich et al. showed that the manufacturing costs (even for an estimate of a nominally low-cost process) are significant and have room for reduction. While the calculation of cost estimates is not the focus of the work presented in this dissertation, one of the motivations for investigating low-temperature heterojunctions is to provide a potentially lower-cost method for making a crystalline silicon solar cell.

In addition to requiring additional processing, thermally driven dopant diffusion introduces some effects that lower the overall efficiency limits of silicon solar cells. It is generally accepted that the strongest limit on open-circuit voltage for a crystalline

silicon absorber is imposed by Auger recombination [18]. This upper limit is achieved for substrates with very low doping levels, as additional doping will decrease the limit [19]. High doping levels such as those used to form the front and back surface fields of the PERL cell also lead to band-gap narrowing effects, which further lower the upper limit for open-circuit voltage [20].

In conclusion, not only do conventional cells make use of processes that may not be friendly to scaled manufacturing (optical lithography, thermal processing), but the upper limit of efficiency is lowered due to the doping used in p-n junction based solar cells. Heterojunction solar cells, if engineered properly, do not require doping of the substrate, and therefore theoretically can achieve higher open-circuit voltage and efficiency than p-n junction solar cells [21]. Furthermore, silicon heterojunctions made with materials such as organic semiconductors can be deposited using solution-based techniques which are amenable to large-scale, roll-to-roll manufacturing. The goal of this dissertation is to provide progress towards such a heterojunction device that offers high-efficiency and facile fabrication.

1.4 Outline of This Dissertation

The purpose of this dissertation is to investigate the use of low-temperature heterojunctions to replace the diffused junctions that allow conventional silicon solar cells reach high-efficiencies, and thereby potentially lower manufacturing costs. In Chapter 2, the requirements for heterojunctions to be able to replace the diffused p-n junction, and BSF of a conventional silicon solar cell is presented. The motivations for using organic semiconductors and metal oxides for silicon heterojunctions is discussed, as well as the current state-of-the-art amorphous silicon heterojunction solar cell. Chapter 3 presents the formation of an electron-blocking heterojunction made between poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS or sim-

ply PEDOT) and crystalline silicon, as an alternative for a diffused p-n junction. The performance and current mechanisms of PEDOT/Si solar cells is evaluated, as well as inherent challenges and limitations. Chapter 4 presents the deposition process used for obtaining thin films of TiO_2, and the hole-blocking and passivating properties of the Si/TiO_2 heterojunction formed with this method. Chapter 5 presents the experimental demonstration of a Si/TiO_2 heterojunction used as a BSF for a PEDOT/Si heterojunction solar cell. The efficacy of the Si/TiO_2 BSF is shown to depend on the the SRV at the Si/TiO_2 interface and the thickness of the TiO_2 films. Chapter 6 discusses the incorporation of silver nanowires onto a PEDOT/Si solar cell to improve the performance of the device. Finally, Chapter 7 summarizes the work presented in this dissertation and provides some directions for future work.

Chapter 2

Overview of Low-Temperature Heterojunctions on Crystalline Silicon

2.1 Introduction

Instead of the p-n junctions discussedin the previous chapter, a monocrystalline silicon solar cell can be made with a heterojunction. As the name implies, a heterojunction is typically an interface between semiconductors of different bandgaps, materials, crystal structure, or some combination of these traits. In contrast, the p-n junction is a homojunction (same material with different dopants). The combination of inorganic and organic semiconductors to form hybrid heterojunction-based solar cells is of particular interest, and comprises the past work of Avasthi et al. that this thesis derives from [22–24].

Heterojunction solar cells offer several advantages over those based on homojunctions:

1. Heterojunction solar cells can achieve higher open-circuit voltages than homojunction cells [25]. The highest efficiency crystalline silicon-based solar cell was achieved using heterojunctions with amorphous silicon [26].

2. Hybrid heterojunctions may offer lower cost processing opportunities, due to the solution-based processes that can be used to deposit organic semiconductors.

3. Hybrid heterojunctions and heterojunctions using amorphous metal oxides can form wide-bandgap heterojunctions on crystalline silicon without the need for lattice matching.

4. Organic semiconductors and transition metal oxides offer a wide assortment of materials from which to choose. This aids the selection of materials with the ideal electronic and physical properties for making a heterojunction solar cell.

This chapter will discuss the requirements of a heterojunction to make an efficient solar cell, and how complementary heterojunctions affect each other. Additionally, the properties of amorphous silicon, organic semiconductors, and transition metal oxides and the advantages of heterojunctions comprising these materials will be discussed.

2.2 Requirements for Effective Heterojunctions on Crystalline Silicon

2.2.1 Band Alignments

This section will discuss the band alignment requirements of a heterojunction to be an effective replacement for a p-n junction or as a back-surface field in a silicon solar cell. The band alignments of a heterojunction should allow it to be carrier selective. This is accomplished by presenting an energy barrier in either the valence or conduction

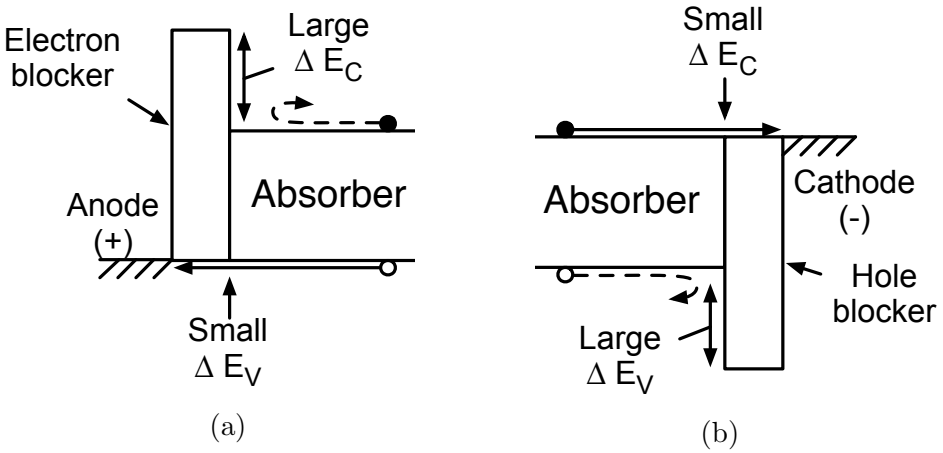


Figure 2.1: Band diagram showing ideal (A) electron-blocking and (B) hole-blocking heterojunctions. The electron blocking heterojunction has a large offset to the conduction band of the absorber, while being aligned to the valence band. The hole-blocker has the opposite band alignments. The filled and hollow circles in the band diagram represent free electrons and holes, respectively. The dashed and solid arrows represent blocked dark current and photocurrent, respectively.

band to block one type of carrier from flowing out of the absorber, yet allowing the opposite type to pass.

For example, a hole-selective, electron-blocking heterojunction, would block electrons from recombining at the anode (and therefore contributing to dark current) while allowing holes to freely pass. The energetic offset at the conduction band of the absorber ΔE_C serves as the energy barrier that blocks electrons. This reduces the dark current in the solar cell and improves the open-circuit voltage. The heterojunction allows holes carrying photocurrent to pass by minimizing the energetic offset at the valence band ΔE_V. The band alignments of an ideal hole-blocker are illustrated in Figure 2.1a.

Conversely, an electron-selective, hole-blocking heterojunction would have exactly the opposite band alignments. This heterojunction would provide an energy barrier to holes in the form of an offset in the valence band ΔE_V while minimizing the ΔE_C to allow electrons to flow freely out of the absorber. The band alignments of an ideal hole-blocker are illustrated in Figure 2.1b.

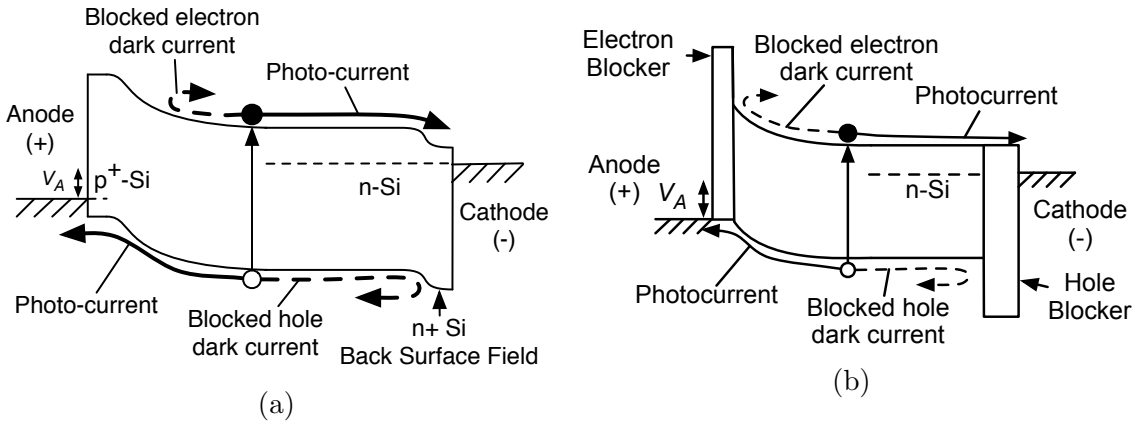


Figure 2.2: Comparison of (A) conventional n-type silicon solar cell with (B) ideal heterojunction solar cell under illumination and slight forward bias. The p^+ emitter and n^+ BSF are replaced with electron blocking and hole-blocking heterojunctions, respectively.

An additional requirement for the heterojunctions is that the work functions of the anode and cathode contacts must be high and low, respectively, such that they are aligned with the valence and conduction bands as shown in Figure 2.1. If the absorber is n-type, then a built-in electric field will form in the silicon near the electron blocking heterojunction due to the presence of the high work-function (aligned with the valence band) anode contact. This electric field serves to collect photogenerated current in the same manner as the p-n junction. Therefore for n-type solar cells, an electron-blocking heterojunction with a high work-function contact can be though of as an alternative to a diffused p-type emitter. There would be a built-in field at the hole-blocking contact as well, but of smaller magnitude due to the n-type doping of the absorber. Therefore for n-type solar cells, the hole-blocking heterojunction can be seen as an alternative for the diffused n^+ back-surface field. The band diagram of a conventional n-type silicon cell is shown in Figure 2.2a in comparison to an n-type heterojunction solar cell with near ideal band alignments, which is shown in Figure 2.2b.

2.2.2 Interface Passivation

An effective heterojunction must not only have the band alignments shown in Figure 2.1, but the interface must also prevent recombination via surface defects. As discussed in Chapter 1, defect states from dangling bonds at the surface of a semiconductor crystal can provide recombination centers. Since there is also a disruption of the crystal lattice of the absorber at a heterojunction there may be a large amount of defect states from dangling bonds. The defects can be passivated by the formation of new bonds to the heterojunction material. This is known as chemical passivation due to the formation of new chemical bonds. Alternatively, an electric field can be utilized to prevent minority carriers from reaching the defects in the first place. This is referred to as field passivation.

Surface passivation is particularly important for a heterojunction to be used as a back surface field. Continuing with the example of the n-type substrate solar cell, the hole-blocking heterojunction would act as the back-surface-field replacement. As previously mentioned, even with an ideal low work-function metal contact the band bending at the hole blocker will be less than that of the front junction. In addition, an ideal low work-function contact may be difficult to achieve in practice. Therefore, at the back interface, there may be little to no beneficial electric field to block minority carriers from reaching the heterojunction. This is the case for the hole-blocker illustrated in Figure 2.2b. Therefore, achieving a low SRV is critical in order for a heterojunction to act as an effective BSF.

Effect of SRV at Heterojunction Back-Surface Fields

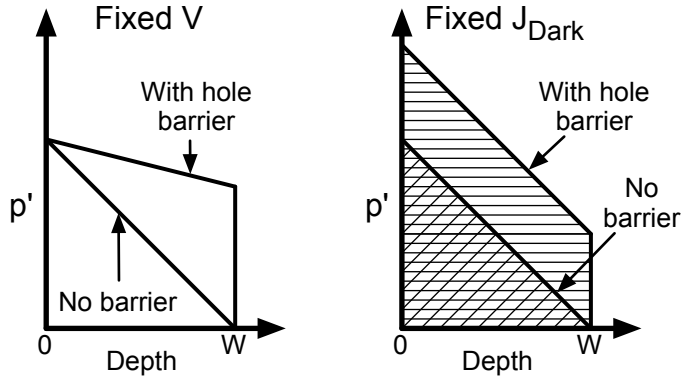
Section 2.2.1 presented the concept of using complementary electron and hole-blocking heterojunctions to replace the p-n junction and n^+ BSF of a conventional n-type silicon solar cell. Section 2.2.2 explained why the hole-blocking heterojunction is more sensitive to recombination than the front electron-blocking heterojunction due

to the lack of a large electric field. In this section, the effect of the SRV at the rear heterojunction on the dark current and the open-circuit voltage of the solar cell will be presented.

In the discussion that follows, it is assumed that the front junction of the device blocks majority carriers to the extent that minority-carrier injection into the substrate is the dominant dark current mechanism. In device terminology, this means the emitter injection efficiency of the front junction is unity. For an n-type substrate, this could be accomplished by using a heavily doped p^+ emitter, or by an electron-blocking front heterojunction.

The diffusion current carried by the injected holes is proportional to the slope of the excess minority carrier concentration profile through the depth of the n-type base region. In a short-base diode (no bulk recombination) the injected holes will all diffuse to the cathode and (if there is no hole-blocker) recombine there. The presence of a hole-blocking-heterojunction at the cathode, however, will reduce the holes that recombine at the cathode, and therefore reduce the dark current. As a result, for the same forward bias voltage, the slope of the hole concentration profile is reduced in a device with a hole-blocker at the cathode, in comparison to a device with no hole-blocker. This is illustrated in Figure 2.3a.

Similarly, for the same forward bias current, finite recombination at the hole-blocker results in a non-zero hole population at the rear interface. This corresponds to a higher concentration of holes at the edge of the depletion region, which occurs due to the greater applied voltage on the device with the hole-blocker. This bias condition is illustrated in Figure 2.3b. A fixed bias current is used in order to take measurements of the amount of stored charge in devices with and without a hole-blocker in Chapter 5. In Figure 2.3b cross-hatching is used to illustrate that a greater stored charge due to injected holes will be present in the device with the hole-blocker.



(a) (b)

Figure 2.3: Excess minority carrier hole concentration in the quasi-neutral region of silicon substrate with (A) fixed forward bias voltage and (B) fixed forward bias current. Compared are the hole profiles of a device with and without a hole-blocker at the cathode. The crosshatched area in (B) indicates the amount of stored charge due to the injected minority carriers in the quasi-neutral region of the devices.

Equation 2.1 gives the dark current due to the diffusion of injected holes across the quasi-neutral region of a short-base diode.

$$J_{p,diff} = \frac{qD_{p,N}}{W}\left[p'(0) - p'(W)\right] \tag{2.1}$$

In the single sided device, $p'(x) = 0$ due to the recombination of holes at the cathode, and Equation 2.1 reduces to Equation 2.2.

$$J_{p,SS} = \frac{qD_{p,N}}{W}p'(0) \tag{2.2}$$

For double-sided devices with the same forward bias voltage, the concentration of holes in the silicon at the edge of the depletion region will be the same as the single-sided case. However, the concentration of minority carriers at the cathode $p'(W)$ depends on the recombination rate at the Si/Hole-blocker interface. The current due to holes recombining at this interface is given by Equation 2.3 where $S_{Si/H_{blocker}}$ is the

recombination velocity at the Si/Hole-blocker interface.

$$J_{p,Si/H_{blocker}} = qS_{Si/H_{blocker}}p'(W) \tag{2.3}$$

Of course, due to current continuity $J_{p,Si/H_{blocker}} = J_{p,diff}$, and combining Equations 2.1, 2.2 and 2.3 yields an expression for the current in a double-sided device, as shown by Equation 2.4.

$$J_{p,DS} = \frac{qD_{p,N}}{W}p'(0)\left[\frac{1}{1+\frac{D_{p,N}}{WS_{Si/H_{blocker}}}}\right] = J_{p,SS}\left[\frac{1}{1+\frac{D}{WS_{Si/H_{blocker}}}}\right] \tag{2.4}$$

We can now define the blocking factor (BF), or the factor by which the dark current is reduced by the hole-blocker in comparison to a single-sided device, as shown by Equation 2.5.

$$BF \equiv \frac{1}{1+\frac{D_{p,N}}{WS_{Si/H_{blocker}}}} \tag{2.5}$$

The reduction in dark current due to a rear heterojunction will result in an increase in the open-circuit voltage. Using Equation 1.3, an expression for the difference in open-circuit voltage between a single and double-sided solar cell, ΔV_{OC} can be written (assuming low-level injection) as shown in Equation 2.6.

$$\Delta V_{OC} = V_{OC,DS} - V_{OC,SS} = \frac{nkT}{q}\ln\left(\frac{\frac{J_{SC,DS}}{J_{0,DS}}+1}{\frac{J_{SC,SS}}{J_{0,SS}}+1}\right) \tag{2.6}$$

Recognizing that $\frac{J_{SC}}{J_0} \gg 1$ for both the single and double-sided devices, $J_{SC,DS} \approx J_{SC,SS}$, and $J_{0,DS} = J_{0,SS}[1 + D_{p,N}/WS_{Si/H_{blocker}}]^{-1}$ from Equation 2.4, Equation 2.7 is obtained. The ΔV_{OC} under the assumption of low-level injection (n=1) is plotted as a function of $S_{Si/H_{blocker}}$ in Figure 2.4.

$$\Delta V_{OC} = \frac{nkT}{q}\ln\left(1+\frac{D_{p,N}}{WS_{Si/H_{blocker}}}\right) = \frac{nkT}{q}\ln\left(\frac{1}{BF}\right) \tag{2.7}$$

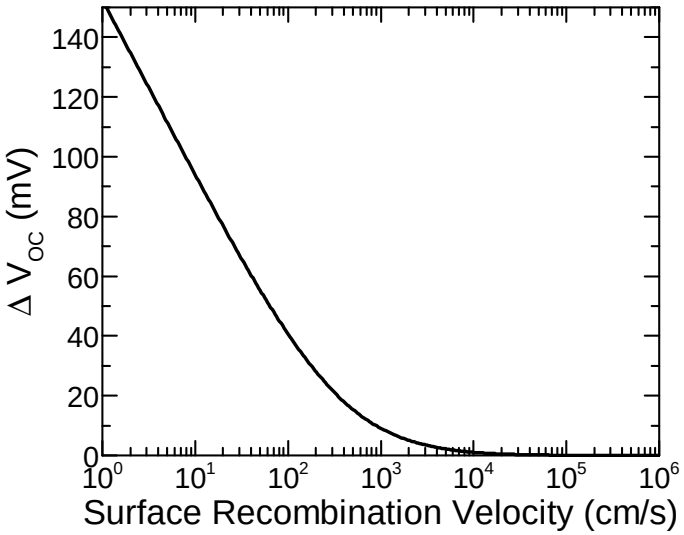


Figure 2.4: Dependence of ΔV_{OC} on the SRV of a hole-blocking heterojunction BSF.

Quasi-Steady-State Photoconductance Decay Measurement

In order to quantify the surface recombination velocity at a heterojunction interface, a method for measuring carrier lifetimes is needed. The Quasi-Steady-State Photoconductance Decay (QSSPCD) method is an extremely useful technique that allows the measurement of the effective minority carrier lifetime of a sample as a function of carrier density [27]. The QSSPCD setup is shown schematically in Figure 2.5. During the measurement, excess carriers are generated in the sample via illumination from a flash lamp held above the sample. The number of excess carriers that are generated due to the flash lamp can be estimated by measuring the conductivity of the sample via an inductive coil. The photogeneration rate that occurs within the silicon is known by utilizing a photodiode to measure the amount of light provided by the flash lamp during the measurement.

The Quasi-Steady-State name derives from the fact that the decay of the flash lamp is slow in comparison to the lifetime of carriers generated in the sample. The decay rate of the flash lamp is on the order of 5 ms to 10 ms, whereas the highest effective lifetime samples measured is about 1 ms. Because of this, the carrier distri-

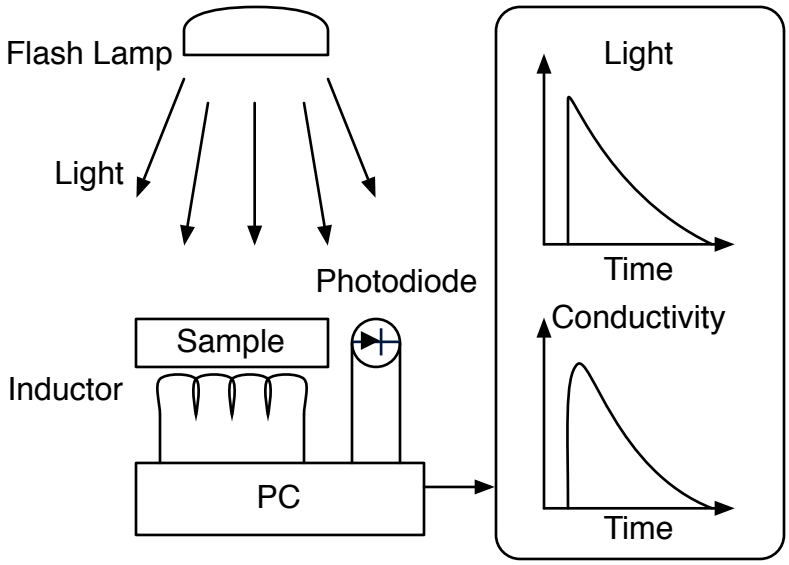


Figure 2.5: A schematic of the QSSPCD measurement setup. Shown on the left is the flash lamp light source, photodiode, silicon sample under measurement, and inductor for conductivity measurement of sample. On the right, the PC is shown gathering the data from the photodiode and inductor to display the illumination and conductivity of the sample as a function of time.

bution in the sample is assumed to be in quasi-steady-state at each time point during the measurement [27]. The effective lifetime can then be extracted by utilizing Equation 2.8. The relation between τ_{eff} and SRV was discussed in section 2.2.2. Therefore the QSSPCD technique allows the SRV of a sample to be measured.

$$\tau_{eff} = \frac{\Delta n_{ave}}{G_{ave} - \frac{dn_{ave}}{dt}} \tag{2.8}$$

2.3 Materials for Crystalline-Silicon-Based Heterojunction Solar Cells

2.3.1 Organic Semiconductors

Organic semiconductors are a unique class of materials that differ from inorganic semiconductors in several key ways. To start, the energy levels in many organic

semiconductors arise from delocalized bonding of π-symmetry orbitals of the atomic constituents. As a result, rather than possessing valence or conduction bands, organic semiconductors have many energy levels; the two of interest are aptly referred to as the Highest Occupied Molecular Orbital (HOMO) and Lowest Unoccupied Molecular Orbital (LUMO). As the names imply, the Fermi level in an organic semiconductor normally lies between these two energy levels (above the HOMO and below the LUMO) and the distance between the HOMO and LUMO levels is the band gap of the material. Therefore the HOMO of an organic semiconductor is analogous to the valence band of an inorganic semiconductor, and a similar comparison can be made for the LUMO to a conduction band. To be more specific, the location of the HOMO and LUMO levels result from the number of electrons and atoms in the π-system.

These π-orbital electrons, if good orbital overlap is present, may become delocalized, creating a conjugated system. A common example of this is the aromatic compound benzene. The charge transport within a system of conjugated organic molecules is dependent on the overlap between the π-orbitals between neighboring molecules. Thus, depending on the ordering of the system and level of overlap, charge transport between molecules and through the system overall may be dependent on quantum mechanical tunneling processes, in what is referred to as 'hopping' transport. This hopping transport has important consequences on the macroscopic electronic properties of organic semiconductors by drastically reducing carrier mobility in comparison to inorganic semiconductors.

Another important difference between organic semiconductors is that an excitation from the HOMO to the LUMO level (such as from optical absorption) does not immediately result in free carriers. Instead an exciton is created, in which the excited electron and resulting hole are tightly bound, with binding energies typically $\sim$0.1 eV to 0.5 eV [28]. This presents a major practical problem for organic photovoltaics, as an energetic interface (typically a heterojunction between two organic semiconductors)

must be used to separate the electron-hole pair. In contrast the excitonic binding energy in silicon much smaller (15.0 meV [29]), and is easily overcome by thermal energy near room temperature. The higher exciton binding energies in organics is due to the strong localization of wave functions in an organic system and the much lower dielectric constant of organic materials.

The properties of some organic semiconductors offer advantages over inorganic semiconductors. Small molecule organic semiconductors can be deposited by evaporation, while semiconducting organic polymers can typically be deposited via various solution-based methods such as spin-coating, dip-coating, doctor blading, spray-coating, etc. Solution based methods are particularly interesting due to their relative simplicity and potential for adoption into roll-to-roll manufacturing processes. Since organic molecules or polymers in a system may be held together only by relatively weak van der Waal's forces (in contrast to hydrogen bonding or the strong covalent bonds of inorganic semiconductors), they can demonstrate flexible mechanical properties. Organic semiconductors have also been shown to exhibit good surface passivation of crystalline silicon [30]. Additionally, organic semiconductors offer a huge variety of materials to choose from, ranging from small molecules to polymers. This large selection of materials allows for a broad range of electronic and optical properties to select from for a given application.

These unique properties allow organic semiconductors to be an attractive choice for making low-temperature heterojunction solar cells. Avasthi et al. demonstrated a hybrid silicon-organic heterojunction using poly(3-hexylthiophene) (P3HT) [22, 24] that achieved $\eta = 10.1\,\%$. In that work, PEDOT was used as a cathode contact due to its high work function and compatibility with solution processing. In this thesis, we seek to further this work by omitting the P3HT and forming a heterojunction directly between PEDOT and silicon, which will be discussed in Chapter 3.

2.3.2 Transition Metal Oxides

The properties of transition metal oxides make them interesting for a range of applications, including making heterojunctions on silicon. They typically have large bandgaps (3.15 eV for ZnO [31], 3.0 eV to 3.2 eV for crystalline TiO_2 [32]), and thus can be used as UV-absorbers in commercial products such as sunblock and paint pigments. Thin films of transition metal oxides are also useful as anti-reflection coatings on solar cells due to their relatively high values of refractive index ($\sim$2.1 for MoO_3 [33], 2.49 to 2.9 for crystalline TiO_2 [34]) within the visible spectrum.

Metal oxide films have also demonstrated excellent surface passivation of crystalline silicon. Alumina (Al_2O_3) thin films have been shown to provide excellent passivation on crystalline silicon via both atomic layer deposition (ALD) [35] and plasma enhanced atomic layer deposition (PEALD) [36]. These Al_2O_3 films have also been observed to maintain excellent surface passivation even after undergoing high-temperature firing processes [37]. The nature of the surface passivation of Al_2O_3 has been shown to be due to field passivation. A high density of negative charges in the Al_2O_3 induces a large amount of band bending at the silicon surface, which reduces recombination [35, 38].

Titanium dioxide has been shown in previous work to act as a hole-blocking heterojunction to crystalline silicon [39]. The band alignments and excellent surface passivation capabilities titanium dioxide of the Si/TiO_2 heterojunction are presented in this work in Chapter 4. The application of a Si/TiO_2 heterojunction as a back-surface-field in a solar cell will be discussed in Chapter 5.

2.4 Amorphous-Silicon/Crystalline-Silicon Heterojunction Solar Cells

The 'Heterojunction with Intrinsically Thin layer' (HIT) solar cell uses heterojunctions formed between amorphous silicon and crystalline silicon [40]. The amorphous silicon is deposited on a high-quality (very low bulk recombination) crystalline silicon substrate using Plasma Enhanced Chemical Vapor Deposition (PECVD) and is performed at temperatures $\sim$200 °C. In modern HIT solar cell structures, a thin layer of intrinsic amorphous silicon is used as a passivation layer, and a heavily doped amorphous silicon layer is added to achieve carrier selectivity. A band diagram is presented in Figure 2.6a to schematically show the function of an HIT solar cell.

Amorphous silicon possesses a larger bandgap than crystalline silicon ($\sim$1.7 eV [41]), and naturally forms an offset in both the conduction and valence band when forming a heterojunction with crystalline silicon. Given the electron affinity of amorphous silicon reported in the literature of (3.93 ± 0.07) eV below vacuum [42], this results in a ΔE_C of $\sim$0.1 eV and ΔE_V of $\sim$0.4 eV. The high valence band offset can potentially block photocurrent when forming the hole selective contact [43]. However, by heavily doping the p-type amorphous silicon during deposition, holes in the valence band are able to tunnel through the valence band offset, allowing photocurrent to flow.

The HIT solar cell currently holds the record for the highest efficiency of a crystalline silicon based solar cell, at 25.6 % efficiency under AM1.5G illumination [26]. The high efficiency of the HIT solar cell can be attributed to several key factors:

1. HIT solar cells do not require a thermal diffusion step to form the emitter, and can therefore take advantage of n-type substrates, which have greater minority carrier lifetimes than p-type substrates [44]. In contrast, making a p-n junction solar cell on an n-type substrate requires a boron diffusion, which can cause misfit dislocations that degrade the minority carrier lifetime.

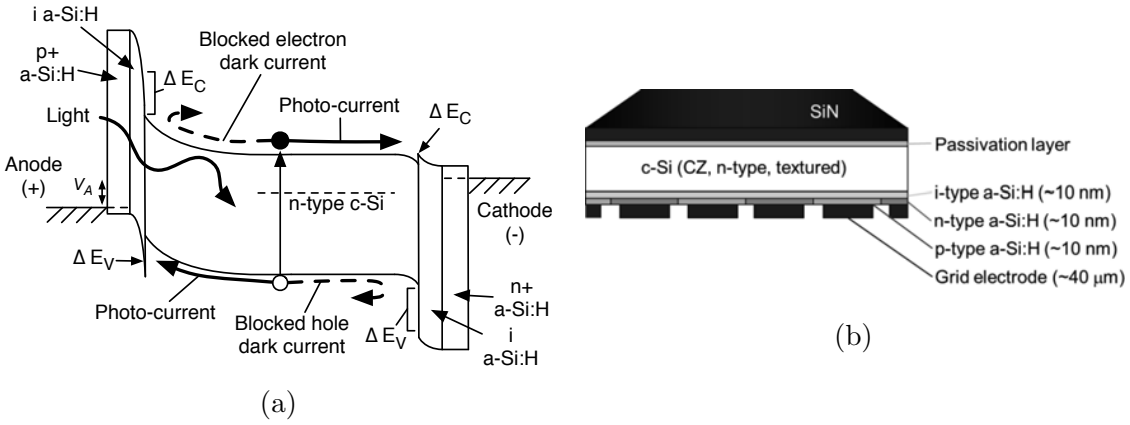


Figure 2.6: (A) Band diagram of a one-dimensional Heterojunction with Intrinsic Thin layer solar cell and (B) structure of the all-back contact HIT cell which achieved 25.6 % efficiency [26] (reprinted with permission).

2. The surface passivation quality of amorphous silicon can be extremely good (<2 cm/ sec), which allows for high V_{OC} values of up to 750 mV [45].

3. At the anode contact, the intrinsic layer of amorphous silicon underneath the heavily doped p-type layer is kept very thin. This allows carriers to tunnel through the valence band offset and reach the anode.

4. Recently, the Panasonic corporation has been able to demonstrate an HIT solar cell with an all-back contact approach, to minimize shadowing losses and maximize short-circuit current [26]. The structure of the device is shown in Figure 2.6b.

The HIT solar cell proves that silicon heterojunction solar cells can achieve very high efficiency, albeit at the cost of manufacturing complexity. A previous study, which was briefly discussed in Section 1.3, estimated the cost for sustainable large scale manufacturing of an HIT inspired solar cell to be \$0.62 /W [17]. The manufacturing costs account for \$0.30 /W, and the 140 µm-thick silicon wafer accounts for \$0.23 /W (the remainder is 'required margin' for debt and equity investors). Within the manufacturing costs, the PECVD of amorphous and nanocrystalline silicon accounts for ∼\$0.11 /W, or about 37 % of the manufacturing cost of the cell and about

18 % of the total cost of the cell. This goes to show that there is significant room for cost reductions, even within the low estimated manufacturing costs of the HIT inspired solar cell discussed here.

An approach that may achieve lower manufacturing costs is to use alternative materials, such as the organic semiconductors and metal oxides discussed in section 2.3, to make heterojunctions to crystalline silicon. As described previously, these materials may offer manufacturing methods more suited to large-scale manufacturing than the plasma-deposition of amorphous silicon. For example, the use of organic semiconductors may allow solution-based, roll-to-roll manufacturing techniques. If the band alignment and surface passivation requirements can be met to the level that HIT achieves, similar solar cell efficiencies will be possible with these other heterojunction materials. Therefore, the work in this dissertation seeks to investigate the merits of crystalline silicon heterojunctions using organic semiconductor and metal oxide materials as an alternative to amorphous silicon.

Chapter 3

PEDOT/Silicon Heterojunction Solar Cells

3.1 Introduction

The purpose of this chapter is to discuss the heterojunction formed between the organic semiconductor Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS or simply PEDOT) and crystalline silicon. PEDOT:PSS is a polymer that can be formulated to be highly conductive and transparent, making it useful for a variety of applications [46]. Some examples include use as a static dissipative coating, for flexible transparent electrodes, and for hole contacts in organic photovoltaic devices [47–49]. When coated onto an n-type crystalline silicon wafer, the resulting heterojunction behaves as an excellent rectifying diode for photovoltaic applications.

The PEDOT and PSS represent two charged polymers, as shown in Figure 3.1. Together they form a macromolecular salt in which the oxidized PEDOT is the cation and the PSS is deprotonated as the anion [46, 50]. Due to this charge transfer, the PSS effectively acts as a dopant, which causes the PEDOT to behave as a degenerately doped p-type organic semiconductor [51, 52]. The charge density resulting in

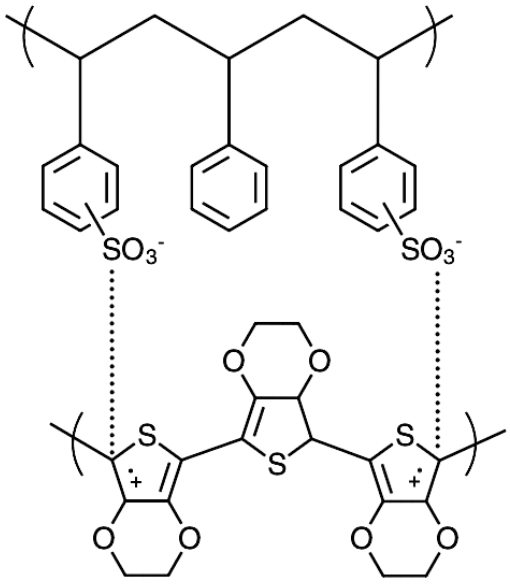


Figure 3.1: PEDOT (bottom) and PSS (top) ionomers, showing charge transfer of an electron from the PEDOT to the PSS.

PEDOT:PSS films can therefore be very high, and leads to the conductive properties of the film [46]. The electronic properties of PEDOT:PSS will be discussed in detail within this chapter.

PEDOT:PSS is commonly available as an aqueous solution that results from polymerizing EDOT monomers using PSS as the aqueous polyelectrolyte and $Na_2S_2O_8$ as the oxidizing agent (this is known as the 'Baytron P' process) [50]. This allows PEDOT:PSS to be compatible with a variety of solution-based coating processes, which are attractive as potentially low-cost/large volume manufacturing methods [53].

In this chapter, PEDOT:PSS films and PEDOT/Si solar cells are discussed. Section 3.2 presents the fabrication process of PEDOT:PSS resistivity test structures and PEDOT/Si solar cells and spectroscopy samples. Section 3.3 describes the conductivity of PEDOT:PSS films and how it can be enhanced through additives. Section 3.4 presents the band structure and work function of PEDOT:PSS on silicon as measured by photoemission spectroscopy. Section 3.5 presents the current-voltage

characteristics and reverse recovery measurements of the PEDOT/Si solar cell [54] and section 3.6 discusses some of its limitations.

3.2 Fabrication

PEDOT:PSS was purchased as 1.4 % dispersion by weight in water (Clevios PH1000) and 10 % w/w dimethyl sulfoxide (DMSO) was added to enhance the conductivity of the film as discussed in section 3.3. 0.25 % Zonyl FS-300 surfactant was added to the solution to facilitate wetting [55–57]. While oxidized silicon is hydrophylic, hydrogen terminated silicon surfaces are hydrophobic, and a surfactant is commonly needed to promote wetting with the water-based PEDOT:PSS solution [33, 55–61].

For measurements of sheet resistance, PEDOT:PSS films were fabricated on 1 inch×1 inch glass slides. The glass slides were cleaned using a solvent clean, which involved successive baths of acetone, methanol, and isopropanol, all with ultrasonic (US) agitation at room temperature for 5 min each. The slides were then dried using a nitrogen gun. PEDOT:PSS thin films were obtained by spin-coating the PEDOT:PSS solution onto the glass slides at 4000 rpm for 210 seconds to obtain ∼70 nm dried films. The samples were then placed in a thermal evaporator for deposition of 200 nm silver in the geometry of a transmission line measurement structure.

The fabrication of the PEDOT/Si solar cell can be done at a lower maximum temperature (<100 °C) than that of a conventional p-n junction solar cell (∼800 °C). The fabrication process and the finished structure of the device is shown in Figure 3.2 First, the starting substrates of 2 Ω cm to 4 Ω cm phosphorus doped, single-side polished $< 100 >$ (CZ) silicon wafers were coated with photoresist and diced into 16 mm×16 mm samples. The samples were then solvent cleaned, which involved

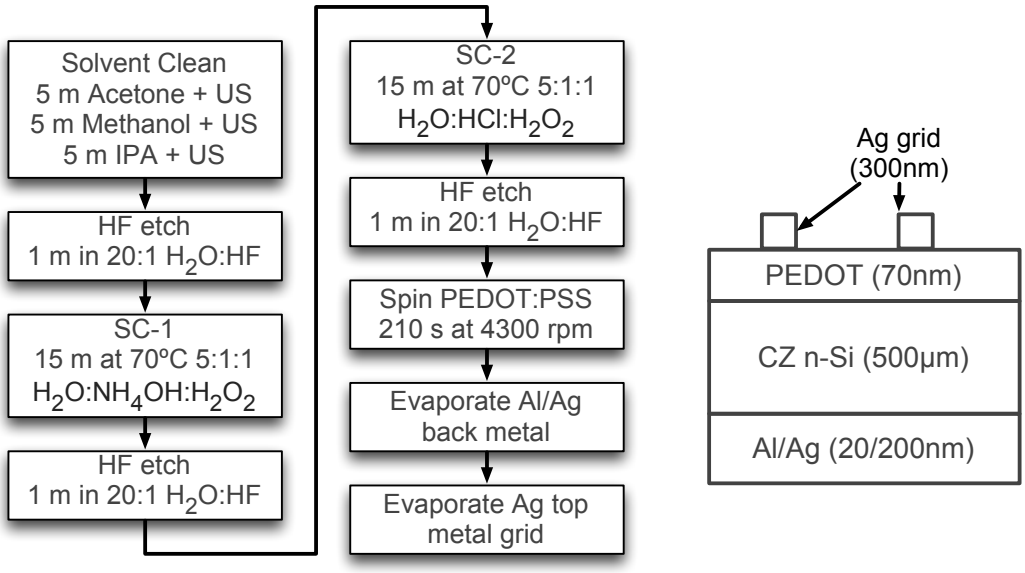


Figure 3.2: Fabrication process and structure of PEDOT/Si solar cell

successive baths of acetone, methanol, and isopropanol, all with ultrasonic agitation at room temperature for 5 minutes each.

The silicon wafers are then cleaned using the standard RCA cleaning procedure [62]. The cleaning begins with a 20:1 H_2O:HF acid dip for 1 minute to remove native oxide, and is followed by 15 minutes in 'standard clean one' or SC-1, which is a bath of 5:1:1 H_2O:NH_4OH:H_2O_2 heated to 75 °C. The purpose of the ammonium-hydroxide-based clean is to remove organic contaminants from the surface of the silicon and grow a thin sacrificial surface oxide. This oxide is removed with another 20:1 H_2O:HF acid dip for 1 minute before the SC-2 clean, which is a bath of 5:1:1 H_2O:HCl:H_2O_2 heated to 75 °C. The hydrochloric acid in SC-2 serves to remove metallic contaminants, and another sacrificial oxide is grown within the bath. The samples are again dipped in a 20:1 H_2O:HF acid dip for 1 minute immediately prior to coating with PEDOT:PSS. This final HF dip removes all surface oxide and provides a hydrogen-terminated silicon surface [63]. A volume of 200 µL of PEDOT:PSS is dropped onto the top, polished side of the 16 mm×16 mm silicon sample and spun at 4300 rpm for 210 seconds.

No baking process is utilized after PEDOT:PSS coating to avoid any ambient oxidation of the hydrogen-passivated silicon surface. Instead, the devices are immediately placed into a high-vacuum chamber to remove excess water from the PEDOT:PSS and to receive thermal evaporation of 20 nm aluminum and 100 nm silver to form the cathode contact on the back of the device. The base pressure of the evaporator is typically 5.0×10^{-7} torr to 8.0×10^{-7} torr. Another thermal evaporation of silver is performed with a shadow mask onto the top of the PEDOT:PSS to form the anode contact. The top metal is made up of a finger and busbar grid pattern to allow light to enter the PEDOT/Si device and reduce lateral resistive losses in the PEDOT:PSS film. The devices presented in this Chapter use a grid that covers 9.7 % of the surface (the grid layout is shown in Figure A.2). Device fabrication is completed by using a probe and optical table to accurately scribe the PEDOT:PSS into separate devices with active regions of 4 mm×4 mm.

The fabrication of PEDOT/Si samples for photoemission spectroscopy follows the procedure for solar cells, but with different substrates. Highly-doped 10^{19} cm^{-3} phosphorus <100> n-type silicon wafers were used for these measurements to ensure good sample conduction during the measurement. The samples were smaller (10 mm×10 mm) and received no metallization on top of the PEDOT:PSS, while the back contact was formed using InGa eutectic.

3.3 PEDOT:PSS Conductivity

As described in Chapter 2, the conductivity through organic semiconductors can be dependent on hopping transport between localized electronic states, and this is true for transport in PEDOT:PSS films as well. PEDOT:PSS does not form an ordered (crystalline) system, however the arrangement of the PEDOT and PSS chains has consequences for the conductivity of the films [46]. A PEDOT:PSS dispersion

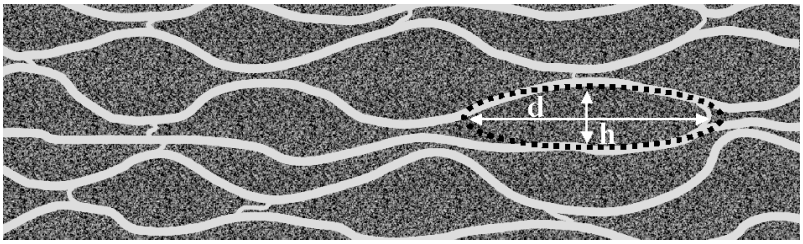


Figure 3.3: Cross-section view of the morphological model of PEDOT:PSS film presented by Nardes et al., reprinted with permission [66]. The dark PEDOT clusters are separated by the light PSS lamellas. The pancake-like, PEDOT-rich island is outlined by the dotted line. The typical diameter d is 20 nm to 25 nm, and the typical height h is 5 nm to 6 nm.

in water takes the form of gel particles, with a PEDOT inner core and PSS outer core [64]. When the dispersion is spin-coated, the resulting films of PEDOT:PSS form flattened, disk-like structures where PEDOT cores are surrounded by insulating PSS shells. Since the conduction is carried by the conjugated PEDOT and the PSS-rich shells are insulating [65], the formation of flat disks of PEDOT between shells of PSS contributes to an anisotropic conduction behavior [66, 67]. This phenomena is also observed in sputtered PEDOT:PSS films [51] The structure of the PEDOT:PSS films is shown in Figure 3.3. The main limiting factor of conductivity is based on the arrangement of insulating PSS shells with regard to the conductive PEDOT islands.

The conductivity of PEDOT:PSS films can be increased by several orders of magnitude through the use of so-called secondary doping techniques [46]. The arrangement of the PEDOT and PSS can be modified via the addition of solvents, which essentially allow the PEDOT and PSS to reach a more favorable configuration for current transport [53]. This likely occurs via solvation to break up the cation and anion aggregates. This rearrangement allows for the PEDOT grains to form favorable conductive pathways that allow for higher conductivity in the resulting films. A variety of solvents have been shown to accomplish this including sorbitol [68], methanol [47], ethylene glycol [64, 69, 70], and dimethyl sulfoxide (DMSO) [48, 49, 70–74] (combi-

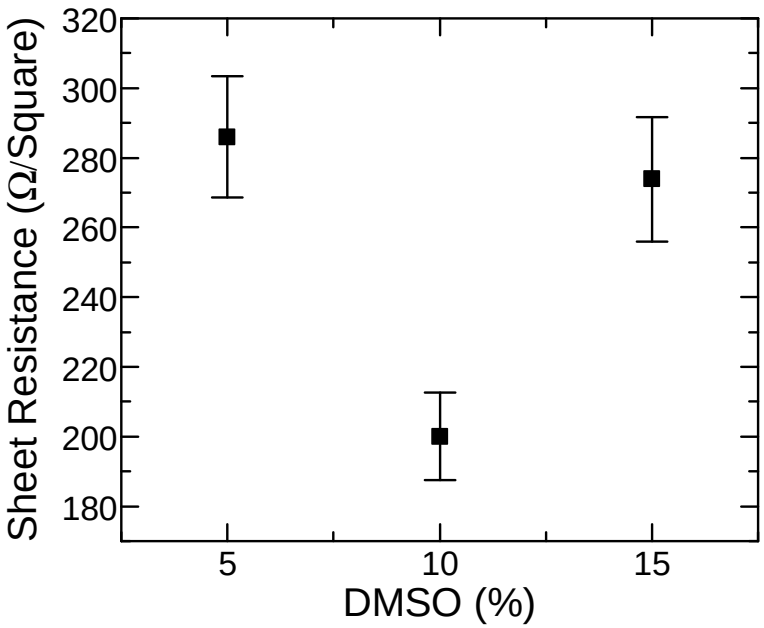


Figure 3.4: Sheet resistance of a dried film of PEDOT:PSS (thickness $\sim$ 70 nm) on glass versus weight/weight concentration of DMSO in Clevios PH1000 PEDOT:PSS aqueous solution (1.0 % to 1.3 % solids)

nations of solvents have also been demonstrated [75]). Other work has shown that sulfuric acid treatment serves to replace PSS by inorganic solvation in PEDOT:PSS films and thereby enhance conductivity [76].

While the studies cover different brands and types of PEDOT:PSS formulations, in general, the greatest conductivity enhancements from solvent modification have been achieved using DMSO [46]. As such, in this work, DMSO was used to enhance the conductivity of the PEDOT:PSS films. The lowest sheet resistance of 197 $\Omega/\square$ for 70 nm PEDOT films on glass was observed via the addition of 10 % w/w DMSO to Clevios PH1000, as shown in Figure 3.4. The maximum conductivity of 714 S/cm obtained is close to those obtained in other studies using PH1000 of 966 S/cm [72].

3.4 Band Structure of PEDOT:PSS

The location of energy levels of the PEDOT:PSS was measured via photoelectron spectroscopy (PES) techniques in collaboration with Gabriel Man. These techniques involve the excitation of electrons by a photon from a solid into a vacuum. By measuring the kinetic energy and number of electrons emitted, a picture of the binding energies of electrons in a material can be constructed. This therefore gives information regarding the filled electron states in a material. Ultraviolet Photoemission Spectroscopy (UPS) enables the measurement of the work function of the material and the valence band location with respect to the Fermi level. The work function of the PEDOT:PSS is determined via the photo-emission cut-off of the UPS spectra, as shown in Figure 3.5.

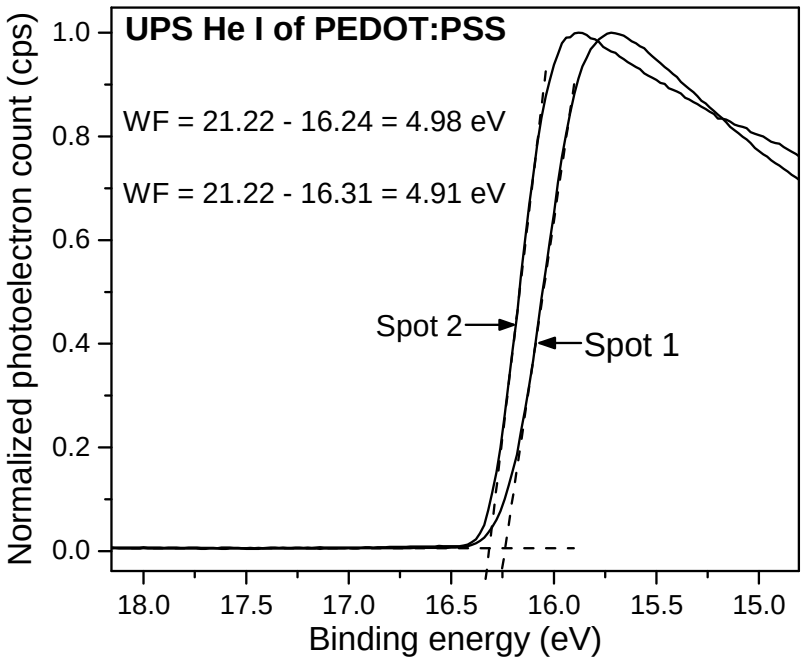


Figure 3.5: UPS scan of PEDOT:PSS on n^+-Si substrate using 21.22 eV He light emission. Shown is the photoemission cut-off and calculation of the work-function of the PEDOT. Measurement courtesy of Gabriel Man.

The photo-emission cut-off occurs at a binding energy of 16.24 eV to 16.31 eV for the two measurement sites. Since the excitation energy of the He I line is known

to be 21.22 eV, the work function can be calculated to be 4.94 eV (average of two spots). The measured work function in this work agrees with others presented in the literature [52].

Figure 3.6 shows the UPS photoemission spectra showing the edge of the HOMO of the PEDOT:PSS with respect to the Fermi level. The data show energy states that reach up to the Fermi energy and beyond, indicating degenerative doping of the PEDOT. The HOMO level of the PEDOT:PSS is very closely aligned with the work function of the PEDOT:PSS at ∼4.94 eV below the vacuum level. The location of the Fermi level at the HOMO provides evidence that PEDOT:PSS is a degenerately doped p-type semiconductor.

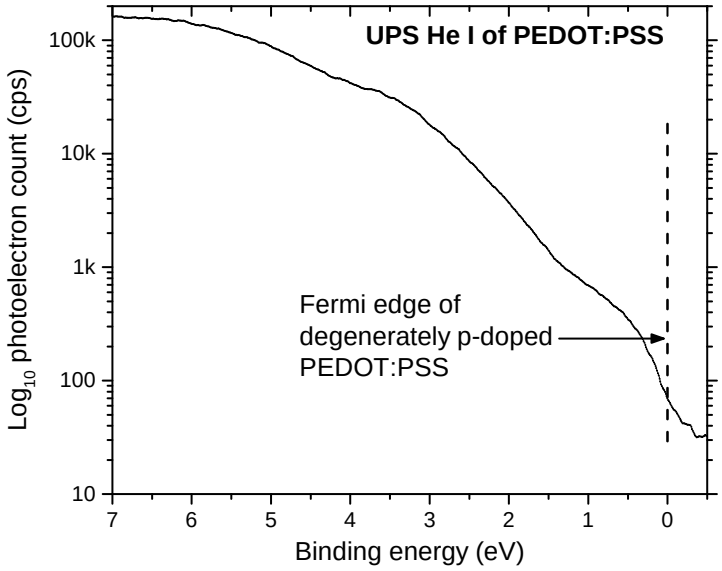


Figure 3.6: UPS Helium 1 scan of PEDOT:PSS on n^+-Si substrate showing HOMO location aligned with the Fermi level. Measurement courtesy of Gabriel Man.

A complementary technique to UPS is Inverse Photoemission Spectroscopy (IPES). In IPES electrons of a known kinetic energy are directed at a sample and couple into empty energy states. The decay of these electrons from higher to lower unoccupied states results is partially due to radiative transitions, and the photons given off are observed. IPES therefore measures the energy levels of empty states

within materials, and is a complementary technique to UPS because it provides information regarding the location of the valence band or LUMO with respect to the Fermi level. Figure 3.7 shows the IPES data from a PEDOT/Si device. The data show the beginning of the LUMO states at a binding energy of ~ -1.48 eV with respect to the Fermi level.

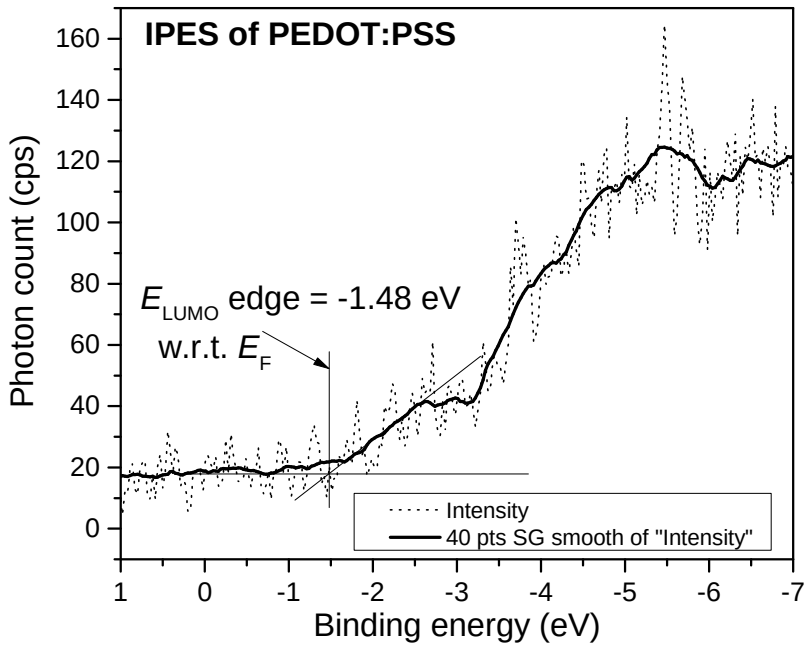


Figure 3.7: IPES scan of PEDOT:PSS on n^+-Si substrate showing LUMO edge 1.48 eV above the Fermi level. Dots are data points and solid line is a 40 pt moving average smooth of data. Measurement courtesy of Gabriel Man.

The UPS and IPES data together confirm several key electronic properties of the PEDOT:PSS. First, the location of the LUMO level at 3.46 eV below the vacuum level, which is 0.59 eV above the conduction band of silicon (4.05 eV below vacuum). This shows that PEDOT:PSS provides an energetic barrier for electrons in the conduction band of silicon from recombining at the device anode. This barrier is crucial for PEDOT:PSS to function as a hole-selective contact. Second, the PEDOT:PSS is observed to have a HOMO level at 4.94 eV below vacuum, which is closely aligned with the silicon valence band location of 5.16 eV. This shows that there is no barrier

to impede holes in the valence band of the silicon from flowing into the PEDOT:PSS. Finally, the data confirm the high work function of the PEDOT:PSS of 4.94 eV. This observation supports the model of PEDOT:PSS pushing electrons away from the surface of the silicon and thereby converting the surface region from n-type to p-type ('inversion'). Capacitance-voltage measurements of PEDOT/Si heterojunctions presented in the literature also show evidence of surface inversion of the n-type silicon [56, 61]. The spectroscopic data observed are also consistent with the values presented in the literature [52, 56], and confirm the function of PEDOT:PSS as having the band-offsets needed to act as a carrier-selective heterojunction to silicon. The offsets are summarized in Figure 3.8.

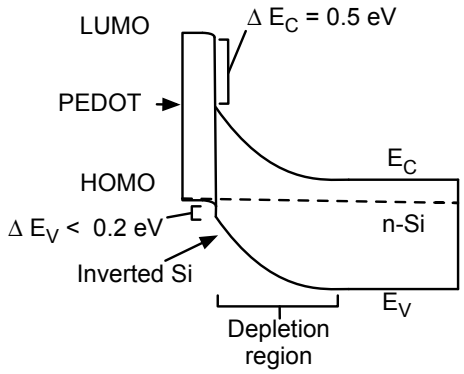


Figure 3.8: Schematic illustration of band-alignment at PEDOT/Si interface as measured by PES by Gabriel Man.

3.5 Silicon/PEDOT Photovoltaic Devices

While there have been many examples in the literature of PEDOT/Si photovoltaic devices, the exact character of the junction that forms at the PEDOT/Si interface is somewhat debated. Some examples of PEDOT/Si devices in the literature describe the interface as a Schottky-type junction [33, 57, 60]. However this model does not accurately represent the PEDOT/Si device J-V characteristics or charge storage

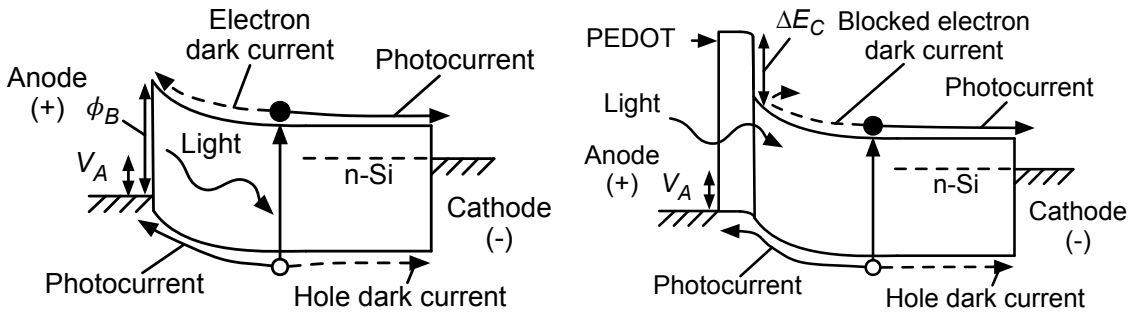


Figure 3.9: Band diagrams of photovoltaic devices under illumination with small forward bias. (A) A simple Schottky-junction device compared to a (B) PEDOT/Si device.

behavior to be shown in this work. As Erickson, et al. describe, the PEDOT/Si heterojunction operates similarly to a p-n junction because the high work-function of the PEDOT converts the surface of the n-type silicon to p-type (surface inversion) [56]. The verification of the high-work function of the PEDOT:PSS was presented in the previous section. Within the model of an inverted junction, the carrier-selective offsets of the PEDOT:PSS band structure are important as they act to further reduce the recombination at the silicon interface.

An illustration of the band diagram of a PEDOT/Si device under illumination and small forward bias along with a Schottky-junction device under the same conditions are presented in Figure 3.9. In the band diagrams, filled and hollow circles represent electrons and holes, respectively. The dashed lines show the flow of dark current while solid lines represent photocurrent.

In the Schottky-junction of Figure 3.9a, electrons in the conduction band are prevented from flowing towards the anode by the built-in electric field present within the diode. When a forward bias is applied, the barrier is reduced, and the flow of electrons to the anode dominates the dark current characteristics of the Schottky diode.

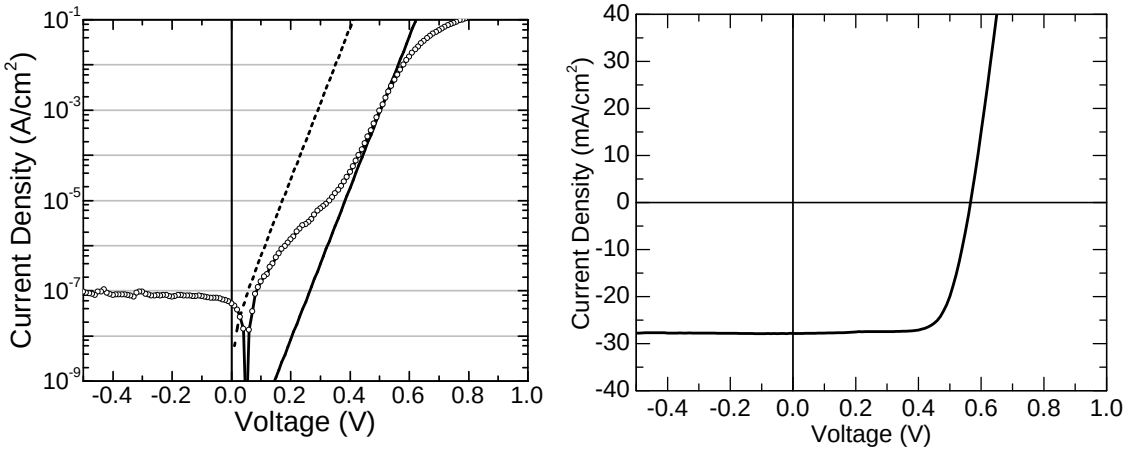
However, in the PEDOT/Si device of Figure 3.9b, electrons in the conduction band of silicon are blocked from entering the PEDOT:PSS because of both the electric field in the silicon and the offset ΔE_C of the PEDOT:PSS LUMO from the conduction band of silicon. Conversely, the lack of an offset between the silicon valence band and the PEDOT:PSS HOMO level allows holes to flow towards the anode and carry photocurrent. Because of the barrier to electron current present in the PEDOT/Si device, the dark current flowing in the device is carried by holes injected into the body of the n-type silicon. This conclusion is supported by the current-voltage and reverse-recovery measurements in the following sections.

3.5.1 Current-Voltage Measurements

Figure 3.10a presents the J-V characteristics for a PEDOT/Si heterojunction cell under dark conditions (continuous black line). The diode shows some non-ideality ($n = 2$) at lower current levels ($\sim 10^{-6}$ to $10^{-7}\,\mathrm{A\,cm^{-2}}$), which may be due to small amounts of surface defect states at the PEDOT/Si interface. The diode regains an ideality factor of close to 1 at higher values of forward-bias (>0.4 V). As the bias increases further, the voltage drop due to current flowing through series resistance in the device causes the J-V curve to curl over. The ideal portion of the J-V curve and the ideal diode Equation 1.1 can be used to fit a saturation current. At $1.3\,\mathrm{mA\,cm^{-2}}$ forward current, and using an ideality factor of 1 we can extract a saturation current (J_0) to be $3.8 \times 10^{-12}\,\mathrm{A\,cm^{-2}}$ (the solid line in Fig. 3.10a).

The saturation current observed is much lower than would predict from a Schottky-junction device. The dark current for a Schottky diode is dominated by electrons, the majority carrier, and is given in Equation 3.1 where A^* is the Richardson constant, T is temperature, ϕ_B is the Schottky barrier height, and k is the Boltzmann constant.

$$J_{0,electrons} = A^* T^2 e^{-\frac{\phi_B}{kT}} \tag{3.1}$$



(a) (b)

Figure 3.10: Current-density vs voltage characteristics of a SOH solar cell on (A) a semi-log plot in the dark and (B) a linear plot under AM1.5G illumination. On the semi=log plot, the dashed line is the current expected from a Schottky device with the same work-function as PEDOT and the solid line is an fit to the ideal (n=1) exponential region of the device data, which is represented by hollow circles.

The Schottky barrier, ϕ_B, of a metal to an n-type semiconductor is dependent only on the work-function of the metal (ϕ_{metal}) at the silicon interface and the electron affinity of the semiconductor (χ_{semi}), as shown by Equation 3.2.

$$q\phi_{B,n} = q\phi_{metal} - \chi_{semi} \tag{3.2}$$

Given the work function of PEDOT:PSS of $\sim$4.94 eV and the electron affinity of silicon of 4.05 eV, Equation 3.2 predicts a Schottky junction with a barrier height of $\phi_B = 0.89\,\text{eV}$. Using Equation 3.1, the saturation current density of such a Schottky diode is calculated to be $1.17 \times 10^{-8}\,\text{A cm}^{-2}$. The resulting dark J-V characteristics calculated from the ideal diode Equation 1.1 and the Schottky diode J_0 given by Equation 3.1 is shown by the dashed line in Figure 3.10a. The dark current observed in the PEDOT/Si device is lower by over four orders of magnitude than that expected from a simple Schottky device with the same work-function as the PEDOT:PSS,

supporting the view that the PEDOT/Si heterojunction does not behave as a Schottky junction.

However, Schottky barriers that are obtained in actual devices are in practice never exactly as predicted by the metal work function as in Equation 3.2. If Equation 3.1 is used to calculate the size of the Schottky barrier needed in order to provide the observed J_0 of $3.8 \times 10^{-12}\,\mathrm{A\,cm^{-2}}$ of the PEDOT/Si device, a value of $\phi_B = 1.09\,\mathrm{eV}$ is obtained. This ϕ_B is higher than is realistically obtained for a metal-semiconductor interface, as interface states typically limit the barrier formation to a value *less* than that predicted by Equation 3.2 [77]. This supports the conclusion that a Schottky-junction model is not appropriate for describing the PEDOT/Si heterojunction, and that the PEDOT does provide an electron barrier.

The current-voltage characteristics of the SI/PEDOT:PSS device under AM1.5G illumination are presented in Figure 3.10b. AM1.5G measurements were made using an OAI systems AAA Tri-sol solar simulator equipped with a $4\,\mathrm{mm}\times4\,\mathrm{mm}$ aperture; the solar simulator output was measured using a silicon reference cell (PV Measurements Inc.) that was calibrated using Newport Corporations PV Cell Lab. The sample was put on a vacuum stage to create contact with the backside metal and illuminated measurements are typically taken in less than 5 s to avoid excess heating of the sample.

The solar cell performance parameters are summarized in Table 3.1. An open-circuit voltage is achieved of 570 mV, as well as a short-circuit current-density of $27.7\,\mathrm{mA\,cm^{-2}}$ and a fill factor of 74 %. The open-circuit voltage is in good agreement with that predicted from the J_0 extracted from the dark J-V measurement and Equation 1.3 of 0.587 V. The overall power conversion efficiency of this device was 11.7 %, which is among the best reported for this class of photovoltaic device.

Table 3.1: Performance parameters of PEDOT/Si solar cell

Device	V_{OC}(mV)	J_{SC}(mA cm^{-2})	FF(%)	η(%)
PEDOT/Si Solar cell	570	27.7	74.3	11.7

3.5.2 Current Mechanisms in Silicon/PEDOT Devices

The J-V characteristics of the PEDOT/Si heterojunction support the view that the heterojunction does not act as a simple Schottky junction. However, it is still unclear whether the source of dark current is carried by majority carriers or minority carriers. Majority carrier electrons may contribute to the dark current by thermionic emission over the barrier presented by the LUMO of the PEDOT:PSS, as illustrated in Figure 3.11a. The presence of surface defect states at the interface between the silicon and PEDOT:PSS would facilitate recombination, and electrons reaching the interface will recombine via these states rather than overcome the LUMO barrier. Due to the degenerately doped PEDOT:PSS there are a large number of holes available for the electron to recombine, and this process is shown in Figure 3.11b. It is also possible that the heterojunction serves to reduce electron current to such an extent that the dark current is actually carried by holes being injected from the PEDOT:PSS into the n-type silicon (Figure 3.11c). While each mechanism is possible, only in the case of hole injection is there a stored charge of minority carriers present in the n-type silicon. A stored charge does not form as a result of carrier recombination at the interface, and likewise electrons injected into PEDOT:PSS will immediately recombine [46].

Reverse recovery measurements were used to measure the amount of stored charge in the n-Si formed by injected minority carriers. This measurement has been described in the literature for a variety of p-n junction devices, in the short-base limit [78–80], semi-infinite base limit [79,81,82], and for arbitrary base widths [83–85]. The biasing circuit used for such a measurement is shown in Figure 3.12a. The device under test is placed in series with a bias resistor, and both components are switched between

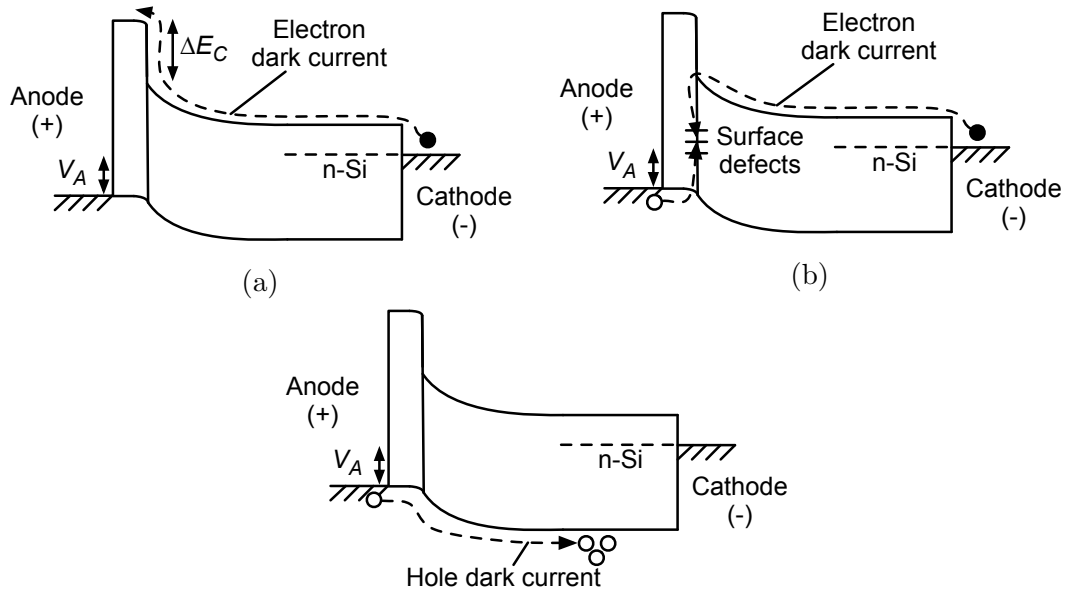


Figure 3.11: Band diagrams showing (A) thermionic emission of electrons over electric field and ΔE_C, (B) electron recombination via surface defects at PEDOT/Si interface, and (C) minority carrier holes being injected into the n-type silicon, and forming a stored charge.

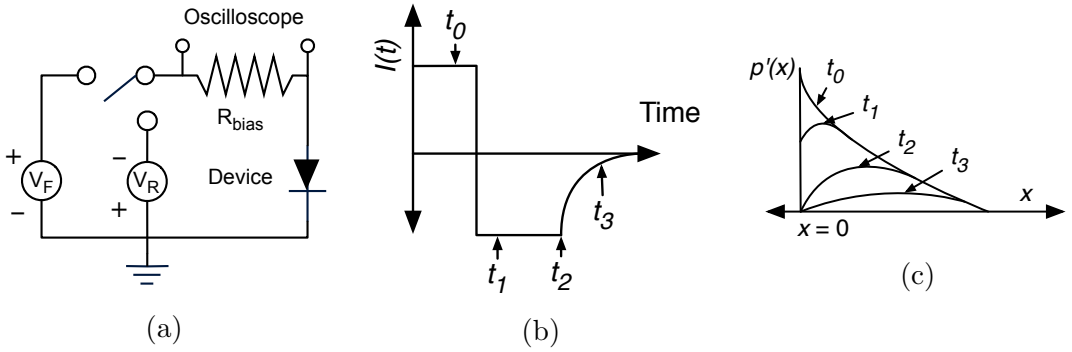


Figure 3.12: (A) Circuit used for the reverse recovery experiment to measure effective injected hole lifetime τ_{bulk} and hole injection ratio α. (B) Device current as a function of time and (C) stored charge behavior at corresponding time points.

a positive applied bias V_F to a reverse bias V_R. The current flowing in the device is known by observing the voltage drop across the bias resistor using an oscilloscope. While the ideal diode equation predicts very little current flow under reverse bias (this current is essentially the reverse leakage current I_0), this does not take into account the transient behavior that occurs as a result of stored minority carriers.

This transient behavior will first be described qualitatively in terms of the device current and minority carrier behavior. The transient behavior of the current in the device vs time is shown schematically in Figure 3.12b. At t_0, the forward bias causes minority carriers to be injected into the n-type silicon, and a steady state population of holes is formed. The profile of minority carrier hole concentration $p'(x)$ at t_0 as a function of distance from the depletion region is shown in Figure 3.12c. When the device is switched to reverse bias at t_1, there is a finite time in which a large reverse current flows through the device. This is caused by the injected hole population diffusing back out through the substrate to the depletion region, and then moving rapidly to the anode, as shown in Figure 3.12c. The voltage across the diode is held relatively constant due to the excess population of holes at the edge of the depletion region in the n-type silicon, and therefore the current is set by the reverse bias and resistor $(V_{diode}-V_R)/R_{bias}$ and is relatively constant until time t_2. At this time the hole concentration at the edge of the depletion region $p'(0)$ reaches the equilibrium value, $p'(0) = p_0$. This is commonly referred to as the 'switching' time or 'storage' time t_{store} of the diode, as it represents the transition point between the diode conducting current in reverse bias and preventing current flow in reverse bias. Past t_2, the voltage across the device drops rapidly and the reverse current begins to decay as the minority carrier profile becomes shallower and the diffusion of holes to the depletion region slows, as indicated by time t_3. Eventually the system reaches steady state in which the excess holes are gone and the reverse current flowing through the diode reduces to the saturation current J_0.

The stored holes in the n-type silicon can be removed via diffusion to the anode as reverse current, but they can also be subject to recombination. The reverse current can be modulated via either the reverse bias voltage source or the bias resistor, and therefore can be used as an experimental parameter. If the reverse current is low, the holes diffuse slowly out of the device and more recombination will take place.

Conversely if the reverse current is high, more holes will be pulled out of the device before recombining. The storage time therefore has a dependence both on the reverse current in the device and the recombination dynamics in the base region of the device.

The relation between t_{store} for a one-sided junction of semi-infinite base width is given by Equation 3.3 [79, 81], in which erf is the error function, τ_{bulk} is the bulk lifetime in the n-type silicon, I_F is the current during the forward bias phase, and α is the proportion of forward current carried by injected holes. As described earlier and shown in Figure 3.11, only injected hole current will contribute to the stored minority carriers in the quasi-neutral region and be measured using reverse recovery, and thus α shows the proportion of the overall current carried by injected holes.

$$\operatorname{erf}\sqrt{\frac{t_{store}}{\tau_{bulk}}} = \frac{1}{1+\frac{I_R}{\alpha I_F}} \tag{3.3}$$

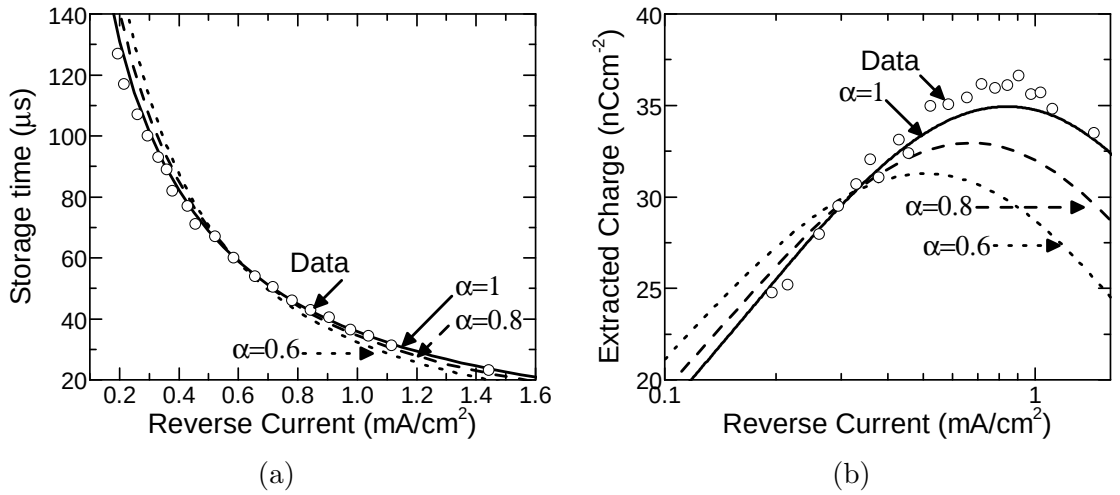
The extracted charge (the stored charge which did not recombine) can be calculated from the product of the reverse current and the storage time of the device, as shown in Equation 3.4.

$$Q_{extracted} = I_R t_{store} \tag{3.4}$$

The extracted charge can be visualized by the area under the curve of $I(t)$ during the recovery period in Figure 3.12b. Combining Equations 3.3 and 3.4 yields Equation 3.5, a direct expression for the extracted charge.

$$Q_{extracted} = I_R \tau_{bulk} \left[\operatorname{erf}^{-1}\left(\frac{1}{1+\frac{I_R}{\alpha I_F}}\right)\right]^2 \tag{3.5}$$

A PEDOT/Si solar cell was measured in the dark using the reverse recovery method with the forward bias current set to $1.33\,\mathrm{mA\,cm^{-2}}$. The storage time was measured at various reverse current levels from $\sim 0.2\,\mathrm{mA\,cm^{-2}}$ to $1.4\,\mathrm{mA\,cm^{-2}}$ and is



(a) (b)

Figure 3.13: (A) Storage time and (B) Extracted charge plotted versus reverse current I_R for a PEDOT/Si device under 1.3 mA cm^{-2} forward bias. Circles represent experimental data; solid and dashed lines are fits of Equations 3.3 and 3.5 for various values of α.

plotted in Figure 3.13a. The extracted charge for the PEDOT/Si device measured via reverse recovery is plotted in Figure 3.13b.

Equations 3.3 and 3.5 are used to fit the measured storage time and extracted charge and extract the minority carrier bulk lifetime. The experimental data were fit for various values of α, and values for τ_{bulk} were obtained from the best fit to the data. The results are shown as solid lines in Figure 3.13a and Figure 3.13b. From these fitted curves it is clear that an α value of 1 provides the best fit to the experimental data.

The extracted values of τ_{bulk} can also be used to calculate a saturation current J_0, to compare to the current-voltage characteristics of the diode. The saturation current for holes being injected into the n-type region (which is what is being measured by reverse recovery) is given by Equation 3.6, where N_D is the n-type silicon doping level in the base region, D_{hole} is the hole diffusion coefficient, and n_i is the intrinsic carrier concentration of silicon.

$$J_{0,holes} = \frac{qn_i^2}{N_D}\sqrt{\frac{D_{hole}}{\tau_{bulk}}} \tag{3.6}$$

The total current in the device is calculated by Equation 3.7.

$$J_{0,total} = \frac{J_{0,holes}}{\alpha} \tag{3.7}$$

Table 3.2: Extracted τ and calculated J_0 from stored charge measurements

α	$\tau_{bulk}(\mu\,\mathrm{sec})$	$J_{0,holes}(\mathrm{mA\,cm^{-2}})$	$J_{total}(\mathrm{mA\,cm^{-2}})$
1	112 ± 1	$(3.60 \pm 0.02) \times 10^{-12}$	$(3.60 \pm 0.02) \times 10^{-12}$
0.9	121 ± 2	$(3.46 \pm 0.03) \times 10^{-12}$	$(3.85 \pm 0.03) \times 10^{-12}$
0.8	132 ± 3	$(3.31 \pm 0.04) \times 10^{-12}$	$(4.14 \pm 0.05) \times 10^{-12}$
0.7	147 ± 5	$(3.14 \pm 0.05) \times 10^{-12}$	$(4.49 \pm 0.08) \times 10^{-12}$
0.6	167 ± 7	$(2.95 \pm 0.06) \times 10^{-12}$	$(4.91 \pm 0.11) \times 10^{-12}$

Table 3.2 summarizes the values obtained from fitting the reverse recovery data. Table 3.2 shows that as α decreases, τ_{bulk} must increase to fit the storage time data. The physical interpretation here is that if the forward bias current due to holes is decreased, then τ_{bulk} must increase in order to account for the observed t_{store}. Furthermore, since lowering α increases τ_{bulk}, then the predicted injected current from holes decreases according to Equation 3.6. We can then calculate using Equations 3.6 and 3.7 the total saturation current flowing in the diode (this assumes the electron current follows an ideal injection behavior, which is valid because the reverse recovery measurements are made in the ideal (n=1) exponential region of the device). The hole current and total current expected is calculated from τ_{bulk} values extracted from the reverse recovery data using various values of α. While the hole current for various values of alpha decreases, the total current predicted in the device increases. We can also calculate the diffusion length for the extracted value of $\tau_{bulk} = 112\,\mu\,\mathrm{sec}$ to be $\sim$340 µm. Since the thickness of the wafers used were 500 µm thick, the modeling could perhaps be improved using a model for arbitrary base widths.

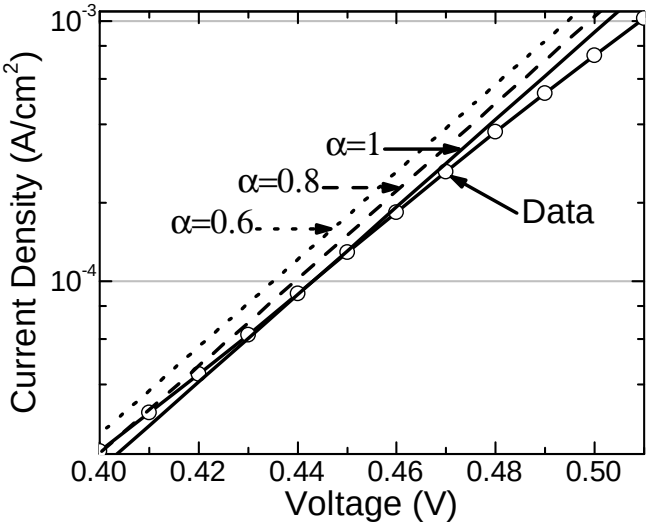


Figure 3.14: Ideal (n=1) exponential region of the current-voltage characteristics of a PEDOT/Si device (data, solid line with hollow circles). This device was measured with reverse recovery in order to estimate τ_{bulk} for various values of α. Equations 3.6 and 3.7 are then used to calculate the total current in the device, as is shown by the solid and dashed lines.

The expected current-voltage characteristics for various values of α in Figure 3.14, along with the actual device measured with reverse recovery. As Figure 3.14 shows, the best match for the dark current is given by $\alpha = 1$, which shows that the dominant current mechanism in the device is due to holes injected from the PEDOT:PSS into the n-type silicon. While the modeling could stand to be improved, the reverse recovery measurements demonstrate that PEDOT:PSS acts as an electron-blocking contact in which dark current is dominated by hole injection into the n-type silicon. As will be shown in the following chapters, this is an essential requirement if adding a complementary hole-blocking heterojunction on the cathode is to reduce dark current.

3.6 Limitations and Future Directions of PEDOT/Si Solar Cells

PEDOT:PSS satisfies many of the requirements for making a low-temperature silicon heterojunction solar cell; however it is not without flaws. First, while PEDOT:PSS performs as a serviceable transparent conductor, its performance is not nearly on-par with Indium Tin Oxide (ITO), the standard for high-performance transparent conductors. Second, PEDOT:PSS also does not act as an ideal anti-reflective coating (ARC) for silicon (For example, the refractive index of an ideal single-layer ARC for silicon at 500 nm would be ∼2.1, while the refractive index of PEDOT at 500 nm is ∼1.4). Third, PEDOT:PSS does not offer any surface passivation at the interface of the silicon. The high work-function of the PEDOT works well to invert the surface of the silicon to create a p^+-n junction and prevent electrons from reaching the interface. However, in order to achieve even higher values of V_{OC}, any surface defects at the PEDOT/Si interface must be passivated to prevent recombination. Finally, PEDOT:PSS has been shown to be very corrosive [86, 87], which is unfavorable for long-term incorporation into a solar cell.

3.6.1 PEDOT:PSS on Planar Silicon

The use of PEDOT:PSS for the top contact in PEDOT/Si solar cells comes with a few trade-offs. This allows the electric field generated by the PEDOT:PSS to be at the silicon surface where most light is absorbed, increasing the likelihood that photogenerated carries become collected. However, this also means that the collected photocurrent must then travel laterally through the PEDOT:PSS film in order to reach a busbar, creating ohmic losses. The problem of ohmic losses cannot be simply fixed by using thicker PEDOT:PSS, because thick films absorb significant amounts of the incident radiation. One solution could involve using an ITO film on top of

the PEDOT, but this would complicate processing. Furthermore, the PEDOT:PSS refractive index ranges between 1.3 to 1.6, which is not ideal for a single layer ARC for silicon.

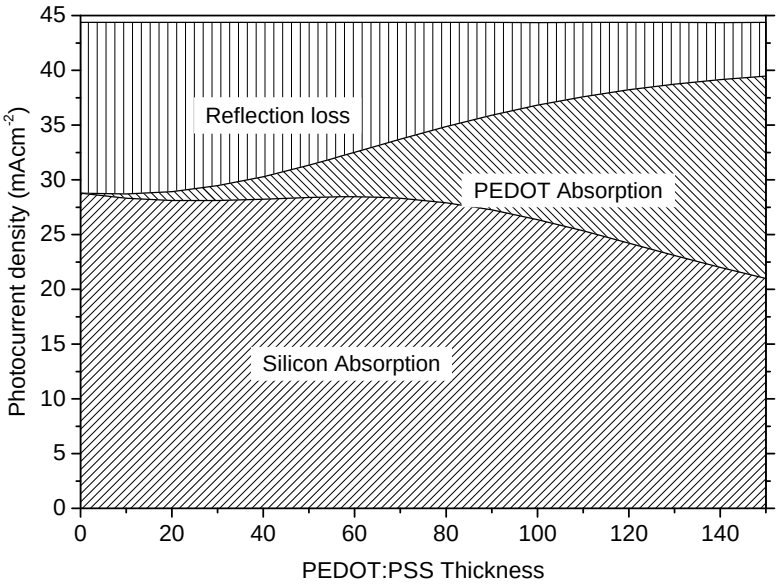


Figure 3.15: Short-circuit current losses from absorption and reflection as a function of PEDOT:PSS thickness for planar silicon substrate (modeled with OPAL 2 [88]).

The optical losses due from absorption or reflection from PEDOT on a planar silicon substrate were modeled as a function of the PEDOT thickness, and is shown in Figure 3.15. The modeling was carried out using the OPAL2 simulation software [88–94]. The best case short-circuit current predicted is only $28.5\,\mathrm{mA\,cm^{-2}}$, and this occurs at a film thickness of 60 nm. At such film thicknesses, the sheet resistance of the PEDOT:PSS is on the order of several hundred $\Omega/\square$. A lower resistance sheet resistance is desired in order to reduce the area that must be covered by the low-resistance metal grid. This would help minimize short-circuit current loss due to shading from the metal grid fingers.

3.6.2 PEDOT:PSS on textured Silicon

As discussed in Chapter 1, surface texturing is a commonly employed method for decreasing optical losses in a solar cell. The effect of using PEDOT:PSS on a randomly pyramidal textured wafer from anisotropic etching is shown in Figure 3.16, as modeled using the OPAL 2 software. The modeling is achieved via computational ray tracing, where the pyramid height is uniformly distributed between 5 µm to 10 µm, as described by [90]. First, it is clear that the amount of light lost to reflection for a textured sample is significantly lower (by roughy 10 mA cm^{-2}) than was shown for a planar silicon substrate in Figure 3.15. However, also shown is the amount of short-circuit current lost due to absorption in the PEDOT:PSS, which becomes very significant with thicker PEDOT:PSS layers.

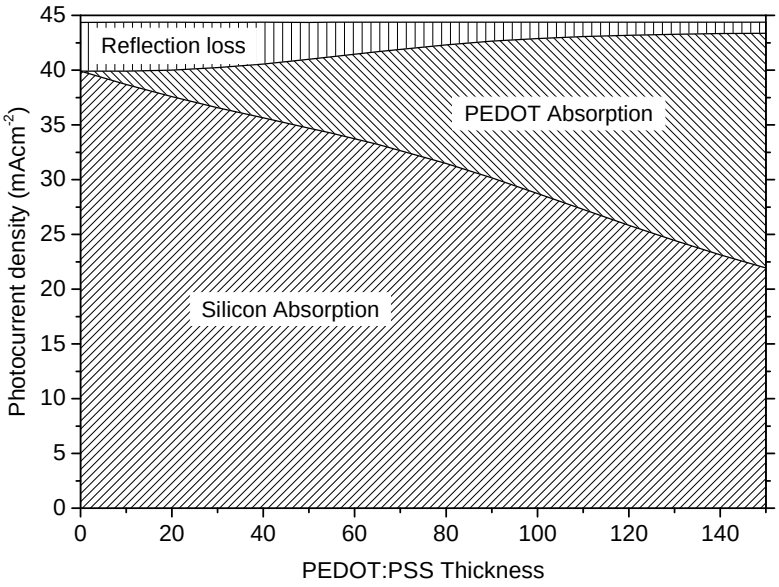


Figure 3.16: Short-circuit current losses from absorption and reflection as a function of PEDOT:PSS thickness for randomly pyramidal textured silicon substrate (modeled with OPAL 2 [88]).

The optical modeling is promising because it shows that PEDOT:PSS on textured substrates can offer better light absorption in the silicon. However, this is only ac-

complished by making the PEDOT:PSS layer as thin as possible. Unfortunately, as previously discussed, this is a non-ideal situation because thinning the PEDOT:PSS increases the lateral resistance of the layer. On a textured surface the lateral resistance plays an even bigger role, because current traveling laterally must travel up and down the pyramidal structures. The effective path length that the current must travel is increased by a factor of 1.7 due to this effect. One potential solution is to simply thin the PEDOT:PSS film as much as possible, and use another transparent conductor to carry the bulk of the current laterally. This will be presented in Chapter 6.

3.6.3 PEDOT/Si Interface recombination

For the PEDOT:PSS to be even more effective as a selective contact, any surface recombination at the interface must be reduced. Figure 3.17a presents an illustration of how surface defects may allow electrons in the n-type substrate to recombine at the PEDOT/Si interface. Admittedly, the data presented in section 3.5.2 suggest that the dominant dark current mechanism in the PEDOT/Si device is not surface recombination. However, if a high quality BSF field is implemented to block the dark current flowing due to hole injection into the n-type base region (as will be discussed in Chapter 5), then PEDOT/Si surface recombination may be the limiting factor in the device performance.

One approach to passivate the PEDOT/Si interface is to utilize a passivating tunnel oxide, as shown in Figure 3.17b. The oxide serves to passivate the dangling bonds at the surface of the silicon, yet must simultaneously be thin enough to allow current to pass via tunneling. The simplest approach to forming a thin oxide layer is to allow a native oxide to grow on the silicon surface. The use of native silicon oxide has been shown to improve the open-circuit voltage performance of PEDOT/Si devices significantly [95]. Native silicon oxide is attractive due to the simplicity of

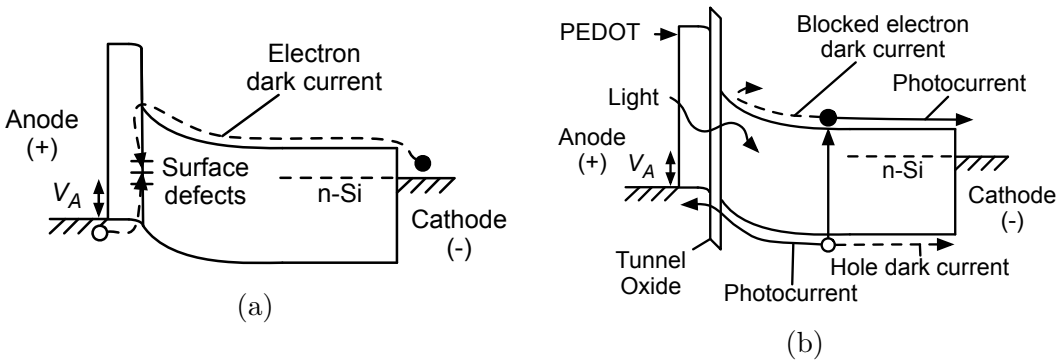


Figure 3.17: Band diagrams showing PEDOT/Si solar cell with (A) electron recombination via surface defects at PEDOT/Si interface, and (B) with a thin tunneling oxide for silicon surface passivation.

ambient air exposure and the self-limiting nature of growth. However, as will be shown, the native oxide films can be observed to cause poor fill factor due to the blockage of current flow through the oxide.

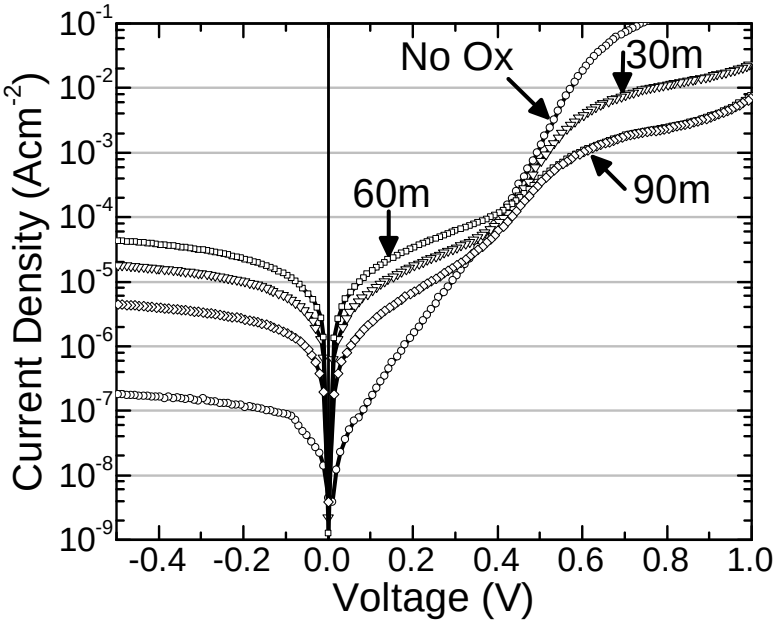


Figure 3.18: Current-density vs voltage characteristics in the dark of PEDOT/Si solar cells with interfacial native oxide grown for 0, 30, 60 and 90 minutes in laboratory ambient.

Figure 3.18 shows the dark current characteristics of PEDOT/Si solar cells with native oxide interfacial layers grown under laboratory ambient at room temperature.

The devices followed the same fabrication procedure as discussed in section 3.2, but after sample cleaning and HF acid etch the samples were allowed to grow native oxide for 0, 30, 60 and 90 minutes before spin-coating with PEDOT:PSS. The dark current characteristics show that even for just 30 min left in ambient air, the resulting native oxide is presents a significant tunneling barrier to current flow in forward bias. This results in a voltage drop beginning at relatively low current levels of $\sim$1 mA cm^{-2}. A longer oxidation time of 60 min results in an even greater tunnel barrier, as the forward current is reduced even further. The oxide growth then seems to saturate, as 90 min in ambient is not observed to add significantly to the tunnel barrier thickness compared to the 60 min device.

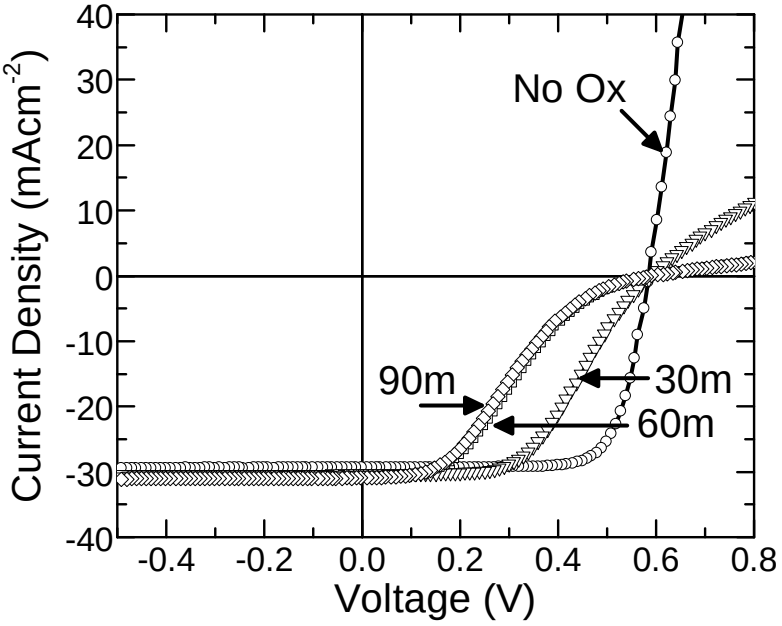


Figure 3.19: Current-density vs voltage characteristics under AM1.5G illlumination of PEDOT/Si solar cells with interfacial native oxide grown for 0, 30, 60 and 90 minutes in laboratory ambient.

The barrier has a clearly negative effect on the fill factor of the solar cells, as is apparent in the J-V characteristics under illumination (Figure 3.19). The presence of the native oxide creates a barrier to the passage of photocurrent from the silicon to the PEDOT:PSS, which results in the 's'-shape of the J-V curve. The ultimate

result is a very poor fill factor and low solar cell efficiency, as shown by the solar cell parameters, summarized in Table 3.3. While there is a small increase in the observed open-circuit voltage for the oxidized solar cells, the thickness of the native oxide layer must be much thinner to facilitate conduction and good solar cell efficiency.

Table 3.3: Performance parameters of PEDOT/Si solar cells with native SiO_2

Front surface passivation	V_{OC}(mV)	J_{SC}*(mA cm^{-2})	FF(%)	η*(%)
PEDOT:PSS only	586 ± 4	29.6 ± 0.2	76.0 ± 0.4	13.2 ± 0.2
30 min Native SiO_x	589 ± 3	30.2 ± 0.4	52.4 ± 1.8	9.3 ± 0.2
60 min Native SiO_x	591 ± 3	30.8 ± 0.1	33.9 ± 3.2	6.2 ± 0.6
90 min Native SiO_x	591 ± 1	30.8 ± 0.2	29.5 ± 3.8	5.4 ± 0.7
**Not AM1.5G Illumination*				

Despite the experimental data shown here, groups have been able to show good performance using native oxides grown by ambient conditions, albeit with different PEDOT mixtures. These Si/SiO_x/PEDOT:PSS heterojunctions show very good passivation as measured by contactless PCD measurements. The studies have shown that a planar c-Si/SiO_x/PEDOT:PSS (Clevious F HC Solar) interface has a dark current J_0 contribution of just (80 ± 3) fA cm^{-2}, which implies a V_{OC} of 692 mV [96]. While such results differ from those presented here in their approach to device structure, surface treatment, and sources for PEDOT:PSS material, they nonetheless that the PEDOT/Si heterojunction may be able to overcome some of its limitations by utilizing tunnel oxides. A more controlled approach towards the humidity of the laboratory ambient may allow reproduction of the more encouraging results.

Chapter 4

Growth and Properties of Silicon/TiO_2 Heterojunctions

4.1 Introduction

Titanium dioxide is a transition metal oxide that is a widely used both commercially and in research settings. TiO_2 commonly occurs in the anatase and rutile crystalline phases, which have bandgaps of 3.2 eV and 3.0 eV, respectively [32]. The material is typically n-type due to oxygen vacancies and has a relatively high refractive index (2.49 for anatase and 2.9 for rutile [34]). Due to the optical properties of TiO_2, it has found wide use as a pigment additive for paints, as a coating for optical components, and as a ultraviolet light absorber for sunscreens. Toxicology has been studied, and TiO_2, even in nanoparticulate form, is considered safe for such usages [97].

The properties of titanium dioxide have also made it a subject of intense research as a photocatalyst. TiO_2 gained significant interest after being shown to facilitate water splitting [98], and since has been used to create surfaces that demonstrate self-cleaning and photoinduced hydrophilicity [99,100]. A large body of work has focused on using TiO_2 for photo-assisted degradation of organic molecules [34].

Additionally, the electronic and optical properties of TiO_2 films have led to its use in various photovoltaic applications. For organic solar cells, TiO_2 has proven effective as an electron-selective contact due to the alignment of the valence band with the LUMO level of [6,6]-phenyl C61 butyric acid methyl ester ($PC_{61}BM$) (a commonly used acceptor material used in bulk heterojunction cells) [101, 102]. The effectiveness of the use of TiO_2 and PEDOT:PSS as electron and hole-selective contacts in a poly[N-9"-hepta-decanyl-2,7-carbazole-alt-5,5-(4',7'-di-2-thienyl-2',1',3'-benzothiadiazole) (PCDTBT) and $PC_{70}BM$ bulk heterojunction cell led to an internal quantum efficiency nearing 100 % [103]. Mesoporous TiO_2 films have also been used as a substrate and hole-blocking contact for perovskite solar cells [104].

TiO_2 films can be deposited via a large variety of fabrication methods, many of which have been demonstrated on silicon substrates. Such methods include Atomic Layer Deposition (ALD) [105–118], Metal-Organic Chemical Vapor Deposition (MOCVD) [102, 119–123], Plasma-Enhanced Chemical Vapor Deposition (PECVD) [124–128], Pulsed-Laser Deposition (PLD) [129, 130], sol-gel [131–133], and sputtering [134–138].

In this work, the main interest in TiO_2 is to form a Si/TiO_2 heterojunction that can be used as a back-surface field in silicon solar cell. Such a heterojunction would act as a complementary selective contact to the PEDOT/Si heterojunction described in the previous chapter. Section 4.2 presents the deposition process used in this work to obtain thin films of TiO_2. The requirements for such a selective heterojunction to be useful in a photovoltaic device, as outlined in Chapter 2, are excellent surface passivation combined with the correct band alignments. Sections 4.3 and 4.4 present how the Si/TiO_2 heterojunction meets these requirements. Section 4.5 presents the fabrication of p-type Si/TiO_2 diodes to study the effects of metalization and annealing on the TiO_2 films.

4.2 Titanium Dioxide Growth Method

The TiO_2 in this work was deposited by a novel low-temperature Chemical Vapor Deposition (CVD) process [39]. It is fundamentally different from ALD processes; because the precursor molecule contains a Ti atom already bonded to four oxygens, thus there is no need for water vapor to oxidize the metal. The metal-organic precursor used was titanium(IV) tetra-(*tert*-butoxide) or $Ti[OC(CH_3)_3]_4$, which is shown in Figure 4.1. The process also differs because of the relatively low-temperatures used; the maximum temperature reached is 80 °C to 100 °C, in contrast to conventional CVD of TiO_2 which can reach 275 °C to 675 °C [119, 121–123] . This process achieves ultra-thin, conformal films of TiO_2 on the order of 1 nm to 4 nm thick.

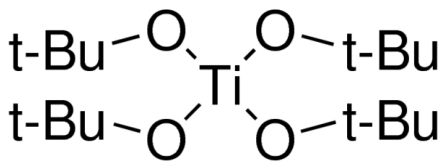


Figure 4.1: Titanium tetra-(*tert*-butoxide) precursor molecule

Overall, the TiO_2 deposition system is very simple and involves a minimal number of components, as illustrated in Figure 4.2a. The main chamber contains a stage with a thermoelectric device for heating and cooling. A mechanical roughing pump is connected to one end of the chamber. On the other end, a valve connects the chamber to a vial of the precursor liquid. The main chamber also has a nitrogen inlet for venting purposes and a window for observation of samples during depositions.

The fabrication sequence begins with cleaning of an electronic-grade, polished silicon sample. The cleaning process is the same as described in Chapter 3, and involves a solvent cleaning procedure and an RCA clean. Immediately before entering the TiO_2 deposition chamber, a dip in 20:1 H_2O:HF acid for 1 minute is performed to remove any oxides and form a hydrogen-terminated silicon surface [63]. After

samples are placed in the chamber, it is pumped down to a base pressure of 20 mtorr to 50 mtorr and the chamber remains pumped for the remainder of the deposition.

The process that takes place within the chamber is illustrated in Figure 4.2b. The samples are first cooled by the thermoelectric stage to $-10\,^{\circ}\mathrm{C}$, and the samples are then exposed to vapor from the precursor vial. The standard length of the adsorption step used is 10 min. The cooling of the sample stage facilitates adsorption of a thin layer of Ti-alkoxide on the samples. Because the precursor adsorbs on the stage as well, a thin layer of precursor also wicks underneath the samples, so that adsorption occurs on both sides of the sample. The growth process is not performed one atomic layer at a time, in contrast to ALD, because more than one monolayer of the alkoxide is adsorbed onto the sample during the cooling step.

After adsorption, the samples are heated to $100\,^{\circ}\mathrm{C}$ for 10 min in order to thermolyze the alkoxide. The thermolysis step serves to break the iso-butene from the titanium, leaving hydroxyl groups that condense to give a stoichiometric TiO_2 film with elimination of water. Because the alkoxide adsorbs to both surfaces of the sample (top and bottom), TiO_2 is obtained on both surfaces. The adsorption and thermolysis steps comprise one cycle, and a standard deposition uses three cycles, which results in a film thickness of 2 nm to 3 nm. The TiO_2 films is thought to be amorphous, due to the lack of any visible grain boundaries in tapping-mode atomic force microscopy phase images. It is possible that the TiO_2 forms a polycrystalline structure that is not detectable via these measurements. Modifications of this growth process that where used to obtain thicker TiO_2 films are discussed in the following chapter, in Section 5.4.1.

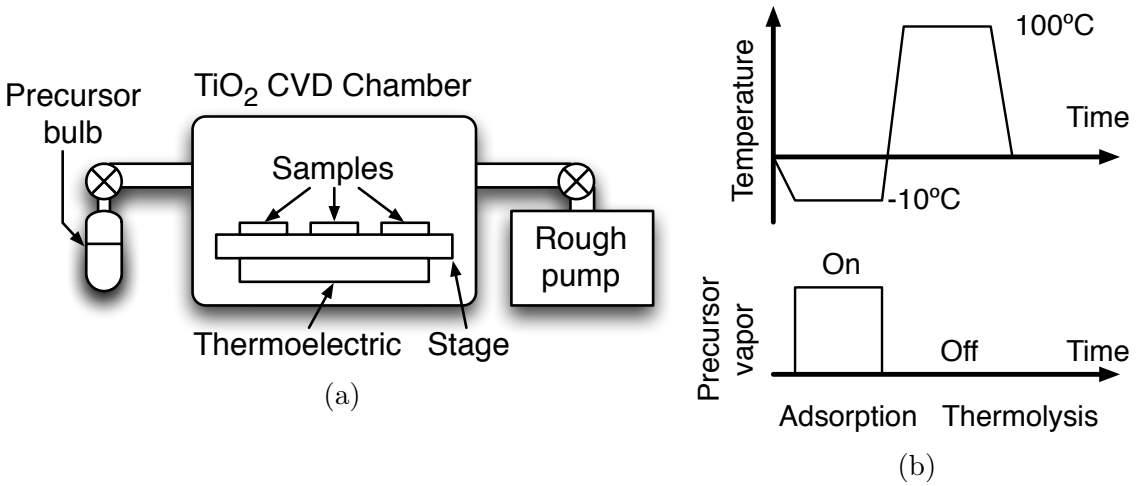


Figure 4.2: Illustration of (A) TiO_2 deposition chamber and (B) temperature and precursor setting for one cycle.

4.3 Si/TiO_2 Band Alignments

The electronic states of the titanium dioxide were characterized using photoemission spectroscopy techniques. As presented in Chapter 3 for PEDOT:PSS, UPS was utilized to extract the work function of the material as well as the location of the valence band edge, and IPES was utilized in order to measure the location of the conduction band. Additionally, since the TiO_2 thin films are less than 10 nm, XPS can probe the silicon 2p core levels levels underneath the TiO_2. This provides an insight into the silicon band bending (S_{BB}) that occurs at the TiO_2 heterojunction.

The spectroscopy measurements were performed on samples which received standard 3-cycle depositions and were measured either as-deposited or after 250 °C annealing in N_2. The XPS data show the that composition of the thin films is stoichiometric TiO_2, similar to the thin films described in previous work [39]. The UPS, IPES, and XPS were performed by Gabriel Man, and the detailed data will be included in a forthcoming publication. A summary of the data obtained from the spectroscopy measurements is presented in Table 4.1, and an illustration of the band alignments and offsets at the Si/TiO_2 interface is presented in Figure 4.3.

Table 4.1: Summary of Si/TiO_2 spectroscopy measurements

TiO_2 on n^+ silicon	E_G (eV)	ΔE_C(eV)	ΔE_V (eV)	Si_{BB} (eV)
As-deposited	3.4 ± 0.3	0.1 ± 0.2	2.0 ± 0.1	0.40 ± 0.05
250 °C Anneal in N_2	3.4 ± 0.3	0.1 ± 0.2	2.0 ± 0.1	0.40 ± 0.05
Room-temperature Anneal in N_2	3.2 ± 0.3	0.2 ± 0.2	1.9 ± 0.1	0.27 ± 0.05

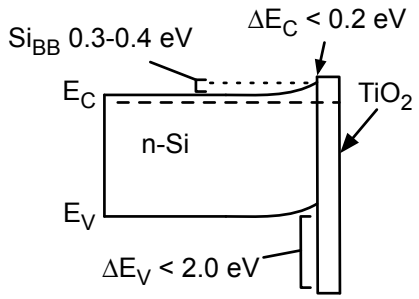


Figure 4.3: Band offsets and band-bending at Si/TiO_2 Heterojunction as measured by photoemission spectroscopy (not drawn to scale)

4.4 Passivation of Silicon with TiO_2

As described in section 2.2.2, an effective heterojunction must passivate any dangling bonds at the surface of the crystalline silicon that act as recombination centers. The passivation of these defects at the surfaces of crystalline silicon has been demonstrated with titanium oxide deposited by various methods. In particular, PLD [130, 139], APCVD [140], sol-gel [141], and ALD [117,142] methods were demonstrated to achieve surface passivation with varying degrees of success. Of particular note are the efforts of Liao et. al, who used a low-temperature ALD process to achieve extremely low SRVs on both n-type and p-type silicon wafers (2.8 cm/ sec and 8.3 cm/ sec, respectively) [117].

The low-temperature CVD TiO_2 used in this work was also shown to achieve excellent surface passivation of crystalline silicon. The size of the samples used for lifetime measurements were 25 mm×25 mm or larger for good inductive coupling with

the QSSPCD measurement system (Section 2.2.2). The substrates used for lifetime measurements, unless otherwise specified, were 3 Ω cm phosphorus doped, double-side polished < 100 > float-zone (FZ) silicon wafers. The bulk lifetime is estimated to be >1 ms based on the highest measurements of lifetimes on these substrates with thermal oxide passivation layers. The τ_{eff} was measured using the QSSPCD method and the S_{eff} calculated according to the geometry of the individual sample (depending on if the surface passivation being studied was on one side or both).

The quality of the c-Si surface passivation was observed to depend greatly on the treatment of the TiO_2 film. 'As-deposited' films refer to those measured just after the deposition process and thermolysis described in Section 4.2. The passivation quality of as deposited films was observed to vary, with S_{eff} ranging from 550 cm/ sec to 900 cm/ sec.

Various post-treatment methods have been shown to enhance the passivation of the TiO_2 films. Annealing the Si/TiO_2 at 250 °C for 2 minutes in nitrogen using a Rapid Thermal Annealer (RTA) was observed to lower the SRV to ∼50 cm/ sec to 150 cm/ sec. The work of Liao et. al, although using a different deposition method, also employed an anneal of 200 °C to 250 °C in nitrogen [117]. The passivation of the low-temperature CVD films used in this work after 250 °C anneal in nitrogen has been shown to be stable for several months [143].

The TiO_2 films are also observed to achieve outstanding passivation of c-Si without heating to 250 °C. A 'room temperature anneal', in which samples are left in a

Table 4.2: Summary of Si/TiO_2 surface passivation

TiO_2 on n-type silicon	SRV (cm/ sec)
As-deposited	>500
250 °C Anneal in N_2	50-150
Room-Temperature Anneal in N_2	20-100

nitrogen filled glovebox environment for several hours, was utilized as an alternative to the 250 °C anneal. This process is observed to provide very low values of SRV, in the range of 20 cm/ sec to 100 cm/ sec. A summary of the SRVs achieved by these methods is shown in Table 4.2.

4.5 Titanium Dioxide Diodes on p-type Silicon

The band alignment data that were presented in Chapter 4.3 agree with previous work by Avasthi et al. which showed TiO_2 acts as a hole-blocking contact to silicon [39]. In this previous work, Schottky diodes were fabricated using aluminum deposited on p-type silicon. This device was observed to have a relatively low Schottky barrier, which allowed holes to flow from the p-type silicon to the aluminum. It was also shown that incorporating TiO_2 (aluminum/TiO_2/p-Si) blocked the majority carrier holes from flowing from the p-type silicon to the aluminum, resulting in an improved, rectifying p-type diode. Similar devices on n-type silicon were fabricated (aluminum/TiO_2/n-Si) to demonstrate that no conduction band barrier was present and electrons can flow through the TiO_2 easily to reach the aluminum. The band diagrams of these devices are shown in Figure 4.4 and the current-voltage data from such devices are shown in Figure 4.5.

Since p-Si/TiO_2 diodes demonstrate the hole-blocking behavior of the Si/TiO_2 interface, such devices can provide a useful indicator of the quality of the TiO_2 films obtained. This proved useful experimentally when developing the process methods used to obtain high-quality TiO_2 films for use in the solar cells discussed in Chapter 5. The quality of the p-type diodes obtained were observed to vary with the metalization and post-processing performed. Specifically, the evaporator used for aluminum deposition was observed to have a great effect on the p-Si J_0 obtained. The annealing

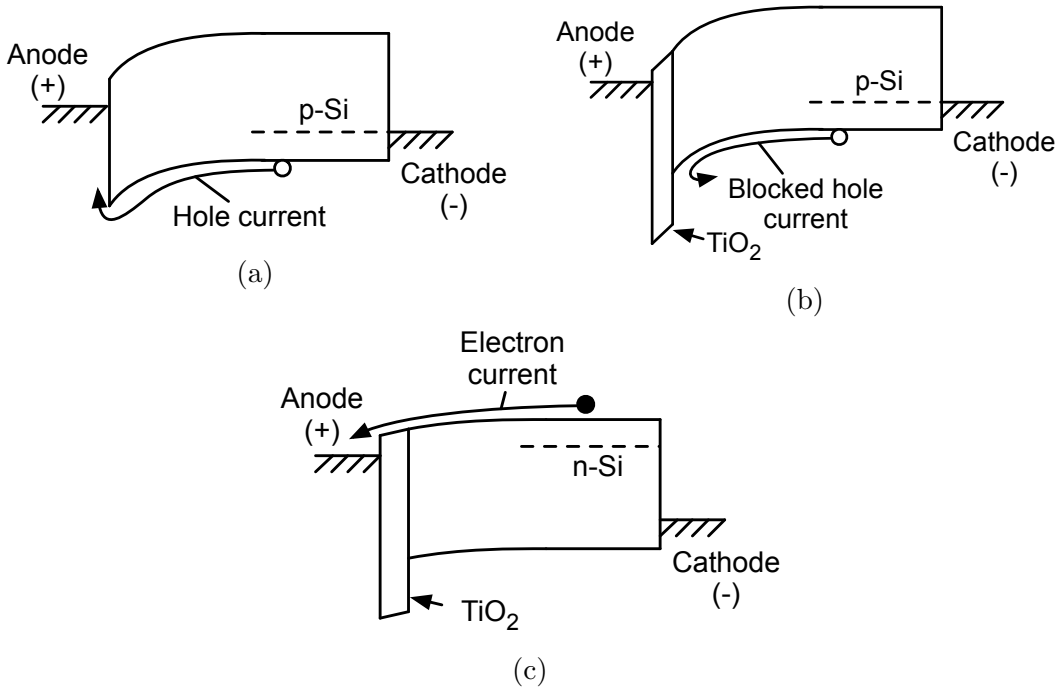


Figure 4.4: Band diagrams showing (A) p-type Schottky diode and hole dark-current (B) p-type diode with TiO_2 hole blocker to reduce majority carrier hole current and (C) TiO_2 heterojunction forming an ohmic contact on n-type silicon.

process described in Section 4.4 was also observed to result in poorer p-type diodes with higher J_0 values.

4.5.1 Evaporator Effects

Figure 4.6 shows two Al/TiO_2/p-Si diodes which received Al using different thermal evaporators (Evaporator 1 is an Edwards 306 system, Evaporator 2 is an Ångstrom Engineering system. Both use a filament to directly heat the aluminum). The data from these devices clearly show that the diode that received Al in Evaporator 1 offers a much higher rectification ratio and lower J_0. The J_0 and ideality factor were extracted by fitting ideal diode equation to the semi-log current-voltage data at the point of greatest slope, as shown in the figure. The $\log_{10}(J_0)$ is then used to give an indication of the quality of the diode and is used for comparison of different device batches.

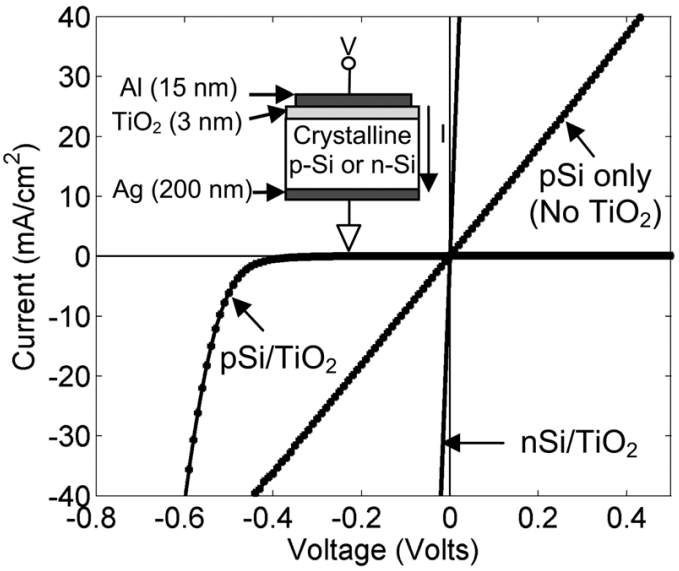


Figure 4.5: Current-voltage measurements of Al/p-Si, Al/TiO_2/p-Si and Al/TiO_2/n-Si devices. Voltage bias (x-axis) is applied to the top metal contact with respect to the bottom metal contact. Reproduced with permission [39]

The $\log_{10}(J_0)$ data from a sample with 16 Al/TiO_2/p-Si diodes processed in Evaporator 1 is compared to 16 devices which were processed in Evaporator 2 in Figure 4.7. Clearly the devices which received Al from Evaporator 1 have significantly lower J_0 values. The base pressures of the two evaporators are comparable, so it is hypothesized that differences in heating of the sample during the evaporation may account for the difference in device quality. Another hypothesis is that the diode quality depends on the evaporation rate of the aluminum, which is significantly different in the two evaporation systems (1 nm/ sec to 3 nm/ sec in Evaporator 1 vs 0.1 Å/ sec to 0.5 Å/ sec in Evaporator 2) due to different distances between the source and substrate. While neither of these hypotheses have been confirmed, the information proved nonetheless very valuable in achieving the devices discussed in Chapter 5.

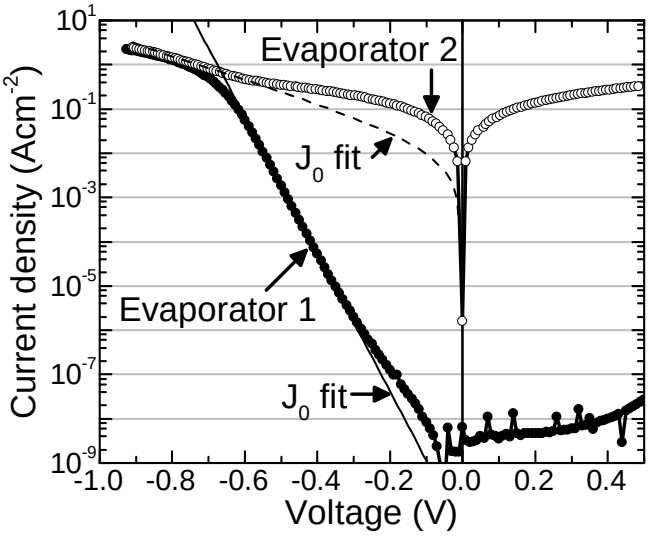


Figure 4.6: Semi-log plot of current density versus voltage characteristics for two p-type diodes from metalized in different evaporators. Circles represent data, while solid and dashed lines are fitted to the point of highest slope on the curve to extract J_0 values.

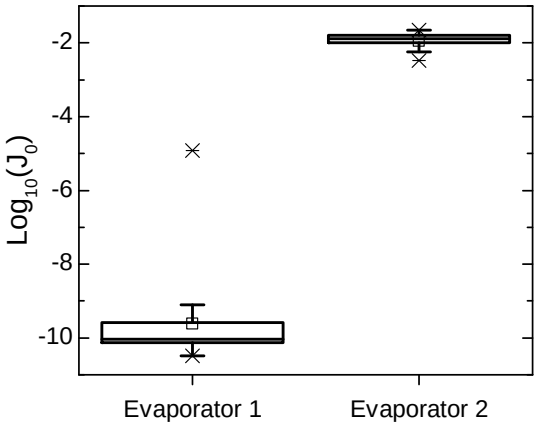


Figure 4.7: Comparison of the log(J0) of p-Si/TiO_2 diodes fabricated in Edwards thermal evaporator (1) versus Ångstrom thermal evaporator (2).

4.5.2 Annealing Effects

Fabrication of Al/TiO_2/p-Si diodes also offered some insight into the effects of annealing on device behavior. As discussed in section 4.4, annealing for 2 min in 250 °C nitrogen ambient was observed to provide low SRVs for Si/TiO_2 interfaces without

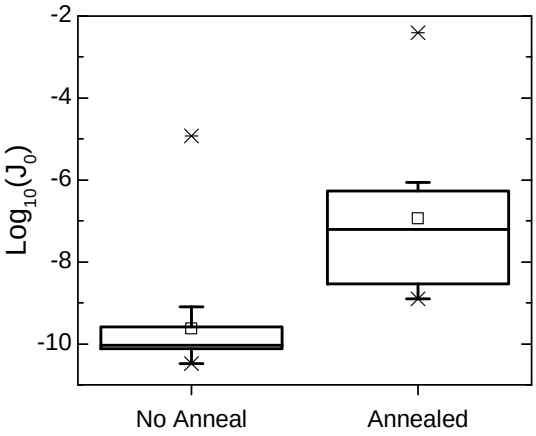


Figure 4.8: Comparison of the $\log(J_0)$ of p-Si/TiO_2 diodes with and without 2 min anneal in 250 °C nitrogen ambient. Aluminum metal for top contact was deposited using Evaporator 1.

any other layer (such as aluminum metal) deposited on top of the TiO_2. These results would lead one to expect better hole-blocking performance as a result of the low SRV from annealing. However, the J_0 of Al/TiO_2/p-Si diodes made with annealed TiO_2 films was significantly higher than those of devices which did not receive annealing, as shown in Figure 4.8. Note that the TiO_2 films in these devices were all deposited in the same standard 3-cycle deposition.

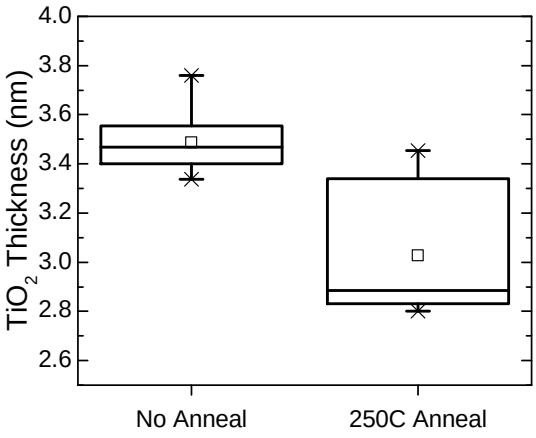


Figure 4.9: Comparison of the thickness of TiO_2 films with and without 2 min anneal in 250 °C nitrogen ambient as measured by ellipsometry.

Further investigation of the TiO_2 films revealed that a significant thickness decrease occurred after annealing of the films. Figure 4.9 shows a comparison of TiO_2 thickness for films deposited in the same run, with and without annealing. The data show that the thickness of the unannealed films is on average 0.6 nm thinner than those which did not receive an anneal. The Al/TiO_2/p-Si diode data show that annealed TiO_2 films, despite providing good surface passivation, make poor devices when metalized and incorporated into actual devices. The effect of thin TiO_2 films will be discussed further in the context of double-sided solar cells in Chapter 5.