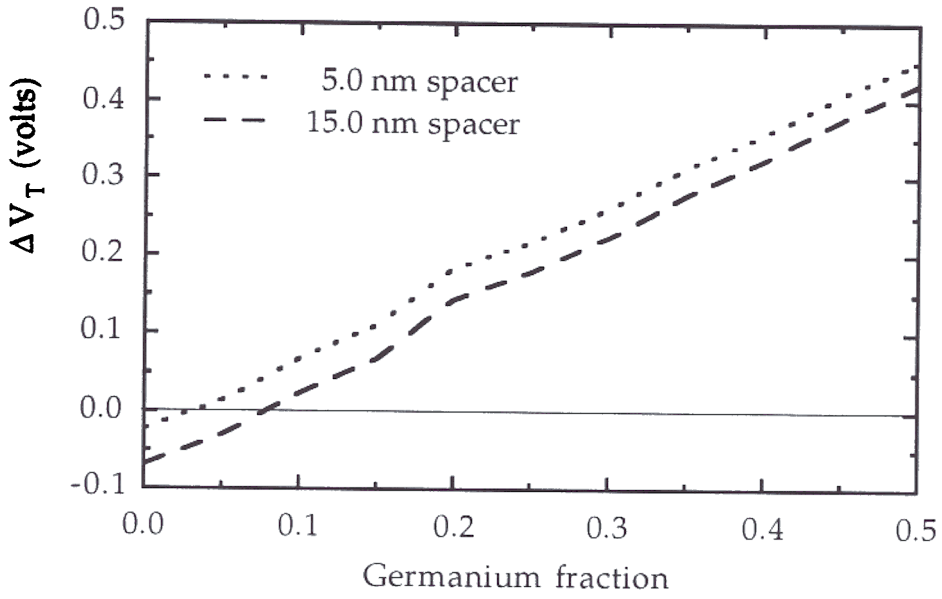


Figure 3.11 Simulated threshold voltage shift vs germanium fraction compared to a silicon MOSFET. A negative threshold shift means the $Ge_xSi_{1-x}$ well does not form an inversion layer. Calculations for devices with a uniform doping of $N_D = 10^{16}$ cm$^{-3}$.

| Spacer Width (nm) | Ge Fraction | $\Delta E_v$ (eV) | Threshold Shift (V) | | |
|---|---|---|---|---|---|
| | | | Poisson Solver | Analytic Model | Experiment |
| 5.0 | 0.1 | 0.08 | 0.04 | 0.07 | – |
| 7.5 | 0.1 | 0.08 | 0.04 | 0.06 | – |
| 10.5 | 0.1 | 0.08 | 0.04 | 0.04 | – |
| 5.0 | 0.2 | 0.16 | 0.15 | 0.19 | – |
| 7.5 | 0.2 | 0.16 | 0.15 | 0.18 | 0.17 |
| 10.5 | 0.2 | 0.16 | 0.14 | 0.17 | – |
| 5.0 | 0.3 | 0.25 | 0.24 | 0.29 | – |
| 7.5 | 0.3 | 0.25 | 0.23 | 0.28 | – |
| 10.5 | 0.3 | 0.25 | 0.21 | 0.27 | 0.43 |

Table 3. 2 Comparison of the threshold shift expected from simulation, analytic model and experimental devices. All used devices with 12.5 nm gate oxides and were doped uniformly at $N_D = 10^{16}$ cm$^{-3}$.

simulation – $V_T$(Si device) = -1.0 V experiment – $V_T$(Si device) = -1.7 V

conductance curves of actual devices. The devices all had a 12.5 nm gate oxide, uniform n-type doping of $10^{16}$ $cm^{-3}$, and varying germanium fractions and spacer thicknesses. The experimental devices were compared to an epitaxial silicon control device which had a threshold voltage of - .72 V. Details regarding the experimental devices are found in section 3.3.

The agreement between threshold shift calculated by the analytic model and the threshold shift from the simulation is good. The agreement of the analytic model with experiment is good for sample 646 which has a 7.5 nm spacer and a $Ge_{.2}Si_{.8}$ well (0.18 V model/ 0.17 V device), but the threshold shift of 649 which has a 10.5 nm spacer and a $Ge_{.3}Si_{.7}$ well is a good deal larger than expected from the model (0.27 model/ 0.43 device). Similar trends in the threshold shift have been seen by Subbanna et al[10]

### 3.2.6 Subthreshold Swing

A MOSFET acts like a bipolar transistor in the subthreshold regime with the drain current being exponentially dependent on the surface potential ($I_D \propto \exp(q\phi_s/kT)$ and independent of the drain voltage when $V_d > 3kT/q$ [11] The subthreshold slope is indicative of the sharpness of the on/off transition when a MOSFET is used as a switch as in digital logic. If interface states are not important, control of the surface potential is through the capacitive divider which consists of the series combination of the oxide capacitance ($C_{ox}$) and the depletion capacitance ($C_{dep}$). Thus the ideality factor $n = (C_{ox} + C_{dep})/C_{ox}$ is introduced into the drain current dependence on gate voltage :

Eq. 3.12
$$I_D \propto \exp\left(\frac{q\phi_s}{kT}\right) = \exp\left(\frac{V_G}{nkT}\right.$$

The subthreshold swing is defined as the change in gate voltage necessary to change the drain current by one decade and is simply

**Eq. 3.13**
$$S = \frac{kT}{q}\ln(10)\left( + \frac{C_{dep}}{C_{ox}}\right)$$

In a MOS-HHMT the capacitive coupling of interest in the subthreshold region is of the gate potential to the potential at the $Ge_xSi_{1-x}$/Si interface rather than to the Si/$SiO_2$ interface. Thus the oxide capacitance should be replaced with the series combination of the oxide and spacer layer capacitance:

Eq.3.14
$$C_{ox} \rightarrow \frac{(C_{ox})(C_{SP})}{C_{ox} + C_{SP}}$$

In a silicon device the depletion capacitance is equal to the dielectric constant ($\varepsilon_{Si}$) divided by the maximum depletion width

Eq.3.15
$$C_{dep}(Si) \sqrt{\frac{q\varepsilon_{Si}N_D}{2(2\phi_F)}}$$

The depletion capacitance for the MOSHHMT is increased since the potential at the onset of inversion in the $Ge_xSi_{1-x}$ well is now reduced to ($2\phi_F - \Delta E_v$) as discussed in section 3.2.5

With these modifications the subthreshold swing becomes:

Eq. 3.16
$$S = \frac{kT}{q}\ln(10) \times \left( 1 + \frac{\left(1 + \frac{C_{ox}}{C_{sp}}\right)}{\left(1 - \frac{\Delta E_V}{q2\phi_B}\right)^{\frac{1}{2}}} \times \frac{C_{dep}(Si)}{C_{ox}} \right)$$

Both increasing the depletion capacitance (lowering the potential at threshold to ($2\phi_F - \Delta E_v$)) and reducing the gate capacitance (adding the additional series capacitance of the spacer layer) serve to weaken the

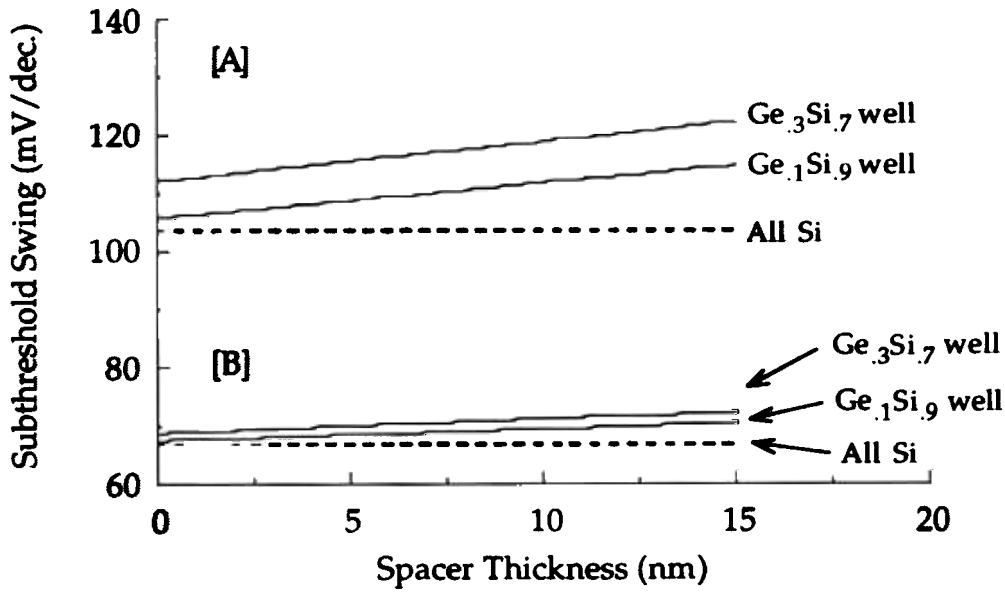


Figure 3.12 Subthreshold swing as calculated using Eq. 3.16 for two different combinations of gate oxide thickness and donor density:
[A] 25.0 nm gate oxide and $N_D = 1 \times 10^{17}$ cm$^{-3}$
[B] 12.5 nm gate oxide and $N_D = 1 \times 10^{16}$ cm$^{-3}$.

capacitive coupling between the gate voltage and the potential in the channel ($Ge_xSi_{1-x}$ well for MOS-HHMTs). The degradation in subthreshold swing will become more pronounced as $\Delta E_V$ approaches $2\phi_B$ and $C_{sp}$ approaches $C_{ox}$. In Figure 3.12 the impact of the bandgap offset and the addition of the spacer layer capacitance in the subthreshold swing is compared to silicon MOSFETs using [A]- a 25.0 nm gate oxide and $N_D = 1 \times 10^{17}$ cm$^{-3}$, and [B]- a 12.5 nm gate oxide and $N_D =$ $\times 10^{16}$ cm$^{-3}$

Experimentally the subthreshold swing can be taken from the slope of the drain conductance curves plotted on a log scale (Figure 3 **3**). The subthreshold swing for MOS-HHMT structures and a silicon control were measured for devices with a 12.5 nm gate oxide and a uniform doping of $10^{16}$ cm$^{-3}$ n-type The two MOS-HHMT structures consisted of a $Ge_{0.2}Si_{.8}$ well with a 7.5 nm spacer (sample 646) and a $Ge_{.3}Si_{.7}$ well and a 10.5 nm

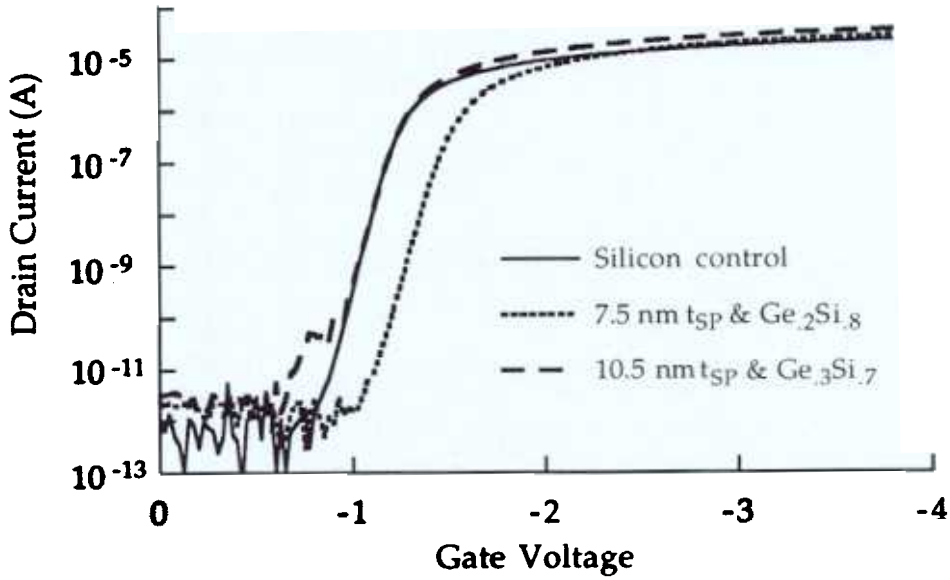


Figure 3.13 Subthreshold slope for two MOSHHMTs and a silicon MOSFET. The measurements were made using devices with W/L = 314μm/97μm and a drain bias of -0.1 V.
646 – 7.5 nm spacer and $Ge_{.2}Si_{.8}$ well
649 –10.5 nm spacer and $Ge_{.3}Si_{.7}$ well

spacer (sample 649). Using Eq. 3.16, the MOS-HHMTs would be expected to have a slightly larger subthreshold swing (≈ 69 mV/decade for sample 646 and ≈ 72 mV/decade for sample 649). Unfortunately the differences in subthreshold swing were masked by process related causes resulting from either an insufficient source/drain implant anneal or surface states in the plasma deposited oxide. In any case, no unexpectedly large increase in the subthreshold swing was noted

### 3.3 Device Fabrication

One of the chief concerns in fabricating the devices was to not only grow abrupt, coherently strained heterojunctions but to maintain them during the course of the device fabrication. This was especially important in light of the fact that several of the structures

considered had $Ge_xSi_{1-x}$ layers which exceeded the equilibrium critical thickness. Keeping this in mind, every attempt was made to keep the thermal budget to a bare minimum.

### 3.3.1 Epitaxial Growth

The epitaxial MOSHHMT structures were grown using Rapid Thermal Chemical Vapor Deposition which is discussed in detail in chapter 2.

The MOS-HHMT epitaxial films were grown on n-type wafers (in order to have body contacts though the substrate) with a resistivity of 1-4 Ω-cm. The $Ge_xSi_{1-x}$ well was grown at either 600°C or 625°C (lower growth temperatures were necessary to obtain the higher germanium fractions) using a flow of 1-3 sccm of $GeH_4$ and 26 sccm of dichlorosilane in a carrier gas of 3.0 lpm hydrogen. The $Ge_xSi_{1-x}$ well width was held constant at 10.0 nm, a compromise between avoiding quantum confinement effects (which would start to appear at smaller dimensions) and minimizing the strain energy (section .2). The silicon spacer layer was grown at 700° C. The width of the silicon spacers varied between 7.5 nm and 10.5 nm during the course of this work.

No dopant was introduced during growth at any time in order to achieve an *intrinsic* background doping of $10^{16}$ n-type. The FETs and capacitors were fabricated in separate processes.

### 3.3.2 Deposited Oxides

The most demanding thermal cycle the epitaxial layers would normally see after epitaxial growth would be during the process of thermal oxidation. In order to minimize the possibility of introducing misfit dislocations in the metastable $Ge_xSi_{1-x}$ layers and to keep the $Ge_xSi_{1-x}$ / Si interface as abrupt as possible the oxides were deposited by plasma enhanced CVD. The deposition was performed with a substrate temperature of 350° C to 400° C using a gas flow of 50 sccm of $NO_2$ and 97 sccm of 2% silane in nitrogen, and an rf power of 10 W. The samples were given an RCA clean prior to all depositions.

The general quality of the plasma deposited oxides was poor and the fixed charge and breakdown strength of the oxide varied from run to run A substantial fixed charge remained in the oxides even after the nitrogen anneal, with values ranging from $2 \times 10^{11}$ $cm^{-2}$ to $1 \times 10^{12}$ $cm^{-2}$. The breakdown strength of the oxide varied from 3.5 to 10 MV/cm. All the gates for the FETs of a given experiment had their oxides deposited in a single run to avoid variation in oxide qualities between devices.

### 3.3.3 Process Specifics

Two different processing schemes were used, one for MOS capacitors and a longer (four mask) process for FETs and Hall devices. The flow diagram of Figure 3.14 depicts the major processing steps in the fabrication of each of these devices.

Some of the details of the individual process steps include

√ Field oxide thickness of 500 - 600 nm

√ Boron source/drain implants at 25 kV and 50 kV with a total dose of $5 \times 10^{14}$ $cm^{-2}$

√ Gate oxide thickness of 10.0 or 12.5 nm

√ Nitrogen anneal at 700° C/ 30 min to reduce oxide fixed charge and anneal the implant

√ Forming gas anneal at 400° C/ 30 min in a 10% $H_2$/ 90% $N_2$ gas mixture

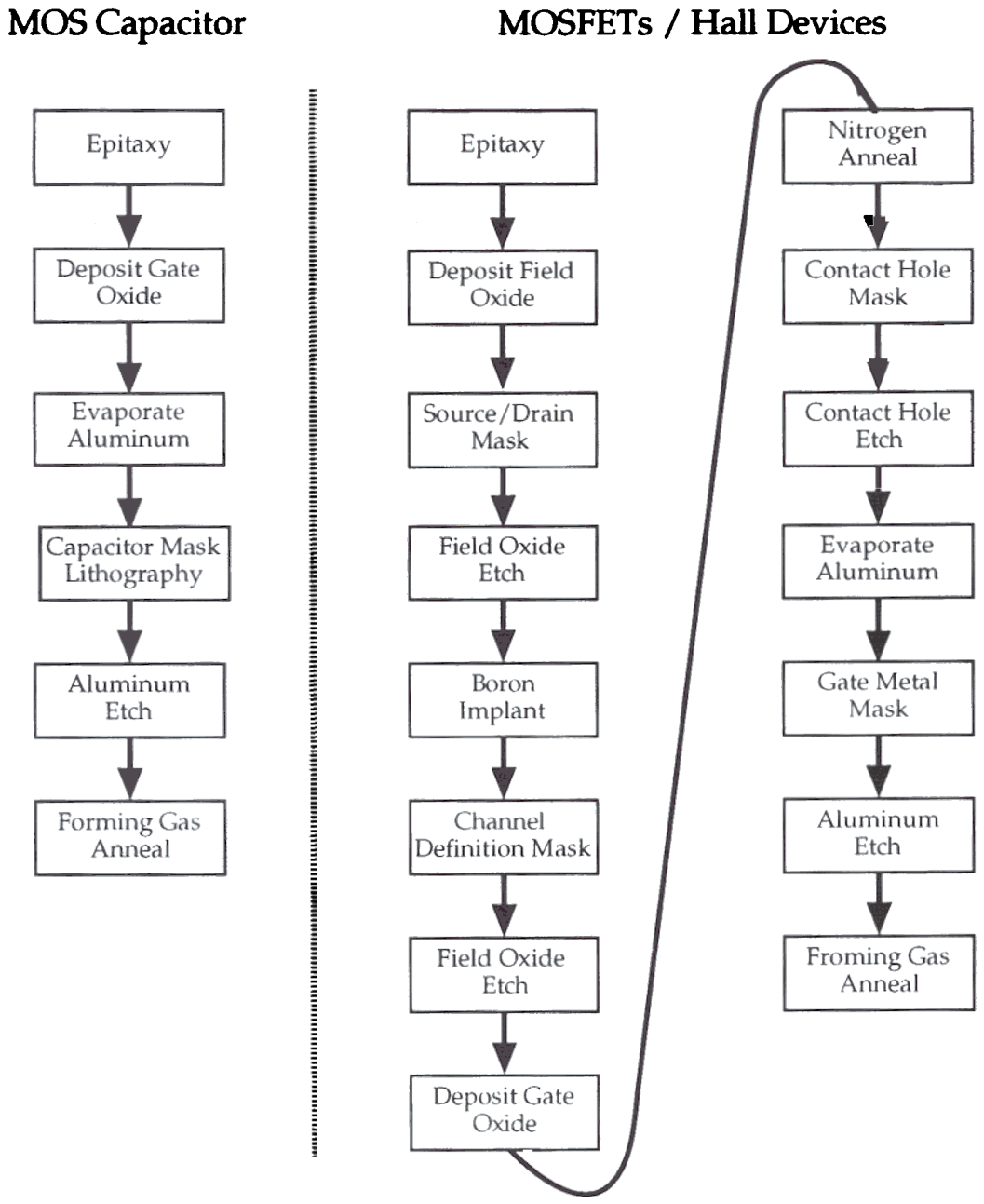


**Figure 3.14** **Process flow chart for MOS capacitors (left) and FET structures (right), including a MOS-gated Hall device.**

√ Body contacts were made using evaporated aluminum or melted indium

√ The FET and Hall process was not a self-aligned gate process and there was an approximately 15 μm overlap between the gate and the source/drains.

## 3.4 Carrier Confinement (Experimental)

To confirm that an inversion layer in the $Ge_xSi_{1-x}$ well actually forms, one can look for the gate capacitance change as holes go from being added predominantly to the $Ge_xSi_{1-x}$ well to being added predominantly to the $Si/SiO_2$ interface. As discussed in section 3.2.2 the gate capacitance is equal to the oxide capacitance when carriers are being added to the $Si/SiO_2$ interface. If the carriers are being added to the $Ge_xSi_{1-x}$ well the gate capacitance is equal to the series combination of the oxide capacitance and the silicon spacer layer capacitance (i.e. the gate capacitance is reduced).

Thus either Hall measurements or low frequency capacitance-voltage measurements should display a transition in the gate capacitance as the carriers go from being added predominantly to the $Ge_xSi_{1-x}$ well to being added predominantly to the $Si/SiO_2$ interface This capacitance change confirms the presence of an inversion layer in the $Ge_xSi_{1-x}$ well

### 3.4.1 Hall Measurements of Carrier Density vs. Gate Voltage

The slope of the hole density vs. gate voltage curve in inversion is equal to the gate capacitance (if interface states at the $Si/SiO_2$ interface are negligible)

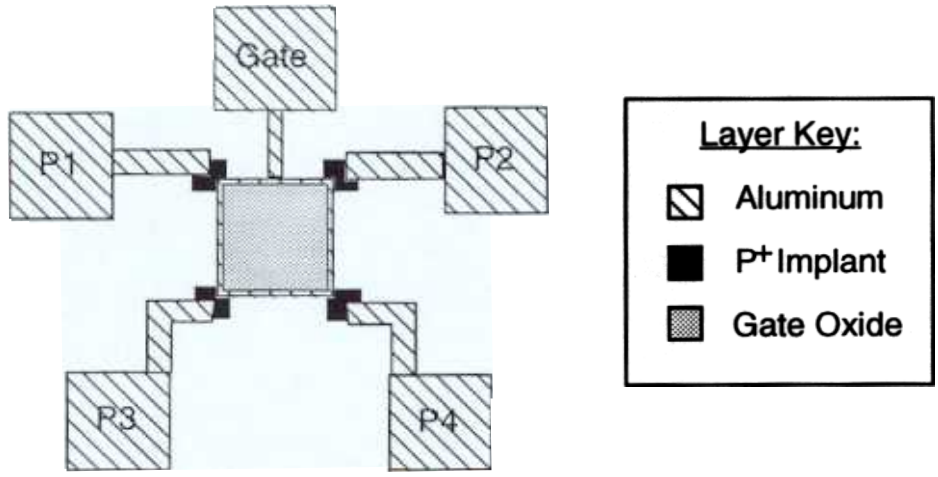


Figure 3.15 MOS-gated Hall Device. Carrier density controled by gate bias and measured by passing current between the diagonally opposite pads (P1/P4 or P2/P3) and measuring the Hall Voltage across the other two pads.

In order to measure the hole density versus gate voltage a MOS-gated Hall device was fabricated. A schematic of the device is shown in Figure 3.15.

The Hall measurements were performed by passing the current across diagonal source/drain pairs (between pads 1-4 or 2-3) and measuring the voltage across the other pads (Hall Voltage). A ramped magnetic field was used to extract the Hall coefficient since there was a voltage offset due to slight geometrical asymmetry of the device (due to alignment variations with the source/drain mask). The measurements were also performed with an AC current and at 100 K to reduce noise.

The hole density versus gate voltage for a structure with a 9.0 nm spacer layer and $Ge_{.4}Si_{.6}$ well is shown in Figure 3.16. Initially (at gate voltages less than V above threshold) the slope is consistent with the 9.0 nm spacer layer in series with the 12.5 nm gate oxide (269 $nF/cm^{-2}$) and at higher gate biases the slope is that of the gate oxide (337 $nF/cm^{-2}$). A thin gate oxide is necessary here in order to obtain a capacitance change large enough to be resolved experimentally.

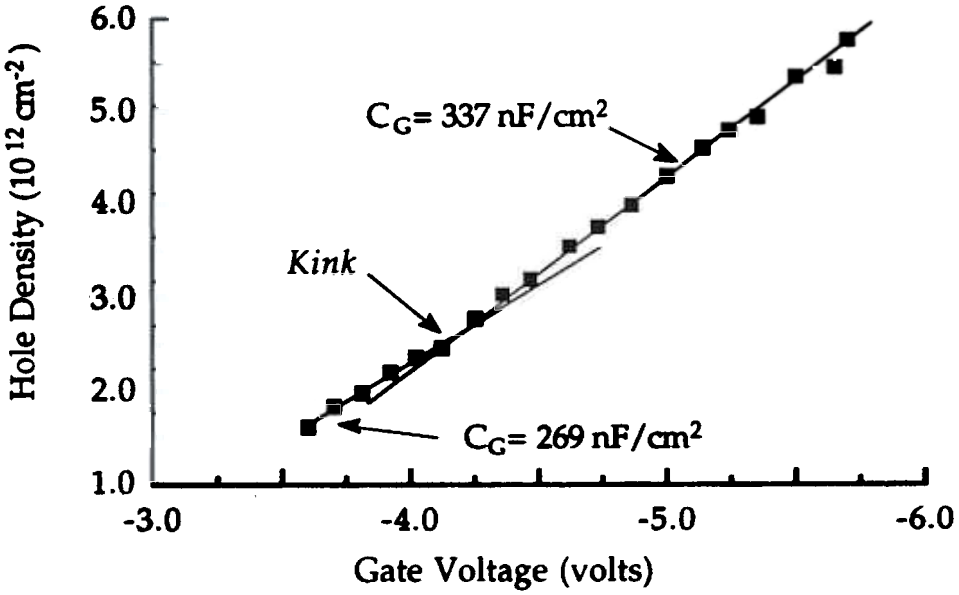


Figure 3.16 : Experimental hole density vs. gate voltage curve as measured by Hall effect. The structure consisted of a 9.0 nm silicon spacer and a $Ge_{.4}Si_{.6}$ well.

### 3.4.2 Quasi-Static Capacitance-Voltage Curves

A simpler way (conceptually) of seeing the capacitance change as holes go from being added to the $Ge_xSi_{1-x}$ well to being added at the $Si/SiO_2$ interface is with a low-frequency capacitance-voltage measurement. A low-frequency measurement is necessary to obtain the response of the holes (minority carriers) in the inversion regime This can be accomplished without going to extremely low frequencies (and therefore measuring low currents since $i_c = C\ dV/dt$) by either doing the measurement on a FET with the source (or drain) tied to the substrate (acting as a source of holes) or by a quasi-static measurement. Both of these techniques can encounter problems The FETs had a lot of parasitic capacitance from the source/drain overlap In the quasi-static method the gate leakage current must be very low since this is essentially a DC measurement and the current from the voltage ramp is small

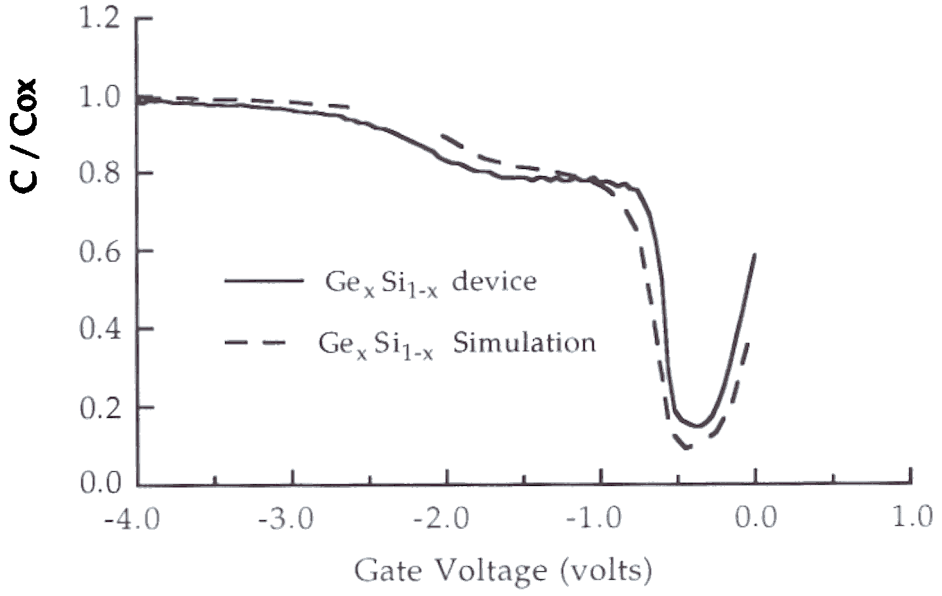


Figure 3.17 Comparison of the experimental quasi-static C-V measurement with simulation. The initial low capacitance plateau as the capacitor goes into inversion (carriers added to the $Ge_{.4}Si_{.6}$ well) is clearly seen and agrees well with simulation.

because of the slow ramp needed to achieve a quasi-static measurement (100-600 mV/sec).

The deposited gate oxides were occasionally of sufficient quality to perform a quasi-static measurement and one such curve is shown in Figure 3 7 for a structure with a 9.0 nm spacer and a $Ge_{.4}Si_{.6}$ well. As expected there is an initial low capacitance (plateau) when the capacitor first goes into inversion as the carriers are being added to the $Ge_{.4}Si_{.6}$ well. This plateau is followed by a transition to the higher capacitance of the gate oxide as the $Si/SiO_2$ interface also inverts and most of the carriers are added here. An estimate of $p \approx Q = \int C(v)\, dv)$ if the interface state density in the oxide is negligible. The carrier density in the $Ge_{.4}Si_{.6}$ well is estimated to be

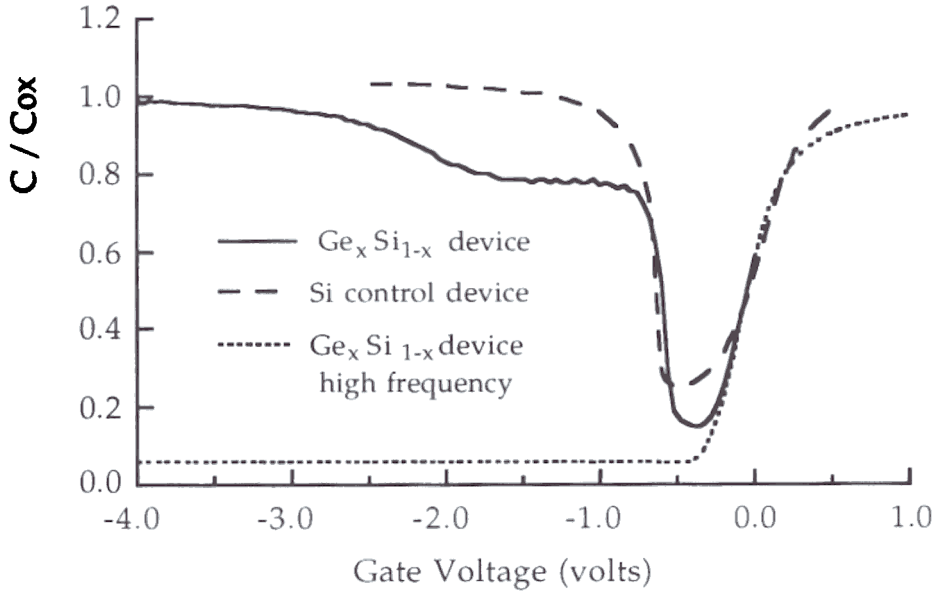


Figure 3.18 : The quasi-static C-V curve of the MOS-HHMT is shown along with one from the silicon control. Note that the silicon control, which has the same deposited oxide does not have an initial lower capacitance plateau at the onset of inversion eliminating the possibility that the plateau in the MOS-HHMT is due to oxide defects.

$\approx 2.0 \times 10^{12}$ cm$^{-2}$ from the C-V measurement, which agrees well with hole density at crossover calculated from simulation. The C-V curve from a simulation of the structure is also plotted in Figure 3.17 and is in good agreement with the measurement.

The quasi-static measurement of the Si control is shown in Figure 3.18 along with that of the $Ge_{.4}Si_{.6}$ device. The silicon control does not have a plateau in the initial stages of inversion. This removes the possibility that the plateau in the MOS-HHMT structure is the result of an interface trap in the deposited oxide pinning the surface potential

### 3.4.3 Carrier Confinement Postscript

Both Hall measurements and quasi-static C-V measurements provide convincing proof that an inversion layer can be formed in the $Ge_xSi_{1-x}$ well. The ability to form an inversion layer in the $Ge_xSi_{1-x}$ well does not mean that there is any transconductance benefit obtained by doing so. The reduced capacitance of the $Ge_xSi_{1-x}$ well reduces the gate control of the FET and hence the number of carriers. Therefore the mobility gain must outweigh the reduction in the number of carriers in order to achieve an increase in the transconductance compared to a standard MOSFET. Experimental results and modelling for mobility and conductance enhancement are examined in chapter 4.

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# Chapter 4 : MOS-HHMT Current-Voltage Characteristics and Conductance

## 4.1 MOSFET I/V Characteristics

Long-channel MOSFETs were fabricated in three different $Ge_xSi_{1-x}$ MOSFET structures, as well as in a prime Si(100) wafer which was included as a control[1] The spacer layer thickness and germanium fraction in the well for samples 646, 649 and 650 are given in Table 4.1. The germanium fractions in samples 646 and 649 were confirmed by photoluminescence measurements. The width of the $Ge_xSi_{1-x}$ well was held fixed at 10.0 nm as a compromise between critical thickness considerations (section .2.1) and the desire to have the well wide enough to keep the energy levels as close as possible to the band edge.

The $Ge_{0.2}Si_{0.8}$ layer in sample 646 was below the critical thickness (for x=0.2, $h^*$=14.4 nm) while the $Ge_{0.3}Si_{0.7}$ layer of sample 649 was slightly above critical thickness (for x=0.3, $h^*$= 8.6 nm), and the $Ge_{0.4}Si_{0.6}$ layer of sample 650 was well above the equilibrium critical thickness (for x=0.4, $h^*$= 5.9 nm). The position of the $Ge_xSi_{1-x}$ wells of each sample is plotted in relation to the equilibrium critical thickness curve in Figure 4.

Table 4 Sample structures for the MOS-HHMT devices fabricated and measured in this chapter.

| sample | spacer thickness (nm) | germanium fraction |
|---|---|---|
| silicon control | – | – |
| 646 | 7.5 | 0.21 |
| 649 | 10.5 | 0.33 |
| 650 | 7.5 | 0.40 |

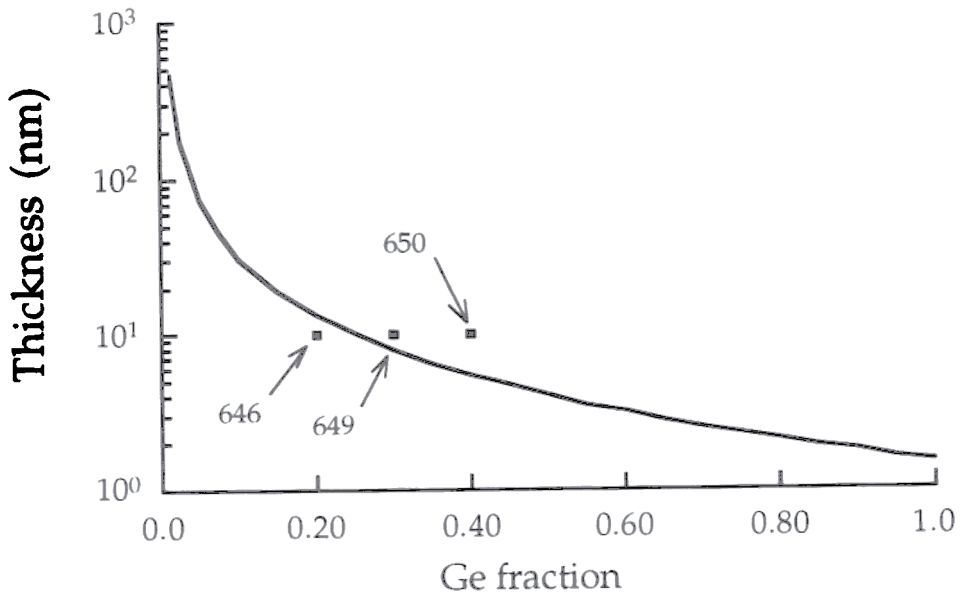


Figure 4.1 Relation of the $Ge_xSi_{1-x}$ layers in samples 646, 649 and 650 to the equilibrium critical thickness (section 1.2).

Simulations predict (section 3.2.3) that the structures of both sample 646 and sample 649 have a maximum hole concentration of $\approx 1.2 \times 10^{12}$ $cm^{-2}$ in the $Ge_xSi_{1-x}$ well. Any difference in transconductance will therefore result from different channel mobilities rather than as a consequence of a difference in the fraction of carriers in the $Ge_xSi_{1-x}$ well between these two structures.

The gate lengths of the MOSFETs ranged from 7 μm to 300 μm The drain conductance and saturation current was measured over a range of temperatures from 300 K to 90 K. Additional information regarding the device fabrication is found in section 3.3

### 4.1.1 Drain Conductance Measurements

The drain current versus gate voltage was measured with drain biases of -0.1, -0.2, and -0.3 volts on the FETs. Three measurements were made to

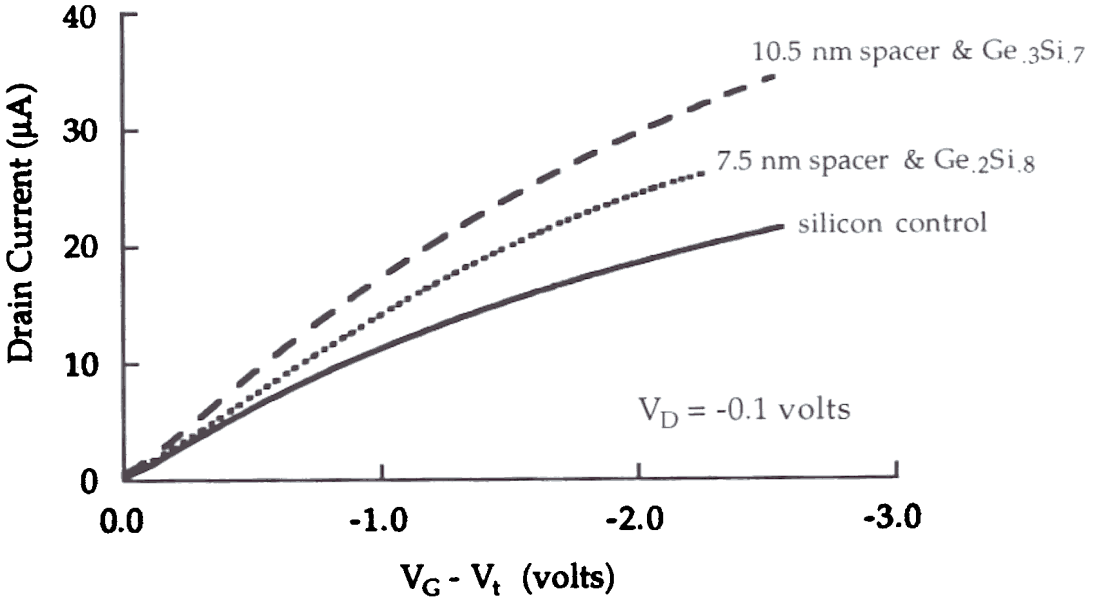


Figure 4.2 Drain conductance at 300 K for MOSFETs with W/L = 314μm/97μm. Sample 646 (7.5 nm spacer & $Ge_{.2}Si_{.8}$ well) has a 25% larger drain current than the silicon control and sample 649 (10.5 nm spacer & $Ge_{.3}Si_{.7}$ well) has a 50% larger drain current.

ensure that the drain current was linear with the drain voltage (i.e. FET operating in the linear region)

Figure 4.2 shows the room temperature (300 K) drain conductance of MOSFETs with a 97 μm gate length and 315 μm width measured with zero source-substrate bias and a drain bias of -0 V The MOS-HHMTs from sample 646, which had a 7.5 nm spacer and a $Ge_{.2}Si_{.8}$ well, had a 25-30% larger drain current than the Si control devices and the MOS-HHMTs from sample 649, which have a 10.5 nm spacer and a $Ge_{.3}Si_{.7}$ well, had a 50% larger drain current over the whole range of gate voltages The gate voltage was normalized ($V_G$–$V_T$ used instead of $V_G$) to account for the threshold shift caused by the valence band discontinuity at the $Ge_xSi_{1-x}$ /Si interface (section 3.2.5) This is important for a fair comparison since the drain current is

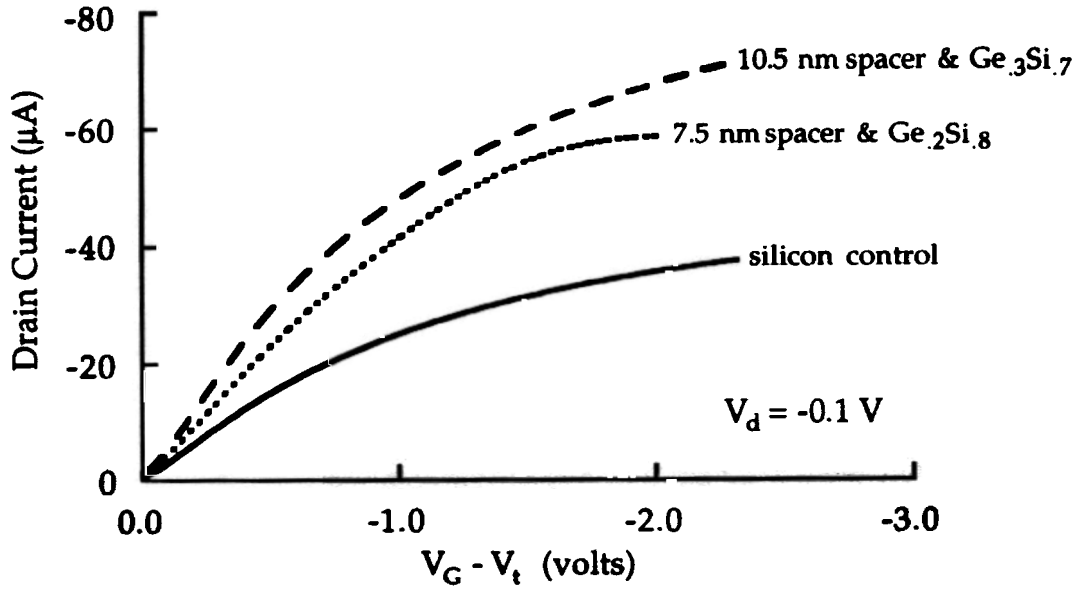


Figure 4.3 Drain conductance at 90 K for MOSFETs with W/L = 314μm/97μm. Sample 646 (7.5 nm spacer & $Ge_{.2}Si_{.8}$ well) has a 70% larger drain current than the silicon control and sample 649 (10.5 nm spacer & $Ge_{.3}Si_{.7}$ well) has a 120% larger drain current.

proportional to ($V_G$ - $V_T$) rather than $V_G$ The improved performance at 300 K can be attributed to either a reduction in the hole effective mass (which depends on germanium fraction and the strain) or to the increased average separation of the holes from the $Si/SiO_2$ interface.

At 90 K the drain conductance of sample 646 which had a 7.5 nm spacer and a $Ge_{.2}Si_{.8}$ well, was 70% higher than that of the silicon control and the drain conductance of sample 649 which had 10.5 nm spacer and a $Ge_{.3}Si_{.7}$ well was 120% higher (Figure 4.3). This increase in the relative performance enhancement of the MOS-HHMTs over the silicon MOSFETs at low temperatures shows that the improved perfarmance of the MOS-HHMTs results from a decreased surface scattering rather than a reduced effective mass in the $Ge_xSi_{1-x}$ well. If a reduced effective mass were the cause of the

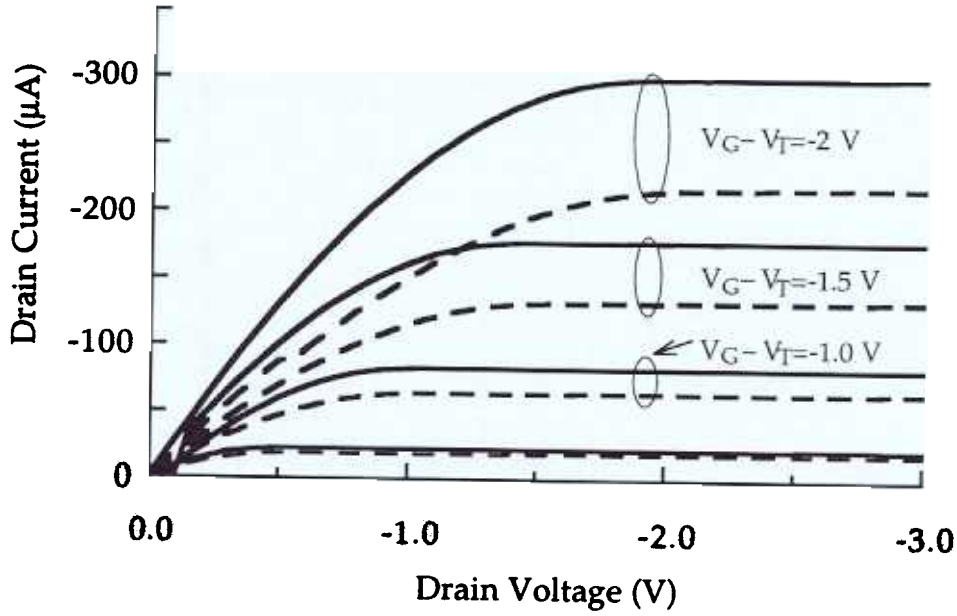


Figure 4.4 : Comparison of the characteristic curves for MOSFETs with W/L = 314μm/97μm. made from sample 649 (10.5 nm spacer & $Ge_{.3}Si_{.7}$ well)) and the silicon control. Gate voltages were normallized for threshold voltage differences. Sample 649 had a 40% higher saturation current than the silicon control.

performance improvement the enhancement over the silicon MOSFET would not change with temperature. As the temperature is lowered the drain conductance of all the devices was increased due to the decreased number of phonons at low temperature (and subsequently lower phonon scattering).

### 4.1.2 Saturation Current

The characteristic MOSFET curves (drain current vs. drain voltage) were measured in order to see the saturation characteristics of the devices. Again the gate voltage was normalized with respect to the threshold voltage in order to compare the currents at roughly equal carrier concentrations. In saturation the drain current is approximately

Eq. 4.1 $$I_D \approx \left(\frac{W}{2L}\right)\mu_p C_{ox}(V_G - V_T)^2$$

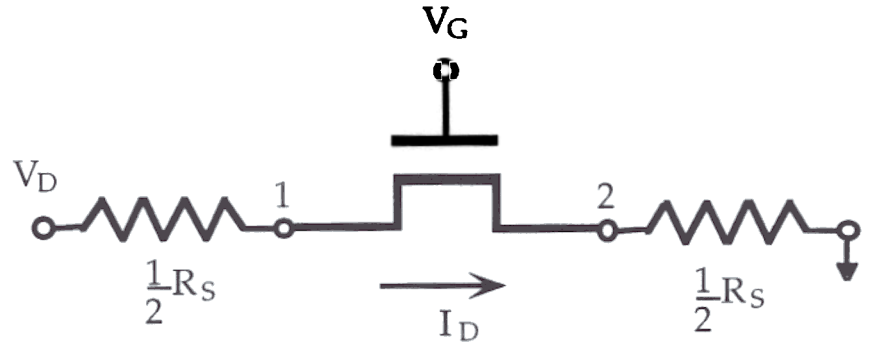


Figure 4.5 Equivalent circuit showing parasitic series resistance of a MOSFET. The actual voltage drop across the source/drain is equal to the potential between nodes 1 and 2 i.e. $V_{DS} \rightarrow V_D - I_D \cdot R_S$.

and is dependent on $(V_G - V_T)$ rather than $V_G$.

At 300 K the FETs from sample 649 had a 40% higher saturation current than the silicon control devices (Figure 4.4). The drain current was constant with respect to drain voltage in the saturation region, as expected for ideal long-channel MOSFETs.

### 4.1.3 Effective Mobility

#### 4.1.3.1 Extraction of the Parasitic Series Resistance

Parasitic series resistance ($R_S$) in a MOSFET reduces the actual voltage drop across the channel of the device

Eq. 4.2 $$V_{DS} = V_D - I_D \cdot R_S$$

A circuit schematic of the device is shown in Figure 4.5. If not corrected for this parasitic series resistance will lead to an underestimate of the effective mobility. The parasitic series resistance from the source/drains was extracted using the method Terada and Muta [2]. In this method the drain current is measured in the linear region of operation so that the measured resistance between the source and drain is

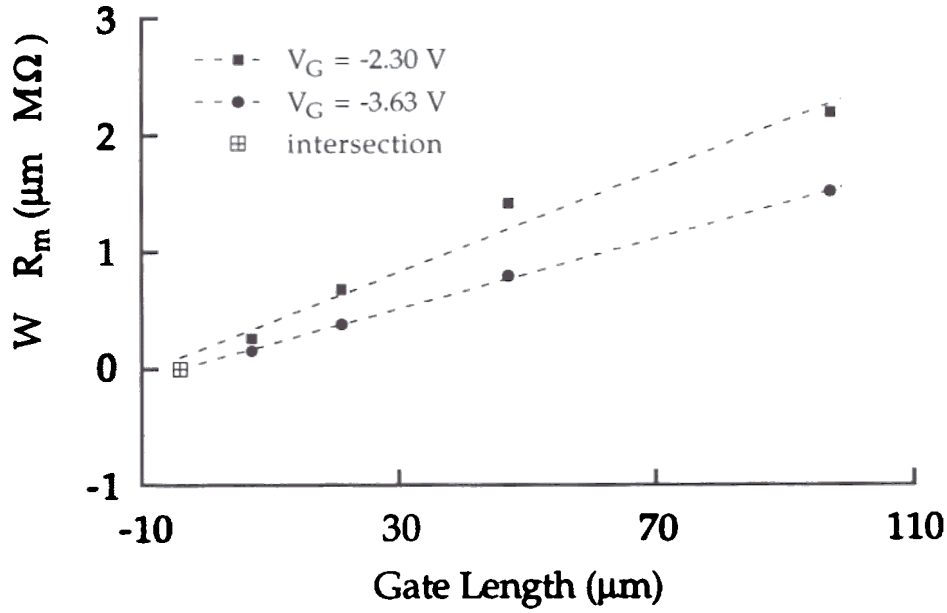


Figure 4. 6 Plot of $W \cdot R_m$ vs. $L_m$ for series resistance extraction. The intersection of curves for two different gate biases gives the series resistance ($W \cdot R_S = 4.4k\Omega \cdot \mu m$) and the change in the effective gate length ($\Delta L = -4.1\ \mu m$).

Eq. 4.3
$$R_m = \frac{(L_m - \Delta L)}{W \mu_{V_g} C_{ox}(V_G - V_T)} + R_S$$

where $(L_m - \Delta L)$ is the effective channel length of the MOSFET.

If the measured channel resistance is plotted as a function of the measured gate length ($L_m$) a straight line results. If the measured resistance for two different gate voltages is plotted, the curves intersect at the point where

Eq. 4.4
$$L_m = \Delta L$$

and

Eq. 4.5
$$R_m = R_S$$

The gate width of the MOSFETs was not held constant in this work so a plot of the measured resistance times the gate width versus the measured gate length was made. A typical plot is shown for the silicon control devices at

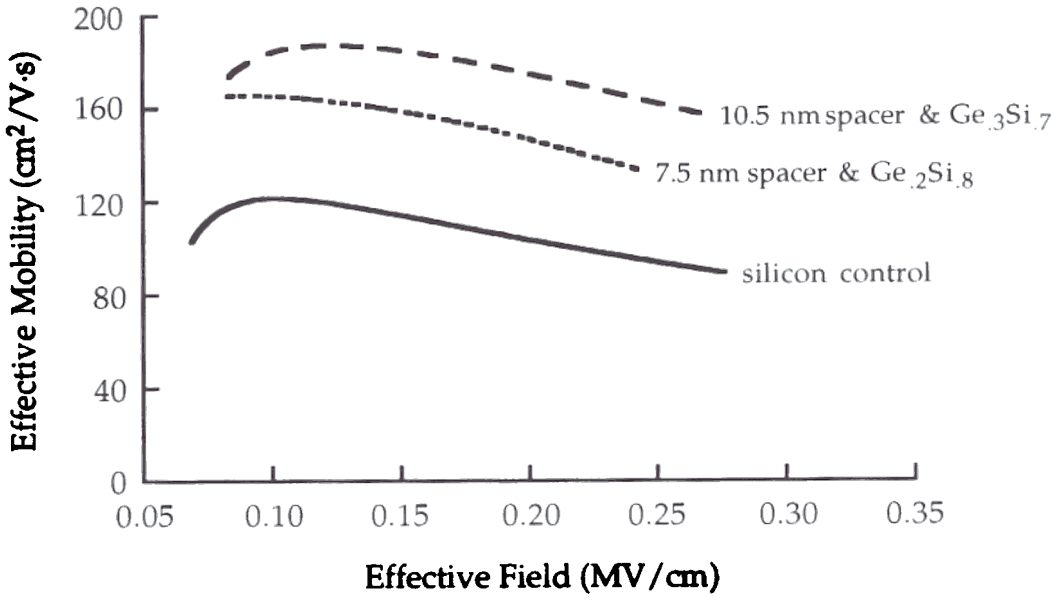


Figure 4. 7 Effective mobility plotted as a function of the effective vertical field at 300 K Extracted from the data in Figure 4.2.

300 K in Figure 4.6. The intersection of the curves for gate voltages of -2.30 and -3.63 volts indicates that the measured channel width was ≈4.1 μm too small and the series resistance times the gate width had a value of ≈4.4 kΩ·μm. The corrections made to the drain source voltage were less than 5% (5 mV).

#### 4.1.3.2 Effective Mobility Results

The effective mobility vs. effective vertical field for samples 646, 649 and the silicon control was extracted from drain conductance measurements ranging from 90 - 300 K as described in section 3.1.2

The effective mobility is plotted as a function of the effective vertical field for 97μm gate length FETs at 300 K in Figure 4.7. The peak effective mobility of sample 649 was over 180 $cm^2/V \cdot s$ and had a 50% improvement in the effective mobility across the whole range of effective vertical fields compared to a silicon control device. Sample 646 had a peak effective mobility of 165 $cm^2/V \cdot s$ and a 35% effective mobility enhancement over the

silicon control devices. At first the almost constant enhancement of the effective mobility over the whole range of effective vertical fields may seem surprising since increasing the effective vertical field reduces the fraction of holes in the $Ge_xSi_{1-x}$ well (section 3.2.4) This might lead one to believe that the difference in effective mobilities between the $Ge_xSi_{1-x}$ FETs and the silicon MOSFETs should decrease as the fraction of carriers in the $Ge_xSi_{1-x}$ well falls off. This apparent discrepancy results from the overestimate of the hole density in the MOS-HHMTs while holes are being added to the $Ge_xSi_{1-x}$ well caused by using $C_G = C_{ox}$ (section 3.2.2 and 4.1.2.1). In section 4.2, when modeling the inversion layer hole mobility (as opposed to effective mobility) the correct hole density is used and the relative mobility enhancement does decrease with increasing effective vertical field as expected.

Comparison with the literature shows that FETs from sample 649 have a 25% improvement in effective mobility (drain conductance) at 300 K over silicon MOSFETs with thermal oxides [3]. It is possible that further effective mobility improvements could be seen with better quality oxides since the performance of the silicon control devices was markedly worse than those typically seen in literature (the fixed charge of the plasma deposited gate oxides was $\approx 4\text{-}6 \times 10^{11}$ $cm^{-2}$).

At lower temperatures the performance enhancement of the MOS-HHMTs becomes even larger (Figure 4.8) with sample 649 demonstrating a 100-125% improvement across the range of effective vertical fields and a peak effective mobility of 780 $cm^2/V \cdot s$ at 90 K. The widening performance gap between the MOS-HHMTs and the silicon FETs, as the temperature is reduced, is clearly seen by comparing the peak effective mobility vs temperature (Figure 4.9).

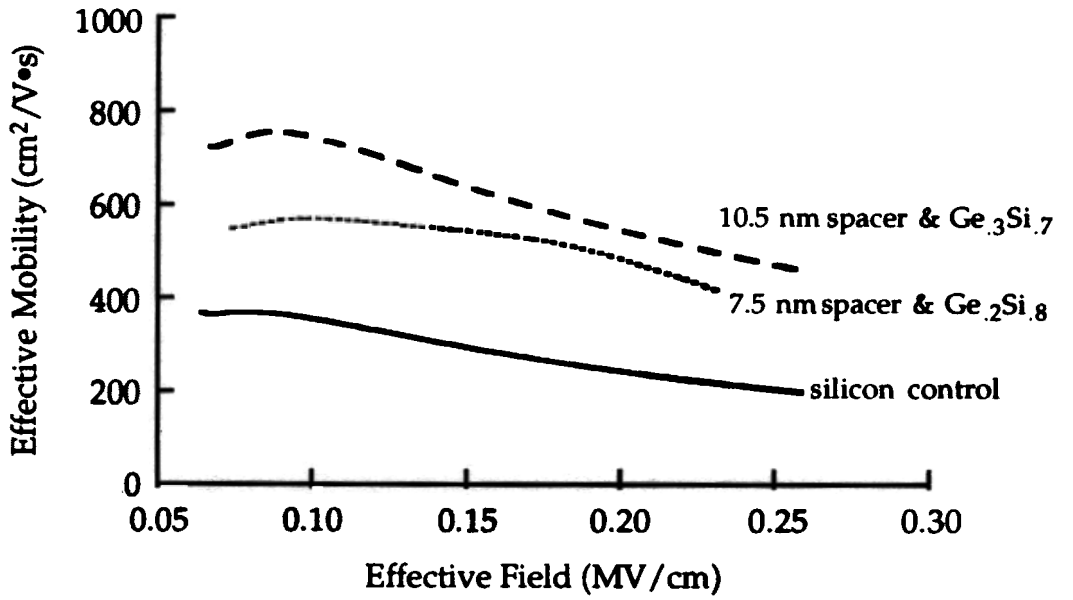


Figure 4. 8 Effective mobility plotted as a function of the effective vertical field at 90 K. Extracted from the data in Figure 4.3

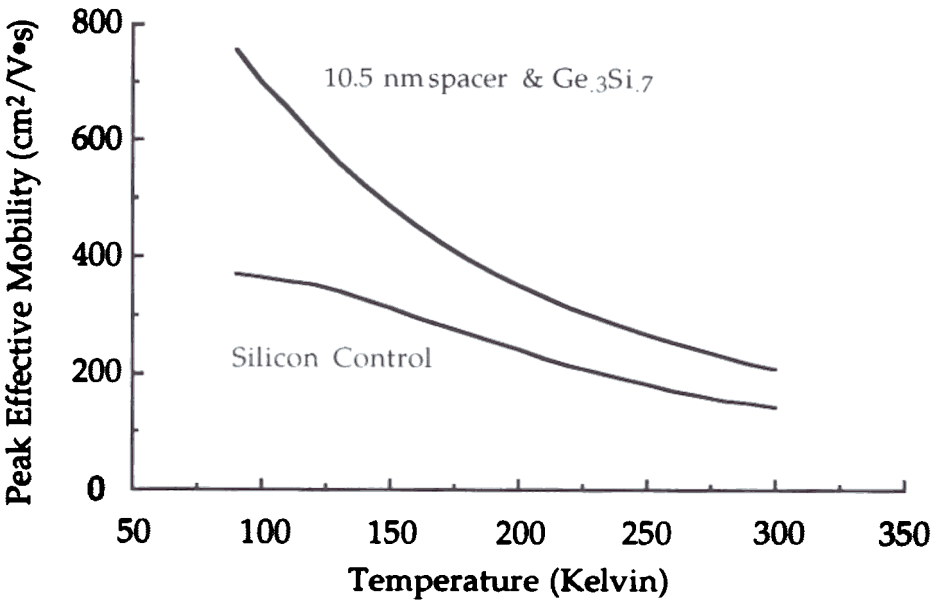


Figure 4. 9 Peak effective mobility as a function of temperature for sample 649 (10.5 nm spacer & $Ge_{.3}Si_{.7}$ well) and the silicon control. The performance enhancement of the MOS-HHMTs grows larger at low temperature.

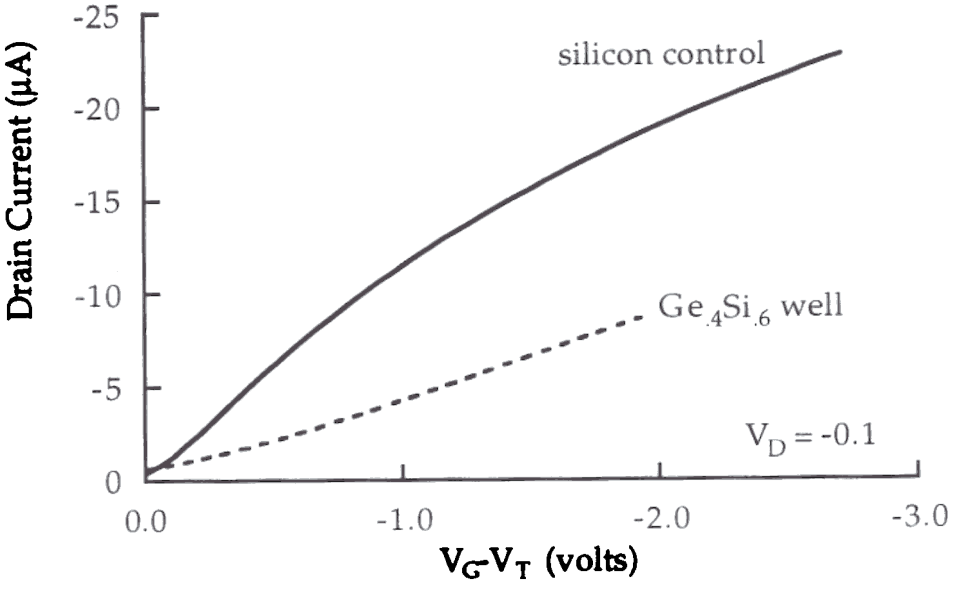


Figure 4.10 Drain conductance of sample 649, which has a $Ge_{.4}Si_{.6}$ layer well above critical thickness, is substantially worse than that of the silicon control. It is believed that sample 650 had misfit dislocations.

### 4.1.4 Relaxed $Ge_xSi_{1-x}$ Structures

In contrast to the significant improvement in effective mobility seen in samples 646 and 649 the performance of PMOS devices made from sample 650, which had a $Ge_{.4}Si_{.6}$ well and a 7.5 nm Si spacer, was markedly worse than that of the Si control (see Figure 4.10). In addition, poor lifetimes (capacitors would not deep deplete) and poor subthreshold swings (twice those of the other devices) seen in the MOSFETs made from sample 650 lead us to believe that this sample had misfit dislocations at the $Si/Ge_xSi_{1-x}$ interface This is consistent with the fact that this device had a $Ge_{0.4}Si_{0.6}$ well that was almost twice the equilibrium critical thickness for this germanium fraction (see Figure 4.1). The resulting misfit dislocations at the heterojunction interface would act as scattering sites to severely reduce mobility. It is not known whether the dislocations were process-induced or whether the as-grown layer was relaxed.

## 4.2 Low Field Mobility Model

Many models have been proposed to interpret the low field mobility of a MOSFET. Most approaches to mobility modeling have been either strictly empirical[4,5,6] or based on Monte-Carlo simulations[7,8]. The empirical models are used in device simulations in order to obtain simple expressions for the effective mobility. They tend to avoid many of the complex scattering mechanisms in favor of simple, easily measurable, device parameters. Unfortunately these empirical models tend to obscure the important device physics. The Monte-Carlo approach is particularly valuable for time dependent studies and non-equilibrium phenomena but can be very CPU intensive. Monte-Carlo simulations also use purely phenomenological models for the surface scattering.

The goal of this section is to develop an analytic inversion layer mobility model for MOSFETs which clearly shows the dependence of the surface scattering (surface mobility) on the average separation of carriers from the $Si/SiO_2$ interface ($Z_{avg}$)[9]. This relation is necessary for modeling MOS-HHMTs since the average separation of carriers from the $Si/SiO_2$ interface can be changed by varying the silicon spacer layer thickness ($t_{sp}$). To avoid the added complexity of a non-uniform hole density across the channel this model considers the inversion layer mobility of the FETs in the linear region of operation.

### 4.2.1 Overview

To model the inversion layer mobility enhancement achieved in the MOS-HHMTs by moving the holes away from the $Si/SiO_2$ interface a relation between the inversion layer mobility and the average separation of the carriers from the $Si/SiO_2$ interface ($Z_{avg}$) must be developed. In this model these two quantities are linked through their relation to the effective vertical field.

The approach is to treat the inversion layer mobility ($\mu_{inv}$) a consisting of two components

(1) bulk mobility ($\mu_{bulk}$) - which includes the effects of bulk phonons and ionized impurities, and

(2) surface mobility ($\mu_{surf}$) - which includes the effects of oxide fixed charge and $Si/SiO_2$ interface roughness

It is further assumed that these two mobility components may be combined using Matthiessen's rule so that

Eq. 4.6
$$\frac{1}{\mu_{inv}} = \frac{1}{\mu_{bulk}} + \frac{1}{\mu_{surf}}$$

Tabulated data from Jacoboni [10] are used for the bulk hole mobility with a n-type doping of $10^{16}$ $cm^{-3}$. The bulk mobility of $Ge_xSi_{1-x}$ is assumed to be the same as that of silicon. This simplification is suggested by the increase in the performance of the MOS-HHMTs, compared to the silicon MOSFETs, as seen in section 4. and is discussed further in section 4.5

A relation between the surface mobility and the average separation of carriers fom the $Si/SiO_2$ interface is extracted from the silicon MOSFETs and then applied to the MOS-HHMTs

### 4.2.2 Development of the model from silicon MOSFET

The relationship of the surface mobility to the average separation of carriers from the $Si/SiO_2$ interface is the heart of this model. There are several key assumptions made in establishing this relation

1. The surface mobility of carriers can be described in terms of the average separation of carriers from the $Si/SiO_2$ interface instead of needing to consider the surface scattering over the whole probability distribution
2. Both the average separation distance from the $Si/SiO_2$ interface ($Z_{avg}$) and the surface mobility can be related to the effective vertical field ($E_{eff}$)

3. The simple empirical form

Eq. 4.7 $$\mu_{surf} \propto \beta \left(Z_{avg}\right)^2 + \mu_0$$

can be used to relate the surface mobility to the average separation of carriers from the $Si/SiO_2$ interface, where $\beta$ and $\mu_o$ are fitting parameters

In order to find the dependence of the average separation of the carriers from the $Si/SiO_2$ surface in a Si MOSFET it is necessary to know the hole probability distribution in the potential well A semi-classical treatment of the MOSFET, such as the one presented in section 3.2.3, will result in a probability density with a peak at the $Si/SiO_2$ interface, underestimating the average separation of carriers from the $Si/SiO_2$ interface. In order to get a realistic hole probability distribution it is necessary to solve Schröedinger's equation and Poisson's equation simultaneously This is a complicated problem for pMOSFETs since the valence band is six-fold degenerate (light hole, heavy hole and split-off hole - plus spin degeneracy) Instead of solving this problem from scratch the results of Ohkawa and

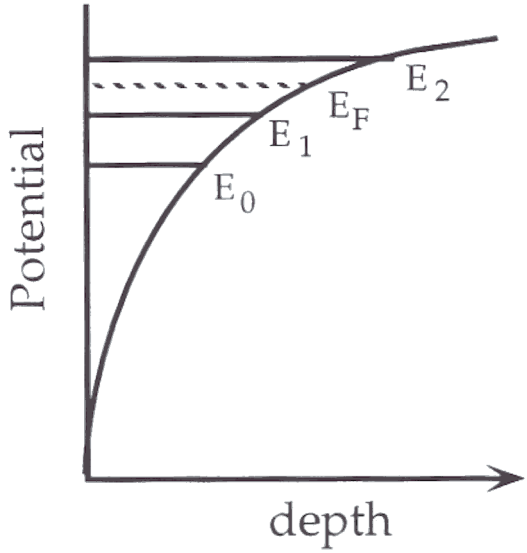


Figure 4.11 Subband Energy Levels in a pMOSFET. $E_0$ and $E_2$ correspond to the heavy hole bands while $E_1$ corresponds to the light hole band.

Uemura[11] are used. They calculated the subband energy levels in the gate potential for several inversion layer hole densities. A drawing of the hole potential well near the $Si/SiO_2$ interface and the subband energy levels is shown in Figure 4 1 The $E_0$ and $E_2$ energy levels correspond to the heavy hole band and the $E_1$ energy level corresponds to the light hole band.

Ohkawa and Uemura calculated the subband energies with respect to the Fermi level for four different inversion charge densities ($q \times N_{inv}$) at zero Kelvin (see Figure 4.12) In order to use this data several assumptions were necessary

The relative position of the subband energy levels does not change much with temperature (i.e. no large shifts caused by the redistribution of holes among the sub-bands).

2. The hole distributions associated with the individual sub-bands can be closely approximated using variational wavefunctions[12] of the form

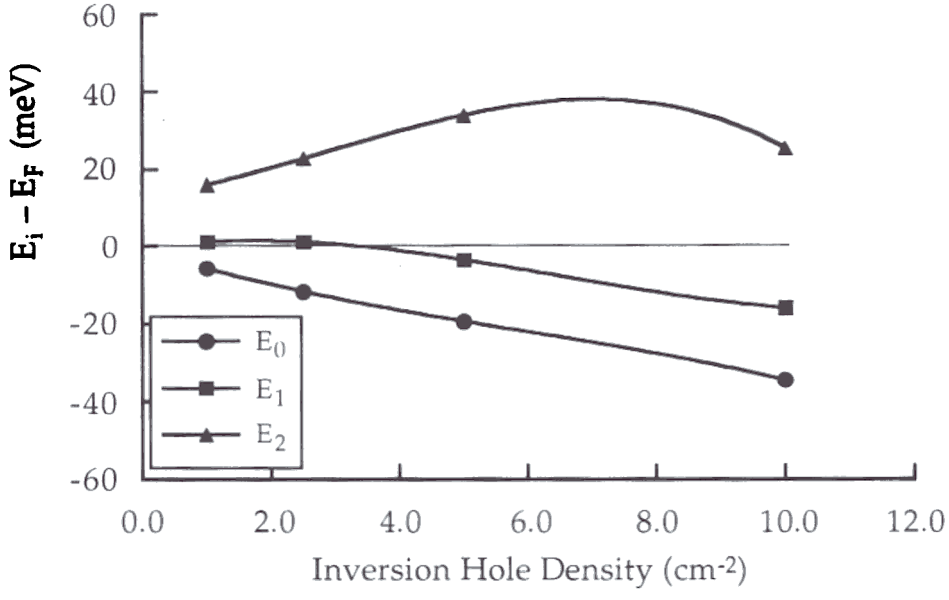


Figure 4.12 Energy levels for the three lowest subbands in a pMOSFET for several inversion hole densities ($N_D = 10^{15}$ $cm^{-3}$). After Reference [11].

Eq. 4.8 $$\psi_i(z) = z\sqrt{\frac{3}{2}b_i^3}\; e^{\frac{-(b_i z)^{\frac{3}{2}}}{2}} \quad \text{for } i = 0, 2$$

and

Eq. 4.9 $$\psi_1(z) = z(1 - C_1 b_1 z)\sqrt{\frac{3}{2}b_1^3 A_1}\; e^{\frac{-(b_1 z)^{\frac{3}{2}}}{2}}$$

These assumptions were necessary to calculate the average separation of the holes in each subband from the $Si/SiO_2$ interface.

Starting with the subband energy spacings and the two assumptions mentioned above the average separation of the carriers, in each subband, from the $Si/SiO_2$ interface was calculated. The average carrier spacing from the $Si/SiO_2$ interface was then calculated by taking a weighted average of the subband spacings Weighting was done by iterating the Fermi level until the

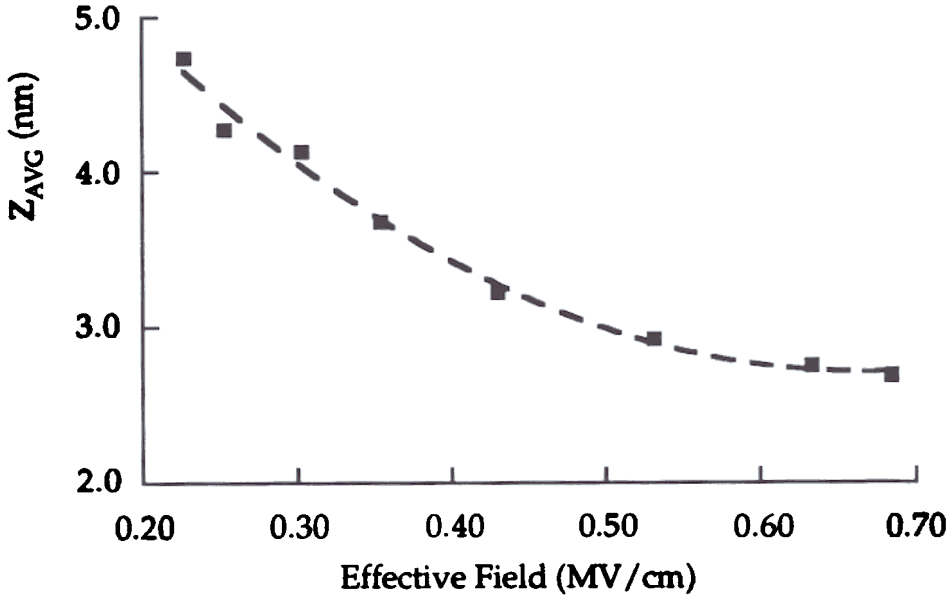


Figure 4.13 Average seperation of holes from the Si/SiO2 interface as a function of the effective (vertical) field at 290K.

total hole density was correct and then calculating the fraction of holes in each subband.

The inversion density ($N_{inv}$) used by Ohkawa and Uemura was converted to the corresponding effective vertical field using equation 4.3 and the resulting average separation of the carriers from the $Si/SiO_2$ interface ($Z_{avg}$) is plotted vs. effective vertical field in Figure 4.13 (T=290 K). The decreasing average separation of the carriers from the $Si/SiO_2$ interface with increasing effective vertical field agrees with the qualitative description of section 3 Similar results are obtained at 90 K. (The average separation of carriers from the $Si/SiO_2$ interface at 90 K is actually somewhat less since a larger fraction of the carriers reside in the lower energy states)

The surface mobility vs. effective vertical field is extracted from the experimentally measured inversion layer mobility of the Si control devices Rearranging Matthiessen's rule

Eq. 4.10
$$\frac{1}{\mu_{surf}(E_{eff})} = \frac{1}{\mu_{eff}(E_{eff})} - \frac{1}{\mu_{bulk}}$$

Thus the surface mobility ($\mu_{surf}$) as a function of effective vertical field can be extracted from the measured effective mobility ($\mu_{eff}$) and tabulated values of the bulk mobility

Now that the average separation of carriers from the $Si/SiO_2$ interface and the surface mobility have been described in terms of the effective vertical field the two can be related using Eq. 4.7, determining the coefficients $\beta$ and $\mu_0$ The extracted surface mobility and the empirical fit of Eq. 4.7 taken from the silicon control MOSFET are shown in Figure 4.14

### 4.2.3 Applying the surface mobility model to the MOS-HHMT

The inversion layer mobility in the MOS-HHMTs is more complicated than the silicon pMOSFET. In addition to the different scattering mechanisms discussed in section 3 the MOS-HHMT also has scattering terms due to interface roughness at the $Ge_xSi_{1-x}$ /Si interface and alloy scattering in the $Ge_xSi_{1-x}$ well and the change in effective mass in the strained $Ge_xSi_{1-x}$ Initially it will be assumed that the alloy scattering and $Si/Ge_xSi_{1-x}$

interface scattering are of relatively minor importance and that the change in effective mass is inconsequential.

It now remains to apply the surface mobility derived from the silicon FETs to the MOS-HHMTs in an appropriate manner. Since the holes in the MOS-HHMT are confined to two different channels - one in the $Ge_xSi_{1-x}$ well and one at the $Si/SiO_2$ interface - it will be assumed that these two channels

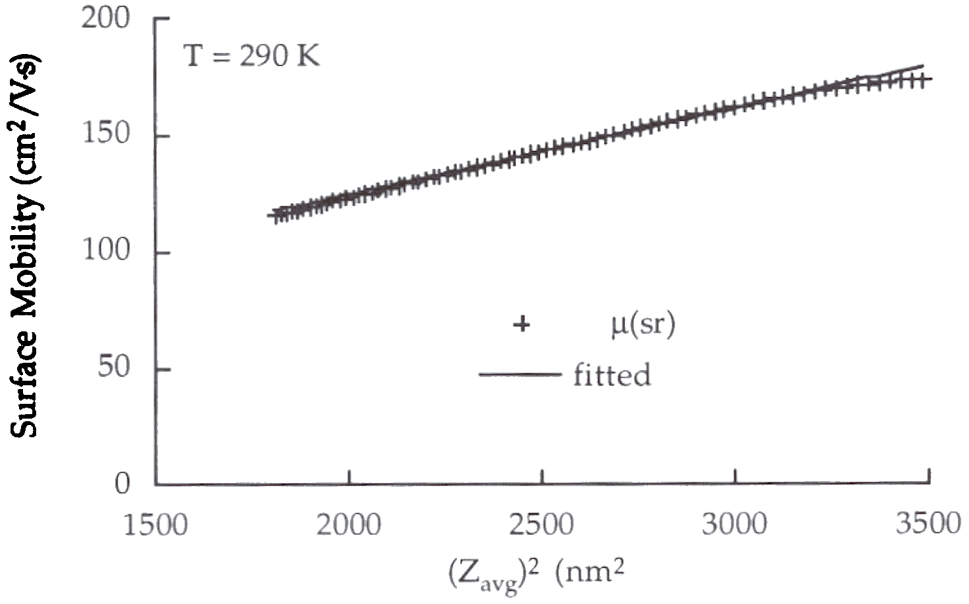


Figure 4.14 Surface mobility (component) extracted from the silicon control device vs the average carrier spacing from the $Si/SiO_2$ interface squared. The fit of the surface mobility Eq. 4.7 is also shown.

can be treated independently and an inversion layer mobility for each channel is calculated separately. The inversion layer mobility in a MOS-HHMT structure will then be a weighted average of the two channel mobilities :

Eq. 4.11
$$\mu_{avg} = \left[\frac{p_{Ge_xSi_{1-x}}}{p_{total}}\right]\mu_{Ge_xSi_{1-x}} + \left[\frac{p_{Si/SiO_2}}{p_{total}}\right]\mu_{Si/SiO_2}$$

where $p_{GeSi}$ , $p_{Si/SiO_2}$ , and $p_{total}$ are the hole densities in the $Ge_xSi_{1-x}$ well, at the $Si/SiO_2$ interface, and the total hole density respectively. The hole densities were taken from simulations using the previously described Poisson solver (section 3.2.3)

The average separation of carriers from the $Si/SiO_2$ interface and effective vertical field must be treated differently for each channel as graphically depicted in Figure 4.15 The effective vertical field seen by the carriers in the $Ge_xSi_{1-x}$ well will be

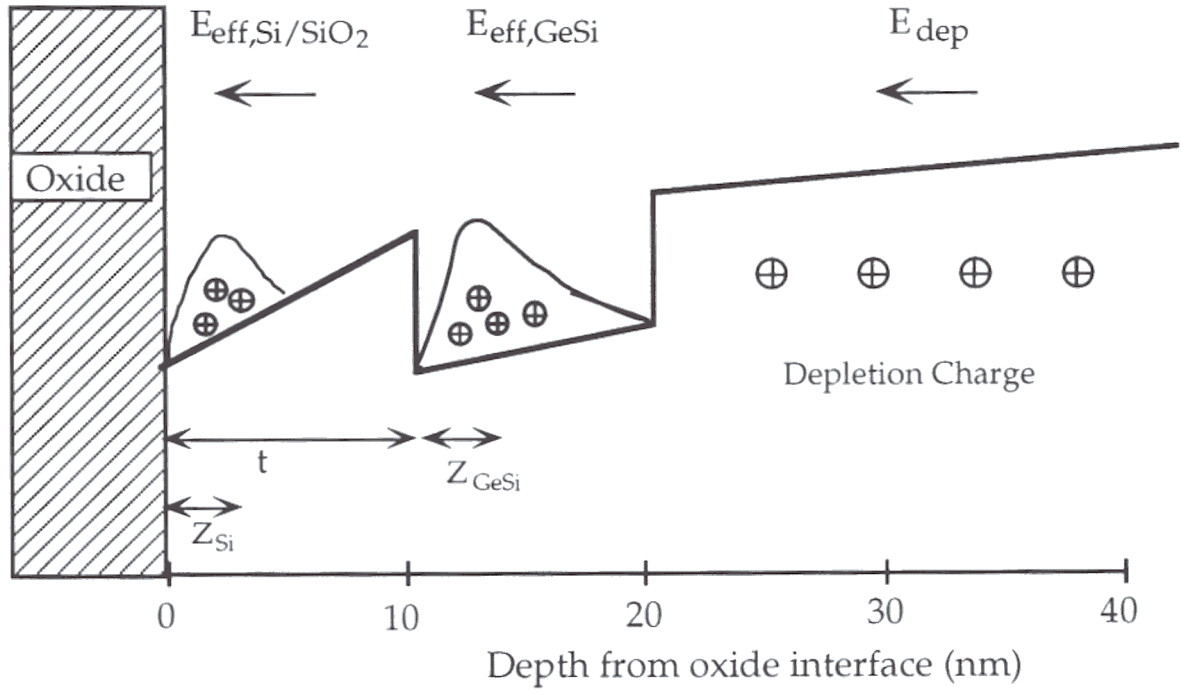


Figure 4.15 The two conduction channels in a MOS-HHMT, in the $Ge_xSi_{1-x}$ well and at the $Si/SiO_2$ interface, and their average separation of carriers and effective vertical fields are graphically depicted using the hole potential under the gate (simulation) and a schematic hole probability distribution.

less than that seen by the carriers at the $Si/SiO_2$ interface since the carriers at the $Si/SiO_2$ interface will feel the field due to the complete charge in the $Ge_xSi_{1-x}$ well ($Q_{GeSi}$) plus a fraction of the charge in the $Si/SiO_2$ channel ($Q_{Si/SiO_2}$)

Eq. 4.12
$$E_{eff,Si/SiO_2} = \frac{\left[Q_{dep} + Q_{Ge_xSi_{1-x}} + \eta\, Q_{Si/SiO_2}\right]}{\varepsilon_{Si}}$$

while the carriers in the $Ge_xSi_{1-x}$ well will feel only the field due to a fraction of the charge in the $Ge_xSi_{1-x}$ well (the charge at the $Si/SiO_2$ interface screens the gate potential)

Eq. 4.13 $$E_{eff,Ge_xSi_{1-x}} = \frac{\left[Q_{dep} + \eta\, Q_{Ge_xSi_{1-x}}\right]}{\varepsilon_{Si}}$$

The average separation of carriers from the $Si/SiO_2$ interface for the $Si/SiO_2$ channel will use the relation extracted from the quantum-mechanical simulation of the pMOSFET with the effective vertical field of Eq. 4.12 :

Eq. 4.14 $$Z_{avg,\ Si/SiO_2} = z\left(E_{eff,\ Si/SiO_2}\right)$$

In the $Ge_xSi_{1-x}$ well the average separation of carriers from the $Si/SiO_2$ interface will be be equal to the silicon spacer layer thickness ($t_{sp}$) plus the average separation of the carriers from the $Ge_xSi_{1-x}/Si$ interface To determine the average separation of the carriers in the $Ge_xSi_{1-x}$ well from the $Ge_xSi_{1-x}$ /Si interface it is assumed (for simplicity) that the potential well at the $Ge_xSi_{1-x}$ /Si interface can be treated as being the same as the potential at the $Si/SiO_2$ interface. This allows the use of the previously calculated average separation so that

Eq. 4.15 $$Z_{avg,\ Ge_xSi_{1-x}} = t_{sp} + z\left(E_{eff,\ Ge_xSi_{1-x}}\right)$$

This is an approximation The average separation should be less since the lower barrier at the $Si/SiO_2$ interface will allow the wavefunction to penetrate into the silicon spacer layer and reduce the average separation of carriers from the $Ge_xSi_{1-x}$ /Si interface

The surface mobilities for each channel are calculated by inserting the average separations from the $Si/SiO_2$ interface into the surface mobility formula Eq. 4.7 so that

Eq. 4.16 $$\mu_{surf,\ Si/SiO_2} = \beta\left[Z_{avg,\ Si/SiO_2}\right]^2 + \mu_0$$

and

Eq. 4.17 $$\mu_{surf,\ Ge_xSi_{1-x}} = \beta\left[Z_{avg,\ Ge_xSi_{1-x}}\right]^2 + \mu_0$$

The surface mobilities are combined with the bulk mobility term using Matthiessen's rule and a weighted average of the two channel mobilities is taken using Eq. 4.11

It is important to distinguish the *effective* mobility calculated in section 4.2.3 from the inversion layer mobility in $Ge_xSi_{1-x}$ / Si transistors (this model) The effective mobility assumes that the hole density under the gate is equal to $Q_{inv} = C_{ox}\cdot(V_g - V_t)$. For silicon FETs this is approximately correct, but for MOS-HHMTs the gate capacitance is less than $C_{ox}$ near threshold because of the additional series capacitance of the silicon spacer layer. Thus the number of carriers in the MOS-HHMT is overestimated by assuming that $C_{gate} = C_{ox}$ and the effective mobility will be less than the inversion layer mobility The effective mobility is useful for circuit modeling but obscures the physics of these devices

The effective vertical field in the two channels ($Ge_xSi_{1-x}$ well and the $Si/SiO_2$ interface) is different so for comparison to silicon MOSFETs the inversion layer mobilities are plotted versus the effective vertical field as given by Eq. 3.2

$$E_{eff} = \frac{\left[Q_{dep} + \eta\, Q_{inv}\right]}{\varepsilon_{Si}}$$

where $Q_{inv}$ is the total charge density of the two channels as predicted by simulation (Poisson solver)

### 4.2.4 Comparison with Experiment

The results of applying this model to the structure of sample 649, which had a 10.5 nm spacer and a $Ge_{.3}Si_{.7}$ well, at 290 K is shown in Figure 4.16 The inversion layer mobility extracted from the drain conductance of 97 μm gate length FETs is shown along with the inversion layer mobility predicted by the model For comparison, the effective mobility, extracted using

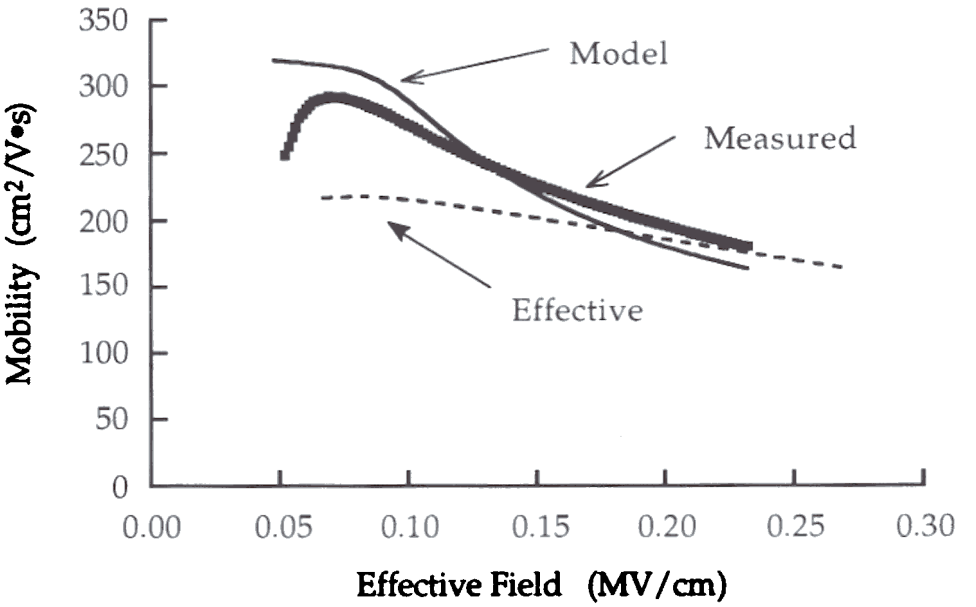


Figure 4.16 Inversion layer mobility for sample 649 at 290 K, which has a 10.5 nm spacer and a $Ge_{.3}Si_{.7}$ well. The measured mobility is extracted from experiment using hole densities taken from simulation and is compared to the mobility calculated with the model.

$Q_{inv} = C_{ox} (V_G - V_T)$, is also shown. The agreement between the inversion layer mobility calculated using the mobility model and that extracted from experimental measurements is within 10% across the whole range of effective vertical fields The deviation between the model mobility and the inversion layer mobility extracted from the long-channel FETs is predominantly at low effective vertical fields where most of the carriers are in the $Ge_xSi_{1-x}$ channel. This suggests that the estimate of the average separation of the carriers from the $Ge_xSi_{1-x}$ /Si interface (Eq. 4.15) could be too large or that one of the scattering mechanisms in the $Ge_xSi_{1-x}$ well (alloy scattering or $Ge_xSi_{1-x}$ /Si interface roughness) which were neglected, is important In Figure 4.16 it is also seen how the effective mobility underestimates the inversion layer mobility, especially at low effective vertical fields. The inversion layer mobility has a peak value of almost 290 $cm^2$/V-sec compared to a peak effective mobility of only 220 $cm^2$/V-sec. Also notice that the inversion layer

mobility decreases much more rapidly with effective vertical field than the effective mobility. This is expected since the fraction of carriers in the $Ge_xSi_{1-x}$ well is dropping as the effective vertical field (gate potential) increases

The inversion layer mobility extracted from the drain conductance and that predicted by the model for sample 646 at 290 K are shown in Figure 4.17 This sample had a 7.5 nm spacer and a $Ge_{.2}Si_{.8}$ well. The deviation at low effective vertical fields is somewhat larger (17%) than that seen with sample 649, but the agreement is still quite good

At low temperatures the model greatly overestimates the mobility Figure 4.18 shows the inversion layer mobility predicted by the model for sample 649 (10.5 nm spacer and a $Ge_{.3}Si_{.7}$ well) at 90 K is substantially larger than what was seen in the devices. To fit the data at 90 K an additional, scattering term must be incorporated into the estimates of the hole mobility in the $Ge_xSi_{1-x}$ well (corrected model curve in Figure 4.18). This additional term could be attributed to either alloy scattering or interface "roughness" scattering by the $Ge_xSi_{1-x}$/Si interface. Assuming a scattering mechanism that operated only on the carriers in the $Ge_xSi_{1-x}$ well, a best fit with the data was found with a scattering process that has a mobility component of 1470 $cm^2/V \cdot sec$ Similar results are seen while modelling sample 646 at 90 K

The addition of this mobility component would not be as noticeable at higher temperatures, because the other mobility terms are much lower, except when most of the carriers are in the $Ge_xSi_{1-x}$ well, i.e. at low effective vertical fields This is just what is seen (Figure 4.16 and Figure 4 7)

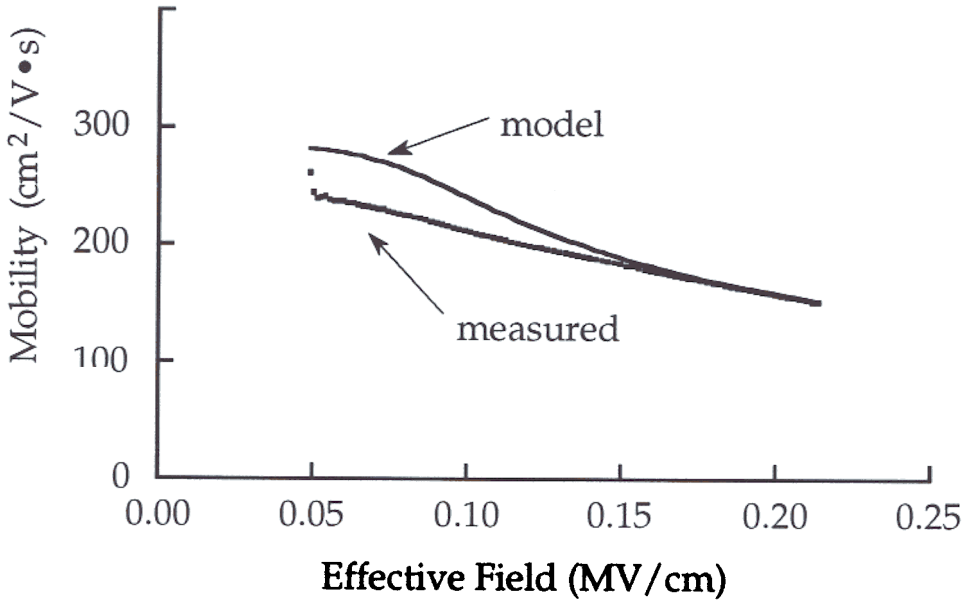


Figure 4.17 Inversion Layer mobility at 290 K for sample 646, which has a 7.5 nm spacer and a $Ge_{.2}Si_{.8}$ well. The measured mobility is extracted from experiment using hole densities taken from simulation compared to the mobility calculated with the model.

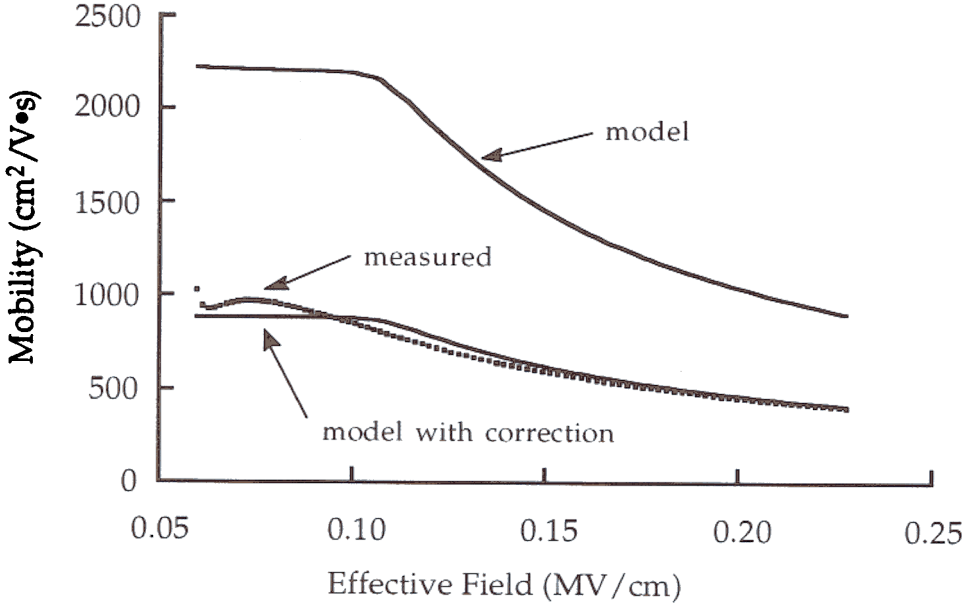


Figure 4.18 Inversion Layer mobility at 90 K for sample 649, which has a 10.5 nm spacer and a $Ge_{.3}Si_{.7}$ well. The model mobility greatly overestimates the inversion layer mobility extracted from experiment. Also shown is the corrected model.

The inversion layer mobilities seen with sample 649 (10.5 nm spacer and a $Ge_{.3}Si_{.7}$ well) are comparable to results seen in MOD-MOS devices with similar $Ge_xSi_{1-x}$ structures [13] (i.e. the same spacer layer thickness and germanium fraction in the well).

## 4.3 Optimizing MOS-HHMT Structure for Drain Conductance

In designing MOS-HHMT structures, the key device parameter to optimize is not the mobility or the the carrier density in the $Ge_xSi_{1-x}$ well, but rather the device conductance. The MOS-HHMT has two key structure parameters for optimizing the device conductance, the germanium fraction and the spacer layer thickness.

It is seen in section 3.2.4 that increasing the germanium fraction increases the number of carriers in the $Ge_xSi_{1-x}$ well The maximum germanium fraction is limited by the critical thickness of the $Ge_xSi_{1-x}$ layer as seen in section 4.2.4. Since the valence band offset at the top of the $Ge_xSi_{1-x}$ well is most important for confining carriers in the $Ge_xSi_{1-x}$ channel a graded $Ge_xSi_{1-x}$ well with the maximum germanium fraction at the top interface is attractive as a means of reducing the total stress in the film while maintaining a large fraction of carriers in the $Ge_xSi_{1-x}$ well. This approach has been used Verdonckt-Vandebroek et al to attain higher fractions of carriers in the $Ge_xSi_{1-x}$ well[11]

The optimal spacer layer thickness ($t_{SP}$) will be a tradeoff between increasing the mobility by moving the carriers farther away from the $Si/SiO_2$ interface as discussed in section 4.2 and weakening the capacitive coupling of the gate and thus reducing the number of carriers in the $Ge_xSi_{1-x}$ well (section 3.3.2). Since the effect of the spacer layer thickness on both the carrier density and the mobility has been explored a simple model is developed to describe the effect of the spacer layer thickness on the drain conductance.

### 4.3.1 The Model

The drain conductance in the linear region divided by the device width is modeled. MOSFET devices are usually optimized for transconductance in saturation, however the

saturation conductance is difficult to model because the carrier density across the channel is not uniform. Experimental work has shown (section 4.1) that there is a strong correlation between the performance enhancement seen in the linear region and in saturation for MOS-HHMTs. Therefore optimizing the drain conductance in the linear region may yield a reasonable estimate of MOS-HHMT structure optimization for digital applications. The units of conductance will be mS/mm (1mS = $10^{-3}\ \Omega^{-1}$).

The drain conductance in the MOS-HHMT will be split into two parts, the contribution due to the carriers in the $Ge_xSi_{1-x}$ well and the contribution due to carriers at the $Si/SiO_2$ interface

Eq. 4.18 $$\left(\frac{g_d}{W}\right) = \left[\frac{1}{L}\right]\left[Q_{Ge_xSi_{1-x}}\mu_{Ge_xSi_{1-x}} + Q_{Si/SiO_2}\mu_{Si/SiO_2}\right]$$

Eq 3.5 is used to calculate the charge density at crossover and it is assumed that the maximum charge density in the $Ge_xSi_{1-x}$ well is the same. Therefore

Eq. 4.19 $$Q^{max}_{Ge_xSi_{1-x}} \approx Q_{x\text{-}over} - \frac{\varepsilon_{Si}\,\Delta E_V}{q\,t_{sp}} - Q_{dep}$$

The calculations will be simplified by assuming that until the crossover charge density is reached all the holes are added to the $Ge_xSi_{1-x}$ well and the gate capacitance is equal to the series combination of the oxide and spacer layer capacitances. Above the crossover voltage Vxover ), defined as the gate voltage at which the crossover charge density is reached ( $V_{xover} = V_T - Q_{xover}/C_G$ ), all the holes are assumed to be added to the $Si/SiO_2$ interface and the gate capacitance is equal to the oxide capacitance ($C_{ox}$). The resulting hole density versus gate voltage and gate capacitance versus gate voltage are shown in Figure 4.19a,b These curves can may be compared with hole density vs. gate voltage calculated with the Poisson-solver in section 3.2.4 (Figure 3.7) and the with low frequency capacitance-voltage measurements in section 3.4.2 (Figure 3.17).

The charge densities in the $Ge_xSi_{1-x}$ well and at the $Si/SiO_2$ interface are then

$$Q_{Ge_xSi_{1-x}} = \frac{C_{ox}\,C_{SP}}{(C_{ox}+C_{SP})}(V_G - V_T)$$

$$Q_{Si/SiO_2} = 0$$

for $|V_G - V_T| \leq |V_{xover} - V_T|$

and

$$Q_{Ge_xSi_{1-x}} = Q_{x\text{-}over}$$

$$Q_{Si/SiO_2} = C_{ox}\left(V_G - V_{x\text{-}over}\right)$$

for $|V_G - V_T| > |V_{xover} - V_T|$.

The mobility of the two conduction channels is be determined using the inversion layer mobility model described in section 4.2, with no corrections made for alloy/surface roughness scattering A gate length of .0 μm, an oxide thickness of 12.5 nm, and operation at 290 K is assumed in these calculations.

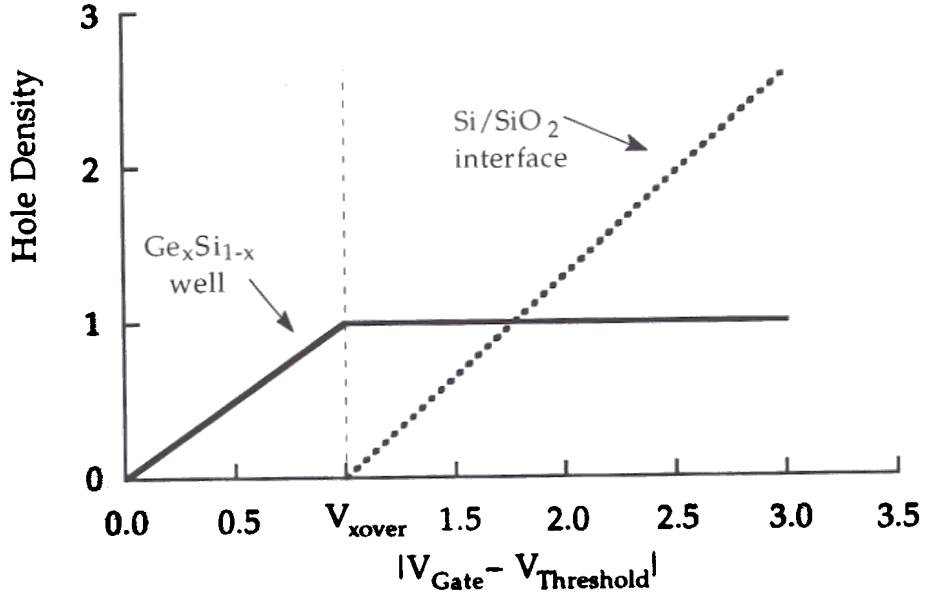


Figure 4.19a : Simplified hole density vs.gate voltage used in the conductance optimization model.

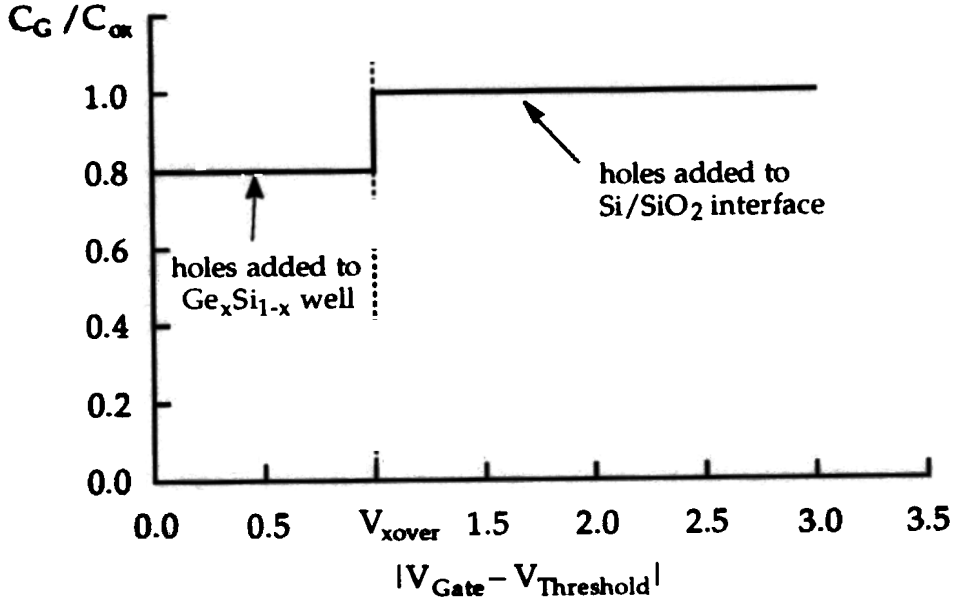


Figure 4.19b Simplified gate capacitance used in the conductance optimization model.

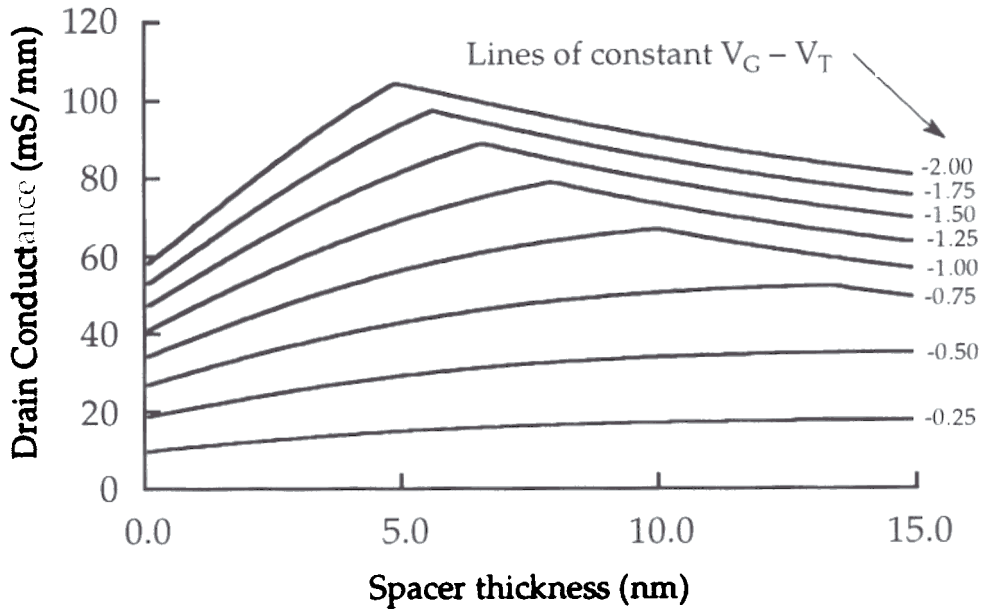


Figure 4.20 Optimization of the spacer thickness for drain conductance with a $Ge_{.3}Si_{.7}$ well at several different gate voltages above threshold

### 4.3.2 Results for Drain Conductance Optimization

In Figure 4.20 the calculated drain conductance for MOS-HHMTs with a $Ge_{0.3}Si_{0.7}$ well is plotted vs. spacer thickness for a series of different gate voltages above threshold The curves each have the same basic shape - the drain conductance rises with increasing spacer thickness until it reaches a peak value, then slowly declines thereafter The initial increase in the conductance is due to the fact that up to a certain spacer thickness all the holes are contained in the $Ge_xSi_{1-x}$ well and as the carriers are moved away from the $Si/SiO_2$ interface the carrier mobility increases This increase the mobility more than offsets the declining number of carriers due to the decreased gate capacitance The conductance reaches a maximum value when the spacer layer thickness is such that the crossover hole density is reached for that particular gate voltage and begins to decline for larger spacer thicknesses as an increasing fraction of the carriers are found in the $Si/SiO_2$ channel rather than in the $Ge_xSi_{1-x}$ channel. The maximum conductance does not come at

a single spacer thickness but depends on the gate bias. As the gate bias is increased the spacer thickness for maximum conductance becomes smaller. This is because at higher gate biases, thinner spacer thicknesses are necessary to have a crossover hole density large enough for all the holes to be located in the $Ge_xSi_{1-x}$ well

The optimal spacer thickness for a MOS-HHMT with a $Ge_{0.3}Si_{0.7}$ well, a 12.5 nm oxide and a gate bias of -1.0 volts above threshold is 10.0 nm has a drain conductance of 67 mS/mm. At -2.0 volts above threshold the optimal spacer thickness drops to 4.7 nm, with a drain conductance of 104.3 mS/mm. It is obvious that there is no spacer thickness that is optimal for the whole range of gate biases.

The drain conductance vs. gate voltage above threshold for several spacer thicknesses is shown in Figure 4.21 For drain currents just above threshold the devices with larger spacer layer thicknesses will have the higher drain conductance. As the bias increases the devices with a larger spacer thickness will have a smaller fraction of holes in the $Ge_xSi_{1-x}$ well, since their maximum (crossover) hole density is lower, and the relative performance enhancement drops off. Assuming that a MOS-HHMT is used in a digital circuit and is optimized for a gate voltage of 2.0 volts above threshold the optimum spacer layer thickness is approximately 4.7 nm. Such a device is predicted to have a 79% improvement in the drain conductance compared to a silicon MOSFET

If a smaller germanium fraction is used the optimal spacer thickness is smaller (Figure 4.22) This is because the smaller valence band offset requires a smaller spacer thickness to achieve significant carrier densities in the

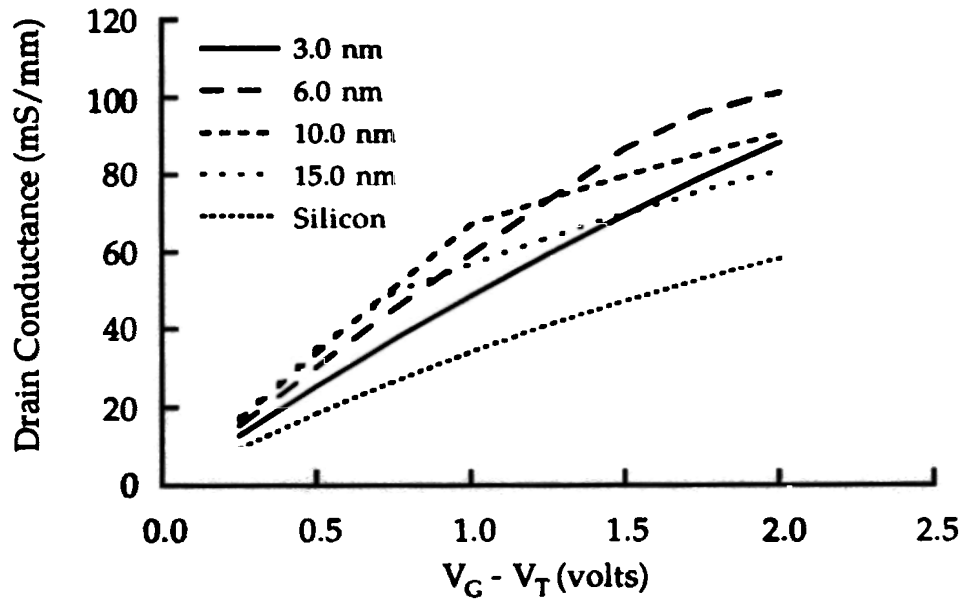


Figure 4.21 Drain conductance vs. gate voltage (normalized for threshold voltage) with a $Ge_{.3}Si_{.7}$ well and several spacer thicknesses.

$Ge_xSi_{1-x}$ well. The drain conductance improvement is less with a smaller germanium fraction because the fraction of carriers in the $Ge_xSi_{1-x}$ well is less for a given spacer layer thickness. For example the maximum drain conductance for a MOS-HHMT with a $Ge_{0.1}Si_{0.9}$ well at -1.0 volts above threshold is only 47.0 mS/mm ($t_{SP}$ = 2.8 nm), while a MOS-HHMT with a $Ge_{0.3}Si_{0.7}$ well can achieve a maximum conductance of 67.0 mS/mm at -1.0 volts above threshold ($t_{SP}$ = 10.0 nm) Likewise at -2.0 volts above threshold the maximum conductance for a MOS-HHMT with a $Ge_{0.1}Si_{0.9}$ well is only 71.6 mS/mm ($t_{SP}$ = .5 nm) compared to a maximum conductance of 104.3 mS/mm for a MOS-HHMT with a $Ge_{0.3}Si_{0.7}$ well ($t_{SP}$ = 4.9 nm)

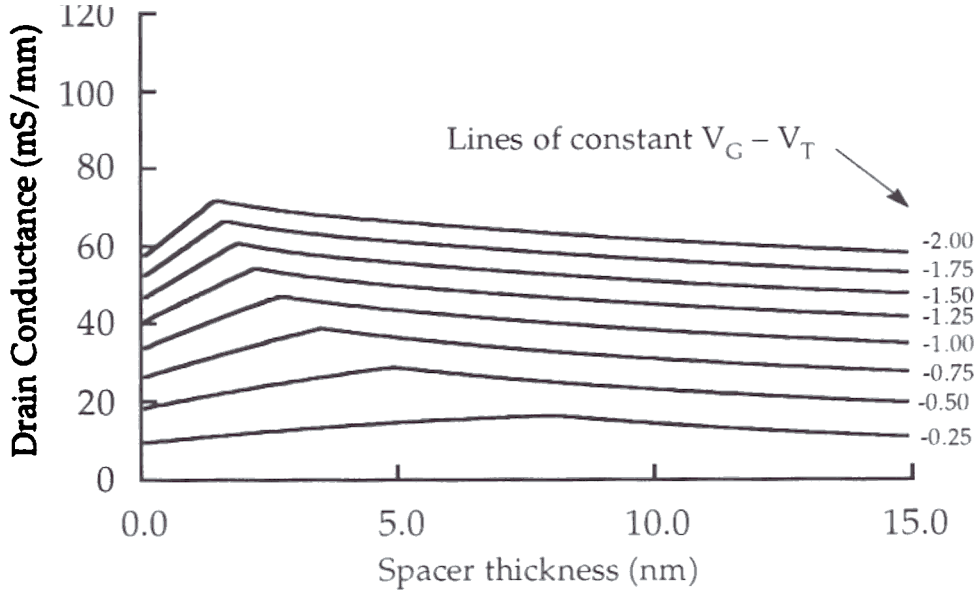


Figure 4.22 Optimization of the spacer thickness for drain conductance with a $Ge_{.1}Si_{.9}$ well at several different gate voltages above threshold

## 4.4 Summary

The placement of a $Ge_xSi_{1-x}$ layer underneath the gate of a pMOSFET does lead to an increased drain conductance. A 50% increase in the room temperature drain conductance over silicon devices is seen in MOS-HHMTs with a 10.5 nm silicon spacer layer and a $Ge_{.3}Si_{.7}$ well The relative performance enhancement of the MOS-HHMTs increases, relative to the silicon MOSFETs, with decreased temperature At 90 K MOS-HHMTs with a 10.5 nm silicon spacer layer and a $Ge_{.3}Si_{.7}$ well had a 120% higher drain conductance then the silicon MOSFET control devices

The mobility enhancement of MOS-HHMTs can be modeled at room temperature to result from reduced scattering with the $Si/SiO_2$ interface. At low temperatures (90 K) an additional scattering term, associated with the carriers in the $Ge_xSi_{1-x}$ well, must be added It is speculated that this additional scattering term may be the result of alloy scattering or $Ge_xSi_{1-x}$ /Si interface roughness scattering

A simple model for optimization of the drain conductance in the linear region of operation predicts that the optimal spacer width for a MOS-HHMT with a $Ge_{.3}Si_{.7}$ well is 4.7 nm for device operation at a gate voltage two volts above threshold. This is an almost 80% improvement in the drain conductance over a silicon p-MOSFET.

## 4.5 Future Considerations

There are still many questions to be answered regarding the material and electronic properties of the strained films $Ge_xSi_{1-x}$ films and the potential for the introduction of MOS-HHMTs into CMOS circuits. These questions are not unrelated and may not be easy to answer

One question regards the effective mass in strained $Ge_xSi_{1-x}$ films. People suggests[14] that the hole effective mass near the zone center (k=0) can be estimated from strain measurements on silicon and germanium From this he estimates an in-plane Shubnikov-de Haas (SdH) mass of $\approx 0.2m_0$ for 20% germanium alloys. He then explains that the SdH mass of $0.32 \pm 0.3m_0$ measured in Reference [15] was the result of the non-parabolicity of the valence bands in strained $Ge_xSi_{1-x}$. A schematic representation of the valence band structure of strained $Ge_xSi_{1-x}$ is shown in Figure 4.23. The hole effective mass increases rapidly as one moves away from the zone center due to the mutual repulsion between the strain split valence bands. Since transport is

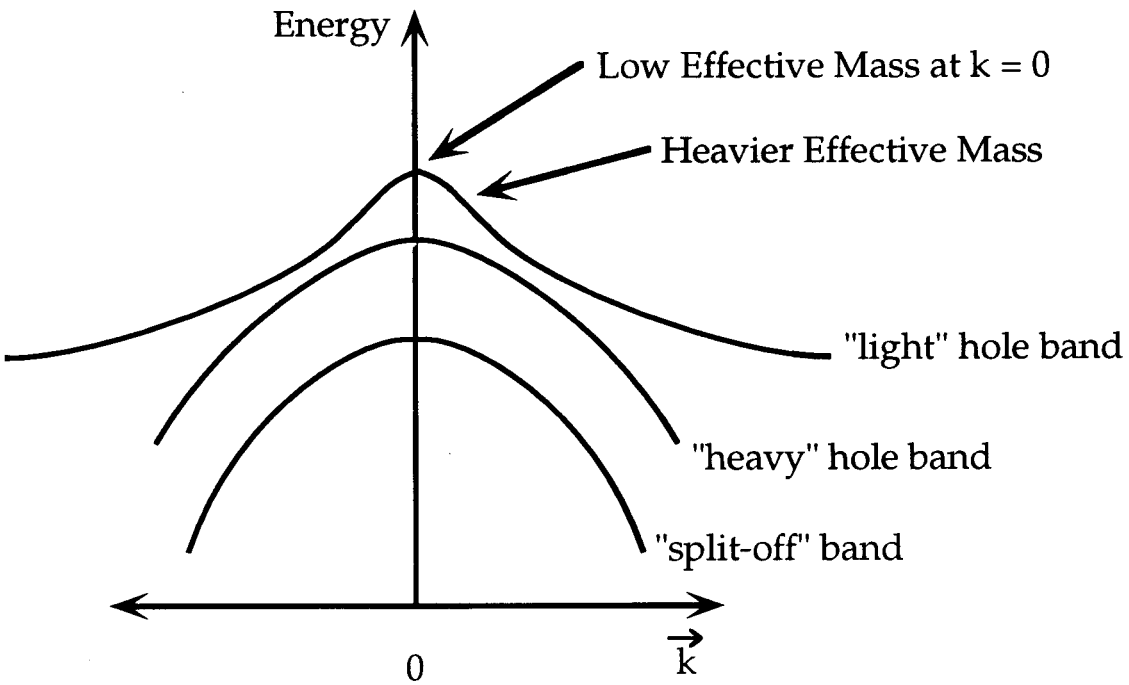


Figure 4.23 : Schematic of strained $Ge_xSi_{1-x}$ valence bands. The degeneracy at the zone center (k = 0) is broken by the strain. The valence bands are highly non-parabolic.

governed by the effective mass at the *high* energy tail of the holes, the effect of a lower effective mass near the zone center will be reduced.

At low electric fields the carrier velocity is proportional to the applied field (i.e. $\mathbf{v} \alpha \mathbf{E}$ ). The proportionality constant is the mobility. All the measurements in this thesis were made in this low field regime. As the electric fields approach a value of approximately $10^4$ V/cm the carrier velocities in silicon and germanium begin to flatten out and become practically independent of the applied field. This high field phenomena is referred to as velocity saturation. With gate lengths of less than one micron FETdevice operation is moving into this high field regime. The question is : "Will the mobility enhancement seen in MOS-HHMTs at low electric fields still be present as the devices enter into the high field regime ?"

The answer is not at all clear but there are some indications that an improved performance may still be seen at high fields.

1. Performance enhancement of the MOS-HHMTs over silicon FETs was seen to decrease by Kesan et al [16] as the channel length is reduced to 0.5 μm, but is still present.
2. The modeling of Hinckley et al suggests that of the removal of the valence band degeneracy due to the strain in the $Ge_xSi_{1-x}$ layer reduces the number of states to scatter into should result in an enhanced hole velocity at all fields [7].
3. It is possible that velocity overshoot may be seen with shorter gate lengths. If so the MOS-HHMTs will continue to have improved performance because of their superior low-field mobilities.

Verdonckt-Vandebroek et al report that the hole density in $Ge_xSi_{1-x}$ well can be increased by using a modulation doped structure [11]. The device basically operates like a HEMT except that it uses an oxide gate to modulate the charge density at the $Ge_xSi_{1-x}$/Si heterojunction. They claimed that this structure had approximately three times the number of holes in the $Ge_xSi_{1-x}$ well as a MOS-HHMT with a comparable threshold voltage. The inversion layer mobilities were almost identical to those seen in this thesis for very similar $Ge_xSi_{1-x}$ structures (except for doping). This increased carrier density should lead to an improved conductance and looks to be an attractive area of device research.

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## Summary

Good quality epitaxial silicon and $Ge_xSi_{1-x}$ films can be grown at low temperatures in a low pressure epitaxial reactor (6 torr) if care is taken to reduce the partial pressures of oxygen and water vapor. Precise temperature control in the reaction rate limited growth regime (T<800° C) is essential because the growth rate at these temperatures is exponentially dependent on temperature. Infrared transmission has proven to be a reliable and highly accurate method for monitoring and controlling the temperature in this range.

It is found that the addition of germane to dichlorosilane catalyzes the epitaxial growth rate in the reaction rate limited growth regime allowing reasonable $Ge_xSi_{1-x}$ growth rates to be achieved at temperatures down to 605° C. In the reaction rate limited growth regime boron doping kinetics are determined by kinetics rather than by equilibrium considerations (solid solubility).

The utility of epitaxially grown $Ge_xSi_{1-x}$ / Si heterojunctions is demonstrated with an application to an improved pMOS device, the MOS-gated High Hole Mobility Transistor (MOS-HHMT). Hall measurements and quasi-static C-V measurements demonstrate that an inversion layer can be formed in the $Ge_xSi_{1-x}$ well of this type of structure. Electrical measurements demonstrated a 50% increase in the room temperature drain conductance, over silicon devices, for a MOS-HHMTs with a 10.5 nm silicon spacer layer and a $Ge_{.3}Si_{.7}$ well. The relative performance enhancement of the MOS-HHMTs increases, relative to the silicon MOSFETs, with decreased temperature indicating that a decreased surface scattering rather than a reduction in the effective mobility is responsible for the improved performance. At 90 K MOS-HHMTs with a 10.5 nm silicon spacer layer and a $Ge_{.3}Si_{.7}$ well had a 120% higher drain conductance then the silicon MOSFET control devices.

The mobility enhancement of MOS-HHMTs can be modeled at room temperature to result from reduced scattering with the $Si/SiO_2$ interface. At low temperatures (90 K) an additional scattering term, associated with the carriers in the $Ge_xSi_{1-x}$ well, must be added. It is speculated that this additional scattering term may be the result of alloy scattering or $Ge_xSi_{1-x}$ /Si interface roughness scattering.

A simple model for optimization of the drain conductance in the linear region of operation predicts that the optimal spacer width for a MOS-HHMT with a $Ge_{.3}Si_{.7}$ well is 4.7 nm for device operation at a gate voltage two volts above threshold. This is an almost 80% improvement in the drain conductance over a silicon p-MOSFET.

# Appendix I : Symbols

As often as possible the most common symbol was used in the equations. Also an attempt was made to use each symbol only once and define it just before or after its first use. The symbols are listed here alphabetically with the Greek alphabet first.

$\alpha$ absorption coefficient

$\beta$ firring parameter for surface scattering

$\Delta E_n$ band offset of band n

$\delta$ misfit accomodated by dislocations

$\varepsilon$ misfit accomodated by strain

$\varepsilon_o$ dielectric permitivity of free space

$\varepsilon_{Si}$ dielectric constant of silicon

$\eta$ effective field weighting factor

$\theta$ fraction of open sites on a surface

$\mu$ mobility

$\nu$ Poisson's ratio

$\nu$ frequency

$\tau$ relaxation time

$\phi$ angle

$\phi_s$ surface potential

$\phi_F$ Fermi potential in the bulk

$\phi_G$ potential at $Ge_xSi_{1-x}$ /Si interface

$|\Psi|^2$ carrier distribution probability

**********

$A_1$ variational fitting parameter

$a_o$ epitaxial layer relaxed lattice constant

$a_s$ substrate lattice constant

$b$ Burgher's vector

$b_o$ variational fitting parameter

$C_1$ variational fitting parameter

$C_{ox}$, $C_{dep}$, $C_{sp}$ and $C_G$ oxide, depletion layer, spacer layer and gate capacitance

$C_n$ concentration subscript refers to the species or location

$D$ diffusion constant

$E_\delta$ strain energy from dislocation

$E_\varepsilon$ elastic strain energy

$E_0$, $E_1$, $E_2$ subband energies in an MOS inversion layer

$E_a$ activation energy

$E_G$ bandgap

$E_{sp}$ electric field across the spacer layer

$F$ flux

$f$ misfit

modified hydrogendesorption probability for a $Ge_xSi_{1-x}$ surface

$G$ shear modulus

$g_D$ drain conductance

$h$ epitaxial layer thickness

$h^*$ equilibrium critical thickness

gas phase mass transfer coefficient

$I$ intensity or current

$J$ quantized momentum

$J$ growth model parameter

$K_{Si}$, $K_{Ge}$ equilibrium reaction constants

$k$ momentum vector

$k$ Boltzman's constant

$k_n$ reaction rate constant of species n

L gate length

$L_o$ other optical losses

mass of nucleous n

m mass

m effective mass

N density

$N_A$, $N_B$ concentration of constituents A and B in a film

donor density

$N_s$ normallized transmission of reference wafer

$N_x$ normallized transmission

$P_n$ partial pressure of gas n

$p_n$ hole density in location n

depletion charge density

$Q_F$ oxide fixed charge

inversion charge density

q electronic charge

R distortion radius of a dislocation

$R_s$ series resistance

adsorption rate

$R_{collision}$ collision rate

growth rate

S subthreshold swing

S spacing between misfit dislocations

T temperature

energy loss from inelastic collisions with nuclei

time

$t_{ox}$ oxide thickness

$t_s$ reference wafer thickness

$t_{sp}$ silicon cap or spacer layer thickness

$t_x$ wafer thickness

$V$ dislocation velocity

$V_n$ voltage at node n

threshold voltage

$V_{x\text{-}over}$ gate voltage when number of holes at the $Si/SiO_2$ interface equals the number of holes in the $Ge_xSi_{1-x}$ well.

$W$ gate width

$w$ stagnant layer thickness

$x$ germanium fraction

$Y_n$ collision rate constant for species n

$z$ or $Z$ depth

average separation of carriers from the interface

# Appendix II : One Dimensional Poisson Solver for a MOS capacitor

## I. Overview

This appendix describes the details of the program *model.π* which finds the electrostatic solution for a MOS capacitor with a given gate voltage. A flow diagram of the program is shown on the next page The squares correspond to functions or key segments of the main() function found in the file model.c The diamonds correspond to key logic steps that direct the program flow Finally the arrows signify the flow of the program from section to section

The program code is written in ANSI standard C, which was chosen because of its portability and flexibility in handling input and output The code was originally written on a Silicon Graphics Iris™ workstation but later moved to an Apple Macintosh

In the following sections the key aspects of the program are discussed and then in the last section the key C code is included (data input and output are excluded)

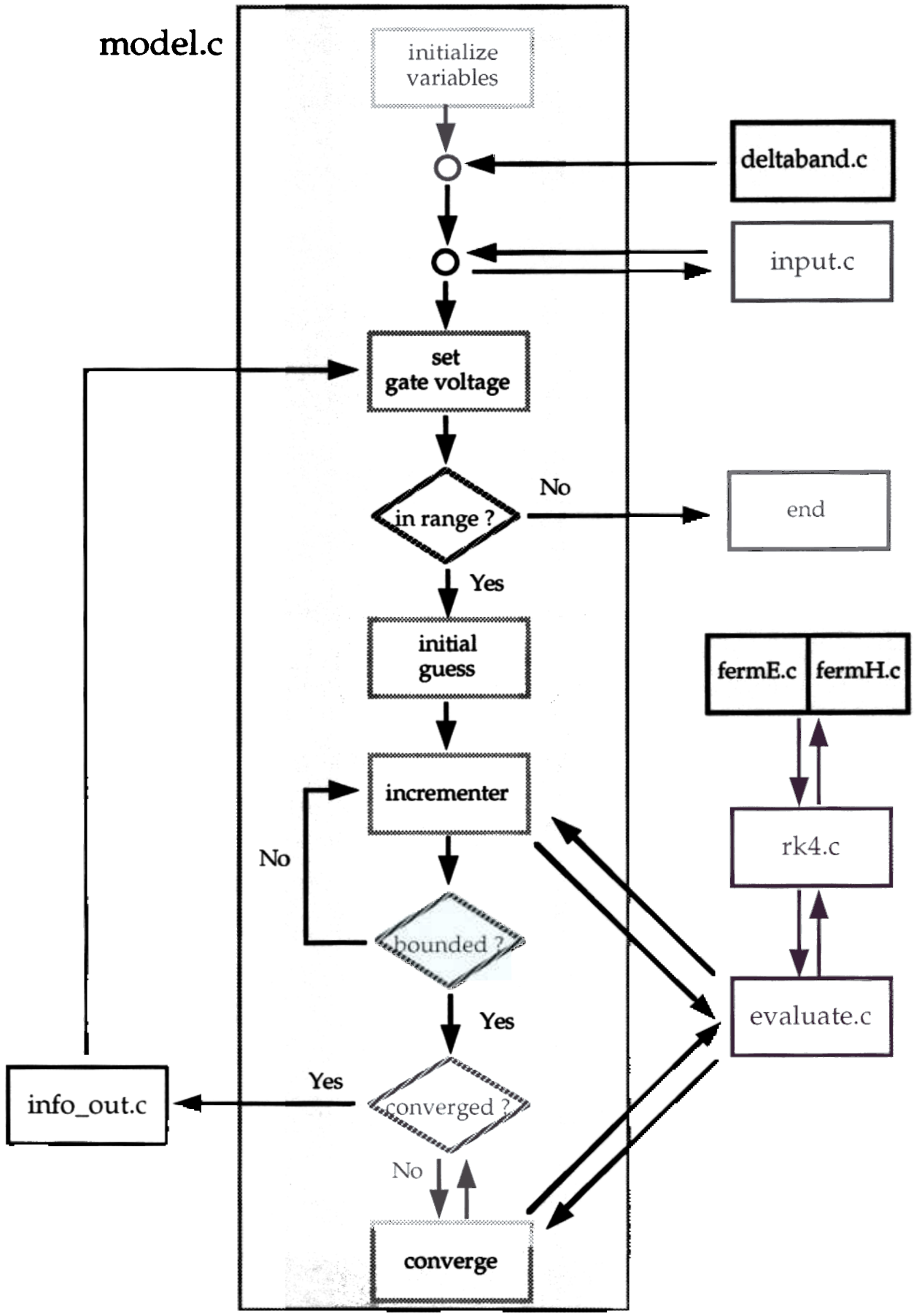
## II. Comments on Key Aspects of the Program

### A. deltaband.c

The bandgap offset data as calculated by Van de Walle and Martin[1] is entered in for germanium fractions ranging form 0 to 0.5 in increments of 0.05 Intermediate germanium fractions are handled by interpolating between these points. The three valence bands and the two conduction sub-bands are all used The data is read into the arrays Ev1[], Ev2[], Ev3[], Ec1[] and Ec2[]

### B. Data Input

Three groups of data are input for the structure - oxide structure, semiconductor structure and the bias conditions


model.c
initialize variables
deltaband.c
input.c
set gate voltage
in range ?
No
end
Yes
initial guess
fermE.c
fermH.c
incrementer
No
rk4.c
bounded ?
Yes
evaluate.c
info_out.c
Yes
converged ?
No
converge

The thickness, fixed charge and the interface states are entered by the user interface states are treated simply as a fixed number of states per eV

The semiconductor is entered in as a series of layers with a constant germanium fraction and doping level. In addition the thickness and the size of the step for the 4th order Runge-Kutta technique are input Typically small values are used for the step size are used near the surface (1-2 Å) where most of the carriers are located with progressively larger step sizes going deeper into the bulk to reduce computation time. The sum of the individual layer thicknesses should be ≈50% larger than the depletion layer width to converge properly. The program assume that the semiconductor is *not* doped degenerately since Boltzman's approximation is used in order to determine the Fermi level in the bulk

The bias conditions consist of the the initial, final and incremental gate voltages as well as the temperature of operation The program assumes that the dopants are completely ionized

C. Initial Guess of the Surface Potential

For a given gate voltage an initial guess is made at the surface voltage corresponding surface electric field is determined by the potential difference across the gate and the oxide thickness The previous solution is used as the initial guess except, of course, for the first gate bias point The initial guess for the first gate bias depends on the value of the first gate bias and the gate voltage increment The details are in the code

D. Evaluate.c

The function evaluate.c is given the surface potential and the surface electric field and is responsible for using the 4th order Runge-Kutta (rk4.c) function to propagate the solution for Poisson's equation for this set of initial conditions. It feeds rk4.c the appropriate doping density, germanium fraction, potential, step size and electric field. If the value of the potential exceeds ±1.5 volts it assumes the solution is diverging and cuts off the

evaluation It returns an integer to model.c which indicates whether the given surface potential and field are correct or how it deviates

| | |
|---|---|
| q=0 | potential at *infinity* (in the bulk) deviates from zero by less than the preset criteria, typically 1 mV |
| q=-1,-2 | potential at *infinity* is greater than zero and larger than the convergence criteria. |
| q=+1,+2 | potential at *infinity* is less than zero and larger than the convergence criteria |

**E. rk4.c**

This function uses the 4th order Runge-Kutta method to propagate the solution to Poisson's equation across a given step (distance). The function is specifically set up to propagate the solution Poisson's equation and calls the functions fermE.c and fermH.c which calculate the electron and hole density.

**F. Fermi Statistics**

Fermi-Dirac statistics are used to calculate the electron and hole density in the functions fermE.c and fermH.c. An approximate form is used in place of the Fermi-Dirac integral[2] The error is not supposed to exceed 0.4% for any position of the Fermi level

$$F_{1/2}(\eta) \approx \frac{1}{2}\sqrt{\pi}\left[\frac{3}{4}\sqrt{\pi}\,a(\eta)^{-3/8} + e^{-\eta}\right]^{-1}$$

where $$a(\eta) = \eta^4 + 33.6\eta\left\{1 - 0.68e^{\left[-0.17(\eta+1)^2\right]}\right\} + 5C$$

The electron and hole density is calculated using each of the valence and conduction bands separately for $Ge_xSi_{1-x}$ layers and appropriately weighting the density of states.

**G. Incrementer**

The incrementer steps the surface potential until the value of q returned from evaluate.c changes sign or converges (q=0) The previous value of the surface potential and the current surface potential then form upper and lower limits for the surface potential. These limits for the surface potential are passed down to the convergence routine

### H. Convergence

The convergence routine sends the midpoint between the upper and lower limits on surface potential to the function evaluate.c. The return value of q is used to decide whether the midpoint will be used to replace the upper or lower bound on the surface potential

If q>0 midpoint value for the surface potential is higher than the correct value.

If q<0 midpoint value for the surface potential is less than the correct value.

The convergence routine will keep dividing the upper and lower bounds on the surface potential in half until the solution for the surface potential and electric field meets the convergence criteria of $phi_{bulk} < \pm 1mV$.

## III. Program Code

```
#include "function.h"

/* External Variable Declarations */
double Tox, depth[ARRAY], h[ARRAY], doping[ARRAY];
double Qfixed[ARRAY], Qfast[ARRAY];
double Ge[ARRAY], Temp;
double Phi,E;
double Vmin,Vmax,Vstep;

main()
{       /* Variable declarations */

    extern double Tox, depth[], h[], doping[];
    extern double Qfixed[], Qfast[];
    extern double Ge[], Temp;
    extern double Phi,E;
    extern double Vmin,Vmax,Vstep;
    int n,low;
    int q,llast;
    double charge[ARRAY],elec[ARRAY],hole[ARRAY],quad,
    double Phizero,Phizero_previous,increment;
```

```
double Pfloor,Pceiling,del_bot,del_top,delta,sumcharge;
double gap,Kx;
double Esurf,Ecinf,Evinf,gummel;

/* setting up file variables */
FILE *stat;
char notes[LEN];
FILE *rat;
char carr[LEN];
FILE *gate;
char kind[5];

/* variables used for GeSi bandgap offsets */
double Ev1[12],Ev2[12],Ev3[12],Ec1[12],Ec2[12];
double Vg,Gehigh,Gelow,interp,delEv,delEc1,delEc2;

int xlow,xhigh;
```

```
/* setting up notes file */
 strcpy(notes,"notes");
 stat=fopen(notes,"w");
/* Titles for Vgate File */
 strcpy(kind,"Vgate");
 gate = fopen(kind,"a");

 fprintf(gate,"Gate_Voltage Holes_in_Ge Holes_in_Si Integrated_Holes \
        Total_Charge\n");

 fclose(gate);
```

*/* call to input.c */*

```
/* inputs device struture interactively */
 llast = input(stat);
```

*/* inputing bandgap offset data */*

```
deltaband(Ev1,Ev2,Ev3,Ec1,Ec2);
```

```
/* calculates the bandgap for the given temperature */
    gap = 1.170 - (4.73e-4)*pow(Temp,2)/(Temp + 636);

/* sets boundary conditions at depth["infinity"] */
    if(doping[llast]<0)
    {
            Evinf = K * Temp * log(-doping[llast]/NV);
            Ecinf = Evinf + gap;
    }
    else if(doping[llast]>0)
    {
            Ecinf = -K * Temp * log(doping[llast]/NC);
            Evinf = Ecinf - gap;

    fprintf(stat,"\nEcinf=%f\tEvinf=%f\n",Ecinf,Evinf);
    fclose(stat);

/* beginning of main loop which increments Vg */
    Phizero = 99;
    for(Vg=Vmin; fabs(Vg)<=fabs(Vmax); Vg +=(Vstep))
    {
            printf("Vg is %f\n",Vg);

    /* Initial guess routine*/
            if(Phizero == 99)
            {
                    if((Vg<=0) && (Vstep<0))
                    {
                            Phizero = +0.05;
                            increment = -0.05;
                    }
                    else if((Vg<=0) && (Vstep>0))
                            {
                            Phizero = -1.2;
                            increment = +0.05;
                    }
                    else if((Vg>=0) && (Vstep<0))
                    {
                            Phizero = +1.2;
                            increment = -0.05;
                    }
```

```
        else if((Vg>0) && (Vstep>0))
        {
                Phizero = -0.5;
                increment = -0.05;
                }
        else if(Vg==0)

        {
                printf("Program ended since Vstep = 0.0");
                return;
        }
        else
        {
                printf("Problem in initial Phizero set");
                return;
        }
}
else   /* else use value from previous vstep */
        increment = Phizero - Phizero_previous;
```

```
Phizero_previous = Phizero;
```

*/* Incrementer : sets upper and lower bounds for Phi[surface] */*

```
if(increment<0)
        q=-33;
else
        q=+33;
while((q*increment)>0)
{
        Pfloor=Phizero;
        Phizero += increment;
        Phi = Phizero;
        E = (Vg - Phizero) * (KOX/KSI)/Tox;
        q = evaluate(Evinf, Ecinf, llast, Ev1, Ev2, Ev3, Ec1,Ec2);
        Pceiling= Phizero;
}
```

***/* convergence routine */***

```
        while(q!=0)
        {
```

```
Phizero = (Pceiling - Pfloor)/2 + Pfloor;
E = (Vg - Phizero) * (KOX/KSI) / Tox;
Phi = Phizero;
q = evaluate( Evinf, Ecinf, llast, Ev1, Ev2, Ev3, Ec1, Ec2);
if(q==1)
{
        if(increment<0)
                Pceiling = Phizero;
        else
                Pfloor = Phizero;
        delta = 99;
}
else if(q==2)
{
        if(increment<0)
                Pceiling = Phizero;
        else
                Pfloor = Phizero;
        delta=Phi;
}
else if(q==-1)
{
        if(increment<0)
                Pfloor = Phizero;
        else
                Pceiling = Phizero;
        delta = -99;
}
else if(q==-2)
{
        if(increment<0)
                Pfloor = Phizero;
        else
                Pceiling = Phizero;
        delta =Phi;
}
else if(q==0)
{
        printf("Yeh!! I converged for voltage = %f\n",Vg);
        delta = Phi;
}
else /* Error case */
{
```

```
                    printf("\n\nfine tuning out of whack\n");
                    printf("%d %f %f\n",q,Phi,E);
                }
            }
```

```
    /* Reinitialize Phi & E to the proper starting values for convergence */
        Phi = Phizero;
        E = (Vg - Phizero)*(KOX/KSI)/Tox;

    /* basic results for notes */

    /* call to info_out.c */

        Esurf = info_out(Evinf,Ecinf,llast,Ev1,Ev2,Ev3,Ec1,Ec2,Vg,&gummel);

        stat=fopen(notes,"a");
        fprintf(stat,"\n\nVg = %f\n",Vg);
        fprintf(stat,"Surf. voltage is determined to be %f\n",Phizero);
        fprintf(stat,"Phi[inf] is %f\n",Phi);
        fprintf(stat,"Surf. field is %e",(Vg-Phizero)*(KOX/KSI)/Tox);
        fprintf(stat,"  surf field from integrated charge is %e\n",Esurf);

        fprintf(stat,"%%Δ Esurf is %e\n",(Esurf - ((Vg-    \
            Phizero)*(KOX/KSI)/Tox))*100/Esurf);
        fprintf(stat,"\nGummel number for holes is %e cm-2\n",gummel);
        fclose(stat);

    } /**************END OF VG LOOP*************/
    return;
}


int evaluate( double Evinf, double Ecinf,int llast, double Ev1[], double Ev2[], \
        double Ev3[], double Ec1[],double Ec2[])

    extern double Tox, depth[], h[], doping[];
    extern double Qfixed[], Qfast[];
    extern double Ge[], Temp;
    extern double Phi,E;
    FILE *errur:
```

```
        char argg[LEN];
        int q,p;
        double ldepth, Qss, epsilon,slope;
        double Kx, Gelow, Gehigh, interp;
        int xlow, xhigh;
        double delEv1, delEv2, delEv3, delEc1,delEc2;
        double Phim1, Phim2, Phim3;

        strcpy(argg,"argg");
        q=0;
        ldepth = 0.0;
        q = 0;
        for(p=0;p<=llast && q == 0;p++)
        {
    /* Interface Effects */
                Qss = Qfixed[p] - Qfast[p] *  Phi;
    /* Electric Displacement Field Adjust */
                if(Ge[p-1]==0.0 && Ge[p]>0.0)
                {
                        Kx = (Ge[p])*KGE + (1.0 - Ge[p])*KSI;
                        E *= KSI/Kx;
                }
                else if(Ge[p-1]>0.0 && Ge[p]==0.0)

                        Kx = (Ge[p])*KGE + (1.0 - Ge[p])*KSI;
                        E *= KSI/Kx;


                epsilon = (Ge[p] * KGE + (1.0 - Ge[p])*KSI)*EO;

    /* Entering bandgap offset data */
                xlow = 20*Ge[p];
                xhigh = xlow + 1;
                Gelow = xlow/20.0;
                Gehigh = xhigh/20.0;
                interp = (Ge[p] - Gelow)/(Gehigh - Gelow);

                delEv1 = interp * (Ev1[xhigh] - Ev1[xlow]) + Ev1[xlow];
                delEv2 = interp * (Ev2[xhigh] - Ev2[xlow]) + Ev2[xlow];
                delEv3 = interp * (Ev3[xhigh] - Ev3[xlow]) + Ev3[xlow];
                delEc1 = interp * (Ec1[xhigh] - Ec1[xlow]) + Ec1[xlow];
                delEc2 = interp * (Ec2[xhigh] - Ec2[xlow]) + Ec2[xlow];
```

```
/* Interface States Accounted for */
        if(Qss!=0.0)
        {
                E += Qss/epsilon;
                Phi -= E * (1e-8);
        }

/* rk4 across the region */
        if(p<llast)  /* for all layers except the last */
        {
                ldepth = 0.0;
                q = 0;
                while(ldepth<depth[p] && q==0)
                {

                        rk4(Evinf, Ecinf, delEv1, delEv2, delEv3, \
                                delEc1,delEc2, epsilon, p);
                        if(Phi>1.5)
                                q = -1;
                        else if(Phi<-1.5)
                                q = 1;
                        else
                                ldepth +=h[p];
                }
        }
        else  /* for the last layer of the structure */
        {
                ldepth = 0.0;
                Phim1 = 0.0;
                Phim2 = 0.0;
                Phim3 = 0.0;
                while(ldepth<depth[p] && q == 0)
                {
                        Phim3 = Phim2
                        Phim2 = Phim1
                        Phim1 = Phi;

                        rk4(Evinf, Ecinf, delEv1, delEv2, delEv3, \
                                delEc1,delEc2, epsilon, p);
                        if(Phi>1.5)
                                q = -1;
                        else if(Phi<-1.5)
                                q = 1;
                        else
```

```
                ldepth += h[p];


        }
    /* evaluating the results of the numerical solution for the given surface voltage */
        if(q == 0 && fabs(Phi) < CONVERGE)
                q = 0;
        else if(q == 0 && fabs(Phi) >= CONVERGE){
                if(Phi > 0.0 )
                        q = -2;
                else if(Phi < 0.0 )
                        q = 2;
                else
                {
                        q = 99;

        }
        return q;
    }  /* end of evaluate function */

    int rk4(double Evinf, double Ecinf, double delEv1, double delEv2,      double
delEv3, double delEc1,double delEc2, double epsilon,int l)

        extern double Tox, depth[ARRAY], h[ARRAY], doping[ARRAY];
        extern double Qfixed[ARRAY], Qfast[ARRAY];
        extern double Ge[ARRAY], Temp;
        extern double Phi,E;

        double charge, field, pot, K1E, K2E, K3E, K4E, K1P, K2P, K3P, K4P;

        charge = doping[l] + fermH(Phi,Evinf,delEv1,delEv2,delEv3,Temp) -
                        fermE(Phi,Ecinf,delEc1,delEc2,Temp);
        K1E = charge/epsilon;
        K1P = -E;

        field = E + (charge/epsilon)*(h[l]/2.0);
        pot = Phi - field*h[l]/2.0;
        charge = doping[l] + fermH(pot,Evinf,delEv1,delEv2,delEv3,Temp) -
                \ fermE(pot,Ecinf,delEc1,delEc2,Temp);
        K2E = charge/epsilon;
        K2P = -field;
```

```
    field = E + K2E*h[l]/2.0;
    pot = Phi - field*h[l]/2;

    charge = doping[l] + fermH(pot,Evinf,delEv1,delEv2,delEv3,Temp) -
                    fermE(pot,Ecinf,delEc1,delEc2,Temp);
    K3E = charge/epsilon;
    K3P = -field;

    field = E + K3E*h[l];
    pot = Phi - K3P*h[l];
    charge = doping[l] + fermH(pot,Evinf,delEv1,delEv2,delEv3,Temp) -
          \ fermE(pot,Ecinf,delEc1,delEc2,Temp);
    K4E = charge/epsilon;
    K4P = -field;

    E += (h[l]/6.0)*(K1E + 2.0*K2E + 2.0*K3E + K4E);
    Phi += (h[l]/6.0)*(K1P + 2.0*K2P + 2.0*K3P + K4P);
} /* end of rk4 function */


double fermE(double pot,double Ecinf,double delEc1,double delEc2,double
        Temp)

    double eta,fermi,aeta;
    double density;


/*** Doubly degenerate subbands*******/
    eta = -(Ecinf+delEc1-pot)/(K*Temp);
    aeta =pow(eta,4.0) + 33.6*eta*(1-0.68*exp(-0.17*pow((eta+1),2))) + 50.0;
    fermi =1.0/(0.75*sqrt(PI)*pow(aeta,(-3.0/8.0)) + exp(-eta));
    density = ( 2.0/3.0)*NC*pow((Temp/(double)300),1.5)*fermi;

/*** Single subband ****/
    eta = -(Ecinf+delEc2-pot)/(K*Temp);
    aeta =pow(eta,4.0) + 33.6*eta*(1-0.68*exp(-0.17*pow((eta+1),2))) + 50.0;
    fermi =1.0/(0.75*sqrt(PI)*pow(aeta,(-3.0/8.0)) + exp(-eta));
    density += ( 1.0/3.0)*NC*fermi*pow((Temp/(double)300),1.5);

    return density;


double fermH(double pot,double Evinf,double delEv1,double delEv2,double
```

```
            delEv3,double Temp)
{
    double fermi1,fermi2,fermi3,eta,aeta;
    double density;
/* Sub-band One */
    eta = (Evinf+ delEv1 -pot)/(K*Temp);
    aeta =pow(eta,4.0) + 33.6*eta*(1-0.68*exp(-0.17*pow((eta+1),2))) + 50.0;

    fermi1 = (1.0/3.0)*NV*pow((Temp/(double)300),1.5)/ \
                (0.75*sqrt(PI)*pow(aeta,(-3.0/8.0)) + exp(-eta));
/* Sub-band Two */
    eta = (Evinf+ delEv2 -pot)/(K*Temp);
    aeta =pow(eta,4.0) + 33.6*eta*(1-0.68*exp(-0.17*pow((eta+1),2))) + 50.0;

    fermi2 = (1.0/3.0)*NV*pow((Temp/(double)300),1.5)/ \
                0.75*sqrt(PI)*pow(aeta,(-3.0/8.0)) + exp(-eta));
/* Sub-band Three */
    eta = (Evinf+ delEv3 -pot)/(K*Temp);
    aeta =pow(eta,4.0) + 33.6*eta*(1-0.68*exp(-0.17*pow((eta+1),2))) + 50.0;

    fermi3 = (1.0/3.0)*NV*pow((Temp/(double)300),1.5)/ \
                (0.75*sqrt(PI)*pow(aeta,(-3.0/8.0)) + exp(-eta));
    density = fermi1 + fermi2 + fermi3;
    return density;
}
```

---

[1] C.G. Van de Walle and R.M. Martin, "*Theoretical Calculations of Heterojunction Discontinuities in the Si/Ge system*", Physical Review B , vol.34, no.8 (1986), p.5621

[2] D. Bednarczyk and J. Bednarczyk, *"The Approximation of the Fermi-Dirac Integral $F_{1/2}(\eta)$"*, Physics Letters vol.64A, no.4, (1978), p.409.