Chapter 4

Silicon/Organic Heterojunction to Block Minority Carriers

4.1 Introduction

The best silicon solar cells are typically fabricated on thin high-quality silicon wafers ($< 200\mu$m) so most of the minority carrier recombination losses happen at silicon surfaces, specifically the silicon/metal contacts (Fig. 4.1(a)). Conventional silicon solar cells use diffused p/p^+ back-surface fields to reduce the surface recombination (Fig. 4.1(b)). A potentially cheaper and more effective alternative to diffused back-surface fields could be a minority-carrier blocking silicon/organic heterojunction (Chapter 2), e.g as an electron-blocking p-type contact at the anode (Fig. 4.1(c)).

To demonstrate such a heterojunction, two critical issues were needed to be solved: midgap states at unpassivated Si surfaces and band-alignment at Si/organic interface. The former can be solved using using PQ-passivated Si surfaces (Chapter 3), but finding an organic with the correct band-alignment is still an open problem. The two specific band-alignment criteria for an electron-blocking layer are:

(a) The LUMO of the organic should be much higher than conduction band edge

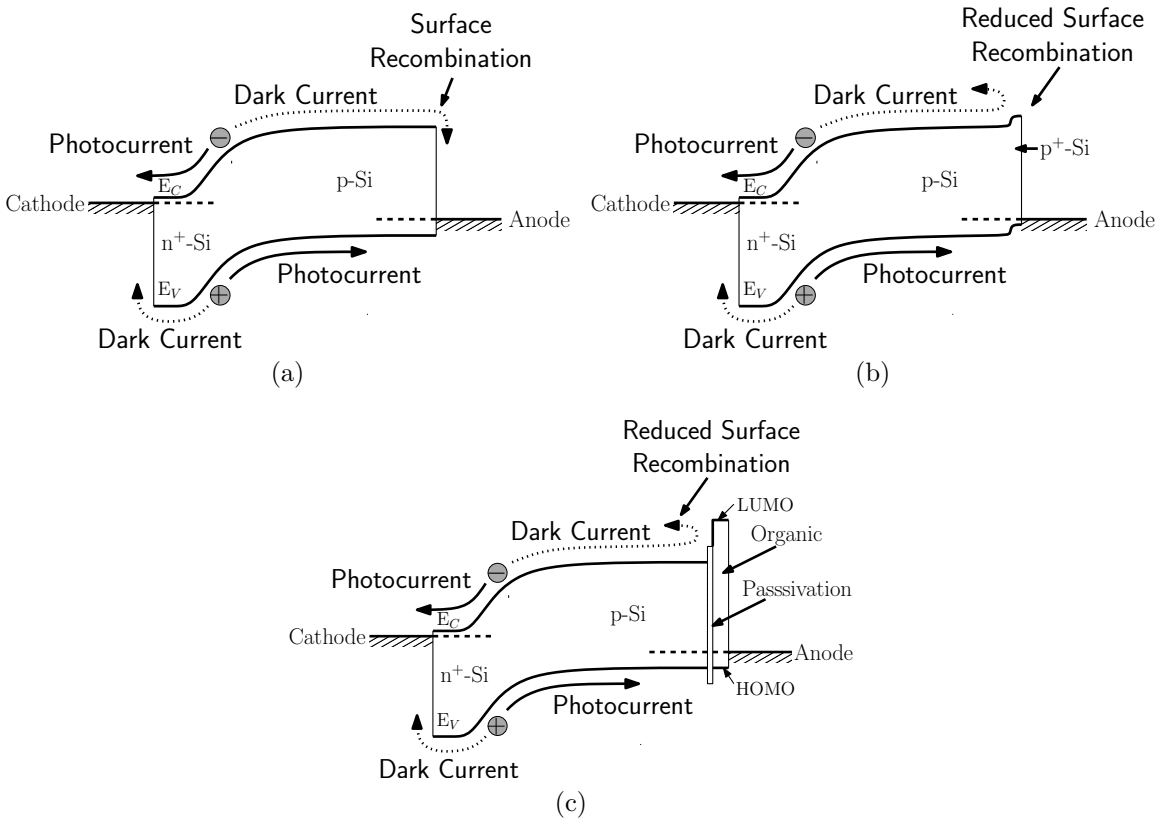


Figure 4.1: (a) Band Diagram of solar cell in which recombination at the metal contact dominates. The solid lines are desired direction of photogenerated carrier flow and the dashed line represents dark current, or equivalently the loss mechanism. (b) Effect of a p/p^+ back surface field in reducing the electron recombination at the anode. (c) Effect of a suitable silicon/organic heterojunction that reduces the electron recombination at the anode due to the offset in the conduction band.

of silicon, i.e. there should be a large conduction band offset, so that electrons are repelled away from the surface,

(b) The HOMO and the valence band edge of Si should be aligned, i.e. there should be almost no valence band offset, so that photogenerated holes can be efficiently extracted at the anode.

The goal of this chapter is to demonstrate that such an electron-blocking Si/organic heterojunction can reduce electron recombination at a Si/metal interface.

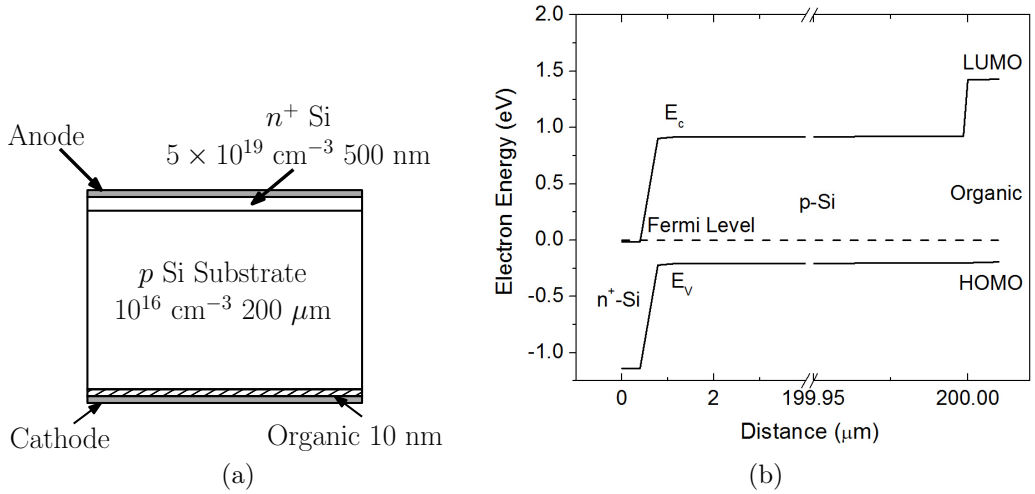


Figure 4.2: (a) The structure of a n$^+$-p diode with silicon/organic heterojunction that is used in simulations to confirm the expected reduction in J_0. (b) The band structure of the n$^+$-p-organic diode.

4.2 Proof of Concept: Simulations

First principle simulations were used to confirm that an electron-blocking silicon/organic heterojunction can reduce the J_0 of a p-n junction diode. All simulations were done using the "Taurus Device" tool from Synopsys®. The simulated structure is shown in Fig. 4.2(a). The recombination lifetime in silicon was set at 1 ms. The energy levels of the organic were chosen such that the Si/organic interface had a conduction-band and valence-band offset of 0.5 eV and 0 eV, respectively (Fig. 4.2(b)). The bulk mobility of the organic layer was 10^{-3} cm^2/V·s. For simplicity, the organic semiconductor was modeled as a conventional semiconductor with density of states that were 10 times lower than the density of states of silicon. The reduced density of states were supposed to simulate the fact that at room-temperature only those states are occupied that are within around 50 meV of the band-edge. While not exact, this should qualitatively reproduce the expected behavior.

Simulations confirm the electron-blocking effect of the Si/organic heterojunction. Without the heterojunction, the electron density in silicon near the anode is pinned

to zero, similar to what is expected in a short-base diode (Fig. 4.3(a)). With the heterojunction, the electron density increases by several orders of magnitude because it is no longer pinned to zero at the contacts. Since the diffusion current of the electrons in p-type silicon is directly proportional to the slope of electron density profile, J_0 of the heterojunction device is lower than an equivalent device with no heterojunction (Fig. 4.3(b)). Looking at the simulated current-voltage characteristics, an issue that is immediately apparent is the high series-resistance of the heterojunction device. At higher currents (>10 mA/cm^2), ohmic losses in the organic layer are the primary reason for the series resistance. This could be a potential issue in a solar cell.

To confirm the importance of surface defects at the silicon/organic heterojunction, simulations were also performed with a varying values of surface recombination velocity (SRV). As expected, at higher recombination velocities, the electron density at the contact decreases and the electron current increases (Fig. 4.3(b)).

The total current in the simulated device consists of two components, electron current and hole current. At a forward bias of 0.5 V the hole and electron-current components of the device were separately plotted as a function of surface recombination velocity (Fig. 4.3(c)). Also shown in the data are the asymptotic values: the minimum current obtained at an SRV of zero and the maximum current from a Si/metal device (no heterojunction). While the electron current continues to decrease as the SRV at the silicon/organic interface decreases, the total current stagnates at $\approx$ 35 µA. This is because the hole current from the p-type to the n-type region does not depend on the SRV of the p-type contact and at a SRV of $\sim$30 cm/s the total current becomes dominated by holes. This highlights an issue that will reoccur again, a single heterojunction can reduce only one of the carriers, electron or holes, and the device performance soon becomes limited by the current due to the other carrier.

Finally, the analytical expression for electron current, mentioned in Section 2.4.1 and derived in Appendix A.5, is compared with the simulated electron current.

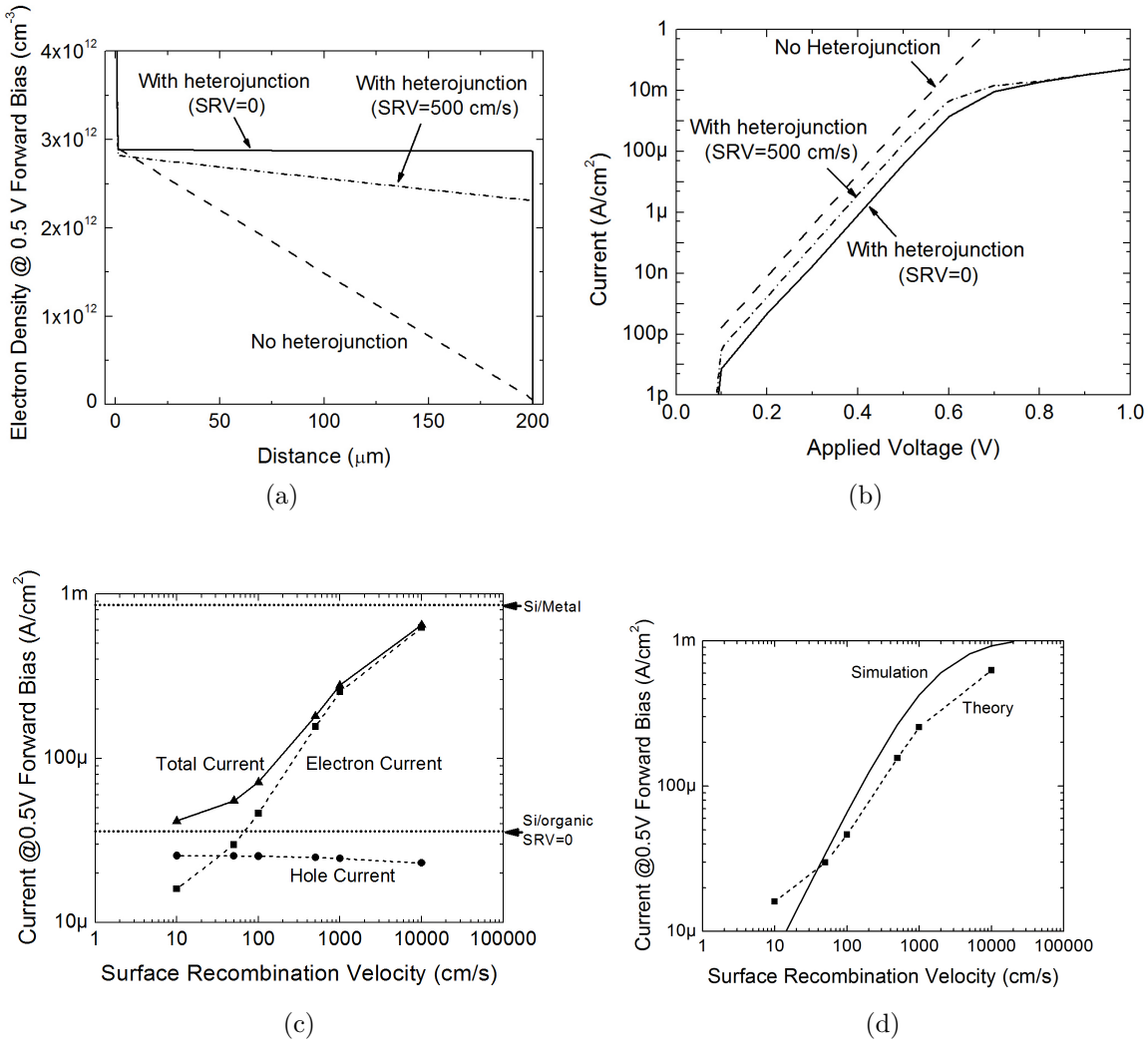


Figure 4.3: (a) Simulated electron-density profile and (b) simulated current-voltage characteristics of a n^+-p diode with and without the electron-blocking organic layer. Curves for the non-ideal Si/organic interface, with a surface recombination velocity of 500 cm/s, is also shown. (c) Contribution of hole and electron current to the total current at 0.5 V forward bias. (d) Comparison between the simulated and analytically derived (Eq. (2.4)) values of electron current at 0.5 V forward bias.

Clearly, the theory and simulations qualitatively agree over a wide range of SRV.

4.3 Probe of Minority Carrier Current

One way to test the performance of a minority-carrier blocking contact would be to integrate it onto a high-efficiency solar cell, to form a structure similar to the one

shown in Fig. 4.2(a), and see if J_0 is reduced. However fabricating high-quality n^+-p diodes with millisecond bulk lifetimes requires access to high-quality Si wafers and ultra-clean furnaces. Furthermore, to validate the performance of Si/organic heterojunction, we want to measure a decrease in the device J_0. If the J_0 of the fabricated devices varies from sample-to-sample, due to differences in processing and/or wafer quality, the experiments will be inconclusive. In order to reliably compare the performance of different silicon/organic heterojunctions for the role of a electron-blocking p-type contact, a test structure that is very sensitive to surface recombination of minority-carriers (a "Minority Carrier Probe") is required.

4.3.1 Design

The structure designed for this purpose is shown in Fig. 4.4(a). Simulations were used to optimize the doping levels and thicknesses of all the layers, such that total current is dominated by the electron injection current from n^+ to p layer (Fig. 4.4c. Additionally the top p-Si implant layer was kept thin so that most of the electron recombination happens at the top Si/metal interface (diffusion length of electrons >> thickness of the p-Si implant layer).

If an electron-blocking silicon/organic heterojunction is introduced at the p-type contact between silicon and the anode (Fig. 4.5(a)), the electron recombination at the Si/metal interface will decrease and a lower J_0 will be measured as confirmed by the simulated current-voltage characteristics (Fig. 4.5(c)).

The surface recombination velocity at the Si/organic interface is parameter that is least under our control. To increase the chances of observing a decrease in electron recombination, the minority-carrier probe should should work over a large range of surface recombination velocities. Suppose the probe is too sensitive to surface recombination, capable of showing a lower of J_0 only when SRV <50 cm/s, no electron-blocking effect would ever be observed at PQ-passivated silicon surface (SRV ∼100

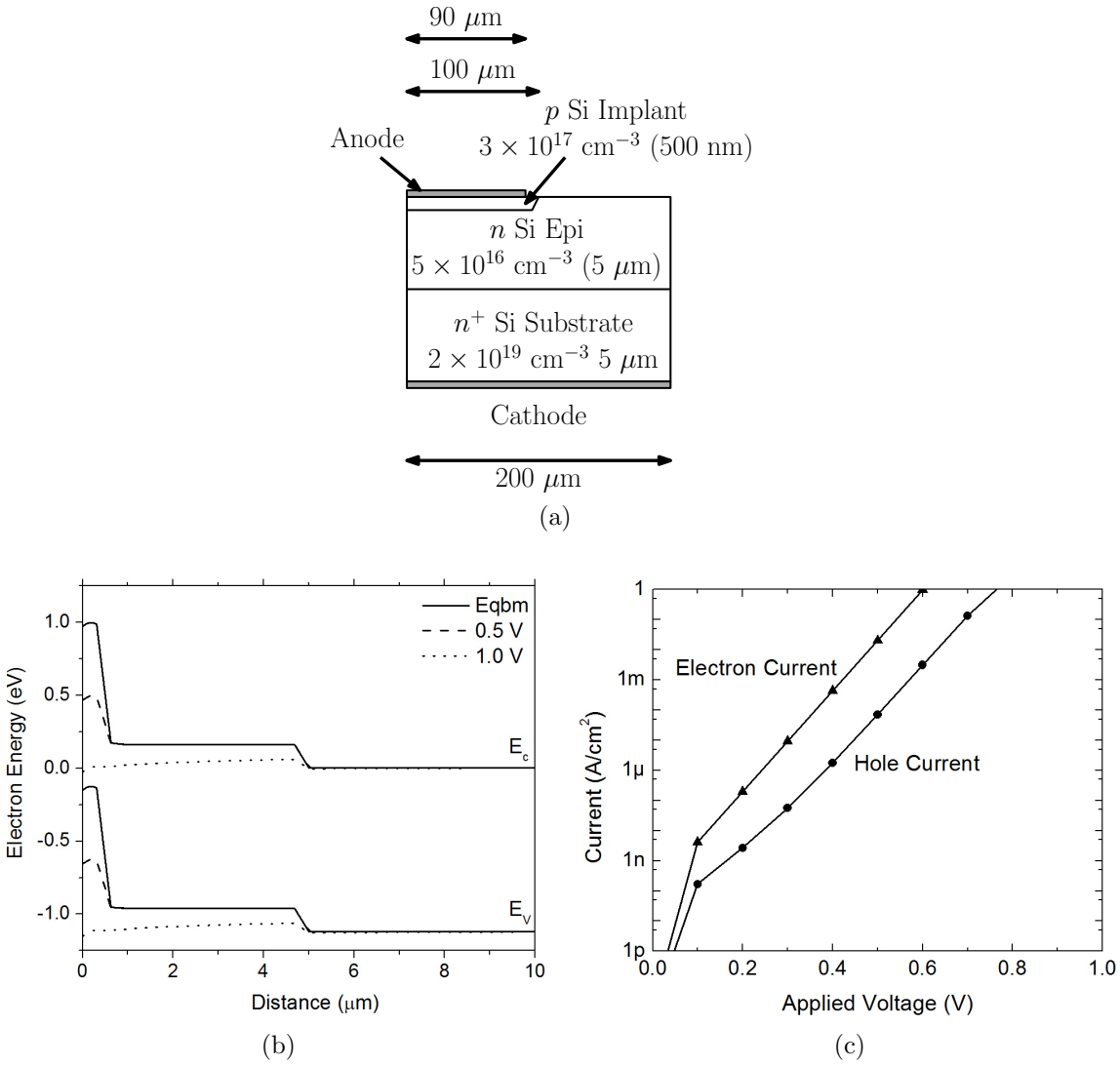


Figure 4.4: (a) The structure of the minority-carrier probe used to test electron-blocking in silicon/organic heterojunctions. (b) The band diagram of the minority-carrier probe. (c) The simulated forward-bias current-voltage characteristics of the minority-carrier probe. The electron current dominates the hole current.

cm/s, measured in Chapter 3). Simulations with different values of Si/organic recombination velocity show that the designed minority-carrier probe is fairly insensitive to SRV, and will show a decrease in J_0 if SRV <10000, good enough for PQ-passivated surfaces (Fig. 4.4(a)).

A practical minority-carrier probe that follows the exact specifications of Fig. 4.4(a) should be sensitive to reduction in electron current, i.e. it should have a current se-

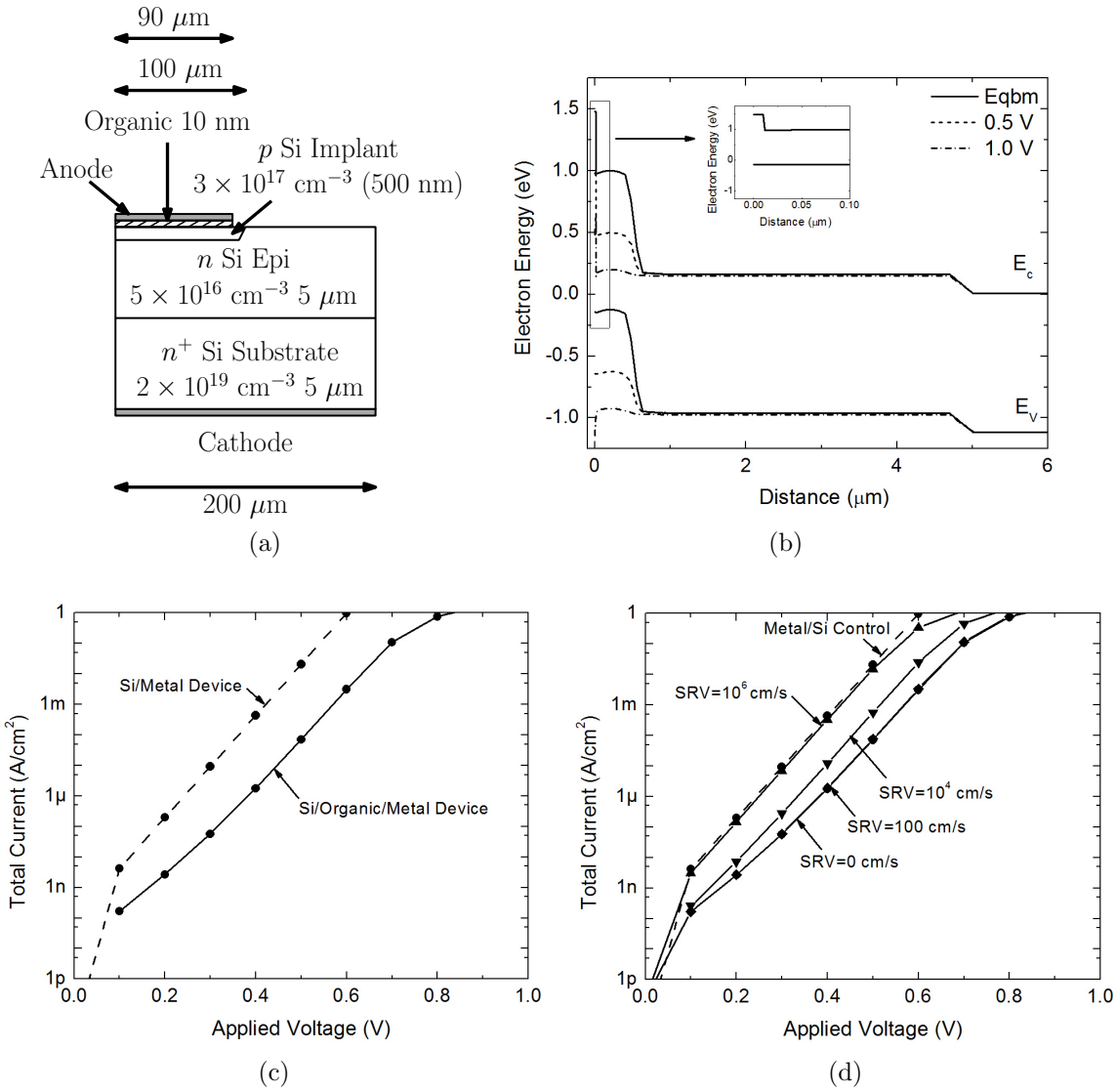


Figure 4.5: (a) The device structure and (b) band diagram of the minority-carrier probe with a silicon/organic heterojunction at the p-type contact. (c) The simulated forward-bias current-voltage characteristics showing reduction in current. (d) The simulated forward-bias current-voltage characteristics at different levels of silicon surface recombination velocity.

lectivity ratio ($I_{electron}/I_{hole}$) of >10. However, practical devices always have some deviations from the intended structure. To insure that the minority-carrier probe design is robust against such unintended variations, dependence of selectivity on parameters, like doping, carrier lifetime, and implant depth were also analyzed, As shown in Fig. 4.6, simulations reveal that the design of the probe is quite robust and

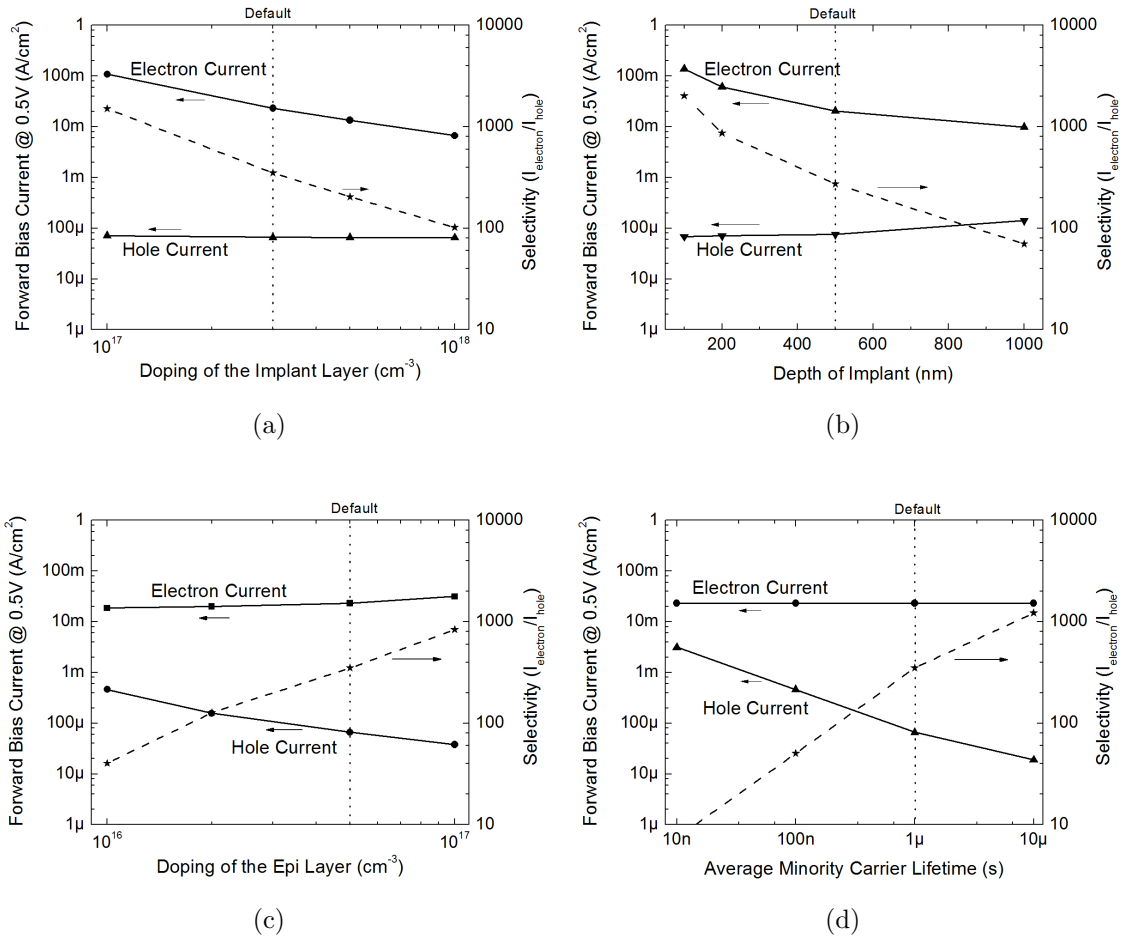


Figure 4.6: The selectivity of the designed minority-carrier probe as a function of (a) implant doping, (b) implant depth, (c) Epi layer doping, and (d) average minority-carrier lifetime.

electron current dominates the hole current by at least a factor of ten for a wide range of parameters.

4.3.2 Fabrication

The minority-carrier probe was fabricated on a highly-doped n-type CZ silicon (100) wafer (<0.005 Ωcm, ∼10^{19} cm^{-3}). First, wafers were cleaned by Piranha clean [78]. This was followed by a 1 minute HF dip (1:100) to remove the surface oxide. Wafers were then loaded into a Rapid Thermal Chemical Vapor Deposition (RTCVD) system

to grow a 6 µm thick epitaxial layer of silicon. The precursor gas was dichlorosilane (26 sccm) diluted in Hydrogen (4 slpm). The growth temperature was 1000 ℃ (29 % lamp power) and growth rate was approximately 200 nm/min. The epitaxial layer was unintentially doped n-type ($<5\times10^{16}$ cm^{-3}). Next, a 750 nm thick wet oxide was grown at 1050 ℃ in the Thermco furnace. The oxide layer served as hard mask for the subsequent ion-implantation. Photolithography was used to etch holes into the oxide layer to define the implant area. Patterned samples were implanted with boron at Core Systems, CA. Unless otherwise stated, the implant dosage and energy were 10^{13} cm^{-2} and 50 keV, respectively. After implantation, samples were cleaned and again loaded into the Thermco furnace, this time for dopant activation and annealing. Annealing temperatures were around 1000 ℃ and annealing time was 20 minutes. Samples were always introduced into the furnace in an oxygen atmosphere, and after 10 minutes nitrogen was turned on. To estimate the final doping profiles of the structure, simulations were done in Taurus TSuprem4 (a Synopsys® tool). The expected doping profile of the structure, before and after annealing, is shown in Fig. 4.7(a). To form the Si/metal structure (Fig. 4.7), samples were dipped in a 10:1 buffered HF solution for 10s to remove any native oxide and then Ag or Al was deposited by thermal evaporation.

4.3.3 Characterization

Before the minority-carrier probe can be used to test Si/organic heterojunctions, its baseline performance needs to be characterized. The critical questions to demonstrate performance of the minority-carrier probe are:

(a) Is the electron current the dominant component of the total current?

(b) Is the device in short-base condition? i.e. do most of the electrons recombine, at the Si/metal interface?

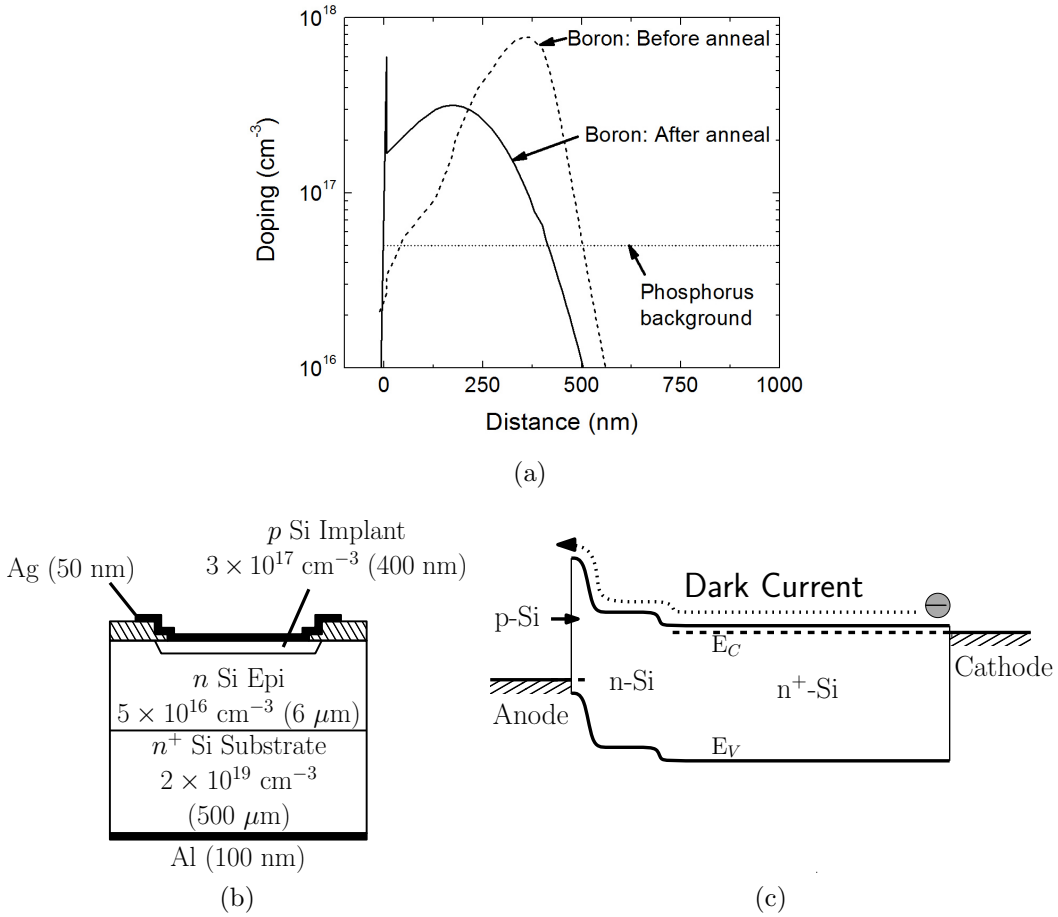


Figure 4.7: (a) Simulated doping profile of the implanted region before and after annealing. The implant dosage and energy was 10^{13} cm^{-2} and 50 keV, respectively. (b) Structure and (c) band-diagram of the minority-carrier probe.

(c) Are the current-voltage characteristics of the diodes ideal? Specifically, can values of J_0 be extracted reliably from the data?

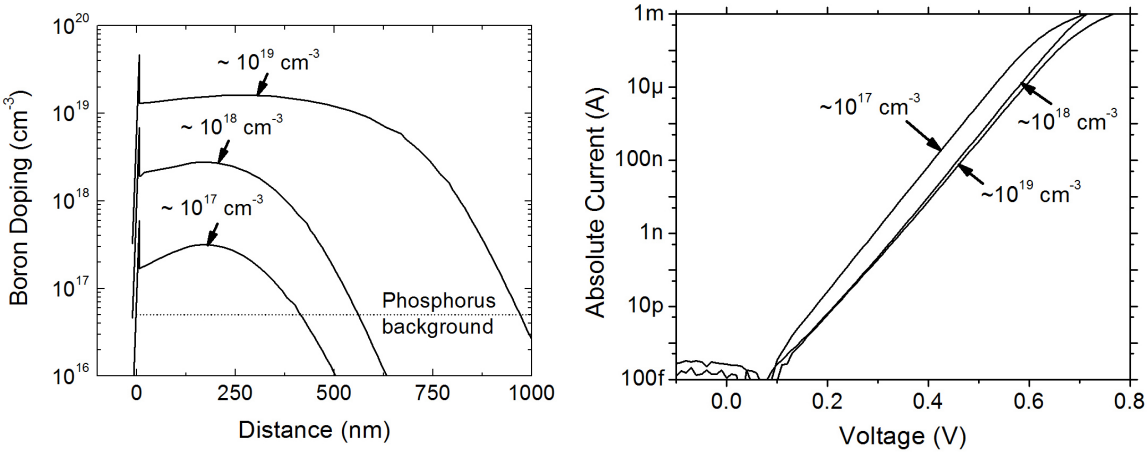
Does the electron current dominate?

In a short-base diode, the electron current scales with p-type doping (N_A) and length of the quasi-neutral region (W):

$$J_{electron} \propto \frac{1}{N_A W} \tag{4.1}$$

Table 4.1: Implant doses, energies, and annealing conditions used to fabricate devices with different p-type doping. The measured value of J_0 are also given. Device area is 200 µm × 200 µm

p-Si doping (cm^{-3})	Implant conditions			Annealing conditions		J_0 (A/cm^2)
	Species	Dosage (cm^{-2})	Energy (keV)	Temp (°C)	Time (min) & ambient	
$\sim 10^{17}$	B	10^{13}	50	1000	10 (in O_2) + 10 (in N_2)	4.7×10^{-11}
$\sim 10^{18}$	B	10^{14}	50	1000	10 (in O_2) + 20 (in N_2)	4.5×10^{-12}
$\sim 10^{19}$	BF_2	10^{15}	100	1000	5 (in O_2) + 10 (in N_2)	4.5×10^{-12}



(a) (b)

Figure 4.8: Effect of increasing implant doping on the characteristics of the minority-carrier probe. (a) Simulated doping profiles of the structures after annealing at 1000 °C. (b) Measured I-V characteristics for the three devices. The device area is 200 µm × 200 µm.

To test if the fabricated minority-carrier probe is electron limited and is in short-base condition, two diodes with higher p-type doping and larger junction depth were also fabricated. In these higher doped devices, the electron injection from the n^- layer to the p-implant layer is expected to decrease because of Eq. (4.1). If electron current dominates the total current, the decreased electron injection will lead to a decrease in the total current.

The implant dose, implant energy and annealing conditions for all the three cases are given in Table 4.1. TSPUREM4 simulations showed that the expected doping

levels in these devices is $\sim 10^{17}$, 10^{18}, and 10^{19} cm^{-3}.

Current-voltage characteristics of the finished Si/metal diodes are shown in Fig. 4.8(b). As expected, the highest current is measured in the sample with p^- doping of $\sim 10^{17}$ cm^{-3} and a junction depth of 400 nm. As the doping level and junction depth are increased to $\sim 10^{18}$ cm^{-3} and 560, respectively, the current falls by a factor of 10. When the doping is increased even further (to $\sim 10^{19} cm^{-3}$), the current does reduce more, but only marginally. This probably signifies that the diode is now dominated by hole current or the bandgap narrowing in the heavily-doped layer is very significant. Overall the data confirms that in the $\sim 10^{17}$ cm^{-3} doped structure, the electron current is at least 10 times larger than the hole current.

Is the diode in the short-base regime?

One possible objection to the implant test is that all three samples were processed completely separately during the implant and anneal steps and the difference in I-V characteristics may just be an artifact of unaccounted variations in process conditions and wafer quality. Another, and possibly more serious objection is that the test does not tell if the diode is in short-base regime or not. Current reduction would be observed even if most of the electrons recombine in the bulk and not the surface.

To work around this issue, two implanted and annealed devices were chosen from the same silicon wafer. One of the devices was put back into the RTCVD and a 200 nm thick highly-doped p-Si epitaxial layer was grown on top of the p-type implant layer (Fig. 4.9(a)). Finally, metal electrodes were deposited on both of the samples.

The device with the extra epitaxial layers has as surface field due to the $p\text{-}p^+$ junction which is expected to reduce the electron recombination at the anode in much the same way as a silicon/organic heterojunction. Significantly, the epitaxy process is only 1 min long (at 1000 ℃), so no major changes in the doping or depth of the p^-/n^- junction are expected. A decrease in current can only happen if the diode

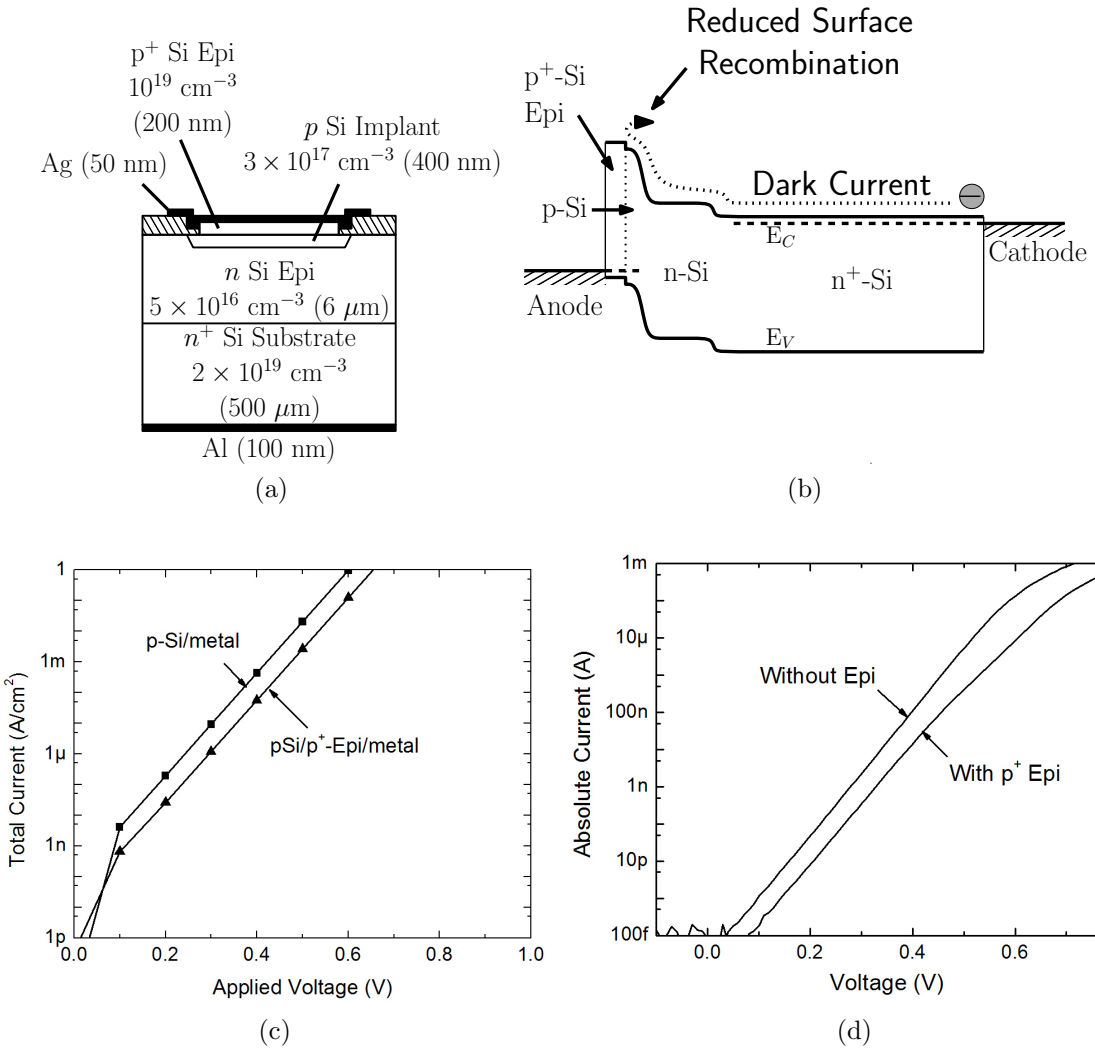


Figure 4.9: (a) Structure and (b) band-diagram of the 'Epitaxial' device. (c) The simulated IV characteristics of the minority-carrier probe with different p-type contacts: silicon/metal, ideal silicon/organic heterojunction, and p-p^+ homojunction. (d) Measured I-V characteristics of devices with and without the 'Epi' layer. The device area is 200 µm × 200 µm.

was originally in the short-base condition. Simulated current-voltage characteristics of a simulated structure confirm the same. Compared to a control device without the epitaxial layer, the epitaxial p^+-Si layer shows a decrease in total current.

The experimentally measured characteristics are shown in Fig. 4.9(d). Compared to the Si/metal structure (without Epi layer), the I-V characteristics of the structure with the 'Epitaxial' layer shows a 6× decrease in J_0, arguably due to reduced electron

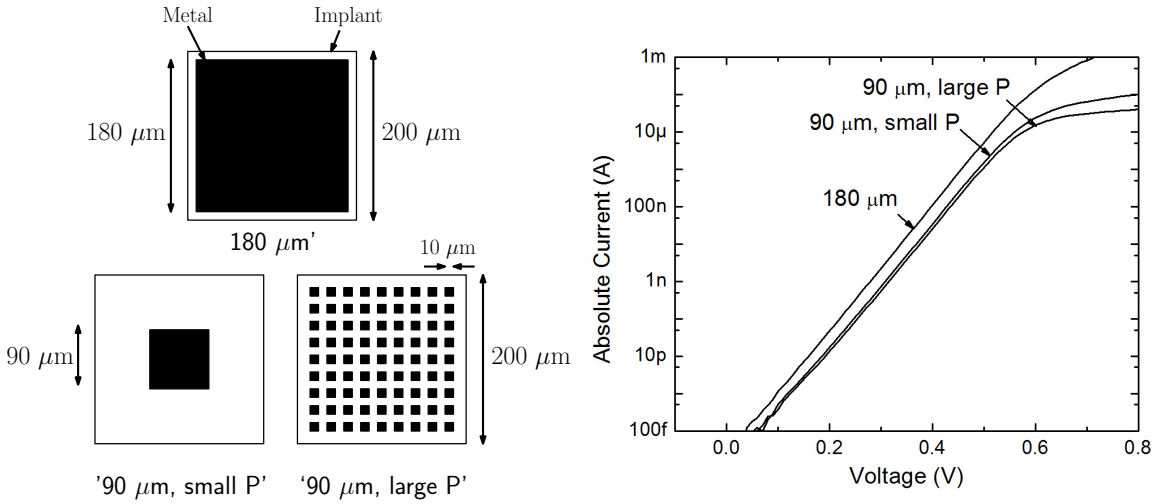


Figure 4.10: Do currents in minority-carrier probe scale with contact area? (a) Top view of the minority-carrier devices with different contact shapes. Black area represents metal. (b) Measured I-V characteristics of devices with different contact shapes.

Table 4.2: Test if current in the minority-carrier probes of Fig. 4.10 scales with contact area or contact perimeter. Implanted area is fixed at 4×10^{-4} cm^2. Ideality factor of the diodes was extracted from data between 0.2-0.4V.

Device	Contact				Current at 0.4V	Current scales by	n
	Area (μm^2)	Scales by	Perimeter (μm)	Scales by	(nA)		
'90 μm, small P'	8100	1	360	1	34	1	1.00
'90 μm, large P'	8100	1	3240	9	26	0.8	1.01
'180 μm'	32400	4	720	2	111	2.9	1.00

current. The experiment reaffirms that electron injection is the dominant current carrying mechanism in the minority-carrier probe and conclusively shows that the I-V characteristics are sensitive to electron recombination at the top silicon surface.

Are the I-V characteristics of the diode ideal?

To test surface recombination, the minority-carrier probe needs to have near-ideal I-V characteristics. Any large deviation due to edge effects, leakages, poor ideality factor, etc. would make it impossible to compare the J_0 of two different devices.

To test the Si/metal interface, three devices were fabricated with the same im-

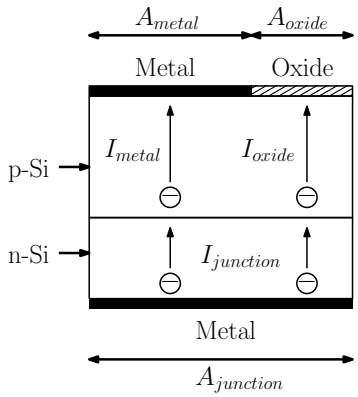


Figure 4.11: Explanation for dependence of total current on Si/metal area. The total electron injection current ($I_{junction}$) and its two components: J_{metal} and J_{oxide}

planted area (200 µm × 200 µm) but different Si/metal contacts (Fig. 4.10(a)). The device named '180 µm' is the same structure as the standard Si/metal device used before. The devices, named '90 µm, small P' and '90 µm, large P', both have the same contact area (90 µm × 90 µm) but different perimeter. The perimeter of '90 µm, large P' is 9 times larger ('large P') than '90 µm, small P'.

If the Si/metal interface has any edge effects, the current in the 'small P' and 'large P' devices would be substantially different. The measured current-voltage characteristics show that this is not the case (Fig. 4.10(b)). The differences in currents between 'small P' and 'large P' device are minimal - at 0.4 V the currents in the two diodes are 34 nA and 26 nA, respectively (Table 4.2).

The currents in the '90 µm, small P' device and the '180 µm' device are not equal, even though the junction area is equal. At 0.4 V, the current in the '90 µm, small P' device is 34 nA while in '180 µm' device it is 111 nA - a factor of 2.9 different. The only difference in the two devices, to justify the different currents, is the contact area which is 4× larger in the latter device. This dependence on Si/metal contact area is not surprising because the minority-carrier probe is dominated by electron recombination at the top electrode and larger metal area should increase electron current.

A simple one-dimensional model of the p-n junction diode does not capture this

dependence. To visualize the argument, consider a simple two dimensional p-n junction (Fig. 4.11). Assume that all minority-carrier current in the p-region of the diode flows vertically, i.e. there is no lateral current flow. The total current flowing across the junction, characterized by $J_{0,junction}$, is a area-weighted sum of two components: the current recombining at the metal (characterized by a $J_{0,metal}$) and current recombining at the oxide (characterized by a $J_{0,oxide}$).

$$J_{0,junction} = \frac{J_{0,metal}A_{metal} + J_{0,oxide}A_{oxide}}{A_{metal} + A_{oxide}} \tag{4.2}$$

where A_{metal} and & A_{oxide} represents the area covered with metal and oxide, respectively. If the oxide passivation is as bad as the Si/metal interface, i.e. $J_{oxide} = J_{metal}$, and total current scales with total area ($I_{0,junction} = J_{0,metal}(A_{metal} + A_{oxide})$). However, if the Si/oxide interface is perfectly passivated, i.e. J_{oxide} =0, then $I_{0,junction} = J_{metal}A_{metal}$, and the device current scales with area of the contact metal, not area of the p-n junction. Practical devices are expected to lie somewhere in the middle. This is confirmed in the I-V characteristics of devices, '90 µm, small P' and '180 µm', where the total current in the latter device is 2.9× bigger (Table 4.2).

From the given value of A_{metal} and A_{oxide} (=A_{total} - A_{metal}), we can estimate $J_{0,oxide}$ and $J_{0,metal}$ using Eq. (4.2).

$$J_{0,\text{`180µm'}} = J_{0,oxide}\frac{7600}{40000} + J_{0,metal}\frac{32400}{40000} = 4.7 \times 10^{-11}$$
$$J_{0,\text{`90µm,smallP'}} = J_{0,oxide}\frac{31900}{40000} + J_{0,metal}\frac{8100}{40000} = 1.8 \times 10^{-11}$$

Solving for $J_{0,oxide}$ and $J_{0,metal}$,

$$J_{0,oxide} = 8.3 \times 10^{-12} A/cm^2 \quad \& \quad J_{0,metal} = 5.6 \times 10^{-11} A/cm^2 \tag{4.3}$$

Non-idealities can also arise at the edge of the p-n junction due to un-annealed

implant damage or trapped charges at the Si/oxide interface. In the I-V characteristics, the tell-tale sign of these issues is evidence of currents that scales with the device perimeter. To test for any perimeter effects at the edges of the implanted region, devices with different implanted areas were fabricated: '200 µm', '50 µm', and '20 µm' (Fig. 4.12(a)).

If the diodes are ideal and there are no edge-effects then the simple model derived above (Fig. 4.11) would fully describe the currents. Using values of J_{oxide} and J_{metal} calculated in Eq. (4.3) along with Eq. (4.2), the 'expected' scaling factor between '200 µm' and '50 µm' devices in the absence of edge effects is:

$$\frac{I_{0,\text{`200µm'}}}{I_{\text{`50µm'}}} = \frac{7600J_{0,oxide} + 32400J_{0,metal}}{1600J_{0,oxide} + 900J_{0,metal}}$$
$$= 29 \tag{4.4}$$

Between '20 µm' and '50 µm', expected scaling factor is:

$$\frac{I_{0,\text{`20µm'}}}{I_{\text{`50µm'}}} = \frac{300J_{0,oxide} + 100J_{0,metal}}{1600J_{0,oxide} + 900J_{0,metal}}$$
$$= 0.13 \tag{4.5}$$

The measured I-V characteristics of the three devices is given in Fig. 4.12(b). At 0.4 V, the currents measured in the '200 µm', '50 µm', and '20 µm' device is 110 nA, 3.5 nA , and 0.13 nA, i.e. scaling factor of 31 and 0.14 (Table 4.3). These experimentally measured values are remarkably close to what our model predicts (Eq. (4.4) & Eq. (4.5)). This proves not only the predictive power of the model but also confirms that perimeter effects are indeed absent in the "minority-carrier probe" devices.

In summary, the designed minority-carrier probe has near-ideal characteristics: an ideality factor of ≈1, and a J_0 that predictably scales with area.

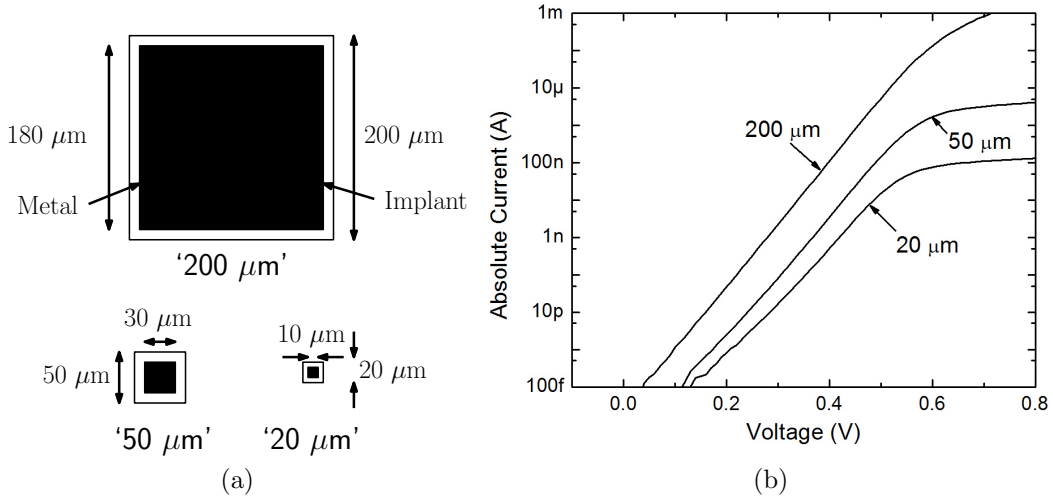


Figure 4.12: Do currents in minority-carrier probe scale with area? (a) Top view of the minority-carrier devices with different implant area. Black area represents metal. (b) Measured I-V characteristics of devices with different implant areas.

Table 4.3: Test if the current in the minority-carrier probes of Fig. 4.8 scales with device area or contact area. Ideality factor of the diodes was extracted from data between 0.2-0.4V.

Device	Implant		Contact		Current at 0.4V	Current scaling factor		n
	Area (μm^2)	Scales by	Area (μm^2)	Scales by	(nA)	Expected	Measured	
'200 μm'	40000	16	32400	36	110	29	31	1.00
'50 μm'	2500	1	900	1	3.5	1	-	1.01
'20 μm'	400	0.16	100	0.11	0.51	0.13	0.14	1.08

4.4 Reduced Minority Carrier Recombination at the P-type Contact

After validating the design of the minority-carrier probe, organic/silicon heterojunctions were fabricated to test for reduced recombination at the metal/silicon contacts.

4.4.1 Materials and Fabrication

For fabrication of Si/organic diodes, patterned and annealed "minority-carrier probe" devices were prepped for PQ-passivation, using the recipe described before (3.6). In all the experiments, PQ layer thickness was fixed at $\sim$ 10 nm. Next, a second organic, in this case N,N-Bis(3-methylphenyl)-N,N-diphenyl benzidine (TPD), was thermally deposited (15 nm) on top of PQ-passivated Si to make a Si/PQ/TPD p-type contact. The organic depositions were done in Angstrom evaporator in room C405A. To encourage growth of amorphous layers, organic deposition rates were kept low at $\sim$0.02 nm/s. Depositions were monitored by quartz crystal, which had been calibrated using a profilometer. Top electrode were patterned using shadow masks with 1-mm radius holes. Back electrode was a blanket layer of aluminum.

TPD was bought from Sigma Aldrich and used as is.

4.4.2 PQ-passivated Si/TPD Heterojunction

Devices from the same implanted and annealed wafer were processed in three different ways: Si/metal diode (Fig. 4.13(a) & (b)), Si/p^+-Epi/metal diode (Fig. 4.13(c) & (d)), and Si/TPD/metal heterojunction diode (Fig. 4.13(e) & (f)). The I-V characteristic of these structures is shown in the Fig 4.14.

The metal-silicon diode is the control structure, in which the dark-current is mostly due to recombination of electron at the Si/anode interface. The Si/p^+-Epi/metal diode was fabricated by growing a 200nm highly-doped silicon layer ($\sim 10^{19}$ cm^{-3}) epitaxially on the p-Si surface before depositing the top metal. The thick p^+ epitaxial Si layer increases the surface field near the anode, which repels electrons and reduces electron recombination. Consequently, the current of the p^+-Epi diode is around 5 times lower than the control structure: at 0.3 V, currents fall from 2.2 nA to 0.34 nA. The extracted value of J_0, from the y-intercept on the semilog I-V plot, in 'Epi' diode is around 9.8 pA/cm^2 instead of 47 pA/cm^2 for the Si/metal diodes (Table 4.4).

The silicon/TPD/metal heterojunction was fabricated by depositing TPD on PQ-passivated silicon. Since PQ layer is thin, it was assumed that energy levels of PQ layers will not matter and the carriers will just tunnel through PQ (This ultimately turned out to be an incorrect assumption. For details please look at Chapter 5). TPD is a hole-conducting organic with reported HOMO & LUMO levels at 5.3 eV and 2.3 eV, respectively. Silicon/TPD is expected to be an electron-blocking heterojunction [105], so if it is introduced between silicon and the top metal in the minority carrier probe device, the electron recombination at the top electrode is expected to decrease.

Experimentally, currents in the heterojunction device are lower: at 0.3 V, the current in heterojunction device is only 0.34 nA. The extracted J_0 of the heterojunction device is around 23 pA/cm^2. Thus compared to Si/metal device, currents in the heterojunction device are reduced by a factor of at least two, proving the electron-blocking nature of Si/TPD heterointerface. The values of the ideality factor (extracted from data between 0.2-0.3 V) further show that diode characteristics are near-ideal, so the effect is not expected to be due to some unaccounted non-linearity (Table 4.4).

A big concern is the large series resistance of the heterojunction devices, probably due to low conductivity of the undoped TPD layer. In a practical solar cell, such large ohmic losses are unacceptable so a intrinsically more conductive or doped organic thin-film would be needed.

Assuming the simple model of Fig. 4.11 holds and the $J_{0,oxide}$ is equal among them (all samples were annealed together so oxide was formed together), one can calculate the saturation current density associated with the Si/p$^+$-Epi homojunction ($J_{0,pEpi}$) and Si/organic heterojunction ($J_{0,heterojunction}$). The J_0 of the Si/p$^+$-Epi diode and

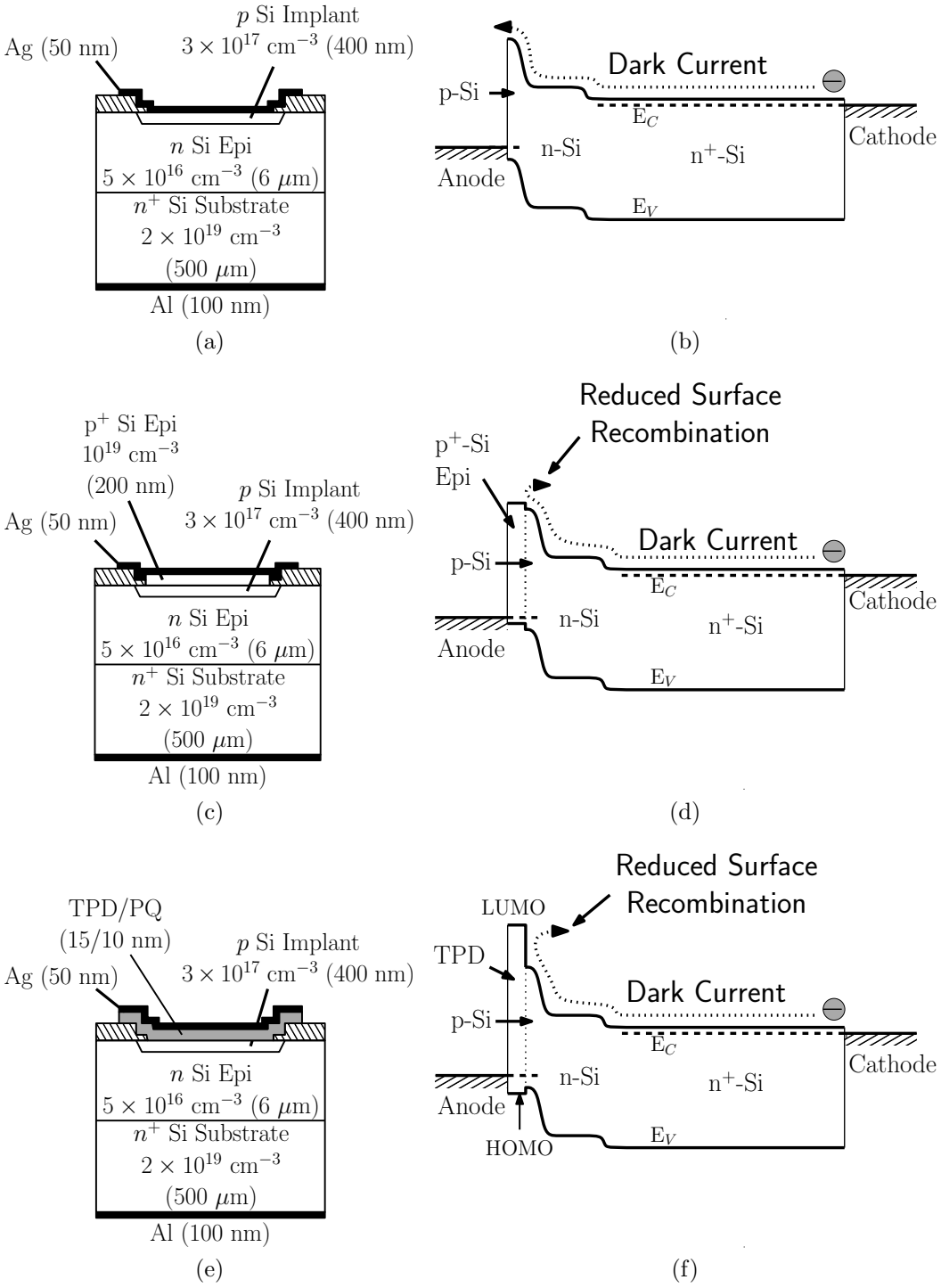


Figure 4.13: Structure and band diagrams of the minority-carrier probe with different p-type contacts (a) & (b) Si/metal contact (baseline) (c) & (d) Si/p^+-Epi/metal and (e) & (f) Si/TPD/Metal.

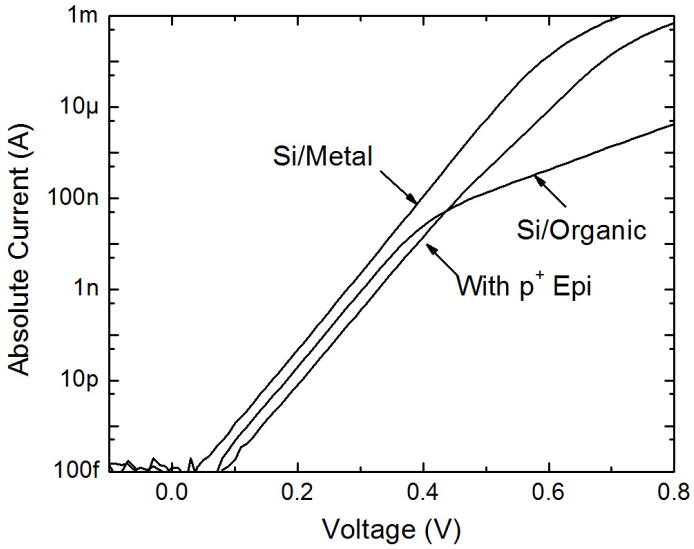


Figure 4.14: Effect of PQ-passivated Si/TPD heterojunction on minority-carrier probe. Measured I-V characteristics of the device with and without heterojunction. For reference the I-V of the Epi structure is also shown. The device area is 200 µm × 200 µm.

Si/organic diode are give n in Table 4.4. Using Eq. (4.2)

$$J_{0,`Si/p^{+}-Epi'} = J_{0,oxide}\frac{7600}{40000} + J_{0,pEpi}\frac{32400}{40000} = 9.8 \times 10^{-12} \tag{4.6}$$

$$\Rightarrow J_{0,pEpi} = 1.0 \times 10^{-11} A/cm^2 \tag{4.7}$$

Table 4.4: Current scaling, extracted ideality factor, and extracted J_0 diode of the heterojunction from data between 0.2-0.3V. For calculating J_0 implanted area was used as the device area: 200 µm × 200 µm.

Device	Implant Area (µm^2)	Contact Area (µm^2)	Area scales by	Current at 0.3V (nA)	Current scales by	J_0 (A/cm^2)	n
Si/metal	40000	32400	1	2.20	1	4.7×10^{-11}	1.00
Si/p$^+$-Epi/metal	40000	32400	1	0.34	0.15	9.8×10^{-12}	1.02
Si/organic/metal	40000	32400	1	0.89	0.40	2.3×10^{-11}	1.01

Table 4.5: Calculated J_0 of the four types of p-type contacts fabricated in this study

p-type Contact	J_0 (A/cm^2)
Si/metal	5.6×10^{-11}
Si/p$^+$-Epi	1.0×10^{-11}
Si/oxide	8.6×10^{-12}
Si/PQ/TPD	2.6×10^{-11}

and

$$J_{0,`Si/organic'} = J_{0,oxide}\frac{7600}{40000} + J_{0,heterojunction}\frac{32400}{40000} = 2.3 \times 10^{-11} \quad (4.8)$$

$$\Rightarrow J_{0,heterojunction} = 2.6 \times 10^{-11} A/cm^2 \quad (4.9)$$

Table. 4.5 summarizes the J_0 values for all fours of the p-type silicon interface measured in this study.

The results do provide a first proof-of-concept that silicon/organic heterojunctions can be used to selectively reduce the minority-carrier recombination, while allowing transport of the majority carriers, at the p-type Si/metal contacts. More work in needed to reduce the series resistance, optimize the band offsets, understand the interaction of metal on the silicon and organic surfaces, and further reduce the surface recombination at the Si/organic interface.

4.5 Conclusion

A minority-carrier probe structure was demonstrated, in which the doping profiles were carefully designed to make the electron current exceed the hole current by a factor of at least ten. The shallow p-type implant ensures that most of the electron recombination occurs at the metal/silicon contact and not in the bulk. Further we demonstrated that the characteristics of the minority-carrier probe structure are near-ideal, and hence can be used to test the electron recombination at the Si/organic

heterojunction. Finally, using the PQ-passivated Si/TPD heterojunction we showed reduced minority-carrier recombination at the p-type metal-silicon contact.

Using such minority-carrier blocking heterojunctions in place of back-surface field in conventional silicon solar cells is a low-cost pathway towards more efficient solar cells. In an silicon-based solar cell with two silicon/organic heterojunctions, like the one depicted in Fig. 2.1(b) or Fig. 1.5(c), such a heterojunction would be one of the heterojunction. It would play a key role in reducing dark-current to achieve a large open-circuit voltage.

Chapter 5

Silicon/Organic Heterojunction to Block Majority Carriers

5.1 Introduction

Conventional silicon solar cells use diffused p/n junction to block majority carriers and separate photogenerated carriers, yielding a photocurrent (Fig. 5.1(a)). A potentially cheaper but just as effective alternative to diffused junctions could be a majority-carrier blocking silicon/organic heterojunction like that one introduced in Chapter 2 (Fig. 5.1(c)). The heterojunction is different, and technologically more useful, than the silicon/organic heterojunction described in Chapter 4 because it functions as an alternative to the p-n junction, a essential component of every solar cell.

As we shall demonstrate, silicon surface passivation is less important in majority carrier blocking heterojunctions because of a large electric field at the surface of silicon that reduces carrier recombination. The critical issue in this type of structure is band-alignment at the Si/organic interface. The hetero-interface even in this case is an electron-blocker so the specific band-alignment criteria remain the same as in Chapter 4:

(a) The LUMO of the organic should be much higher than the conduction band edge of silicon, i.e. there should be a large conduction band offset, so that electrons are repelled away from the surface,

(b) The HOMO and the valence band edge of Si should be aligned, i.e. there should almost no valence band offset, so that photogenerated holes can be efficiently extracted at the anode.

In this chapter, first some proof-of-concept simulations will be presented. Next two different majority carrier blocking heterojunctions on n-type silicon are discussed a) silicon/PQ/pentacene and b)silicon/Poly(3-hexylthiophene) heterojunction. The performance of the silicon/PQ/pentacene heterojunction is very poor, primarily due to poor band-alignment and high series resistance, but the discussion will help highlight the technical challenge of making such a cell. The silicon/P3HT heterojunction functions very well and using it heterojunction solar cells with 10.1 % effficiency will be demonstrated.

5.2 Proof of Concept: Simulations

First principle 1D simulations were used to confirm that p-n junction solar cells can be substituted by an electron-blocking silicon/organic heterojunction. As before, all simulations were done using the Taurus Device tool from Synopsys®. The simulated structure is shown in Fig. 5.2(a). The recombination lifetime in silicon was set at 100 µs. The organic had a conduction-band and valence-band offset of 0.5 eV and 0 eV, respectively (Fig. 5.2(b)). The bulk mobility of the organic layer was 10^{-3} $cm^2/V{\cdot}s$. For simplicity, the organic semiconductor was modeled as a conventional semiconductor with density of states that were 10 times lower than the density of states of silicon. The reduced density of states were supposed to simulate the fact that at room-temperature only those states are occupied that are within around 50 meV of

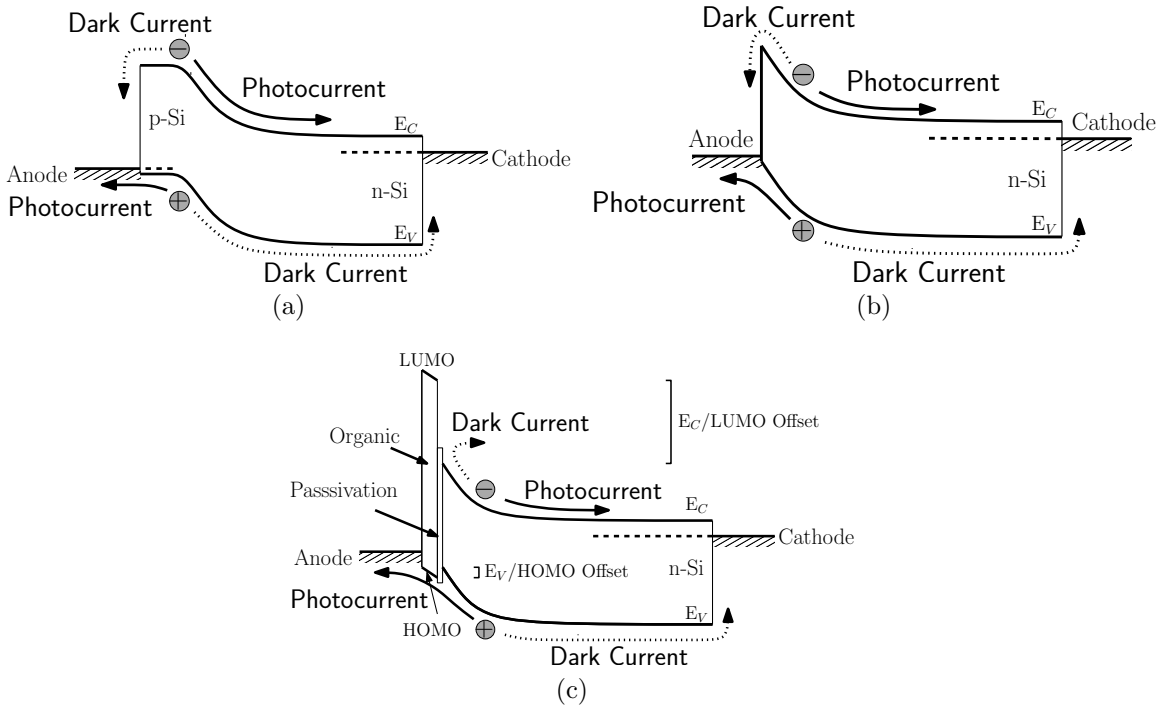


Figure 5.1: Band diagram of a (a) p-n junction and (b) Si/metal Schottky solar cell. The solid lines are desired direction of generated carrier flow and the dashed line represents dark current, or equivalently the loss mechanism. (c) An electron-blocking silicon/organic heterojunction with lower J_0 than Schottky junction.

the band-edge. While not exact, this should qualitatively reproduce the expected behavior. Since the surface recombination velocity (SRV) at the silicon/organic heterojunctions is important, simulations were performed with a SRV of 0, 500, and 5000 cm/s.

Under the assumption that surface defects do not cause any Fermi-level pinning in Si/metal or Si/organic heterojunction, simulated band-diagrams show a depletion region in silicon in both Si/metal and Si/organic/metal junctions (Fig. 5.2(a)). The strength of the built-in field is also the same in both cases, decided only by the difference in work-function between the top metal (5.1 eV) and n-type silicon. However due to the conduction-band offset, the simulated forward-bias currents in the passivated Si/organic device are much lower (Fig. 5.2(c)). Under a simulated illumination of

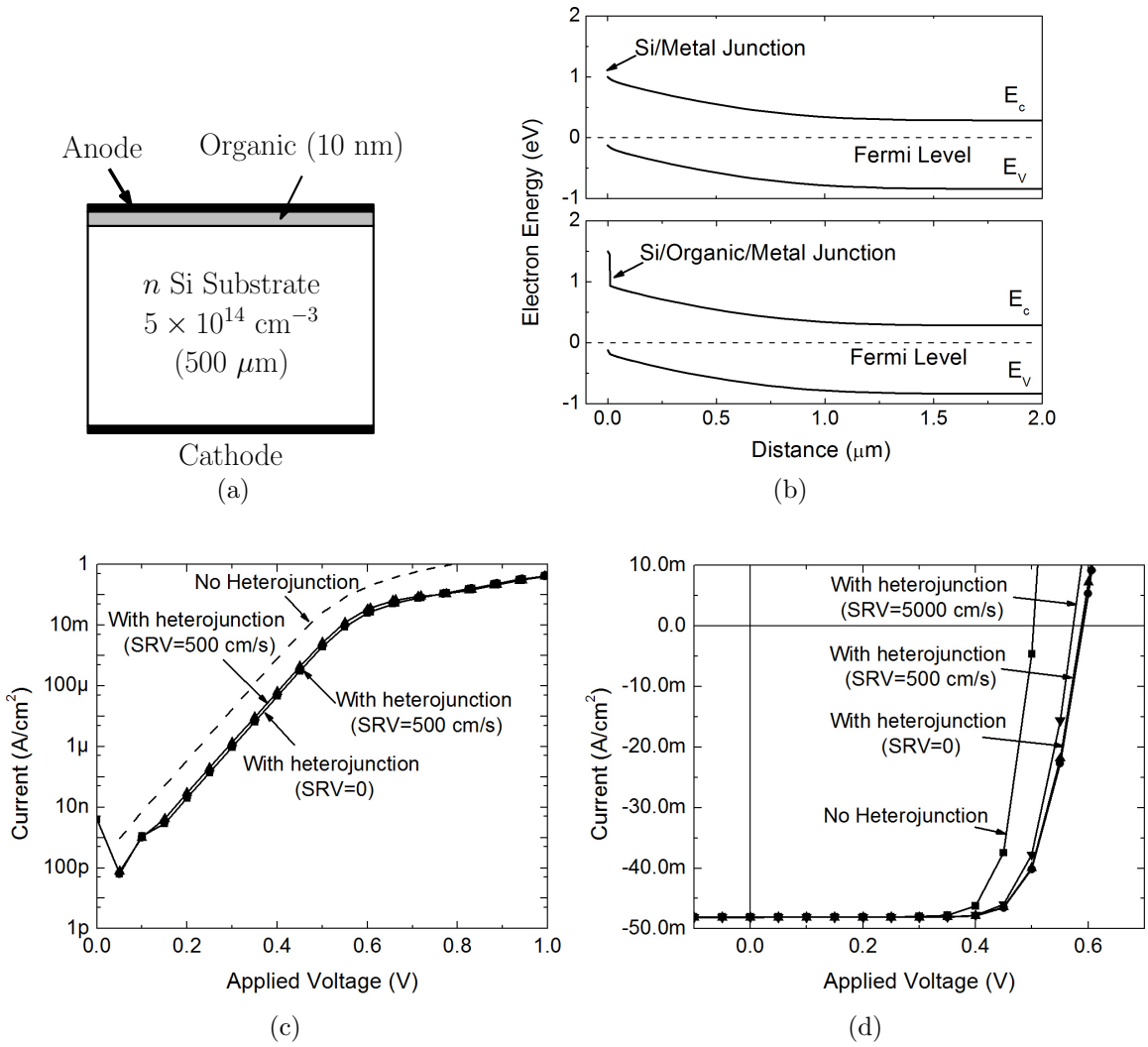


Figure 5.2: (a) The structure and (b) The band diagram of a metal-organic-silicon diode used in simulations. The inset shows the heterojunction at the top of the structure in more detail. (c) The simulated current-voltage characteristics in dark and (d) under a illumination of ≈ 1.1 Sun illumination, for a device with and without heterojunction. Non-ideal heterojunctions with non-zero surface recombination velocity are also shown. Performance of the cell has a relatively weak dependence on surface recombination velocity.

approximately 1.1 Sun (photon-flux of 3×10^{17} cm^{-2}), the depletion region in the two devices cause the same photocurrent in both the devices, but the lower dark-current allows a higher open-circuit voltage in heterojunction device. From the results it is clear that a) heterojunctions can yield diodes with lower J_0 than metal/Si diodes and b) that the built-in electric field in a heterojunction can efficiently separate photo-

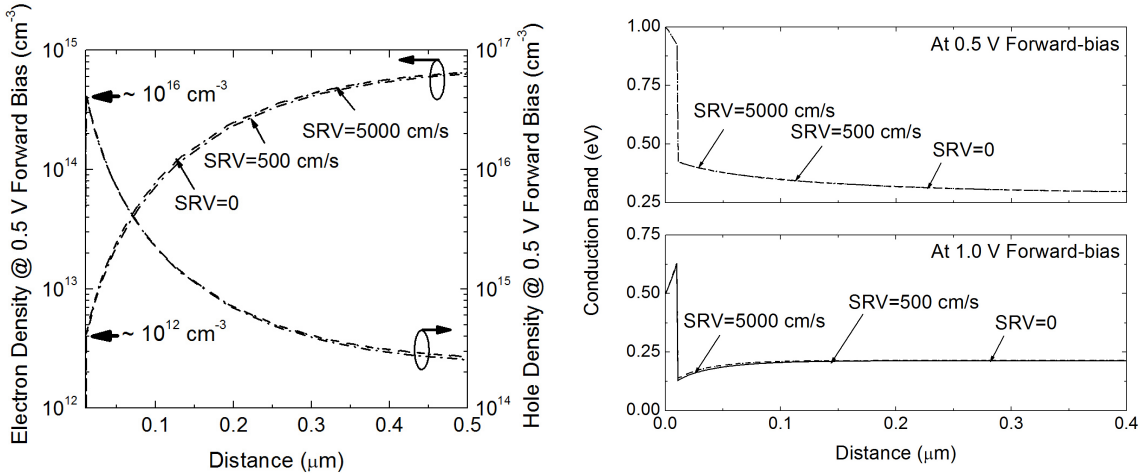


Figure 5.3: (a) The simulated electron-density profile at the silicon/organic interface at 0.5V forward bias and 1.1 Sun illumination. (b) The simulated conduction band profile at the silicon/organic interface at 0.5 V forward bias under 1.1 Sun. Notice there is an electric field in silicon that responsible for the keeps electrons away from the interface.

generated carriers to yield a photocurrent.

One interesting aspect of the structure is its relatively weak dependence on surface recombination velocity of the silicon/organic interface. Unlike the p-type contact structure of Fig. 4.3, which is very sensitive to surface recombination (Chapter 4), the dark-currents in the structure of Fig. 5.2(a) are low even for a device with fairly high surface-recombination-velocity of 5000 cm/s (Fig. 5.2(c)). Under illumination, the surface recombination does degrade the open-circuit voltage but the effect is marginal (Fig. 5.2(d)).

To better understand the reason behind the weak dependence of currents on surface recombination, the current lost to recombination can be analytically estimated. The rate of surface recombination depends not only on the surface recombination velocity (s in cm/s), but also on the electron and hole density near the surface (n_s

and p_s in cm^{-3}).

$$U_{surface} = s\frac{n_s p_s - n_i^2}{n_s + p_s + 2n_i}$$
$$\approx s n_s \tag{5.1}$$

The approximation is valid because under illumination $p_s, n_s >> n_i^2$, and at the edge of the depletion region, $p_s >> n_s$. In the simulated diode, at 0.5 V forward bias and 1.1 Sun illumination, the electron and hole densities at the silicon surface are only $\approx 10^{12}$ cm^{-3} and $\sim 10^{16}$ cm^{-3}, respectively (Fig. 5.3(a)). The current lost due to surface recombination is directly related to the rate of surface recombination (U).

$$J_{loss,SRV} = qU$$
$$= qsn_s \tag{5.2}$$

So even for a large SRV of 5000 cm/s, the current lost due to surface recombination is only $\approx$0.5 mA, i.e a loss of only around 1% of the total photocurrent. The reason for such a low surface carrier density is the depletion region that exists at the silicon surface due to work function difference between anode and n-type silicon (Fig. 5.2(b)). As the voltage increases from 0.5 V to 1 V the surface field starts to reduce till it turns negative (Fig. 5.2(b)), and effect of surface recombination starts to affect the currents (Fig. 5.2(d)). However, near the peak-power point of the solar cell (around 0.5 V), the recombination losses are insignificant.

5.3 Silicon/Pentacene Heterojunction

5.3.1 Pentacene

Pentacene is a well known hole-conducting organic small molecule, with HOMO and LUMO edges at 5.1 eV and 3.2 eV, respectively [106]. The silicon band edges are at 5.17 eV and 4.05 eV for E_V and E_C, respectively, and so the silicon/pentacene interface is expected to have a large E_C/LUMO barrier (0.8 eV) but a negligible E_V/ HOMO barrier. Another motivation for choosing pentacene to form the heterojunction was its high field-effect hole mobility, which in the best crystalline films is >1 cm^2/V·s [107]. The bulk-mobility of pentacene in amorphous thin-films is, however, considerably lower and bulk resistivity of 10^{14} Ωcm have been reported [108]. The high resistivity of amorphous pentacene films, as we shall in the last paragraph of this section, is an issue with these devices.

5.3.2 Device Fabrication

Sublimed pentacene was bought from H. W. Sands and was deposited on silicon by thermal evaporation using the Angstrom Evaporator in C405A. Prior to pentacene deposition, silicon wafers were cleaned and PQ-passivated by the method described in Section 3.6.

Test structures with a Si/PQ/pentacene heterojunction were fabricated on crystalline CZ n- and p-type Si substrates (Fig. 5.4(a) & (c)). The function of the PQ layer was to passivate the silicon surface. The pentacene layer was supposed to set the effective band-offsets of the Si/organic heterojunction because the PQ layer is very thin. The top electrode was patterned by a shadow mask with an active area of 3.1×10^{-2} cm^2 (1-mm radius circles). Adjacent devices were not explicitly separated. Rather it was assumed that the high lateral-resistance of the organic layer would be enough to prevent any current spreading, and the device area would be defined by

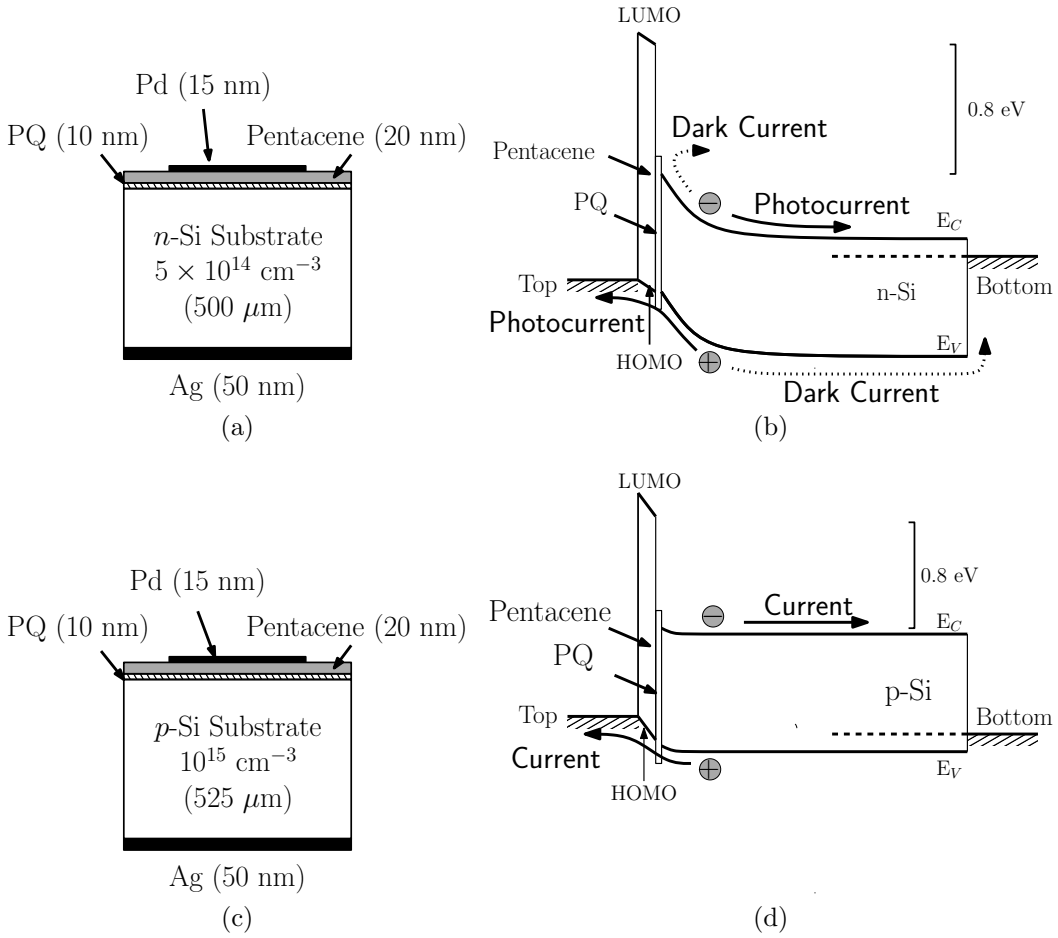


Figure 5.4: (a) Structure and (b) expected band structure of a n-Si/PQ/pentacene test device at a small positive voltage on top electrode. (c) Structure and (d) expected band structure of a p-Si/PQ/pentacene test device at a small negative voltage on top the electrode. It is assumed that carriers tunnel through PQ.

the top electrode. The top electrode was designed to be semi-transparent, by making the metal (Pd) very thin (15 nm), allowing the transmission of some of the incident light to Si. All electrical measurements were done using the Agilent 4155 parameter analyzer.

All spectroscopic measurements were performed in Prof. Kahn's lab by Dr. Yabing Qi.

5.3.3 Current-Voltage Characteristics of Silicon/PQ/Pentacene Heterojunctions

We initially assumed that the passivating PQ layer is thin enough that carriers can tunnel through, so the band structure of PQ is not considered in the band digram of Fig. 5.1(c). The n-Si/pentacene device is expected to have a large electron barrier at the Si/organic heterointerface (Fig. 5.4(b)) and should function like a heterojunction diode. For the case of p-Si, there is no equivalent barrier for holes to from silicon to the top contact and the structure should simply function as a resistor (5.4(d)).

For n-Si/pentacene/metal heterojunction, experimentally measured dark I-V characteristics are diode-like. The J_0 of the pentacene device is lower than the J_0 of an equivalent Si/metal device (Fig. 5.5(a)). This suggests that the electron barrier-height at the semiconductor/metal interface is larger in the pentacene device than in the Shcottky barrier device, arguably due to the larger conduction band offset. Under illumination, the field in silicon helps separate the photogenerated carriers, and an open-circuit voltage of 0.37 V is observed, which is higher than the open-circuit voltage of the Si/metal device (Fig. 5.5(a)).

The thin Pd is semi-transparent. With no heterojunction, i.e. for the n-Si/metal Schottky diode, the short-circuit current is approximately 2.1 mA/cm^2. The measured value of short-circuit current in n-Si/PQ/pentacene device is not only far lower, only 0.45 mA/cm^2, but also increases with negative bias, giving an 'S' shaped characteristics (Fig. 5.5(b)). The voltage dependence suggests that the lower photocurrent at zero-bias is not due to poor light absorption, since higher internal electric field is not expected to improve absorption. Intuitively too, poor absorption should not be the problem because most of the light absorption is expected to occur in silicon, which is known to have a high light absorption efficiency. More likely, the problem is in carrier collection - photogenerated holes are not being efficiently collected at the top electrode.

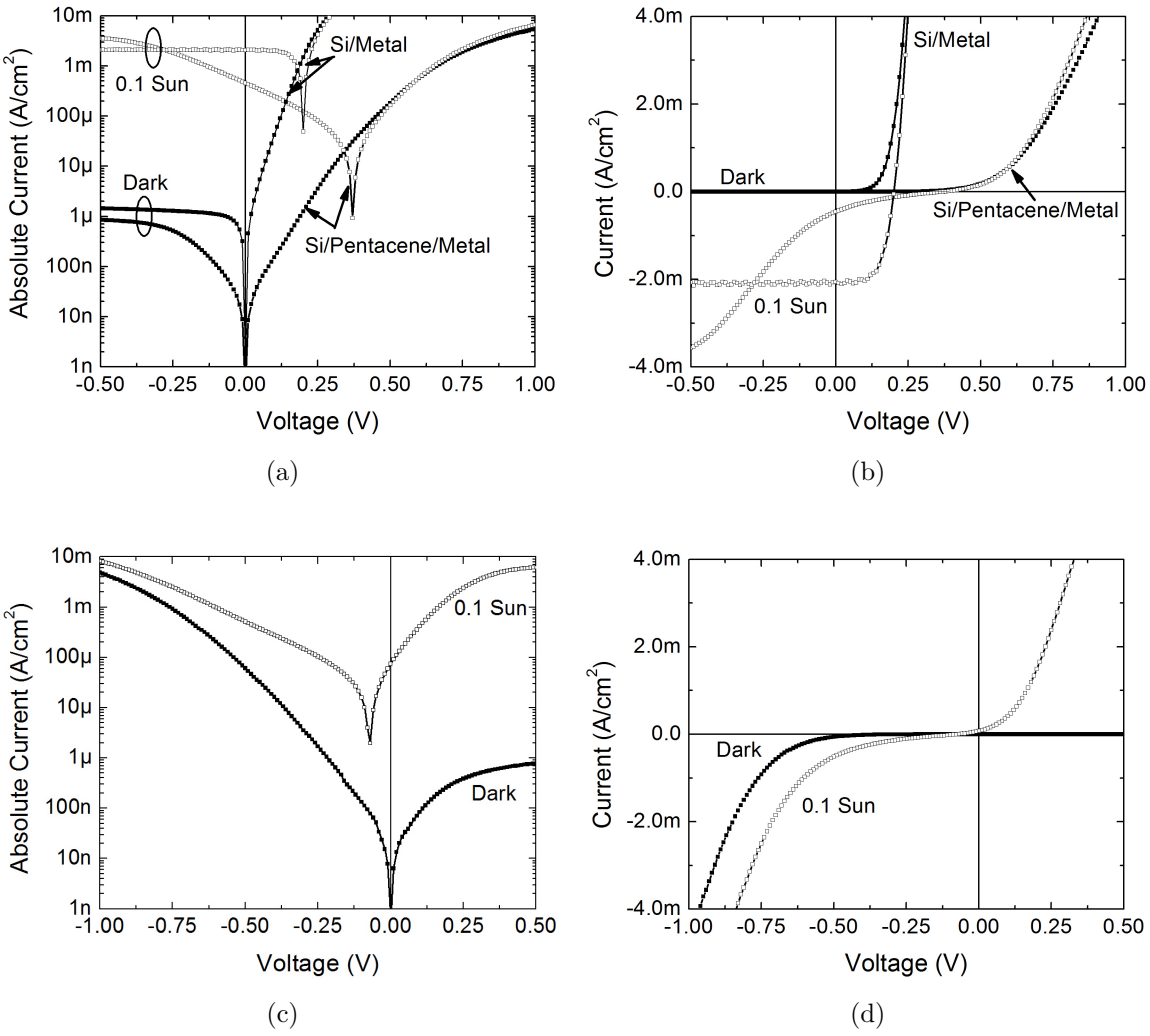


Figure 5.5: I-V characteristics of n-Si/PQ/pentacene heterojunction of Fig. (a) in dark and $\approx$ 0.1 Sun illumination plotted on (a) log and (b) linear scale. I-V characteristics of p-Si/PQ/pentacene heterojunction of Fig. (c) dark and $\approx$ 0.1 Sun illumination plotted on a (c) log and (d) linear scale.

One hypothesis for the poor collection could be that valence band offset at the Si/organic interface is not zero but significant. At positive bias the barrier blocks the flow of photogenerated holes from silicon to anode, leading to a lower photocurrent (Fig. 5.6(a)). As the bias is made more negative, the field at the surface increases and more of the carriers are able to cross the valence-band barrier to get collected at the anode, leading to a higher photocurrent (Fig. 5.6(b)).

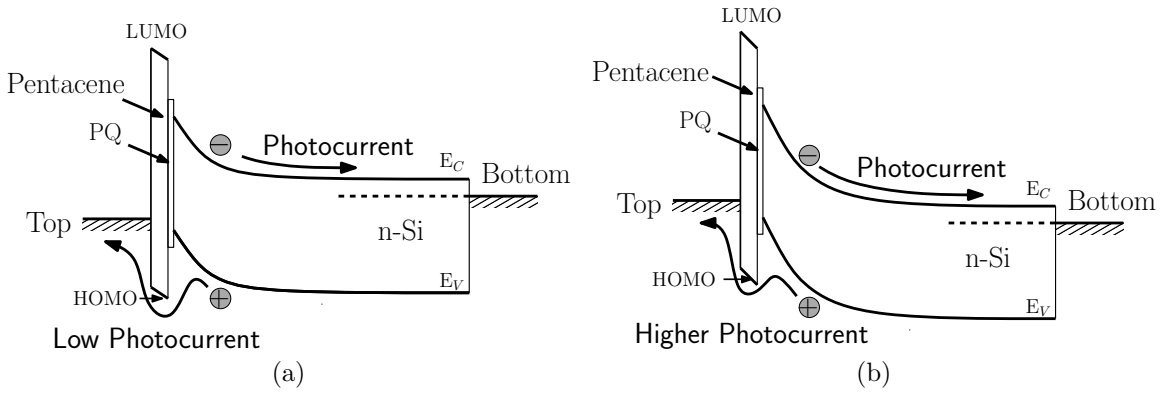


Figure 5.6: Effect of surface field on photocurrent when the n-Si/PQ/pentacene diode has a valence band offset. Band structure at (a) positive-bias and (b) negative-bias. Photocurrent is higher in negative-bias.

The dark characteristics for p-Si/PQ/pentacene heterojunction are not ohmic but diode-like and under illumination a small open-circuit voltage is observed (0.07 V), hinting at the presence of a small internal electric field in silicon (Fig. 5.5(c)). These observations too can be explained by considering a small valence-band offset at the Si/organic interface (Fig. 5.5(c)). The photocurrent on the p-Si diode also shows a bias voltage dependence ('S' shaped characteristics of Fig. 5.5(d)), suggesting poor collection of electrons at the top electrode. However this is expected because we expect a LUMO/conduction-band barrier.

In summary, I-V characteristics of the PQ-passivated Si/pentacene heterojunctions are not consistent with the band structure of Fig. 5.4(b) & (d). There is evidence that not just the electrons, but holes also see a barrier at the Si/organic interface. The hole-barrier could be present either because of HOMO of pentacene does not align with the conduction band edge of silicon or because PQ is not thin enough and the carriers are being blocked at the Si/PQ interface.

5.3.4 Spectroscopy of the Silicon/PQ/Pentacene Heterojunction

To investigate the reasons for the anomalous I-V characteristics, the band-alignment of the Si/PQ/pentacene heterojunction was studied using X-ray and ultra-violet photoelectron spectroscopy (XPS & UPS).

For the experiment PQ-passivated n^+ and p^+-Si samples loaded into the UHV chamber and the band-alignment and Si band bending were measured using the same process described in Section 3.6.3. The band-bending in PQ-passivated silicon was higher than measured before (Table 3.2), 0.4 eV and 0.3 eV for n-Si and p-Si, respectively, suggesting imperfect passivation but the band-offsets at the Si/PQ interface were consistent with previous experiments (Fig. 3.11).

Next, pentacene was deposited (in-situ) at a very slow rate on top of the Si/PQ interface. At regular intervals pentacene deposition was paused and UPS spectrum was measured again. Plotting the work-function (Φ) and ionization energy (IE) as a function pentacene thickness (Fig. 5.7(a) & (c)), allows us to observe the evolution of the Si/PQ/pentacene interface for the first few nm of pentacene. After only 2-3 nm the energy levels of pentacene stabilize, suggesting that most of the interface effects have been accounted for and bulk properties of pentacene dictate properties for thicker films.

The Si/organic valence-band offset ($\Delta E_{V,org}$) in any system is the difference between the ionization energies of the Si/organic interface (IE_{org}) and silicon surface(IE_{Si}), adjusted for the 'net' interface dipole ($\Delta ID_{Si/org}$).

$$\Delta E_{V,org} = IE_{org} - IE_{Si} + \Delta ID_{Si/org} \tag{5.3}$$

Assuming IE_{Si}, i.e. energy of the valence-band edge, for pristine silicon is 5.2 eV [95], the band offset for Si/pentacene interface ($E_{V,pent}$) can be calculated. For n^+-

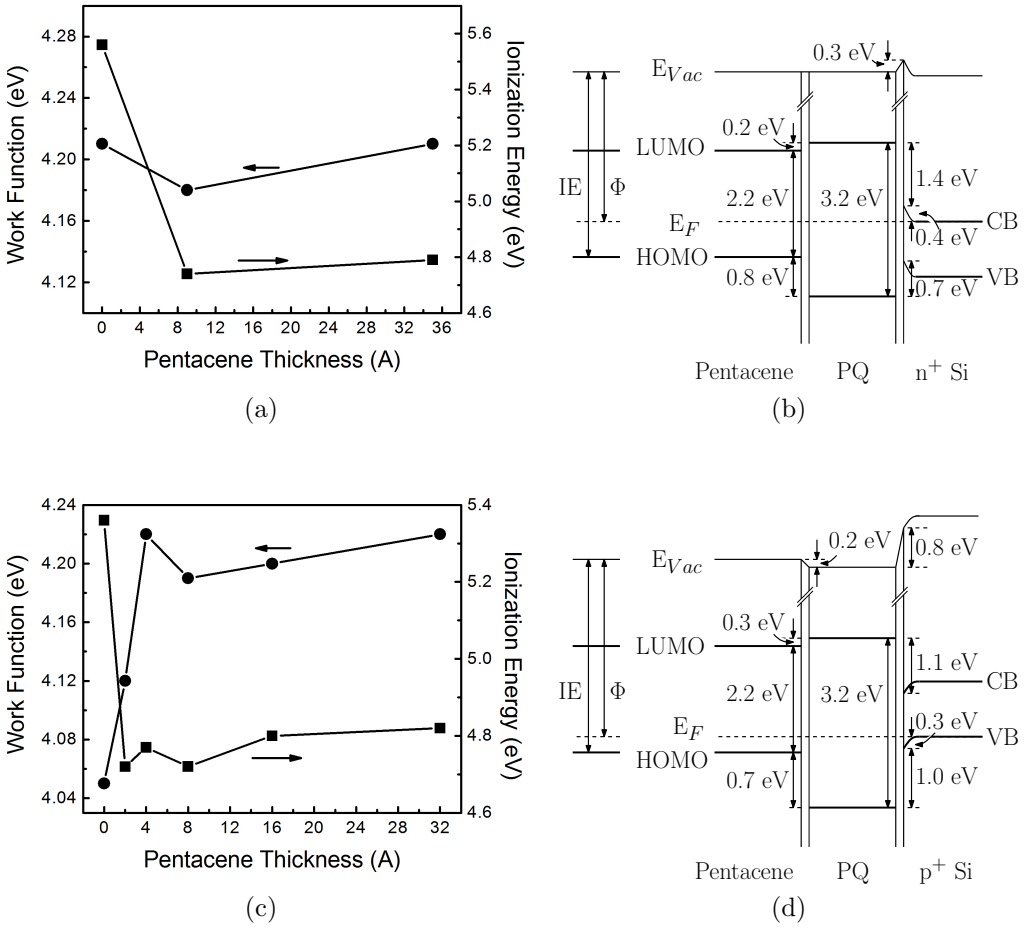


Figure 5.7: (a) Evolution of work-function and ionization energy as a function of pentacene thickness for n-Si/PQ/pentacene heterojunction. The data at zero thickness represents the underlying n-Si/PQ interface. (b) The band alignment at the n-Si/PQ/pentacene interfaces. (c) Evolution of work-function and ionization energy as a function of pentacene thickness for p-Si/PQ/pentacene heterojunction. The data at zero thickness represents the underlying p-Si/PQ interface. (b) The band alignment at the n-Si/PQ/pentacene interfaces.

Si and p^+-Si the measured valence band-offset for pentacene ($\Delta E_{V,pent}$) is -0.1 and 0.2 eV, respectively (Table 5.1). While not perfectly zero, these offsets are in the ballpark of our original assumption that $\Delta E_{V,pent} \approx 0$, suggesting that pentacene is not responsible for the valence band offset. The only other source of a valence band offset is the passivating PQ-layer. Similar calculation done on the data presented in Fig. 3.11 (Section 3.6.3) for the valence band-offset at Si/PQ interface reveals a large

Table 5.1: Measured ionization energy (IE), interface dipoles, and valence-band offset (ΔE_V) at Si/pentacene and Si/PQ interface for n^+-Si and p^+-Si. IE_{Si} is assumed to be 5.17 eV.

Interface	n^+-Si			p^+-Si		
	IE_{org} (eV)	$\Delta ID_{Si/org}$ (eV)	$\Delta E_{V,org}$ (eV)	IE_{org} (eV)	$\Delta ID_{Si/org}$ (eV)	$\Delta E_{V,org}$ (eV)
Si/pentacene	4.8	0.3	-0.1	4.8	0.6	0.2
Si/PQ	5.6	0.3	0.7	5.4	0.8	1.0

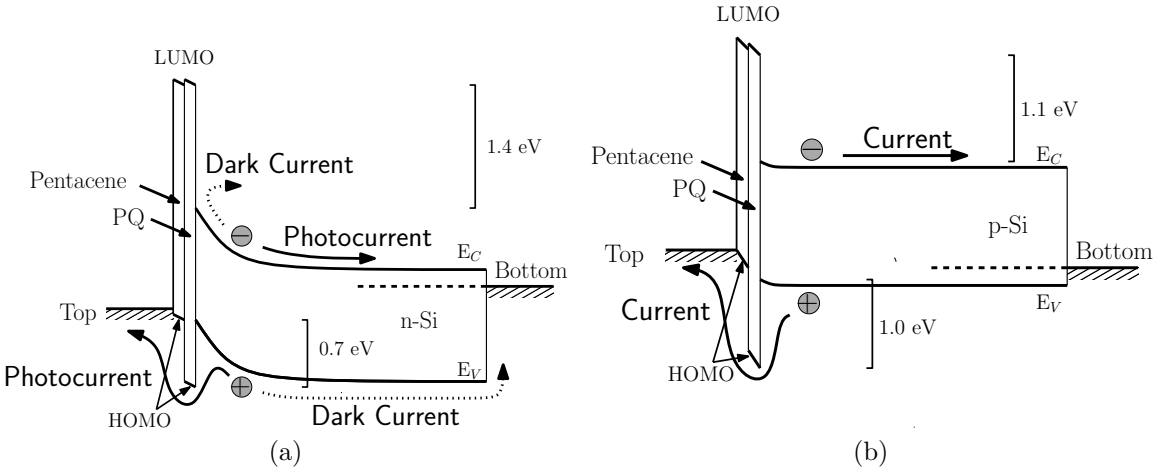


Figure 5.8: Band structure of the Si/PQ/pentacene heterojunction devices based on data from the spectroscopy. (a) Device on n-type Si at a small positive voltage on top electrode.(d) Device on p-type Si device at a small negative voltage on top the electrode.

barrier (0.7 to 1.0 eV) at both n^+ and p^+-Si surfaces (Table 5.1). So if PQ is not thin enough for carrier tunneling, holes in silicon could experience a barrier and the I-V characteristics would be limited by the properties of the Si/PQ interface and not the Si/pentacene interface.

Data from spectroscopic measurements shows that if there is a valence-band offset, then the most likely culprit is not the pentacene layer but PQ. Most likely, the carriers are unable to tunnel through the PQ layer. Assuming that the trend of the spectroscopic data is the same for lightly and highly doped Si, the revised band structure of the Si/PQ/pentacene heterojunction, which includes the PQ band structure,

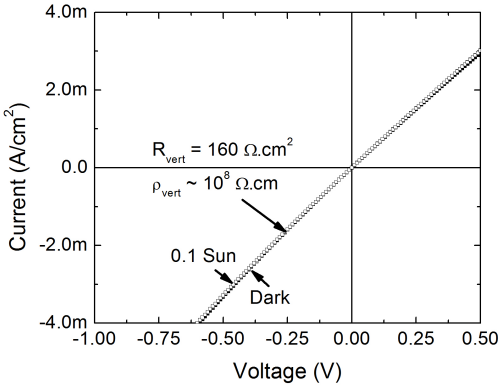
is shown in Fig. 5.8.

5.3.5 Improved Silicon/PQ/Pentacene Heterojunction Solar Cell

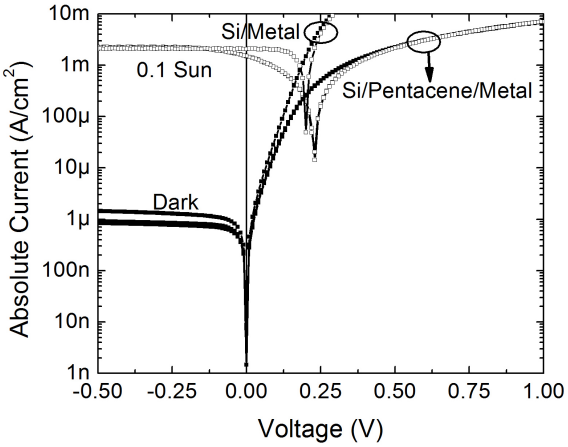
If the large valence-band offset at the Si/PQ layer is the reason for poor hole collection in Si/PQ/pentacene devices, then thinner PQ layers should help. Once the thickness of the PQ layer is reduced sufficiently, carriers will be able to tunnel through the barriers at the Si/PQ interface. Devices with thinner PQ layers, 2 nm as opposed to 10 nm, were fabricated to test the hypothesis. To reduce the large series resistances observed in previous sets of devices, the pentacene thickness was also reduced to from 20 nm to 5 nm.

The measured J-V characteristics of the p-Si device are ohmic (Fig. 5.9(a)) with a specific contact resistance (R_{vert}) of $\sim$ 100 kΩcm^2, confirming that the hole barrier is negligible at all the Si/organic interfaces. Assuming that most of the resistance is due to the 7 nm (5 nm of pentacene and 2 nm of PQ) thick organic layers, the resistivity (ρ_{vert}) of the organic layer stack is calculated to be $\sim 10^8$ Ωcm. Dark characteristics of the n-type device are still diode-like, and under illumination an open-circuit voltage of 0.23 V is observed (Fig. 5.9(b)). The short-circuit current is $\approx$ 2.2 mA/cm^2 - in line with what we expected from 0.1 Sun illumination through the semi-transparent metal (Fig. 5.9(c)). There is no 'S' shape curve, and the photocurrent is independent of bias-voltage. The R_{vert} and ρ_{vert} of this device are consistent with the values measured for the p-type Si device. Overall, the Si/(thin)PQ/pentacene interface functions as an electron-blocking heterojunction.

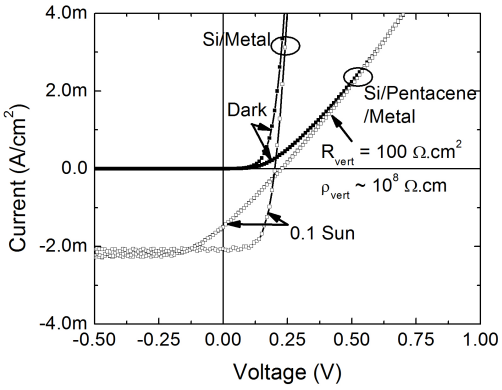
Unfortunately, the photovoltaic performance of the device is not very good. While the short-circuit current is high, the obtained open-circuit voltage is barely higher than the Si/metal control diode (0.23 V instead of 0.2 V), and is too low for a practical solar cell.



(a)



(b)



(c)

Figure 5.9: (b) J-V characteristics of the p-Si/PQ/pentacene device with thinner organic layers (2 nm of PQ and 5 nm of pentancene) in dark and ≈ 0.1 Sun illumination plotted on a linear scale. (c) J-V characteristics of the n-Si/PQ/pentacene device solar cell with thinner organic layers (2 nm of PQ and 5 nm of pentacene) in dark and ≈ 0.1 Sun illumination plotted on a log and (b) linear scale.

One reason for the low V_{OC} could be that we reduced the thicknesses of the pentacene layer too much, and somewhere between 5 nm and 15 nm is a pentacene thickness that will yield a higher V_{OC}. Unfortunately, such an optimization is not useful simply due to the high series resistance of the device. For just for 5 nm thick pentacene layer the measured specific contact resistance is around 100 Ω.cm^2 ($\rho_{vert} \sim$ 100 MΩcm). The vlaue of resistivity is lower than some previously reported values, e.g. 10^{14} Ωcm [108], but it is still a very high number. The expected I^2R loss at 1 sun

illumination (current density of ~ 40 mA/cm^2, assuming an ideal photocurrent for a silicon solar cell) is 160 W/cm^2. Since the incident light at 1 sun is only 100 mW/cm^2, power dissipation due to the resistance will overwhelm any power generated. A more conductive organic is required to make a practically useful heterojunction.

The implied bulk mobility of holes (μ_h) in the organic stack can be calculated from the measured value of ρ_{vert}. Since pentacene is a hole conductor the resistivity (ρ_{vert}) can be written as

$$\rho_{vert} = \frac{1}{qp\mu_h} \tag{5.4}$$

Ideally at 1 Sun, the photon-flux in a solar cell is on the order of 10^{17} cm^{-2}. Assuming a silicon wafer thickness of 500 µm, the carrier density in the device is on the order of 10^{18} cm^{-3}. The carrier density in the organic layer should be of the same order. So the implied bulk-mobility of the organic layer is

$$\begin{aligned} \mu_h &= \frac{1}{qp\rho_{vert}} \\ \Rightarrow \mu_h &\sim 10^{-7} \quad cm^2/Vs \end{aligned}$$

In comparison, the required value of μ_h for the organic, such that voltage drop across the organic layer (ΔV_{org}) is less than 10 mV at the current density (J) expected at 1 Sun (40 mA/cm^2), is

$$\begin{aligned} R_{vert} &< \frac{\Delta V_{org}}{J} \\ \Rightarrow R_{vert} &< 0.25 \quad \Omega cm^2 \\ \Rightarrow \rho_{vert} &< 50 \quad k\Omega cm \\ \Rightarrow \mu_h &> 2 \times 10^{-4} \quad cm^2/Vs \end{aligned} \tag{5.5}$$

5.4 Silicon/Poly(3-hexylthiophene) Heterojunction

5.4.1 Poly(3-hexylthiophene)

Poly(3-hexylthiophene) (P3HT) is a well known organic polymer, with HOMO and LUMO edges at 5.0 eV and 2.8 eV, respectively [9]. Comparing to silicon energy levels of 5.17 eV and 4.05 eV for E_V and E_C, respectively, we expect a the silicon/P3HT interface with a large E_C/LUMO barrier (0.8 eV) and a negligible E_V/ HOMO barrier. One reason we switched from pentacene to P3HT is ease of processing - P3HT is a polymer that, unlike PQ or pentacene, can be dissolved in a solvent to form an ink that can be spin-coated on top of silicon. The second reason was the need for a more conductive organic layer. Finally, P3HT boasts a thin-film bulk-mobility of $\sim 10^{-4}$ $cm^2/V{\cdot}s$ [109], which is high enough to satisfy the mobility threshold calculate in (5.5).

Structures similar to the Si/pentacene diodes were made with P3HT. The one major change was that silicon was not passivated by PQ prior to P3HT deposition. The reasons for this design decision will be explained later, but they relate to the fact that surface recombination is not very important in these devices.

5.4.2 Device Fabrication

P3HT deposition were done using the recipes provided by the Prof. Lynn Loo's group in the Department of Chemical Engineering. First, P3HT inks were formulated by dissolving the requisite amount P3HT in chlorobenzene and agitating the solution by a magnetic stirrer on a hot plate set at 90℃, till the particles of P3HT dissolved away and the solution turned clear. Typically this took only around a minute. Though the solution was formulated in air, the P3HT stock and inks were stored in a glove box under inert atmosphere. To prevent photoinduced degradation, solutions were stored in dark-tinted vials. P3HT was bought from Merck KGaA under the brand name

Table 5.2: The spin-coating recipes of P3HT used in this work. Thicknesses were measured by the Tencor profilometer.

Solution Formulation		Spin-Coating Conditions			Thickness (nm)
Concentration (gm/ml)	Solution	Spin Speed (rpm)	Acceleration (rpm/s)	Time (s)	
0.500%	Chlorobenzene	1000	1000	120	25
0.250%	Chlorobenzene	1000	1000	120	10
0.125%	Chlorobenzene	1000	1000	120	5
0.062%	Chlorobenzene	1000	1000	120	2
0.250%	Chlorobenzene	6000	1000	120	8

SP001 Lisicon^{TM} (Batch number EE98202) with a stated average molecular weight (M_W) of 46115 gm/mol. Chlorobenzene was bought from JT Baker (CMOS Grade).

Prior to depositing P3HT, silicon (100) substrates were first rinsed in solvents to remove organic impurities - acetone, methanol and 2-propanol in an ultrasonic bath for 5 minutes each. Next, trace metal contaminants were removed by the standard RCA clean - first SC-1 step: Ammonium hydroxide + hydrogen peroxide + DI Water (1:1:5) at 80° for 15 minutes, followed by 1:100 hydrofluoric acid for 1 min, and finally SC-2 step: hydrogen chloride + hydrogen peroxide + DI Water (1:1:5) at 80° for 15 minutes [78]. Lastly, the wafers were dipped in a 1:100 aqueous hydrofluoric acid solution for 1 min to strip the native oxide layer. On the resulting hydrogen-passivated Si wafers, P3HT was spin-coated from a pre-formulated P3HT solution. Table 5.2 shows the various recipes used in this work and the resulting P3HT layer thickness. Unless otherwise specified, no thermal processes were used to dry the P3HT layer.

The depletion region in silicon is set by the difference in the work function of the top electrode and silicon. For high V_{OC} the depletion region should be as large as possible. Since the substrate were n-Si, high-work function metals were preferred for top electrode. Best results were obtained with palladium, though devices with gold were also fabricated. The bottom electrode was a simple ohmic contact to the silicon.

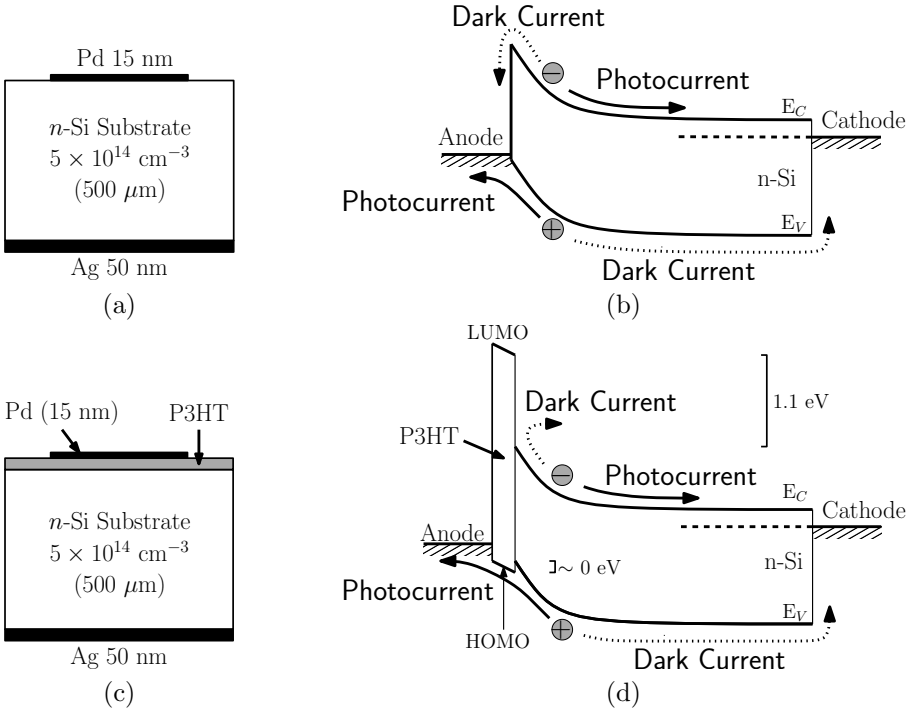


Figure 5.10: (a) Structure and (b) expected band structure of a Si/metal Schottky test device which serves as the control. (c) Structure and (d) expected band structure [9] of the heterojunction device test device used to evaluate effect of Si/P3HT heterojunction.

Due to the large area surface and etched surface, ohmic Si/metal contacts were formed quite easily on the backside. Metals used were either aluminum or silver. Electrodes were deposited by thermal evaporation in the Angstrom Evaporator in C405A. The top electrode was patterned by a shadow mask with an active area of 3.14×10^{-2} cm^2 (1-mm radius circles). The top electrode was also kept very thin (15 nm) so that it is semi-transparent, allowing some of the light to be absorbed in Si. All electrical measurements were done using the Agilent 4155 parameter analyzer, HP 4175 LCR meter, and Techtronix oscilloscope. For AM 1.5 measurements, a xenon-lamp solar simulator was used.

To investigate Si/P3HT heterojunctions, tests structures with and without P3HT were fabricated (Fig. 5.10) on crystalline phosphorous-doped silicon wafers.

5.4.3 Band Modulation at the Unpassivated Si/P3HT Heterojunction

Unlike the Si/PQ/pentacene heterojunction diodes, the silicon surface at the Si/P3HT heterojunction in the test devices is unpassivated (Fig. 5.10(c)). There are thee major reasons for this design decision:

(a) PQ causes series resistance and valence-band offset in devices, both of which degrade photovoltaic performance (as demonstrated in the previous section.).

(b) Surface passivation is not very crucial in this type of heterojunction device and hydrogen passivation should be sufficient, as demonstrated by simulations in Section 5.2.

(c) PQ passivation did not seem stable under solvent processing (Section 6.3.3). So there was concern that PQ would get washed away while spin-coating P3HT on silicon.

However, to obtain a photocurrent there still needs to be an electric field in silicon that can separate the photogenerated carriers. If the surface defect pin the Fermi-level such that there was no depletion region in silicon, the device would be unable to generate a photocurrent. To confirm, the presence of such an electric field at the unpassivated silicon/P3HT surfaces, the small signal capacitance-voltage (C-V) characteristics of the test diodes were measured at 1 MHz.

The capacitance measured in a typical Si diode, is due to the depletion region in silicon (C_{Si}), which has a characteristic dependence on appied voltage across the depletion region (V_{Si}) as [110].

$$\frac{1}{C_{Si}^2} = \frac{2}{q\epsilon_{Si}N_{Si}}\left(V_{bi} - V_{Si}\right) \tag{5.6}$$

where, q is the electronic charge, ϵ_{Si} is the permittivity of Si, N_{Si} is the Si substrate doping, and V_{bi} is the built-in voltage. In a Schottky junction such a depletion region exists at the silicon surface, as confirmed by the linear dependence of $1/C^2$ on V_{Si} for Si/metal diodes ('No P3HT' curve of Fig. 5.11(b)).

For the Si/P3HT heterojunction devices, the measured capacitance ($C_{measured}$) and applied voltage ($V_{applied}$) include contribution from not just the depletion region (C_{Si}) but also the organic layer (C_{org})

$$\frac{1}{C_{measured}} = \frac{1}{C_{Si}} + \frac{1}{C_{Org}} \tag{5.7}$$

$$V_{applied} = V_{Si} + V_{Org} \tag{5.8}$$

where V_{Org} is the voltage drop across organic layer. The capacitance due to the thin organic layer can be approximated by

$$C_{org} = \frac{\epsilon_{Org}}{t_{org}} \tag{5.9}$$

To extract the values of C_{Si} and V_{Si} in the heterojunction devices from the measured values, following equations can be used:

$$\frac{1}{C_{Si}} = \frac{1}{C_{measured}} - \frac{1}{C_{Org}} \tag{5.10}$$

$$V_{Si} = V_{applied} - \frac{q\epsilon_{Si}N_{Si}}{C_{Org}C_{Si}} \tag{5.11}$$

Irrespective of P3HT thickness, the resulting $1/C_{Si}^2 - V_{Si}$ curves are linear with the same slope (Fig. 5.11(c)). From the slope, the value of implied Si substrate doping as function of distance can be extracted (Eq. (5.6)), which suggests that Si is uniformly doped with doping density of $\sim 4\times10^{14}$ cm^{-3} - consistent with expected

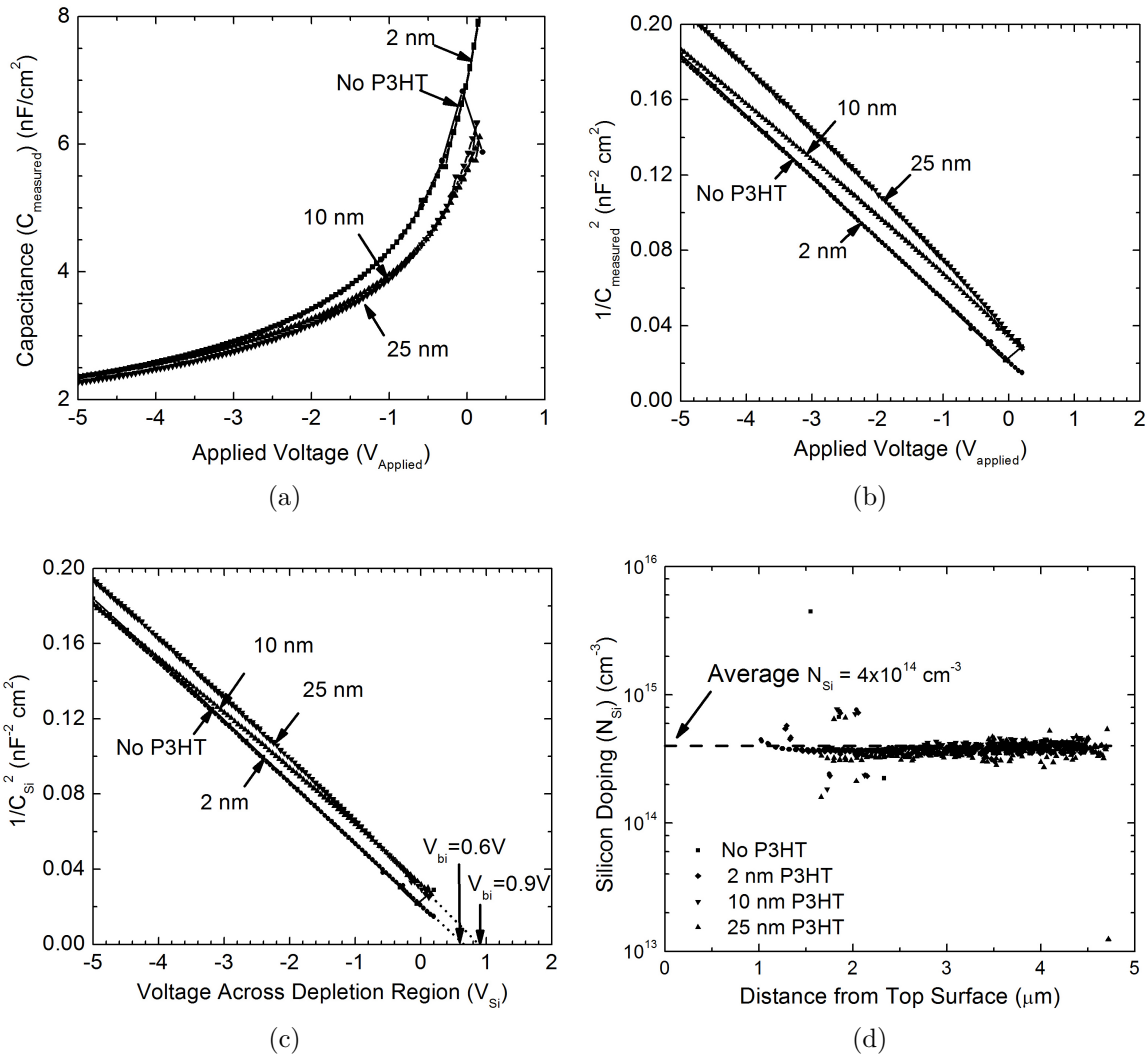
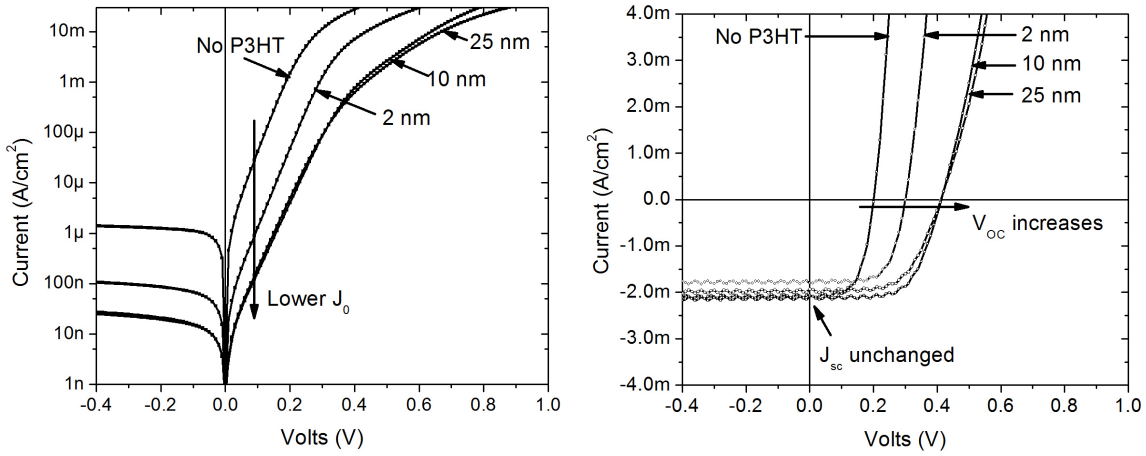


Figure 5.11: (a) Small signal capacitance of n-Si/P3HT heterojunctions with different P3HT layer thicknesses. (b) $1/C^2$-V characteristics the same n-Si/P3HT heterojunctions. (c) $1/C_{Si}{}^2$-V_{Si} characteristics extracted from the raw data using Eq. (5.10) & (5.11). (d) Implied silicon substrate doping for different Si/P3HT devices.

n-type doping density of the 10-20 Ω.cm wafer used in these experiments. The built-in voltage inferred from the x-axis intercept varies from ∼0.6 V for metal/Si devices to ∼ 0.9 V for thicker P3HT layers. Quantitatively, the difference in V_{bi} may not be significant, but qualitatively it proves the existence of a depletion region in silicon that can separate photogenerated carriers.



(a) (b)

Figure 5.12: (a) Current-voltage characteristics of Si/P3HT heterojunction diodes in dark with different P3HT layer thicknesses. (a) Current-voltage characteristics of the same devices under $\sim$ 0.1 sun illumination from a microscope light.

5.4.4 Band Alignment at the Silicon/P3HT Heterojunction

To experimentally verify that the Si/P3HT interface satisfies the band-alignment criteria, the current-voltage characteristics with and without light were measured for the test diodes.

The current-voltage characteristics measured in the dark for the different thicknesses of the P3HT layer (2, 10 and 25 nm) and a control device without P3HT are shown in Fig. 5.12(a). Clearly the currents in forward and reverse-bias are lower for devices with thicker P3HT films. The diode saturation current density (J_0), extracted from the intercept on the vertical axis from the semilog current-voltage graph in forward-bias, falls from a high of 9.2×10^{-7} A/cm^2 for diodes with no P3HT, to 7.0×10^{-9} A/cm^2 for diodes with 10-25 nm of P3HT. It is well known that the dark current in a Schottky diode is dominated by majority carrier injection of electrons into the metal anode [75], so this reduction in current in an n-Si device is clear evidence of reduced electron current.

P3HT is an ambipolar conductor that is known to conduct electrons [109]. So

it is conceivable that the current reduction observed in devices with thicker P3HT layers is purely due to the resistive drop across the P3HT. However in that case the current reduction would scale inversely and continuously with P3HT layer thickness - something not seen in the data of Fig. 5.12b. The observed initial current reduction is rapid and after a certain threshold (P3HT thickness of 10 nm) independent of P3HT layer thickness. This allows us to further that the reduction in electron current is strictly an interface effect due to the electron barrier at the Si/P3HT heterojunction.

To test the transport of holes, current-voltage characteristics of the same devices were measured under illumination from a microscope lamp Fig. 5.12(b). The intensity of the lamp caused a short-circuit current of ~ 4 mA/cm^2 in a commercial silicon diode with anti-reflection coating and no blocking metal, roughly corresponding to $1/10^{\text{th}}$ the intensity of sunlight. Since the top metal in these devices is semi-transparent, some of the carriers are expected to reach the underlying silicon layer, generating electrons and holes. At zero bias the photogenerated holes in silicon would flow from silicon to anode, across the Si/P3HT interface, giving rise to a photocurrent. As discussed in Section. 2.5 and Section 5.3.3, any hole-barrier at the hetero-interface, e.g. due to band-offset between the valence band of Si and the HOMO of P3HT, would impede the flow of photogenerated holes leading to a reduced short-circuit current. Experimental data suggests that this is not the case because in devices, both with and without P3HT, the values of short-circuit current were similar (~ 2 mA/cm^2) and not dependent on the applied voltage (in contrast Si/PQ/Pentacene devices shown in Fig. 5.5(b)). This points to a lack of a hole barrier at the Si/P3HT interface, so the HOMO of the P3HT must be closely aligned to the valence band edge of silicon.

The lower J_0 enables higher V_{OC} according to Eq. (1.4). This is reflected in the data, where under around 0.1 sun illumination, the V_{OC} increases from 0.20 V for Si/metal device to 0.41 V for the best Si/P3HT device.

Table 5.3: The extracted device parameters for Si/P3HT device parameters of Fig. 5.12. Implied J_0 calculated from Eq. (1.4), using measured V_{OC} and J_{SC} and Eq.(1.4).

P3HT thickness	Device Parameters				
(nm)	Extracted J_0 (A/cm^2)	n	J_{SC} (mA/cm^2)	V_{OC} (V)	Implied J_0 (A/cm^2)
No P3HT	9.2×10^{-7}	1.01	2.06	0.20	9.0×10^{-7}
2 nm	3.5×10^{-8}	1.06	1.80	0.30	1.6×10^{-8}
10 nm	7.0×10^{-9}	1.21	2.08	0.41	2.6×10^{-10}
25 nm	7.7×10^{-9}	1.18	1.93	0.41	2.4×10^{-10}

As mentioned before, the J_0 (as measured from the intercept on the y-axis) of the best Si/P3HT heterojunction device is lower than the J_0 of the Si/metal Schottky device, 7.0×10^{-9} A/cm^2 instead of 9.2×10^{-7} A/cm^2. However, other than the Si/metal Schottky device, whose n=1.01, the ideality factors of heterojunction devices are all greater than 1 - from 1.06 to 1.25. These high ideality factors affect the extraction of J_0 from the semilog characteristics, which conflates the comparisons between device. Fortunately, the ideality factors are not our primary concern, V_{OC} and J_{SC} are. From the measured V_{OC}, J_{SC}, and assuming $n = 1$ an "implied J_0" can be calculated from Eq. (1.4), i.e. the J_0 that an ideal diode should have to justify the measured V_{OC} at the measured J_{SC} (Table 5.3). To compare the performance of devices, "implied J_0" is a better metric than the extracted J_0. The implied J_0 of heterojunction devices is more than 3 orders of magnitude lower than the Si/metal device (Table 5.3).

Overall the results of Si/P3HT heterojunctions are consistent with the proposed theory and simulations of Section 2.5. At the Si/P3HT heterojunction, there exists an electric field in silicon that can separate photogenerated charge carriers, yielding a photocurrent. The n-type-Si/P3HT heterojunction blocks electrons due to the electron barrier, resulting in a lower saturation current density, but allows unimpeded transport of holes.

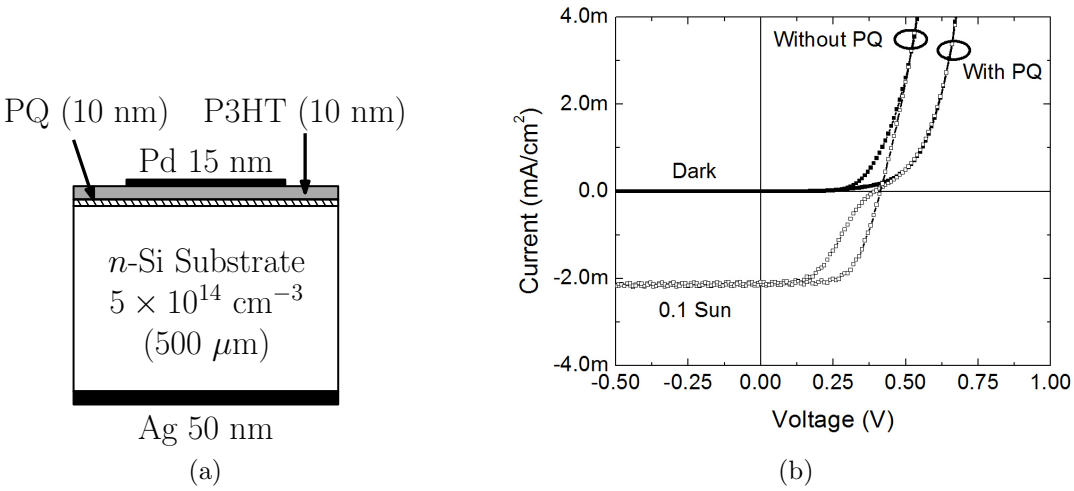


Figure 5.13: (a) Struture of a n-Si/P3HT heterojunction device with PQ passivation. (b) I-V characteristics of n-Si/P3HT heterojunction devices, in dark and under ~ 0.1 sun illumination, with and without PQ passivation.

5.4.5 Effect of PQ Passivation

Theoretically, Si passivation should reduce surface recombination at the top surface, leading to lower dark-current and higher open-circuit voltage. Unfortunately addition of PQ may also add a valence band offset which can impede hole collection and cause a loss in photocurrent (See the section on Si/PQ/pentacene diodes). To test the effect PQ passivation has on the I-V characteristics of the Si/P3HT heterojunction, test structures on PQ passivated n-Si were fabricated (Fig. 5.13(a)).

Compared to a device without PQ, the fill factors of device with PQ are worse, arguably due to the hole-barrier introduced by PQ (Fig. 5.13(b)). This loss is not compensated by any improvement in the open-circuit voltage, hinting that dark-currents did not fall. Overall the photovoltaic performance of the structure with PQ is worse than without. This is not very surprising, because simulations of Section 5.2 already demonstrated that this type of heterojunction structure is pretty insensitive to surface recombination at the Si/organic interface. Unless the H-passivated surface is extremely poor (>5000 cm/s) passivation from PQ would not buy much in terms of reduced J_0. The bottom line is that passivation by PQ (10 nm thick) does not

improve the performance of Si/P3HT heterojunction, in fact it degrades it.

5.4.6 Minority Carrier Injection

For a n-Si/metal device in forward-bias, the dominant component of J_0 is electron current. However, the minority-carrier (hole) current, from the metal to the n-type silicon (the dotted curve in valence-band of Fig. 5.10(a)), also contributes a small part to the saturation current density [111].

While the Si/P3HT heterojunction does achieve impressive reduction in implied J_0 (10^{-10} A/cm^2) compared to the Si/metal Schottky junction (10^{-6} A/cm^2), the performance is still not comparable to the best p-n junction diodes (10^{-13} A/cm^2). To reduce J_0 even more, a better understanding of the dominant component of the dark-current is required. For example, if the dark-current is mostly composed of electrons going from silicon to metal via the LUMO of the organic, then an organic with a higher LUMO is required. If dark-current is limited by holes being injected from the anode metal into silicon, then this hole-injection needs to be reduced.

Which is the Dominant Current Component, Electrons or Holes?

First principle simulations were performed to separately plot the electron and hole currents in the heterojunction device of Fig. 5.2(a). The simulation assumed a conduction band offset of 0.5 eV at the Si/organic interface. The recombination lifetime of the silicon was set at 100 µs and the doping of the silicon wafer was 5×10^{14} cm^{-3}. Without the heterojunction (with Schottky barrier), the I-V characteristics show a dominant electron current and a smaller hole current (Fig. 5.14(a)). When the heterojunction is introduced, the hole current remains essentially unchanged but the electron current is reduced by several orders of magnitude (Fig. 5.14(b)). The reduction in electron current is so dramatic in the heterojunction device, that the hole-current becomes the limiting factor for further reduction in J_0. This is significant because it

tells us that further reduction in J_0 will not be achieved by making the Si/organic barrier larger (say by increasing it to 1.5 from the present 1.1 eV). Rather it must be achieved by reducing minority-carrier (hole) injection from anode into silicon.

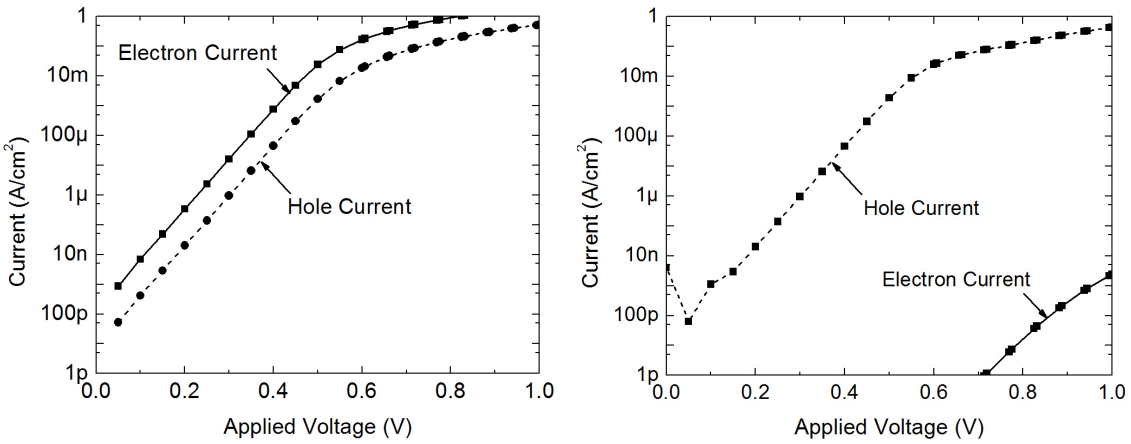


Figure 5.14: Simulated values of current in a (a) Si/metal and (b) Si/organic device, tp highlight the relative contribution of electron and hole currents to total dark-current. Electron current dominates the former and hole-currents dominate the latter. The conduction-band offset at Si/organic interface was set at 0.5 eV. The recombination lifetime of the silicon was set at 100 µs and the doping of the silicon wafer was 5×10^{14} cm^{-3}.

The analytically derived expression for current in heterojunctions (Eq.(2.14)) also support the idea that current in heterojunction diodes is hole limited. According to the derived expression (2.16), the $J_{0,electron}$ of a Si/organic heterojunction device is an exponential function of the electron barrier at the metal/organic interface

$$J_0 = \underbrace{J_{electron}}_{\text{Large}} + J_{hole} \Rightarrow J_0 \approx J_{electron}$$

Si/metal Junction

$$J_0 = \underbrace{J_{electron}}_{\text{Small}} + J_{hole} \Rightarrow J_0 \approx J_{hole}$$

Si/P3HT Heterojunction

Figure 5.15: Unlike Si/metal Schottky junctions, minority-carrier currents (hole current) may dominate J_0 in Si/P3HT heterojunction devices

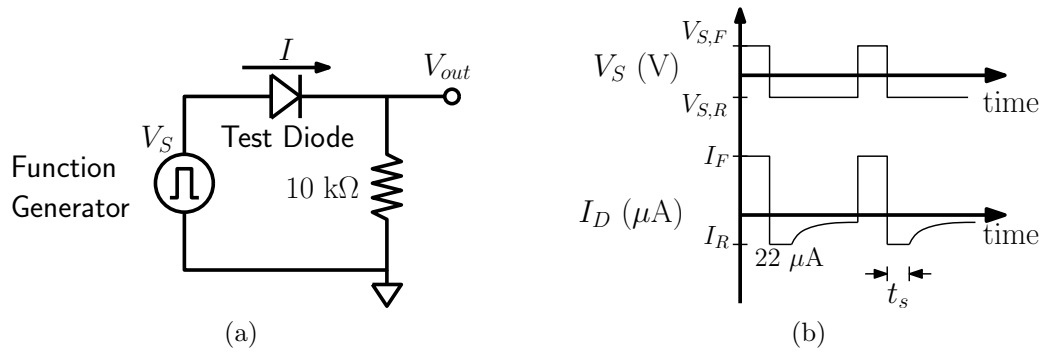


Figure 5.16: (a) The experimental set up to measurement storage times in heterojunction test diodes, in order to detect stored minority-carriers. (b) Applied and measured waveforms for the experiment.

(Section 2.5) and J_0 for Si/P3HT device were $\sim 10^{-33}$ A/cm^2, much lower than the expected hole current.

Direct evidence of minority-carrier dominance can be obtained by measuring the minority-carrier storage times and observing the effect of doping and recombination lifetime. In the next few sections, these measurements will be used to experimentally demonstrate that in Si/P3HT heterojunction devices the electron current has been lowered to a point where the hole current starts to dominate J_0.

Minority Carrier Storage Time

In a typical silicon p-n diode, the forward-bias current causes minority-carriers to get stored into the quasi-neutral regions. The presence of these stored minority-carriers can be probed by measuring the reverse-bias storage times [112, 113].

When a minority-carrier diode is suddenly switched from forward to reverse bias, the stored charges (and hence the voltage across the p-n junction) cannot switch instantaneously. Till the junction maintains its forward-bias, the junction remains in the 'On' state, and a simple voltage loop equation tells us that a negative current will flow in the circuit (Fig. 5.16(b)). Once the stored charges density has fallen enough to turn off the junction, the current reverts back to its equilibrium value (Fig. 5.16(b)).

The circuit used to measure this transient delay, also called 'storage' time (t_s),

along with the voltage waveforms is shown in the Fig. 5.16(a) and (b). The circuit consists of a pulse-waveform generator. The output of the generator (V_S) is such that it first forward-biases the diode at $V_{S,F}$ and then quickly switches it to reverse-bias voltage $V_{S,R}$. The transient current though the diodes I_F in forward-bias and I_R in reverse-bias) is estimated by a storage oscilloscope by measuring the voltage across a resistor connected in series with the diode. The value of the reverse current I_R can be quite high and is set by the value of the resistor R (in this case R=10 kΩ) - higher the value of R, lower the transient reverse-current (I_R). For a hole-current limited diode, t_s is given by the equation [112]:

$$erfc\sqrt{\frac{t_s}{\tau_r}} = \left(1 + \frac{I_R}{I_{F,hole}}\right)^{-1} \tag{5.12}$$

where τ_r is the hole recombination lifetime, $I_{F,hole}$ is the hole component of the total forward-bias current (I_F) and I_R is the total reverse-bias current (I_R) during the storage transient. Also

$$I_F = I_{F,electron} + I_{F,hole}$$

At fixed value of total forward-bias current (I_F), reverse-bias current (I_R) and recombination lifetime (τ_r), devices with higher hole-currents ($I_{F,hole}$) would yield longer storage times. For this experiment, all the diodes were fabricated on the same Si wafer, so the recombination lifetime can be assumed to be the same. The total reverse-bias current was fixed at 0.22 µA by keeping resistance (R) at 10 kΩand tuning the $V_{S,R}$, and storage times were measured at two different values of total forward-bias current - 100 µA and 1 mA.

In the diode without P3HT, the contribution of minority-carriers towards the total current is very small, so the measured storage time at 100 µA forward-current was very low (t_s <0.1 µs) (Fig 5.17(a)). For diodes with thick P3HT layers (>10 nm)

the storage times increased to $\sim$ 2.6 µs, indicating that hole current is a much larger fraction of total current. Similar results were also obtained at a forward-bias current of 1 mA for the same set of devices (Fig. 5.17(e)).

While the storage time results do not conclusively prove that hole-currents exceed electron-currents in heterojunction devices, they do demonstrate that compared to Si/metal Schottky devices, minority-carrier (hole) currents are a bigger component of total current in Si/P3HT heterojunction devices.

Effect of Doping and Recombination Lifetime

If a n-Si/P3HT heterojunction device is hole-current dominated, reducing hole injection from anode to silicon will lower the J_0 of the device. It is well-known that hole current in to n-type silicon due to minority-carrier injection (J_{hole}), in both Schottky and p-n junction barriers, is given by the relation [114]

$$J_{hole}(V) = q\frac{n_i^2}{N_{Si}}\sqrt{\frac{D_{hole}}{\tau_r}}\left(e^{qV/kT}-1\right) \tag{5.13}$$

where, q is the electronic charge, n_i is the intrinsic carrier density in silicon, D_{hole} is the hole diffusion coefficient, and V is the applied voltage. We assume that the diode is in the long-base regime, i.e. $L_{hole} <<$ Si wafer thickness. By increasing the n-type doping level (N_{Si}), and/or increasing the minority-carrier lifetime in the silicon (τ_r), the hole-injection current can be reduced.

Simulation show the beneficial effect of increased doping. A structure similar to the one shown in Fig. 5.2(a), but with a higher doping (N_D=10^{16} cm^{-3}), was simulated in dark and under $\sim$1.1 sun illumination. Compared to the lower doped (N_D=5×10^{14} cm^{-3}) Si/organic devices, higher-doped devices have a lower J_0 and higher V_{OC}.

Typically, silicon wafers grown by the Czochralski (CZ) process have lower minority-carrier recombination lifetime than those grown by Float-Zone (FZ) method : <1 ms

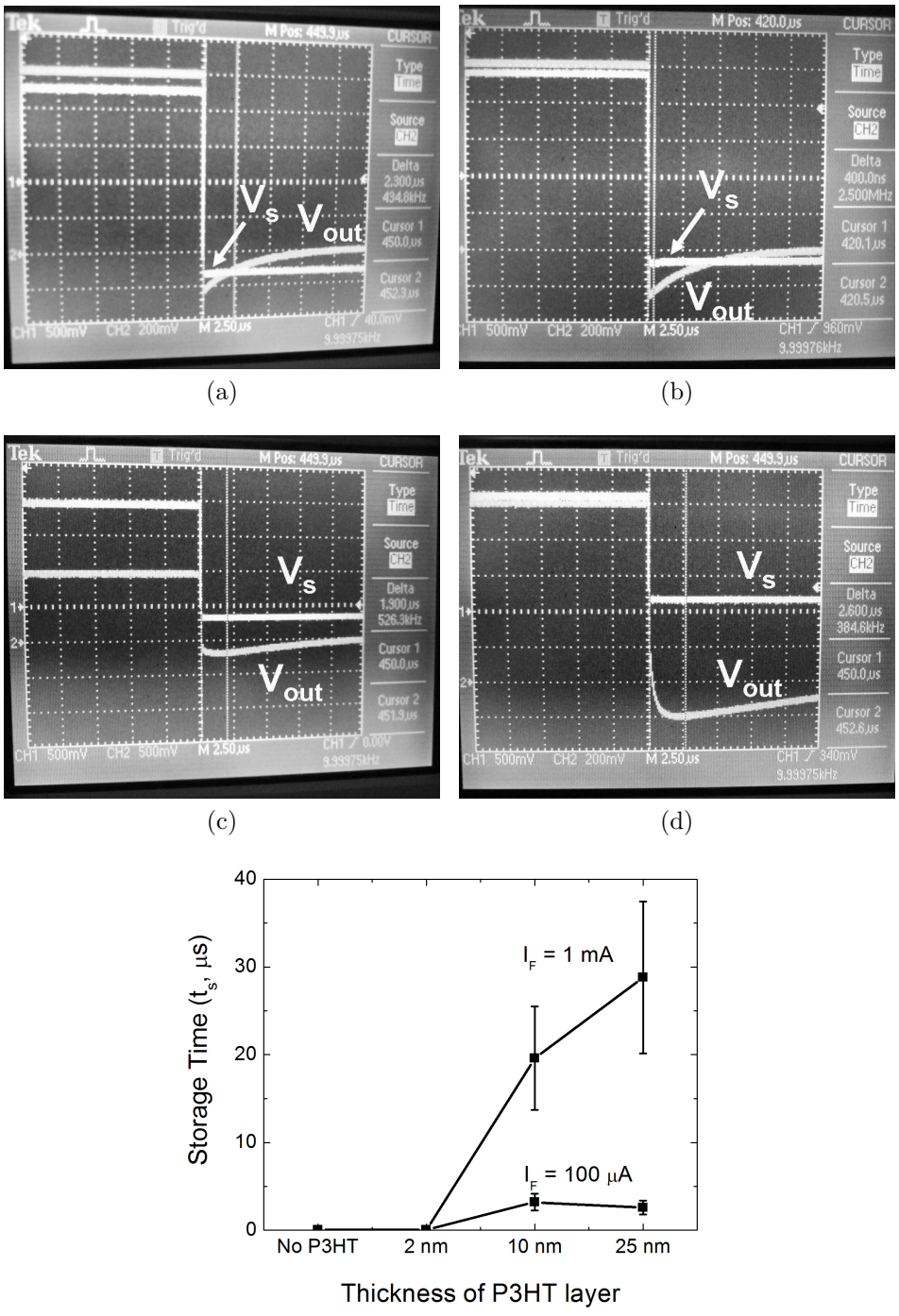


Figure 5.17: Output waveforms measured at the oscilloscope for test devices with (a) no P3HT, (b) 2 nm P3HT layer, (c) 5 nm P3HT layer, and (d) 25 nm P3HT layer. Devices were forward-biased at 100 µA current. (e) Measured storage time (t_s) at forward-bias current of 100 µA and 1 mA.

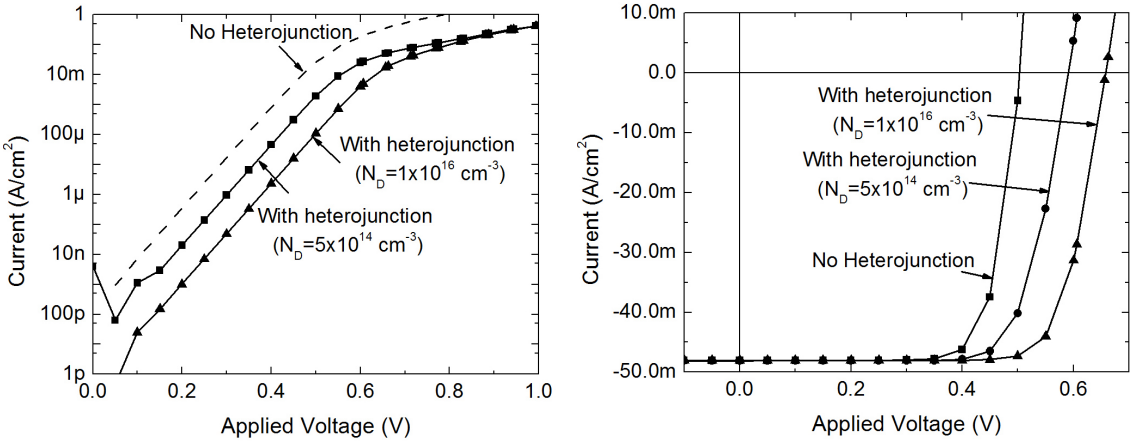


Figure 5.18: IV characteristics of Si/organic device with different Si substrate doping (a) in Dark and (a) under ≈1.1 sun illumination.

Table 5.4: The extracted device parameters for Si/P3HT device made on higher-doped FZ wafers. Implied J_0 calculated from Eq. (1.4), using measured V_{OC}, n and J_{SC}.

Device (nm)	Device Parameters				
	Extracted J_0 (A/cm^2)	n	J_{SC} (mA/cm^2)	V_{OC} (V)	Implied J_0 (V)
No P3HT (5×10^{14} cm^{-3}, CZ)	9.2×10^{-7}	1.01	2.1	0.20	9.0×10^{-7}
25 nm (5×10^{14} cm^{-3}, CZ)	1.6×10^{-8}	1.14	1.6	0.41	2.0×10^{-10}
25 nm (7×10^{15} cm^{-3}, FZ)	2.9×10^{-9}	1.25	1.6	0.44	6.3×10^{-11}

for CZ compared [26] to ∼ 10 ms for FZ [27]. The wafers used in the experiments of Fig. 5.12a and 5.12b were grown by CZ process. To experimentally observe the effect of lowering hole-injection on J_0 of Si/P3HT heterojunction devices, wafers grown by the FZ process were used instead of CZ to make devices with the structure shown in Fig. 5.10(c). The doping of the FZ wafers was also higher: 7×10^{15} cm^{-3} instead of 4×10^{14} cm^{-3} for CZ wafers used in earlier experiments. The P3HT layer was 25 nm thick.

Compared to heterojunction devices on lower-doped CZ Si, Si/P3HT devices fabricated on higher-doped FZ substrates show an marked decrease in J_0 - from 1.6×10^{-8}

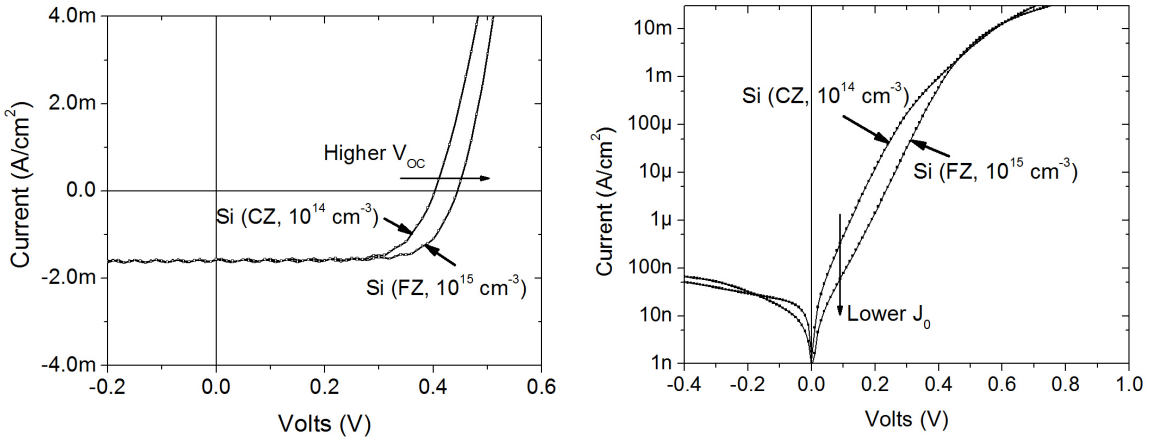


Figure 5.19: The I-V characteristics of Si/P3HT devices fabricated on 4×10^{14} cm^{-3} doped CZ Si and 7×10^{15} cm^{-3} doped FZ Si. (a) In dark. (a) Under $\approx$ 0.1 sun illumination.

to 2.9×10^{-9} (Fig 5.19(a) and Table. 5.4). The open-circuit voltage under 0.1 sun illumination also showed a corresponding increase; from 0.41 to 0.45 V (Fig 5.19(b)). Ideality factors are once again high, which makes it hard to compare the performance between devices. To make a fair comparison between the photovoltaic performance of the devices, the "implied J_0" is calculated. In terms of "implied J_0", the currents in the FZ device are three times lower than the CZ device (Table 5.4).

These results conclusively prove that dark-currents in Si/P3HT devices are dominated by minority-carrier injection from the anode into silicon, and not electron injection from silicon into the anode. Furthermore, we have demonstrate devices with an "implied J_0" of only 63 pA/cm^2, while keeping processing temperatures below 150 ℃.

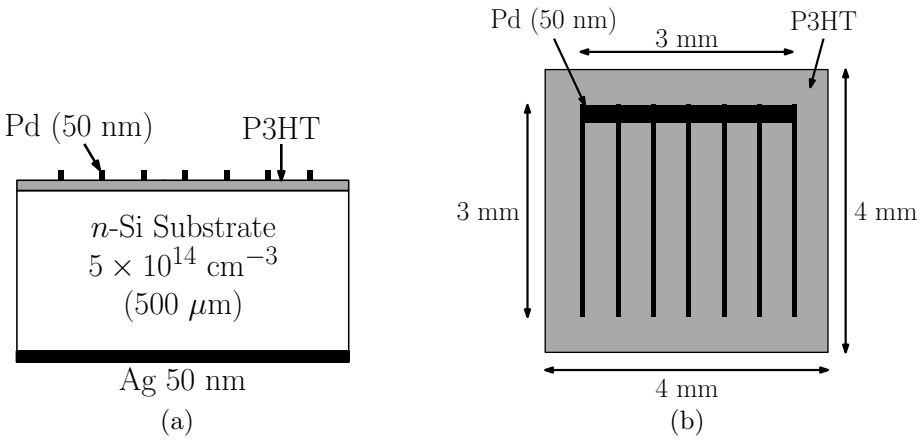


Figure 5.20: Device structure of Si/P3HT heterojunction solar cells where the semi-transparent blanket metal is replaced with a 20% metal grid for the top electrode. (a) Side View and (b) top view.

5.4.7 Si/P3HT Heterojunction Solar Cell

Top metal grid

All the Si/P3HT heterojunction devices fabricated until now had a semi-transparent Pd-layer as the top electrode, which absorbs roughly 50% of the incoming light. In an actual solar cell, such high tranmission losses would be unaccpetable and an anode structure with less light absorption is required.

The easiest alternative is to replace the blanket Pd-layer with a metal-grid with fingers. Depending on the density of metal fingers, ∼5 to 40% of the surface area in our experiment is covered by metal and does not transmit light. The fabrication procedure for making such devices was similar as before, except for anode metal pattering. Instead of using a shadow mask with 1 mm radius holes, a shadow mask with 100 µm wide fingers was used (Fig. (b)). The separation between fingers was varied to get patterns with approximately 5, 10, 20 and 40 % shadowing. The active area of the solar cell is not very well-defined, because the extent of lateral conduction is unknown. In the results presented here, the area was assumed to be 4 mm x 4 mm.

Current-voltage characteristics of the metal-grid devices were measured under a microscope light calibrated with an approximate intensity of 0.1 and 1 sun (Fig. 5.21).

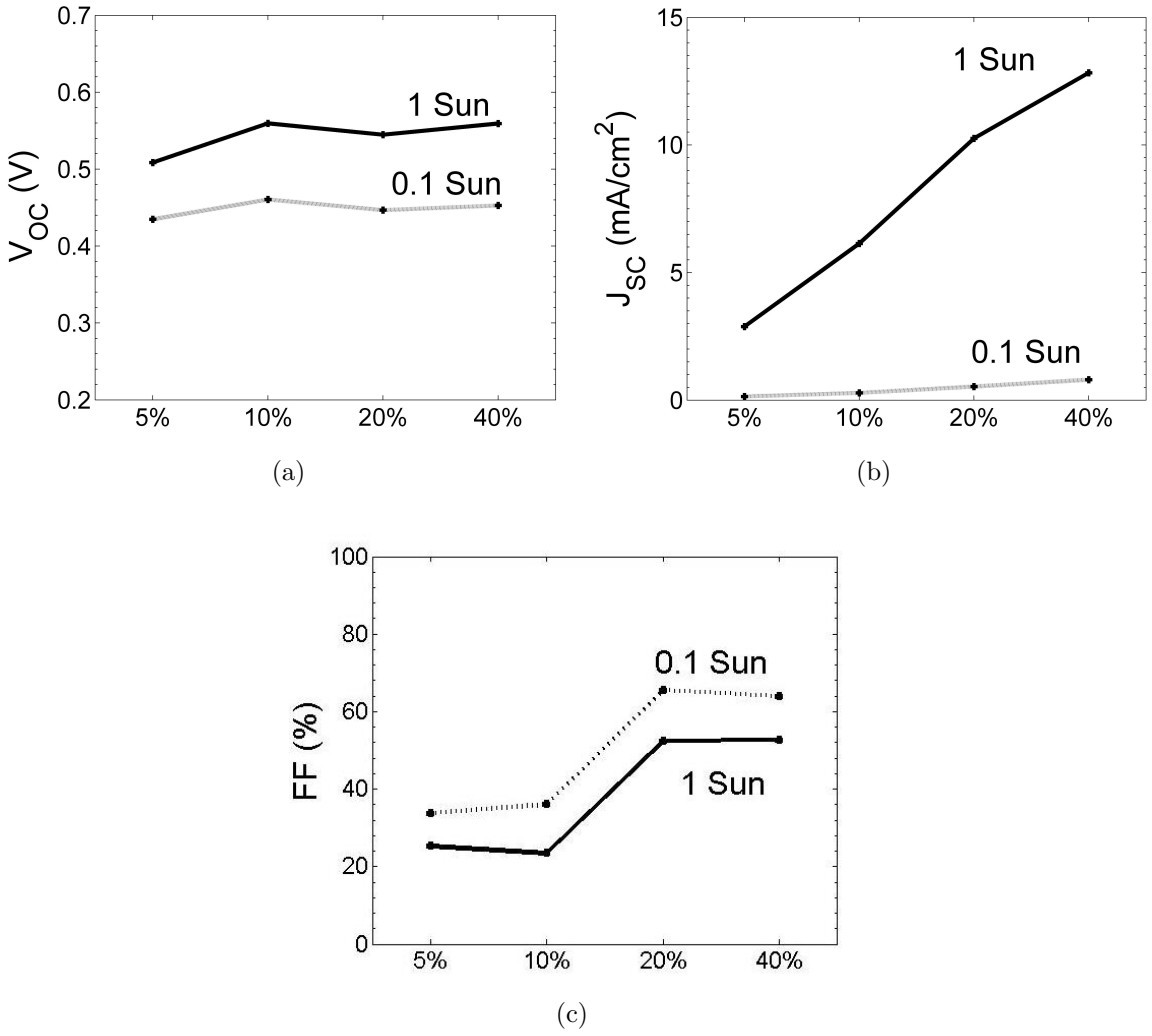


Figure 5.21: Photovoltaic response of Si/P3HT heterojunction solar cells, at approximately 0.1 and 1 sun illumination, with different area density ratio of the top metal grid. (a) Open-circuit voltage (a) Short-circuit current (a) Fill factor

As before an open-circuit voltage of ~ 0.4 V was obtained for all devices (Fig. 5.21(a)). One expects that higher shadowing losses in a more dense metal-grid would lead to *lower* J_{SC}, but interestingly, the values of J_{SC} show a monotonic *increase* with increasing metal-grid density (Fig. 5.21(b)).

The issue lies with poor lateral conductivity of the P3HT layer, which forces the photogenerated holes in silicon to diffuse laterally in silicon, to a location with a metal finger, instead of going vertically towards the anode. The longer the distance

the carriers need to diffuse in silicon, the higher the chance they will be lost to recombination. By reducing the spacing between metal fingers, i.e. increasing the grid density, the lateral diffusion in silicon is reduced and consequently J_{SC} increases.

The data for fill factor also confirm the presence of lateral resistance effects in these devices. Since the resistance is limited by lateral conduction, smaller spacing between metal fingers reduces total series resistance and increases fill factors (Fig. 5.21(c)).

Thicker P3HT layers might be used to ameliorate the problem of lateral resistance to some extent, but the improvement would come at the expense of increased transmission losses (lights transmits through a thicker P3HT layer) and a higher vertical resistance (carrier need to travel longer in the vertical direction). A more robust solution is to integrate a transparent conductor on top P3HT-coated silicon wafers.

Transparent conductor - PEDOT:PSS

The transparent conductive semiconductor used in this study is the organic Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) which was bought from Sigma Aldrich (High-conductivity grade, 2.2-2.6% in water). Chemically PEDOT:PSS is a water-based dispersion of a wide energy-gap organic semiconductor, PEDOT, doped with the acid PSS. The fact that PEDOT is a doped-semiconductor is not important, the reason it is used in this work is because it is transparent. PEDOT:PSS dispersion is a bluish-colored ink that can be spin-casted to form thin tranparent films that absorbs <5% of the solar light. The advantages PEDOT has over conventaional tranparent conductors, like ITO and ZnO, are a) PEDOT does not need to be sputtered, a process that can mechanically damage the delicate organic layers underneath, instead PEDOT layers are spin-coated. b) PEDOT has a higher work function of $\sim$ 5.1 eV than $\sim$4.5 eV of ITO, which should result in a higher built-in field in silicon and consequently a higher V_{OC} should be obtained.

To measure the vertical resistivity of PEDOT:PSS layer, a special test structure

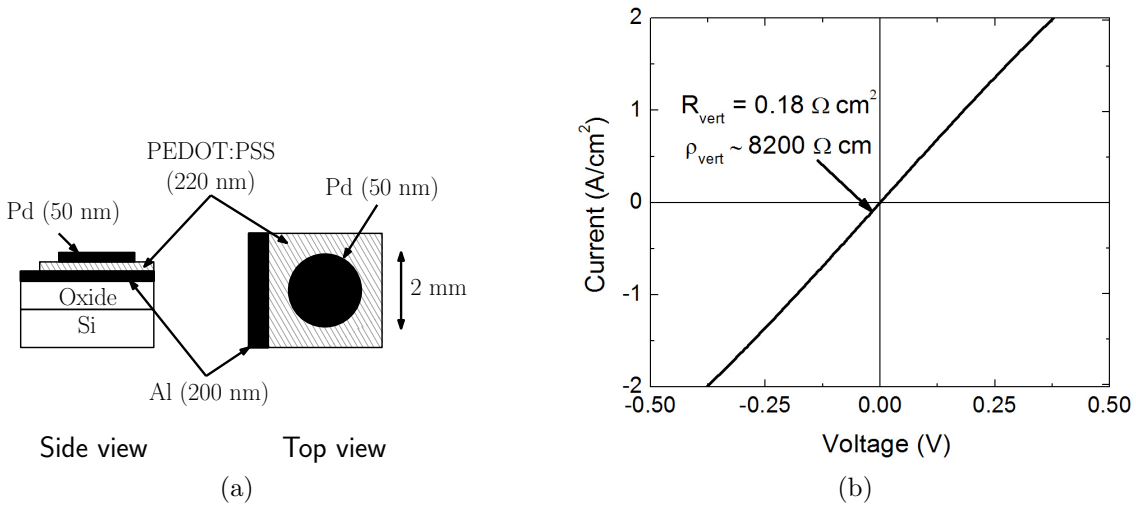


Figure 5.22: (a) Structure and (b) IV characteristics of the device used to measure vertical resistivity of PEDOT.

was fabricated (Fig. 5.22(a)) in which PEDOT was sandwiched between two layers of metal. The bottom metal (200 nm Al) and top metal (50 nm Pd) were deposited by thermal evaporation, while PEDOT was spin-coated before the top metal deposition. If the lateral current-spreading is ignored then the top-metal electrode defines the device area. The top electrode was pattered by a shadow mask with holes (1-mm radius). The I-V characteristics were linear with voltage, as they should be for a resistor-like structure. Ignoring the contact resistance, the vertical resistivity of the PEDOT layer can be simply extracted from the measured resistance, given the thickness of the PEDOT layer (t=220 nm) and top-metal electrode area ($A = 3.14\times10^{-2}$ cm^2):

$$\rho_{vert} = \frac{V}{I}\frac{A}{t} \tag{5.14}$$
$$= 8200\ \Omega cm$$

For lateral resistance of PEDOT, a different test-structure was used. There was no back-electrode. Instead PEDOT was spin-coated on an oxide covered silicon wafer. The top electrode was then deposited through a shadow mask. In the fi-

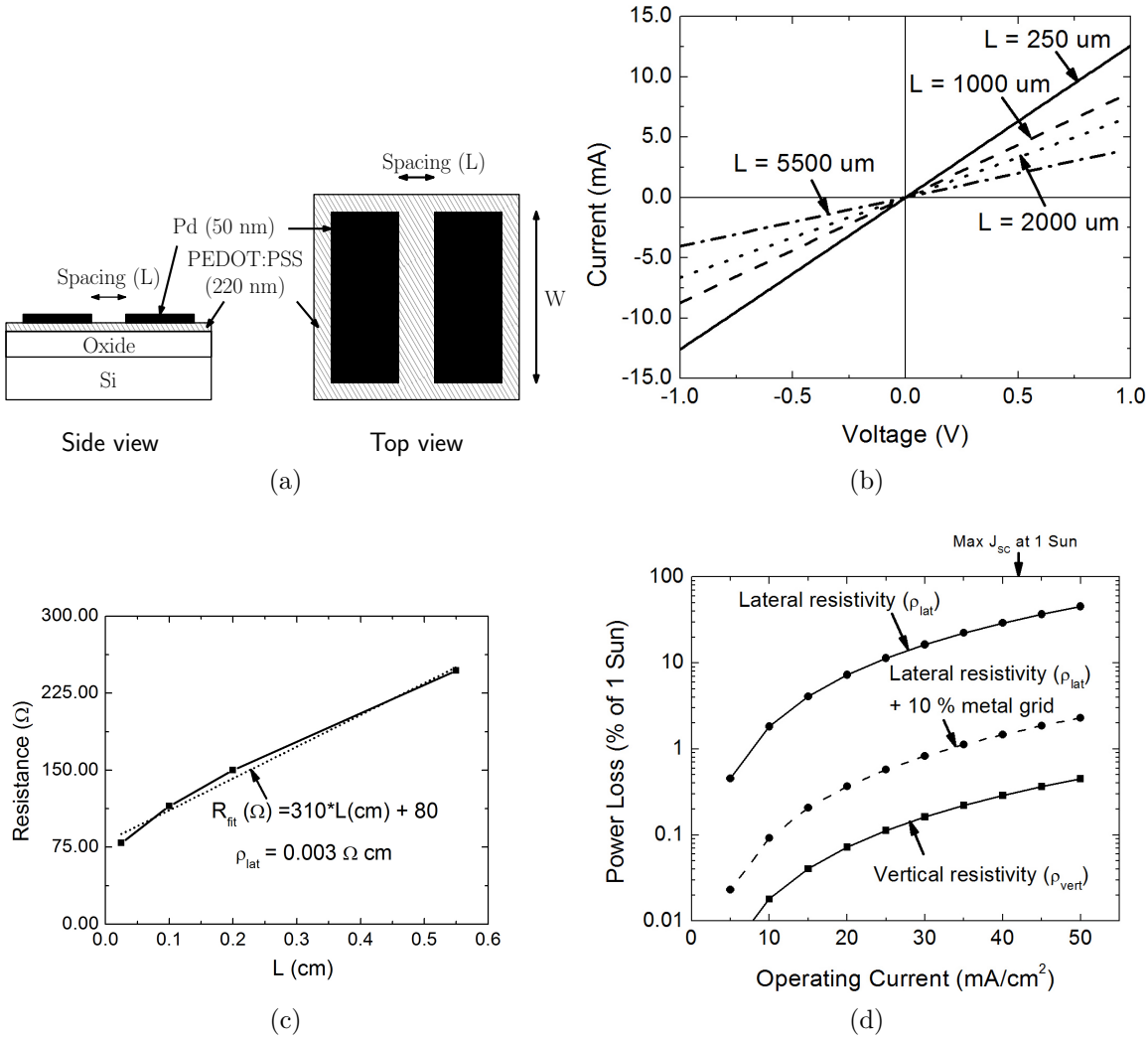


Figure 5.23: Structure and (b) I-V characteristics of the device used to measured lateral resistivity of PEDOT. (c) Extracted lateral resistance for different spacing (L). $W = 0.5$ cm. (d) Calculated power lost due to lateral and vertical resistivity of PEDOT as a function of operating current level. An additional metal grid (with 10 % shadowing) reduces the lateral loss to $\sim 1\%$ at a current density of 35 mA/cm^2.

nal structure metal pads were placed at various spacings(L) - from 250 µm to 5500 µm (Fig. 5.23(a)). The measured I-V characteristics between any two adjacent pads were linear (Fig. (b)), and the extracted resistance (R_{lat}) increased monotonically with spacing L (Fig. (c)). The linear fit of the dependence of R_{lat} on L has an intercept on the y-axis, which is a measure of the contact resistance of the test fixture and is not a PEDOT property. On the other hand, the slope of the linear fit directly

relates to the lateral resistivity of PEDOT (ρ_{lat}). Given pad width (W=5 mm) and PEDOT thickness (t = 220nm)

$$\begin{aligned} \rho_{lat} &= slopeWt \\ &= 0.003 \quad \Omega cm \end{aligned} \tag{5.15}$$

It is worth noting that the resistivity is the two orthogonal directions is different by 6 order of magnitude ($\rho_{vert}/\rho_{lat} \sim 10^6$). Anisotropy in conductivity has been previously reported in PEDOT:PSS films [115], though the difference in conductivity was only three orders of magnitude ($\rho_{vert}/\rho_{lat} \sim 10^3$) and not six. The reason for the large anisotropy was traced to the morphology of the PEDOT layer, where PEDOT and PSS domains were formed in a manner that charge hopping in one lateral direction was much easier than vertical direction [115]. In-depth morphological study of the PEDOT:PSS layers used in this study have not yet been conducted.

Due to vertical and lateral resistivity, PEDOT will suffer ohmic losses. To estimate the severity of the losses in the solar cell due to the PEDOT layer, ohmic losses were calculated for different values of current density. We are particularly interested in the losses at 1 sun illumination, or at a current density of 40 mA/cm^2.

Assume a the device is operating at a current density of J_{op} (in mA/cm^2). The ohmic losses due to vertical resistance, $P_{loss,vert}$ (in W/cm^2), is given by

$$P_{loss,vert} = J_{op}^2 \rho_{vert} t \tag{5.16}$$

where t is the PEDOT thickness.

The calculation for power loss due to lateral resistance is more complicated because the current flowing in the lateral direction is not constant at all points (Fig. 5.24). Assume there is a thin highly conductive metal finger across the length of the device, and all current needs to be collected along its edges. Ohmic losses for current gen-

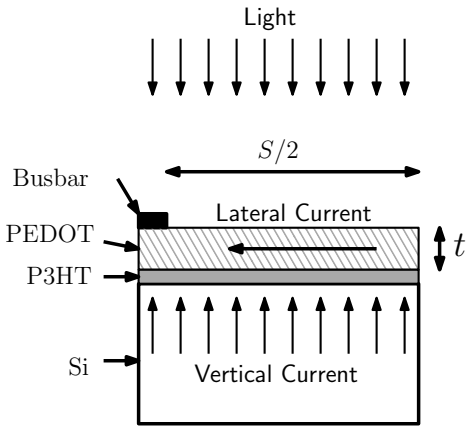


Figure 5.24: Power losses due to lateral resistance of PEDOT layer. Current in the lateral direction is not uniform so loss calculations is not simple.

erated close to the busbar are minimal but the current generated far from the metal finger needs to travel a long resistive path to the finger, so its lateral ohmic losses are higher. The power losses ($P_{loss,lat}$, in in W/cm^2) in such a scenario can be estimated by [116]

$$P_{loss,lat} = J_{op}^2 \rho_{lat} \frac{S^2}{12t} \tag{5.17}$$

where S is the average distance between two fingers and t is the PEDOT thickness. For a 4 mm$\times$ 4 mm device with one metal finger in the middle of the device S is 4 mm.

Using the above equation, the ohmic losses due to the vertical and lateral resistance at different current density can be calculated (Fig. 5.23(d)). At AM1.5 the total optical power incident on a device is 100 mW/cm^2. The fraction of the total optical power lost due to finite vertical resistivity is

$$P_{loss,vert}(\%\ of\ 1\ Sun) = \frac{P_{loss,vert}}{100\ mWcm^2} \times 100$$

Similarly, the fraction of total power lost to lateral resistivity is

$$P_{loss,lat}(\%\ of\ 1\ Sun) = \frac{P_{loss,lat}}{100\ mWcm^2} \times 100$$

In Fig. 5.23(d), these normalized power-loss values are plotted as a function of operating current level (J_{op}). While the losses due to vertical resistivity are minimal - <1% of total incoming power at 1 sun illumination - the losses due to lateral resistivity are significant - $\sim$ 10 %. The simplest way to reduce the lateral resistance is to add more fingers connected by a busbar, i.e. add a metal grid on top of PEDOT layer. This reduces the average S, which decreases lateral ohmic losses, a per Eq.(5.17). For a 10 % metal-grid with 100 µm wide fingers, the average finger spacing is 900 µm. With the metal grid, the calculated ohmic losses due to the lateral PEDOT resitivity are only 1% of total power (Fig. 5.23(d)). Of course, the decreased resistance comes at the expense of a lower J_{SC} due to increased light reflection losses at the top surface. Algorithms to precisely optimize the trade-off between J_{SC} and fill factor have been published elsewhere [37, 117]. In devices fabricated in this study a 5-10 % metal grid was added on top of the PEDOT:PSS layer.

Heterojunction Solar Cell with PEDOT:PSS

Next, Si/P3HT heterojunction solar cells with a PEDOT and metal grid as the transparent anode stack were fabricated. The fabrication procedure was same as before - P3HT was spin-coated on clean and hydrogen-passivated silicon - except for two additions:

(a) PEDOT layers were spin-coated at 2000-6000 rpm (for 120 s) on top of P3HT-coated wafers to form the PEDOT-P3HT-Si structure of Fig. 5.25(a).

(b) In heterojunction solar cells of Fig. 5.20b, the high lateral resistance of P3HT automatically isolated two adjoining devices on a silicon wafer. However, due to lower lateral resistance of the PEDOT later, a more robust method is needed to isolate adjoint devices. In this study, devices were isolated by scratching away the organic layers (Both PEDOT and P3HT) using a thin probe. On a 16 mm $\times$ 16 mm Si piece, 3 vertical and 3 horizontal scratches were made,

each 4 mm apart, to give sixteen 4 mm × 4 mm sized devices. The scratching method does lead to some inaccuracies in calculating device area, e.g. carriers collected within a diffusion length of the device edge may also contribute to the photocurrent, artificially increasing the short-circuit current. However, the uncertainty due to these effects is small (∼ 100 µm for CZ wafers) compared to the size of the device (4 mm), so it is ignored in the calculations.

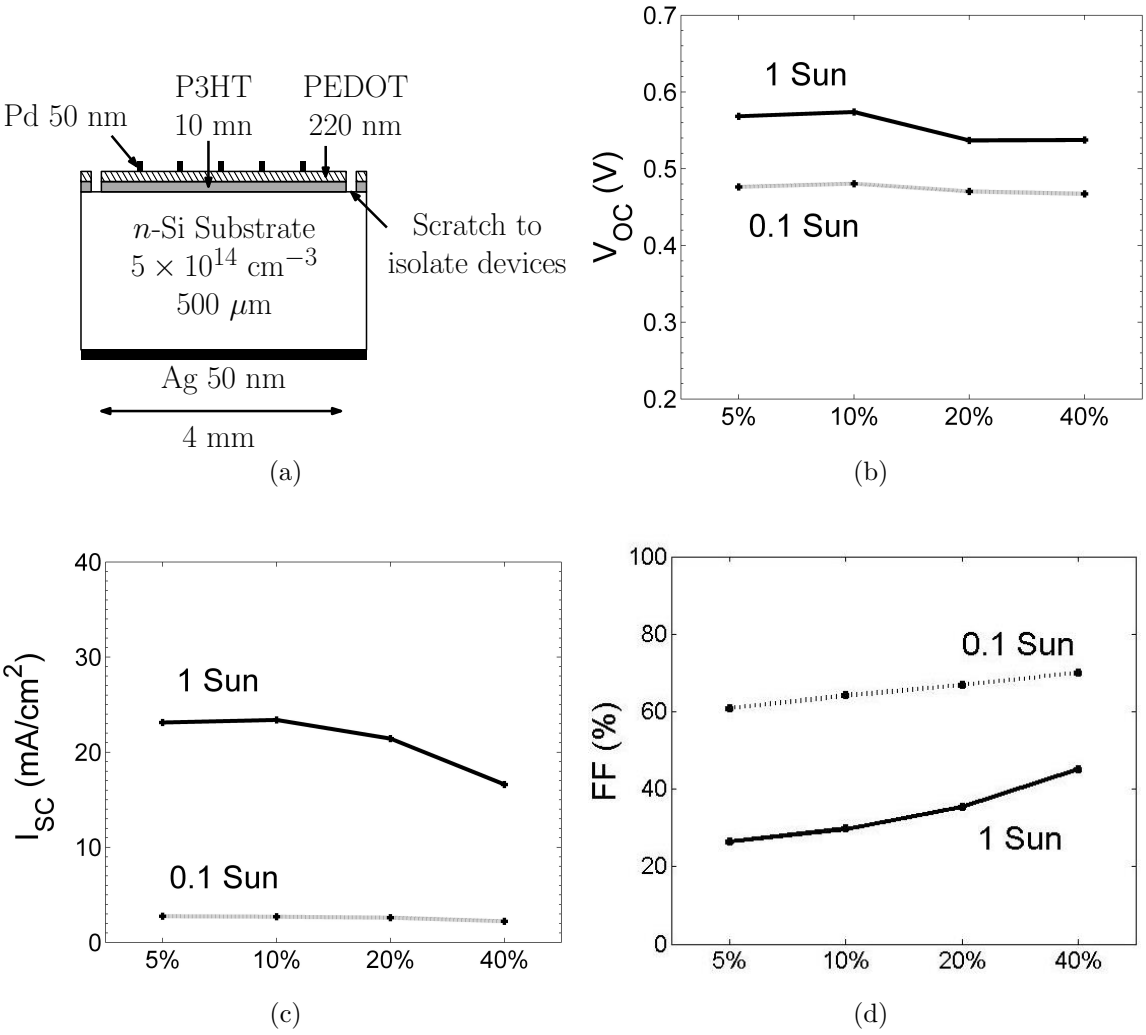


Figure 5.25: Photovoltaic response of Si/P3HT heterojunction solar cells with PEDOT:PSS, at approximately 0.1 and 1 sun illumination, with different density of top metal grid - 5%, 10%, 20 %, and 40%. (b) Open-circuit voltage (c) Short-circuit current (d) Fill factor

The photoresponse of heterojunction devices with PEDOT and different top metal grids is shown in Fig. 5.25. The open-circuit voltages of these devices were around 0.57 V under a microscope light roughly with an intensity of approximately 1 sun. Due to better carrier collection at the anode and reduced lateral resistance, the devices show substantially higher J_{SC} (Fig. 5.25(c)) than what was measured on devices with just the metal grid (Fig. 5.21(b)). Also, unlike the device with just metal grid, the J_{SC} for device with PEDOT decreases with increasing metal grid shadowing, demonstrating that carrier collection is not a problem anymore. The improved lateral resistance also helped increase the fill factors at lower illuminations (where the current density is <5 mA/cm^2) - from Fig. 5.21(c) to Fig. 5.25(d) verses). However, at higher illumination the current density was high and higher resistance losses caused deterioration in the fill factors - from 60% to only 25% only. Fill-factors still increase by decreasing the distance between metal fingers, suggesting that lateral resistance is still an issue.

Loss Mechanisms

The low fill factors are a result of ohmic losses in the heterojunction device, and to demonstrate high-efficiency devices, series resistance needs to be decreased. Ohmic losses in the PEDOT layer were estimated in previous section, and they are expected to be lower (Fig. 5.23(d) than what is experimentally measured in the devices, so other sources of resistance need to be analyzed.

Organic layers are known source of series resistance. Doping does decrease the resistivity of the organic layers [118], however these methods are neither easy nor well-understood.

Resistivity of the Si wafers used in the devices above was $\sim$ 10 Ωcm. So Si is expected to add around 30 Ω of series resistance to a 4 mm $\times$ 4 mm sized device. By switching to a 0.8 Ωcm doped wafer, the resistance due to Si can be reduced to only $\sim$ 2 Ω. The added benefit of higher-doped wafers is reduced hole injection and

increased V_{OC}.

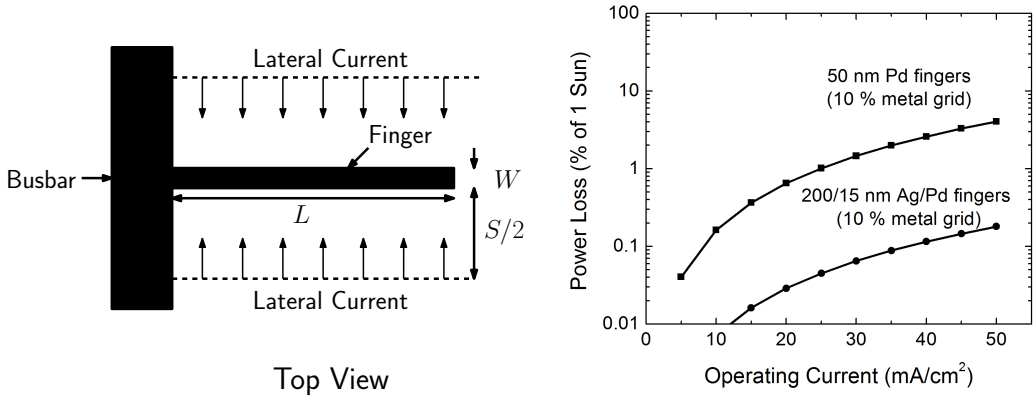


Figure 5.26: (a) Schematic of a metal finger attached to a busbar. The current is collected laterally and transported to the busbar. (b) Calculated ohmic power losses as a function of operating current level, due to resistivity of metal fingers. Compared to the original '50nm Pd' fingers losses in the improved 'Ag/Pd' fingers are lower.

Another sources of series resistance is the metal grid. Typical resistivity of palladium is $\sim 10^{-5}$ Ωcm. One 50 nm thick finger of the metal grid made out of Pd (3 mm long × 100 µm wide) contributes 30 Ωs to series resistance. To reduce the resistance of metal fingers, the Pd layer (50 nm) can be replaced by Ag, whose resistivity is ten times lower ($\sim 10^{-6}$ ohm cm) than Pd. However, the work-function of Ag is only 4.5 eV, while that of Pd 5.0 eV. To maintain the high work-function of the anode, and consequently the built-in field in silicon, the Pd finger is not replaced with Ag, but replaced by a 15nm/200nm thick Pd/Ag stack. Compared to a simple Pd finger (30 Ω), the resistance of a single metal finger made with Pd/Ag is <1 ohm. Calculations of the ohmic losses due to resistive metal fingers is slightly complicated, once again due to non-uniform lateral current.

Assume that the metal-grid consists of metal fingers that are uniformly spaced a distance S apart and run along the length of the device (L). All fingers are connected in parallel to a busbar of zero resistance (Fig. (a)). Each metal finger is L long, w wide, and d thick made of metal with resistivity ρ_m. The current is collected in the

lateral direction from a area $\pm S/2$ around the metal finger. The ohmic losses ($P_{loss,m}$, in W/cm^2) depend how far the current is from the busbar. If the operating current density is J_{op} the ohmic power loss is given by[119]

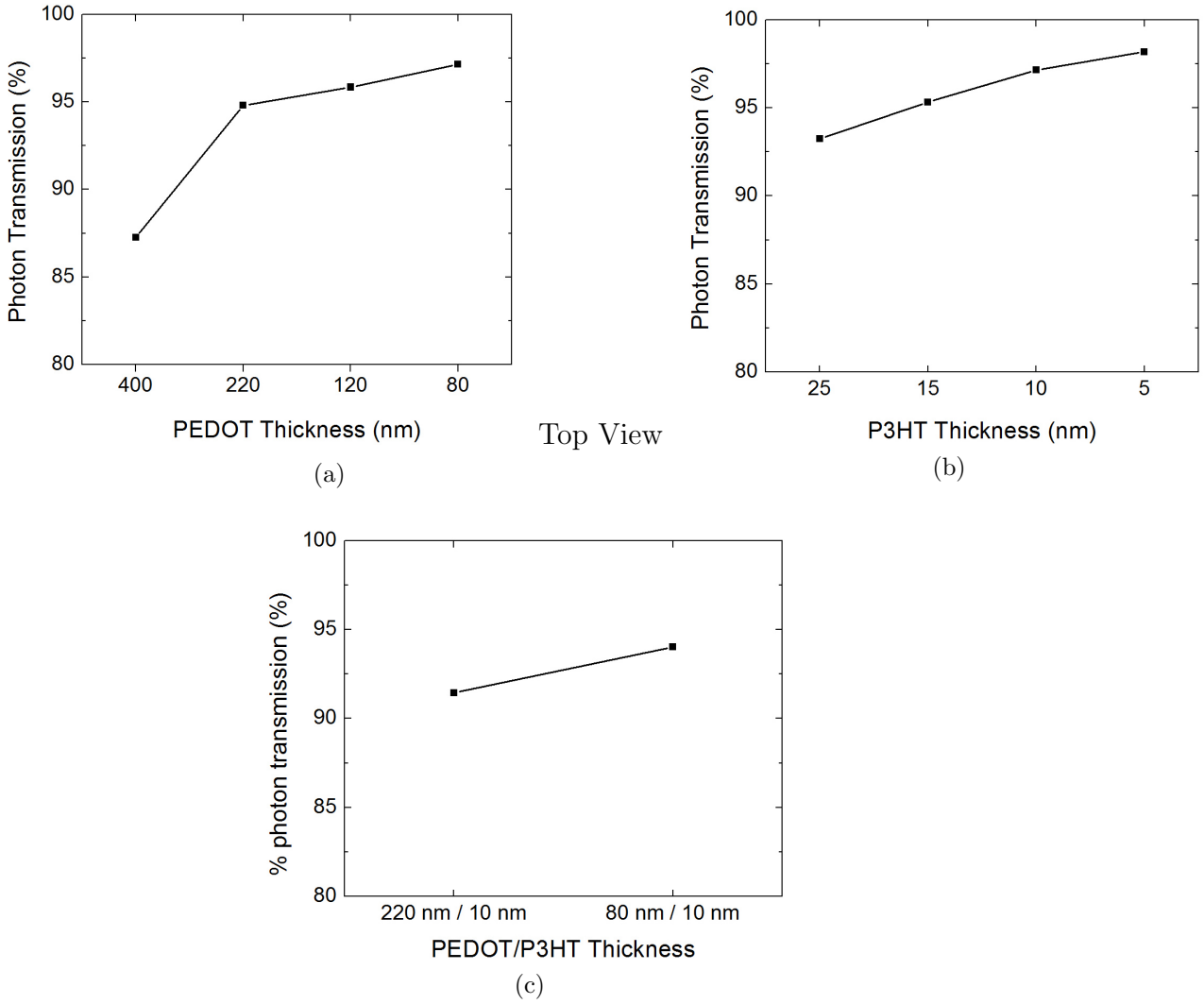
$$P_{loss,m} = J_{op}^2 \rho_{lat} \frac{SL^2}{3wd} \tag{5.18}$$

The calculated power loss values due to the Pd and Pd/Ag metal fingers are shown in Fig. (b). The use of lower resistivity metal along with thicker finger ($d = 200nm$), substantially reduces ohmic losses in the device.

Another area of potential improvement is the short-circuit current. Conventional Si solar cells have a J_{SC} of around 40 mA/cm^2 at AM1.5, while the heterojunction device above yielded a J_{SC} of only 23 mA/cm^2. One obvious source of loss if the metal grid which reflects 10% of the light. Parasitic absorption of photon in the organic layers could also reduce the photon flux seen by silicon. To check for this possibility, transmission measurements were performed using a standard Si photodiode.

Organic layers of differing thicknesses were deposited on glass slides. Next the photodiode was covered by these glass sides and the photoresponse was measured by a ammeter under 1 sun illumination. Assuming the internal quantum efficiency of the silicon diode is unity, the fraction of photons being absorbed in the organic layers were calculated (Fig. 5.27). The results show that losses in a device with a 10 nm P3HT layer and 80 nm PEDOT layer, the organic layers account for only $\sim$ 7% of loss in J_{SC} (approximately 3 mA/cm^2).

The present generation heterojunction cells do not have light trapping structures, such as an anti-reflection coating [120, 121, 122] or surface texturing [123], so photon losses due to reflection off the silicon surface are expected to be high. The refractive index of silicon is around 3.4. If the pristine silicon surface is exposed to air (the worst case), the amount of normally incident light lost due to reflections off the top



(a) (b) (c)

Figure 5.27: Transmission losses, as measured by a photodiode under 1 sun illumination, for (a) PEDOT, (b) P3HT, and (c) combined PEDOT/P3HT stack.

surface, characterized by the reflectance (R), can be as high as 30%

$$R = \left(\frac{3.4-1}{3.4+1}\right)^2 \approx 30\%$$

The refractive index of PEDOT is ∼1.33-1.55 [124]. Thus there is enough contrast in the refractive indexes of Si and PEDOT, that PEDOT can function as a single layer anti-reflection coating on silicon. In the next sub-section, the PEDOT thickness was set at 80 nm, a thickness where it can serve as a quarter-wavelength anti-reflection

Table 5.5: The extracted device parameters for Si/P3HT heterojunction solar cell (Fig. 5.28(a)) under AM1.5. Implied J_0 calculated from Eq. (1.4), using measured V_{OC}, and J_{SC}.

Device	Device Parameters				
(nm)	Extracted J_0 (A/cm^2)	n	J_{SC} (mA/cm^2)	V_{OC} (V)	Implied J_0 (A/cm^2)
No P3HT, No PEDOT Cell	9×10^{-7}	1.01	1.5	0.21	4.4×10^{-7}
Si/P3HT heterojunction	9×10^{-9}	1.37	29	0.59	3.4×10^{-12}

coating for 500 nm light.

Optimized Heterojunction Solar cell

Improved heterojunction solar cells were fabricated (Fig. 5.28(a)) by incorporating all the proposed optimizations discussed above i.e.

- Increased Si substrate doping from 5×10^{14} cm^{-3} to 10^{16} cm^{-3}, leading to reduced ohmic losses in Si and increased V_{OC}. Both substrates were CZ grade.
- Thicker Ag/Pd metal grid rather than just Pd.
- A PEDOT layer (80 nm), designed to function as a crude anti-reflection coating.

In the dark, the current-voltage characteristics of silicon/organic heterojunction (SOH) device clearly shows a diode-like behavior (Fig. 5.28(b)). For comparison a Si/metal Schottky-barrier device without the organic layer and just the metal grid was also measured. The SOH device has a much lower extracted J_0 ($\sim9\times10^{-9}$ A/cm^2) than the Si/metal device ($\sim9\times10^{-7}$ A/cm^2). The ideality factor of heterojunction device is 1.37, while that of Si/metal device is 1.

Under AM 1.5 illumination, the reduced J_0, leads to an increased open-circuit voltage (Fig. 5.28(c)). The hybrid heterojunction device has an open-circuit voltage of 0.59 V. At this early stage of demonstration, this compares very well with highly engineered silicon solar cells with diffused p-n junctions, which typically exhibit open-

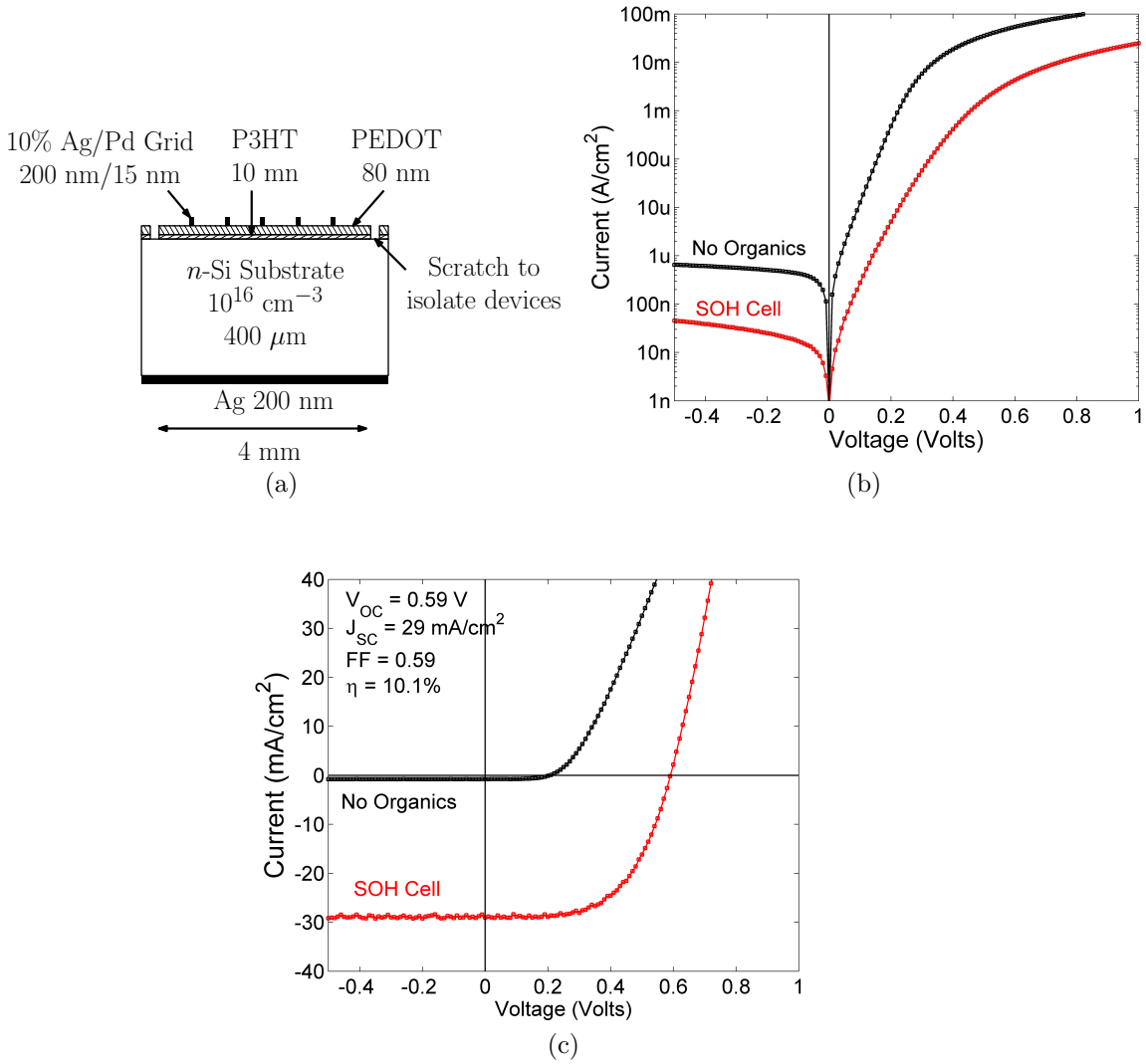


Figure 5.28: (a) The structure of the optimized Si/P3HT heterojunction solar cell. (b) I-V characteristics of the heterojunction solar cell in dark. (c) I-V characteristics of the heterojunction solar cell under AM 1.5 illumination.

circuit voltage of 0.6 - 0.7 V. The measured short-circuit current density is 29 mA/cm^2, which is only about 30% lower than the theoretical maximum of 42 mA/cm^2. Based on the measured valued of V_{OC} and J_{SC}, the "implied J_0" of the heterojunction is only 3.4 pA/cm^2, an improvemt of over five orders of magnitude over the Schottky device (with metal grid but no PEDOT or P3HT) (Table 5.5).

The PEDOT:PSS/P3HT stack and top metal account for around 7% and 10% reduction in the short-circuit current. The rest of the loss in short-circuit current (∼

13%) is either due to the reflections off the silicon and organic surface, or due to loss of the red photon wich are absorbed at depths greater than the diffusion lengths of the silicon substrate. The overall power efficiency of the device is 10.1%, which to the best of our knowledge is a record for these type of devices [125, 59, 54, 62] by a factor of two and better than the state of the art all-organic solar cells [6].

5.5 Conclusion

A hybrid silicon/organic heterojunction for photovoltaic applications is proposed, that could be a viable low-temperature alternative to the traditional p-n junctions for silicon-based solar cells. The crucial design parameters for efficient photovoltaic operation on n-type silicon wafers have been outlined: a) a low offset between silicon valence-band and the HOMO for a high photocurrent and b) a large offset between the silicon conduction-band and organic LUMO for a high open-circuit voltage.

The fundamental current transport mechanisms in organic(P3HT)/silicon heterojunction solar cells were investigated. The absorption and separation of photocarriers in these devices happen predominantly in silicon and not P3HT. The role of P3HT as an electron-blocking organic was confirmed. The open-circuit voltage of these devices is limited by the minority-carrier injection of the holes into the silicon. By integrating a transparent conductor on top of the Si/P3HT heterojunction, and optimizing the structure, a 10.1% efficient silicon/organic heterojunction solar cell was demosntrated.

While the 63 pA/cm^2 value is still lower than the state of the art p-n junction solar cells (¡100 fA/cm^2), there is still considerable room for improvement. At present the device does not have any light trapping structures, there is no back-surface field, etc. All these reasons will be discussed in more detail in Chapter 7.

Chapter 6

Stability of Silicon/Organic Heterojunctions

6.1 Introduction

Organic thin-films degrade in oxygen and water rich environments. The problem is especially acute in organic solar cells, because light accelerates many of the degradation mechanism, limiting the performance even further [10, 11, 126]. On the other hand, silicon solar cells are very stable, with guaranteed performance for 25+ years. In order to compete with conventional silicon solar cells, the heterojunction solar cells also need to demonstrate 20 year lifetimes.

The first step toward improved stability is characterization. In this chapter data from some preliminary stability studies are presented for PQ-passivated silicon surfaces and Si/P3HT heterojunction solar cells. The basic question we are asking is: how quickly do silicon/organic heterojunctions degrade?

The stability of PQ passivation is studied using the minority-carrier lifetimes and I- V characteristics of field-effect devices. The stability is found to be a strong function of encapsulation. At an unprotected PQ-passivated silicon surface (Chapter 3), the

minority-carrier recombination lifetime were stable for only 1-2 days (Section 6.3.2). However, at resin encapsulated silicon/PQ surfaces, the quality of the passivation not only stays stable but *improves* over a period of 2-4 months (Section 6.3.3). A simple mechanism to explain this behavior is proposed in Section 6.3.4.

"All-organic" solar cells degrade via many mechanisms [11] (Table 6.1). Out of the known mechanisms, the first two are not relevant in the silicon/organic heterojunction cells simply because the materials and interfaces most susceptible to degradation in "all-organic" cells are not present in heterojunction cells, e.g. there is no ITO/PEDOT interface or low work-function electrodes such as Ca/Al. Furthermore, most of the light absorption and carrier separation occurs in silicon, which is stable material, so issues relating to stability of the bulk heterojunction are not relevant for SOH solar cells.

The two materials that are used in SOH solar cells and whose stability is circumspect, are the organic polymer P3HT - which is known to photo-oxidize [127, 128], and transparent conductor PEDOT:PSS - which degrades with both humidity [129, 130], heat [131], and light [132]. Also of concern is the stability of Si/organic interface because the unpassivated Si surface may get more "defective" with time and lose its ability to efficiently separate photogenerated charge carriers. As of yet, we have not conducted any stability studies on the Si/P3HT heterojunction solar cells, but stability is a prime subject for future research.

6.2 Fabrication and Methods

All the PQ passivation steps were consistent with recipes described before (Chapter 3). A 10 nm thick layer of thermally evaporated PQ was used to passivate silicon. All the minority-carrier recombination lifetime measurements were done with WCT-120 using test structures that are sensitive to recombination at the top surface. Metal-insulator-

Table 6.1: Known degradation issues of "all-organic" solar cells, and their relevance to Si/organic heterojunction solar cells.

Degradation Mechanisms of "All-organic" PV	Relevant for Si/organic solar cells?
Degradation & leaching of cathode metal into active layer [126, 133, 134]	No low-work function electrodes and Si/metal interface is stable.
Degradation of ITO due to PEDOT [135, 136]	No, ITO/PEDOT interface in the anode stack
Phase separation of bulk heterojunction changes due to diffusion [137]	No bulk heterojunctions and silicon is stable
Diffusion of O_2 and water into P3HT layer [134]	Yes
Photo-induced degradation of P3HT [127, 128]	Yes
Degradation of PEDOT:PSS [129, 130, 132]	Yes

semiconductor capacitors (MISCap) and metal-insulator-semiconductor field-effect transistors (MISFET) were fabricated with an organic resin as the insulator (AZ5214 photoresist), deposited on the PQ-passivated silicon.

6.3 Stability of PQ-passivated Silicon Surfaces

6.3.1 Effect of Illumination: Light Annealing

The PQ-passivated wafers showed a strong response to intense light and in certain cases a marked improvement in passivation quality was measured. The effect is referred to as "light-annealing" in this thesis.

The effect was observed, quite by accident, while conducting routine minority-carrier recombination lifetime measurements using the WCT-120. The process flow was similar to lifetime experiments described in Section 3.6. As before, the recombination lifetime of a special silicon wafer was measured, whose front and back surfaces were passivated with a high-quality thermal-oxide. Next a 1-inch diameter hole was etched on the top surface. After chemical cleaning, PQ was deposited on the exposed

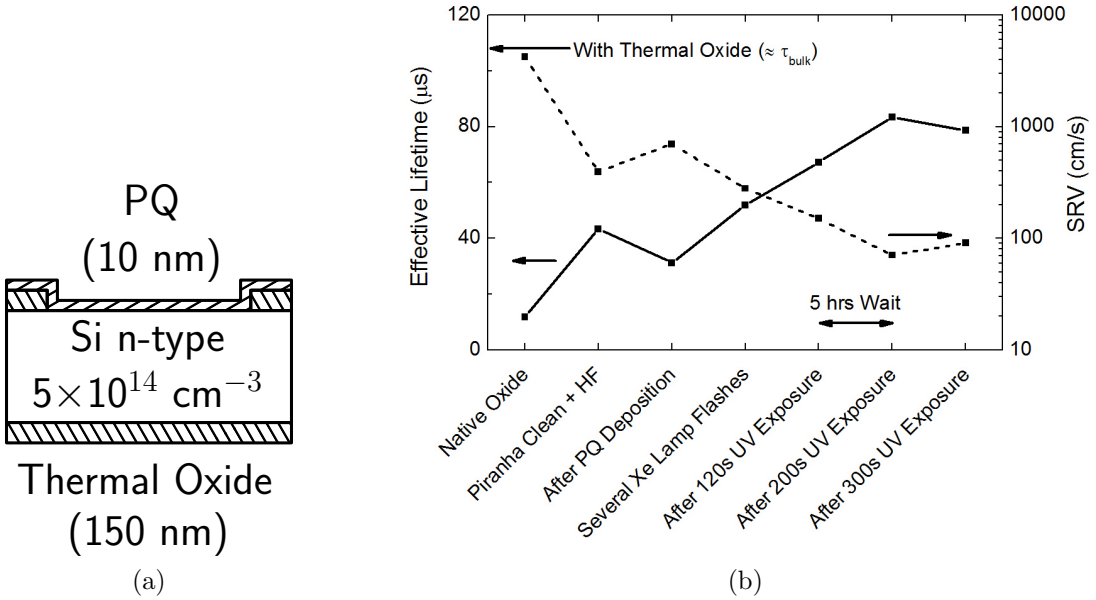


Figure 6.1: (a) Structure of the PQ-passivated test device. (b) Light from a Xe-flash bulb and UV light increases the effective recombination lifetime of minority-carrier in the test device. The extracted surface recombination velocity (SRV) at the Si/PQ interface is also plotted.

silicon, and the recombination lifetime was measured again. The structure of the test device is shown Fig. 6.1(a).

Each measurement by the WCT-120 is accompanied by a light pulse from a Xe-flash bulb, to generate excess carriers in silicon (details of the instrument were discussed in Chapter 3). It was observed that after each successive flash, the PQ-passivated samples showed a small but steady improvement in the recombination lifetime. The effect was cumulative and stable so that, after 20-30 flashes, the effective lifetime of a p-Si wafers, at a minority-carrier density of 10^{15} cm^{-3}, increased from 31 µs to 52 µs (Fig. 6.1(b)). This corresponds to a decrease in surface recombination velocity from 700 cm/s to 279 cm/s. Th effect is quite striking and points to some light-mediated reaction between silicon and PQ that is reducing the electrically active defect-states at the interface.

Some of the known reactions between organics and silicon are induced by light [138, 139, 140]. It is possible that the wide-spectrum intense light from the Xe-bulb,

is enabling a similar chemistry between PQ and silicon. To investigate, samples were exposed to ultra-violet light from a mercury lamp stabilized at an intensity of 2 W/cm^2 at 365 nm wavelength (lamp of the MA6 mask aligner in the cleanroom at CI1 setting). First the sample was exposed for just 10 s. The lifetime jumped from 56 µs to 69 µs. The sample was then exposed for another 20 s, and again the lifetime increased to 72 µs. The lifetime remained at 72 µs even after a subsequent 90 s long UV exposure, and so the experiment was paused and sample was left in air for the next 5 hours.

After 5 hours when the sample was remeasured. Surprisingly, the slow increase in lifetime continued, and with every flash the lifetime increased a little bit, till it got stabilized at 80 µs. A subsequent 200s UV exposure yielded the peak lifetime of 88 µs. A further 300 s UV exposure caused a small drop in lifetime so no further UV experiments were performed.

The full evolution of the recombination lifetime, from the initial native-oxide covered sample to light-annealing is shown in Fig. 6.1(b). The corresponding values of surface recombination velocity, extracted using Eq. (3.9), are also plotted. The bulk lifetime of the silicon was estimated from the lifetime measured when thermal oxide covered the sample (107 µs).

All the PQ-passivated devices described in this thesis showed a similar improvement in measured lifetime after light exposure, albeit with varying performance . The UV exposure turned out to be tricky because the optimum dosage of light, above which passivation starts getting worse, varied from sample to sample. In fact in some cases UV only made the passivation worse. This variability is a problem when making actual devices, because it was not possible to measure lifetime and figure out the optimum UV dosage for each sample individually - actual samples were only 16 mm $\times$ 16 mm, while the WCT-120 requires a samples that at least 25 mm in diameter. Using the Xe-flash multiple times was a more practical option. Typically, samples

were flashed $\sim$ 10 times after PQ deposition.

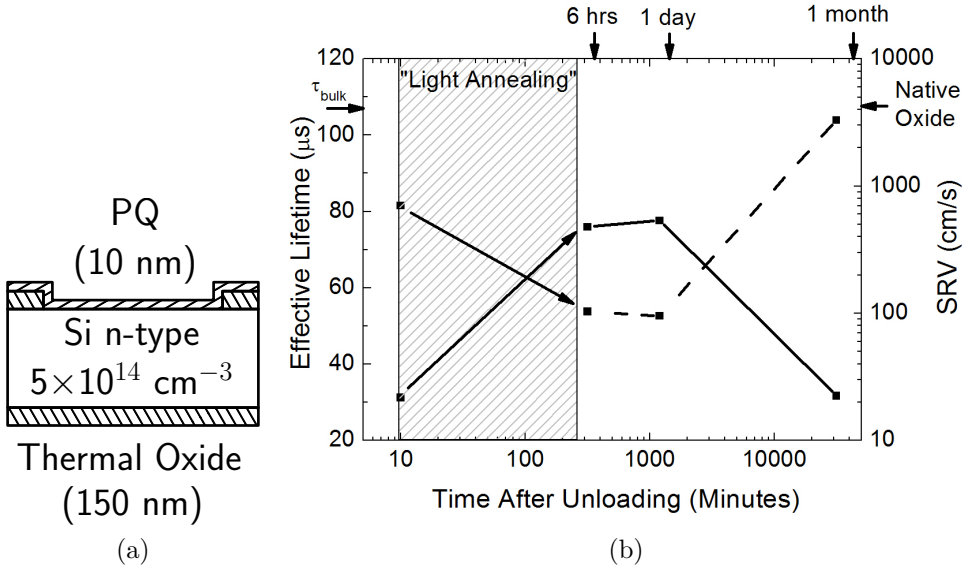
It is possible that the light-annealing we observe is nothing special. The surface states at the silicon/PQ interface might just be trapping charges which causes a decrease is electrical activity of the defects without affecting their density. There are two reasons that this scenario is unlikely:

(a) The effect was never observed in other samples, even those with large defect densities such as native-oxide coated wafers or HF/I_2 passivated wafers. If anything a decrease in lifetime is the norm (Fig. 3.3(b)).

(b) WCT-120 performed a contact-less measurement. The trapped charges have nowhere to go but back into the silicon at some point. If the charges are indeed getting trapped, then over time they will de-trap and the decreased activity of surface defects will be reversed. As we shall show in the following sections, this is not the case and the increase in passivation is maintained for more than 24 hours for un-encapsulated Si wafers and longer for encapsulated Si wafers.

6.3.2 Temporal Stability: Without Encapsulation

The PQ layer is a soft organic material and only a 10-nm-thick layer covers the silicon surface, so there is not much protection for the silicon-PQ bonds. Fig 6.2(b), shows the recombination lifetimes and surface recombination velocity of the same PQ-passivated Si wafer that was measured in Section 6.3, as function of time that the wafer was exposed to ambient air. The time is measured from the moment the sample was unloaded from the PQ evaporation chamber, which was maintained under vacuum, until it was exposed to atmosphere for unloading. During the whole window of measurement, from 10 minutes to approximately 1 month, the sample was kept in ambient air in the clean room, with no special protection from the water, oxygen or light.



(a) (b)

Figure 6.2: (a) Structure of the PQ-passivated test device. (b) The effective lifetime and extracted surface recombination velocity (SRV) of the test device, demonstrating air stability of an unprotected Si/PQ interface.

The details of measurements taken between 10 minutes and 600 minutes, were discussed in previous section. After the "light-annealing", the passivation remains pretty stable for at least another 24 hours Fig 6.2(b). However, measurements taken a month later reveal that the lifetimes falls and reverts bck to the value measured when sample was covered with native oxide Fig 6.2(b). The lifetime could not be improved by any further light-annealing.

There is a remote possibility that the improved passivation was simply a result of good-quality oxide being formed during the UV treatment (we could be forming ozone). However, it is hard to imagine that at room temperature a good quality oxide can form on silicon. Secondly, if such an oxide did form, it is hard to find a reason for it to disappear over 1 month. Therefore we believe that passivation is actually result of PQ bonding on silicon. A possible hypothesis to explain the degradation in passivation that is observed will be discussed in Section 6.3.4.

6.3.3 Temporal Stability: With Encapsulation

The PQ-passivated metal-insulator-semiconductor devices demonstrated in Chapter 3 used a Novolac resin as an insulator (AZ5124 photoresist). Compared to the thin PQ layer, the 1.4 µm thick photoresist can provide substantially more protection to the silicon surface from the ambient oxygen/water. To test if the encapsulation leads to improved passivation and/or passivation stability, recombination lifetimes and device characteristics of encapsulated devices were measured.

Lifetime Measurements

The recombination lifetime test was similar to the one described in the last section. The test samples were PQ-passivated p-type silicon wafer with oxide on the back surface. Other than the Xe-flash, no other light-annealing was performed on these samples (No UV treatment).

Over a period of days, the effective recombination lifetimes improved from 43 µs to 69 µs, ultimately reaching 71 µs. Using the generalized lifetime analysis of Chapter 3 (Eq. (3.8)), surface recombination velocities were extracted from lifetime data. From day 0 to day 6, the surface recombination velocity at Si/PQ interface fell from 250 cm/s to only ≈3 cm/s, comparable to very high quality Si/SiO_2 interfaces.

On the seventh day the samples was washed with methanol to remove the photoresist (and if possible PQ). If the improved passivation was due to some "magical" oxide and not PQ, the lifetimes would continue to be high. However, the measured lifetime permanently fell to only 18 µs, the value expected when the wafer was coated with native oxide. These results show that a) the passivation is due to some silicon/organic interaction that can be washed sway with a solvent and b) if encapsulated, PQ-passivation improves in passivation quality over a period of 8 days.

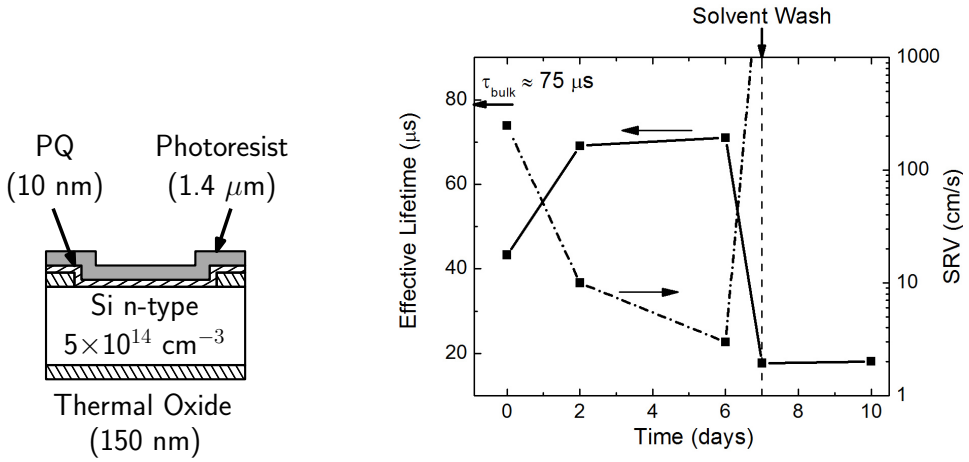


Figure 6.3: Evolution of minority-carrier recombination lifetime in a PQ-passivated silicon wafer, when encapsulated with 1.4 µm thick layer of a Novolac resin (AZ5124 Photoresist). (a) Test structure and (b) Measured lifetime and extracted surface recombination velocity.

Metal-Insulator-Semiconductor Capacitor

The field-effect devices fabricated in Chapter 3 used AZ5124 as an insulator. If AZ5125 also functions an excellent encapsulation and allows the PQ passivation to improve with time, then metal-insulator-silicon devices would also reflect that change.

To confirm the improvement in the quality of an encapsulated PQ/Si interface, the characteristics of a metal-insulator-semiconductor capacitor (MISCap) was measured over time. Between the measurements, the samples were stored in ambient air without any special protection against water oxygen or light. The structure of the MISCap was the same as Chapter 3 (Fig. 6.4(a)): PQ-passivated silicon coated with AZ5214 as the insulator and a gate on the top. Capacitance characteristics measured right after fabrication and 4 months after fabrication show no degradation in the C-V curves but two changes are observed: a) the hysteresis is lower and b) the silicon surface showed deep-depletion.

When the applied bias of across a MISCap is swept from accumulation towards

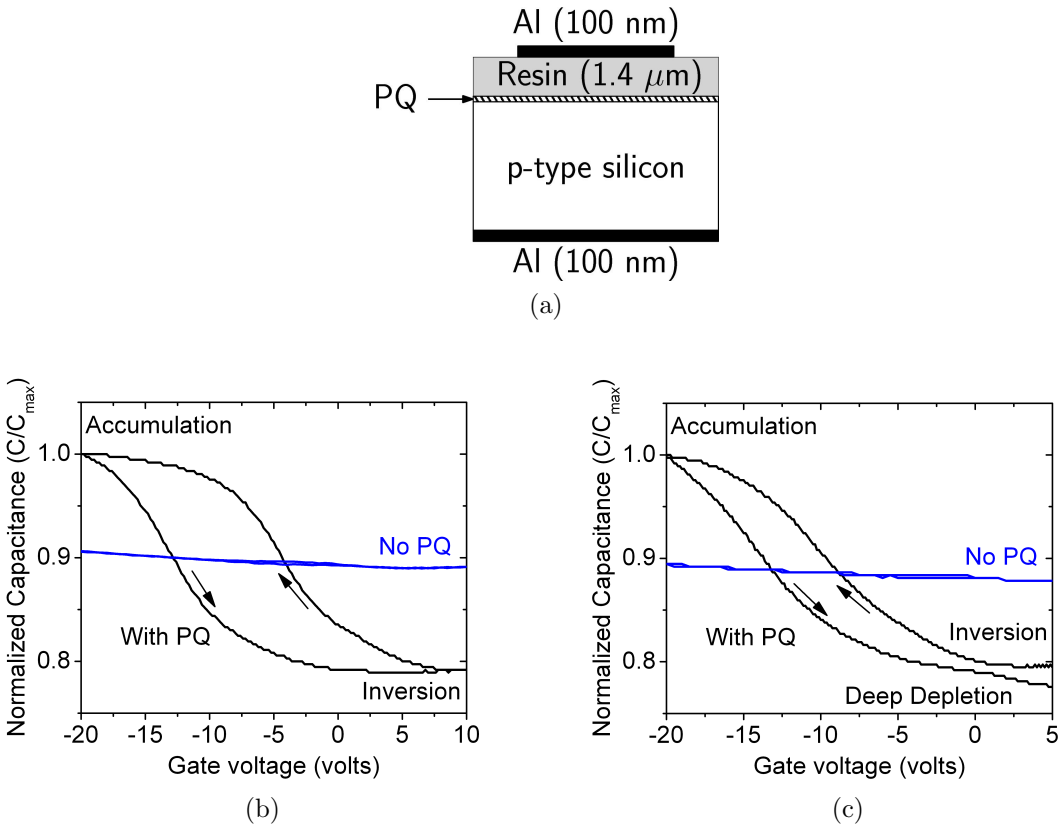


Figure 6.4: Stability of PQ-passivated metal-insulator-silicon capacitor stored in a air. Small-signal capacitance-voltage characteristics at 1 MHz (b) just after fabrication and (c) after 4 months.

inversion, initially there are't enough minority-carriers in silicon to form the inversion layer. According to Shockley-Read-Hall theory, thermal processes try to correct this lack of carriers by a net generation process. The rate at which minority carriers are generated in silicon is characterized by the generation lifetime (τ_g) which, like the recombination lifetime (τ_r), increases with a decrease in the desnity of bulk/surface defects in the silicon. If the generation lifetime is short enough, then the inversion layer is quickly formed and a flat inversion capacitance is measured as one increases the gate voltage (e.g. Fig. 6.4(b)). If however, the generation lifetime is high, the generation rate is unable to generate carriers fast enough to form the inversion layer and the device goes into "deep-depletion", characterized by the decreasing capacitance in one sweep direction - from negative to positive bias (e.g. Fig. 6.4(c)).

Since the "4 months later" characteristics (Fig. 6.4(c)) show evidence of deep depletion, i.e. improved generation lifetimes, it stands to reason that PQ-passivation has improved. In comparison, a similar device, coated with AZ5124 but without PQ, does not show any modulation of the Fermi level or improvement in C-V characteristics. In both "before" and "after" characteristics, the Fermi-level is pinned, indicating very high surface defect densities. So clearly, the improvement is related to Si/PQ interaction and not Si/AZ5124 interaction.

Metal-Insulator-Semiconductor Field-Effect Transistor

Fundamentally the MISCap device is similar to the metal-insulator-silicon field-effect transistor (MISFET) device, so we expect MISFET devices to also improve over time. The current-voltage characteristics of a MISFET are very sensitive to the quality of the semiconductor/insulator interface. Specifically, the sub-threshold slope, mobility and leakage current (I_{OFF}) are all affected by surface defects.

The measured characteristics of a n-channel MISFET, separated by 2 months, are shown in Fig 6.5 & 6.6. This particular batch of samples were stored in a dark glove-box between measurements. However the I-V characteristics evolved along the same line for other devices that were stored in ambient air. I-V characteristics, convincingly show inversion and channel formation, with an extracted electron mobility of ≈600 cm^2/Vs at drain voltage of 0.1 V. After 2 months, the sub-threshold slope becomes steeper: 4.7 V/decade to 3.0 V/decade (Table 6.2). In terms of interface defect-density this change in slope corresponds to 3.6×10^{11} m^{-2} eV^{-1} fewer defects (Table 6.2). The leakage currents, i.e. the drain-source current at zero gate-bias, also reduces by a factor of 10 after 2 months - from 4.7 nA to 0.36 nA (Table 6.2). All these changes are are consistent with a lowering defect-density and improved passivation of silicon by PQ.

In summary, lifetime data, MISCap characteristics, and MISFET characteristics

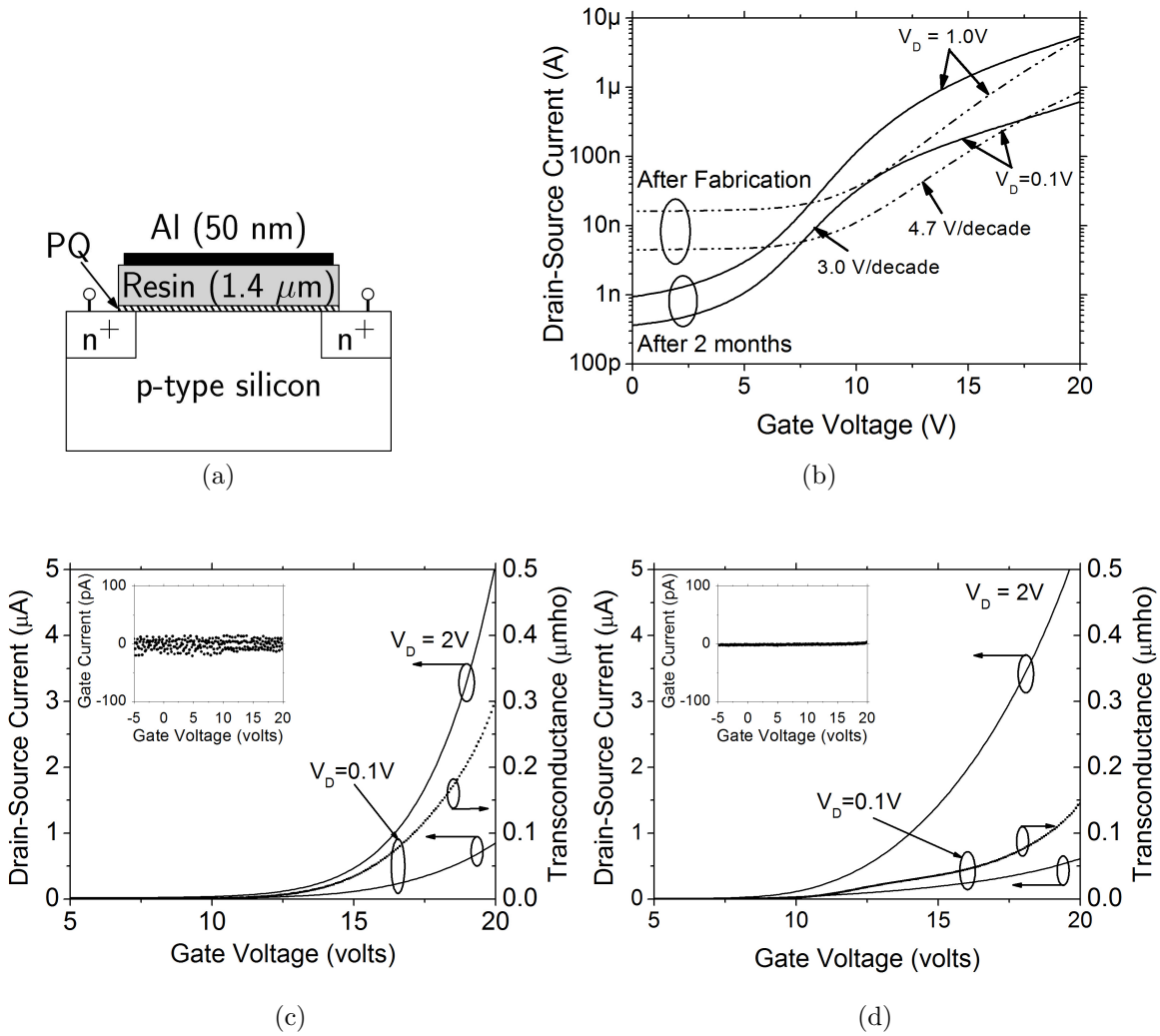
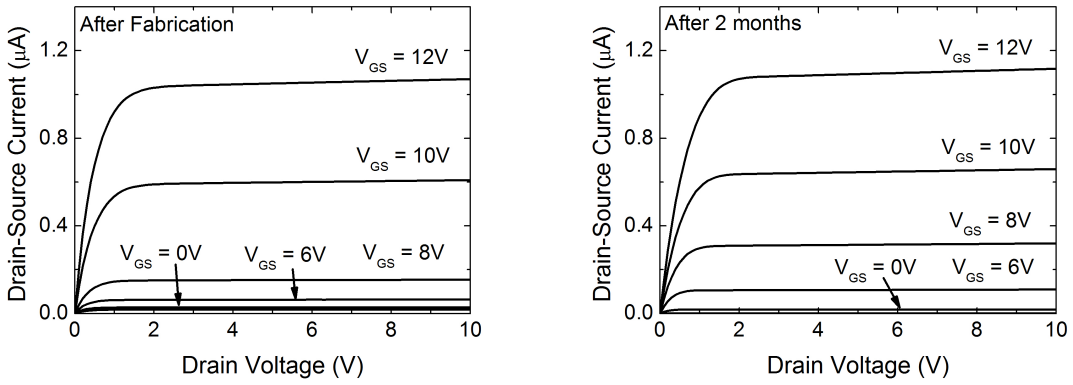


Figure 6.5: Stability of PQ-passivated metal-insulator-silicon field-effect transistor stored in a glove box. (a) Device structure (W/L≈1/1.91). (b) Drain current vs. gate voltage characteristics on log scale, just after fabrication and after 2 months. Transconductance characteristics of the transistor (c) just after fabrication and (d) after 2 months. (b) Drain current vs. drain voltage characteristics at different gate voltages (V_{GS}).(c) Drain current vs. gate voltage characteristics at different low drain voltages in linear and (d) log scale.

measurements show that the silicon surface passivation with the organic molecule 9,10-phenanthrenequinone improves with time, if the surface is protected with AZ5124. AZ5124 on its own does not lead any improvements, so Si/PQ interface must account for the improvements. The capacitors show deep depletion and n-channel transistors show steeper subthreshold slopes and lower off currents. The results can be explained



(a) (b)

Figure 6.6: Stability of I_{DS}-V_{DS} characteristics of a PQ-passivated metal-insulator-silicon field-effect transistor stored in a glove box, (a) just after fabrication and (b) after 2 months.

Table 6.2: The change in the PQ-passivated MISFET characteristics, over a period of two months. Samples were stored in a glove box.

Parameter	After Fabrication	After 2 months
Leakage Current at V_G =0 V & V_D = 0.1 V (nA)	4.5	0.36
Sub-threshold slope (V/decade)	4.7	3.0
Interface density (cm^{-2} eV^{-1})	5.8×10^{11}	3.6×10^{11}

by asserting that, over time, PQ reacts with more of the unsatisfied Si dangling bonds.

6.3.4 Possible Mechanism

Summarizing the results from PQ stability experiment we know that:

- PQ passivation improves with light exposure.
- PQ is stable for at least a day without encapsulation. If encapsulated the device is stable for months in ambient air.
- Encapsulation helps in increasing the quality of PQ passivation.

In this section a simple model to explain these two observations at the Si/PQ interface is presented. This is only a working hypotheses and more experimentation

is required to make a strong statement about its validity. The model is based on two assertions:

1. *The reaction between PQ and silicon is slow.* As discussed in Chapter 3, it has been proposed that PQ bonds to the Si surface dimers through a heteroatomic Diels-Alder reaction [77]. In general, Diels-Alder reactions can be pretty slow, especially in the absence of catalysts, taking several hours to complete [141]. Also exposure to light is known to increase the reaction rate of PQ to C=C (which are chemically similar to Si=Si) [77, 85]. If we are to assert that the reaction of PQ with silicon is very slow, then it is expected that over time PQ will react with more of the silicon dangling bonds and the passivation quality will increase.

2. *Oxygen and humidity can diffuse through the thin PQ layer to reach the silicon surface.* Even at room temperature, a native oxide is formed within hours on a pristine H-terminated silicon surface. During native oxide formation, oxygen penetrates and oxidize the first few monolayers of silicon. If we assert that PQ is a permeable organic layer that can allow oxygen and water vapor to pass through, then silicon atoms underneath the PQ layers could oxidize over time, forming a native-oxide layer underneath the PQ-passivated Si surface. The underlying silicon atoms can continue to get oxidized, even if the uppermost silicon atoms remain bonded to PQ.

The overview of the proposed mechanism is shown in Fig 6.7. When the PQ-passivated surface is left unencapsulated, oxygen and water diffuse through the PQ layer and, over time, start oxidizing the silicon atoms underneath PQ. The resulting native-oxide underlayer is electrically very "defective". When lifetime measurements are taken, the surface recombination properties are limited not by the Si/PQ interface, but by the Si/native-oxide interface. Thus, even though PQ atoms are bonded to

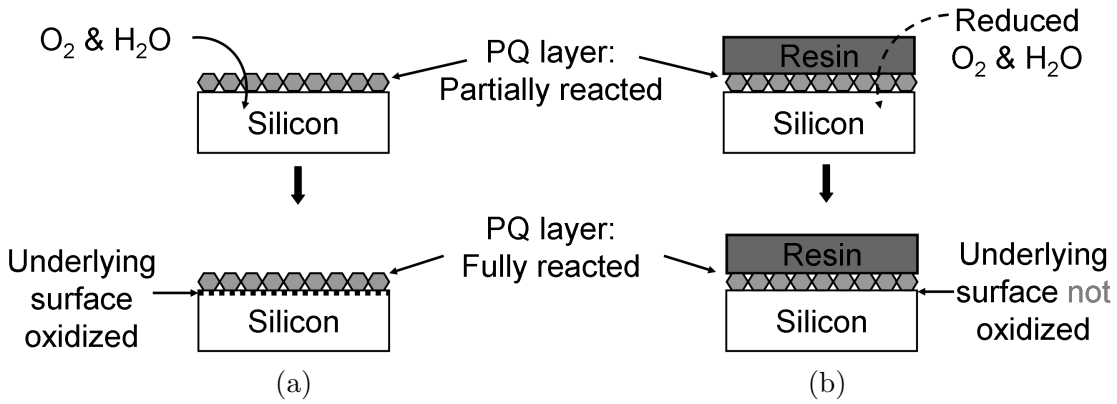


Figure 6.7: Mechanism to explain stability of encapsulated Si/PQ interface. (a) When un-protected, passivation degrades. (b) When encapsulated, passivation improves.

silicon at the top surface, a degradation in passivation quality is observed.

When the PQ-passivated surface is encapsulated, the rate of oxygen and water diffusing through the PQ layer is slowed. Over time the PQ reaction with silicon goes to completion and all the dangling bonds react with PQ. In the absence of a native-oxide underlayer, lifetime measurements are still sensitive to the surface recombination properties of the Si/PQ interface. Since this interface has improved, a improvement in the passivation quality is observed.

6.4 Conclusion

Stability is an issue at the Si/organic heterojunctions, with unprotected devices degrading in several hours. The single most effective method to increase stability is , not surprisingly, encapsulation. Photoresist is found to be an effective encapsulant for Si/PQ interface. Minority carrier lifetime and field-effect devices show that photoresist not just reduces degradation but, over time (up to 4 months), enables an increase in the passivation quality.

Chapter 7

Conclusions and Future Work

7.1 Summary of Results

In this thesis we discussed the use of silicon/organic heterojunctions for photovoltaic applications. Crystalline-silicon based photovoltaics is a high-performance technology but the costs associated with the multiple high-temperature steps and low-throughput equipment makes silicon solar cells expensive to manufacture. Organic semiconductors are purported to be a low-cost alternative to conventional inorganic semiconductors but the performance of organic solar cells is very poor. The goal in this project was to integrate low-cost organic semiconductors on high-performance crystalline silicon to demonstrate low-cost high-performance solar cells.

The key contributions of this work are:

1. Identification of two critical issues that have limited performance in previous devices - unpassivated midgap defects at silicon surface and band-alignment at silicon/organic interfaces. These concepts were used to propose two different types of silicon/organic heterojunctions - one to block minority-carriers from recombining at the Si/metal contacts, and a second to separate photo-generated carriers by blocking majority-carriers at one one of the electrodes. The hetero-

junctions could be used in crystalline silicon photovoltaics as a replacement for diffused p/p^+ and p-n junctions, thereby eliminating all the high-temperatures steps required for dopant diffusions.

2. A novel organic-based passivation scheme for Si (100) surfaces has been developed, that reduces silicon surface defect density, to less than 10^{12} cm^{-2}, without the use of any high temperature steps. The passivation precursor, 9,10-phenanthrenequinone (PQ), is a semiconducting small-molecule that forms a type-I heterojunction with silicon. The low surface defect density is demonstrates by the low surface recombination velocity, less than 150 cm/s, measured at the Si/PQ interface. Furthermore, Fermi-levels at the Si surface are not pinned and can be modulated over a wide range under the electric field of an insulated gate. Low surface defect-density also allows high field-effect mobility to be obtained at the PQ-passivated surfaces - 600 cm^2/V.s and 50 600 cm^2/V.s for electrons and holes, respectively.

3. A minority-carrier blocking p-Si/PQ/TPD heterojunction that prevents electrons in silicon from recombining at the Si/metal contact.

4. A majority-carrier blocking n-Si/P3HT/Pd heterojunction that can be used as a p-n junction replacement in silicon solar cells. The large difference between the LUMO of P3HT and the conduction-band of silicon blocks the electrons in silicon, reducing the majority-carrier current and enabling a high V_{OC}. The heterojunction has a built-in electric field at the silicon surface, due to the difference in work-function of metal and silicon, that can separate photogenerated carriers to give rise to a photocurrent. Using the heterojunction, a 10% efficient crystalline silicon hybrid solar cell was demonstrated.

5. Preliminary stability studies to test stability of the silicon/organic heterojunctions were conducted. The advantageous effects of light exposure and encapsu-

lation on the stability of silicon/organic heterojunctions were demonstrated.

7.2 A Case for Silicon/Organic Heterojunctions

The viability of any photovoltaic technology should ultimately be judged on three criteria:

1. **Efficiency:** The AM1.5 power conversion efficiency of the Si/P3HT solar cells demonstrated in this work is 10.1%, the highest number reported for Si/organic heterojunction devices. Furthermore, 10.1% is at least as high if not higher then published efficiencies for all-organic solar cells ($\sim$ 8 %) [6]. Further, simulations of double-sided silicon/organic heterojunction show that hybrid cells can achieve power efficiencies of over 20%, matching the current state-of-the-art homojunction and heterojunction HIT solar cells.

2. **Cost:** While cost advantages provided the motivation for the work, the thesis does not analyze the cost implications in any detail. However, the energy and capital-investment savings achieved by replacing high-purity/high temperature processing with room-temperature spin-coating (as in all-organic photovoltaic) are self-evident. There are further cost advantages. For instance, common impurities in silicon are known to get activated (thereby killing carrier lifetimes) at high temperatures, so a low temperature process may allow use of cheaper silicon wafers. Overall, we expect significant cost savings in the fabrication costs of crystalline Si solar cells.

3. **Reliability:** As mentioned in the manuscript, crystalline Si solar cells are very stable (>25 years), and heterojunction cells need to demonstrate similar longevity. Our preliminary studies show that as of yet this is not the case ,and heterojunction cells are stable only for a few hours arguably because organic

layers degrade. Good news is that the device has not been optimized for stability yet. Many of the known solutions that increase the device lifetime have not been integrated into the device, e.g. encapsulation barriers, more stable organics, etc. The issue of stability is a more general problem that plagues all organic-based devices and there is growing body of research that deals with precisely this issue. Heterojunction cells will also benefit from these advances. In fact this leads to a related question - are silicon/organic structures more reliable than all-organic cells? We have reason to believe that they are. Simply because the silicon/organic structures are inherently immune to many of the reliability problems that plague all-organic cells. For example, the silicon/organic cells do not have a degradation-prone low work-function metal/organic interface; unlike P3HT/PCBM organic devices, in heterojunction cells there is no metastable inter-penetrating bulk heterojunction; silicon is the primary absorbing layer which is known to be long-term stable; and in the ultra-thin P3HT ($\sim$10 nm)layers of heterojunction device there aren't many excited states which are usually the cause for photo-oxidize of the polymer.

In summary, silicon/organic cells have a very high possibility of achieving an efficiency/cost/reliability combination that could have substantial long-term impact. The work in this thesis explicitly deals with efficiency component of the argument, the other criteria could be the subject of future work.

7.3 Future Work

7.3.1 Improving Efficiency of Silicon/P3HT Heterojunction

The power conversion efficiency of silicon/organic heterojunction can be further increased from the present 10% to around 15% by incremental improvements in the design of the present Si/P3HT solar cell. A set of possible approaches could be:

Increasing the Short-Circuit Current

In baseline heterojunction device, the short-circuit current is only 29 mA/cm^2, lower than $\sim$ 40mA/cm^2 achieved in the best p-n junction Si cells. The primary reason for lower J_{SC} is substantial top-surface reflection due to lack of light-trapping - there is no anti-reflection coating or surface texturing. Solution processed AR coatings using commercially available fluorinated polymers can be used [142, 143]. Another option is integrate "moth-eye" textured plastic films on top of the silicon/organic heterojunction solar cell using optical adhesives [120, 122]. Silicon surface could also be textured, using anisotropic etchants, to increase carrier absorption in silicon [123].

Some of the blue photons get absorbed in the top organic layers, which accounts for another 7% of the loss in J_{SC}. To reduce absorption losses, thickness of the organic layers can be reduced by changing deposition conditions and formulation of organic inks. To reduce absorption losses in the top electrode stack (metal grid + PEDOT layer), more transparent and more conductive electrodes can be used, e.g. ITO or doped ZnO [144]. However, if the sputtered metal-oxide causes too much mechanical damage on the underlying organic (P3HT) layer, solution-processed ZnO [145, 146] and ITO [147] films could be used. Finally, nanowire metallic meshes can be used to increase the conductivity of top electrode [148], allowing a sparser top metal-grid.

Increasing the Fill Factor

The fill factor of baseline silicon/organic heterojunction cell is only 0.59, mainly due to the ohmic losses in the organic films, especially PEDOT:PSS. Addition of solvents like DMSO, ethylene glycol, isopropyl alcohol, etc. is a well-known method of boosting PEDOT conductivity [149, 150]. Certain surfactants, like Zonyl [151] and sodium dodecyl sulfate [152], are also known to enhance the conductivity of PEDOT:PSS thin films. Series resistance can also be reduced by doping P3HT layers with organics

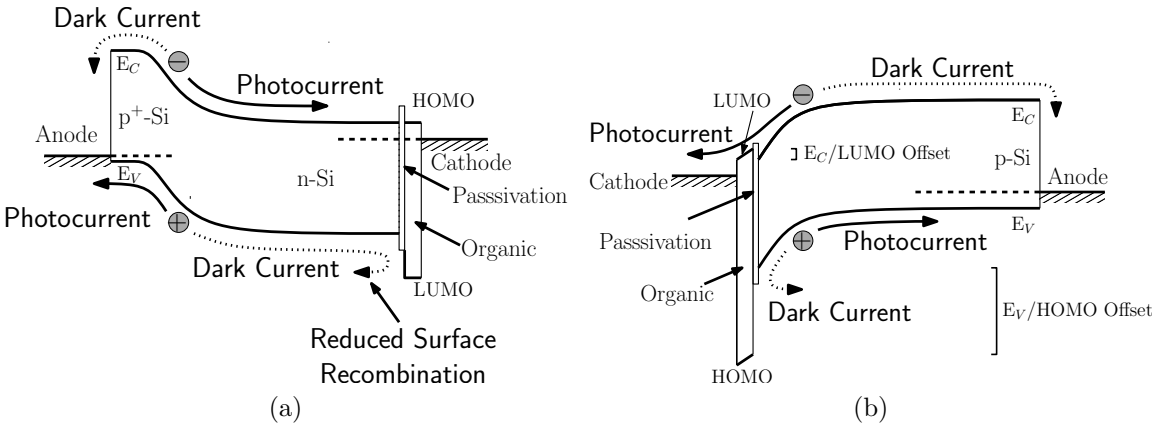


Figure 7.1: Band-diagram of a hole-blocking heterojunction configured as (a) a minority-carrier blocking layer on n-type Si and (b) a majority-carrier blocking layer on p-type Si.

such as F4-TCNQ [118].

7.3.2 Hole-Blocking Silicon/Organic Heterojunctions

Both the heterojunctions demonstrated in the thesis block electrons but no hole-blocking heterojunction were presented. Complimentary heterojunctions that block holes could be a possible direction of future work. As in the electron-blocking heterojunctions, hole-blocking heterojunction can also be in two flavors: minority-carrier blocking (Figure 7.1a) and majority-carrier blocking heterojunctions (Figure 7.1b).

Many electron-conducting organic materials are known ($PC_{60}BM$, C60, DCNnCQA, etc.) with reported LUMO levels around 4.0 eV and HOMO levels greater than 5.2 eV, so they should form hole-blocking heterojunction with silicon.

7.3.3 Double-Sided Silicon/Organic Heterojunction Solar Cell

As demonstrated in Chapter 4 and 5, the dark-current in a single-sided heterojunctions is invariably dominated by the current due to the complimentary carrier, e.g. the dark-current in a majority-carrier blocking heterojunction is dominated by minority-carrier current. In order to drive down the dark-current even further and obtain >

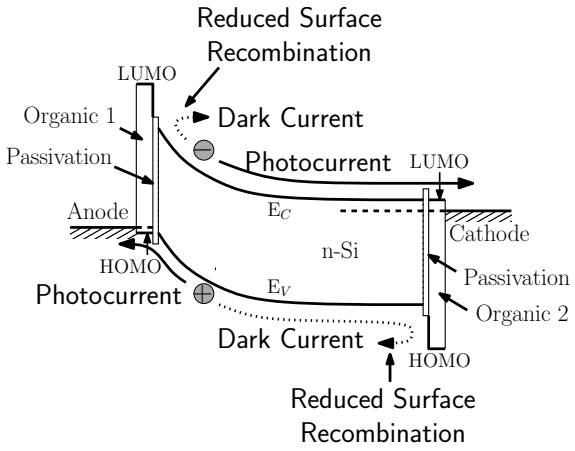


Figure 7.2: Band Diagram of double-sided heterojunction solar cell with a electron-blocking layer at the top and hole-blocking layer on the bottom.

20% efficient heterojunction solar cell, two heterojunctions need to be integrated on the same device to form a double-sided heterojunction cell that block both carriers.

Figure 7.2 shows one possible double-sided heterojunction cell fabricated on a n-type silicon, with an electron-blocking heterojunction on the front side and a hole-blocking heterojunction on the back side.

7.3.4 Improve Stability of Silicon/P3HT Heterojunction

Heterojunction solar cells use organic materials, so the device lifetime is limited by the stability of the organic layers. Fortunately, the organic layers perform a very narrow role in silicon/organic heterojunction solar cells and many of the most damaging degradation mechanisms of "all-organic" solar cells are not active in silicon/organic heterojunction solar cells (discussed in the introduction of Chapter 6). One future endeavor could be to characterize and improve the stability/reliability of silicon/organic solar cells.

Lifetime Measurement Setup

Presently there is no infrastructure to measure solar cell stability. The measurement system should be capable of temperature, humidity, & oxygen concentration control.

The design of a lifetime measurement setup for organic solar cells has been detailed in literature [153]. Commercial systems are also available [154]. A similar set up needs to be built/bought for silicon/organic heterojunction stability studies.

Degradation Mechanisms

Degradation rates would need to be measured in controlled environment (dry air, nitrogen, humid nitrogen) to isolate the conditions under which degradation is most severe [155]. Also the primary physical location of the degradation (PEDOT, P3HT, or silicon/organic interface) needs to be found. One way could be to substitute PEDOT with a semi-transparent layer of metal (<15 nm) to form silicon/organic heterojunction devices without PEDOT:PSS. Alternatively, P3HT could be replaced with a more stable organic, e.g. P3CT [126]. While the absolute efficiency of these devices maybe lower, a change in degradation rate will tell if degradation in PEDOT or P3HT layers limits lifetime of silicon/organic heterojunction cells.

Low-temperature Encapsulation Layer

Present generation heterojunction cells do not have any encapsulation barriers to protect organic layers from environment. The commercially available BARIX encapsulation uses sputtered AlO_x [156], which may cause mechanical damage on the top organic layers, so an alternative encapsulation barrier is required. Quality of the encapsulation is usually measured, by the Ca encapsulation test, in terms of WVTR ($gm/m^2/day$) and a WVTR below 10^{-6} $gm/m^2/day$ is required to demonstrate lifetimes of >10 years. Some of the possible encapsulations that can be considered are "Hybrid-permeation barrier", ALD deposited AlO_X, parylene/AlO_X, parylene/SiNx, etc. [157, 158, 159].

More Stable Organics

If PEDOT limits the lifetime of heterojunction solar cells, it could be substituted with more stable transparent conductors, such as SPDPA [160], Aedotron [161], ZnO and ITO [145, 146, 147]. If the hydrogen-passivated Si/organic interface degrades quickly, intermediate layers could be added between silicon and organic to stabilize the heterojunction interface, e.g. SAMs [73] or thin-oxide films [67]. If P3HT degradation limits stability, any organic with the correct HOMO/LUMO offsets can be used in place of P3HT for silicon/organic heterojunction cells, e.g. P3CT [126], transition metal oxides, such as V_2O_5 [162], solution-processed MO_3 [163], and solution-processed NiO_X [164].

Accelerated Lifetime Measurements

Lifetime of current generation silicon/organic heterojunction devices is only hours but with improvements the lifetimes are expected to increase. Once the lifetimes exceed 1 month, real-time studies are not practical and test will be done at accelerated conditions [165].