Sub-100nm Vertical MOSFET's with $Si_{1-x-y}Ge_xC_y$ Source/Drains

Min Yang

A DISSERTATION
PRESENTED TO THE FACULTY
OF PRINCETON UNIVERSITY
IN CANDIDACY FOR THE DEGREE
OF DOCTOR OF PHILOSOPHY

RECOMMENDED FOR ACCEPTANCE
BY THE DEPARTMENT OF
ELECTRICAL ENGINEERING

June 2000

SUB-100NM VERTICAL MOSFET'S WITH SIGEC SOURCE/DRAINS

Min Yang

A DISSERTATION

PRESENTED TO THE FACULTY

OF PRINCETON UNIVERSITY

IN CANDIDACY FOR THE DEGREE

OF DOCTOR OF PHILOSOPHY

RECOMMENDED FOR ACCEPTANCE

BY THE DEPARTMENT OF

ELECTRICAL ENGINEERING

June 2000

Abstract

Vertical MOSFET's have been widely studied for two practical reasons. First, the channel length may be determined by the epitaxial layer thickness instead of lithography resolution. Second, the vertical structures may save chip area and increase packing density.

In the present work, the channel lengths of vertical p-channel MOSFET's have been scaled down to sub-100nm for the first time by introducing thin $Si_{1-x-y}Ge_xC_y$ layers to significantly suppress boron diffusion from the heavily doped source/drains into the channel region during gate oxidation and other high temperature processing after epitaxy. The effects of doped and undoped SiGeC layers on the device performance have been studied.

Ultra-sharp phosphorus profiles in the in-situ doped silicon epitaxial layers grown by low pressure rapid thermal chemical vapor deposition have been achieved for the first time in this work. This was made possible by using an interrupt-growth technology. Using an ex-situ etching of 2-5nm off the Si surface after n^+ epitaxy, a sacrificial wafer growth to reduce the background doping inside the reactor chamber, and an in-situ 800^oC bake in H_2 before re-growth, the trailing edge of the phosphorus profile has been improved from 155nm/decade to 13nm/decade, with an oxygen and carbon-free interface, enabling the fast dopant transitions in the vertical MOSFET's.

Combining the technologies of highly-doped SiGeC in the source and drain for boron diffusion control during process and interrupt-growth for phosphorus profile control during epitaxy, sub-100nm vertical p-channel MOSFET's on the sidewalls of wide mesa, have been demonstrated for the first time. The devices exhibit well-behaved on and off characteristics. No leakage current due to the SiGeC layers or the growth interruption has been observed. Device operation with a 25nm channel length has been achieved. Vertical n-channel MOSFET's on wide mesas have also been demonstrated.

To eliminate the short channel effects for MOSFET's with sub-100nm channel lengths, vertical double-gate MOSFET's with ultra-thin pillars have been proposed. Use of epitaxy to form the device active region is proposed as our approach. Key fabrication technologies have been developed in this work, including selective epitaxy, side wall thin gate oxide growth on a low thermal budget, self-aligned polysilicon etching, etc.

While MOSFET's are aggressively scaling into sub-100nm regime, novel three-dimensional structures and effects become very important. The effects of elastic relaxation on 1-D and 0-D $Si_{1-x}Ge_x/Si$ pseudomorphic structures have been calculated both by analytical and numerical methods in this work.

The carbon levels used to reduce the dopant diffusion in the vertical MOSFET's of this work were low (0.4%), and a negligible carbon effect on the bandgap is expected (~8meV). In chapter 8, the effect of higher levels of carbon (~1%) on the conduction band, valence band, and bandgap of $Si_{1-x-y}Ge_xC_y/Si(001)$ (in planar 2-D structures) is systematically evaluated, considering both the strain and intrinsic effect of carbon atoms.

Acknowledgements

The work presented in this dissertation would not have been possible without the contribution of many individuals. These people deserve my most sincere gratitude for their assistance during my graduation education at Princeton.

First and foremost, I thank my advisor, Professor James Sturm, for encouraging me to come to Princeton in 1994, which has become a critical step in my career. His support and optimistic attitude through out this work was essential for all the achievements of the present work. Special thanks go to Prof. Steven Chou and Prof. Sigurd Wagner for reading this thesis.

I would like to thank all the members of Prof. Sturm's group for their help and collaboration. Outside the lab, I would like to thank Michael Valenti, Duane Marcy and Joe Palmer for the help in the clean room, Nan Yao for educating me in the use of the SEM machine at the Princeton Materials Institute, and Temel Büyüklimanli of Evans East for performing all the SIMS measurements. Special thanks go to Dr. Shalom Wind of IBM for his joint initiation of this project, his helpful discussions and assistance in the area of E-beam lithography.

I thank all my friends who have brought me many wonderful memories in the past five years. I am greatly indebted to Mrs. Dorothy Katz and her family for their hospitality. I also own a great gratitude to my music teacher, William Sheibinger, who made my last year at Princeton truly enjoyable.

No words can describe the appreciation for all the support from my parents through out all these years. I would like to thank my fiancé, Louis Ernst, for being my best friend and giving the greatest level of support which I have come to rely on.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Thesis Overview

When CMOS is scaled into the sub-100nm regime, short-channel effects, punch-through, dopant fluctuation, etc., limit the device performance. The double-gate MOSFET is predicted to have superior advantages over the conventional single-gate MOSFET because the gate has more control over the channel. It also has high immunity to short-channel effects and the punch-through problem. For an ultra-thin channel, the subthreshold slope is also significantly improved. The double-gate also gives a high transconductance and allows for high packing density. Various fabrication approaches for double-gate MOSFET's have been reported. A vertical structure is used in this work, so that the channel length may be determined by the epitaxial layer thickness instead of the resolution of lithography or reactive ion etching (RIE). The channel length of a vertical MOSFET can be controlled to a few tenths of a nanometer by molecular beam epitaxy or chemical vapor deposition.

Two critical problems with regard to the scaling of vertical MOSFET's were addressed in this thesis. For p-channel MOSFET's, boron diffuses from the heavily doped source and drain into the channel region during gate oxidation or other high temperature processing after epitaxy. For both p-channel and n-channel MOSFET's, ultra-sharp n-type dopant profiles are very difficult to obtain by conventional low pressure chemical vapor deposition (LPCVD).

With respect to the first problem, it was found that boron diffusion is mainly due to

the oxidation-enhanced-diffusion effect. During oxidation, silicon interstitials are injected and subsequently enhance boron diffusion. We found that by adding $Si_{1-x-y}Ge_xC_y$ layers into vertical p-channel MOSFET's, boron diffusion can be effectively suppressed, as substitutional carbon atoms can act as an intersitial sink. The position of the $Si_{1-x-y}Ge_xC_y$ layer in the structure has been studied. The highly doped $Si_{1-x-y}Ge_xC_y$ layers inside the source and drain region can eliminate the deleterious effects from the alloy or alloy/gate oxide interface. No excess leakage current is observed due to the SiGeC layers.

Phosphorus doping in Si and $Si_{1-x}Ge_x$ epitaxy is studied in the rapid thermal vapor deposition (RTCVD) system using dichlorosilane as a silicon source and phosphine as a phosphorus source. At temperatures of 700$\sim$1000^{o}C, the silicon growth rate decreases with an increase in the phosphine flow rate. The phosphorus doping level saturates at high phosphine flow rates. The transition slope, especially on the trailing edge after shutting off phosphine flow, is very slow, leading to a high background doping level in the subsequent layers. For SiGe grown at 625^{o}C, higher levels and sharper profiles of phosphorus doping are observed. To improve phosphorus doping in silicon epitaxy, the growth is interrupted after n^+ epitaxy and the wafer is removed from the growth reactor. A thin layer is chemically etched away from the silicon surface. A SiGe sacrificial wafer is also grown during the interruption to reduce the residual phosphorus in the system. An *in-situ* 800^{o}C 10torr bake in hydrogen is used before the subsequent growth. The end result is a phosphorus doping profile improvement from 155nm/decade to 13nm/decade. No oxygen or carbon contamination is observed at the interruption interface. The improved phosphorus doping profile enables the fabrication of vertical n-channel MOSFET's, where the sharp transitions of source and drain are required, as well as p-channel MOSFET's, where controlled channel n-type doping for wide mesa structures is required.

Vertical p-channel MOSFET's with channel lengths down to 25nm are demonstrated on the side-walls of wide mesas, using SiGeC to control the boron doping profile in the source and drain and using interrupt-growth to improve the phosphorus doping profile in the channel. No excess leakage current resulting from either of these two novel techniques are observed. Vertical n-channel MOSFET's have also been fabricated.

In the study of vertical MOSFET's, a "planar epitaxy" approach has been used in this work, where the wide mesa was created by RIE after the epitaxy. Some fabrication technologies associated with vertical MOSFET's as well as some general Si processing techniques have been developed for the first time at Princeton during the course of this work. High quality thin gate oxide (<100Å) grown at low temperature (T≤750^{o}C) in wet oxygen has been achieved, both on planar silicon substrates and on the side-walls of silicon pillars. *In-situ* highly doped p^+ and n^+ poly-silicon has been successfully deposited in the RTCVD system. Poly-silicon gate RIE has been investigated and approaches to reduce the damage on the underlying thin gate oxide have been achieved by using very selective chemistry and using an interferometric technique to control the end-point. Highly anisotropic SiO_2 and Si etching have been obtained, enabling ultra-thin vertical pillars for double-gate MOSFET's.

The ultimate goal of this work is to fabricate double-gate MOSFET's with sub-100nm channel lengths on ultra-thin pillars. Although double-gate devices on ultra-thin pillars have not been finally demonstrated, key fabrication techniques have already been developed. A "selective epitaxy" approach is proposed to grow an ultra-thin channel and form a "mushroom" structure for the self-aligned poly-silicon gates. Up to 120nm silicon layers have been selectively grown through patterned oxide windows at 700^{o}C. At such a low temperature, dopant diffusion during epitaxy can be completely suppressed. Poly-Si self-aligned etching has been demonstrated. Gate oxide and MOS devices have been made on the side wall of the epitaxy layers.

In advanced CMOS technology, there is increasing interest in heterostructures, such as SiGe poly-silicon gates[1, 2, 3], SiGe MOSFET's[4, 5, 6], etc. Recently there have been many studies on SiGeC alloys due to the strain adjustment and dopant diffusion control afforded by the carbon atoms. In this work, systematic calculation of band gap and band alignments are performed for strained $Si_{1-x-y}Ge_xC_y$ alloys on a planar silicon substrate, and for SiGe quantum dots and quantum wires buried in a silicon matrix. Numerical calculations using the finite element method have been used for calculations of the band structure of V-grooved SiGe quantum wires.

1.2 Thesis Outline

Chapter 2 gives an overview of advanced CMOS technology and the limitations of scaling. Characteristics of double-gate MOSFET's are presented using MEDICI simulations. Various approaches for fabrication of double-gate MOSFET's are discussed. The method of using epitaxy to grow a vertical channel is proposed in this work.

Chapter 3 lists the process flows for two epitaxial approaches used in the present work for the fabrication of vertical MOSFET's. The "selective epitaxy" approach is used to fabricate vertical double-gate MOSFET's on ultra-thin pillars, and the "planar epitaxy" approach is used to fabricate vertical MOSFET's on wide mesas to study the scaling of vertical structures. Key process steps have been discussed in detail.

In Chapter 4, phosphorus doping in Si and SiGe epitaxy using dichlorosilane as a silicon source is investigated. Ultra-sharp phosphorus doping profiles in silicon grown at 700^o are achieved by a growth-interruption in this work.

Chapter 5 addresses two key novel techniques introduced in the fabrication of vertical p-channel MOSFET's during this thesis work. They are the use of SiGeC in the source and drain to control boron doping profiles and the implementation of the phosphorus doping profile control strategy of Chapter 4. Sub-100nm vertical p-channel MOSFET's are demonstrated.

Chapter 6 presents the current ongoing work on vertical n-channel MOSFET's and the related problems. Thermal stability of vertical MOSFET's is also under investigation. Future work regarding vertical heterojunction MOSFET's are included.

Calculations of the band structure of one-dimensional quantum wires and zero-dimensional quantum dots in the Si/SiGe system are given in Chapter 7. Finite-element simulation is used to calculate the band structure of a buried V-groove structure. Quantum confinement energies are also calculated and photoluminescence results are predicted.

In Chapter 8, band gap and band offset of $Si_{1-x-y}Ge_xC_y$ strained layers on silicon (001) substrates are calculated using Van de Walle's "model-solid" model. Both tensile and compressive strained conditions are considered and results are compared with published

experimental data. Band structures under the strain-compensated condition are predicted.

Chapter 9 is a summary of the contributions of this thesis. The appendices give specific details of the experimental conditions used in this work. The exact growth condition of epitaxial structures for typical vertical p-channel MOSFET's and for p^+ polysilicon are given in Appendix A and B, respectively.

Chapter 2

Motivations for Vertical Double-Gate MOSFET's

In this chapter, the problems associated with CMOS scaling down to sub-100nm channel lengths are summarized. To suppress the short-channel effects, double-gate MOSFET's (DG-MOSFET's) are demonstrated to be a promising alternative. Simulation results of the device properties of DG-MOSFET's are presented. For an ultra-thin fully-depleted channel, drain induced barrier lowering, drive current, and subthreshold slope are all improved in DG-MOSFET. Various fabrication approaches of DG-MOSFET's are discussed. A method using epitaxy to define the channel length is proposed in this work to fabricate vertical DG-MOSFET's.

2.1 CMOS Scaling into the Sub-100nm Regime

2.1.1 Scaling Trend and Goals

After more than two decades of relentless scaling to ever smaller dimensions, the metal-oxide-semiconductor field effect transistor (MOSFET) has become the prevailing technology for very large scale integration (VLSI) applications today. These advances have led to computers and networks with far superior performance and dramatically reduced cost per function. Currently, 0.35-μm CMOS technology with 0.25-μm channel length is being used in the manufacturing of 64-Mb DRAM's and 200-MHz microprocessors with the number of

transistors per chip in the 10^7-10^8 range. Meanwhile, sub-100nm MOSFET's with ultra-thin gate oxide (<35 Å) have recently been fabricated in research laboratories [7, 8, 9, 10, 11, 12, 13, 14, 15]. Table 2.1 gives the historical trends [16] and Table 2.2 gives the future projection from the *1998 Semiconductor Industry Association Roadmap* [17].

Year of Introduction	1977	1980	1983	1986	1989	1992	1995	1997
Minimum Feature (μm)	3	2	1.5	1	0.7	0.5	0.35	0.25
DRAM Density	16K	64K	256K	1M	4M	16M	64M	256M
Gate Oxide (nm)	70	40	25	25	20	15	7-12	4-5
V_{CC} (V)	5	5	5	5	5	5	3.3	1.8-2.5

Table 2.1: Historical scaling trend of the MOSFET [16].

MOSFET scaling is driven by two goals: (1) to increase the *packing density* of the transistors on a chip and/or (2) to increase the *speed* of the transistors. The first goal of MOSFET scaling directly leads to the size reduction of the planar dimension of MOSFET, reducing manufacturing cost assuming the cost per wafer is constant. The delay of CMOS can be expressed by [18]:

$$\tau_{pd} = k_1 \frac{C_L V_{DD}}{I_{Dsat}} + K_2 R_w C_w = k_3 \frac{C_j + C_{ox} + C_{w'}}{C_{ox} \frac{(V_{DD}-V_{th})^{\Gamma}}{L_{eff}^{\beta}}} + K_2 R_w C_w \tag{2.1}$$

where V_{DD} is operation voltage, C_L is the total load capacitance, and R_w and C_w are interconnect resistance and capacitance. To increase the *speed* of digital integrated circuits, the MOSFET saturation current I_{Dsat} must be increased. Despite the onset of some velocity saturation, it has been observed that the drive current still increases as L decreases. If the other dimensions of the transistor remain constant, the speed of the transistor will increase by reducing the gate length. This is essential in modern devices where C_L is dominated by the interconnect capacitance and V_{DD} is reduced for low power consumption and reliability

Year	1997	1999	2002	2005	2008	2011	2014
DRAM (bits/chip)	256M	1G	4G	16G	64G	256G	1T
DRAM chip size (mm^2)	280	400	560	790	1120	1580	2240
μP Transistor/cm^2	3.7M	6.2M	18M	39M	84M	180M	390M
μP chip size (mm^2)	300	340	430	520	620	750	901
wafer diameter (mm)	200	200	300	300	450	450	450
General lithography (nm)	250	180	130	100	70	50	35
μP Gate length (nm)	200	140	100	70	50	35	25
T_{ox} Equivalent (nm)	4-5	3-4	2-3	1.5-2	$<$1.5	$<$1.0	
supply voltage (V)	1.8-2.5	1.5-1.8	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6	0.37-0.42
Clock (MHz) (local)	750	1250	2100	3500	6000	10000	16903
DRAM Cost (μcent /bit)	120	40	15	5.3	1.9	0.66	0.23
μP Transistor Cost (μcent /transistor)	3000	1735	580	255	110	49	22

Table 2.2: Technology roadmap for semiconductors by Semiconductor Industry Association (SIA) [17].

concerns. Increasing MOSFET drive current also requires larger gate oxide capacitance (thinner gate oxide and/or higher dielectric gate insulator).

The scaling of MOSFET's is constrained by two requirements: First is the achievement of an acceptably low leakage current when the transistor is "off". However, I_{off} will increase in short-channel MOSFET's due to the following effects: drain-induced barrier lowering (surface DIBL), punch-through (bulk DIBL), gate-induced drain leakage (GIDL), impact ionization from hot carriers, and others. Second, scaling requires acceptable reliability and reproducibility, which may also be decreased by: the short channel effect (threshold voltage V_{th} roll-off at short channel length L), gate oxide degradation due to the hot carrier injection, metallization reliability, effects of random doping distribution, etc. As CMOS scaling approaches sub-100nm dimensions, all the problems mentioned above become increasingly significant [19, 20, 21, 16, 22, 23, 24, 25, 26]. Some of the above effects on short channel MOSFET's will be discussed in the following sections.

2.1.2 Short Channel Effect and Threshold Voltage

When the channel length is reduced close to the source-substrate or drain-substrate junction depletion region width, a greater part of the channel-depletion region begins to consist of space charge in the junction depletion region (as illustrated in Fig. 2.1). Hence, less gate charge is needed to turn on the inversion in short channel MOSFET's, meaning a lower threshold voltage. This problem is called the *short channel effect*. Two dimensional simulation shows that the surface potential is lowered in a short channel MOSFET due to

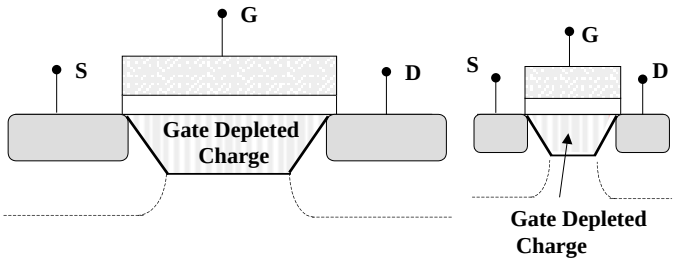


Figure 2.1: Illustration of the charge sharing between the channel and source/drain, which leads to a reduction of the threshold voltage in short channel MOSFET's.

the influence of lateral electrical field from source and drain [27].

The dependence of threshold voltage on channel length is undesirable from a manufacturing point of view. First, if MOSFET's with different channel lengths are designed on a single chip, then the threshold voltage for these devices will be different. Second, for a designed channel length, process variations will induce the variation of effective channel length, resulting in a shift of threshold voltage and inconsistencies in circuit performance.

Beside the dependence on the channel length, threshold voltage is also dependent on the drain bias for short channel MOSFET's. Because the depletion width near the drain increases with the drain bias, the threshold voltage decreases when the drain bias increases for a fixed channel length. This phenomenon is called *drain induced barrier lowering* (DIBL). Two dimensional simulation shows that the surface potential is further lowered at a higher drain bias [27].

In general, subthreshold current exponentially depends on the surface potential and thus on the gate voltage in the following manner:

$$I_{sub} \sim \exp(\frac{q\varphi_{surf}^{source}}{kT}) \tag{2.2}$$

$$\sim \exp[\frac{q(V_G - V_T)}{nkT}], \tag{2.3}$$

$$n = (1 + \frac{C_{dep} + C_{int} + C_{parastic}}{C_{ox}}) \tag{2.4}$$

where C_{ox}, C_{dep}, C_{int}, and $C_{parasitic}$ are the capacitance from the gate oxide, channel depletion region, gate oxide interface density, and parasitic capacitance. The speed to turn on and off a MOSFET is represented by the subthreshold slope (S_t):

$$S_t = \frac{\Delta V_{DS}}{\Delta(\log I_{DS})} = 2.3\frac{kT}{q}n \tag{2.5}$$

For long channel MOSFET's, $C_{parasitic}$ is negligible and S_t is independent of channel length and drain voltage.

The short channel effect (surface barrier lowering) and the DIBL effect lower the threshold voltage and thus increase subthreshold current (from Eqn. 2.3). For short channel MOSFET's, the capacitance coupling between the source and drain depletion region and the

channel depletion region cannot be ignored and may be modeled as an additional parasitic capacitance. Therefore, the subthreshold slope also degrades for short channel MOSFET's [28]. The increase of the subthreshold current will increase the standby power consumption ($P_S = I_{leak} * V_{DD}$) for logic devices and may cause the loss of stored data in memory devices. This is also the reason that while CMOS linear dimensions are scaling aggressively, threshold voltage has not been scaled accordingly. For example, to achieve 10^6 current on/off ratio, a threshold voltage of 0.4V is required, assuming a 70mV/decade subthreshold slope (at 25^oC).

2.1.3 Punch-through (subsurface DIBL) Problem

For a given channel doping concentration, as the channel length is reduced, the sum of the source and drain depletion widths may be larger than the channel length. In this case, the majority carriers in the source region can be injected into the depleted channel region, swept by the lateral electric field and collected by the drain. It is called that the device is operating under the *punch-through* condition. The total drain current will be dominated by the space-charge-limited current, which is proportional to $\sim V_{DS}^2$ [29].

For long channel MOSFET's, avalanche breakdown at the drain junction often appears earlier than the punch-through. However for sub-100nm MOSFET's, punch-through may exist even when the V_{DS} is very low. Because the surface-channel region is usually doped for threshold adjustment, punch-through often happens in the lightly doped region below the surface channel, and thus also called *subsurface DIBL*.

Punch-through also affects the device subthreshold characteristics. As discussed in the previous section, the DIBL effect lowers threshold voltage and thus increases subthreshold current. The finite slope on the plot of log I_{DS} vs. V_{DS} illustrates the DIBL effect (Fig. 2.2). For short channel MOSFET's, when the gate bias is below the threshold voltage, the subthreshold current increases with drain voltage more than that expected for surface DIBL. In addition, at a high drain bias, the drain current is completely beyond the gate control, as shown in Fig. 2.2. This degraded subthreshold current is a measure for the on-set of punch-through.

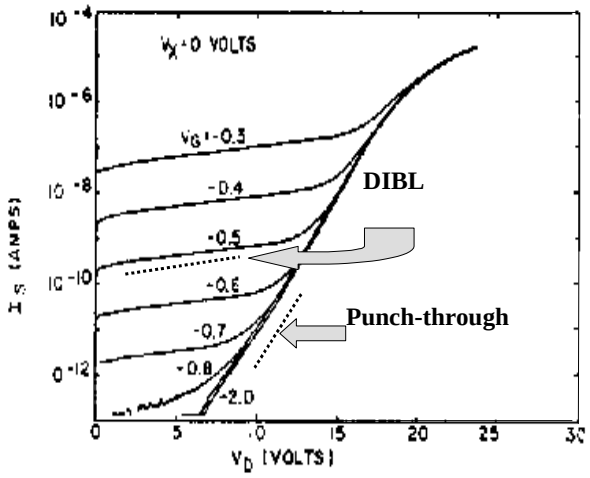


Figure 2.2: Experimental I_{DS} ~V_{DS} characteristics for a MOSFET with L=2.1μm. At high V_{DS}, a subsurface punch-through current flows which is independent of V_{GS} (after [30]).

2.1.4 Effects of Random Doping Distribution

The effects of discrete random dopants become more and more important as the channel length and width are scaled down. The number of dopants in the channel is on the order of hundreds in sub-100nm regime; assuming the channel doping is 10^{18}cm^{-3}, the number of dopant atoms in the depletion region (~30nm wide) of a device with L=100nm and W=100nm is only ~300. The fluctuation of dopant atoms and the variation of their locations will result in variation of the threshold voltage, subthreshold slope, drive current, and so on [24, 31, 32, 33, 34, 35, 36, 37]. To minimize the dopant fluctuation effect, the influence of depletion region charge on the threshold voltage must be reduced. This has been accomplished by either reducing the gate oxide thickness or decreasing the doping level. However, decreasing the doping level is a difficult task in the current CMOS technology as lower channel doping induces more pronounced short channel effects.

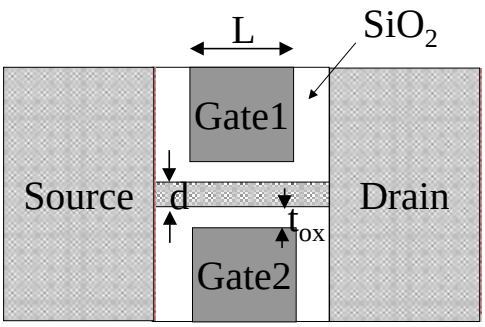


Figure 2.3: Schematic of a double-gate MOSFET (DG-MOSFET).

2.2 Characteristics of Double-Gate MOSFET's

In order to improve device performance in the sub-100nm regime, numerous novel device structures have been reported in the literature. The most widely studied devices included SiGe MOSFET's [4, 5, 6], low-temperature CMOS [15, 38, 39, 40], partially-depleted and fully-depleted SOI MOSFET's, dynamic-threshold MOSFET's [41, 42] and double-gate MOSFET's (DG-MOSFET's). DG-MOSFET's have been shown by various device simulations [43, 44, 45, 46] and analytical calculations [19, 47, 48, 49, 50, 51, 52, 53] to be the best candidate for CMOS devices scaled beyond the 100nm regime. Monte Carlo simulation by Frank *et al.* [43] predicted continuous improvement in device performance down to 20∼30nm gate length, provided silicon channel thickness is of 10-25nm and gate oxide thickness is of 2∼3nm.

2.2.1 Advantages of Double-Gate MOSFET's

The double-gate MOSFET (Fig. 2.3) consists a very thin silicon channel, with two connected gates on each side of the channel. The vertical electric fields from the two gates are coupled with each other. There are five advantages to the design of the double-gate structure.

First, the two gates very effectively terminate the drain field lines. Consequently the threshold voltage roll-off due to the short channel and DIBL effects are suppressed.

Second, the punch-through problem is also suppressed. In the middle of the silicon layer

the potential is close to the surface potential, which is well-control by the two gates.

Third, the DG-MOSFET has near ideal subthreshold slope at long channel length. Once the silicon layer is fully depleted, any increase of gate voltage will not increase the depletion charge, resulting in $C_{dep} = 0$ in Eqn. 2.4 and Eqn. 2.5. At a short channel length, $C_{parasitic}$ induced by the drain bias is also smaller in DG-MOSFET's due to the increased gate control.

Forth, the dopant fluctuation in a short channel MOSFET can be avoided by using an undoped channel, which will not induce the punch-through problem due to the double-gate structure.

Fifth, both gates are strongly coupled with the channel, increasing the transconductance. After the silicon layer is fully depleted, the increase of gate voltage will sharply raise the surface potential and increase electron concentration in the inversion layer. Moreover, the current drive doubles per device layout width.

2.2.2 MEDICI Simulation of Double-Gate MOSFET's

At a long channel length when the thin silicon channel is fully depleted, the threshold voltage of a double-gate MOSFET can be simply expressed as [19, 45]:

$$V_{th}^{DG} = V_{FB} + 2\phi_f + \frac{qN_a}{C_{ox}}\frac{d}{2} \tag{2.6}$$

where $\phi_f = \frac{kT}{a} \ln \frac{N_a}{n_i}$, N_a is the channel doping level, ϵ_{Si} is the permittivity of silicon, and V_{FB} is the flat band voltage. Therefore variation of channel thickness may cause variation of the threshold voltage.

For the case of a short channel double-gate MOSFET, the two-dimensional Poisson's equation must be solved. To fully understand the device characteristics of the double-gate MOSFET's, two-dimensional device simulations have been executed in this work with the help of the MEDICI program [54].

Threshold Voltages and the Channel Thickness Effect

Fig. 2.4a indicates the effect of the channel thickness on the threshold voltage of n-channel double-gate MOSFET's as predicated by MEDICI simulation. For a channel length

of 50nm, channel doping (n-type, unintentional) at 10^{15}cm^{-3}, and a gate oxide of 20Å, variation of the channel thickness causes a shift of threshold voltage with $\frac{\partial V_{th}^{DG}}{\partial d} \approx 3.3$mV/nm. Here an n-type poly-silicon was chosen as the gate material and the threshold voltage is defined by the linear interpolation of I_{DS} vs. V_{GS}. A uniform channel thickness is thus important for a double-gate MOSFET. Furthermore, when the channel thickness is reduced to less than 5nm, quantum shifts will cause threshold voltage to vary by the square of the silicon thickness [46].

As mentioned above, the channels of double-gate MOSFET's are not intentionally doped in the simulation ($\phi_f \approx 0$) to avoid dopant fluctuation. The threshold voltage cannot be adjusted in the same way as conventional CMOS. To obtain suitable threshold voltages for logic p- and n-channel FET's at a low supply voltage, gate material with a mid-gap work function (V_{FB}=0) is needed. Polysilicon/TiN stacked gate designs have been reported [55]. Inverse dual-poly gate, i.e. p^+poly for NMOS and n^+ for PMOS, can also provide symmetrical V_{th}. Recently, it has been reported that the threshold voltage may also be adjusted by using alloyed semiconductors as the gate material, such as $Si_{1-x}Ge_x$ [1, 2, 3].

Short Channel Effect and DIBL Effect on DG-MOSFET's

In Sec. 2.1.2, the short channel effect of conventional MOSFET's was discussed. For double-gate MOSFET's with ultra-thin channel thicknesses, the threshold voltage roll-off is significantly reduced. Fig. 2.5a gives the threshold voltage at various channel lengths for DG-MOSFET's with channel thicknesses of 20nm and 50nm. The channel doping levels of these n-channel devices are chosen as background doping levels (1×10^{15}cm^{-3}). The gate oxide for all devices is 20Å. n^+ poly-silicon is the gate material. For a 50nm thick channel, the threshold voltage starts to roll-off at a channel length of 80nm. The short-channel effect is improved at a thinner channel thickness. For a 20nm thick channel, the roll-off point of the threshold voltage is at L=50nm.

The Double-gate MOSFET also has DIBL immunity if the channel thickness is sufficiently thin. Fig. 2.4b illustrates the DIBL effect (threshold voltage shift at drain bias of 0.1V and 2.0V) by MEDICI simulation. The channel length is 50nm and gate oxide is 20Å.

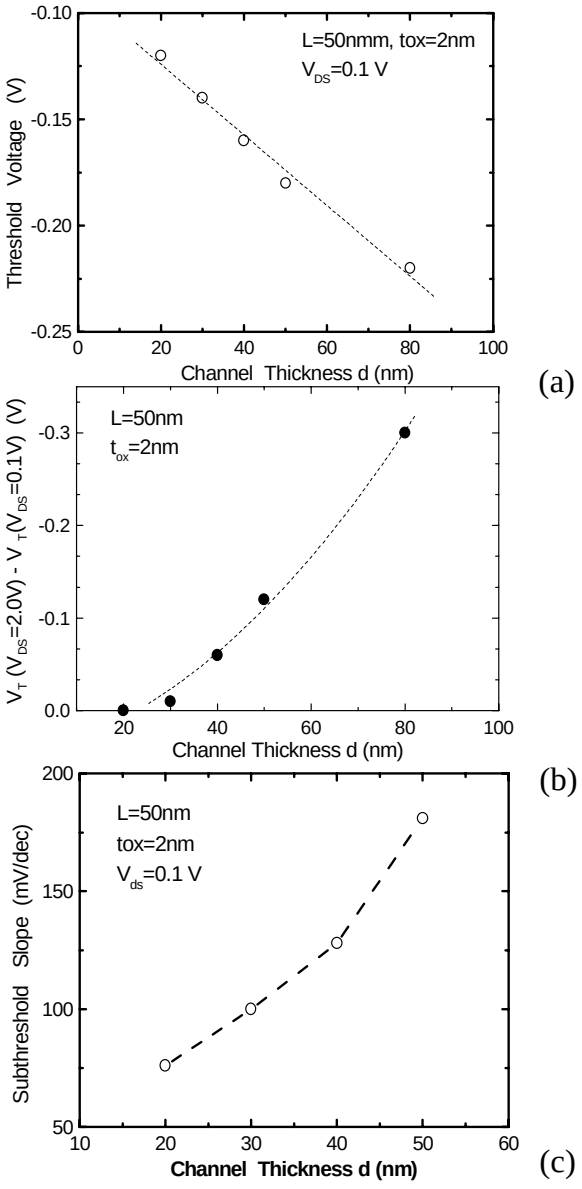


Figure 2.4: Effect of channel thickness on the (a) threshold voltage, (b) drain-induced barrier lowering (DIBL) and (c) subthreshold slope of the double-gate MOSFET's predicated by MEDICI simulation. All the characteristics are calculated at room temperature.

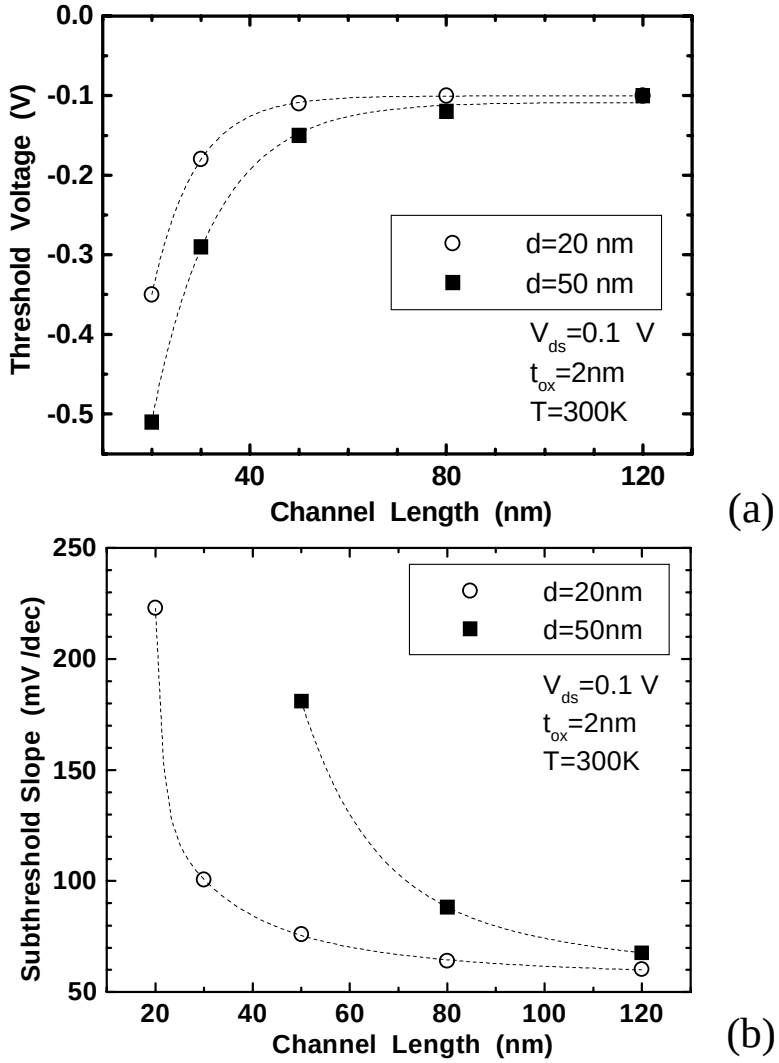


Figure 2.5: (a) Threshold voltage and (b) subthreshold slope for double-gate MOSFET's with various channel lengths and thicknesses, predicated by 2-D MEDICI simulation.

Notice that the DIBL effect decreases when the channel thickness decreases. For $d \leq$30nm, DIBL effect becomes negligible.

Subthreshold Slope of DG-MOSFET's

The subthreshold slope of a double-gate MOSFET with a long channel length is near ideal once the channel is fully-depleted. At short channel length, due to subsurface DIBL effect, the subthreshold slope of a DG-MOSFET also increases, as shown in Fig. 2.5b. However, the increasing rate is slower for thinner silicon thickness. With a 20Å gate oxide, to obtain reasonable subthreshold behavior for a DG-MOSFET with sub-100nm channel length, the silicon thickness has to be less than 50nm. The channel thickness effect on the subthreshold slopes is plotted in Fig. 2.4c for a 50nm channel length and a 20Å gate oxide. Thinner channel thickness leads to reduced subthreshold slope. When $d \leq$20nm, near ideal subthreshold slope may be achieved. In general, to have good gate control, the channel thickness d needs to satisfy $d \leq L/4$ [56].

Projection for Sub-100nm DG-MOSFET's

In summary, the double-gate structure with an ultra-thin channel thickness will provide better device performance for sub-100nm MOSFET's. With the help of MEDICI simulations, it was found that for a channel length of 50nm and for an unintentionally doped channel (1×10^{15}cm^{-3}), the gate oxide thickness and channel thickness should be at most 20Å and 20nm, respectively.

Fig. 2.6a gives the drain current and voltage characteristics of a device of the above proposed structure. The on region is well-behaved, with a record-to-be transconductance of 1350mS/mm. The subthreshold of the same device is plotted in Fig. 2.6b, with a slope of 76mV/decade at room temperature.

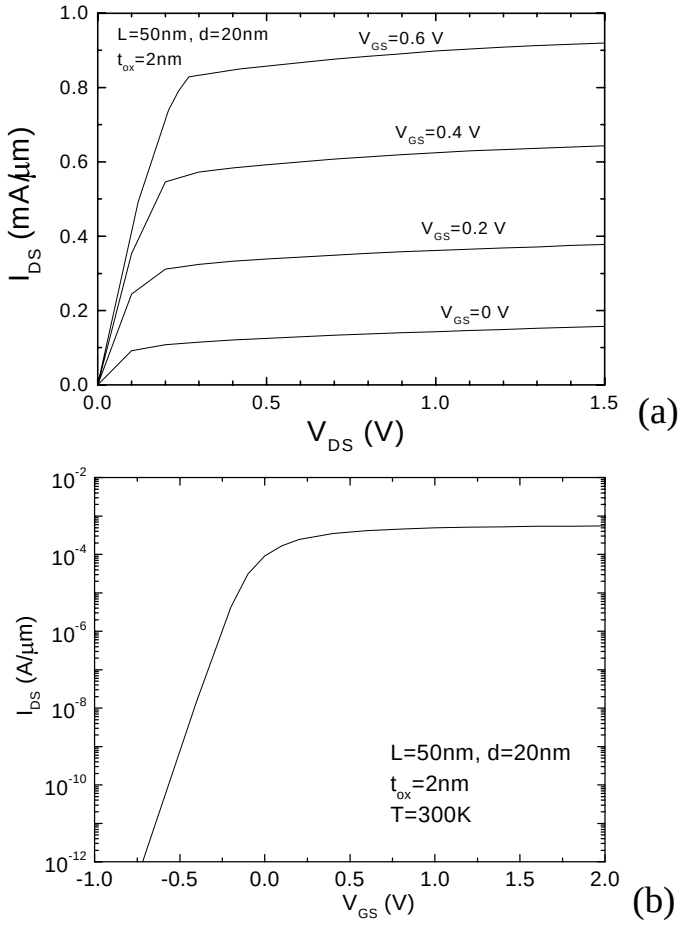


Figure 2.6: (a) Drain current and drain voltage, (b) subthreshold slope of a double-gate MOSFET simulated by MEDICI at room temperature. The channel length is 50nm, channel thickness 20nm, and gate oxide thickness 20Å. The transconductance of this n-channel FET reaches 1350mS/mm, and the subthreshold slope is 76mV/decade.

2.3 Fabrication Approaches for Double-Gate MOSFET's

Simulation and calculation results in the previous section have shown that double-gate MOSFET's can provide adequate short-channel immunity for channel lengths as low as 25nm. However, fabrication of double-gate MOSFET's is not simple, as the "ideal" double-gate MOSFET should have:

1. a well-controlled channel length L with minimum process fluctuation
2. a uniform, thin (10∼25nm) silicon channel (d), with $d \leq$L/4
3. high quality, thin gate oxide (2∼3nm)
4. a thick source/drain contact to reduce series resistance
5. gates perfectly aligned to each other and to the source/drain to reduce parasitic capacitance.

To date, there have been several double-gate MOSFET designs proposed. Fig. 2.7 shows the three possible orientations of a double-gate MOSFET on a silicon wafer in terms of the current-carrying plane. For a planar configuration (Fig. 2.7a), current is carried in the plane of silicon substrate, as is the case with conventional MOSFET's. The two gates are located on top and bottom of the channel. In this configuration, double-gate SOI MOSFET's [57, 58, 59, 60, 45], Gate-All-Around and Wrap-Around-Gate SOI MOSFET's [61, 62] and self-aligned thin channel MOSFET's [56] have been reported. In the second configuration in Fig. 2.7b, the current direction is perpendicular to the substrate. The source/drain regions are on the top or bottom of a pillar structure with the two gates on the side wall of the pillar. Reported devices in this configuration are vertical surrounding gate/double-gate MOSFET's, as are devices presented in this thesis. The DELTA device demonstrated by Hisamoto *et al.* [63] is an example of Fig. 2.7c. As with vertical MOSFET's, the two gates of these devices are also on the side walls of the pillar structures. However, the current direction is in the substrate plane. A comparative study of these advanced device structures will be discussed in this section.

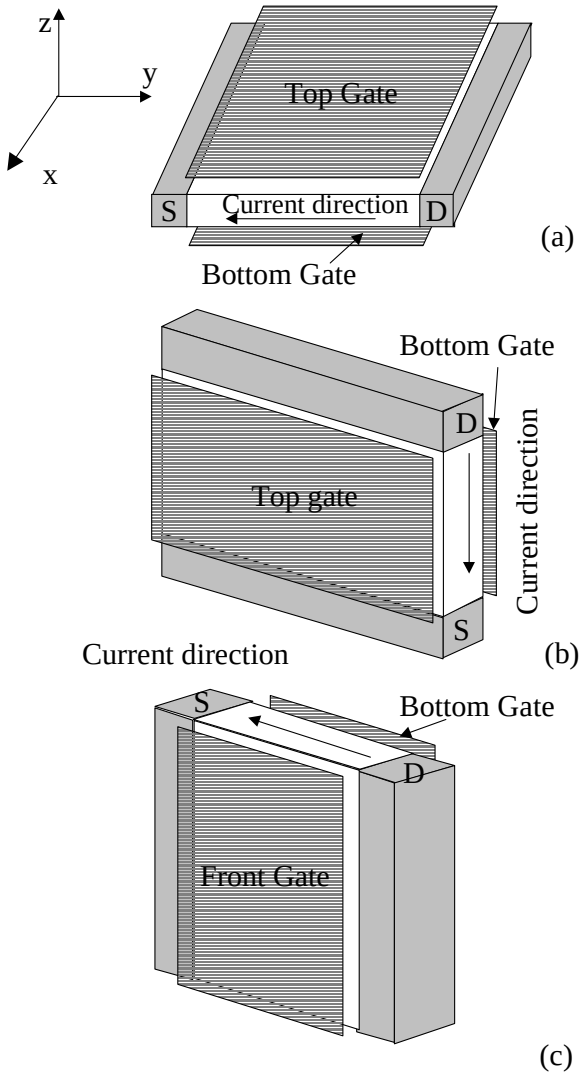


Figure 2.7: Possible orientations of a double-gate MOSFET on a silicon wafer: (a)planar, (b)vertical pillar, (c)vertical DELTA (after [56]).

2.3.1 Planar Double-Gate MOSFET's

The channel length of a planar double-gate MOSFET is defined by lithography. Most of the planar double-gate MOSFET's which have been reported are fabricated on Silicon-On-Insulator (SOI) wafers or other SOI structures.

(I) Double-Gate SOI MOSFET

A double-gate SOI MOSFET is fabricated on an SOI structure by adding bottom gate oxide and gate poly prior to either the wafer bonding or the selective epitaxy of silicon [45, 57, 58, 59, 60]. Fig. 2.8 gives the process flow by using wafer-bonding [58]. First the back-gate oxide and the poly-Si back gate is formed, followed by a CVD SiO_2 deposition. After bonded with a base wafer covered with BPSG, the wafer is flipped over and the top silicon is etched back to give the thin silicon channel. The top gate oxide and poly-gate are then formed, followed by source/drain implantation.

The channel (silicon) thickness of a double-gate SOI MOSFET is often determined by chemical-mechanical polishing after SOI formation. However, the fabrication of the bottom thin gate oxide and the alignment of the front and the back gates are very difficult. Because the back gate oxide is formed before the wafer binding or epitaxy, its quality is affected by the high temperature processes involved later. Also misaligned top and bottom gates will result in extra capacitance and loss of current drive. Wong *et al.* [64] pointed out that 25% misalignment causes a 33% increase in delay.

(II) Self-aligned Double-Gate SOI MOSFET

Wong *et al.* demonstrated a planar double-gate SOI MOSFET with self-aligned top and bottom gates using constrained selective lateral overgrowth to form a free-standing, suspended silicon bridge, shown in Fig. 2.9 [56]. The silicon bridge is the MOSFET channel. Gate oxide and poly-Si are then conformally grown around the bridge to complete the self-aligned process. In this design, the channel thickness is defined by a sacrificial amorphous Si layer, which can have excellent uniformity and can be controlled to be very thin. 25nm

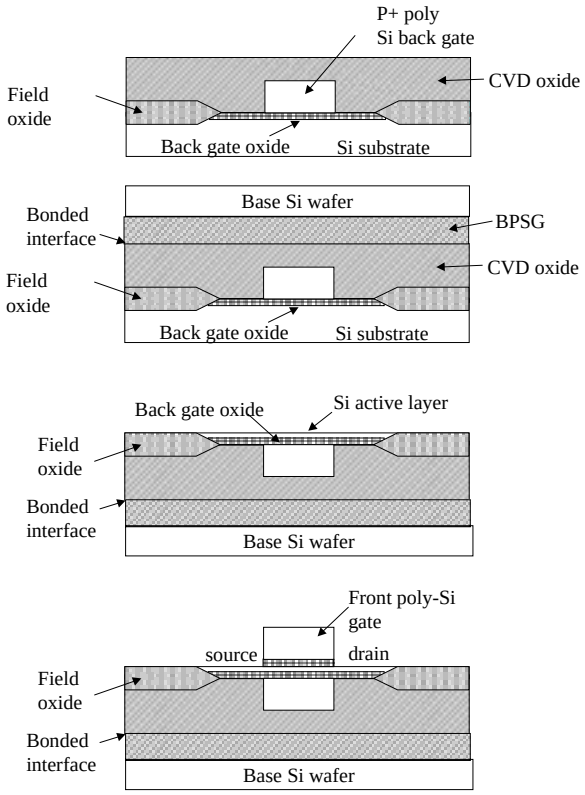


Figure 2.8: Typical process flows for a double-gate SOI MOSFET using wafer bonding (after [58]).

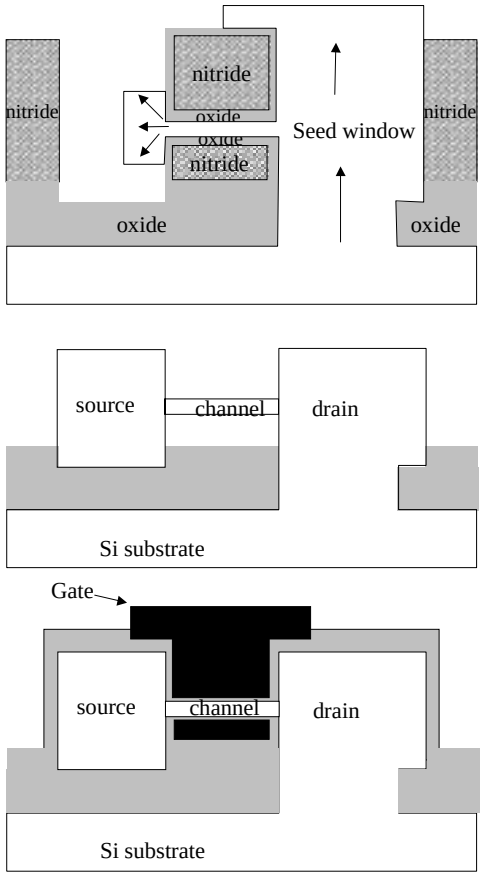


Figure 2.9: Process flow of a self-aligned double-gate SOI MOSFET (after [56]).

thickness has been demonstrated, but the structure is mechanically vulnerable and there is significant overlap capacitance between the gate and source/drain.

(III) Gate-All-Around and Wrap-Around-Gate MOSFET's

In 1990, Colinge *et al.* demonstrated the "Gate-All-Around" MOSFET with the gate oxide and gate electrode not only on top and bottom of the active silicon film but also on the side walls [61]. The key process and structure are shown in Fig. 2.10. Starting from a commercial SIMOX substrate, an active silicon area is first defined, followed by a buffered HF immersion to create a cavity underneath the central part of the silicon island. After gate oxidation, gate polysilicon is conformally grown to cover all surfaces of the exposed

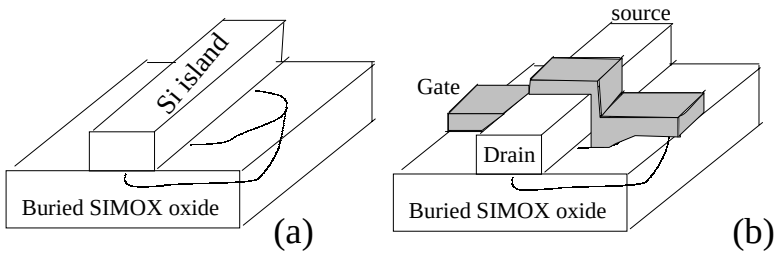


Figure 2.10: (a) Cavity etch underneath the silicon island. (b) Completed "Gate-All-Around" SOI MOSFET (after [61]).

island and subsequently heavily doped with phosphorus by ion implantation. The gate is patterned by lithography and reactive ion etching (RIE). The source and drain are formed by implantation. In this process, high quality gate oxide is grown on both the front and back sides of the device. Leobandung *et al.* reported a similar device with a 70nm channel length, a 35nm channel width, and a 50nm channel thickness [62]. The thin wire-channel requires an additional E-beam lithography step in addition to the one for the channel length. This Gate-All-Around structure requires the undercut of the silicon by wet-etch, which is very difficult. Backside gate patterning and its alignment with the front gate and source/drain is also very challenging.

2.3.2 DELTA Structure

To have better control of the back gate and to simplify the process for ultra-thin SOI film in the planar SOI structures, Hisamoto *et al.* developed a vertical ultra-thin-SOI device with a fully-depleted lean-channel transistor (DELTA) [63]. A Si island is created by RIE and the bulk SOI is formed by selective oxidation, shown in Fig. 2.11. Following gate oxidation and polysilicon deposition, the top and side of the lean channel is wrapped by the polysilicon gate. After another lithography and RIE to pattern the gate, the source and drain are implanted, using the gate-poly as a self-aligned mask. This three-dimensional structure enables the self-alignment between the two gates and source/drain, reducing the overlap capacitance. Furthermore, it has the highest packing density because the transistor width, the longest dimension, is perpendicular to the plane. However, to fabricate devices

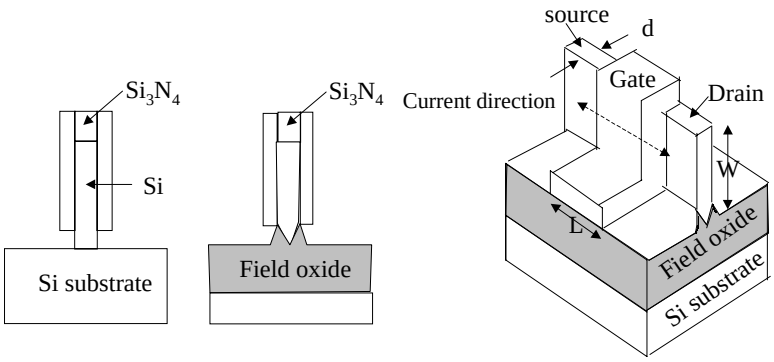


Figure 2.11: Process flow and schematic cross-section of "DELTA" structure (after [63]).

with sub-100nm channel length and fully depleted channel, two E-beam lithography and RIE steps are required to define the thickness of the silicon island and the poly-silicon length. This results in the variation of both of the critical dimensions due to process fluctuations. Also lithography for the high aspect ratio structure requires large depth of focus for the material along the sidewalls.

2.3.3 Vertical Double-Gate MOSFET's

Vertical surrounding-gate or double-gate MOSFET's have been proposed by many groups. The schematic structure is shown in Fig. 2.12. This is the second orientation configuration discussed in Fig. 2.7. The channel is a vertical silicon pillar and the gate materials are on the side walls. The source and drain are on the top and bottom of the pillar. For a fully depleted double-gate or surrounding-gate MOSFET, the pillar thickness d is very small and is defined by E-beam lithography.

Compared with other structures for double-gate MOSFET's, vertical MOSFET's provide distinctive advantages; First, the channel lengths may be determined by epitaxy rather than lithography resolution. Second, the source/drain may be designed to self-align to the gate. The problem of misalignment of the front and back gate of planar double-gate SOI does not exist here. Third, the packing density of the vertical structure in some cases can be much higher than the conventional lateral devices. For example, Takato *et al.* reported that a CMOS inverter can be shrunk to 50% of that using planar transistors [65].

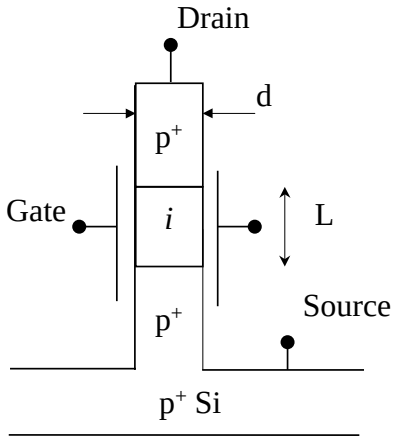


Figure 2.12: Schematic of a vertical double-gate MOSFET.

There are two ways to fabricate vertical double-gate MOSFET's, depending on how the channel length is determined. One approach is to use RIE to define the channel length, shown in Fig. 2.13. The silicon pillar is created on a silicon substrate by RIE, followed by gate oxidation and gate poly-silicon deposition. The poly-silicon is then etched back using anisotropic RIE, with the height of the poly-silicon determining the channel length. Tilted implantation is performed using the poly-silicon as a self-aligned mask for source and drain doping. In 1985, the first vertical transistor proposed for DRAM by Texas Instruments was fabricated in this way [66]. Vertical transistors on a wide mesa have been widely studied since then [65, 67, 68, 69, 70]. Recently double-gate fully depleted vertical transistors have also been reported by Zheng *et al.* [71] with L=0.3μm, d=80nm and Auth *et al.* [72] with L=0.6μm and $d \leq$70nm. This approach provides a self-aligned source/drain with the side gates. However, the RIE rate is difficult to control, thus using RIE of the poly-silicon gate to define the channel length will lead to device performance strongly dependent on process fluctuations. Perhaps for this reason, vertical double-gate MOSFET's with channel lengths down to sub-100nm have not been demonstrated using this method.

In a second approach to fabricate vertical double-gate MOSFET's, silicon epitaxy is used to grow the vertical structure (source, channel and drain). This enables the channel length of the MOSFET to be defined by the epitaxial layer thickness rather than by lithography or

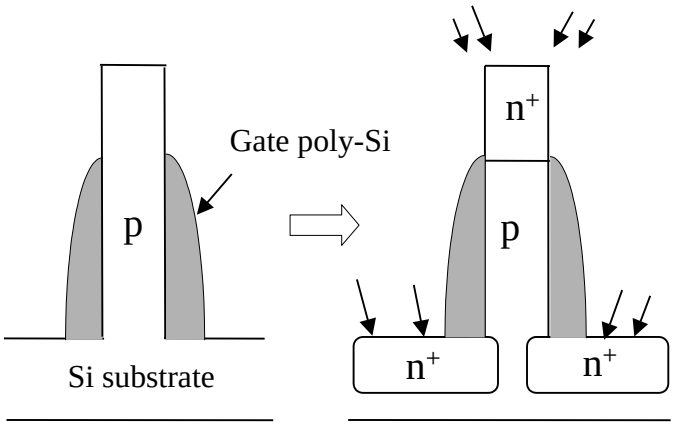


Figure 2.13: Schematic of vertical double-gate MOSFET's using RIE to define the channel length.

RIE. Today's epitaxy technology, either molecular beam epitaxy (MBE) or chemical vapor deposition (CVD), is very mature and can control the epitaxial layer thickness to a few tenths of a nanometer. As such, this technique is attractive for use in the development of sub-100nm vertical MOSFET's. By using epitaxy, it is also very easy to tailor the vertical doping profile in the channel and form a lightly-doped drain (LDD) region. This is currently formed by the low-energy implantation and careful spacer technology in conventional lateral structures. Using epitaxy, LDD regions and doping levels can be controlled precisely in vertical MOSFET's. It is also possible to engineer the bandgap or strain of the channel and source/drain by introducing $Si_{1-x}Ge_x$ alloy. Vertical MOSFET's on a wide mesa using epitaxial channel have also been widely studied [73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86]. However, a fully-depleted channel on an ultra-thin pillar has not been reported thus far.

In this thesis, vertical double-gate MOSFET's using epitaxy to define the channel length are proposed. The process design will be discussed in Chapter 3. Note that in all the vertical structures discussed in this chapter, independent of whether the gate length is defined by RIE or epitaxy, gate oxidation and/or high temperature annealing is performed after implantation or epitaxy. The control of the doping profiles after pillar formation is a critical problem. Diffusion of source/drain dopant during gate oxidation or annealing

after implantation is greatly enhanced by the oxidation enhanced diffusion and transient enhanced diffusion effects. The major contribution of this thesis is in overcoming these effects to achieve vertical p-channel MOSFET's with the shortest channel length to date.

2.4 Double-Gate vs. Surrounding-Gate MOSFET's

Studies show that surrounding-gate MOSFET's with ultra-thin cylindrical structures provide stronger electrostatic confinement from the gate than that from double-gate structure [87, 88], where for comparison the silicon channel thickness d and the cylinder diameter are the same. The enhanced confinement allows the surrounding-gate structure to be scaled about 50% smaller than the double-gate. This advantage has been predicted previously by Leobandung *et al.* [62], Auth *et al* [72], and Zheng *et al.* [71]. The three-dimensional gate control may also relax the thickness requirement on silicon pillar ($d \leq L/4$ for double-gate) for a given channel length. Vertical surrounding-gate MOSFET's possess the dual advantage of having both a vertical structure and a surrounding gate. Slight process changes in the fabrication of vertical double-gate devices allow for the fabrication of vertical surrounding gate MOSFET's. The process modifications will be discussed in Chapter 3.

2.5 Potential Applications of Vertical MOSFET's in Memories and Stacked FET's

While double-gate MOSFET's have been widely studied for their potential applications in logic circuits (by virtue of their high drive current and fast speed at short-channel length), vertical MOSFET's have been of specific interest in the memory devices (due to high packing density and low cost). The scaling of the lateral dimensions and the introduction of trench and stacked capacitors have led to dramatic reductions in Dynamic Random Access Memory (DRAM) cell size. The conventional DRAM cell, which consists of a "planar" MOSFET and a capacitor, has already been minimized to it structural limit, $8F^2$, where F is the minimum feature size. Fig. 2.14 indicates that the $8F^2$ cell cannot maintain the trend

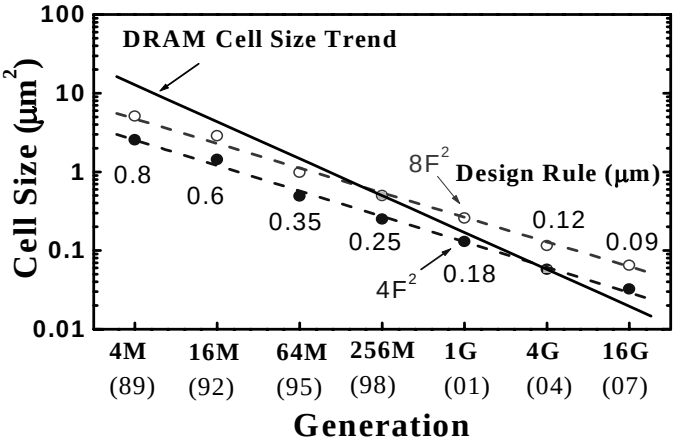


Figure 2.14: DRAM cell size trend, after Maeda *et al.* [89].

beyond 256Mbit. Using vertical transistors, the $4F^2$ cell size may be realized. On the other hand, scaling of the lateral size has made it very difficult to maintain an acceptable level of off-current. Therefore decoupling of the gate length from the cell scaling dimension is necessary. Because of the benefits discussed above, the vertical transistor has been proposed for the forthcoming 1Gb/chip generation of DRAM by some manufacturers.

The vertical transistor used in DRAM is either a pillar structure, such as the surrounding gate [89, 90, 91, 92, 67, 93, 68, 94], or a trench transistor as reported in Ref.[66, 95, 96]. Vertical transistors have also been used to fabricate ROM [97] and Flash EPROM. Flash EPROM, similar to DRAM, has been demonstrated on the sidewalls of narrow silicon pillars [98, 99, 100] or trenches [101], with both the floating gate and the control gate aligned in the vertical direction.

To further reduce chip size, it is possible to stack multiple layers of devices on top of each other. Beyond the existing two-dimensional memory array technology, a 3D array of stacked surrounding-gate transistor DRAM has been proposed by Endoh *et al.* [102, 103]. Nemati *et al.* reported a novel SRAM cell with only two elements: a vertical surrounding-gated PNPN device on top of the source/drain of a planar pass transistor [104], compared with the conventional 6-transistor or 4-transistor cell. For logical devices, a CMOS inverter made from stacked lateral MOSFET's have been demonstrated by Zingg *et al.* [105], where

a double-gate p-channel device is on top of a single-gate n-channel device, with the gate of the n-FET serving as the bottom gate of the p-FET.

2.6 Summary

The limitations of CMOS scaling down to sub-100nm dimensions have been reviewed. Double-gate MOSFET is a promising novel structure for channel length less than 100nm. The device has improved subthreshold slope, high transconductance, and short-channel effect immunity. A vertical double-gate structure has been proposed for the fabrication. Epitaxy is recommended to grow the vertical pillar so that the channel length will be determined by the epitaxial layer thickness.

Chapter 3

Fabrication of Vertical Double-Gate MOSFET's

3.1 Introduction

Double-gate MOSFET's can reduce short channel effects and improve subthreshold slope when compared with the performance of conventional short-channel MOSFET's. There are several ways to achieve the double-gate structure. In Chapter 2, vertical double-gate MOSFET's have been proposed. In one vertical double-gate MOSFET's fabrication method, the channel length is defined by the epitaxial layer thickness rather than the lithography resolution or reactive ion etching rate (Sec. 2.3.3), enabling the precise control of sub-100nm channel length in principle.

There are two approaches to the fabrication of vertical MOSFET's with channel lengths defined by epitaxy, as shown in Fig. 3.1. These depend on whether the vertical pillar is created by selective epitaxy or by reactive ion etching. In the first approach, the pillar thickness d is defined by the size of the SiO_2 window. The pillar is grown by selective epitaxy through the seed window [86, 106, 80, 79]. In the second approach, the epitaxy is performed on a blank silicon substrate followed by RIE to create a pillar structure [77, 74]. Note that for both of the methods, the channel lengths are defined by the epitaxial layer thickness, and note also that gate oxide and poly-Si are grown after the *in situ* doped epitaxial layers.

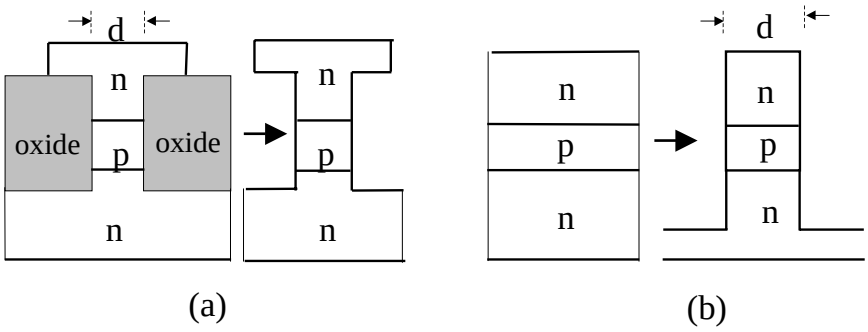


Figure 3.1: Approaches to the fabrication of vertical double-gate MOSFET's with channel lengths defined by epitaxy, by using (a) "selective epitaxy" and (b) RIE after "planar epitaxy", to create the vertical pillar.

This chapter describes the extensive fabrication technologies which have been developed in this work to fabricate vertical double-gate MOSFET's with ultra-thin pillars, using both the "selective epitaxy" and the "planar epitaxy" approaches. In the end, however, only the "planar epitaxy" approach was implemented in the fabrication of vertical short channel MOSFET's (see Chapter 5 for p-channel and Chapter 6 for n-channel). These demonstrated devices are on the side walls of wide mesa, where the two gates are not coupled and the two channels are independent of each other. These devices are fabricated to study the scaling of channel length in the vertical structures. Key technologies, which may be used for general short-channel MOSFET processes, will be presented first in Sec. 3.2. Development of critical technologies for the "planar epitaxy" and "selective epitaxy" approach will be presented in Sec. 3.3 and Sec. 3.4, respectively. The critical process steps developed and characterized for the first time at Princeton University are thin oxide growth on planar and etched silicon surfaces with low thermal budget, profile optimization of SiO_2 and Si dry etching, n^+ and p^+ poly-Si gate deposition, and poly-Si gate anisotropic etching with low gate oxide damage.

3.2 General Silicon Process Technology

3.2.1 Image Reversal During Lithography

Using the "selective epitaxy" approach, vertical silicon pillars are created by optical lithography and reactive ion etching (RIE) of SiO_2, followed by selective epitaxy. The same dark field mask designed for selective epitaxy can be use for the "planar epitaxy" approach. For the latter approach, the silicon pillar RIE is performed by using a negative image of the mask. Photoresist AZ5214 can provide both positive and negative images, depending on the process conditions. 350nm I-line from a mercury lamp is used as the light source of the photo-lithography with an intensity of 20mW/cm^2 on the resist. To obtain a positive image, the regular process is used (same as for AZ1518):

1. Prebake at 110^{o}C on hot plate for 2min to drive out moisture.
2. Spin coat at 5000rpm for 30sec to obtain a uniform thickness of 1.2μm.
3. Soft bake at 105^o $\sim$ 110^{o}C on hot plate for 2min.
4. Pattern exposure for 5$\sim$6 sec
5. Develop typically for 20$\sim$30sec in AZ312 (diluted to 1:1 in deionized water)
6. Hard bake at 110^{o}C on hot plate for 10min.

For a negative image, after pattern exposure and before developing, a hot plate bake at 130^{o}C for 1min followed by a 10sec unmasked exposure is added. The negative image resolution is higher than that for the positive, and the resist can withstand all of the dry and wet etching processes used in this thesis.

3.2.2 Fabrication of Thin Gate Oxide at Low Temperatures

To achieve good gate control over the carrier transport in the channel, the thickness of gate oxide is scaled down to less than 100Å for 0.25μm generation CMOS. The technique of fabrication thin gate oxide (<150Å) with a low thermal budget at Princeton has been

developed here for the first time. Using an "epitaxy" approach to fabricate vertical MOSFET's, the gate oxide is grown after epitaxy and *in situ* doping. As such, lower oxidation temperature and higher oxidation rate is desirable to reduce dopant diffusion. In this section, high quality thin gate oxides grown at ($700^oC \sim 750^oC$) in wet oxygen on planar silicon surfaces are presented.

Fig. 3.2 illustrates the capacitance-voltage measurement from four MOS structures made on these thin gate oxides. The gate oxides were grown on p^- Si (100) substrates after the standard "Silicon Valley" cleaning (H_2O_2:H_2SO_4 /rinse/ diluted HF dip). The gate oxide of samples A and B were grown at 800^oC in dry oxygen for 40min and 20min, respectively. The gate oxide of sample C was grown at 750^oC in wet oxygen for 15min, and that of sample D was grown at 700^oC in wet oxygen for 40min. There was a 5min dry oxidation before and after wet oxidations. All gate oxides were annealed at their oxidation temperature in N_2 for 20min before being unloaded. Al was deposited as the gate material. Postmetallization annealing was performed in the forming gas (N_2 with 10% H_2) at 400^oC for 30min. The high frequency (1MHz) and quasi-static (1V/sec) capacitance-voltage (C-V) measurement technique was used to determine the midgap interface density D_{it} and the effective oxide charge density N_f.

The oxide thickness of each sample is 54, 37, 84 and 73Å, calculated from the capacitance-voltage measurement, in agreement with the results of ellipsometry measurements. D_{it} and N_f on all samples are around $1\times10^{10}cm^{-2}eV^{-1}$ and $1\times10^{11}cm^{-3}$. Fig. 3.3 gives the gate current vs. gate voltage measurement result for the four MOS devices using an HP4145B Semiconductor Parameter Analyzer. For oxide thicknesses greater than 60Å, Fowler-Nordheim tunneling dominates the gate leakage current, as seen in samples A, C, and D. The oxide leakage current is exponentially dependent on the electric field, where the tunneling occurs through a triangle energy barrier. At a lower electric field, where the triangle barrier is not narrow enough, little tunneling occurs. When the oxide is thinner than 40Å, direct tunneling is observed (sample B) at lower electrical field. In Fig. 3.3b, the significant leakage current when the magnitude of gate voltage is less than 3V, results from direct tunneling. The magnitude of the breakdown field for the gate oxides are 16, 15, 16, and 17MV/cm

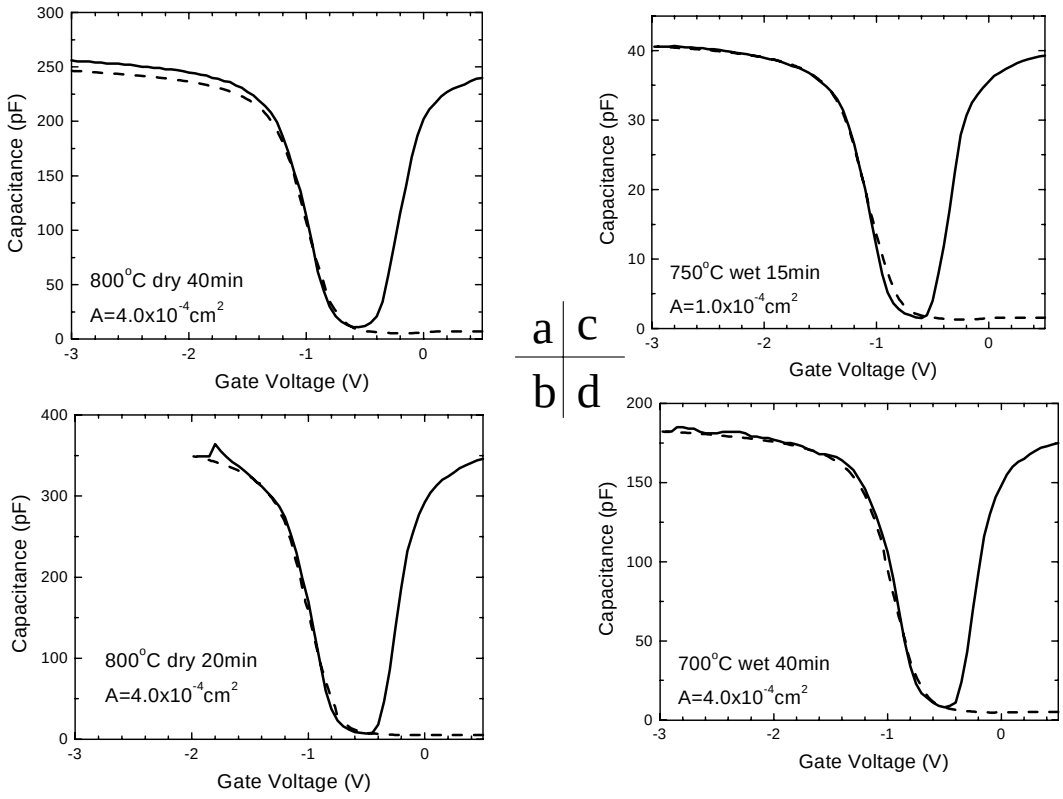


Figure 3.2: Capacitance-voltage measurements from MOS structures on the planar p^- Si (001) substrates, with thin gate oxides fabricated by (a)800^{o}C dry oxidation for 40min, (b)800^{o}C dry oxidation for 20min, (c)750^{o}C wet oxidation for 15min, and (d)700^{o}C wet oxidation for 40min.

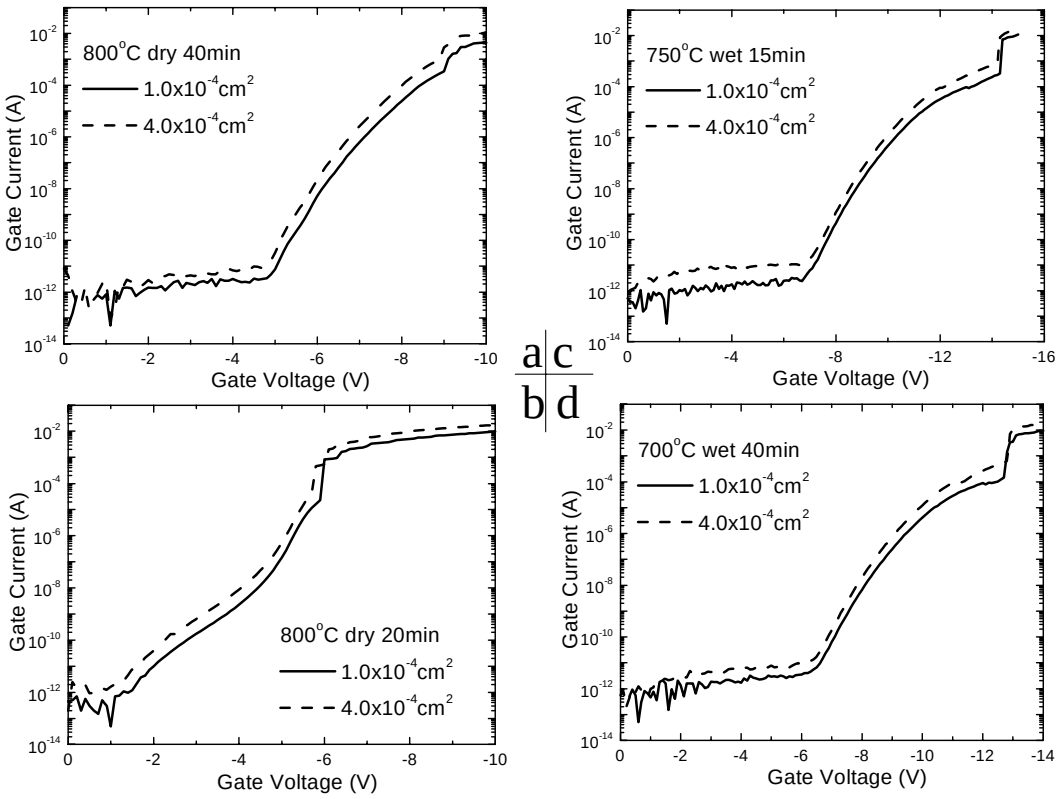


Figure 3.3: Gate leakage current from MOS structures in Fig. 3.2. The breakdown field of each sample is 16, 15, 16, 17MV/cm.

for samples A, B, C, and D, respectively. It shows that the thin gate oxide grown by wet oxidation has a breakdown field at least as high as that by dry oxidation, reducing the overall thermal budget for the vertical MOSFET's processing.

3.2.3 Poly-silicon Gate Deposition

Due to the overhang of the top silicon epitaxial layer using "selective epitaxy" approach (as shown in Fig. 3.1a and will be discussed in Sec. 3.4), a gate electrode deposited by chemical vapor deposition (CVD) is necessary to give a conformal coverage on the sidewall gate oxide under the Si overhang. To provide a highly doped gate near the side wall gate oxide, in-situ doped polysilicon gate has been used for both the "selective epitaxy" and "planar epitaxy" approaches in this work.

After gate oxidation, the wafer was immediately loaded into the RTCVD chamber. For vertical p-channel MOSFET's, ~200nm p^+ polycrystalline silicon was deposited and heavily *in situ* doped with boron at 700^oC using 100sccm silane (diluted to10% in Ar) and 100sccm diborane (120ppm in H_2). The deposition rate is about 66Å/min. Note that without any intentional doping, the poly-Si growth rate is about 50Å/min under the same growth condition. The growth rate enhancement of poly-Si after adding high B_2H_6 flow in SiH_4 has already been reported [107]. A typical p^+ poly-Si deposition sequence is attached in Appendix B. The boron concentration in the polysilicon is $2\times10^{21}cm^{-3}$, measured by the secondary ion mass spectroscopy (SIMS) and the sheet resistance is $10\Omega/\Box$. For n^+ poly-Si, 450sccm PH_3 (100ppm in H_2) was used as phosphorus source, while other growth conditions remained the same as p^+ polysilicon deposition. 200nm n^+-polysilicon gates were used for n-channel MOSFET's with sheet resistance of $160\Omega/\Box$. The deposition rate for the highly phosphorus doped polysilicon at 700^oC is about 40Å/min, less than the undoped poly-Si. The phosphorus doping effect on silicon epitaxy will be discussed in Chapter 4.

To test the gate oxide quality after poly-Si deposition, MOS capacitors with both n^+ and p^+ poly-Si gate and 11nm gate oxides were made on planar (100) p^- Si substrates. The gate oxidation temperature was 900^oC in dry oxygen. The n^+ and p^+ polysilicon layers were deposited under the same conditions as described in the previous paragraph. The

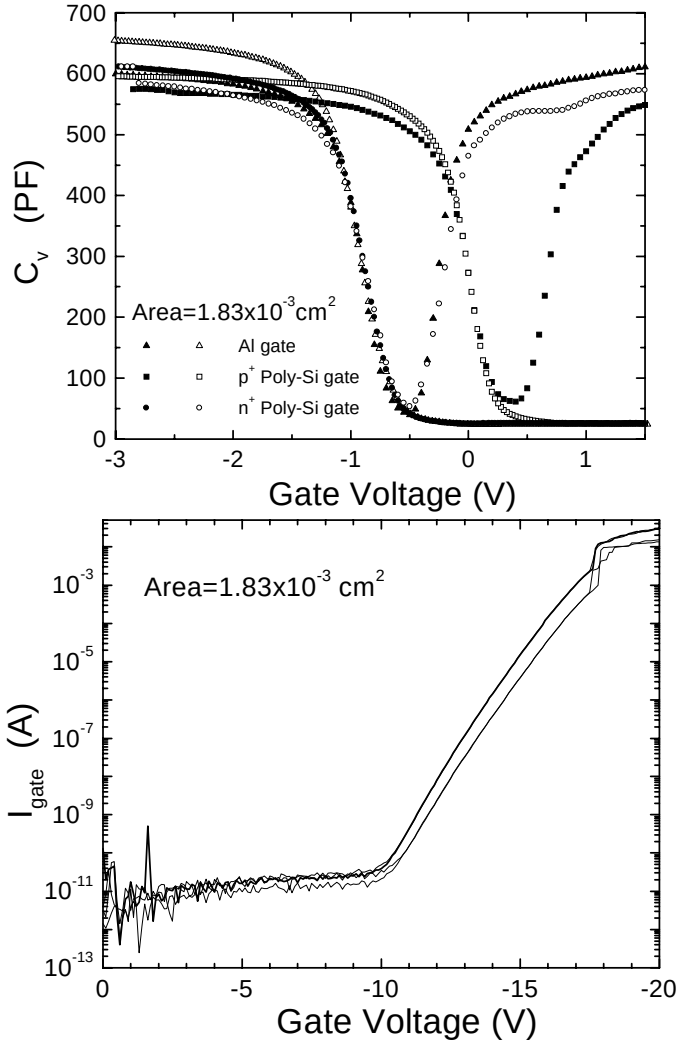


Figure 3.4: (a) Capacitance-voltage measurements from MOS structures on planar p^- Si (001) substrate with wet-etched n^+ and p^+ poly-Si gate, along with that of an Al gate. (b) Gate leakage current from the MOS devices with wet-etched p^+ poly-Si.

front polysilicon gates were patterned in $HF+HNO_3+H_2O$ (6:100:40) using the photoresist masks. The etching rate in this acid mixture for poly-Si is 800nm/min and for thermal SiO_2 25nm/min. Al contacts were evaporated on the front polysilicon and the back side of the silicon wafer (after stripping off the backside oxide and poly-Si). The final annealing was performed at 400^oC in the forming gas for 30min. Fig. 3.4 shows the capacitance-voltage measurement and gate leakage current of these MOS devices with both wet-etched p^+ and n^+ poly-Si gates, along with a reference device with an Al gate. The inversion capacitance from a quasi-static (at 1 V/sec) C-V measurement (Fig. 3.4a) gives the same value of C_{ox} for both p^+ and n^+ poly-Si gated MOS structures, indicating no gate depletion is observed [108]. The interface density at the mid-gap of the MOS with poly-Si gate is similar to that of the reference sample with an Al gate . The threshold voltage difference between the devices with p^+ poly-Si and n^+ poly-Si is 0.9V, corresponding to the Fermi-level difference due to the doping. Fig. 3.4b shows gate current vs. gate voltage in the accumulation bias regime from the MOS with p^+ poly-Si. Compared with the control device with an Al gate, no gate oxide degradation is found due to polysilicon deposition or wet etching. The breakdown field is larger than 13MV/cm.

3.2.4 Reducing Plasma Damage on the Thin Gate Oxide During Plasma Processing

(I) Reducing the Damage on the Thin Gate Oxide During Poly-Si Gate RIE

When this thesis work began, there was no well-developed process for MOS structures with a dry-etched poly-Si gate on a thin gate oxide (<200Å) at Princeton. Fig. 3.5 shows the typical gate current vs. gate voltage curve for MOS devices on a p^- Si substrate, with p^+ poly-Si gates patterned by an early RIE process. The gate oxides and polysilicon deposition conditions were the same as those in Fig. 3.4. The poly-Si gate etching here is carried out in 42.5sccm CF_4 and 7.5sccm O_2 at 200mtorr. The RF power density is $0.04watt/cm^2$. In contrast to those using wet-etched poly-Si gate in Fig. 3.4b, some MOS devices have already exhibited breakdown at a very low bias. The statistical summary of gate oxide breakdown

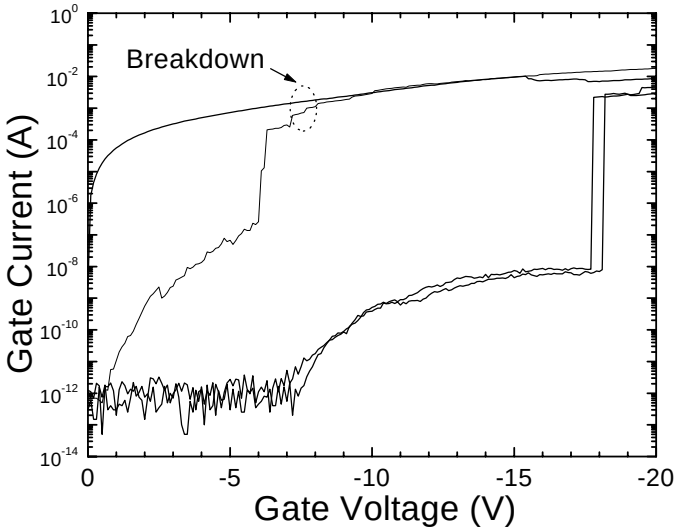


Figure 3.5: Typical gate leakage current from MOS structures on a p^- Si (001) substrate with p^+ poly-Si etched by 42.5sccm CF_4 and 7.5sccm O_2 at 200mtorr and 0.04watt/cm^2.

field after poly-Si gate RIE is given in Fig. 3.6a. 50% of the devices have already exhibited breakdown, 40% breakdown at 10MV/cm, and 10% fail in between.

Various gas mixtures and RF power were studied for poly-Si gate etching. The results are listed in Table 3.1. 11nm gate oxide was grown at 900^{o}C in dry oxygen on p^- Si substrate, followed by 150nm of p^+ polysilicon deposition at 700^{o}C from SiH_4 and B_2H_6. Photoresist was used as a poly-Si etching mask, unless otherwise noted. Al contacts on the front and back of the sample was then deposited and wet-etched. 400^{o}C forming gas annealing for 30min was performed before capacitance-voltage measurement to achieve better interface properties. It should be noted that this annealing has no effect on the current-voltage characteristics of the devices in this work. The structure shown in Fig. 3.7a has been used for all the MOS test in this section unless noted. For this structure, there is no field oxide or insulation layer before the gate oxidation. This test structure is very similar to the vertical MOSFET's at the poly-Si RIE step, and thus the results obtained from the test MOS can be applied to future devices.

Compared to the control devices with an Al gate or wet-etched poly-Si gate, where the gate oxide breakdown field is >13MV/cm, the gate oxides are very leaky after poly-Si

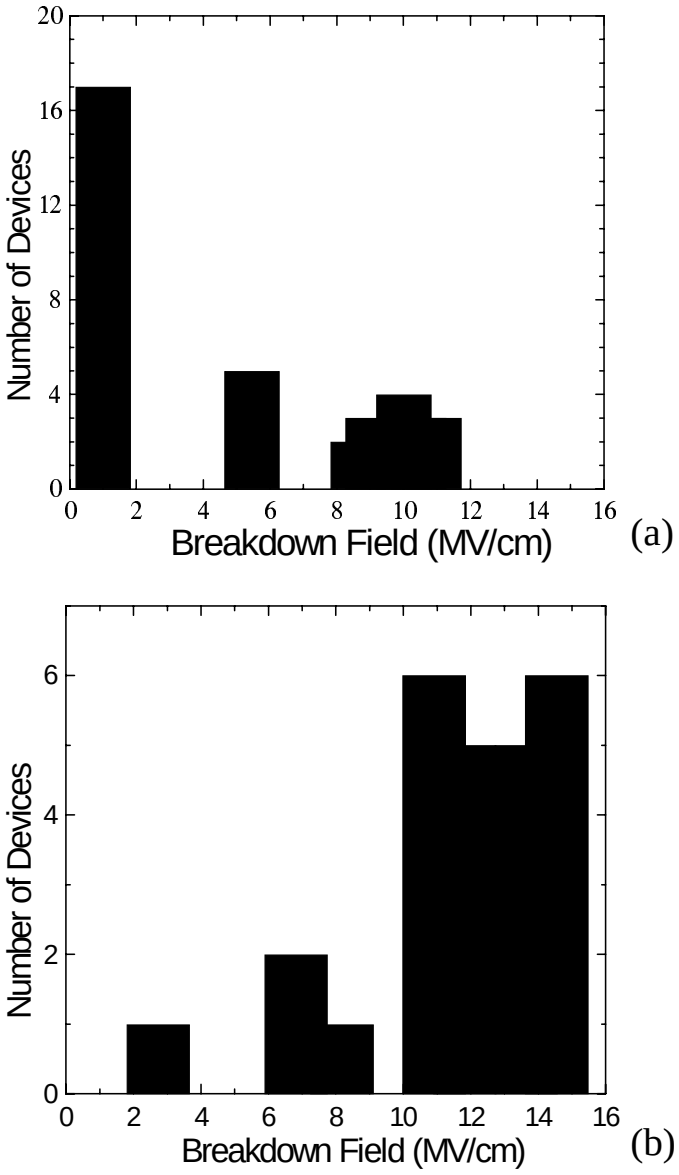


Figure 3.6: Histogram of gate oxide breakdown field after poly-Si etching from test MOS devices in Fig. 3.7a. Poly-Si is etched by 42.5sccm CF_4 and 7.5sccm O_2 at 200mtorr and 0.04watt/cm^2, with (a)one-step RIE for 10min and (b) RIE for 8min and wet-etch to the end-point.

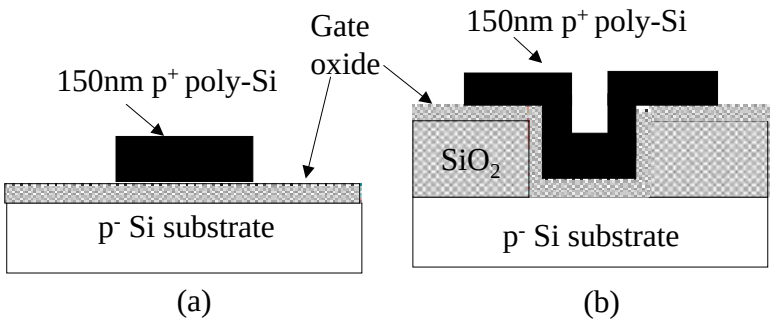


Figure 3.7: MOS structures used to study the effects of poly-Si gate RIE on the thin gate oxides underneath. (a) A structure simulating the processing in vertical MOSFET's. (b) MOS with field oxide before gate oxidation.

gates are etched in RIE system using SF_6, CF_4 or their mixtures with O_2. At higher RF power, the gate oxide quality is worse. There have been many investigations of gate oxide damage from plasma processing in the 1990's. The charging effect, induced by non-uniform plasma, is believed to be the major source of the damage of the thin gate oxide in plasma processing [109, 110, 111, 112, 113, 114]. If the gate oxide breakdown observed here was mainly caused by the charging effect due to non-uniform plasma, the oxide quality would have been dependent on the sample size. However, no obvious wafer size effect is found, even using Al as an etching mask, where larger plasma charging effect would have been expected compared to that using a photoresist etching mask. It is reported that forming gas annealing or 900^oC annealing in nitrogen can improve the oxide quality after electrical stress caused by wafer charging [115]. However, for the MOS devices made under our process conditions, neither 900^oC N_2 annealing nor re-oxidation in pure O_2 improves the already damaged oxides. Additionally, no obvious improvement is found after 650^oC 30min annealing in forming gas.

Although the primary cause of gate oxide degradation during plasma etching has been attributed to charge buildup, gate oxide directly exposed to a plasma can also be degraded by energetic ion bombardment or ultraviolet emission from RF plasma [113, 116, 117, 118]. Under the same oxidation and RIE conditions as the sample in Fig. 3.5/Fig. 3.6a, test MOS structures with field oxides before gate oxidation (Fig. 3.7b), give high quality gate oxides

Poly-Si gate RIE	p^+ poly-Si etching rate (nm/min)	selectivity of SiO_2 over p^+ poly-Si	Results
Al gate (control)	-	-	D_{it} $\sim 10^{10} cm^{-2} eV^{-1}$, E_{bd} >13MV/cm
wet-etched in $HF+HNO_3+H_2O$ (6:100:40) (control)	800	32:1	D_{it} $\sim 10^{10} cm^{-2} eV^{-1}$, E_{bd} >13MV/cm
16sccm SF_6 (150mtorr, 0.1watt/cm^2)	220	75:1	all breakdown (for all t_{ox} <500Å)
21sccm SF_6+ 3sccm O_2 (150mtorr,0.1watt/cm^2) (*b*)	250	<25:1	50% devices breakdown
(*b*)+ 900^{o}C N_2 30min	-	-	all breakdown
CF_4, 0.2watt/cm^2	32	2.7:1	75% breakdown
42.5sccm CF_4+ 7.5sccm O_2 (0.04watt/cm^2, 200mtorr) (*a*)	14	7.5	50% breakdown, 10% E_{bd} <10MV/cm, 40% E_{bd} ~10MV/cm
(*a*) + 900^{o}C dry O_2 20min	-	-	all breakdown
(*a*) + 650^{o}C Forming Gas 30min	-	-	50% breakdown, 50% E_{bd} ~ 13MV/cm
(*a*), using Al as etching mask	-	-	30% breakdown, no wafer size effect
(*a*) with field oxide	-	-	all the devices E_{bd} >12MV/cm
(*a*) + wet etch around end-point	-	-	90% E_{bd} >12MV/cm
CF_4, 0.8watt/cm^2, 100mtorr + wet etch around end point	130	1.3:1	15% breakdown, 25% low E_{bd}, 60% E_{bd} ~13MV/cm
25sccm SF_6+1.5sccm CCl_2F_2 (150mtorr, 0.2watt/cm^2)	950	120:1	E_{bd} >13MV/cm

Table 3.1: Gate oxide (t_{ox}=110Å) quality after p^+ poly-Si gate patterning under various etching conditions. Photoresist was used as etching mask unless noted. The MOS structure is shown in Fig. 3.7a without field oxide unless noted.

after processing. The breakdown fields of all the devices are larger than 12MV/cm, similar to the control devices using wet-etch. This dramatic difference from the results of the MOS structure in Fig. 3.7a, indicates that the exposure of the gate oxide edge to plasma causes the high leakage current during the polysilicon gate over-etch. To reduce the damage on the gate oxide edge, a combination of RIE and wet-etching is used: most of the poly-Si gate was etched using high power RIE to achieve a vertical profile, and then a wet-etch was used for the last point during the etching. Noticeable improvement is achieved. Using the same etching as the devices shown in Fig. 3.5/Fig. 3.6a, i.e. 42.5sccm CF_4 and 7.5sccm O_2 at 200mtorr and 0.04watt/cm^2, 90% of the devices have breakdown field larger than 12MV/cm if using wet-etch around the end-point (Fig. 3.6b). Increasing the RF power to 0.8watt/cm^2 in a CF_4 plasma, 60% of the devices retain a high gate oxide breakdown field (13MV/cm) when stopping the plasma before the end-point and adding a wet-etching step during poly-Si over-etch. This is in contrast to 75% breakdown at 0.2watt/cm^2 using one-step-RIE.

These results confirm that the thin gate oxide is mainly damaged after the end-point, e.g. after the poly-Si is totally etched away. Thus a more highly selective etching of poly-Si over SiO_2 is expected to improve the gate oxide quality after gate poly RIE. Fig. 3.8a gives the typical gate leakage current for MOS capacitors with 11nm gate oxides (800^oC wet oxidation) after the polysilicon gates are etched by RIE using a photoresist mask and a gas mixture of 25sccm SF_6 and 1.5sccm CCl_2F_2 at 150mtorr and 0.2watt/cm^2. The MOS structure is the same as that in Fig. 3.7a. The breakdown voltages from MOS with various device areas are the same as those from the control sample with wet-etched poly-Si gate, with a breakdown field >13M/cm for *99%* of measured devices. Fig. 3.8b gives capacitance-voltage measurement of the sample. No obvious increase of the interface density is observed. Such significant improvement of gate oxide quality after p^+ poly-Si gate RIE, as compared with previous results, is probably due to the high selectivity (120:1) between poly-Si and thermal oxide obtained under this etching condition, enabling less gate oxide damage during poly-Si over-etch. This poly-Si gate RIE condition will thus be used for all the vertical MOSFET's presented in this work.

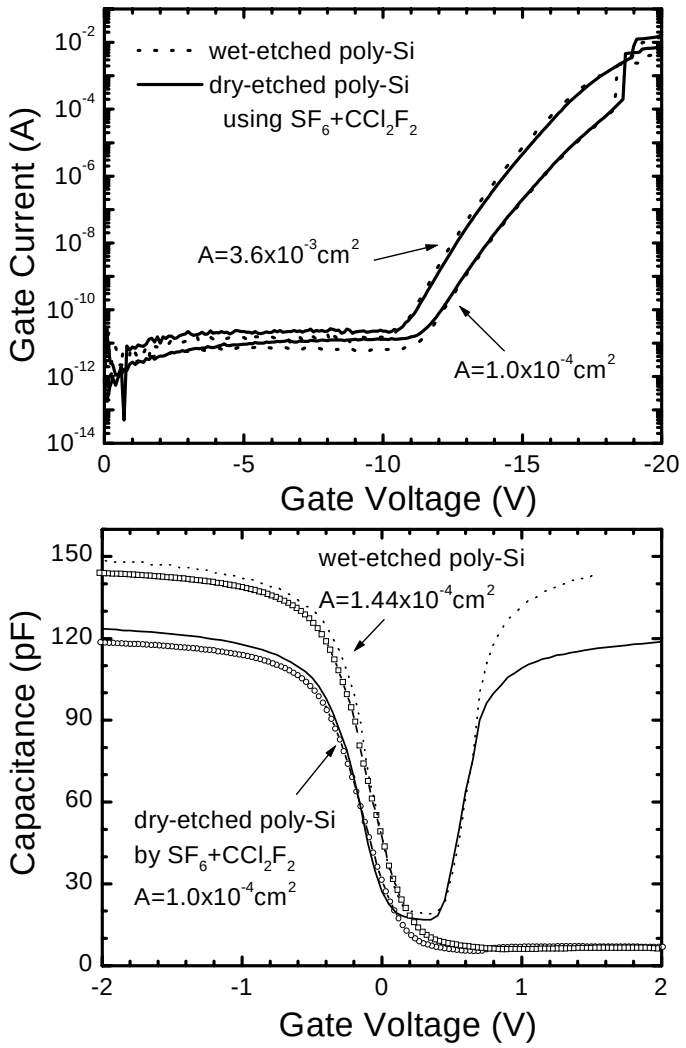


Figure 3.8: (a) Gate leakage current and (b) capacitance-voltage characteristics of MOS with a similar structure as shown in Fig. 3.7a. The poly-Si was etched by 25sccm SF_6 and 1.5sccm CCl_2F_2 at 150mtorr and 0.2watt/cm^2. The gate oxide was grown at 800^{o}C in wet oxygen with a thickness of 11nm. Characteristics of control devices with wet etched poly-Si gates are also plotted for reference.

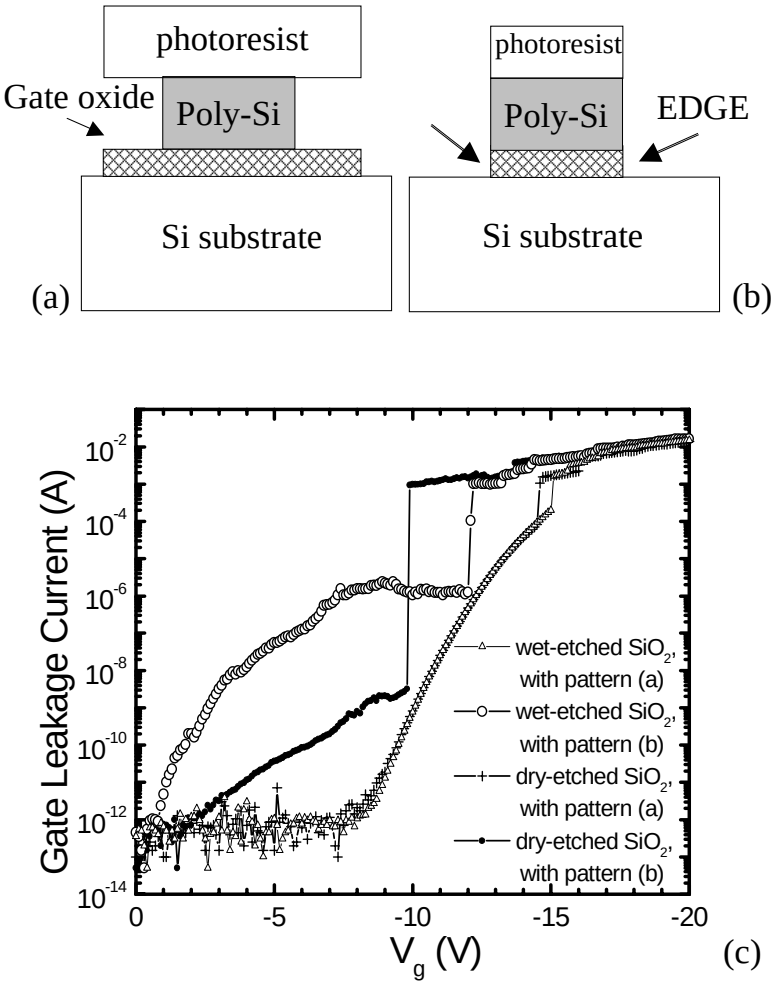


Figure 3.9: Test MOS structures with etched gate oxide edges (a) far from the poly-Si gate, (b) at the edge of poly-Si gate. (c) Gate leakage current from these two structures with gate oxide etched by wet-chemical and by RIE.

Evidence of gate oxide degradation due to the damage on the oxide edge is further proved in the following experiment, shown in Fig. 3.9. First, 90Å gate oxide was grown at 750^oC by wet oxidation (the same condition as that for vertical MOSFET's), followed by 200nm p^+ poly-Si deposition in the RTCVD system. A poly-Si gate was then patterned using 25sccm SF_6 and 1.5sccm CCl_2F_2 at 150mtorr and 0.2watt/cm^2. Finally, the gate oxide was fully etched away using two different masks. One provided a larger protection area than the poly-Si gate (Fig. 3.9a), while the other had the same size as the poly-Si gate, where the edge of the oxide is exposed to the etch process (Fig. 3.9b). Two methods of gate oxide etching are studied: by buffered oxide etching (BOE) and by RIE. 15sccm CHF_3 at 150mtorr and 0.1watt/cm^2 was used for the RIE of gate oxide, giving an etching rate of 65Å/min. The typical current-voltage characteristics of these samples are plotted in Fig. 3.9c. For the devices with gate oxide etching masks larger than the poly-Si gates (Fig. 3.9a), the breakdown fields are >14MV/cm using either RIE or BOE etching, the same as those in Fig. 3.8, where gate oxide etching is strictly limited during poly-Si over-etch due to the high selectivity. However, for those devices with gate oxide etching protection masks with the same size as the poly-Si gates (Fig. 3.9b), lower breakdown voltages are observed, no matter whether the gate oxide was etched by BOE or RIE. This experiment indicates that the end-point control of the poly-Si etching is very critical for the thin gate oxide. Extensive exposure of the gate oxide to the etchant (plasma or acid) will lead to larger leakage current due to the damage on the oxide edges.

(II) In situ Non-invasive Probe of RIE Rate and End-point Using Interferometry

Control of the over-etch of gate polysilicon has become a key to avoiding gate oxide degradation, as demonstrated in the previous section. Several methods have been used to monitor etch rates and end-points in literature. Optical emission spectroscopy is the most widely used technique to measure end-points [119]. An interferometer was installed in the Plasma Technology system in this work and has been used for the end-point control of the poly-silicon etching. Interferometry provides a continuous measurement of the etching rate [119, 120, 121]. The overall scheme is illustrated in Fig. 3.10a. Optical interference occurs as

the light reflects off the top and bottom of the poly-Si layer. The intensity of the reflection can thus be used as an indicator of the poly-Si thickness. A 3mW He-Ne laser (λ=6328Å) was used as a light source and a room temperature Si photodiode was used to measure the reflected light intensity. Note that as Si has very low absorption coefficient ($4\times10^3\text{cm}^{-1}$) in the visible red light region [122], for a 200nm film thickness only 8% of the incident light will be absorbed. A window on top of the chamber was used as the optical access to and from the wafer front surface. During poly-Si RIE, the reflection intensity oscillates, with a period Δd as:

$$\Delta d = \frac{\lambda}{2n} \tag{3.1}$$

at vertical incidence. n is the refraction index of poly-Si. For the poly-Si grown in this work, n=3.25±0.15, and $\Delta d = 970 \pm 45\mathring{A}$. Thus using this set-up, the poly-Si etching rate can be monitored *in situ*.

Fig. 3.10b shows a typical interferogram (reflection intensity vs. etching time) for the etching of a poly-Si gate down to the underlying gate oxide layer. The etching is carried out in a 25sccm SF_6 and 1.5sccm CCl_2F_2 plasma at 100mtorr and 0.2watt/cm^2 RF power. Because the poly-Si etching used here is highly selective over the underlying SiO_2 (120:1), the end-point corresponding to the complete removal of the poly-Si film is clearly visible as a cessation of the oscillation. The delayed oscillation in the beginning of the etching is due to the native oxide on the sample surface. This "incubation" time varies from sample to sample. By using interferometry, the end-point of each sample can be precisely controlled. End-point detection is helpful to turn-off the plasma before over-etching of the underlying thin gate oxide occurs, thus reducing the damage to the thin gate oxide.

Note that during the poly-Si gate RIE, photoresist is used as the protection mask for the contact pad. Light interference from the top of the mask and the etched poly-Si surface also takes place. For all the vertical MOSFET's in this thesis, less than 1% of the area is covered by photoresist, enabling the dominant signal to be that from the interference of reflected light from top and bottom of the poly-Si.

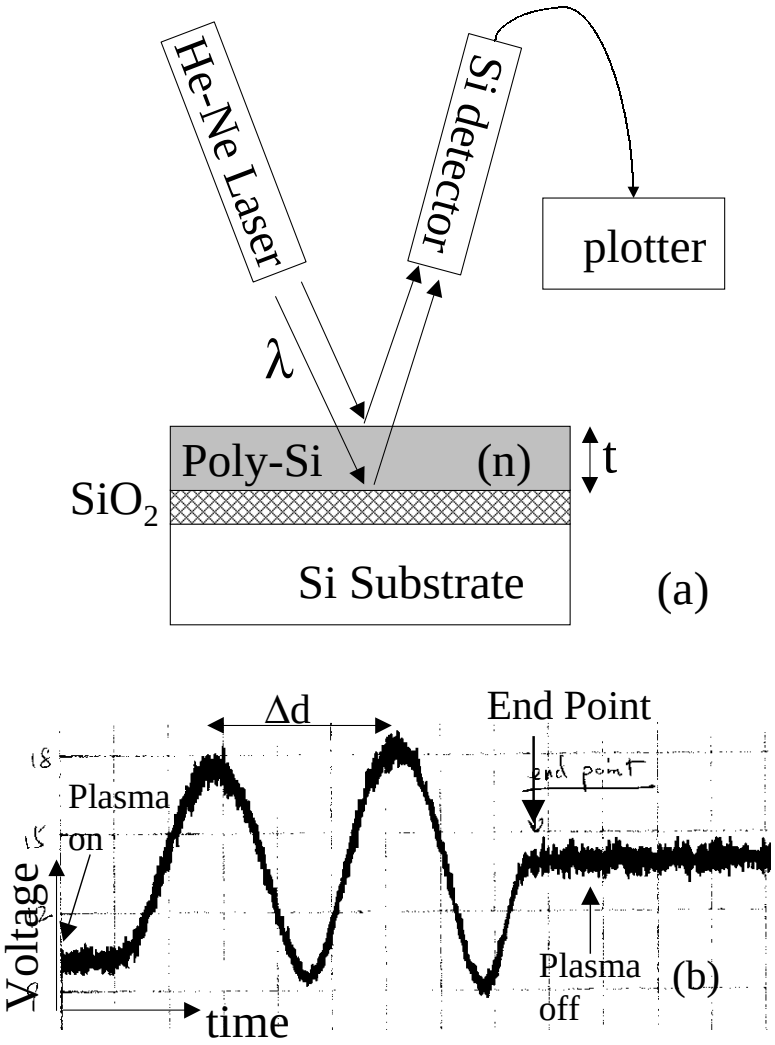


Figure 3.10: (a) Set-up of interferometer for monitoring RIE end-point and etch rate monitor. (b) A typical interferogram (reflection intensity vs. etching time) for poly-Si gate etching.

(III) Effect of Plasma-Enhanced CVD on Thin Gate Oxide

To this point, thin gate oxide quality has been dramatically improved using a highly selective poly-Si RIE and real-time end-point control. However, to maintain a high quality gate oxide, the exposure of it directly to plasma after poly-Si etching should also be avoided. In the device processing, insulation layers before metal contact are required. SiO_2 is the most commonly used insulator for this purpose. To avoid dopant diffusion, low temperature deposition is usually used. During the course of the present work, plasma enhanced chemical vapor deposition (PECVD) was the only low temperature ($\leq 280^oC$) source of SiO_2 deposition. The effect of SiO_2 deposited by PECVD after poly-Si etching thus is discussed below.

The cross-section of the devices is illustrated in Fig. 3.11a. The gate oxides and poly-Si gates are made under the same condition as those in Fig. 3.8. After poly-Si patterning, 550nm insulation oxide was deposited by PECVD at 280^oC and 900mtorr with 475sccm N_2O and 200sccm SiH_4. The RF power was $0.08watt/cm^2$ and the deposition rate is 140nm/min. Contact windows on top of the poly-Si gate were made through the PECVD oxide using BOE. Front and back Al contacts were thermally evaporated and etched in H_3PO_4. Thus PECVD is the only plasma process after poly-Si patterning. As shown in Fig. 3.11b, the gate oxide quality, after exposed to plasma during the deposition, is degraded compared with that from Fig. 3.8, with 30% devices having breakdown field less than 12MV/cm. During PECVD, the edge of the gate oxide is exposed to the plasma. Although no etching occurred, the thin gate oxide suffers from exposure to the radiation from the UV and the energetic ion bombardment. Therefore, after poly-Si is removed from the thin gate oxide, any over etching or exposure to plasma (radiation) will have an adverse effect on the oxide quality and should be avoided in processing.

In summary, the thin gate oxide damage during the poly-Si RIE in this work is mainly due to the oxide edge damage during the over-etch. By using a highly selective RIE (25sccm SF_6 and 1.5sccm CCl_2F_2 at 150mtorr and $0.2watt/cm^2$), the thin gate oxide quality after

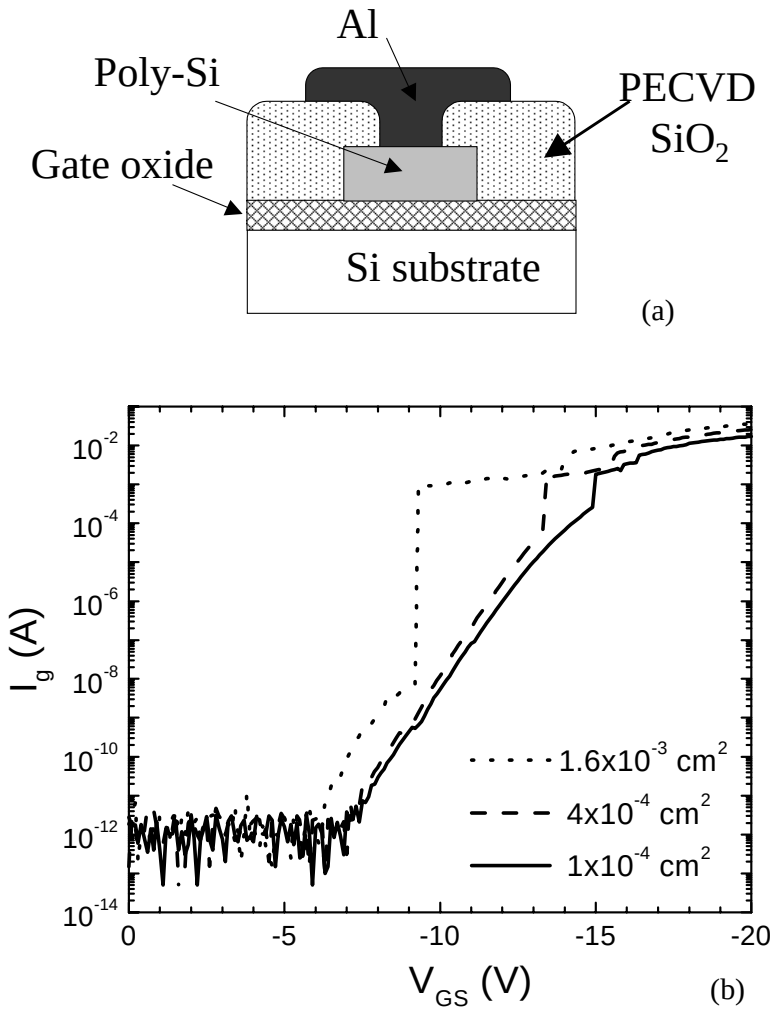


Figure 3.11: (a) I-V curves of MOS structures of various areas with insulation SiO_2 deposited by plasma enhanced CVD after poly-Si etching. The gate oxidation and poly-Si etching conditions are the same as those in Fig. 3.8. (b) Gate leakage current measured from this MOS structure.

poly-Si RIE has been dramatically improved. To reduce the over-etch time, an interferometry technique has been developed as an etching end-point indicator. However, to avoid degradation of the thin gate oxide, plasma exposure should be avoided after poly-Si etching.

3.2.5 Anisotropic Si Etching

Vertical MOSFET's are fabricated on the sidewalls of silicon layers. Using the "planar epitaxy" approach to fabricate vertical double-gate MOSFET's, thin silicon pillar structures with high aspect ratio are required. Using the "selective epitaxy" approach, an anisotropic SiO_2 etching is used to open the seed window for the selective epitaxy. In this work, both anisotropic Si and SiO_2 profiles have been achieved on the then available equipment at Princeton. In this section, only Si RIE will be discussed. The SiO_2 etching will be discussed in Sec. 3.4.4.

A highly anisotropic silicon etching technique was developed as a part of the current work by using gas mixtures of SF_6/CCl_2F_2 in an RIE chamber (Plasma Technology). The RIE system consists two parallel plates with 13.56MHz RF generators and an impedance matching network. The RF power is capacitively coupled to the bottom electrode in the reactive ion etching mode. The bottom electrode is Al, covered with Al_2O_3. A butterfly valve is used to control the pressure. The chamber is cylindrical, about 5cm in height and 25cm in diameter.

Fig. 3.12a gives the cross-section scanning electron microscope (SEM) picture of a 10μm deep trench on p^- Si substrate. Photo-resist AZ1518 was used as the etching mask. The RF power was 0.2watt/cm^2 with self-bias on the cathode of 20V. SF_6 and CCl_2F_2 flow rates were 25 and 1.5 sccm, respectively, while the chamber pressure was kept at 150mtorr. The etching rate for the undoped Si is about 1.8μm/min. It is of note that the etching rate decreases in highly boron doped Si. For the p^+ poly-Si gate used here, the etching rate is 950nm/min. As shown, the side-wall is perfectly straight and the bottom of the trench is very smooth. This etching is also highly selective, with a selectivity over thermal SiO_2 of 120:1 and over AZ1518 of 30:1. In pure SF_6 the silicon etching will have a large undercut due to isotropic fluorine atom etching. The reason for the nearly vertical side-walls obtained in

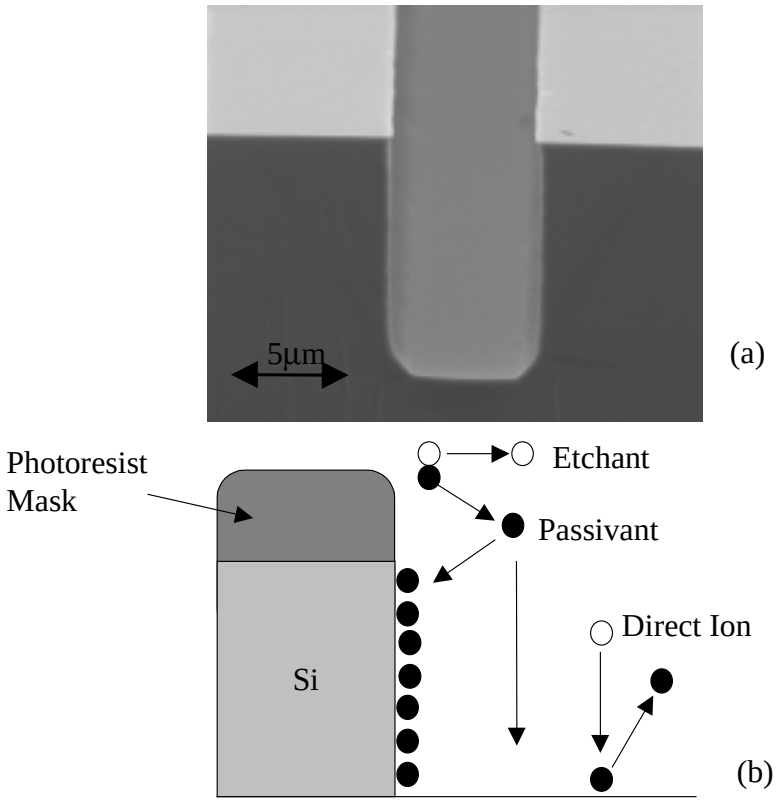


Figure 3.12: (a) Cross-section SEM of a Si trench etched by SF_6 (25sccm) and CCl_2F_2 (1.5sccm) at 150mtorr and 0.2watt/cm^2. (b) Mechanism of anisotropic etching due to side-wall passivation.

the SF_6 and CCl_2F_2 mixture is due to the deposition of polymerized species. The polymer deposited on the side-wall prevents lateral etching, while incident ions has enough energy to desorb those polymer presented on the bottom, as illustrated in Fig. 3.12b.

Under this etching condition, 25μm deep trenches are achieved with various openings (Fig. 3.13). After 14min exposure to plasma, the bottom of the trench starts to look rough. No etching rate variation due to the aspect ratio of the trench is observed. However, it is found that the feature size affects the trench profile. In Fig. 3.13, three patterns are on the same sample with widths of 6, 10, and 55μm. For a 10μm wide window, a vertical profile is achieved. But for a 6μm trench, side-wall "bowing" is observed, while 7^o deviation off the vertical direction is found for the 55μm size. Moreover, the etching is also sensitive to the mask used. If changing the etching mask from AZ1518 to SiO_2, the etching is completely isotropic, which suggests that *photoresist* participates the polymer formation in the presence of CCl_2F_2. In the case of SF_6 and $C_2Cl_3F_3$, the generation of the passivation polymer is attributed to the reaction between photoresist and active species from the plasma and their redeposition on the side wall by ion sputtering [123]. We speculate that a similar mechanism may be applied to the RIE using SF_6 and CCl_2F_2. In Fig. 3.12 and Fig. 3.13, the photoresist covered >90% of the areas.

Fig. 3.14a shows a silicon pillar etched under the same condition as the silicon trench in Fig. 3.12. Using the same mask, image reversal is obtained using photoresist AZ5214, such that only a small part of the sample is covered with photoresist, in contrast to the case in Fig. 3.12. It shows that the profile of the side wall changes from perfectly anisotropic in Fig. 3.12 to isotropic with large undercut. Increasing the CCl_2F_2/SF_6 ratio may reduce the undercut, but will also decrease the etching rate and reduce the selectivity over photoresist. In Fig. 3.14b, the flow rate of CCl_2F_2 and SF_6 was changed to 9sccm and 3sccm, respectively. A thin oxide layer is added under the photoresist during RIE to prevent the possible mask side erosion problem. However, the side-wall is not vertical. Changing the gas to pure CCl_2F_2 resulted in no improvement. A reduction in pressure will increase the ion direct bombardment, while increasing the power will increase the bombardment energy. Both will serve to increase the etching rate and may improve the profile. Shown in Fig. 3.14c, the

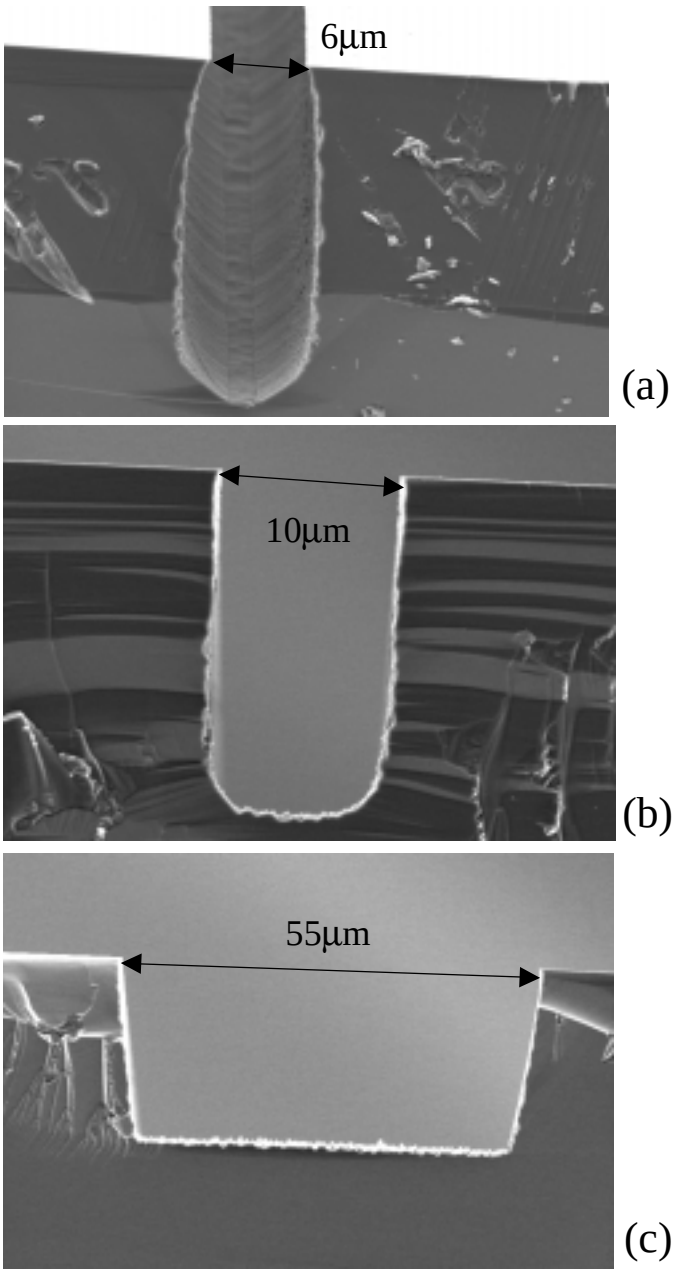


Figure 3.13: Cross-section SEM of the 25μm deep Si trenches etched by SF_6 (25sccm) and CCl_2F_2 (1.5sccm) at 150mtorr and 0.2watt/cm^2. The trench width is (a) 6μm, (b) 10μm and (c) 55μm.

etching is very directional using 3sccm SF_6 and 9sccm CCl_2F_2 at 35mtorr and 0.2watt/cm^2. However, the silicon surface and/or the photoresist mask after the etching is often "black", showing significant pits under SEM. These results suggest that a sufficient (for reliable passivation) thickness of the polymer layer can only be formed in a certain range of gas composition, ion energies, and in presence of *sufficient photoresist*.

There are two ways to increase the polymer concentration in the reaction. H_2 can be added to change the chemistry in the gases or polyimide electro-plate can be used. In this work, photoresist covered Si wafers were introduced and placed on the top of the bottom electrode inside the chamber, and the etching samples were put on top of the photoresist, as illustrated in Fig. 3.15a. The samples were prepared and then etched using the same conditions as in Fig. 3.14a. A cross-section SEM of a sample is shown in Fig. 3.15b. There is still a large undercut below the photoresist, which means that the photoresist added in the chamber still can not produce as much polymer as in the case of silicon trench etching under the same etching condition. However, if one increases the CCl_2F_2/SF_6 ratio to 5sccm/8sccm, there is too much polymer and the side wall is over-protected (Fig. 3.15c). Only by optimizing CCl_2F_2/SF_6 ratio, pressure, and power, can an anisotropic silicon pillar etching be achieved. Shown in Fig. 3.15d, using 21sccm SF_6 and 2.2sccm CCl_2F_2 at 20mtorr, 0.03watt/cm^2, an anisotropic etching of Si pillar is obtained. The etching mask consists of AZ5214 and wet-etched SiO_2. Because the high selectivity, only the photoresist serves as an effective etching mask here.

The etching mask used during RIE will not affect the etching profile after introducing additional photoresist in the chamber and using high CCl_2F_2/SF_6 ratio. Shown in Fig. 3.15e, the perfect vertical pillar is also achieved under the same etching condition as that in Fig. 3.15d, but using pure PECVD SiO_2 as etching mask. Furthermore, the profile of the pillar is independent of the pillar width. Fig. 3.16 shows thin silicon pillars etched under the same RIE conditions after E-beam lithography, with mask sizes of 0.5, 0.2 and 0.1 μm. The right column shows the enlarged profiles before the resist removal, except in Fig. 3.16a. A silicon pillar thickness of 40nm and height of 400nm has been achieved, enabling the fabrication of vertical double-gate MOSFET's and other vertical quantum-devices (e.g. the

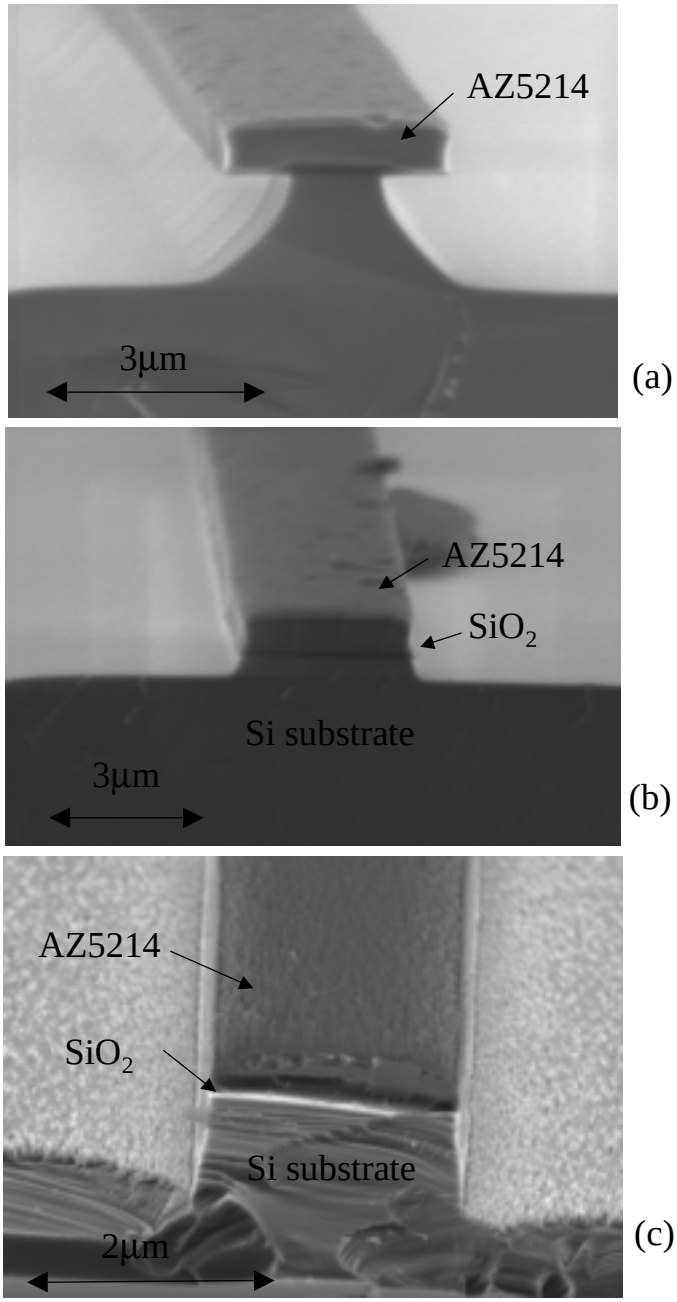


Figure 3.14: Cross-section SEM of Si pillars using AZ5214 image reversal as an etching mask and etched by (a) SF_6 (25sccm) and CCl_2F_2 (1.5sccm) at 150mtorr and 0.2watt/cm^2, (b) SF_6 (3sccm) and CCl_2F_2 (9sccm) at 150mtorr and 0.2watt/cm^2, (c) SF_6 (3sccm) and CCl_2F_2 (9sccm) at 35mtorr and 0.2watt/cm^2.

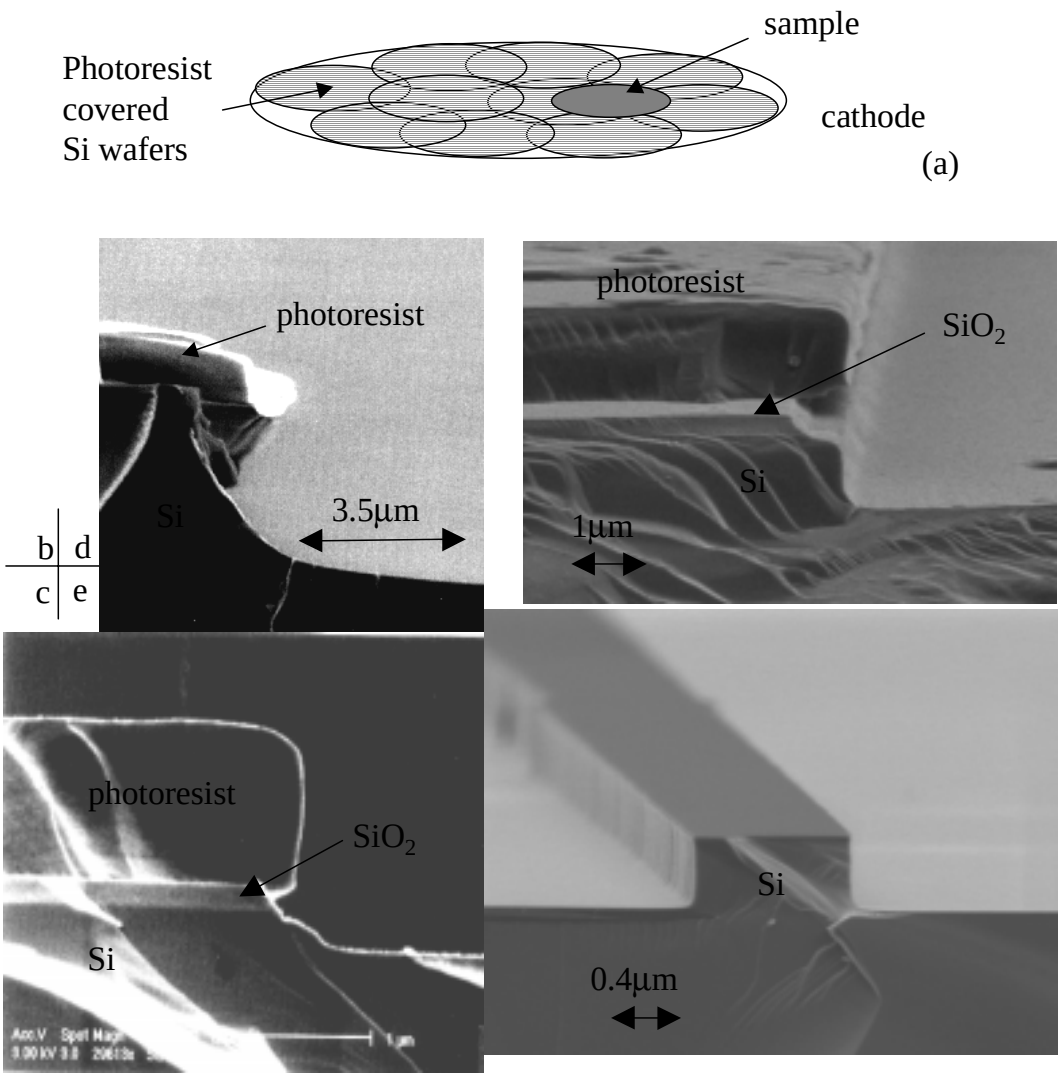


Figure 3.15: (a) Illustration of bottom electrode covered by photoresist-painted silicon wafers to increase the side wall protection. Cross-section SEM of silicon pillars etched on the above electrode with photoresist AZ5214 as the etch-mask, using (b) SF_6 (25sccm) and CCl_2F_2 (1.5sccm) at 150mtorr and 0.2watt/cm^2, (c) SF_6 (8sccm) and CCl_2F_2 (5sccm) at 150mtorr and 0.2watt/cm^2, (d) SF_6 (21sccm) and CCl_2F_2 (2.2sccm) at 20mtorr and 0.03watt/cm^2. (e) Si pillar etched using SiO_2 as the etch mask under the same etching condition as in (d). The cross-section SEM shows the profile after the mask removal.

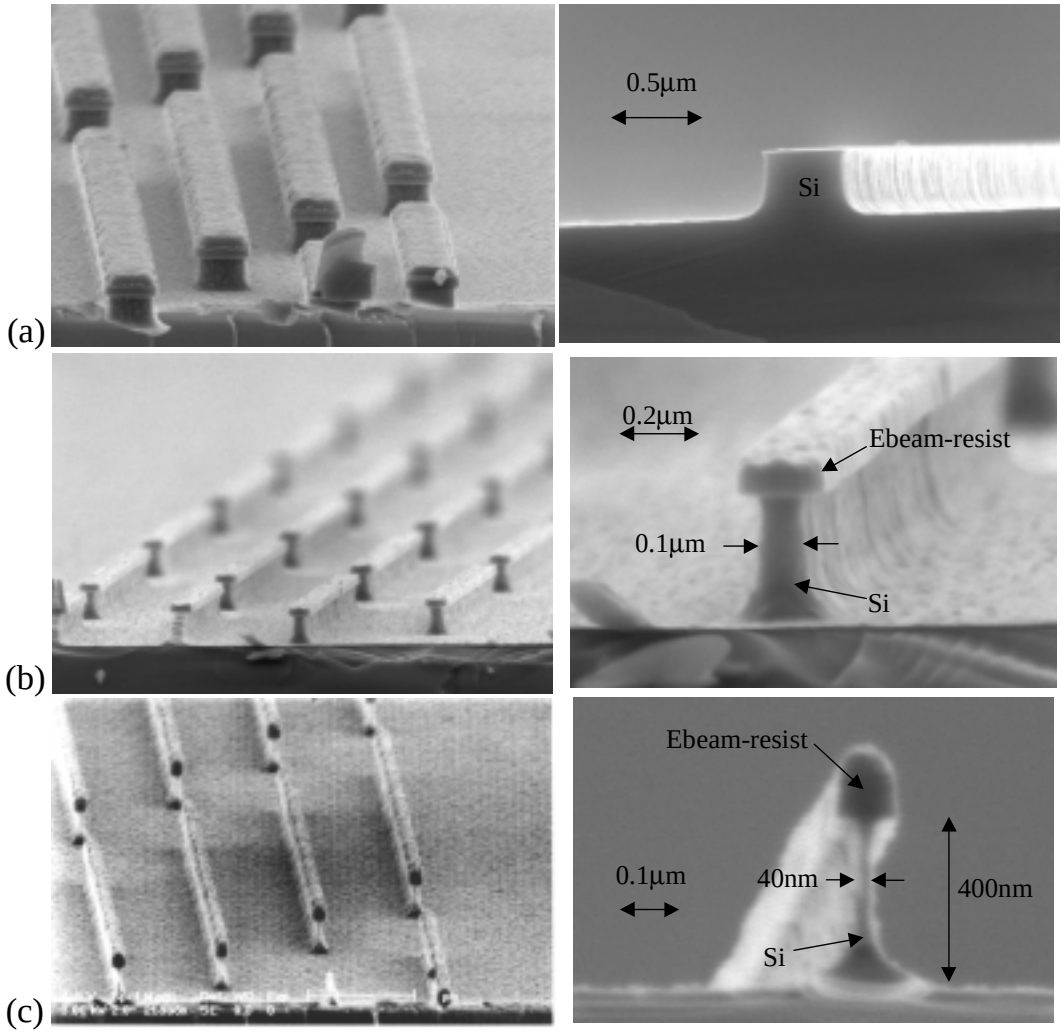


Figure 3.16: Cross section SEM of silicon pillars etched in a gas mixture of SF_6 (21sccm) and CCl_2F_2 (2.2sccm) at 20mtorr and 0.03watt/cm^2, with the presence of additional photoresist placed on the bottom electrode. The etching mask is E-beam resist with a size of (a) 0.5μm, (b)0.2μm and (c) 0.1μm. No obvious feature size dependence is found in the pillar profiles.

single electron transistor), using the "planar epitaxy" approach.

3.3 Fabrication of Vertical MOSFET's Using "Planar Epitaxy"

Because the vertical MOSFET is a novel structure and little work in the literature has been reported in this area, especially for p-channel devices, and because this is the first Princeton attempt at a sub-100nm vertical double-gate MOSFET, it is thus necessary to study the device scaling in the vertical structures first. A simple "planar epitaxy" approach was developed, which will be used in Chapter 5, for studying vertical p-channel MOSFET's in the sub-100nm regime. In this design, the two channels formed on the side-walls of a wide mesa are independent of each other, in contrast to the double-gate MOSFET's discussed in the previous chapter. The main process steps for a vertical p-channel MOSFET are illustrated in Fig. 3.17. Similar processes can be applied to the n-channel devices. Methods used in the demonstration of vertical MOSFET's with sub-100nm channel lengths on the side walls of wide mesa, can be extended to the fabrication of double-gate MOSFET's on the side walls of ultra-thin pillars. The modification of the process will be briefly discussed in the end of this section. The main change from a wide mesa structure to an ultra thin pillar is that a planarization step is necessary to expose the top of the ultra thin pillar for the contact.

Step 1: Grow p^+np^+ epitaxial layers on a planar p^- Si substrate using Rapid Thermal Chemical Vapor Deposition. The channel length is determined by the distance between the two p^+ epitaxial layers. In this thesis, the devices fabricated using this approach are on the side-walls of wide mesa structures, thus the channels have to be doped to suppress punch-through.

Step 2: Define the silicon mesa by optical lithography. Use reactive ion etching to create the wide mesa.

Step 3: A sacrificial oxide is grown and removed before gate oxidation to smooth the side wall. *In situ* doped p^+ poly-silicon is deposited right after the gate oxidation.

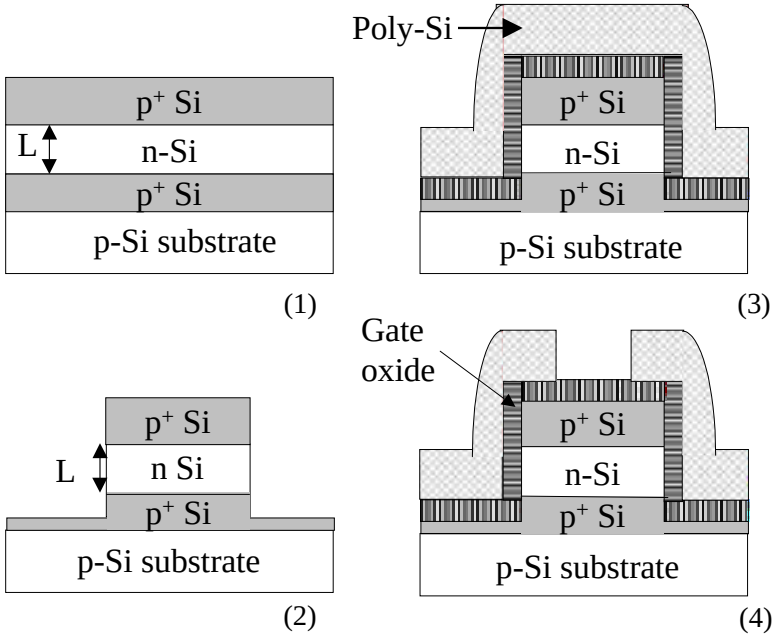


Figure 3.17: Process design for the vertical MOSFET's using "planar epitaxy" approach. The two channels are on the sidewalls of a wide mesa.

Step 4: Poly-Si gate is patterned by optical lithography.

Step 5: The insulation layer is applied on the sample and the contact windows are opened. The device is completed after patterning the metal layer. The final cross-section of the device is shown in Fig. 3.18.

The typical layout of this design is shown in Fig. 3.19. There are four optical lithography layers. The first layer is used to define the mesa etching after epitaxy. The second layer is used for poly-Si gate patterning. The final two layers are used for contact windows and metal pattering. The mesa is wide ($d > 20\mu$m). The width W of each vertical MOSFET on the side wall is 50 or 100μm. Key process steps will be discussed in detail next.

3.3.1 Planar Silicon Epitaxy by RTCVD

(I) Rapid Thermal Chemical Vapor Deposition System at Princeton

The epitaxial silicon layers of all the samples in this thesis were grown on the silicon (001) substrates in a rapid thermal chemical vapor deposition (RTCVD) system at Princeton, as

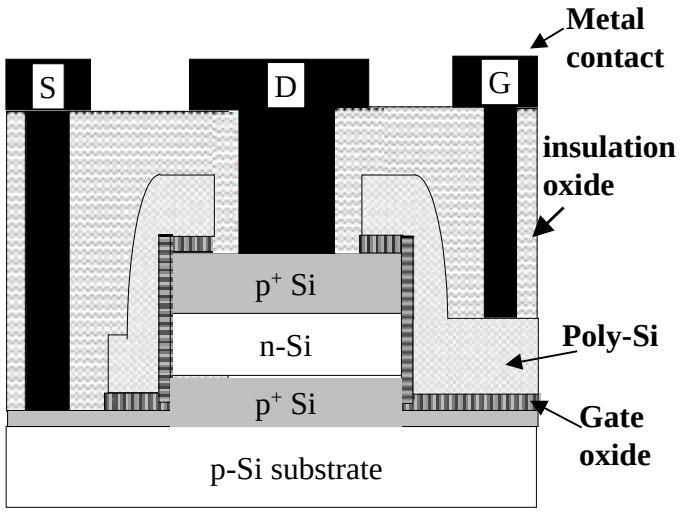


Figure 3.18: Cross-section of a vertical MOSFET made by "planar epitaxy"; the channel length is defined by epitaxy and the wide mesa is created by RIE.

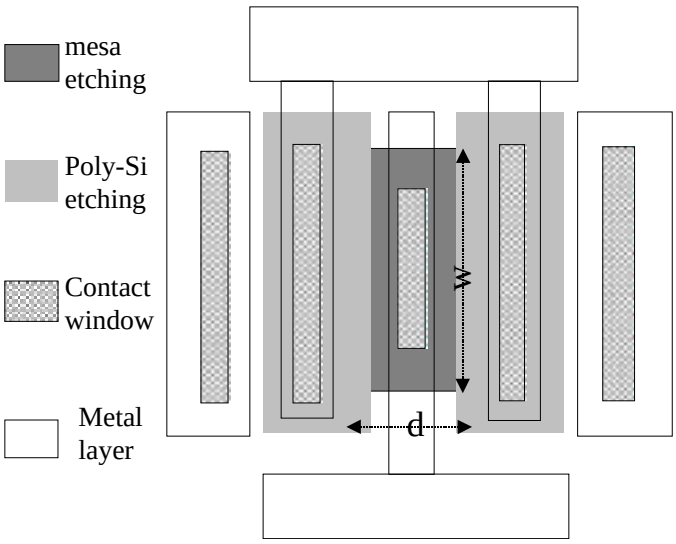


Figure 3.19: Layout of a vertical MOSFET on the side walls of a wide mesa using the "planar epitaxy" approach.

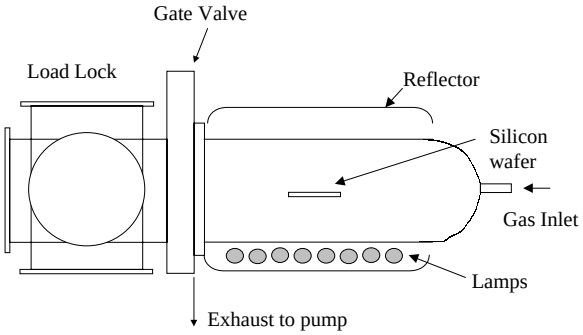


Figure 3.20: Schematic diagram for the RTCVD reactor used in this work.

illustrated in Fig. 3.20[124]. It is a single-wafer cold-wall system. The growth chamber is a cylindrical quartz tube, separated by a gate valve from a load lock system. The wafer sits on a quartz stand and its surface is perpendicular to the cross-section of the tube. It is heated from the backside by tungsten-halogen lamps. The entire tube and lamps are enclosed in a water-cooled gold-plated reflector, thus the wall of the growth chamber is only few hundred Centigrade degree even during high temperature ($\sim 1000^o$C) processes, limiting depositions on the tube. The gas flow rates are controlled by mass flow controllers and the gases can be rapidly switched by five-ported valves. The chamber pressure is adjusted by a butterfly valve on the exhaust line. Between 550 to 800^oC (Si, SiGe and SiGeC growth regime), the lamp power is controlled by a feed back system. The wafer temperature can be monitored by the transmission of infrared light (1.3 and 1.55μm)[125]. Direct calibration of the wafer temperature vs. lamp power has been achieved by attaching a thermocouple to the wafer surface. The result is given in Fig. 3.21. In this work, double-side polished wafers are used to achieve higher light transmission and better temperature control, especially for T$\geq 750^o$C.

(II) Epitaxy for the Vertical MOSFET's on a Planar Silicon surface

All vertical MOSFET's epitaxial layers were grown by rapid thermal chemical vapor deposition using dichlorosilane (DCS) as the silicon source. Si(100) substrate was cleaned in H_2SO_4+H_2O_2 (2:1), followed by a diluted HF dip. In situ cleaning was performed at 1000^oC and 250torr in H_2 for 2min. During the growth, the pressure was maintained at

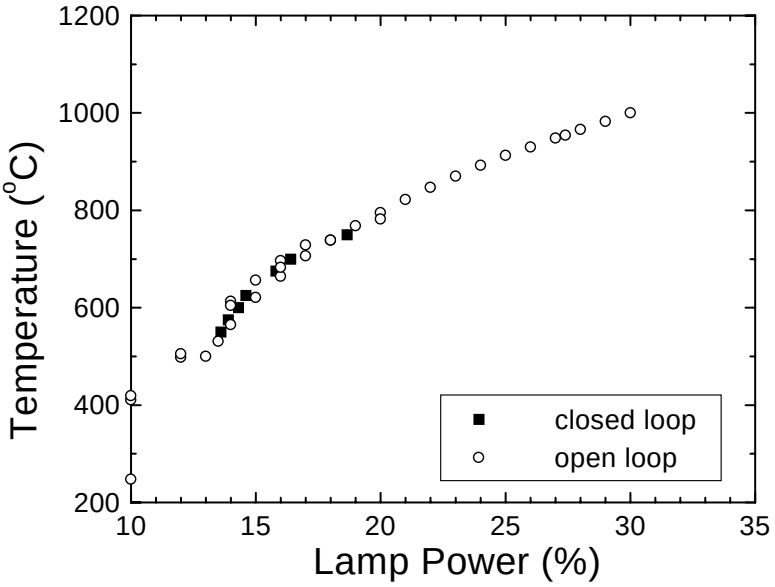


Figure 3.21: Wafer temperature vs. lamp power for the RTCVD system at Princeton calibrated by thermocouple.

6torr, while 26sccm DCS was carried by 3slpm hydrogen. Diborane and phosphine were used the dopant sources. For p-channel MOSFET's, the device active layers were grown on top of a 1 μm Si buffer with a boron doping level of 3×10^{19} cm^{-3}. The silicon channel was grown at 700^{o}C and doped with phosphorus. There were two 60 Å undoped silicon spacer layers on each side of the channel to compensate boron diffusion during the growth. The 200nm top p$^+$ Si layer (4×10^{19}cm^{-3}) was grown subsequently at 750^{o}C. For vertical p-channel MOSFET with wide silicon mesa (as in Chapter 5, d$\geq$ 20μm), the channel has to be doped in order to suppress punch-through in the center of the mesa.

The epitaxial temperatures for all the layers above the bottom p$^+$ region were controlled below 800^{o}C to control dopant diffusion during epitaxy. In our growth system, using 26sccm DCS as silicon source at 6torr, the growth rate of silicon obeys an Arrhenius relationship with an activation energy of 1.9eV [124]. A typical growth rate at 700^{o}C is 30Å/min and 250Å/min at 800^{o}C. Most substitutional dopants (e.g. boron and phosphorus) in silicon diffuse with an activation energy of 3$\sim$5eV. Thus lower temperature (although longer growth time) can reduce dopant thermal diffusion. Fig. 3.22 gives the Tsuprem[126] simulation

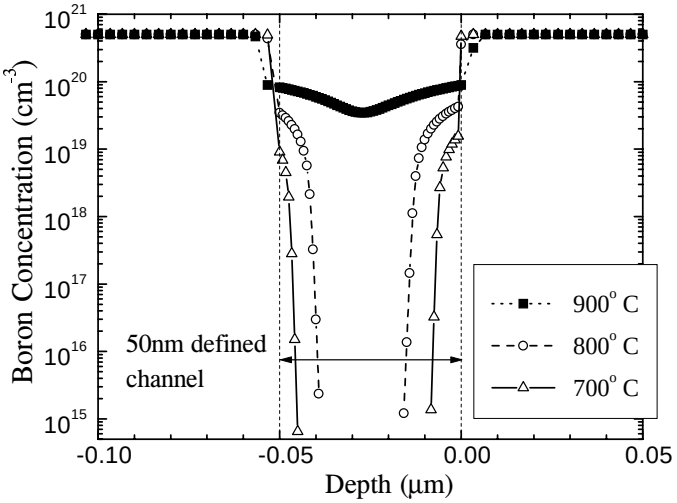


Figure 3.22: Tsuprem4 simulation of boron thermal diffusion during epitaxy. Diffusion coefficients of an inert ambient (N_2) were assumed during epitaxy. The growth takes place at 6torr with 26sccm DCS. The growth rate obeys an Arrhenius function with an activation energy of 1.9eV.

result of boron thermal diffusion during epitaxy at various growth temperatures. It shows that 800^oC is the upper limit at which to grow well-resolved structures with a 100Å scale. Thus to achieve vertical MOSFET's with sub-100nm channel length (especially p-channel), the epitaxy temperatures are controlled less than 800^oC.

To obtain an abrupt transition of the phosphorus profile, simply lowering the epitaxy temperature is not enough. In conventional low pressure CVD systems, phosphorus profiles always have a long tail after the phosphine gas is turned off. Chapter 4 will discuss the improvements in this work concerning phosphorus doping profiles.

For vertical MOSFET's using "epitaxy" to define the channel length, the epitaxial layers are usually grown before the gate oxidation and other high temperature processes (i.e. implantation annealing). In Chapter 5, the post-epitaxy dopant diffusion problem will be addressed.

3.3.2 Side-Wall Gate Oxide

(I) Side-Wall Orientation Effect

All the vertical p-channel MOSFET's using the "planar epitaxy" approach in this thesis are fabricated on the side-wall of nominally (110)-oriented surfaces. The optical lithography for the Si mesa RIE is aligned along [110] rather than [100] crystal directions on the (001) Si substrate, as illustrated in Fig. 3.23. Because the oxidation rate depends on crystal orientation, the side-wall gate oxide thickness is estimated by measuring the oxide grown under identical condition on planar (110) Si wafers. Since the dimension of the Si mesa is $\geq 20\mu m \times 50\mu m$ for the actual devices , 2-dimensional effects on the oxide thickness on the side-wall can be ignored. An oxidation rate enhancement of 60-80% on (110) vs. (100) Si surfaces has been reported in the thin oxide regime by dry oxidation at 800^OC [127]. We studied 750^oC wet oxidation on (100) and (110) n^- Si wafers. Oxide thicknesses derived from capacitance-voltage measurement (and confirmed by ellipsometry) are plotted in Fig. 3.23. In the thin gate oxide region (< 200Å), the wet oxidation rate of (110) surface is 2.2 times faster than that of (100) surface at 750^oC. The reported side-wall gate oxidation thicknesses in Chapter 5 were estimated using Fig. 3.23 to convert control oxide thickness on (100) surfaces grown simultaneously with the sidewall oxides to (110) sidewall oxide thickness. Because the (110) surface has a higher interface density than (100) surface, (110) side-wall is not an ideal surface for the channel. Future work on vertical MOSFET's will be concentrated on the (100) side-wall instead.

(II) Gate Oxide Quality on the Side Wall

After the Si pillar was created by RIE, 10nm of sacrificial oxide was grown and stripped off in diluted HF to provide a smoother side wall. Both sacrificial and gate oxides were grown at 750^oC in wet oxygen. Gate oxide was annealed in N_2 for 20min before 150~200nm p^+ poly-Si deposition to improve interface quality. 100sccm SiH_4 (10% in Ar) and 100sccm B_2H_6 (120ppm in H_2) were used as silicon and boron sources. The deposition temperature was 700^oC. Poly-Si gate was then patterned by RIE using 25sccm SF_6 and 1.5sccm CCl_2F_2

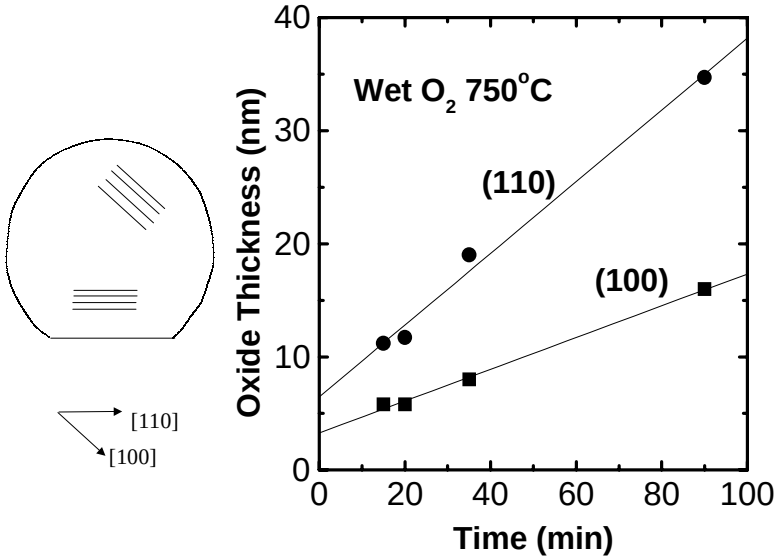


Figure 3.23: (a) Lithography alignment for silicon mesa using the "planar epitaxy" approach for vertical p-channel MOSFET's. (b) SiO_2 thicknesses on (110) and (100) n^- silicon substrates after 750^oC wet oxidation.

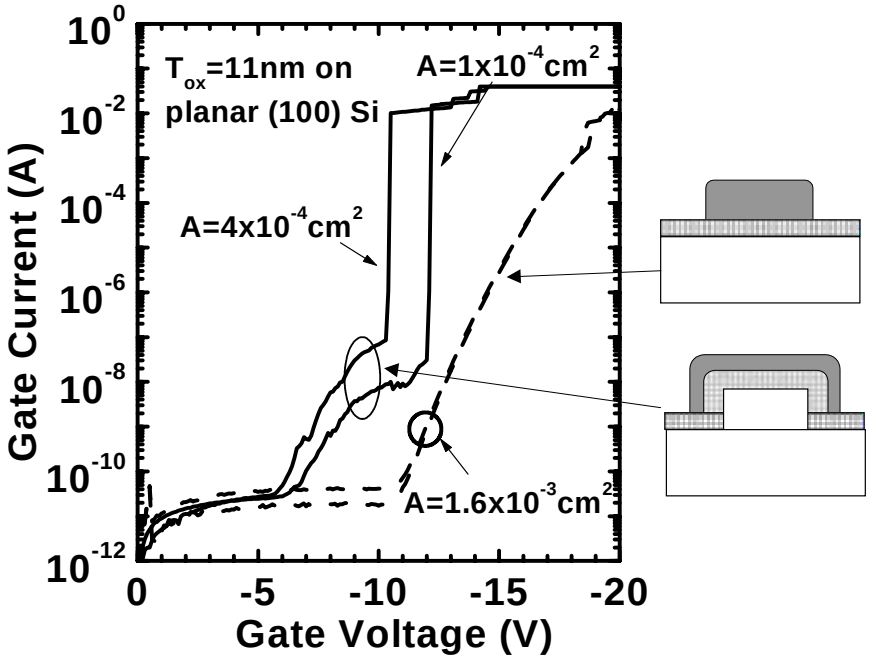


Figure 3.24: Gate leakage current from a MOS capacitor across the (110) side-walls. A reference MOS on a planar Si (100) substrate made simultaneously is also shown.

at 150mtorr and 0.2watt/cm^2. Details of poly-Si deposition and RIE conditions have been described in Sec. 3.2.3 and Sec. 3.2.4. The MOS capacitors across the mesa structure were then completed after the addition of the metal contacts on the front and back of the wafer. MOS capacitors were also simultaneously made on a (001) Si substrate for reference. The gate leakage currents are shown in Fig. 3.24. The gate oxide thickness on the (001) Si substrate is 11nm. Because the side-walls are created by RIE and the surface is relatively rough, and because a high electrical field is located at the mesa corners, a lower oxide breakdown voltage than on the control (100) Si substrate is found, although thicker gate oxide is expected on the (110) side wall. However, in the MOSFET's operation range ($|V_{GS}|$ <5V), the gate leakage current is as low as the reference sample, and both are low enough ($< 6 \times 10^{-7}$watt/cm^2) to meet the requirement of stand-by power consumption.

3.3.3 Spin-on-Glass and End Processing

After poly-Si etching, an insulation layer is needed before metallization. As indicated in Sec. 3.2.4, SiO_2 deposition techniques other than plasma enhanced CVD should be employed to avoid degradation of the thin gate oxide on the exposed edges. Low temperature CVD oxide or polymer are feasible alternatives. To minimize dopant diffusion after epitaxy, spin-on-glass is used as an insulation layer in the vertical MOSFET's in this thesis. The spin-on-glass used here is Methylsiloxane 500F from Filmtronics Inc., with 500nm single coat thickness and 14.5% organic content. The process procedure is [128]:

Spin coat: Spin at 3000rpm for 10sec. Then reduce to 1500rpm for 10sec, blow N_2 to enhance the solvent evaporation. Finally, increase to 3000rpm for another 10sec.

Hot plate bake: Bake at 65, 155, and 255^{o}C for 1min, respectively, and cool down to room temperature.

Cure: Anneal in furnace with N_2 at 400^{o}C for 1hr.

After the high temperature cure, the dielectric constant of this type of spin-on-glass is 3.0, much lower than that of thermal SiO_2. The leakage current through this insulator is

less than 1nA/cm^2 for bias below 20V and its breakdown voltage is greater than 50V.

Spin-on-glass can also smooth the topology of the vertical MOSFET's. With a one layer coating, the 0.75μm deep and 3μm wide trench is reduced to a 0.35μm high step, and can be further reduced to 0.1μm after applying 3-layers, shown in Fig. 3.25. A similar effect is also observed on the mesa structure made from image reversal during lithography. Fig. 3.25c shows the cross-section SEM of a 3μm wide mesa with 0.3μm high step after 1-layer of spin-on-glass is applied.

The remaining process steps for vertical MOSFET's with wide mesa using the "planar epitaxy" approach are described as the following. Spin-on-glass is patterned using photo lithography and etched in BOE. Hot HMDS (Hexamethyl-disilazane) is needed to enhance the adhesion of photoresist to the spin-on-glass. The etching rate of the spin-on-glass in BOE depends on the organic content in the material, but is typically 70nm/min in BOE(6:1). To thoroughly remove the residual organics in the contact window, a low power (0.02watt/cm^2) RIE with 25sccm SF_6 and 1.5sccm CCl_2F_2 at 150mtorr is used to remove 300Å of Si inside the contact window. After the photoresist is removed sequentially by solvents (Acetone, Methanol, and Isopropanol), the sample is cleaned in H_2SO_4+H_2O_2. 3000$\sim$5000Å of Al is then deposited after a brief HF dip. No annealing is done after metallization in this work to avoid possible junction spiking from Al.

3.3.4 Process Modification for the Fabrication of the Vertical DG-MOSFET's with an Ultra-thin Pillar Using "Planar Epitaxy"

The fabrication of vertical MOSFET's on the side walls of wide mesa has been proposed using "planar epitaxy". Key process steps have been developed. Vertical p-channel MOSFET's and n-channel MOSFET's using this approach will be demonstrated in Chapters 5 and 6. As mentioned earlier, in this wide mesa structure, the two channels are independent of each other and the mesa is not depleted during the operation. This structure is only used to study device scaling ability in the vertical structure. To eventually eliminate the short channel effects, double-gate MOSFET's with ultra-thin pillars are preferable for sub-100nm channel lengths. After short channel vertical MOSFET's are achieved on the side walls of

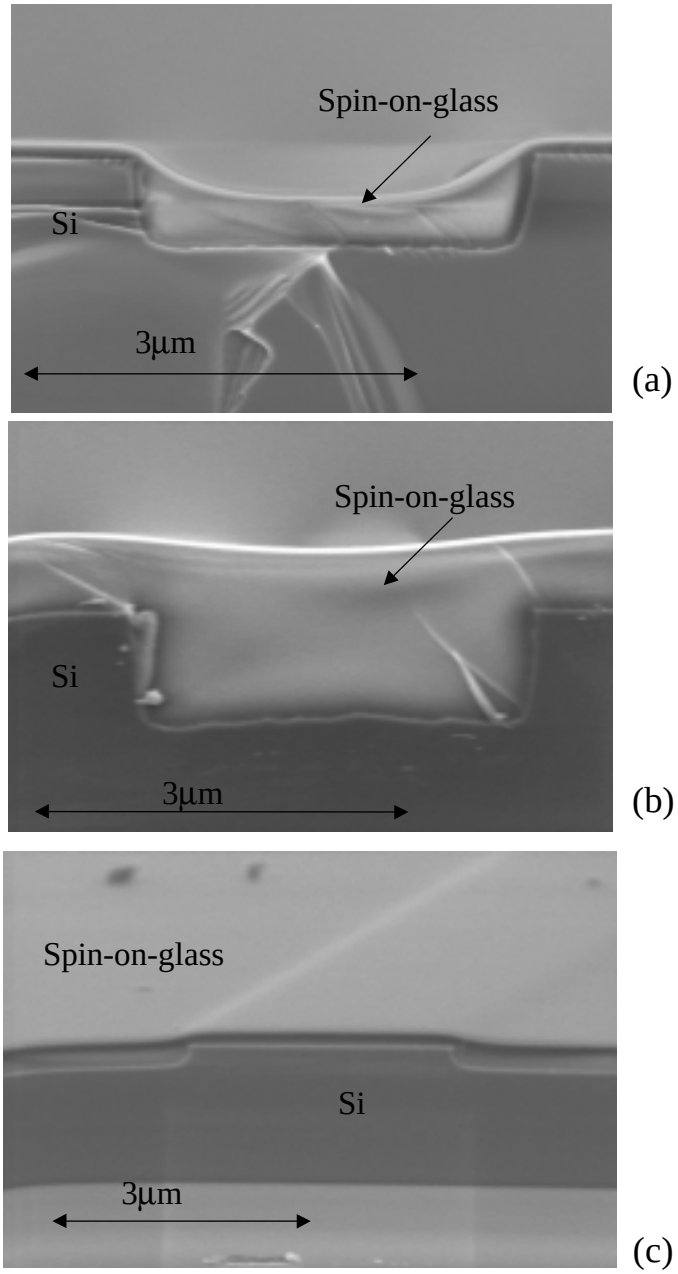


Figure 3.25: Cross-section of a 3μm wide trench with 0.75μm step after applied (a) 1-layer, (b) 3-layers of spin-on-glass. (c) Cross-section of a 3μm wide mesa with 0.3μm step after 1-layer of spin-on-glass.

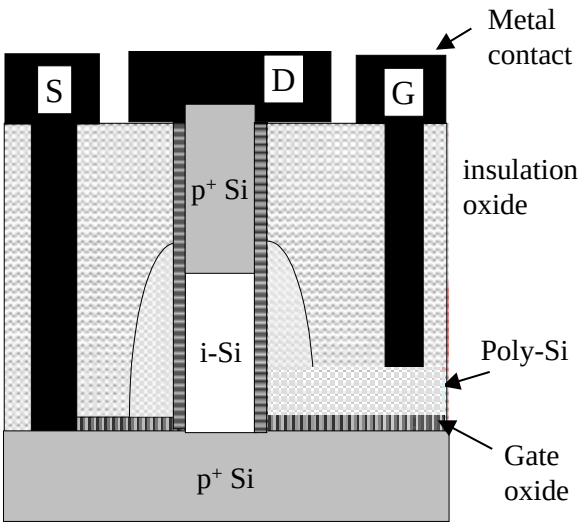


Figure 3.26: Schematic of the cross-section of a vertical double-gate MOSFET using the "planar epitaxy" approach.

wide mesa, some of the process steps discussed in this section may be modified to fabricate double-gate MOSFET's, using a similar approach.

First, the doping in the channel region during the planar epitaxy may be omitted for double-gate structures. Second, E-beam lithography and a high Si anisotropic etching will be used to create an ultra-thin pillar. Third, the polysilicon side gates will be formed and recessed using a spacer etching technique. Lastly, the top contact will be completed by a planarization step. The finally structure is shown in Fig. 3.26.

3.4 Fabrication of Vertical Double-Gate MOSFET's Using "Selective Epitaxy"

Using the "planar epitaxy" approach to fabricate double-gate MOSFET's with an ultra-thin pillar, the gate is not self-aligned with the source and drain. It is also difficult to control the poly-Si gate recess depth. Thus another approach using "selective epitaxy" to form the vertical pillar is proposed here to fabricate the vertical double-gate MOSFET's. The processing steps using "selective epitaxy" are shown in Fig. 3.27. Only p-channel MOSFET's

are demonstrated here, however, the same procedure can be applied to n-channel.

Step 1: A small window is opened in the SiO_2 grown on a p^+-Si(100) substrate, using electron-beam lithography and RIE etching. The width of the window (d) defines the thickness of the vertical double-gate MOSFET's shown in Fig. 3.1, and should be $\ll$100nm according to the simulations in Chapter 2 to achieve better gate control for channel length less than 0.1μm.

Step 2: After cleaning, p^+ip^+ silicon layers are selectively grown through the seed-window. The top p^+ layer is laterally grown over the top of the oxide which defines the seed-window. The reason for the lateral over-growth is given in Step 5. The channel length (L) is defined by the distance between the two p^+ silicon epi-layers.

Step 3: Remove the SiO_2 selective epitaxy mask. Thus a "mushroom" structure is formed.

Step 4: Sacrificial oxide is grown and stripped off to create a smooth side wall. Gate oxide is then grown and followed by polysilicon deposition. Poly-Si deposition is conformal and it is thick enough so that the "over-hang" of the "mushroom" structure is filled up. The poly-Si under the "overhang" serves as gate material for the vertical MOSFET's. It is *in situ* doped, because implantation and annealing may have difficulty driving the dopant atoms laterally far enough to reach the gate oxide interface to avoid gate depletion problems.

Step 5: Polysilicon is anisotropically etched using the "overhang" as a self-aligned mask to reduce the gate overlap capacitance.

Step 6: Because the lateral size of the pillar is small, a self-aligned contact is needed for the top. A planarization method is needed here. For example, a thick spin-on polymer will help to smooth away the topology of the structure; then the polymer is etched down to expose the top contact.

Step 7: Finally metal is deposited and patterned. The cross-section of the device is shown in Fig. 3.28.

There are four lithography steps in this design, with the first step being E-beam lithography. A typical device layout is shown in Fig. 3.29. The first layer is used to etch windows

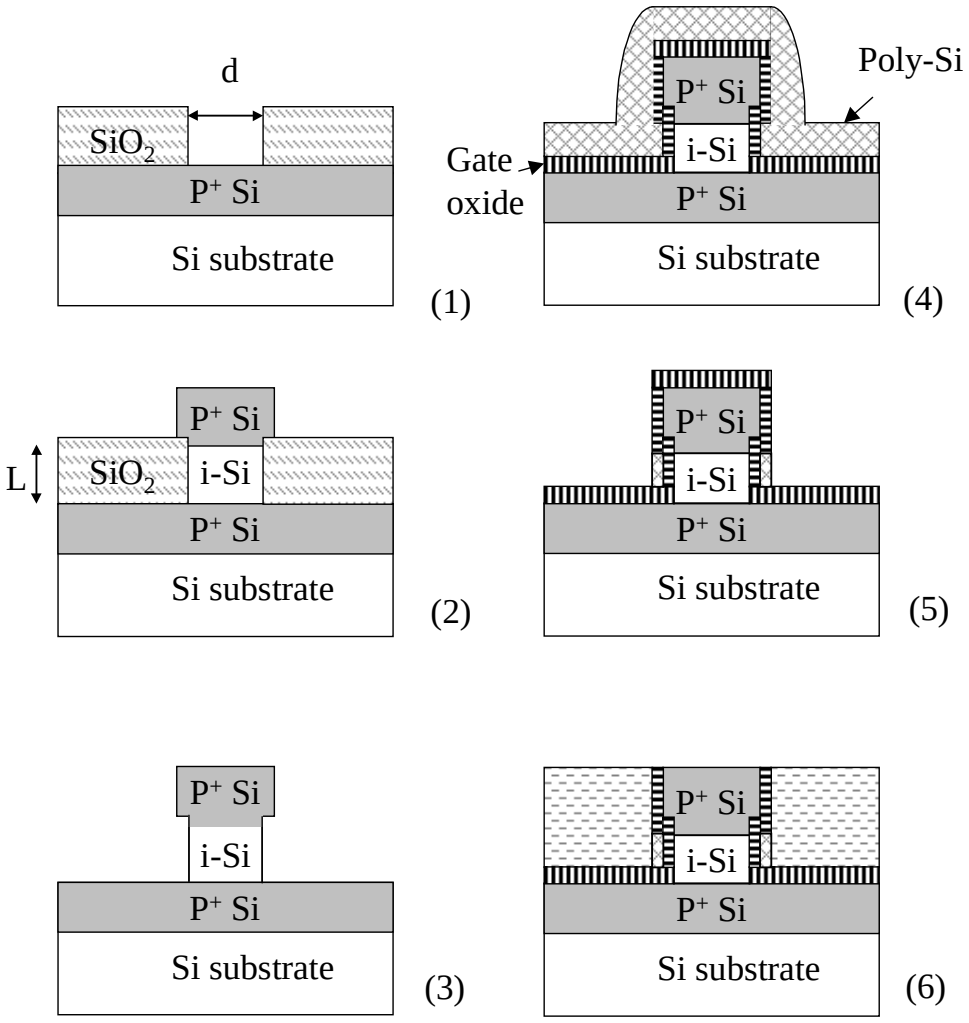


Figure 3.27: Process design for vertical double-gate p-channel MOSFET's using "selective epitaxy" to form the vertical pillar.

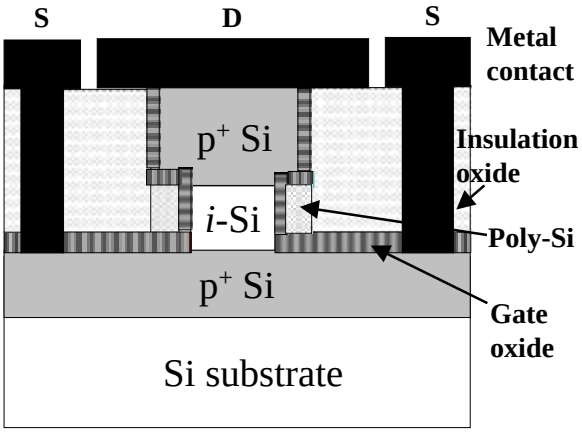


Figure 3.28: Cross-section of a vertical p-channel double-gate MOSFET using the "selective epitaxy" approach.

in SiO_2 for selective epitaxy. The second layer is for poly-Si gate contact pads during self-aligned etching. Contact windows through the insulation polymer for bottom p^+ Si and poly-Si gate are on the third layer. The final lithography is used to pattern the metal. In this design, the gate overlap capacitance is minimized by self-aligned poly-Si etching using the "mushroom" structure created by selective epitaxy. However there are several challenging technologies: anisotropic etching of SiO_2, selective epitaxy, poly-Si gate self-aligned etching, planarization, etc. Each individual process step will be discussed in details which follow.

3.4.1 Silicon Selective Epitaxy by RTCVD

The difference between selective epitaxy and two-dimensional planar epitaxy is that in selective epitaxy, crystalline silicon is grown only in the openings etched through a masking dielectric layer (often SiO_2), as illustrated in Fig. 3.30. When the epitaxial layer is thicker than the masking SiO_2, lateral over-growth across the SiO_2 occurs. Usually HCl is added in H_2-SiH_4 or H_2-DCS systems to suppress the growth on the SiO_2. Due to the complexity introduced by corrosive HCl gas, only a DCS-H_2 gas mixture is used in thesis to study selective epitaxy. The reaction mechanism is well documented in the literature [129, 130, 131]. It is well known that DCS decomposes rapidly to form $SiCl_2$, and $SiCl_2$ is the primary

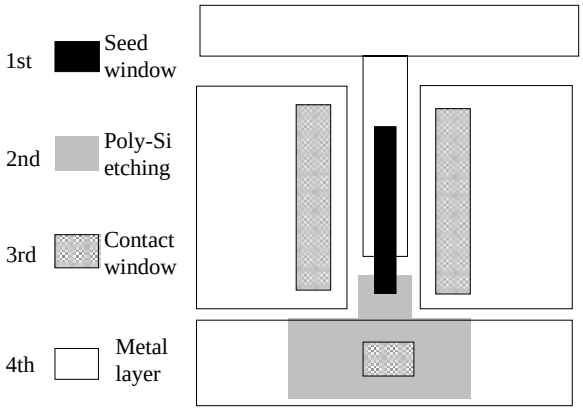


Figure 3.29: Layout of a vertical double-gate MOSFET using the "selective epitaxy" approach. The stated channel length in electrical measurements is twice that shown in the layout due to the two-sides of the pillar.

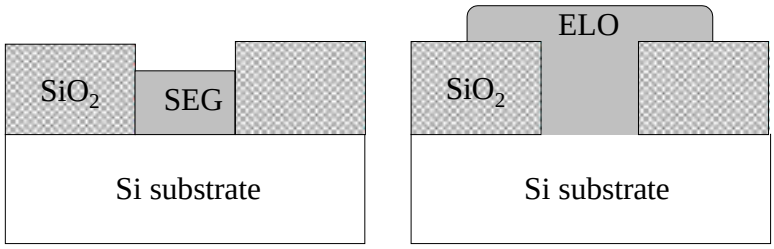


Figure 3.30: Illustration of (a) selective epitaxy growth and (b) epitaxy lateral over-growth.

species responsible for Si growth:

$$SiH_2Cl_2(g) \Rightarrow SiCl_2(g) + H_2(g) \tag{3.2}$$

$$SiCl_2(g) + s \Rightarrow SiCl_2 \cdot s \tag{3.3}$$

$$SiCl_2 \cdot s + H_2 \Rightarrow Si + 2HCl(g) \tag{3.4}$$

where s denotes an adsorption site on the silicon surface. It is shown that HCl is a by-product of the growth reaction and that silicon etching can take place by the reverse reaction of Eqn. 3.4. Fitch related that the etching of silicon nuclei by HCl can be a viable selectivity mechanism only at pressures $\geq$ 100torr and relatively high temperatures ($> 950^oC$) [131]. At low pressure and temperatures, a selective silicon growth requires low levels of H_2O and a high concentration of atomic H, which passivates the defects (nuclei) sites on SiO_2 surface.

In Sec. 3.3.1, it is shown that epitaxy temperatures should be controlled to $\geq 800^oC$ to minimize dopant diffusion during epitaxy. Therefore, to achieve selective growth at 6torr and less than 800^oC, the growth system has to be in high vacuum to keep out water vapor, as suggested by Fitch. Thermal oxide was used as the selective epitaxy mask in this thesis. The seed window was opened by chemical etching or RIE, with SiO_2 coverage of 99.5% of the surface area. The side-wall of the seed windows were aligned to [100] directions to reduce facet formation[132]. Before growth, the wafer was cleaned with H_2O_2+H_2SO_4 (1:2) and a standard RCA cleaning. Diluted HF dip, followed by an *in situ* bake at 900^oC and 250torr in H_2 for 2min, was used to remove residue SiO_2 in the seed-window. During growth, the DCS flow rate was 26sccm with 3slpm H_2 carrier, and the pressure was maintained at 6torr. Without adding HCl, up to 120nm of silicon has been selectively grown through SiO_2 windows. The 620nm thick SiO_2 mask for this sample was etched in BOE (NH_4F:HF). Fig. 3.31a shows that both the Si and SiO_2 surface after epitaxy are smooth and free of poly-Si dots. The sample was then dipped in defect-etchant (3g CrO_3+100ml H_2O +80ml 49% HF [133]) to test the silicon epitaxial layer quality. No pit or defect lines have been observed.

For thicker epitaxial layers, poly-Si dots are observed on top of the SiO_2 surface. Fig. 3.31b shows a sample after $\sim 2\mu$m epitaxy at 800^oC. However, the poly-Si dots on

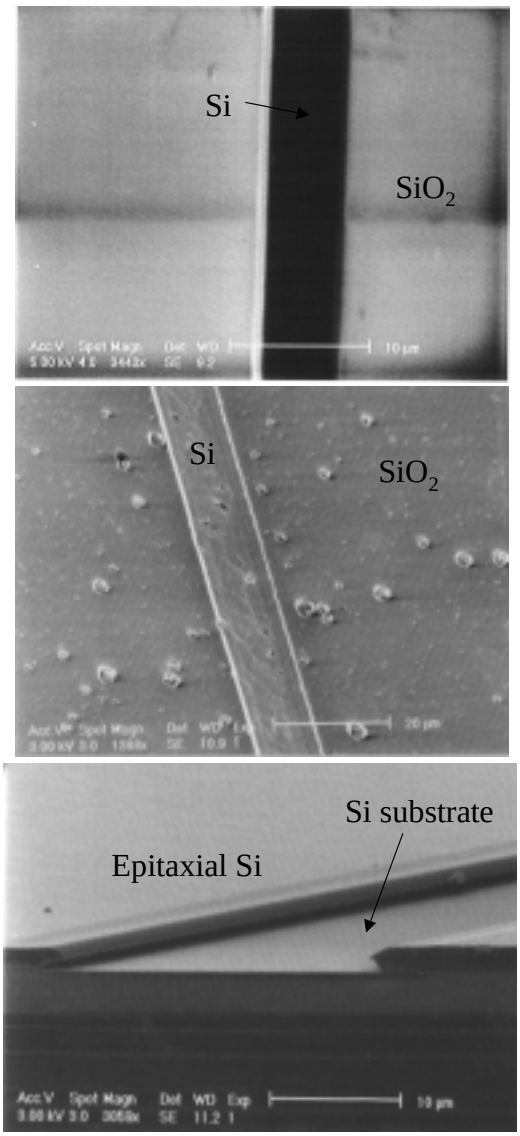


Figure 3.31: (a) Selective epitaxy up to 120nm is achieved through the SiO_2 seed windows, with oxide coverage of 99.5% of the surface. The dust on the left corner is used to focus the SEM picture. (b) Poly-Si dots are observed on SiO_2 surface after $\sim 2\mu$m thick epitaxy. (c) The poly-Si dots on the sample (b) can be removed along with the SiO_2 mask in BOE.

the SiO_2 surface can be removed along with the SiO_2 mask after BOE (NH_4F:HF=6:1) etching for 15min and ultrasonic cleaning in solvent, shown in Fig. 3.31c. The cross-section SEM after removing SiO_2 is given in Fig. 3.32a. Because the selective epitaxy mask is 900nm of SiO_2, lateral over-growth is observed for the 2μm silicon epitaxy. The ratio of lateral growth rate to vertical growth rate is $\sim$0.8. Note that the SiO_2 selective epitaxy mask was etched by BOE. Thus the side wall profile of the pillar is not vertical.

To further test the quality of the silicon film grown by selective epitaxy, MOS structure was made on top of a 300nm silicon epi-layer grown at 800^oC through a wet-etched SiO_2 mask on a p^- substrate, shown in Fig. 3.33a. After removing the 600nm thick SiO_2 mask and the poly-Si dots on the mask, 50nm sacrificial oxide was grown at 850^oC in wet oxygen and stripped off in diluted HF. 10nm gate oxide was then grown at 900^oC in dry oxygen and annealed in N_2 for 25min. After the Al gate and back contacts were made, the sample was annealed at 400^oC for 30min in forming gas. Because the silicon epitaxial layer is not intentionally doped, the depletion width is wide enough to extend deep into the epitaxial layer. No increase of gate leakage current is observed (Fig. 3.33b). The breakdown field is $\sim$15MV/cm. Fig. 3.33c gives the high/low frequency capacitance-voltage measurement of the MOS structure. Derived from the C-V curves, the background doping in the epitaxial-layer is $8\times10^{16}cm^{-3}$, and the interface density at midgap is similar to that seen for fabricated on the Si substrate in Fig. 3.2.

3.4.2 Gate Oxide on the Sidewalls of the Selective Epitaxial Layers

The thickness of oxides grown on the sidewalls could be different from those on the planar substrates because of different surface orientation. For the "selective epitaxy" approach, all the sidewalls are created along the (100) direction, as the selective epitaxy seed-windows are aligned along [010] and [100] directions on the (001) Si substrates. The gate oxide thickness on the side-wall is estimated using a planar Si (100) wafer oxidized simultaneously. If we were to have an ultra thin pillar, it would be necessary to re-calibrate the thickness of the side wall gate oxide as two-dimensional effect has to be considered.

Successful poly-Si deposition enables the processing of gate materials on the side wall.

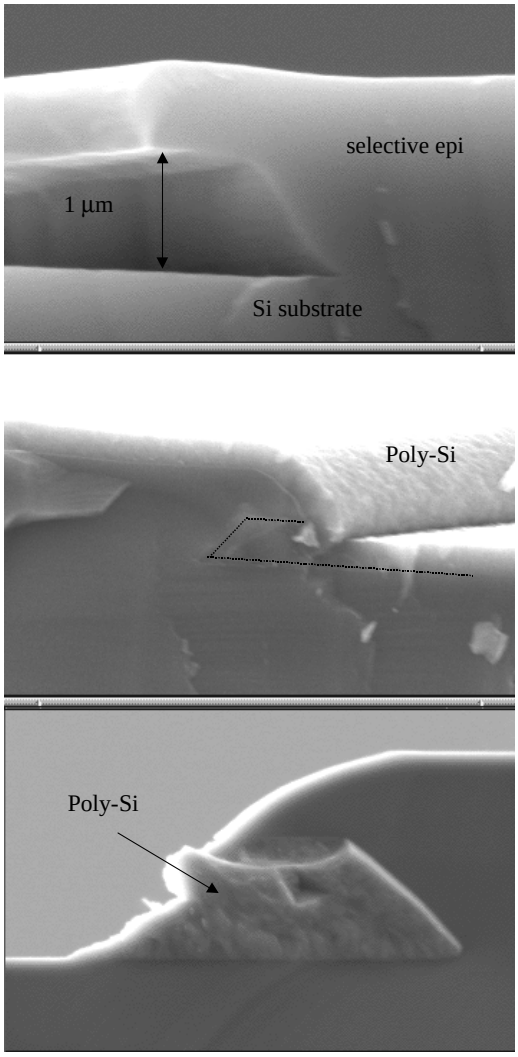


Figure 3.32: Cross-section SEM of a " mushroom" structure grown by selective epitaxy through a wet-etched oxide window (a) after SiO_2 removal, (b) after gate oxidation and poly-Si deposition, (c) after poly-Si self-aligned etching. The alignment of the seed-window is along [100] direction during lithography.

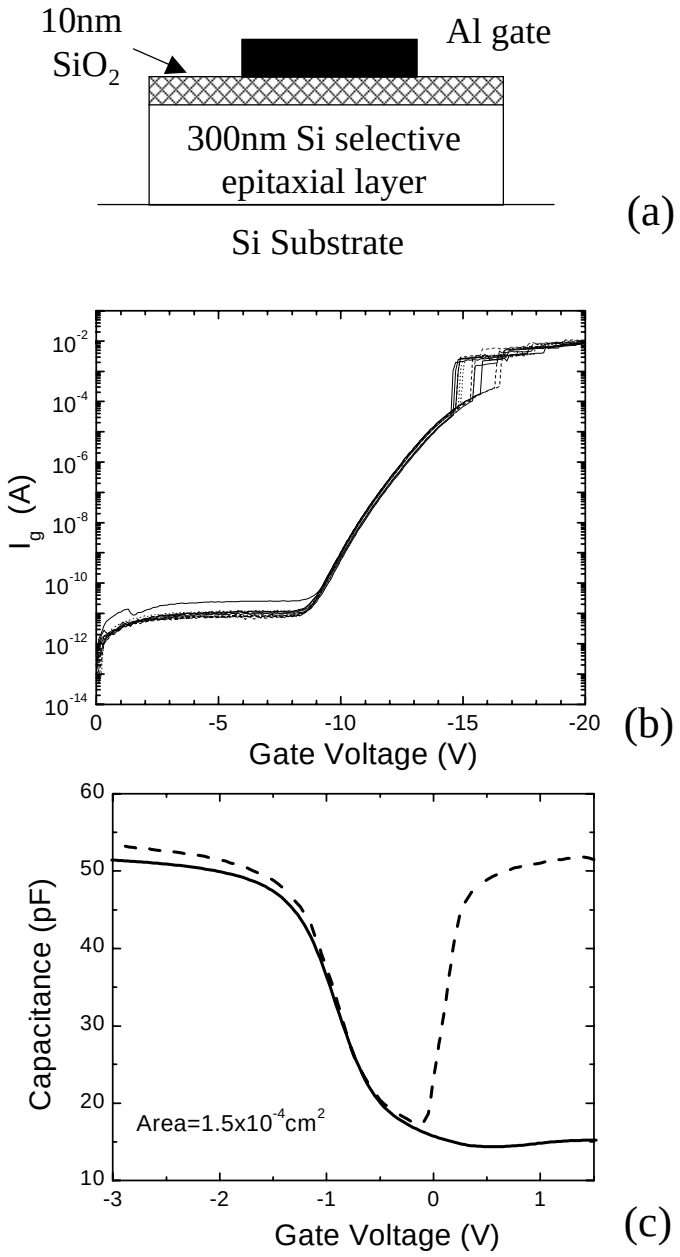


Figure 3.33: (a) MOS structure fabricated on a 300nm silicon epi-layer grown through a wet-etched SiO_2 mask. Al is used as gate material. (b) Leakage current and (c) high-low capacitance-voltage measurement of these MOS devices.

To test the side wall gate oxide, 45nm of sacrificial oxide was grown on the "mushroom" structure shown in Fig. 3.32a after poly-Si dot and SiO_2 mask removal. Gate oxide was then grown at 900^oC in dry oxygen to yield about a 10nm thickness on the control Si (100) substrate. However, due to the isotropic wet-etching of SiO_2, the sidewall of silicon epitaxy layers is mostly along [110] direction. The actual sidewall gate oxide may thus be thicker than 10nm. To fill up the "over-hang", 660nm of *in situ* doped p^+ poly-Si was then deposited (the epi-mask SiO_2 is 900nm thick). The SEM cross-section of the sample after poly-Si deposition is shown in Fig. 3.32b. A MOS device was then fabricated after patterning the poly-Si layer by wet etching. The schematic of the MOS is shown in Fig. 3.34a. A summary of the breakdown field of the side wall gate oxide is plotted in Fig. 3.34b. Due to possible thinner gate oxide and high electrical field on the corners, the average breakdown field is about 7.5MV/cm for the MOS with poly-Si gate covering over the "mushroom" structure. This value is less than that on the planar epitaxial-layer, but still higher than the vertical MOSFET's operating regime (<5MV/cm).

3.4.3 Poly-Si Self-Aligned Etching for Side Wall Gate Formation of Vertical Double-Gate MOSFET's

Using a highly selective poly-Si RIE, combined with interferometry for end-point control, poly-Si gate self-aligned etching is achieved using the "over-hang" from the selective epitaxy as an etching mask. Fig. 3.32c shows the SEM cross-section of the 2μm silicon epitaxial layer grown through a 900nm thick wet-etched SiO_2 window, after poly-Si self-aligned etching. The side wall p^+ poly-Si gate under the overhang remains while other parts were etched off. After using self-aligned etching, poly-Si gate covers fewer corners and higher gate oxide breakdown voltages are found than those without self-aligned etching, as shown in Fig. 3.35. The breakdown voltage with self-aligned poly-Si gate typically is 8V, for 10nm gate oxide measured on a (100) control sample. Although it is lower than the control device on (001) Si substrate (>12V) or on the planar epitaxial layer (>9V), the future devices will be operated below 5V. No increase of gate leakage current appears in this region for the MOS on selective epitaxial structures.

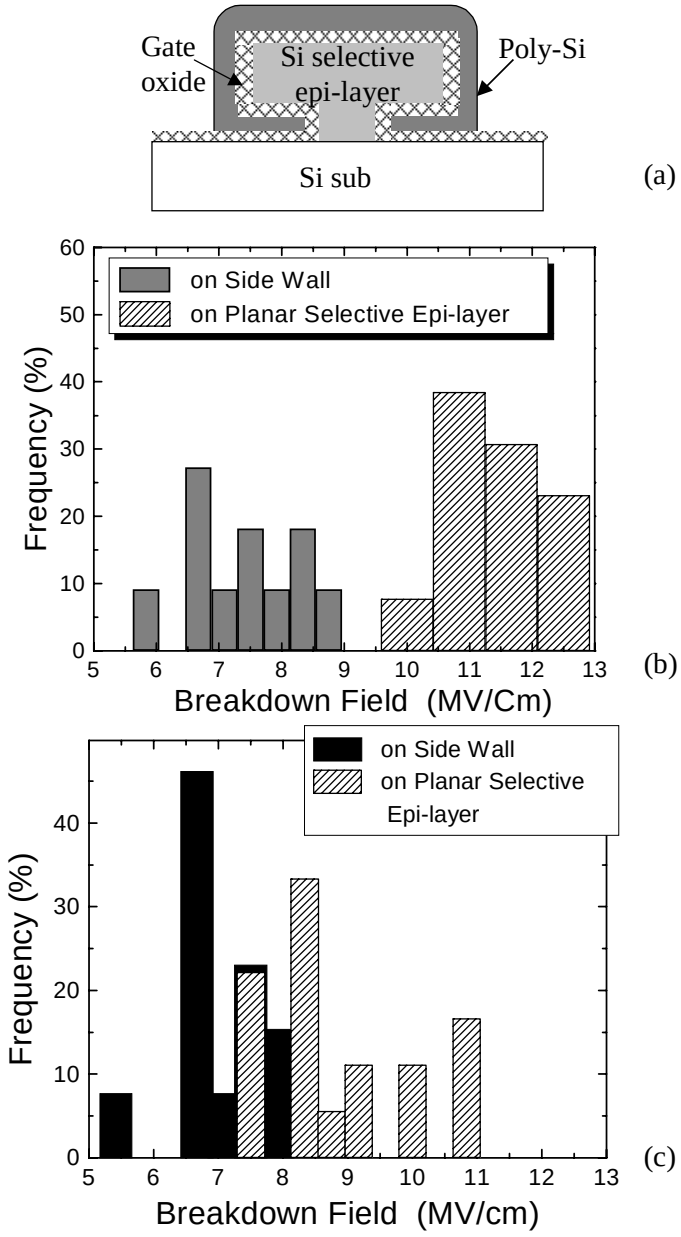


Figure 3.34: (a) Test MOS covering the "mushroom" structures grown by selective epitaxy. Breakdown field of these MOS using selective epitaxy through (b) wet-etched SiO_2, (c) dry-etched SiO_2 mask.

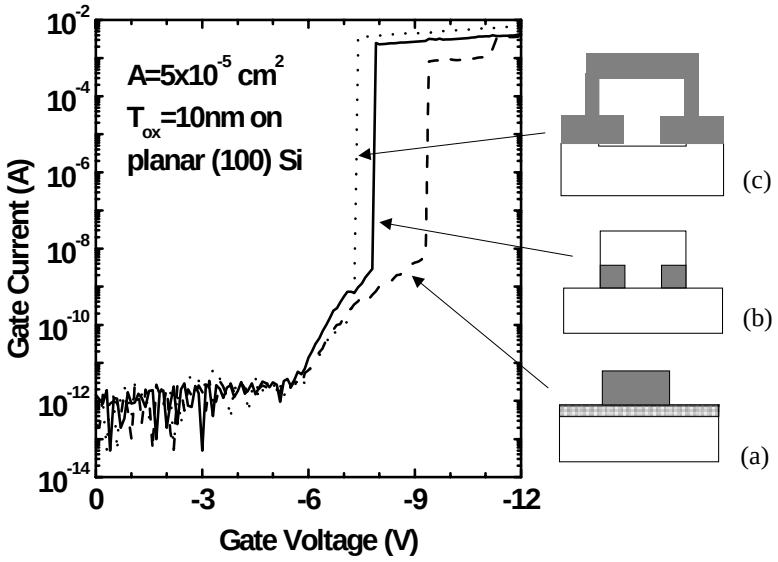
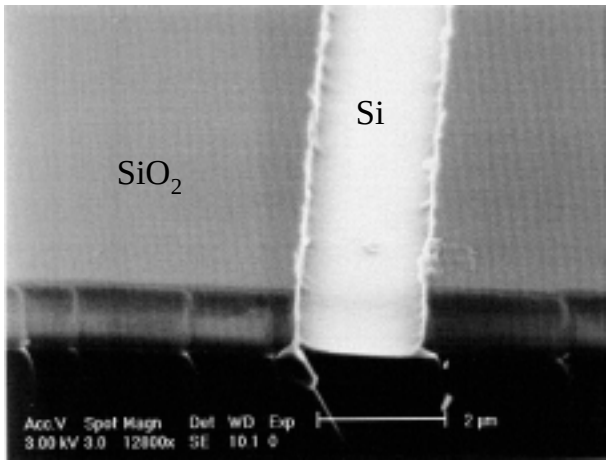


Figure 3.35: Gate leakage current measured from the MOS devices fabricated on (a) a planar selective epitaxial layer, (b) the "mushroom" structure in Fig. 3.32c after poly-Si self-aligned etching, and (c) the "mushroom" structure in Fig. 3.32b without poly-Si self-aligned etching.

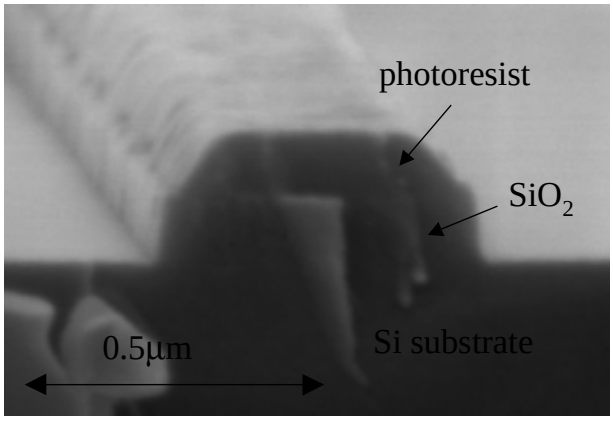
3.4.4 SiO_2 Anisotropic Etching

Reactive ion etching of SiO_2 in this thesis is performed in Plasma Therm VII model 790 with a 250cm^2 Al cathode. Fig. 3.36a shows a 750nm deep SiO_2 trench etched in 42sccm CF_4 and 9sccm H_2 at 200mtorr. The RF power density was 1watt/cm^2, giving a 480V self-bias voltage at the substrate electrode. Al and photoresist were used as etching masks. To reduce the sputtering of Al from the cathode, a Si wafer was used to hold the sample. H_2 was added to the CF_4 to achieve a high selectivity over Si and an anisotropic etching of SiO_2 [134, 135, 136], due to the formed fluorocarbon film [137, 138]. An anisotropic etching of the thermal SiO_2 at a rate of 88nm/min is achieved under our etching condition. The sample surface and trench bottom, after removing the mask, are very smooth, as shown in Fig. 3.36a.

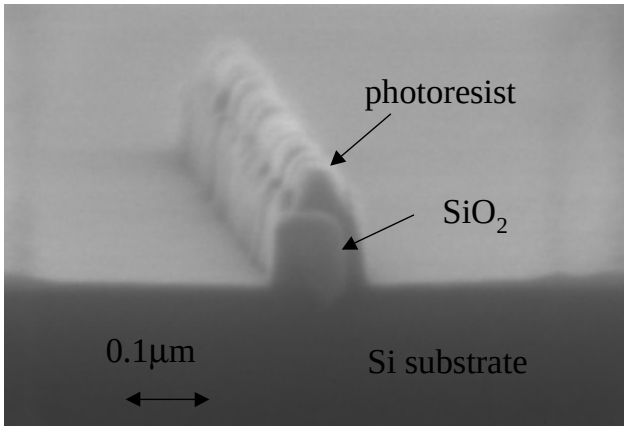
To grow epitaxial layers through the dry-etched SiO_2 window, the exposed silicon surface must be free of contaminations and roughness. To test the roughness after the SiO_2 RIE, two RCA cleanings were performed before a 10nm gate oxide was grown at 900^{o}C. Al contact



(a)



(b)



(c)

Figure 3.36: (a) 750nm deep and 2μm wide thermal SiO_2 etched by 42sccm CF_4 and 9sccm H_2 at 200mtorr and 1 watt/cm^2. (b) 0.5μm and (c) 0.1μm wide PECVD SiO_2 pillars (1000Å in height) etched by 5sccm CF_4 and 1sccm H_2 at 10mtorr and 0.14watt/cm^2.

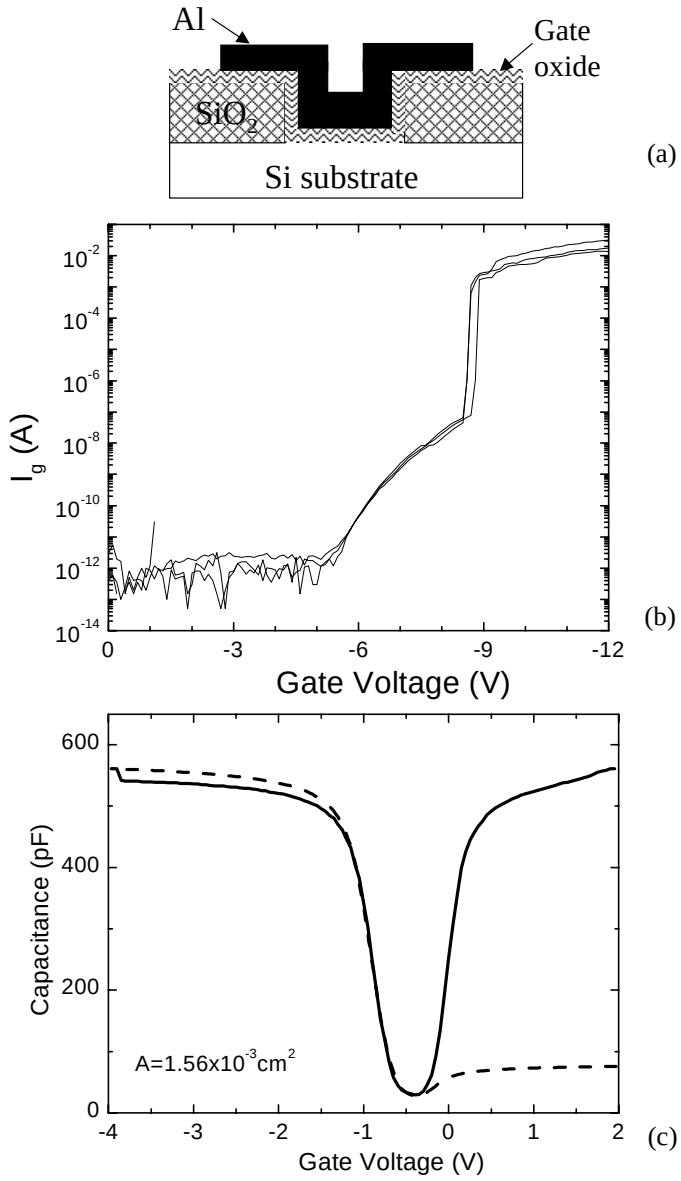


Figure 3.37: (a) Test MOS structure with the gate oxide grown in the dry-etched SiO_2 window. (b) Gate leakage current and (c)high-low capacitance-voltage measurement on the MOS structure.

was then put on the front and the back of the sample to finish a MOS structure (Fig. 3.37a). The D_{it}(midgap) obtained from the capacitance-voltage measurement is $\sim 10^{10}\text{cm}^{-2}\text{eV}^{-1}$, similar to the control sample on a flat Si substrate. However, the breakdown voltage is lower (8MV/cm in Fig. 3.37b), which indicates that the surface of the silicon inside the SiO_2 is relatively rough after a high power RIE.

The silicon surface after epitaxy may provide a smoother surface, but its quality may depend on the silicon surface in the seed-window. To test the epitaxial layer quality, about 1μm silicon layer was grown using a dry-etched SiO_2 as selective epi-mask. After etching the 600nm thick oxide by RIE, a sacrificial oxide of 45nm was grown and stripped off in diluted HF to smooth the exposed Si surface. After selective epitaxy, a "mushroom" structure was formed after removing the SiO_2 mask, similar to the one in Fig. 3.34a. A test MOS capacitor was made covering the side walls of the "mushroom" structure. The gate oxide was about 10nm thick, grown at 900^oC in dry oxygen. The poly-Si gate was wet-etched as in Sec 3.4.2. The breakdown field of the MOS devices on the planar Si selective epitaxial layer, shown in Fig. 3.34c, was slightly lower than the those grown through wet-etched SiO_2. However, for MOS devices covering the sidewalls of the "mushroom", no obvious decrease of the breakdown field was observed, compared with those fabricated by using a wet-etched oxide mask in Fig. 3.34b.

To reduce the damage to the Si surface in the seed-window during SiO_2 etching, lower RF power was investigated. To achieve anisotropic etching, lower pressure was used to increase direct ion bombardment. Fig. 3.36(b) and (c) show 100nm high SiO_2 pillars with 0.5μm and 0.1 μm widths using E-beam resist as the etching mask. The SiO_2 was deposited by plasma enhanced CVD at 280^oC and 900mtorr using a mixture of 475sccm N_2O and 200sccm SiH_4. The SiO_2 RIE was performed in 5sccm CF_4 and 1sccm H_2 at 10mtorr. The RF power density was 0.14watt/cm^2, providing a self-bias of 240V. Using this low power for SiO_2 etching, the silicon substrate is expected to exhibit less damage during the over-etch. Further study is needed to confirm these results.

3.4.5 Planarization

Planarization is proposed to expose the top Si pillar to provide a self-aligned contact for vertical double-gate MOSFET's, with pillar widths of $\ll 0.1\mu$m. Here polymer BCB3022-35 from the Dow Chemical Company was used, with an adhesion material AP8000. Thicknesses of 1μm can be obtained using 5000rpm spin-coating technique, followed by a 75^oC hot plate bake for 2min. The polymer was then cure by rapid thermal annealing in forming gas (N_2 with 10% H_2) for 1min at 250^oC and 5min at 300^oC [139]. After curing, the top surface of a 5μm wide and 0.4μm high step is perfectly flat, shown in Fig. 3.38a. The polymer is then etched back in 22sccm CF_4 and 35sccm O_2 plasma at 40mtorr and 0.2watt/cm^2, with an etching rate of 150$\sim$200nm/min. Fig. 3.38b shows the cross-section of a 5μm wide mesa with 0.4μm step after the polymer is etched back. The underlying surface is exposed with a slight recess as designed.

While this "selective epitaxy" approach was developed for the double-gate devices with narrow pillars, the fabrication of narrow pillar devices with self-aligned gate and top drain contact was not fully implemented, but may be demonstrated in the near future using this approach and the key technologies which have been developed here.

3.5 Fabrication of Vertical Surrounding Gate MOSFET's

A slight revision of our design of vertical double-gate MOSFET's in the previous section could be used to fabricate vertical surrounding-gate MOSFET's. Other than the first E-beam lithography layer, only the contact protection mask during poly-silicon self-aligned etching (the 2nd layer) needs to be changed. The layout is shown in Fig. 3.39. Small square seed-windows would be opened into the oxide by E-beam lithography instead of a thin rectangle in Fig. 3.29. The distance between the adjacent squares has to be small enough ($< 400nm$) so that poly-silicon can easily fill up the region and connect the gates for the adjacent devices. Squares and lithography along [100] directions are preferable, because (100) side-wall has the lowest interface density. A cylindrical structure will not lead to a

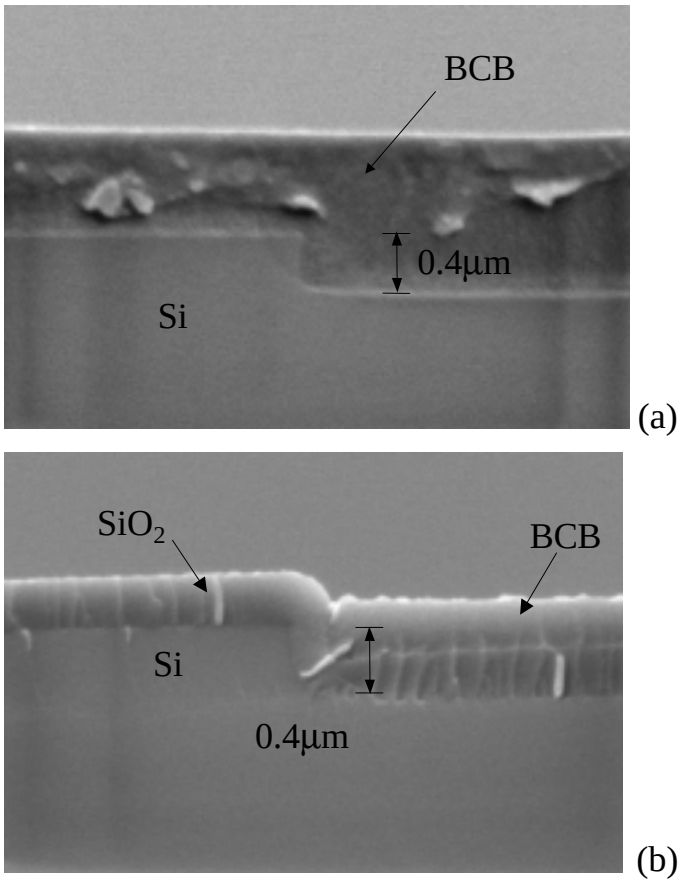


Figure 3.38: Cross-section SEM of a 5μm wide and 0.4μm deep step after (a) planarization with 1μm thick polymer, and (b) with polymer etched back in CF_4+O_2.

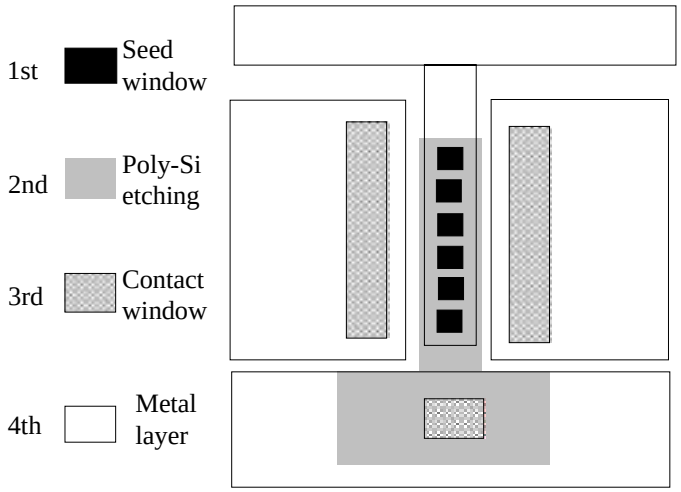


Figure 3.39: Schematic layout of vertical surrounding-gate MOSFET's. Only the first E-beam lithography and the 2nd poly-silicon etching protection mask are changed from those in the vertical double-gate structure in Fig. 3.29.

perfect channel and gate oxide interface [69]. Using the same selective epitaxy and over-lateral growth, a "mushroom" structure would be created through each of the seed-windows (Fig. 3.40a). After gate oxidation, a thick poly-silicon layer would be deposited to fill up the region under the "over-hang" and in between the silicon pillars. A planarization and polysilicon recess step would be added to create surrounding gates and expose the top of the "mushroom" (Fig. 3.40b). The second lithography step would be used to isolate the poly-silicon in the device region and create poly-silicon contact pads, using a protective mask. The subsequent processes are the same as those described in Chapter 3. In our design, all the surrounding-gate transistors along the line are connected in parallel and the drive current is correspondingly increased. Such devices are merely proposed here , however, the mask set has been designed. The fabrication may be carried out in the future.

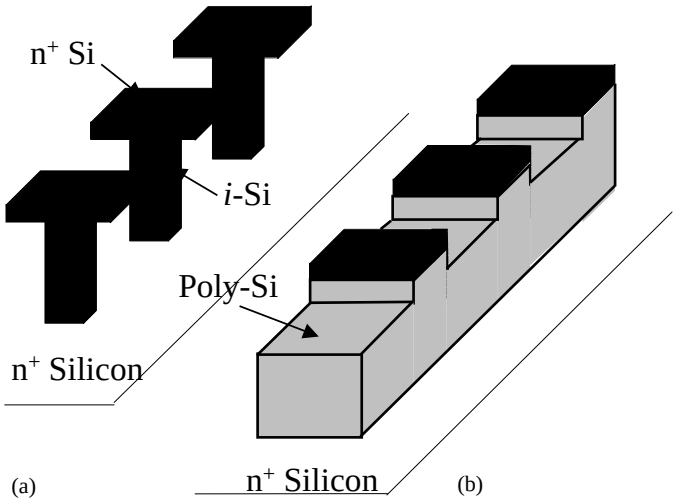


Figure 3.40: Process flow for vertical surrounding-gate transistors (SGT) (a) after selective epitaxy and over-lateral growth. "Mushroom" structures are formed through the seed-windows. (b) After gate oxidation and poly-silicon deposition, planarization is used to exposed the top silicon surface and recess the poly-silicon gates. All the SGT are in serial to increase drive current.

3.6 Alternative approach for the fabrication of vertical DG-MOSFET's using epitaxy

For the vertical MOSFET's fabricated on the side-walls of wide mesa using "planar epitaxy" approach, the poly-silicon gates are not self-aligned with the source/drain in this work. The overlap capacitance degrades the device performance. The "selective epitaxy" approach proposed in this chapter provides self-aligned poly-silicon gates, and thus should be used instead. There are other approaches to the fabrication of vertical MOSFET's using epitaxy to define the channel length and have reduced gate overlap capacitance. Fig. 3.41a details the schematic of the main process steps used by Moers and Klaes *et al.* [106, 140, 141]. The main idea is to grow the poly-silicon layers in between two thick oxides first. The sandwiched layers are then patterned. Gate oxidation is done and seed-windows are cleaned up using anisotropic RIE before the selective epitaxy. Selective silicon source/chanel/drain are grown through the holes between the sandwiched layers. In addition to the reduced gate overlap capacitance on the source/drain, this design also reduces the

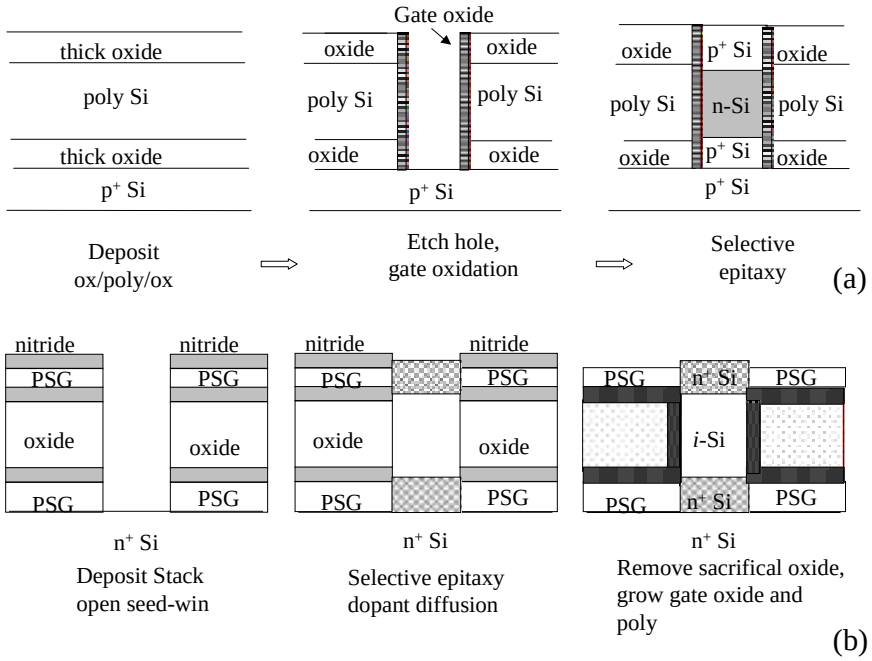


Figure 3.41: Schematic of the main process steps used by (a) Moers and Klaes *et al.* [106, 140, 141] and (b) Hergenrother *et al.* to reduce the gate overlap capacitance.

dopant diffusion in the epitaxial layers. However, the gate oxide is exposed to the epitaxy process, especially the *in situ* high temperature cleaning in hydrogen (usually $\geq 900^o$C). This leads to a problem in fabricating high quality thin gate oxide on the side wall. So far only vertical devices on a wide mesa have been reported using this approach.

Hergenrother *et al.* [86] improved the Moers and Klaes *et al.* idea by introducing a PSG/nitride/oxide/nitride/PSG/nitride stack on n^+ silicon instead of a oxide/poly/oxide stack. The vertical pillar is grown by selective epitaxy through a seed window opened through the stacked layers. The dopant in the PSG layers are diffused into the pillar during epitaxy or during the annealing afterwards. The oxide and nitride layers are then stripped away. Gate oxide and poly-silicon side gates are then grown and filled into the previous sacrificial oxide region. The main process steps are shown in Fig. 3.41b. In this design, the channel length is determined by the sacrificial oxide and nitride thicknesses and the control of dopant diffusion in the high temperature process. The channel thickness is defined by lithography and RIE during the seed-window formation. Gate overlap capacitance is

reduced due to the thick PSG layers.

3.7 Summary

Extensive generic silicon MOSFET process technologies developed in this work have been discussed in detail in this chapter. Two approaches "planar epitaxy" and "selective epitaxy" have been designed for the fabrication of vertical double-gate MOSFET's, using the epitaxy to define the channel length. Each approach has its own special techniques in addition to the generic steps. Vertical MOSFET's on the side walls of wide mesa are also designed and the "planar epitaxy" approach is used to create the mesa. Using "selective epitaxy", vertical double-gate MOSFET's on the side wall of thin Si "mushroom" structures can be made with self-aligned poly-Si gates. Key technologies involved with both of fabrication process have been developed. High quality, thin gate oxide with a low thermal budget ($700\sim750^{o}$C in wet oxygen) has been achieved. Selective epitaxy layers grown by RTCVD using DCS-H_2 has been obtained up to 120nm thick. Effects of poly-Si gate RIE on the thin gate oxide has been studied. Gate oxide degradation has been fully controlled using a highly selective RIE and an interferometric end-point monitor. Anisotropic Si and SiO_2 etching has been achieved for various feature sizes. Planarization, spin-on-glass, and other end-process steps have also been developed. Vertical MOSFET's using the "planar epitaxy" approach will be demonstrated in Chapter 5 and Chapter 6 for p-channel and n-channel devices, respectively. Vertical double-gate MOSFET's using the "selective epitaxy" approach are still under investigation.

Chapter 4

Phosphorus Doping and Extremely Sharp Phosphorus Profiles in Si and SiGe Epitaxy by RTCVD

Sharp transitions of dopant profiles between sources/drains and channels are necessary for short-channel devices. In vertical MOSFET's where the "epitaxy" approach to fabricate the silicon pillar (both the "planar epitaxy' and "selective epitaxy" methods) has been implemented, *in situ* doping during epitaxy is used to define the source/drain and channel regions. p-type doping by boron atoms has been well established, however, n-type doping by phosphorus or arsenic has always been a difficulty.

In this work, *in situ* phosphorus doping of silicon epitaxy from 700^oC to 1000^oC by low-pressure rapid thermal chemical vapor deposition (RTCVD) in a cold-wall system, using dichlorosilane as the silicon source and phosphine as the phosphorus source, has been investigated. At a high phosphine flow rate, the growth rate of silicon decreases dramatically (by $\sim$60%) and the phosphorus incorporation level reaches saturation. A significant persistence effect of phosphorus after shutting off the phosphine flow is observed. Sharper transitions and higher doping levels are observed in $Si_{1-x}Ge_x$ layers grown at 625^oC. An improvement of the phosphorus profile in silicon ($\sim$13nm/decade) is demonstrated by reactor cleaning and *ex-situ* etching of wafer surfaces during a growth interruption after phosphorus-doped

epitaxy. Offsetting the effects of the growth interruption, an *in situ* 800^{o}C bake at 10torr in hydrogen before re-growth can give an oxygen- and carbon-free interface without excessive dopant diffusion.

4.1 Introduction

Low-temperature ($\leq$ 800^{o}C) silicon epitaxy by chemical vapor deposition (CVD) has been applied to a variety of silicon devices. In contrast to boron doping in silicon with high concentrations (>10^{20}cm^{-3}) and sharp profiles (5$\sim$10nm/decade on both the leading and trailing edges)[142, 143], high concentration n-type doping with an abrupt profile has always been difficult. It has been reported that phosphine and arsine severely depress the silicon growth rate, and that residual dopant in the chamber and phosphorus segregation on the wafer surface can also cause an unintentional doping tail after the n-type dopant gas is turned off [144, 145, 146, 147, 148, 149, 150, 151, 152]. Most n-type doping studies employed silane or disilane as the silicon source gas. Dichlorosilane (DCS) n-type studies have not been widely reported in the literature. Although Sedgwick *et al.* [153, 154] reported that at atmospheric pressure growth rate enhancement and sharp profiles were achieved using dichlorosilane and phosphine/arsine, it is well known that using dichlorosilane or other chlorine-containing sources at low temperatures (600^{o}C$\sim$800^{o}C) in low-pressure CVD (LPCVD) leads to similar problems as silane and disilane [155, 156, 157]. Recently, Churchill *et al.* [158] successfully grew arsenic modulation doping in Si/SiGe heterostructures by interrupting the SiGe growth while the surface was exposed to dopant gas and then resuming the growth, similar to what is described in Ref. [159]. The doping level was controlled by the exposure time, temperature, and dopant gas partial pressure. Ismail *et al.* used a growth interruption after n^+ silicon epitaxy by UHV-CVD [160] to improve the phosphorus profile. The main process included purging the system with hydrogen after shutting off the phosphine flow meanwhile removing samples from the growth chamber and etching them in diluted HF prior to reloading. However, the interrupted growth caused an oxygen spike at the interface [161], limiting potential device applications.

In this chapter, we present experimental results of *in situ* phosphorus doping in both Si and $Si_{1-x}Ge_x$ epitaxial layers grown by RTCVD using DCS at temperatures of 625∼800^{o}C. Similar to the growth with silane and disilane, at a high phosphorus flow rate the growth rate is reduced and the level of phosphorus incorporation begins to saturate. Sharper profiles and higher phosphorus doping levels in $Si_{1-x}Ge_x$ samples are observed. Various surface treatments during the growth interruption for epitaxial silicon are studied in order to create sharp phosphorus profiles. We find that after etching 10∼50Å of surface away from the n^+ silicon epitaxial layer outside the growth chamber, the phosphorus profile improves from 155nm/decade in the untreated sample to 13nm/decade for the growth at 700^{o}C with a 5×10^{-4}sccm phosphine flow. Growth of a sacrificial wafer reduces the residual phosphorus in the growth chamber, improving the background doping from 10^{18}cm^{-3} to 10^{17}cm^{-3}. An *in situ* low temperature cleaning (800^{o}C) is used before re-growth. An oxygen- and carbon-free interface is thus achieved, enabling a wide variety of device applications.

4.2 Growth Rate and Phosphorus Levels

4.2.1 In Silicon Epitaxial Layers

n^+ silicon epitaxial layers were grown on (001) silicon substrates. Dichlorosilane (26sccm) and phosphine were used as the silicon and phosphorus sources. The phosphine was diluted to 100ppm in hydrogen, but the phosphine flow rates reported in this work are those of only the phosphine calculated from the measured flow rate of the diluted source and the source concentration. The growth pressure is 6 torr with a hydrogen flow of 3 slpm. A typical phosphorus doping profile without any growth interruption is plotted in Fig. 4.1. This profile was measured by secondary ion mass spectroscopy (SIMS) using a 3 keV Cs primary ion beam. The SIMS measurement errors in the depth scales and concentrations are in the range of 5-10% and 15-20%, respectively. Three all-silicon samples were grown at 700^{o}C, 800^{o}C, and 1000^{o}C, respectively, with constant dichlorosilane and hydrogen flow rates and constant temperatures and pressures for each sample. The phosphine flow was first turned on for a period of 1000sec at a flow rate of 5×10^{-4}sccm, and then turned off for 1000sec,

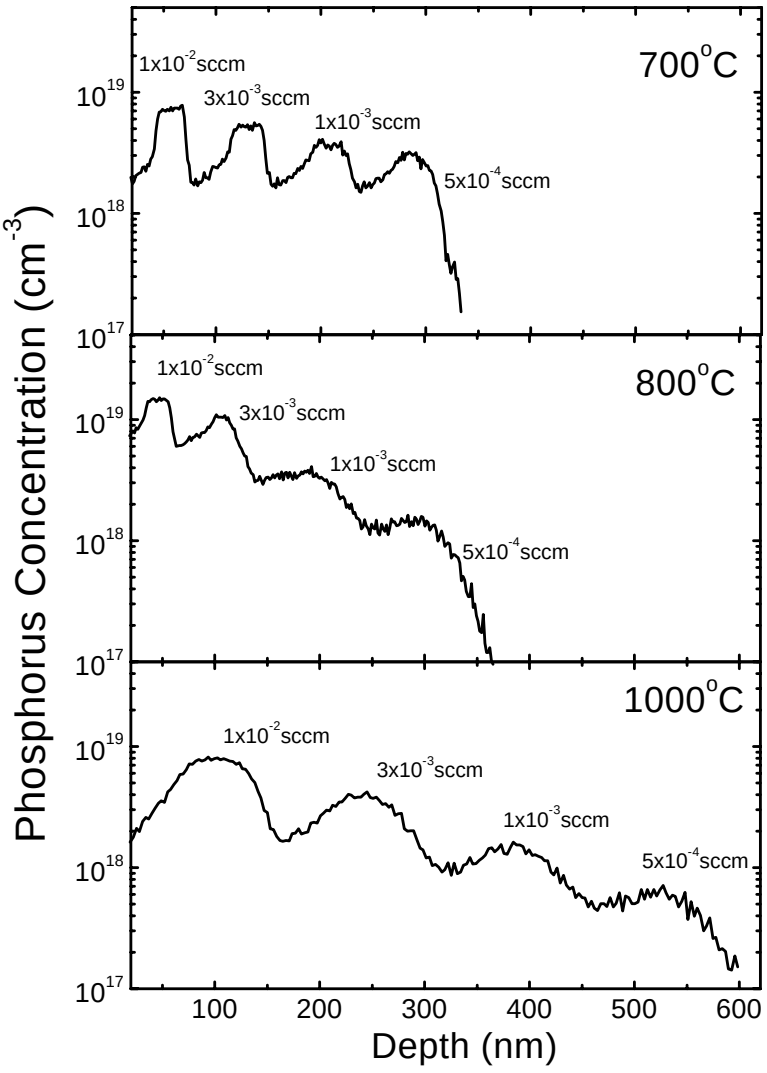


Figure 4.1: Phosphorus profiles from SIMS measurements for samples grown by RTCVD at 700^oC, 800^oC, and 1000^oC using DCS and PH_3. The PH_3 flow was switched on and off periodically, giving four peaks in each sample, corresponding to PH_3 flow rates of 5×10^{-4}, 1×10^{-3}, 3×10^{-3}, and 1×10^{-2} sccm.

with dichlorosilane on the entire time. This 1000sec-on/1000sec-off cycle was then repeated for phosphine flow rates of 1×10^{-3}, 3×10^{-3}, and 1×10^{-2}sccm. Identical experiments were conducted at 800^oC (with 90sec intervals) and 1000^oC (with 20sec intervals).

The silicon growth rate at 700^oC and 800^oC as a function of phosphine flow rate is plotted in Fig. 4.2(a). The silicon growth rate is reduced at a high phosphine flow rate by 60% for both 700^oC and 800^oC growth, which is qualitatively similar to the growth rates using silane or disilane sources in both chemical vapor deposition (CVD) and gas source molecular beam epitaxy systems [146, 148, 162, 147, 150, 107, 163, 164, 144, 152, 151, 165, 166, 167, 168, 169]. There are fewer works using dichlorosilane as the source, but similar phenomenon have been observed in both arsenic [155] and phosphorus [156] doping using dichlorosilane in silicon selective epitaxy at $775 \sim 1050^oC$. In the case of silane, the explanation given [145, 162, 170] is that at temperatures higher than 400^oC (the desorption temperature of hydrogen) phosphorus sticks tenaciously to the silicon surface and blocks all free surface active sites, thus reducing the surface reaction.

Fig. 4.2(b) shows the peak phosphorus levels observed by SIMS as a function of the phosphine flow rate for 700^oC, 800^oC, and 1000^oC growth temperatures. For the silicon layers grown at 800^oC and 1000^oC, the doping level varies linearly with the phosphine flow rate when the flow rate is low. At high phosphine flow, despite presumably high phosphorus levels on the surface (significantly depressing the growth rate), the amount of phosphorus incorporated is small ($1.4 \times 10^{19}\text{cm}^{-3}$ for 1×10^{-2}sccm at 800^oC), and the phosphorus doping level approaches saturation in contrast with other dopants such as boron. For silicon layers grown at 700^oC, the phosphorus concentration goes as the flow rate to the 0.3 power. In the case of silane, Yu *et al.* [171] reported that P_2 dimer formation upon increasing the phosphine concentration limits silane adsorption and prevents monatomic phosphorus incorporation into silicon, in spite of a high degree of surface coverage. P_2 dimer formation is still debatable in the literature[146, 172]. In the present work, for a phosphine flow rate less than 3×10^{-3} sccm, higher phosphorus incorporation is observed at a lower growth temperature. This is consistent with the trend reported in Ref.[150, 163, 173, 174, 175]. It has been suggested that this effect is attributable to the enhanced

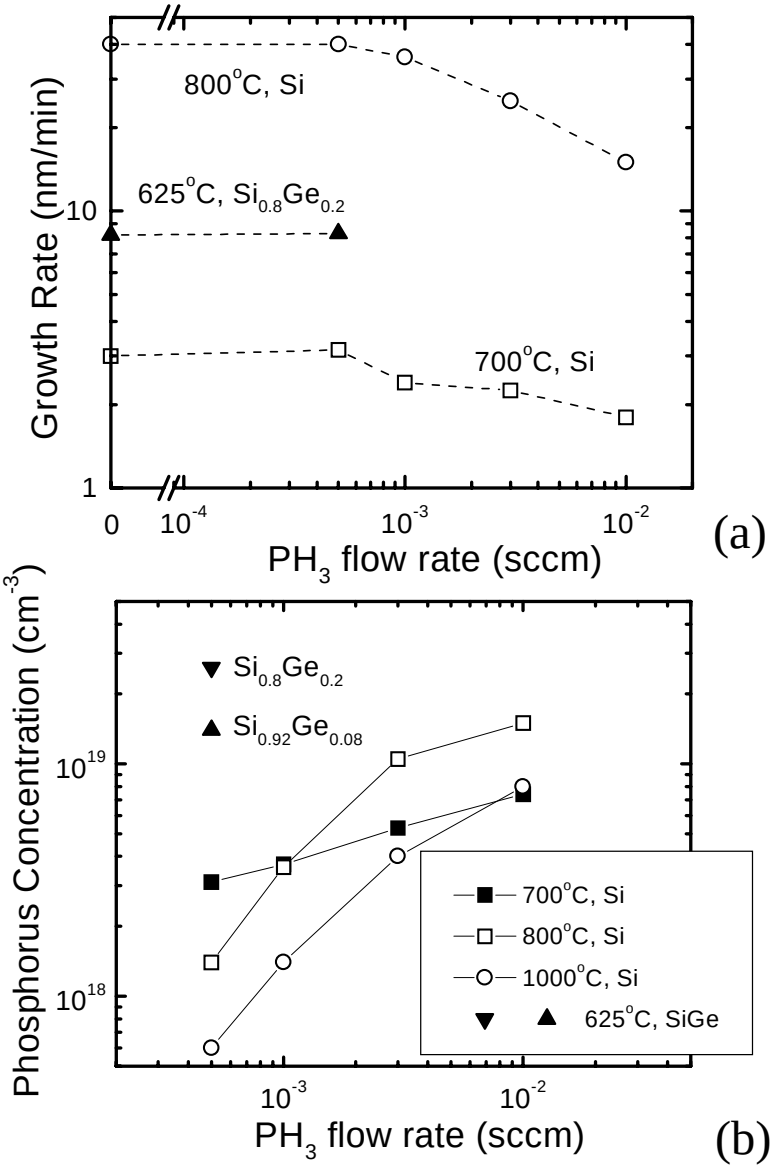


Figure 4.2: (a) Growth rate and (b) phosphorus peak concentration as a function of phosphine flow rate for the growth of silicon at 700^oC, 800^oC, 1000^oC, and $Si_{0.8}Ge_{0.2}$ at 625^oC.

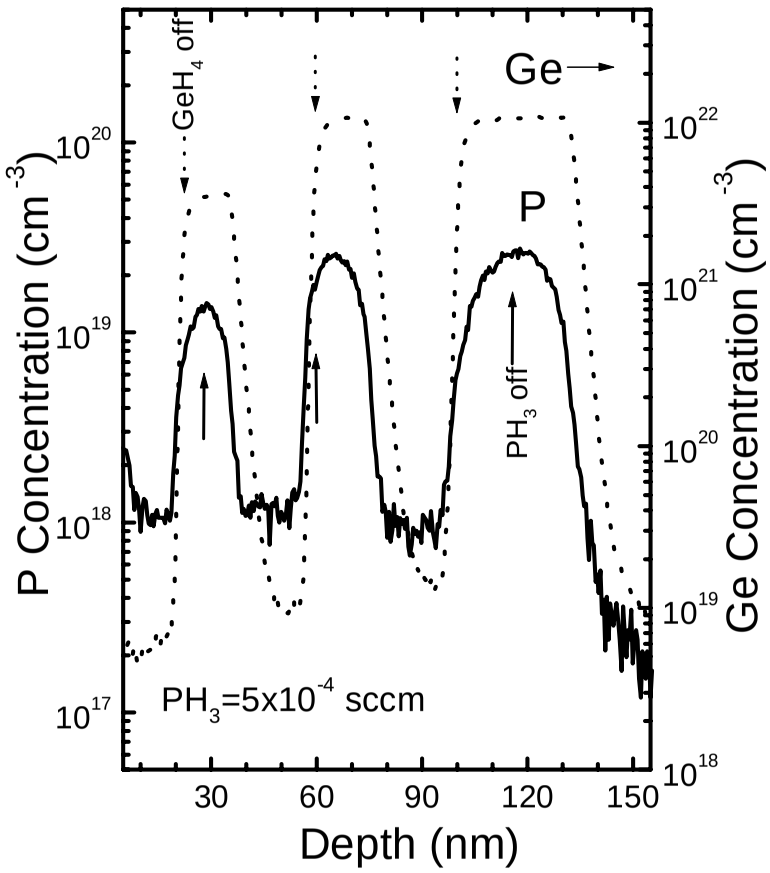


Figure 4.3: Phosphorus doping profiles (by SIMS) in $Si_{1-x}Ge_x$ epitaxy layers grown at 625^{o}C with a PH_3 flow rate of 5×10^{-4} sccm. The SiGe layers are separated by silicon layers grown at 700^{o}C.

desorption of phosphorus from a silicon surface with increasing temperature when T>550^{o}C [145, 171]. However, when the phosphine flow rate is increased to 1×10^{-2} sccm, the highest phosphorus incorporation level occurs at a growth temperature of 800^{o}C. Further studies are necessary to fully understand phosphorus incorporation into silicon epitaxial layers.

4.2.2 In SiGe Epitaxial Layers

Phosphorus profiles for a multi-layer sample with phosphorus doped $Si_{1-x}Ge_x$ alloys separated by nominally undoped silicon layers are shown in Fig. 4.3. The SiGe alloys were grown at 625^{o}C with germane (105 sccm for x=0.2 and 30 sccm for x=0.1) and DCS

(26sccm), while the silicon layers were grown at 700^{o}C. At the end of each silicon layer/start of each SiGe layer, the dichlorosilane flow was left constant and the wafer temperature was lowered from 700^{o}C to 625^{o}C. The germane and phosphine were then turned on simultaneously. At the end of the SiGe layers, the germane source was first shut off, and the temperature was raised 30sec later to 700^{o}C to grow silicon. (The silicon growth rate at 625^{o}C with dichlorosilane is $\sim$4 Å/min). The phosphine flow rate is chosen to be 5×10^{-4}sccm for all the SiGe layers. The exact point at which the phosphine source was turned off varied, as shown in Fig. 4.3. The phosphine was turned off in the center of each SiGe layer, except for the middle SiGe layer where phosphine was turned off simultaneously with germane. We did not grow any undoped SiGe layers in these experiments, but the growth rate for a 5×10^{-4}sccm phosphine flow rate is similar to that previously observed in our lab for undoped SiGe layers under the same condition[176]. Higher phosphorus incorporation in SiGe alloys than that in Si is observed. The phosphorus level increases with the germanium content: 2.5×10^{19}cm^{-3} in $Si_{0.8}Ge_{0.2}$ vs. 1.3×10^{19}cm^{-3} in $Si_{0.92}Ge_{0.08}$ vs. 2×10^{18}cm^{-3} in silicon. The observed enhancement of phosphorus incorporation in $Si_{1-x}Ge_x$ has also been observed using silane [152, 164]. Chen *et al.* attributed the effect solely to the increased hydrogen desorption rate in the presence of germanium [152]. However, this explanation is not convincing because the increased hydrogen desorption is known to increase the growth rate, which would decrease the doping level. Jang *et al.*[164] attributed the effect of germanium to the fact that formation of P_2 dimers are hindered by germanium, so that the fraction of monatomic phosphorus is increased, leading to increased phosphorus incorporation.

4.3 Interface Abruptness

The phosphorus profile for the sample grown at 700^{o}C is re-plotted in Fig. 4.4 as a dashed-line. The phosphine flow rate was 5×10^{-4} sccm, giving a peak phosphorus concentration of 3×10^{18}cm^{-3}. At the leading edge, when the phosphine was turned on, the transition slope is about 19nm/decade. When the phosphine was turned off in the middle of the silicon layer, however, the phosphorus doping density is above 10^{18}cm^{-3} in the 70

nm silicon layer above the intentionally-doped layer, yielding a slope for the decay of the phosphorus concentration of 155nm/decade (trailing edge). Sharper profiles are observed at higher phosphorus flow rates for a given growth temperature, as shown in Fig. 4.1. For example, at 700^{o}C the transition at the leading edges are 13.7nm/decade and 51nm/decade for phosphine flow rates of 1×10^{-2}sccm and 1×10^{-3}sccm, respectively, while the trailing edges are 13.7nm/decade and 93nm/decade. Furthermore, sharper phosphorus profiles also occur at lower growth temperatures for a given phosphine flow rate. For example for a 1×10^{-2}sccm phosphine flow rate, the transition slope at the trailing edges are 45nm/decade and 91nm/decade at 800^{o}C and 1000^{o}C, respectively, while the slope at the leading edges are 19nm/decade and 45nm/decade. The transient responses of the phosphine/silane doping profiles have been studied by Kamins *et al.* [157] on the slow transition at the leading edges. Reif *et al.* [175] reported that at high temperatures (T=1000$\sim$1080^{o}C) in the mass-transport-limited regime, the decay length of the phosphorus profile is proportional to the silicon deposition rate. This is similar to the result in this work using dichlorosilane: a lower growth temperature and a high phosphine flow rate lead to a lower growth rate and thus result in a sharper phosphorus profiles we observed. The physical mechanisms dominating the transient process are related to the time needed by the adsorbed layer to reach the new steady-state population of dopant species. Slower deposition rates lead to shorter thicknesses to achieve this sharp profile condition. The decay rate at 800^{o}C for low phosphorus flows is especially poor, worse than that at 1000^{o}C, perhaps due to the fact that the phosphorus can evaporate from the surface to some degree at 1000^{o}C, but not at 800^{o}C.

As seen in Fig. 4.1, after introducing phosphine, the phosphorus background doping level in the subsequent unintentionally doped silicon layers is higher than 5×10^{17}cm^{-3} in all cases. At a lower temperature and a higher phosphine flow rate, the background doping level is even higher. The high level of background doping after turning off the phosphine has also been reported by Bashir *et al.* [177]. The characteristics of slowly decaying profiles (especially on the trailing edge) and the high background doping level effect of phosphorus doping significantly limit its application in the fabrication of practical devices. There may be three mechanisms of this apparent memory effect: (i) auto-doping

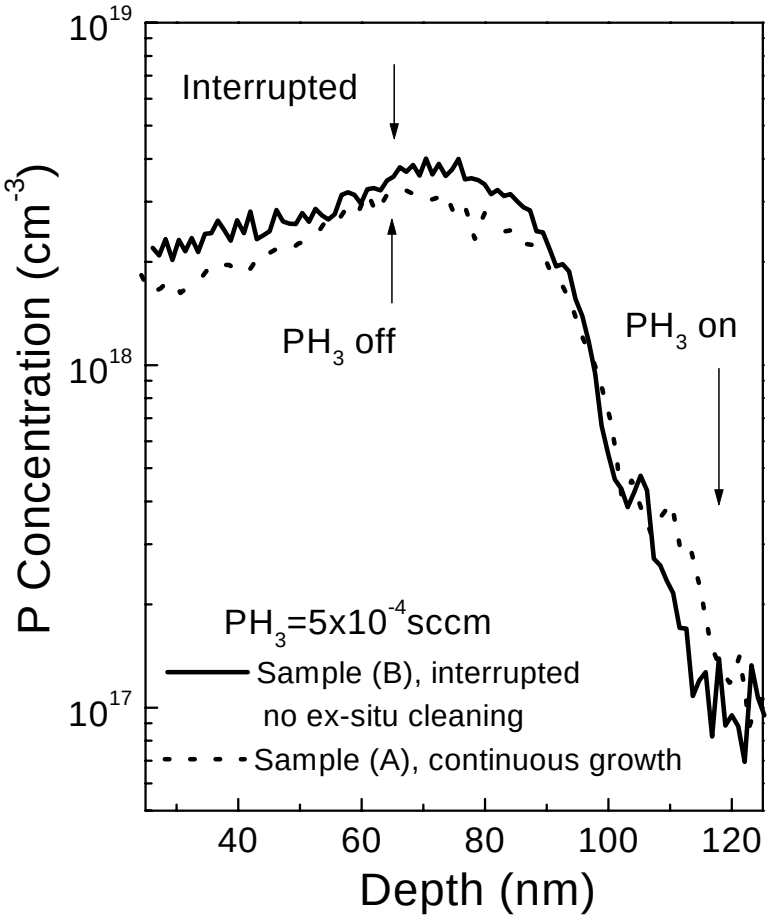


Figure 4.4: Phosphorus profiles (by SIMS) from sample A (using conventional continuous growth) and sample B (interrupted-growth without any *ex-situ* cleaning), grown at 700^oC, with a phosphine flow rate of 5×10^{-4} sccm. The profile of sample A is re-plotted from Fig. 4.1.

from residual phosphorus inside the growth chamber, (ii) the high fraction of phosphorus on the wafer surface, which results from the high phosphorus adsorption coefficient on the silicon surface (mentioned in the previous paragraphs) and the phosphorus segregation at the moving growth interface[177], and (iii) solid state diffusion of phosphorus. The third reason can be ruled out at or below 800^{o}C due to the low diffusion coefficients. The first mechanism is supported by the observation that after high phosphine flow, a significant phosphorus background doping level has been observed in subsequent wafers grown in the same chamber. Similar phenomena have also been published using silane [146, 160, 178].

In the case of SiGe, as mentioned above, the germanium is thought to reduce phosphorus coverage on the wafer and reactor surfaces, and thus results in sharper phosphorus profiles in a $Si_{1-x}Ge_x$ than those in silicon epitaxial layers. Sharper n-type doping profiles have been observed in $Si_{1-x}Ge_x$ alloy (vs. Si) using silane [159, 164]. In our case, for the same phosphine flow (5×10^{-4}sccm), the transition is much faster in $Si_{1-x}Ge_x$ layers than that in silicon. The leading edge of the phosphorus profiles in a $Si_{0.8}Ge_{0.2}$ alloy is only 6.8nm/decade, as shown in Fig. 4.3. However, there is also a slow decay rate of phosphorus in the SiGe layers when the phosphine is turned off. The phosphorus profile falls more rapidly when switching to silicon growth at 700^{o}C, which is obvious when comparing the two trailing edges of the phosphorus profiles in $Si_{0.8}Ge_{0.2}$ layers. The transition is noticeably sharper when phosphine and germane flows are switched off simultaneously. This may be due to the lower growth rate or low level of incorporation of surface phosphorus into silicon layers (as discussed previously).

4.4 Improvement of Phosphorus Profiles

To identify the dominant mechanism of phosphorus persistence effect on silicon epitaxial layers and to eliminate this effect, especially on the trailing edge, the growth was interrupted after the phosphorus-doped layer and various steps were applied to clean the wafer surface and/or the reactor surfaces. The surface treatments studied here are listed in Table 4.1. All the samples discussed in the following sections were grown at 700^{o}C with n-type doping

by using 5×10^{-4}sccm phosphine and 26sccm dichlorosilane. It was reported that phosphine adsorption decreases to 10% of its maximum value at 800^{o}C[145]. To test if 800^{o}C baking may help to remove residual phosphorus in the chamber and on the wafer surface, the n-type growth of sample B (identical to sample A in the dashed-line of Fig. 4.4) was interrupted by turning off the phosphine and dichlorosilane and subsequently cooling the wafer down to room temperature. Hydrogen (3slpm) was flowed for 15min to purge the chamber (6torr), followed by an 800^{o}C bake at 10 torr for 45sec in 3 slpm hydrogen. Another 70 nm silicon layer without additional phosphine was grown at 700^{o}C after the interruption. No obvious improvement in the phosphorus profile was observed (solid-line in Fig. 4.4). We conclude that the 800^{o}C bake does not remove phosphorus from the wafer surface and/or that the residual phosphorus source is on the reactor walls, whose temperature is estimated at a few hundred degrees Centigrade. This kind of growth interruption and *in situ* hydrogen purge has previously been used widely in devices after n-type doping with silane [178], however no significant influence on the dopant profile was found by some research groups[157, 177].

Sample	continuous vs. interrupt growth	wafer removed from growth chamber	sacrificial wafer during interruption	oxidation in H_2SO_4+H_2O_2 and etch in HF	*in situ* cleaning in 3slpm H_2
A	continuous	No	-	-	-
B	interrupt	No	No	No	cold 15min 6 torr and 800^{o}C 45sec 10torr
C	interrupt	Yes	Yes	No	800^{o}C 45sec 10torr
D	interrupt	Yes	Yes	Yes, once	800^{o}C 45sec 10torr
E	interrupt	Yes	No	Yes, 5 times	800^{o}C 45sec 10torr
F	interrupt	Yes	Yes	Yes, 5 times	800^{o}C 90sec 10torr

Table 4.1: Various surface treatments for the samples studied in this chapter to improve the phosphorus doping profiles in silicon.

To more thoroughly clean the sample surface and the growth chamber, samples C and D were removed from the growth chamber after identical n-type growth as samples A and B. A sacrificial wafer was then grown to getter residual phosphorus in the growth chamber. The sacrificial wafer included a 1μm silicon layer grown with dichlorosilane at 1000^{o}C and a 300 nm $Si_{0.65}Ge_{0.35}$ layer at 625^{o}C from dichlorosilane and germane, without flowing any dopant gases. The low-temperature SiGe layer was added because we believe germanium can getter phosphorus residual in the reactor, as previously mentioned. Sample C was dipped in diluted HF (50:1) before reloading into the growth chamber in order to remove any possible native oxide after exposure to air. The sample was baked at 800^{o}C for 45 sec in 3 slpm hydrogen at 10torr before the 700^{o}C undoped Si re-growth. However the phosphorus doping profile is not improved (shown in Fig. 4.5). Sample D was soaked in H_2SO_4:H_2O_2 (2:1) for 20min before the HF dip. The chemical oxide grown on the sample consumes 10$\sim$20Å of the silicon surface thus removing highly concentrated phosphorus on the wafer surface, as suggested in Ref. [160]. After reloading, the same *in situ* cleaning and 700^{o}C undoped epitaxy was performed. SIMS measurements show that in the upper undoped silicon layer, the phosphorus concentration is now successfully lowered to 10^{17}cm^{-3} in sample D with a sharp transition (Fig. 4.5). Thus we conclude that removal of 10$\sim$20Å of the silicon surface is effective in bringing down the background doping level at a rate of 20nm/decade. The phosphorus spike is induced by oxygen contamination at the interrupt interface due to insufficient *in situ* cleaning after the growth interruption.

To investigate the role of the sacrificial wafer in changing the background doping in the growth chamber, sample E was grown the same way as sample D, except that no sacrificial wafer was grown during the growth interruption and that the chemical oxidation/etching step was repeated 5 times. The phosphorus doping profile is shown in Fig. 4.6. Although the doping density drops at 17nm/decade from 3×10^{18}cm^{-3}, the doping level in the upper Si layer is still above 5×10^{17}cm^{-3}. The results from sample C, D, and E indicate that in order to achieve sharp phosphorus doping profiles and low doping densities in the following epi-layers, both sacrificial wafer growth to reduce the background doping in the growth chamber *and* removal of 10$\sim$50Å of the silicon surface are important. Combining these two

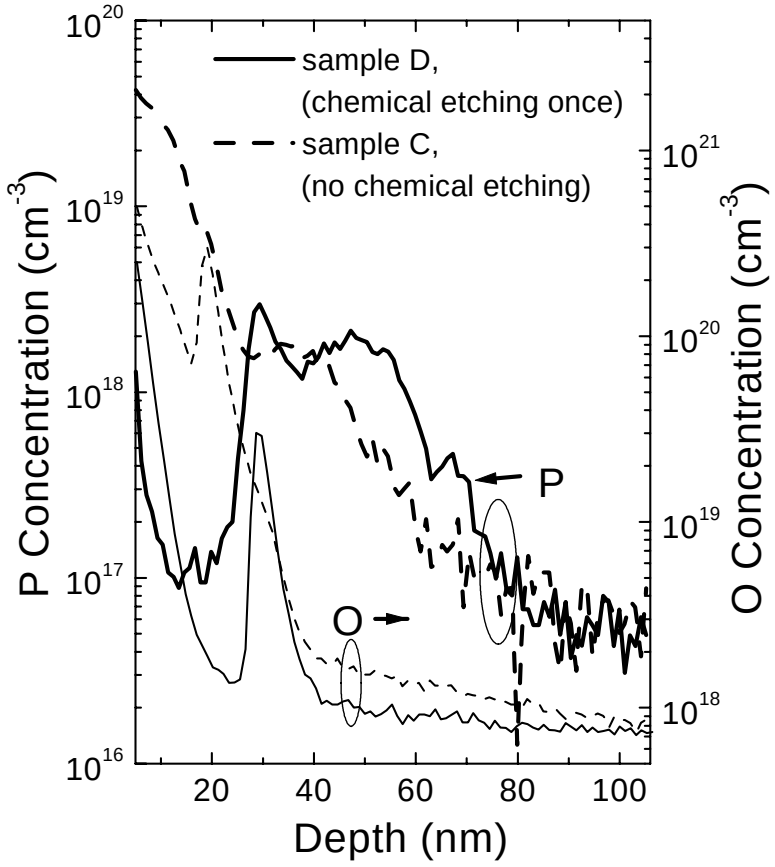


Figure 4.5: Phosphorus profiles (by SIMS) from sample C (without chemical etching) and sample D (with chemical etching) to demonstrate the effect of *ex-situ* etching. During the growth interruption, a sacrificial wafer was grown in the reactor in both cases.

methods of surface etching and sacrificial wafer growth, the result of sample F is shown in Fig. 4.6 along with a continuously-grown sample for comparison. After re-loading the wafer before further growth, the sample was cleaned at 800^{o}C at 10torr in 3 slpm hydrogen for 90sec. It has been reported that this low temperature cleaning procedure before re-growth leads to an impurity-free interface [179]. As shown in Fig. 4.6, the phosphorus trailing edge of sample F is now 13nm/decade vs. 155nm/decade in sample A. The doping level in the upper silicon layer is as low as 5×10^{16}cm^{-3}. At the interrupted interface, no oxygen or carbon spikes are observed by SIMS. Note that this cleaning process has a thermal budget which is sufficiently low to avoid any excessive diffusion of the existing dopant profiles, as can be seen by the similar transition rates of the lower phosphorus interface in all samples. This method allows us to realize devices such as sub-100nm vertical MOSFET's, where very tight control of the phosphorus profile is required, without any excess leakage associated with a contaminated interface [180].

4.5 Device Applications

The sharp phosphorus profile control achieved in this work in silicon epitaxial layers can be directly applied to the fabrication of vertical MOSFET's and other devices. In vertical MOSFET's, sharp doping level transitions at the source/drain and channel interfaces provide less series resistance or junction leakage. The implementation in p-channel vertical MOSFET's will be discussed in Chapter 5.

In addition to sharp profile transitions, high phosphorus doping levels ($\geq 5\times10^{19}$cm^{-3}) are also required in the source/drain region for vertical n-channel MOSFET's with channel lengths below 100nm. In this work, the source/drain regions were grown using DCS as the silicon source and growth pressure was maintained at 6torr for all devices. The highest phosphorus doping level achieved is 1.5×10^{19}cm^{-3} in silicon layers at 800^{o}C for a 0.01sccm phosphine flow. Various experiments have been carried out on the same RTCVD system in the past. Lanzerotti *et al.* achieved an $\sim 3\times10^{20}$ cm^{-3} phosphorus doping level in silicon epitaxy layer by increasing the growth pressure to 250torr [181]. However a high oxygen

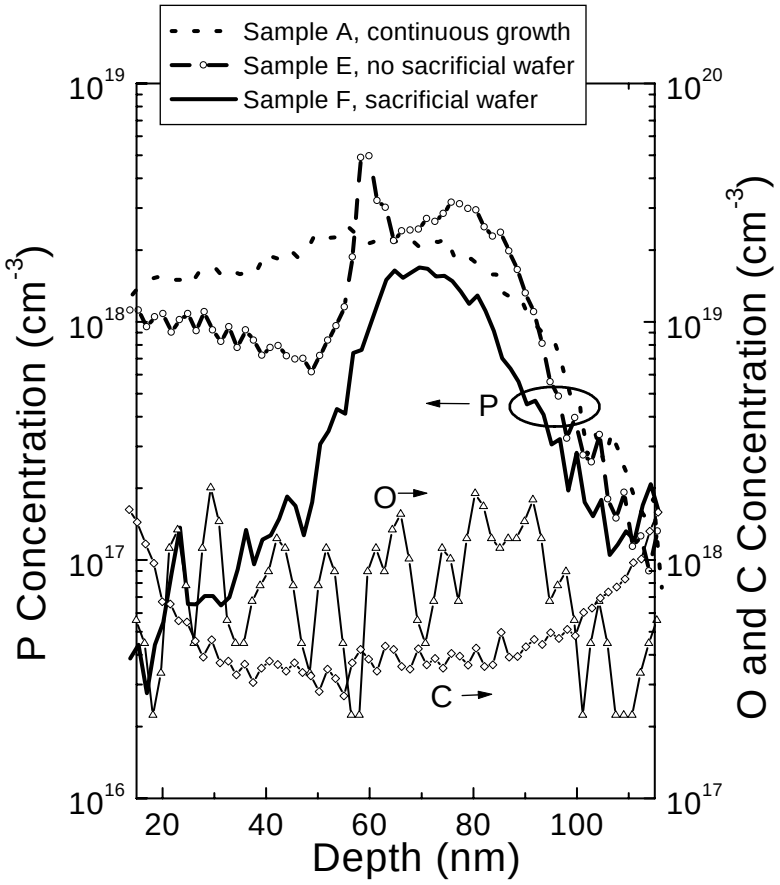


Figure 4.6: Phosphorus profiles (by SIMS) from sample E (without sacrificial wafer growth) and sample F (with a sacrificial wafer growth) with *ex-situ* etching of both of the wafer surfaces. The phosphorus profile from a continuously grown sample is plotted for reference. Oxygen and carbon profiles of sample F are also plotted. Note the *in-situ* cleaning before re-growth is longer for sample F than that for sample C, D and E.

concentration was found using this high growth pressure. Further experiments are necessary to investigate the effect of oxygen contamination on device performance. Optimizing the phosphorus doping level also requires further study.

4.6 Summary

In summary, *in situ* phosphorus doping in Si (700∼1000^{o}C) and SiGe (625^{o}C) alloys grown by RTCVD have been studied using dichlorosilane as the silicon source. Increasing the phosphine flow leads to a decreasing growth rate and saturation of the phosphorus level in silicon layers. Significant background doping and slow transitions are also observed in silicon, while higher doping levels and sharper transitions are possible in SiGe. Ultra-sharp phosphorus profiles have been achieved by removing phosphorus from both the wafer surface and the reactor chamber after n^+ epitaxy. Using an *ex situ* chemical etching of 10∼50Å from the silicon surface, sacrificial wafer growth, and an 800^{o}C maximum temperature *in-situ* cleaning, a phosphorus doping profile of 13nm/decade has been demonstrated for silicon layers grown at 700^{o}C, without oxygen and carbon contamination. Successful implementation of the above processes in vertical p-channel MOSFET's will be demonstrated in Chapter 5. Further study is necessary to obtain the higher phosphorus doping levels ($> 5 \times 10^{19}$cm^{-3}) required for vertical n-channel MOSFET's.

Chapter 5

Sub-100nm Vertical p-Channel MOSFET's

The scaling of vertical p-channel MOSFET's with the source and drain doped with boron during low temperature epitaxy is limited by the diffusion of boron during subsequent side wall gate oxidation. By introducing thin $Si_{1-x-y}Ge_xC_y$ layers in the source and drain regions, this diffusion has been suppressed, enabling for the first time the scaling of vertical p-channel MOSFET's to under 100nm in channel length to be realized. Device operation with a channel length down to 25nm has been achieved. The trade-offs between undoped and doped $Si_{1-x-y}Ge_xC_y$ layers have been studied. By using highly boron doped $Si_{1-x-y}Ge_xC_y$ layers, the influence of the non-ideal surface properties of $Si_{1-x-y}Ge_xC_y$ on the channel current can be avoided. No device degradation (leakage current, drive current reduction) due to carbon-related defects or interrupt-growth induced impurities is observed.

5.1 Introduction

The channel length of a vertical MOSFET may be determined by the epitaxial layer thicknesses instead of the lithography resolution. Since the epitaxy layer thickness can be controlled to a few tenths of nanometer by molecular beam epitaxy or chemical vapor deposition, it is possible in principle to scale the channel length of MOSFET's to deep sub-100nm. However, dopant diffusion from the source/drain into the channel region during gate

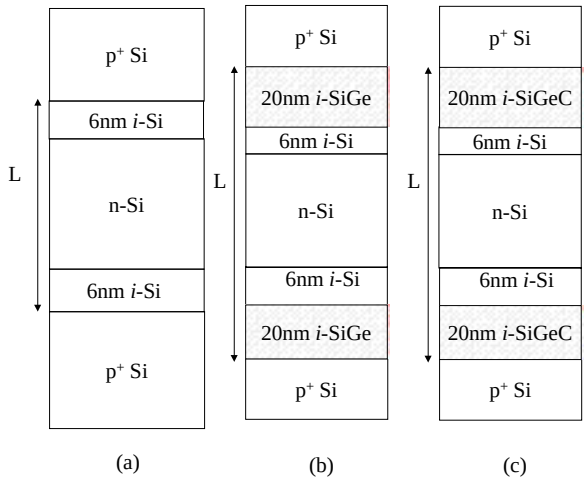


Figure 5.1: Various epitaxial structures grown by RTCVD for vertical p-channel MOSFET's: (a) with Si only, (b) with 200Å of undoped $Si_{0.8}Ge_{0.2}$ and (c) with 200Å of undoped $Si_{0.796}Ge_{0.2}C_{0.004}$.

oxidation is a limitation. Many groups [75, 79, 80, 78] have used low temperatures ($\leq 650^o$C) to fabricate the gate oxide for both p- and n-channel vertical MOSFET's. The critical point is that the diffusion problem is more significant in p-channel devices. Sub-100nm n-channel vertical MOSFET's have already been reported[74, 77], while there are a few reports on p-channel devices (with L>100nm) [70, 79, 80]. In this chapter, we introduce thin $Si_{1-x-y}Ge_xC_y$ epitaxial layers to suppress the boron oxidation enhanced diffusion (OED) effect and demonstrate, for the first time, sub-100nm vertical p-channel MOSFET's with channel lengths down to 25nm. Both doped and undoped $Si_{1-x-y}Ge_xC_y$ layers in the source/drains of vertical p-channel MOSFET's are presented. Due to thicker side-wall gate oxide grown on $Si_{1-x-y}Ge_xC_y$ layers, doped $Si_{1-x-y}Ge_xC_y$ in the source and drain is preferable. No excess leakage current after adding $Si_{1-x-y}Ge_xC_y$ layers is observed.

5.2 Demonstration of Vertical p-channel MOSFET's

In this chapter, vertical p-channel MOSFET's are studied. In order to probe the limitations in scaling of vertical p-channel MOSFET's, a "planar epitaxy" design is used to simplify the fabrication process. The silicon pillars are wide ($\sim 50\mu$m) for all the devices

presented in this chapter. To suppress punch-through in the center of the pillar, high n-type doping is necessary in the channel region. Details of the fabrication have been presented in Chapter 3. For reference, the processing steps are summarized in the following paragraph.

First, epitaxial layers for vertical p-channel MOSFET's were grown by our RTCVD system. The growth pressure was 6torr and 26sccm DCS was used as the silicon source. 3slpm hydrogen was used as the carrier gas. B_2H_6 and PH_3 were used as dopant sources. The device active layers were grown on top of a 1μm Si buffer with a boron doping level of 3×10^{19} cm^{-3}. The overall structure is shown Fig. 5.1a. The silicon channel was grown at 700^{o}C and doped with phosphorus without interruption. There are two 60Å undoped silicon spacer layers on each side of the channel to compensate boron diffusion during the growth. The 200nm top p$^+$ Si layer (4×10^{19}cm^{-3}) was subsequently grown at 750^{o}C. Vertical pillars were then created by optical lithography and RIE in an SF_6/CCl_2F_2 mixture. The side wall faces are 25^o off from perfectly vertical and are aligned along the [110] direction. A sacrificial oxide layer was used before gate oxidation to smooth the side wall. Both sacrificial and gate oxidation were performed at 750^{o}C in wet O_2 (for 20min to give ~100Å on [100] Si surface). The gate oxide was annealed at 750^{o}C in N_2 for 20min, followed by deposition of ~200nm polycrystalline silicon using 100sccm SiH_4 (diluted to 10% in Ar) and heavily *in situ* doped with boron in the RTCVD chamber at 700^{o}C. The boron concentration in polysilicon measured from secondary ion mass spectroscopy (SIMS) is 2×10^{21}cm^{-3} and the sheet resistance is 10$\Omega/\Box$. The polysilicon gate was etched in an RIE system using SF_6/CCl_2F_2. The FET's were encapsulated by spin-on-glass. The contact pads consisted of Ti and Al. The cross-section of the device has been shown in Fig. 3.18.

Vertical p-channel MOSFET's with channel lengths of about 0.5μm were fabricated first and an example is shown in Fig. 5.2. The channel length is estimated from the as-grown sample. The channel doping is estimated to be ~1.0×10^{18}cm^{-3} after processing. The thickness of the side-wall gate oxide is estimated as 17nm. Note that due to dopant diffusion during gate oxidation, the actual channel length of the Si device after processing will be shorter. This device has reasonable I-V and subthreshold characteristics. The threshold voltage is -1.4V and the subthreshold slope is 90mV/dec.

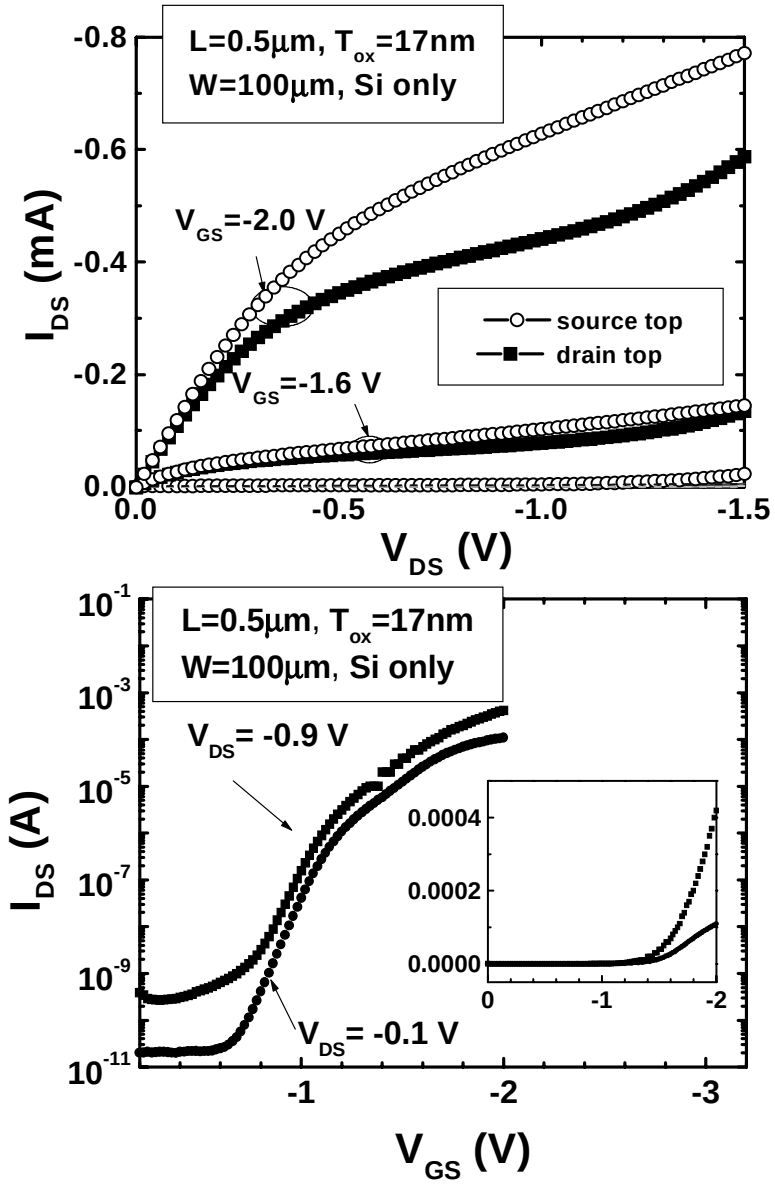


Figure 5.2: Current-voltage and subthreshold characteristics of a vertical p-channel MOSFET with 0.5μm channel length and $\sim 1.0 \times 10^{18}\text{cm}^{-3}$ channel doping.

5.3 Dopant Diffusion During Processing After Epitaxy

As we have successfully demonstrated vertical p-channel MOSFET's with channel length about 0.5μm, the next goal is to scale the channel length down to sub-100nm to pursue high drive current and faster speed, as discussed in Chapter 2.

A vertical p-channel MOSFET with channel length expected to be 70nm (measured by SIMS from as-grown sample) was fabricated. The epitaxial layers are similar to the L=0.5μm device and are also shown in Fig. 5.1(a). The channel region was doped to $\sim 1.0\times10^{18}$cm^{-3}. In this work, the channel length is defined as the epitaxial layer thickness between the two p^+ layers, with the edge of the p^+ profile defined as the point when the boron concentration (as measured by secondary ion mass spectroscopy (SIMS)) drops to $1/\sqrt{2}$ of its value in the heavily doped source/drain, multiplied by 1.1 to account for the fact that the side walls are not perfectly vertical. Fig. 5.3a gives SIMS profiles of boron in the as-grown p^+np^+ structures, which demonstrate the abrupt profiles before any further high temperature processes. The boron slopes are 8nm/dec and 12nm/dec on upper and lower edges respectively, and are limited by SIMS resolution. (The worse profile on lower interface is caused by the primary Cs^+ beam knocking in B atoms further into the substrate).

However, this device (with only Si layers) is shorted between source and drain. Its subthreshold characteristics is shown in Fig. 5.4. This is further confirmed by SIMS measurement. SIMS result from the same sample after all the high temperature processing is given in Fig. 5.3b. It shows that boron in the source and drain has significantly diffused into channel. The boron level in the channel is increased from 10^{17}cm^{-3} to $> 5\times10^{18}$cm^{-3}. This is the key problem, which limits vertical p-channel MOSFET's with channel length in practice to $\gg$100nm. Note that in the literature the shortest channel length of vertical p-channel MOSFET's by a similar process were >130nm [79], although a high pressure (10bar) wet oxidation at low temperature (600^oC) was required to limit diffusion.

A high quality thin gate oxide is a necessity for MOSFET's scaling. For high quality gate oxides, temperatures in excess of 750^oC are commonly used. However, such a temperature will cause boron dopant in the source and drain to diffuse into the channel region,

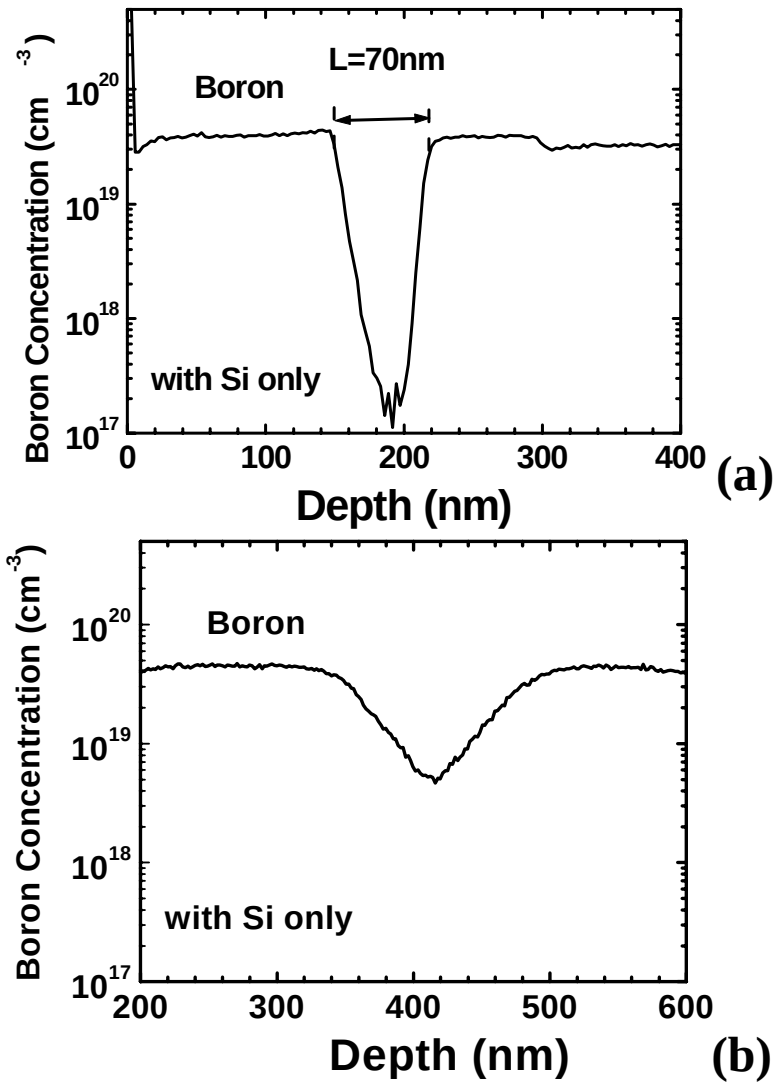


Figure 5.3: Boron profiles from structure with Si only (Fig. 5.1a), measured by SIMS from (a)an as-grown sample, (b) after all high temperature processing (750^oC sacrificial and gate oxidation in wet oxygen for totally 40min and 700^oC 30min poly-silicon deposition). The SIMS primary ion beam was Cs^+ with an energy of 3keV.

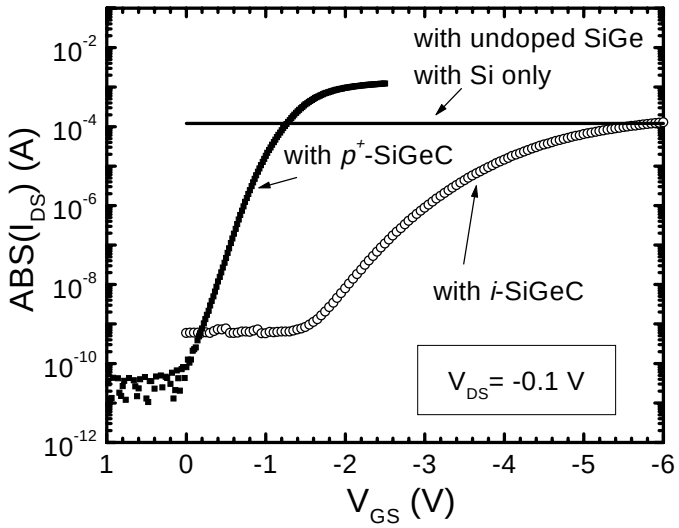


Figure 5.4: Subthreshold characteristics of devices shown in Fig. 5.1 and Fig. 5.12c. Vertical p-channel MOSFET's are shorted for devices with Si only (Fig. 5.1a) and with undoped $Si_{0.8}Ge_{0.2}$ (Fig. 5.1b) layers.

as shown in Fig. 5.3. Boron diffusion may be caused by a purely thermal effect or an oxidation enhanced diffusion (OED) effect. Any ion implantation into the top of the pillar could also cause transient enhanced diffusion (TED) of the boron. Tsuprem-4 [126] process simulation was used to study thermal annealing and the effect of OED on boron diffusion in vertical p-channel MOSFET's. Fig. 5.5 shows the boron profile for a device with L=0.11μm under various process conditions. The boron profile is well defined after epitaxial growth of the p^+np^+ sequence. However, significant boron diffusion occurs after 750^{o}C sacrificial and gate oxidations in wet O_2 for 20min each and an N_2 annealing for 15min. The boron concentration in the channel rises to $>8\times10^{18}$cm^{-3}, in agreement with the SIMS result. Only when the oxidation temperature reduced to 600^{o}C and using high pressure (10 bar) to increase the growth rate (as used in some literature [79]), does the boron profile remain unchanged from the as-grown sample. On the other hand, by simply turning off the interstitial effect (oxidation enhanced diffusion) on boron diffusion in the simulation program, the boron profile remains the same as the as-grown sample after 750^{o}C wet oxidation as well. This indicates that most of the boron diffusion is caused by the OED effect rather

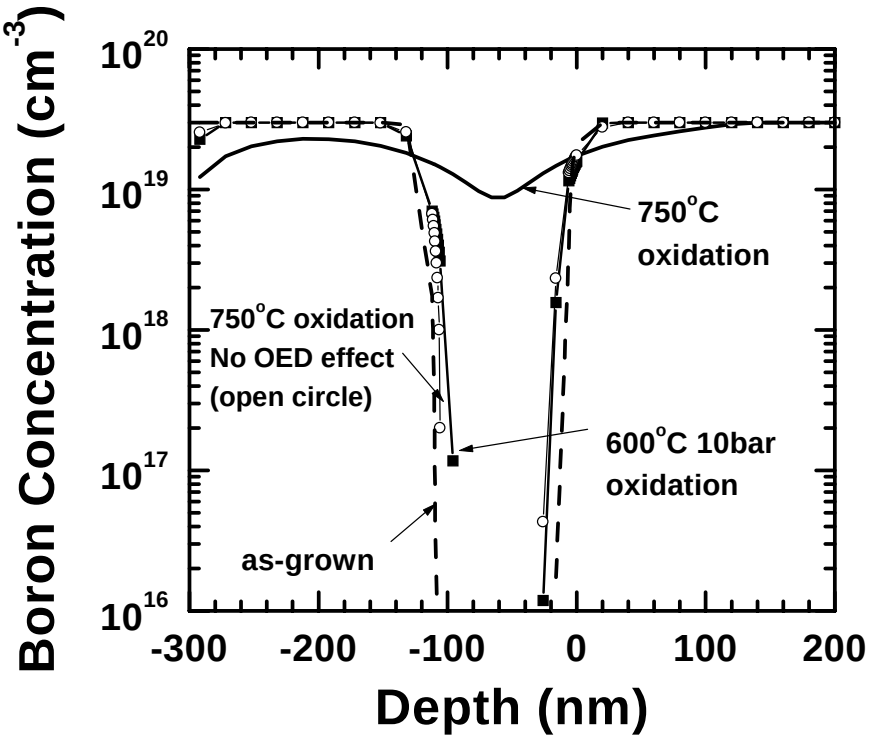


Figure 5.5: Tsuprem-4 simulation of boron profiles in vertical p-channel MOSFET's after 700^oC Si channel and 750^oC top p^+ layer epitaxy (dashed line) and after various oxidation conditions: 750^oC wet oxidation of 40min and N_2 annealing for 15min including OED (solid line); without OED (open circles); 600^oC wet oxidation at 10bar (solid squares) to give the same sacrificial and gate oxide thicknesses.

than a purely thermal effect. Therefore, the reduction of boron diffusion depends on the ability to control boron OED in the vertical p-channel MOSFET's processing steps where in-situ doping during epitaxy before gate oxidation is required.

5.4 Suppression of Boron Oxidation Enhanced Diffusion by Introducing Substitutional Carbon

It is well known that boron diffuses primarily via an interstitial mechanism [182, 183]. Substitutional boron can be displaced by silicon interstitials to form interstitial boron.

$$B_s + I_{Si} \rightarrow B_i \tag{5.1}$$

Boron interstitials are already quite mobile at low temperatures (T$< 600^o$C) [183]. Oxidation and ion-implantation generate excess silicon interstitials and thus cause oxidation enhance diffusion (OED) and transient enhance diffusion (TED) effects. The OED effect dominates at lower temperatures, and as such solely reducing the oxidation temperature is not very effective. Therefore, the reduction of TED and/or OED depends on the ability to reduce the excess silicon interstitials.

Recently, implanted [184] and epitaxially incorporated [185, 186] carbon in the uniform background of silicon epitaxial layers have been found to suppress boron TED. It has been found that substitutional carbon presents an effective trap for the excess silicon interstitials and that interstitial and substitutional carbon then form an immobile carbon complex [187, 188, 189].

$$C_s + I_{Si} \rightarrow C_i \tag{5.2}$$

$$C_i + C_s \rightarrow C - C_{complex} \tag{5.3}$$

Complete suppression of TED has been reported by Stolk *et al.* for a uniform carbon concentration of $2 \times 10^{19}\text{cm}^{-3}$[190]. In practical device applications, localized carbon incorporation is desired to minimize carbon's deleterious effects on carrier transportation. The

reduction of boron TED in hetero-bipolar transistors (HBT) has been reported [191] by using $Si_{1-x-y}Ge_xC_y$ layers in the base region, initiating the investigation in the present work by using $Si_{1-x-y}Ge_xC_y$ layers to suppress the OED effect on dopant diffusion in vertical MOSFET's.

$Si_{1-x-y}Ge_xC_y$ is also a boron diffusion barrier during pure thermal annealing. The boron diffusivity in the SiGeC alloy is approximately 8 times lower than that in SiGe material [192], and its diffusivity in the SiGe alloy is an order of magnitude lower than that in Si [193], when no excess interstitials due to implantation or oxidation are present.

5.5 $Si_{1-x-y}Ge_xC_y$ Epitaxial Layer Growth

Although the solubility of substitutional carbon in Si is only $3 \sim 4 \times 10^{17}cm^{-3}$ at the melting temperature [194, 195, 196], using MBE and CVD operated from 450^oC to 650^oC, high quality $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ films with up to 2% substitutional carbon have been reported [197, 198, 199]. This is so because the "surface solubility" is more important in the kinetically-dominated epitaxial growth range and is four orders of magnitude higher than that in the bulk [200, 201]. However, low temperatures ($< 600^oC$) and high growth rates are required to achieve high fractions of substitutional carbon incorporation [202, 198].

Due to the growth rate enhancement in the presence of Ge [176], $Si_{1-x-y}Ge_xC_y$ epitaxial layers with carbon atoms in their substitutional sites have been successfully grown, using SiH_4 or DCS as the Si source and GeH_4 as the Ge source, at $550\sim625^oC$ on the same RTCVD system [203, 204]. It has been found that higher GeH_4 flow rates and lower temperatures lead to higher substitutional carbon incorporation. Defect-free $Si_{1-x-y}Ge_xC_y$ with carbon concentration up to 1.2% (measured by high resolution transmission electron microscopy) have been achieved at Princeton [205].

All SiGeC epitaxial layers used in this work have the same structure: 20%Ge and 0.4% carbon. Also all $Si_{0.796}Ge_{0.2}C_{0.004}$ layers are 20nm thick. A 26sccm flow of DCS was used as a Si precursor with a 3slpm flow of H_2 carrier gas. 100 sccm of germane (diluted to 0.8% in H_2) and 4 sccm methylsilane (diluted to 1% in H_2) were used as Ge and C precursors.

The growth pressure was 6torr. Ge concentration and film thickness are independent of $SiCH_6$ flow in our experiment range. As with $Si_{0.8}Ge_{0.2}$ layers, the growth temperature for $Si_{0.796}Ge_{0.2}C_{0.004}$ was also kept at 625^oC and the growth rate of both of the layers is about 80Å/min.

The 20nm SiGeC film thickness was chosen so that the $Si_{0.8}Ge_{0.2}$ and $Si_{0.796}Ge_{0.2}C_{0.004}$ epitaxial layers are fully strained during the 17min top p^+ silicon growth at 750^oC and later high temperature processing (40min 750^oC oxidation and 30min 700^oC poly-Si deposition). The 0.4% carbon concentration was chosen as a trade-off: high carbon fraction is desired to sufficiently suppress boron diffusion, but lower fractions are preferable in order to keep all carbon atoms in the substitutional sites and to avoid any possible deleterious effect from carbon. According to Ref. [189], a $4.6\times10^{13}cm^{-2}$ integrated carbon level already can reduce boron diffusivity nearly 50% under 850^oC oxidation conditions.

5.6 Undoped SiGeC Layers in Vertical p-channel MOSFET's

5.6.1 Device Fabrication and Results

To study the effect of SiGeC epitaxial layers on the boron diffusion in vertical p-channel MOSFET's, two identical epitaxial-structures to the all-Si one were grown, with 20nm $Si_{0.8}Ge_{0.2}$ and $Si_{0.796}Ge_{0.2}C_{0.004}$ layers on each side of the channel layer, as shown in Fig. 5.1b and Fig. 5.1c, respectively. The $Si_{0.8}Ge_{0.2}$ and $Si_{0.796}Ge_{0.2}C_{0.004}$ epitaxial layers were not intentionally doped. The channel lengths are 100nm for the undoped SiGe and SiGeC structures, measured from an as-grown sample. The channel doping is also $\sim1.0\times10^{18}cm^{-3}$, same as the all-Si sample. The subthreshold characteristics of the two devices are superposed in Fig. 5.4, for comparison with the all-Si device. Devices with undoped SiGe layers are shorted between source and drain. However, devices with undoped SiGeC have reasonable current on/off ratios.

SIMS results of the boron profiles from the as-grown structures of the two devices with undoped SiGe and SiGeC are plotted in Fig. 5.6a and Fig. 5.7a, showing boron transitions as sharp as those observed in all-Si devices. SIMS results from the two structures after

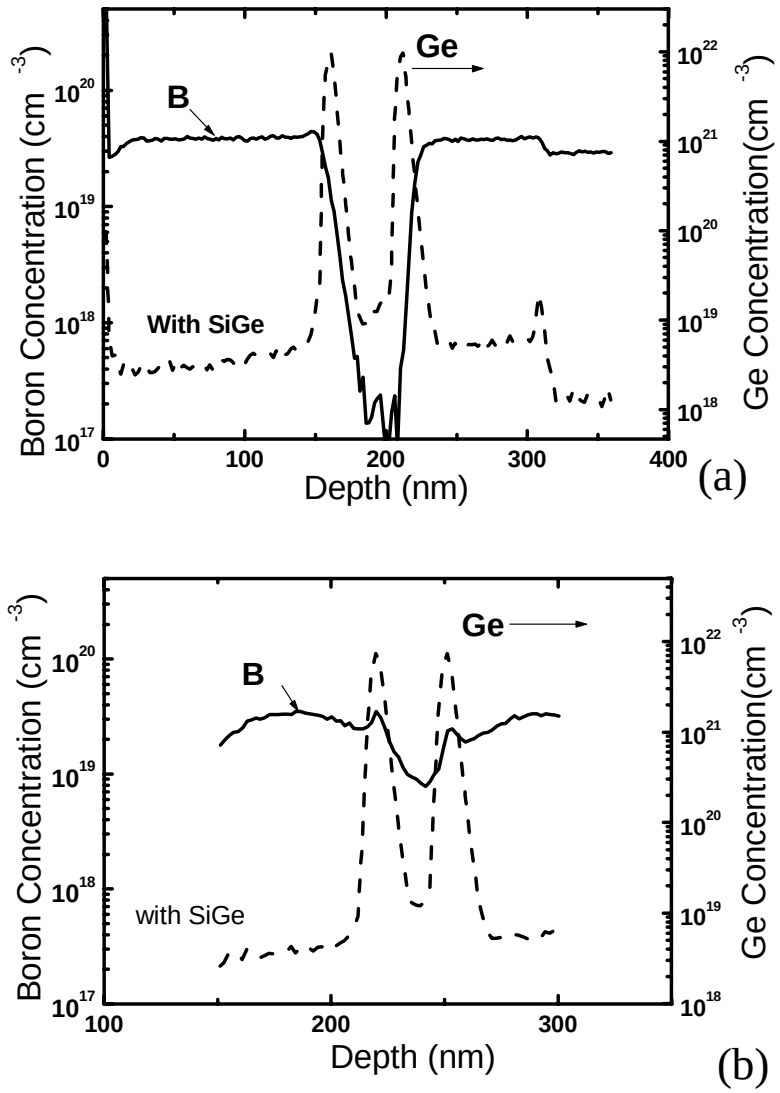


Figure 5.6: Boron profiles from a structure with 20nm undoped $Si_{0.8}Ge_{0.2}$ layers (Fig. 5.1b), measured by SIMS from (a) an as-grown sample, (b) after all high temperature processing (750^oC sacrificial and gate oxidation in wet oxygen for totally 40min and 700^oC 30min poly-silicon deposition).

all high temperature processing, namely 750^{o}C sacrificial and gate oxidation and 700^{o}C polysilicon deposition, are plotted in Fig. 5.6b and Fig. 5.7b. As with the all-Si sample, in the sample with undoped SiGe layers, the boron concentration in the channel region rises from a background level of 10^{17}cm^{-3} before processing to $>5\times10^{18}$cm^{-3} after. In contrast, for a sample with undoped SiGeC layers, the boron profile remains the same as that in the as-grown sample. The different boron diffusion behavior in these three samples (shown in Fig. 5.1) implies that the carbon is crucial in achieving the abrupt boron profiles after oxidation, and that 0.4% substitutional carbon is enough to suppress the OED effect in our process and should thus enable the scaling of vertical p-channel MOSFET's in principle to below sub-50nm channel lengths.

Placing undoped $Si_{1-x-y}Ge_xC_y$ layers near the channel is very effective in preventing boron diffusion during oxidation. However, there is concern as to whether the channel properties are dependent on $Si_{1-x-y}Ge_xC_y$ and the $Si_{1-x-y}Ge_xC_y/SiO_2$ interface. As shown in Fig. 5.7, carbon has diffused into the channel region after all high temperature processing, although boron OED has been suppressed. The carbon level inside the channel region has increased from $< 10^{18}$cm^{-3} in the as-grown sample to 3×10^{18}cm^{-3} after processing. This raises the possibility that the vertical p-channel MOSFET's leakage current may increase.

To evaluate the impact of the SiGeC layers on the electrical properties of vertical p-channel MOSFET's, devices with 20nm undoped $Si_{0.796}Ge_{0.2}C_{0.004}$ layers and channel lengths of $\sim0.5\mu$m were made for comparison with all-Si devices of the same channel length (shown in Fig. 5.2). The channel lengths, channel doping, and gate oxide thickness are identical to those in the all-Si sample. Fig. 5.8, shows the cross-section SEM of a vertical p-channel MOSFET with undoped $Si_{0.796}Ge_{0.2}C_{0.004}$ layers after mesa etching. To more easily view the position of the 20nm SiGeC layers, these layers are selectively etched by using a (1:1:5) ratio of NH_4OH+H_2O_2+H_2O at 60^{o}C for 30min [206] after the mesa etching. The grooves on the picture correspond to the SiGeC layers, which are etched faster than Si, thus showing the estimated channel length between the grooves to be $\sim0.58\mu$m.

The current-voltage and subthreshold characteristics of this device are plotted in Fig. 5.9. I-V curves show a reduced short channel effect than the all-Si device. This is so because

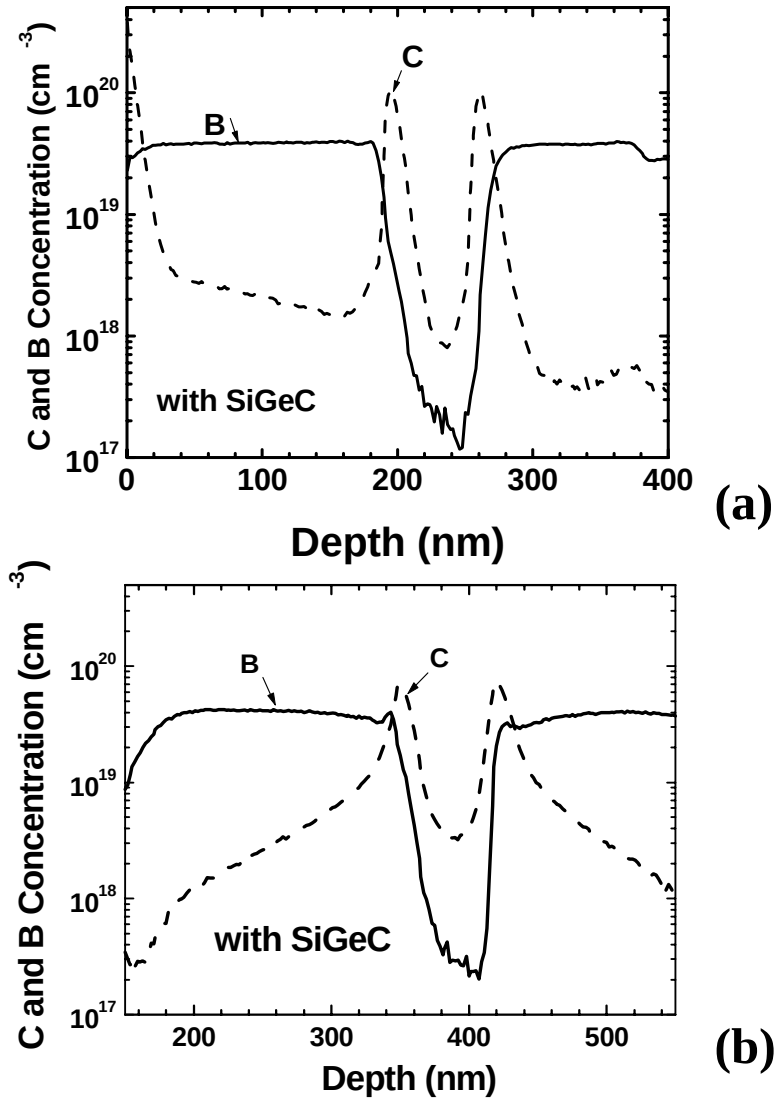


Figure 5.7: Boron profiles from a structure with 20nm undoped $Si_{0.796}Ge_{0.2}C_{0.004}$ layers (Fig. 5.1c), measured by SIMS from (a) an as grown sample, (b) after all high temperature processing (750^oC sacrificial and gate oxidation in wet oxygen for totally 40min and 700^oC 30min poly-silicon deposition).

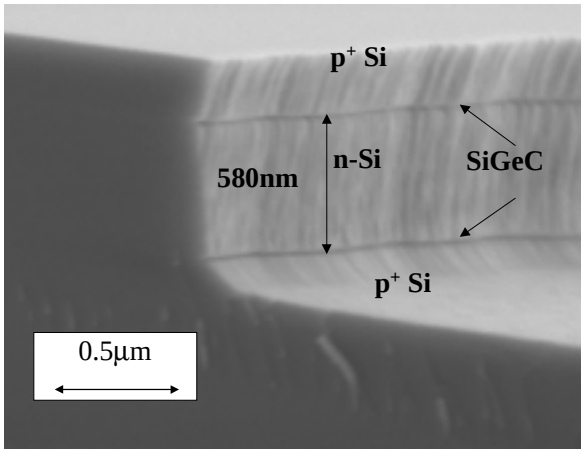


Figure 5.8: Cross-section SEM photomicrograph of epitaxial layers for a vertical p-channel MOSFET with 20nm undoped SiGeC layers after selective etching.

dopant diffusion during gate oxidation causes the actual channel length of the Si device after processing to be shorter than that in the undoped SiGeC device. Also, we notice that although the junction depletion region may penetrate into the undoped SiGeC layers, there is no excess leakage current when compared with all-Si devices. In spite of the positive aspects, there are two major problems involving these devices with undoped SiGeC layers. The first, illustrated on the I-V curve, is the non-symmetric switching of the source and drain. When the drain is on the top of the mesa, i.e. the top p-n junction is reverse biased, high leakage current flows. However, no such problem occurs when the drain is on the bottom. The second problem is that the threshold voltage of the undoped SiGeC device (-4.0V) is much higher in magnitude than that of the Si device (-1.4V), shown in the linear plots of I_{DS} vs. V_{GS} in the inset plot. Furthermore, the subthreshold slope of the undoped SiGeC device (235mV/dec) is worse than that of the Si device (90mV/decade). We will address the second problem in the next section and leave the first problem to Sec. 5.7.

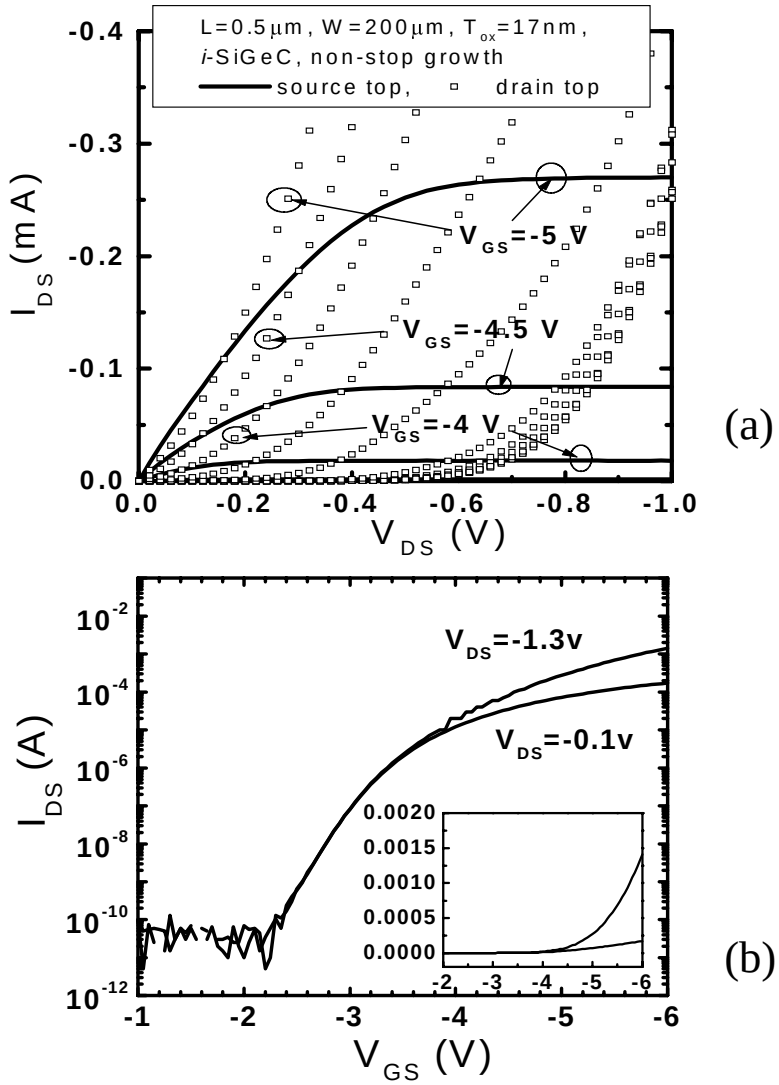


Figure 5.9: (a) Current-voltage and (b) subthreshold characteristics of a vertical p-channel MOSFET (L=0.5μm) with 20nm undoped $Si_{0.796}Ge_{0.2}C_{0.004}$ layers. The epitaxial structure is shown in Fig. 5.1c. The linear scale of I_{DS} vs. V_{GS} is plotted in the inset.

5.6.2 Analysis and SiGeC Oxide Effect

The degraded electrical properties of the vertical p-channel MOSFET's with undoped SiGeC may be caused by three factors. First, carbon atoms may act as scattering or recombination centers and thus influence the carrier motion. Second, the strained $Si_{0.796}Ge_{0.2}C_{0.004}$ layer has smaller bandgap than Si. The band offset at the SiGeC/Si interface may be a barrier to current flow. Third, as mentioned before, these SiGeC layers are not intentionally doped, therefore they are part of the channel. The gate oxide grown on top of the SiGeC layers will affect the channel on- and off-state current. The following experiment was designed to address the third factor. The first two effects will be discussed in Sec. 5.10.

20nm undoped $Si_{0.8}Ge_{0.2}$ and $Si_{0.796}Ge_{0.2}C_{0.004}$ epitaxial layers were grown on a p^- (100) Si substrate. The same oxidation conditions (750^oC wet oxygen) as those in the device fabrication process (Fig. 5.2 and Fig. 5.9) were performed. Test MOS capacitors were made with Al gates, followed by 30min annealing in hydrogen at 400^oC. Fig. 5.10 shows the capacitance-voltage curves measured at high frequency (1MHz), with a Si control sample as reference. The capacitor areas are the same for the three curves. The oxide thicknesses derived from C_{ox} are 10nm, 60nm, and 39nm for Si, $Si_{0.8}Ge_{0.2}$, and $Si_{0.796}Ge_{0.2}C_{0.004}$ respectively, and were confirmed by ellipsometry measurements. The "stretched out" nature of the C-V curves indicates higher interface densities on the SiGe and SiGeC samples. Although the FET's were made on nominal (110) sidewalls and these experiments were carried out on (100) planar surfaces (because of our characterized process for growing SiGeC and SiGe on them), we assume that the characteristics of the higher oxidation rate and poorer interface quality of SiGeC and SiGe are relevant for (110) surfaces as well.

It is well known that the presence of Ge greatly accelerates the wet oxidation of SiGe alloys and that Ge segregation at the oxide/SiGe interface produces a high density of fixed charges and interface traps which adversely affect devices [207, 208, 209]. Recently investigations into the dry [210] and wet [211] oxidation of SiGeC alloys have been published. No obvious influences of carbon on the wet oxidation rate of SiGeC [211] were reported. However, in this work we have observed that the wet oxidation rate of SiGeC is much faster

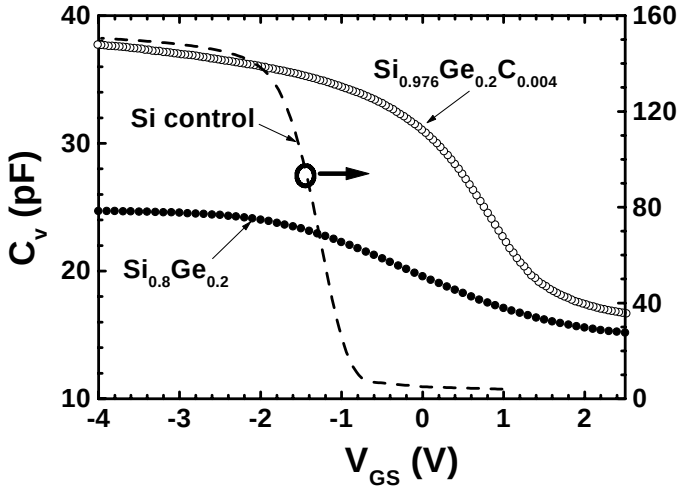


Figure 5.10: High frequency (1MHz) capacitance-voltage characteristics of MOS capacitors with oxide grown at 750^{o}C in wet O_2 on p$^-$ (100) control Si (dotted line), 20nm undoped $Si_{0.8}Ge_{0.2}$ layer (solid circles), and 20nm undoped $Si_{0.796}Ge_{0.2}C_{0.004}$ layer (open circles). Strained SiGe and SiGeC thin films are grown at 625^{o}C on (100) p^- Si substrate. None of these samples are intentionally doped. The gate oxides, calculated from C_{ox}, are 10nm, 60nm, and 39nm thick respectively.

than Si, but relatively slower than SiGe with the same Ge concentration. We believe that the incorporation of carbon, rather than the amount of carbon itself, affects the oxidation mechanism because of its strong influence on film strain and crystalline quality. The difference in the amount of carbon atoms at substitutional sites, and the strain in the SiGeC layers results in the difference of the observed wet oxidation rate of SiGeC in this paper from those in Ref. [211]. The details of the oxidation kinetics of the SiGeC strained layers are currently under study.

The thicker gate oxide and higher interface density probably result in a higher threshold voltage for the short part of the channel over the undoped SiGeC layers, hence explaining the higher observed overall device threshold voltage. The thicker oxides and higher interface density may also account for the less steep subthreshold slopes of the undoped SiGeC vertical p-channel MOSFET's.

5.7 Effect of Phosphorus Doping Profile on Vertical p-channel MOSFET's

In addition to an abrupt boron profile for the source/drain, an abrupt phosphorus profile in the channel is also required in vertical p-channel MOSFET's. In this section, the effect of the n-type dopant profile on vertical MOSFET's is discussed.

In our traditional growth condition (700∼750^{o}C at 6torr with DCS), the doping profile of a typical vertical p-channel MOSFET measured by SIMS, is shown in Fig. 5.11a. Here the PH_3 gas (diluted to 100ppm in H_2) flow rate during growth of the channel region was 5sccm. After turning on the PH_3, the phosphorus concentration increased at a rate of 17nm/decade, and after turning off the gas it fell off at ∼155nm/decade. The residual phosphorus built up in the thin SiGeC layer, and formed a phosphorus spike as high as $\sim 4\times 10^{19}$cm^{-3}. The observed enhancements of residual background P incorporation into the SiGeC layers may be related to the interaction of Ge and residual P on the Si surface or in the growth chamber, which is similar to the phosphorus behavior in SiGe (Chapter 4). Due to the high level of residual phosphorus in the unintentionally doped silicon after turning off the phosphine flow, an extremely highly doped SiGeC layer is inevitable. A larger drain leakage current is thus expected at the resulting n^+p^+ junction in the non-stop growth sample, which is shown in Fig. 5.9a.

The interrupt-growth technique described in Chapter 4 is used here in vertical p-channel MOSFET's to achieve a sharp phosphorus doping profile. In short, after the n-type growth, the wafer is removed from the reactor and its surface is etched. A low temperature cleaning without ultra-high vacuum allows growth to be resumed without any traces of oxygen or carbon at the interrupt interface. In Fig. 5.11b, devices were fabricated with growth sequences interrupted in this manner at the middle of the n-type channel. The improvement in the phosphorus profile compared with that in Fig. 5.11a (without interruption) is obvious. With the interrupt growth, the phosphorus doping now has a slope of 13nm/decade at its top interface (vs. ∼155nm/decade before). The phosphorus spike in the upper SiGeC layer is reduced to $< 10^{18}$cm^{-3}, due to less residual phosphorus after interrupt-growth. Note that

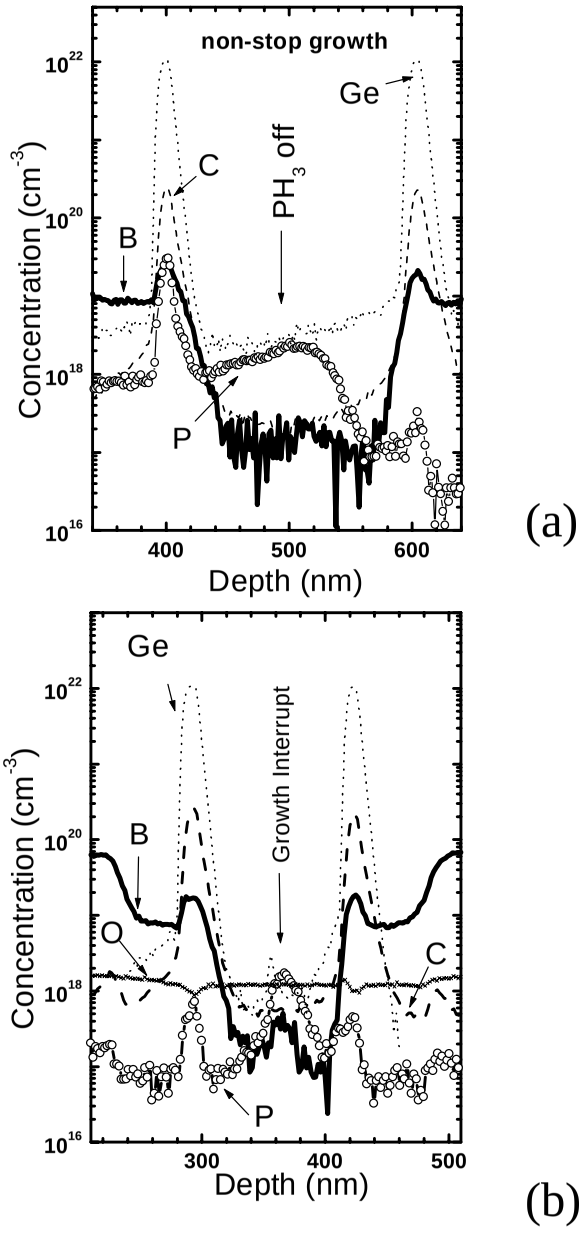


Figure 5.11: Dopant profiles, measured by SIMS, of vertical p-channel MOSFET's with 20nm $Si_{0.796}Ge_{0.2}C_{0.004}$ layers, grown by conventional RTCVD, (a) without and (b) with the interrupt-growth technique.

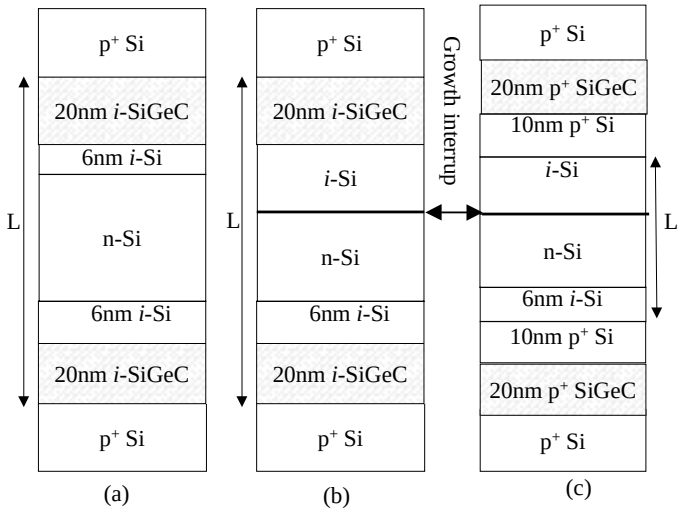


Figure 5.12: Epitaxial layers for vertical p-channel MOSFET's with (a,b) undoped SiGeC and (c) doped SiGeC layers. Growth of structures (b,c) was interrupted in the middle of the channel. Sample (a) is re-plotted from Fig. 5.1c and grown continuously. In sample (c), 10nm p^+ Si layers are also added between the SiGeC and the channel region.

for the interrupt-growth, within the range of SIMS resolution, no oxygen peak is observed at the interruption interface.

Devices where L=0.5μm with undoped SiGeC layers were made, with the same structure as Fig. 5.1c, except that growth interruption was used to control the phosphorus profile. In order to make a clear comparison, the schematic drawing of two different structures is shown in Fig. 5.12a and Fig. 5.12b. Current-voltage and subthreshold characteristics of the device with interrupt-growth is shown in Fig. 5.13. In contrast with Fig. 5.9, the I-V curves are symmetric, without high leakage current for negative bias on top of the mesa, demonstrating the importance of sharp phosphorus profiles. The observed lower saturation current when source is on the top of the mesa is simply due to the higher series resistance on the mesa top. Note that the off-state leakage current for the device with interrupt-growth, shown in Fig. 5.13b, is as low as that in the all Si device (without growth interruption) of Fig. 5.2b, indicating that the interruption does not introduce excess impurities, defects, etc. into the structure and that the undoped SiGeC layers do not increase the device leakage current. However, the threshold voltage, as shown in the inset, is -3.5V, still much higher

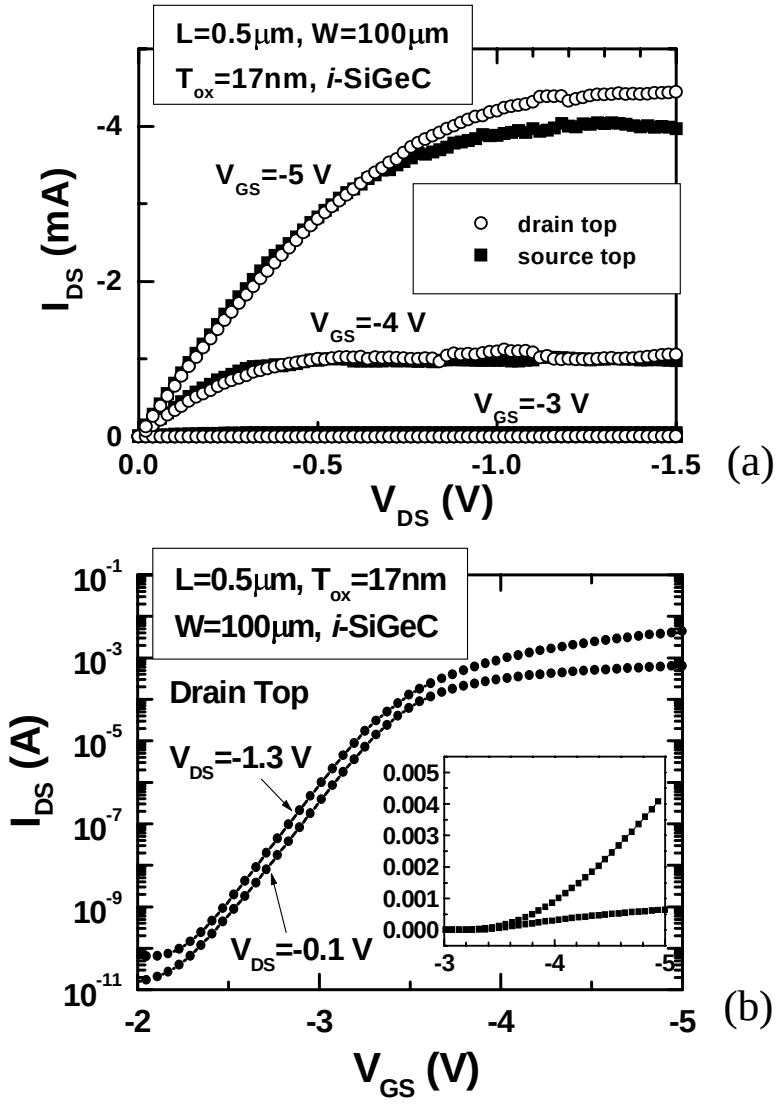


Figure 5.13: (a) Drain current and (b) subthreshold curves of L=0.5μm vertical p-channel MOSFET's with 20nm undoped $Si_{0.796}Ge_{0.2}C_{0.004}$ layers. A linear scale version of I_D vs. V_{GS} is plotted in the inset to determine the threshold voltage. Growth sequences are *interrupted* at the middle of the channel region to achieve sharp phosphorus profiles, as shown in Fig. 5.12b.

than that of an all-Si device (-1.4V). Furthermore, the subthreshold slope (180mV/decade) is also less steep than that of the Si device (90mV/decade).

5.8 Doped SiGeC in the Source/Drain Region

To prevent the deleterious effects of SiGeC oxides on the channel carrier transport, we have fabricated devices where the SiGeC layers were heavily doped with boron to concentration of 2×10^{19} cm^{-3} (as measured by SIMS), separated from the top and bottom p^+ contact layer by 600Å of Si with a $8 \times 10^{18} cm^{-3}$ boron concentration. Thus the SiGeC regions become doped source/drains, and not part of the channel. The structure of these devices is given in Fig. 5.12c. 100Å p^+ Si layers were also grown between the doped SiGeC and channel regions to prevent the penetration of the depletion regions into the SiGeC layers. The growth-interrupt technique was used to grow the n-type channel. It was found that the doped SiGeC layers can still suppress boron diffusion from source and drain into the channel region in vertical p-channel MOSFET's, even though the doped Si regions are closer to the channel than the SiGeC regions. Fig. 5.14a gives the result of SIMS analysis of an as-grown structure with 20nm highly doped SiGeC layers, and Fig. 5.14b gives the SIMS result of the device after all high temperature processing (same conditions as in earlier samples), in which the boron profile remains as sharp as the as-grown sample. Since these SiGeC layers are highly boron doped, and there are doped Si regions outside the SiGeC, the reduction of boron diffusion comes solely from the substitutional carbon suppressing the OED effect rather than the intrinsic diffusion barrier effect of SiGeC layers. Note in this case the suppression is a non-local effect which extends at least 100Å from the SiGeC. A similar non-local effect of SiGeC on TED and OED suppression has also been observed [191, 189].

MOSFET's of L=0.5μm with 20nm p^+ SiGeC layers and interrupt-growth were fabricated to compare with the all-Si control device. The current-voltage and subthreshold characteristics are illustrated in Fig. 5.15. Compared to devices with undoped SiGeC layers and interrupt-growth (Fig. 5.13), the threshold voltages of these devices shift back from -3.5V to

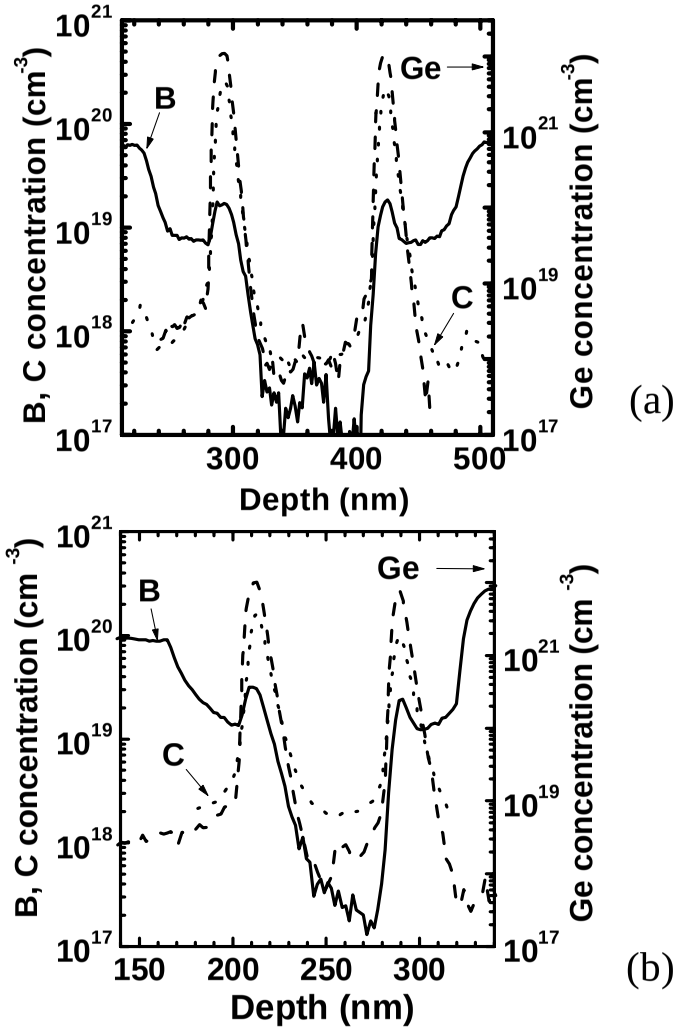


Figure 5.14: Dopant profiles of vertical p-channel MOSFET's with 20nm heavily doped $Si_{0.796}Ge_{0.2}C_{0.004}$ layers, measured by SIMS from (a) an as-grown sample, (b) after all high temperature processing under similar conditions as those in Fig. 5.3b, Fig. 5.6b, and Fig. 5.7b. The device structure is shown in Fig. 5.12c.

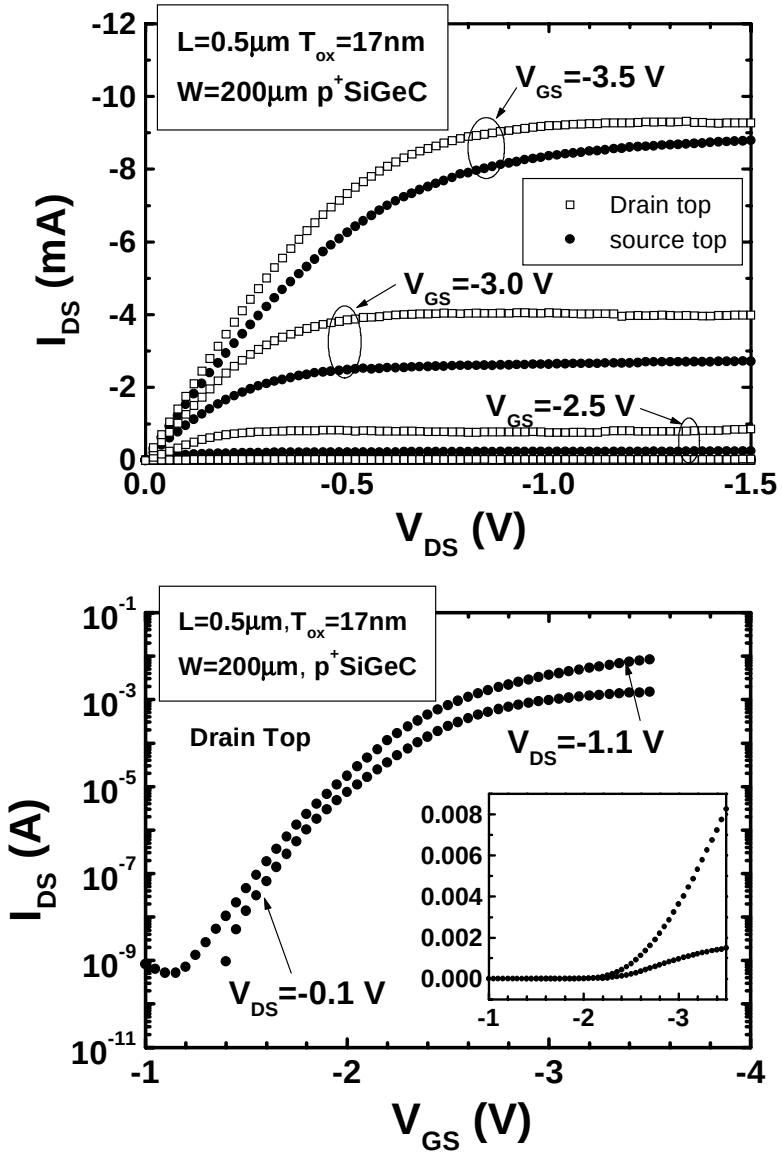


Figure 5.15: Drain current-voltage and subthreshold curves of L=0.5μm vertical p-channel MOSFET's with 20nm heavily boron doped $Si_{0.796}Ge_{0.2}C_{0.004}$ layers. The structure is shown in Fig. 5.12c. The n-type channel region was grown with an interruption to obtain the sharp phosphorus profile. The linear scale of I_{DS} vs. V_{GS} is plotted in the inset.

-2.2V. This is close to an approximate calculation for an ideal long channel device (-1.9V) for ϕ_{ms}=1.04V, a gate oxide thickness of 17nm, and channel doping of $\sim 1.5\times10^{18}\text{cm}^{-3}$. The lower threshold voltage (-1.4V) of the all-Si control device (Fig. 5.2) could be a short channel effect, considering an overall shorter channel length due to significant boron diffusion. Also, phosphorus oxidation-enhanced-diffusion will cause the all-Si control devices have lower doping levels after all high-temperature processing. SiGeC suppression of the phosphorus OED effect will be discussed in Chapter 6. To reiterate, the devices with heavily doped SiGeC layers and interrupt-growth have off-current as low as the all-Si devices, indicating that the SiGeC layers do not lead to excess leakage current due to defects, low lifetimes, etc. Furthermore, interrupt-growth does not induce any leakage current due to impurities or contamination.

5.9 Sub-100nm Vertical p-channel MOSFET's

Combining the technologies discussed to this point of highly-doped SiGeC in source/drain (for boron profile control during processing) and interrupt-growth (for phosphorus profile control during epitaxy), sub-100nm vertical p-channel MOSFET's have been fabricated for the first time. Fig. 5.16 shows the SIMS results for a vertical p-channel MOSFET with L=80nm after all high-temperature processing. L is defined as in Sec. 5.3. The estimated side-wall gate oxide thickness is 10.4nm and the peak channel doping level is $1\times10^{18}\text{cm}^{-3}$. For reference, the growth sequence of this sample is attached in Appendix A. Well-behaved drain currents and subthreshold curves for these transistors are given in Fig. 5.17. A maximum transconductance of 100mS/mm at V_{DS}= -1.1 V has been achieved (Fig. 5.18), which is reasonable considering the thick gate oxide. The subthreshold slope is 88mV/decade. The subthreshold curve of this device is also superposed on to Fig. 5.4 to allow comparison with the device with undoped SiGeC and similar channel length. It is obvious that the threshold voltage and subthreshold slope are dramatically improved.

For L=65nm vertical p-channel MOSFET's, channels are doped to $2.5\times\ 10^{18}\ \text{cm}^{-3}$ to suppress punch-through. Dopant profiles measured by SIMS after all high-temperature

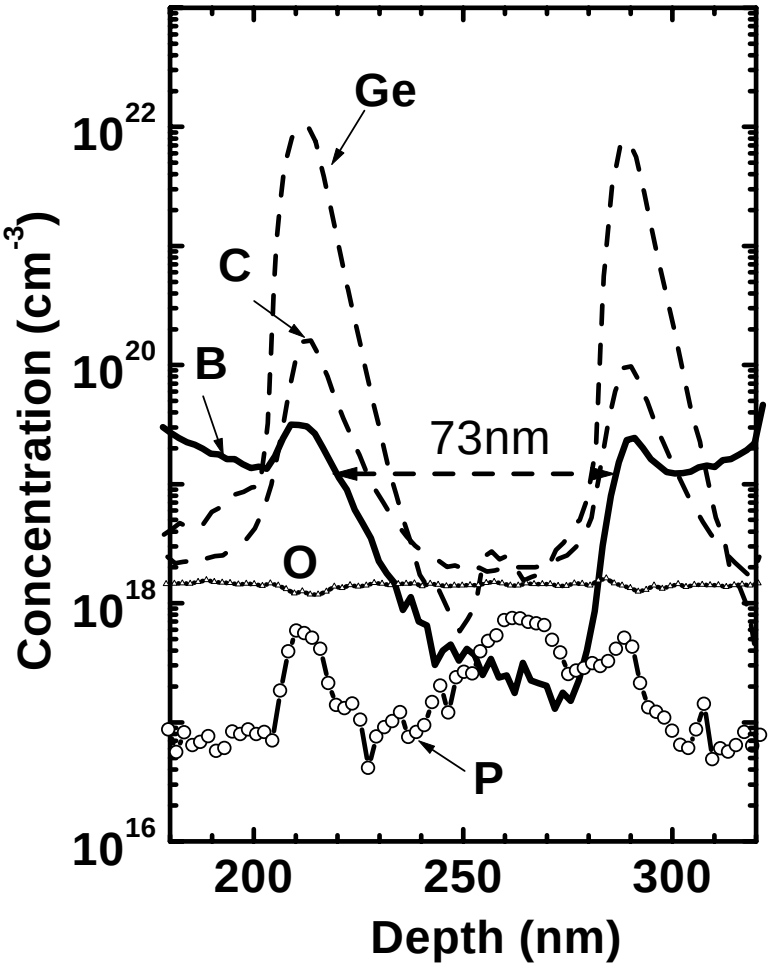


Figure 5.16: Dopant profiles measured by SIMS after all high temperature processing for a vertical p-channel MOSFET with L=80nm. L is determined by the distance between the two p^+ regions, where boron concentration falls to $1/\sqrt{2}$ of its maximum value, multiplied by 1.1 ($1/cos25^o$).

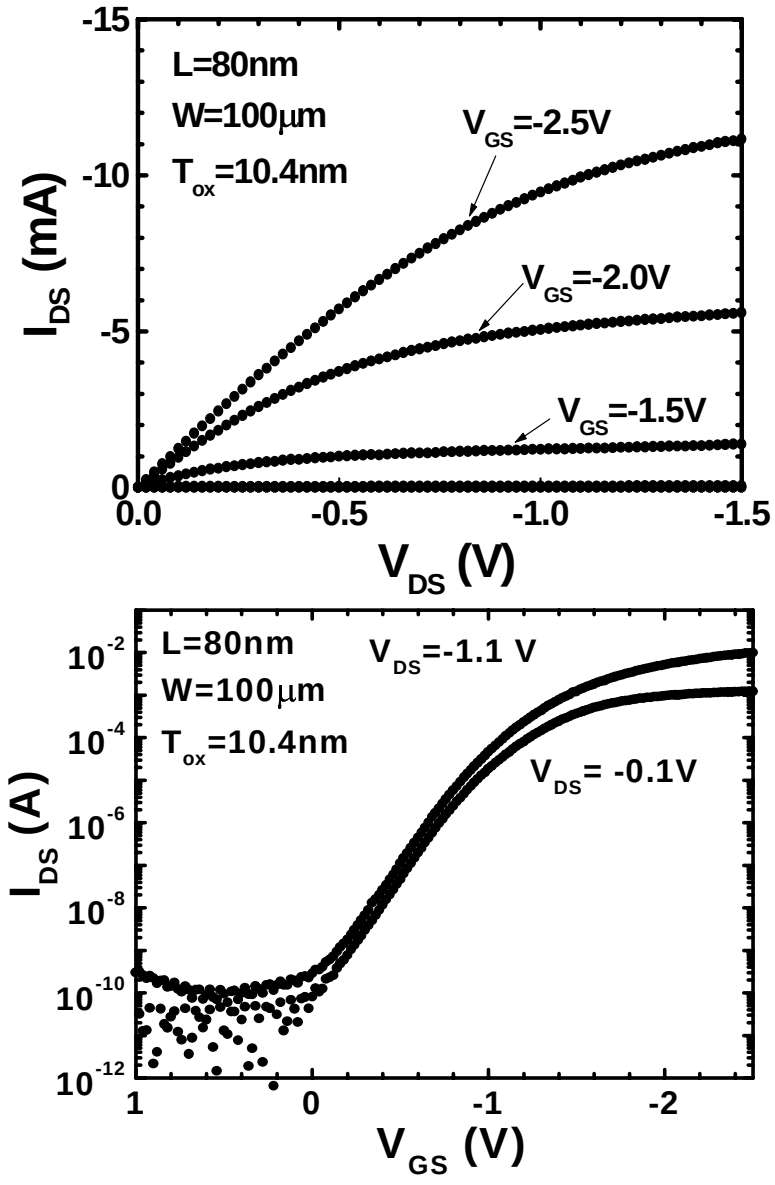


Figure 5.17: Current-voltage and subthreshold characteristics of a vertical p-channel MOSFET with L=80nm. Doped SiGeC source/drains are used to control boron diffusion and growth interruption is implemented to control phosphorus profile.

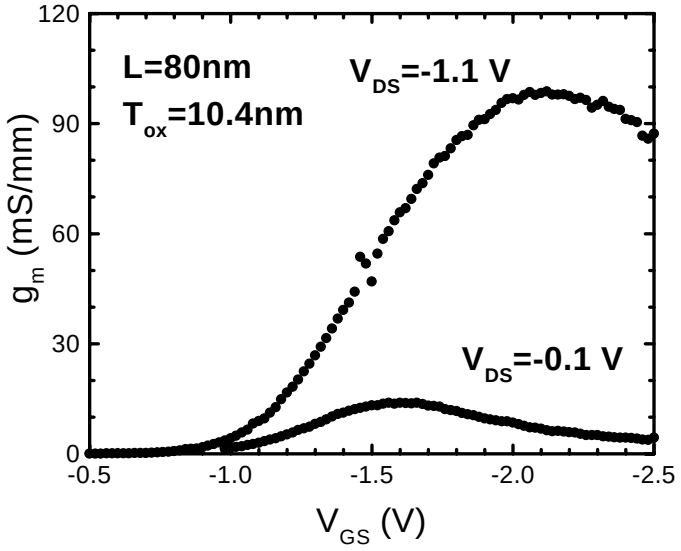


Figure 5.18: Transconductance of a vertical p-channel MOSFET with L=80nm.

processing are shown in Fig. 5.19. Current-voltage and subthreshold characteristics are plotted in Fig. 5.20. With a 10.4nm side-wall gate oxide, transconductance is 136mS/mm at V_{DS}= -1.1 V. The subthreshold slope is 190mV/decade due to the high level of channel doping and the thick gate oxide. With a 3nm sidewall gate oxide, the subthreshold slope would be 84mV/decade, assuming the same interface density.

To study the limit of vertical p-channel MOSFET scaling using boron diffusion suppression by the p^+ SiGeC layers, we also fabricated a device with a 25nm channel length. The center of the channel is doped with phosphorus to 4×10^{18}cm^{-3}. For such a short channel device, the boron doping levels in the channel can not be accurately resolved due to the SIMS knock-on effects. The channel length was estimated using the same definition as for the other devices. The SIMS results of the doping profiles are shown in Fig. 5.21. From the I-V curves in Fig. 5.22, the source and drain are not shorted, in contrast with devices without SiGeC layers. The device current was controlled by the gate above the threshold, although it suffers from the onset of punch-through. For vertical MOSFET's, thickness and doping density of a lightly doped drain (LDD) can be accurately controlled by our epitaxy

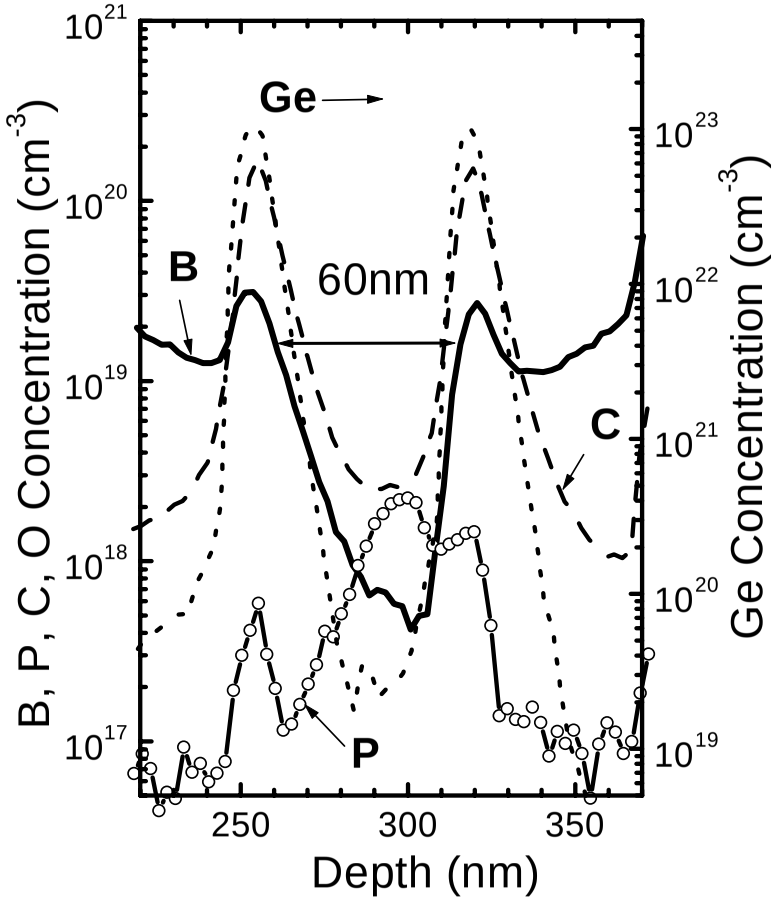


Figure 5.19: Dopant profiles measured by SIMS after all high temperature processing for a vertical p-channel MOSFET with L=65nm. L is determined by the distance between the two p^+ region, where boron concentration falls to $1/\sqrt{2}$ of its maximum value, multiplied by 1.1 $(1/cos25^o)$.

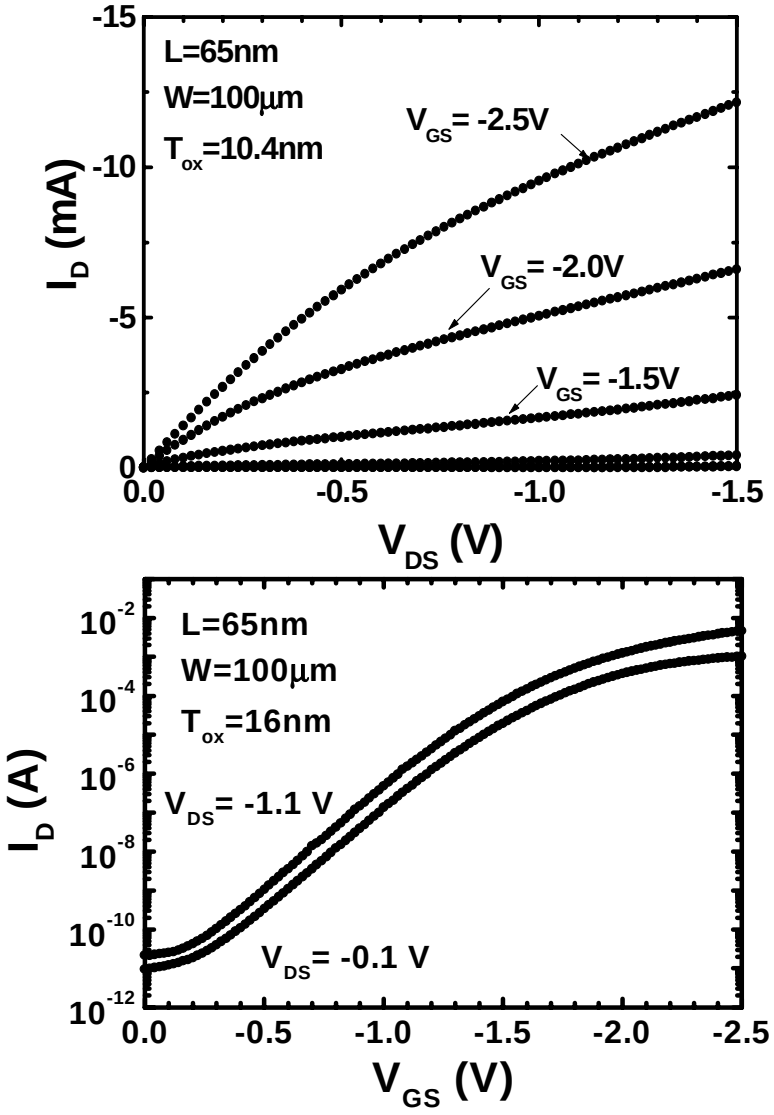


Figure 5.20: Current-voltage characteristics of vertical p-channel MOSFET's with L=65nm. Doped SiGeC source/drains are used to control boron diffusion and growth interruption is implemented to control the phosphorus profile.

technology rather than the shallow implantation seen in the fabrication of conventional lateral MOSFET's. Therefore, optimizing the LDD conditions may help to reduce the off-state leakage current. Improvement at such a short channel length would also be expected by using an ultra-thin pillar rather than a wide mesa so that the surrounding gate can fully deplete the channel region. It is expected that no punch-through would be observed even without a high level of channel doping, and better subthreshold slope will be also achieved, as discussed in Sec. 2.2.

The characteristics of various device structures of vertical p-channel MOSFET's are summarized in Table 5.1. In this work, the gate oxides are relatively thick (>100Å) and the side-walls are along [110] crystal directions. Estimation for the subthreshold slopes with thinner gate oxide (3nm), extracted from our current experimental data, is also listed in Table 5.1 for comparison. With a thinner gate oxide, the subthreshold slope will be improved. The Drain-Induced Barrier Lowering effect $DIBL = V_{th}(V_{DS} = -0.1V) - V_{th}(V_{DS} = -1.0V)$, defined in Sec. 2.1.2, is also listed in Table 5.1 for the various devices.

5.10 Discussions

Two fundamental issues relevant to our use of SiGeC are: 1) the effect of these layers, especially carbon-related precipitation or diffusion, on lifetime and leakage current and 2) the effect of the Si/SiGeC heterojunction.

5.10.1 Leakage Current After Introducing SiGeC Layers

Introducing $Si_{0.796}Ge_{0.2}C_{0.004}$ layers in vertical p-channel MOSFET's with carbon atoms above the solid solubility limit ($<10^{18}cm^{-3}$) to suppress boron diffusion by capturing silicon self-interstitials may lead to the formation of carbon-interstitial pairs, which could act as scattering or recombination centers and thus influence the carrier properties [196]. In recent publications, effects of carbon on the electrical properties of heterojunction bipolar transistors (HBT) [191, 212] have been studied. Large increases in base currents due to the formation of deep level defects and a reduced lifetime in the base-emitter space-charge

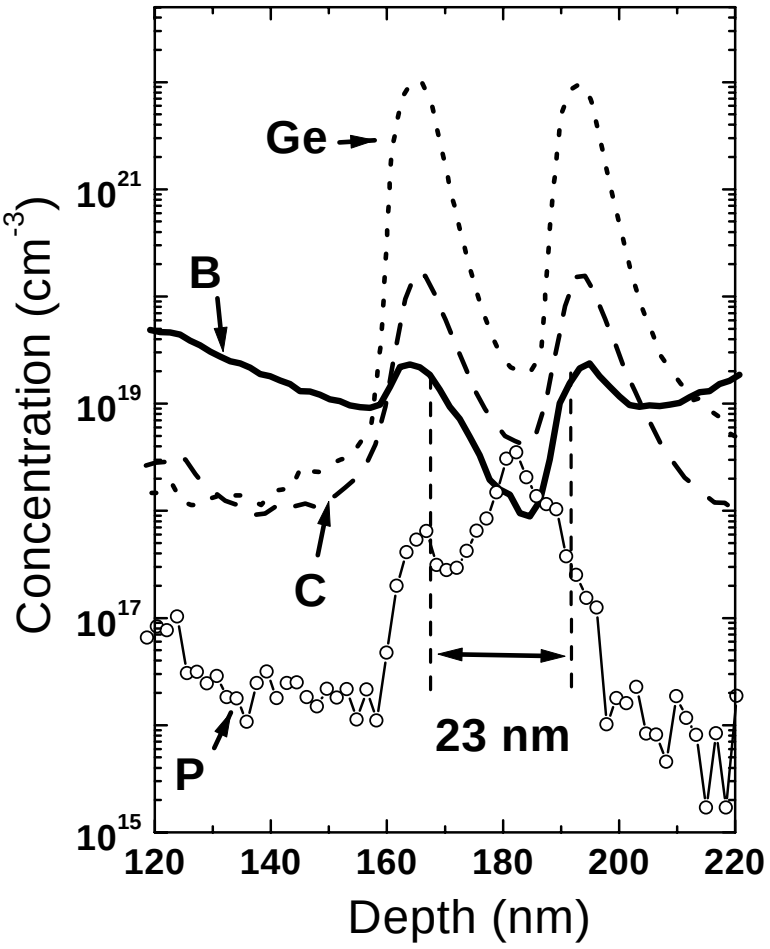


Figure 5.21: Dopant profiles measured by SIMS after all high temperature processing for a vertical p-channel MOSFET with L=25nm. L is determined by the distance between the two p^+ region, where boron concentration falls to $1/\sqrt{2}$ of its maximum value, multiplied by 1.1 ($1/cos25^o$).

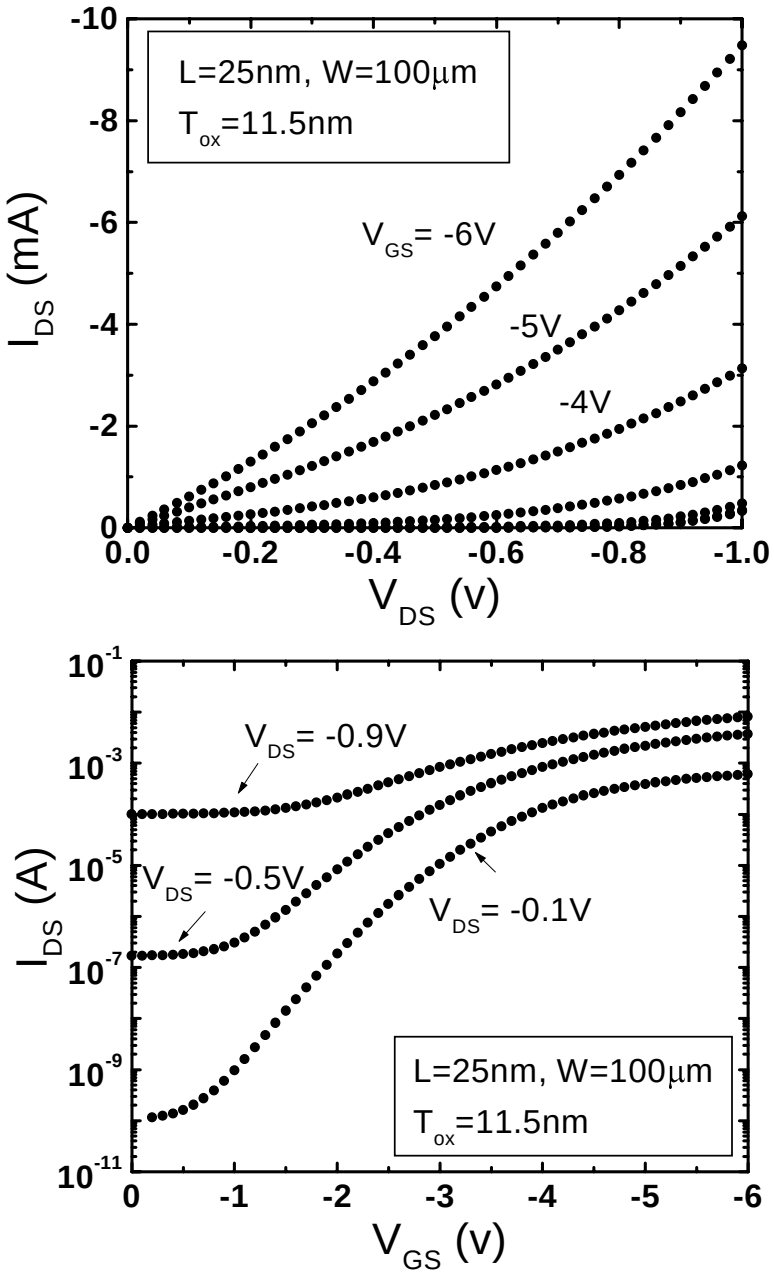


Figure 5.22: Current-voltage and subthreshold characteristics of a vertical p-channel MOSFET with L=25nm. Doped SiGeC source/drains are used to control boron diffusion and growth interruption is implemented to control the phosphorus profile.

Sample	Structure	L (μm)	t_{ox} (nm)	Peak Channel Doping (cm^{-3}) after processing	V_T (V)	I_{off} (A/μm) at V_{DS}=-1V	S_t (mV/decade) at V_{DS}=-0.1V	Predicted S_t (mV/decade) for t_{ox}=3nm	DIBL (mV)
#2332	all Si#	0.5	17	1.0×10^{18}*	-1.4	5×10^{-12}	90	65	95
#2409	*i*-SiGeC#	0.5	17	1.4×10^{18}*	-4.0	5×10^{-11}	235	91	75
#2554	*i*-SiGeC	0.5	17	1.4×10^{18}*	-3.5	10^{-12}	180	81	71
#2556 /2557	*p*-SiGeC	0.5	17	1.4×10^{18}*	-2.0	5×10^{-12}	150	76	78
#2411	all Si	0.07	23	1.2×10^{18}	source/drain shorted				
#2410	*i*-SiGe	0.1	23	1.2×10^{18}					
#2412	*i*-SiGeC	0.1	23	1.5×10^{18}	-4.0	6×10^{-12}	400	104	-
#2566 /2569	p^+-SiGeC	0.08	10.4	1.0×10^{18}	-1.3	10^{-12}	88	68	142
#2599 /2608	p^+-SiGeC	0.065	16	2.5×10^{18}	-1.7	10^{-13}	190	84	165
#2616	p^+-SiGeC	0.025	11.5	4×10^{18}	punch-through				

* *estimated*
\# *non-stop growth*

Table 5.1: Comparison of device performance of various vertical p-channel MOSFET's with 200Å doped and undoped $Si_{0.796}Ge_{0.2}C_{0.004}$ diffusion barriers, along with all silicon devices and undoped $Si_{0.8}Ge_{0.2}$ devices. Some devices are used growth-interruption to achieve sharp phosphorus doping profiles. Channel doping levels are from SIMS after all high temperature processing, except where indicated. The prediction of subthreshold slopes for devices made with thinner gate oxides are also listed.

region were observed in Ref. [191] for carbon levels of $\sim 5\times10^{20}\text{cm}^{-3}$. However, Osten *et al.* reported that the measured base current of the HBT is not affected by the position of the incorporated carbon (20nm, $5\times10^{19}\text{cm}^{-3}$ outside or within the base), and that the base current is similar to that in SiGe HBT's [212]. Conventional lateral n-channel MOSFET's with carbon-implanted channels were reported by Ban *et. al.* [213] and Gossmann *et. al.* [214]. Poor boron activation and large off-state leakage current were shown when carbon dose levels were above a threshold of 10^{14}cm^{-2}.

In the fabrication of our vertical p-channel MOSFET's, the high temperature processes are controlled to below 800^oC. This is very important because above this temperature, three deleterious effects can occur. First, the carbon atoms can move from their substitutional sites to interstitial sites [215], leading to deep levels. Second, SiC precipitates can form because of the low solubility of carbon and because SiC is the only stable compound on the Si-C binary phase diagram. Lastly, the 20nm $Si_{0.796}Ge_{0.2}C_{0.004}$ layers may suffer strain-relaxation and generate misfit dislocations at the SiGeC/Si interfaces. In devices made with 20nm undoped $Si_{0.796}Ge_{0.2}C_{0.004}$ layers, the drain-channel depletion region will penetrate across the SiGeC layers. However, in Fig. 5.9 and for L=0.5μm, the off-state current is as low as that in the Si control device (Fig. 5.2). In contrast to the MOSFET's with carbon implanted channels by Ban *et al.*[213], Gossmann *et. al.* [214] and HBT's with SiGeC bases in Ref. [191], no significant leakage currents from the SiGeC depletion region is observed in this work. Furthermore, for the device with the same structure but after using the interrupt-growth technique for phosphorus profile control (Fig. 5.13), the leakage current is still as low. These results indicate that the two new technologies we introduced in this work, namely SiGeC source/drains and interrupt-growth, do not adversely affect device leakage current.

It is well known that carbon can diffuse fast in silicon-based materials [196]. After the sacrificial and gate oxidation at 750^oC, carbon atoms diffuse from the 20nm $Si_{0.796}Ge_{0.2}C_{0.004}$ layers to the channel region, as shown in Fig. 5.7 for undoped SiGeC and Fig. 5.14 for doped SiGeC. The carbon concentration in the channel increases from $8\times10^{17}\text{cm}^{-3}$ in the as-grown samples to $2\sim3\times10^{18}\text{cm}^{-3}$ after process. But for vertical p-channel MOSFET's

with SiGeC layers (as summarized in Table 5.1), with L=0.5μm in Fig. 5.9 and Fig. 5.13 (undoped SiGeC) and Fig. 5.15 (doped SiGeC); with L=80nm in Fig. 5.17 (doped SiGeC); with L=65nm in Fig. 5.20 (doped SiGeC), no evident junction leakage is observed compared with the Si control sample (L=0.5μm in Fig. 5.2). Within fabrication variations, the off-state currents are between 5×10^{-11} and 10^{-13}A/μm at V_{DS}=-1V. Recently it was found that carbon diffusivity decreases in both oxidizing and non-oxidizing conditions when carbon concentration increases [189, 188]. Further studies are required to investigate the effect of carbon concentration in the SiGeC layers on the device performance of vertical p-channel MOSFET's, and what minimum carbon concentration might be used.

5.10.2 Effect of Carbon on Carrier Mobility

There is concern that the active dopant concentration and carrier mobility may be reduced after addition of carbon. Substitutional boron may react with interstitial carbon or interstitial boron and form deep levels[216]. Osten *et al.* reported that for carbon concentrations less than 10^{20}cm^{-3}, the concentration of electrically active boron and the hole mobility are not affected in highly boron doped SiGeC layers [216]. Chang *et al.* reported that hole mobility in modulation-doped SiGeC channels grown from the same RTCVD system as the present work, decreases as carbon fraction increases [217] at 10K due to the scattering induced by carbon. However for carbon fraction less than 0.3%, no difference is observed for temperatures higher than 100K. The transconductances measured in the vertical p-channel MOSFET's fabricated here are compatible with conventional lateral MOSFET's, even with rough side-walls and thick gate oxides, implying that the carbon level introduced in the devices does not affect carrier transport.

5.10.3 $Si_{1-y}C_y$ vs. $Si_{1-x-y}Ge_xC_y$ As a Substitutional Carbon Source

The strained $Si_{0.796}Ge_{0.2}C_{0.004}$ has a bandgap 0.15eV lower than Si, with most of the offset in the valence band[218]. It has been reported that a narrower bandgap in the source region reduces the floating body effects on n-channel MOSFET's on SOI [219], but their

effect in present p-channel devices is uncertain, because holes have a lower avalanche coefficient than electrons. However, the p^+ Si/p^+ SiGeC heterojunction might introduce some series resistance as carriers must tunnel through a very thin barrier of height ~0.15eV. There are two approaches which can be taken to increase the tunneling current and reduce series resistance. First, doping the Si/SiGeC layers to higher concentrations can reduce the barrier width. Second, the same mechanism for suppressing boron diffusion (sinking of Si interstitials) may take place in $Si_{1-y}C_y$ as in $Si_{1-x-y}Ge_xC_y$, as it is the substitutional carbon atoms that suppress OED/TED effects. Reduced OED/TED effect has been reported for carbon incorporation in silicon (without Ge) by MBE [220, 188]. Therefore replacing $Si_{1-x-y}Ge_xC_y$ with $Si_{1-y}C_y$ should reduce the barrier height.

It is reported that the valence band off-set between $Si_{1-y}C_y$ and silicon is only 20~25meV for carbon concentrations of 1% [218, 221]. Furthermore, wet thermal oxidation of strained $Si_{1-y}C_y$ ($y \leq 0.02$) is similar to that of silicon [222], in contrast with that of the fast oxide growth rate of $Si_{1-x-y}Ge_xC_y$ we observed. Therefore, $Si_{1-y}C_y$ is preferable to $Si_{1-x-y}Ge_xC_y$ to fully eliminate the heterojunction and faster oxidation effects. However, when using DCS and SiH_4 as silicon sources, incorporation of substitutional carbon is difficult. As mentioned in Sec. 5.5, low temperatures ($\leq 600^oC$) and high growth rates are required to achieve a high fraction of substitutional carbon incorporation. At temperatures less than 700^oC, however, the growth rate of $Si_{1-y}C_y$ is very slow using SiH_4 or DCS as the silicon source by RTCVD, in contrast with $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ [176]. Thus $Si_{1-x-y}Ge_xC_y$ has been chosen for this work, but $Si_{1-y}C_y$ may be an attractive option in the future by using Si_2H_6 or other more highly reactive gas sources.

5.11 Summary

In summary, vertical p-channel MOSFET's have been fabricated using *in situ* doped epitaxial layers grown by RTCVD and wide mesa etching. By introducing 20nm $Si_{0.796}Ge_{0.2}C_{0.004}$ layers in the source and drain, boron diffusion has been suppressed during the growth of the sidewall gate oxide. By using a growth interrupt technology, phosphorus profiles in the

channel have been improved. The effect of SiGeC layers on the electrical properties of the MOSFET's has been studied. Highly boron doped SiGeC layers are preferable to undoped SiGeC layers to minimize the influence of SiGeC oxidation on the carrier transport. Vertical p-channel MOSFET's with channel lengths down to 25nm have been demonstrated. No adverse effect of the SiGeC on leakage current or on drive current in devices with doped SiGeC has been observed. Finally, improvement in the characteristics of very short (L=25nm) vertical p-channel MOSFET's are expected when a thin Si pillar with a surrounding gate and $Si_{1-y}C_y$ without Ge are used.

Chapter 6

Current and Future Work on Vertical MOSFET's

In this chapter the current and ongoing work are first presented, as well as associated problems and possible solutions. The ongoing work includes the fabrication of vertical n-channel MOSFET's (Sec. 6.1) and studies of the thermal stability of vertical devices (Sec. 6.2). Vertical n-channel MOSFET's with long channel length have been demonstrated, while devices with sub-100nm channel length are still under development.

In Chapter 5, SiGeC layers are introduced into the vertical p-channel MOSFET's to suppress dopant diffusion from the source and drain into the channel region. In this chapter, it is shown that the vertical devices with SiGeC layers have good thermal stability as well. Little dopant diffusion has been found in the vertical p-channel MOSFET's after 3hr 800^{o}C annealing in N_2.

The application of vertical MOSFET's is not limited to the fabrication of double-gate/surrounding-gate MOSFET's or the vertical cells in DRAM (Chapter 2). The vertical structure also provides a very unique method by which to study heterojunction devices. In Sec. 6.3, several possible Si/SiGe heterojunction MOSFET's are proposed.

6.1 Vertical n-channel MOSFET's

Sub-100nm vertical p-channel MOSFET's on the side walls of wide mesa have been demonstrated in the previous chapter. Vertical n-channel MOSFET's with similar structure can also be fabricated, in principle. In this section, the fabrication process of vertical n-channel MOSFET's will be presented first, and then long channel devices will be demonstrated. Finally, the major problems associated with vertical n-channel MOSFET's (i.e. floating-body effects), will be discussed.

6.1.1 Process Development of Vertical n-channel MOSFET's

In the present work, vertical n-channel MOSFET's with $\sim 0.5\mu$m channel lengths have successfully been fabricated. For these long channel devices, similar to the vertical p-channel MOSFET's, epitaxial layers may only consist of silicon (without SiGeC). The challenge involved with n-channel MOSFET's is how to achieve high source/drain doping level using phosphorus as n-type dopant source in an RTCVD system. In Chapter 4, sharp phosphorus dopant transitions have been demonstrated by using an interrupt-growth technique. This technique may reduce the series resistance in the vertical n-channel MOSFET's. However, lowering the series resistance will require higher level of source/drain doping. Growing high quality silicon epitaxy with a high phosphorus doping level ($> 10^{20}$cm^{-3}) in an RTCVD system still remains a problem.

To simplify the process in the initial studies, all the epitaxial layers were grown continuously in the fabrication of the long channel vertical MOSFET's presented in this section. The n^+pn^+ silicon layers were grown on an n^- silicon (100) substrate. During the growth, a 26sccm flow of DCS was used as the silicon source and the growth pressure was maintained at 6Torr. Note that no SiGeC layers were added in these devices. After a 1000^oC bake in H_2, a $\sim 0.5\mu$m n^+ Si buffer layer was grown with a PH_3 flow of 3.15×10^{-2}sccm. Subsequently, the temperature was lowered to 800^oC and later further to 700^oC with a reduced PH_3 flow rate of 7×10^{-3}sccm, before starting the growth of channel region. The channel was grown at 750^oC. 1.5×10^{-4}sccm of B_2H_6 was used as boron precursor, resulting an *in-situ* boron

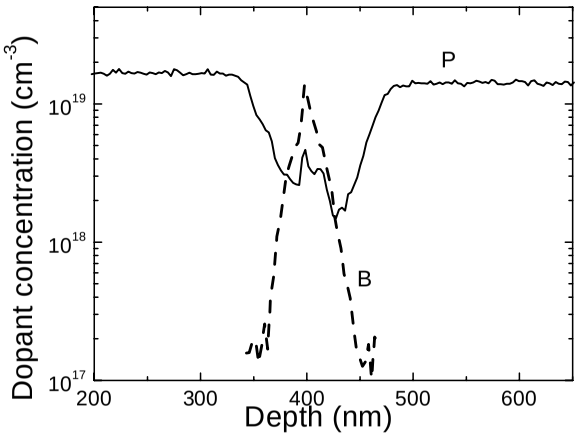


Figure 6.1: Dopant profile measured by SIMS from an as-grown vertical n-channel MOSFET with L∼100nm. No SiGeC layers were added in this device.

doping level of 3.5×10^{18}cm^{-3} in the channel. After turning off the B_2H_6, 7×10^{-3}sccm of PH_3 was turned on at 700^{o}C. The top n$^+$ contact was grown at 800^{o}C with 3.15×10^{-2}sccm of PH_3. From the SIMS measurement after epitaxy, the phosphorus doping level in the source and drain is 1.5×10^{19}cm^{-3}, which should be similar to the profile shown in Fig. 6.1 (L∼100nm).

After epitaxy, the silicon mesa was created using RIE, with the side walls along the (100) directions. As in Chapter 5, the mesa here is also wide ($\geq50\mu$m), rather than a thin pillar. Gate oxide was grown at 750^{o}C in wet oxygen to give a 13nm thickness on a control (001) silicon substrate. The gate material is *in-situ* doped n$^+$ polysilicon deposited in the RTCVD system at 700^{o}C with 3.15×10^{-2}sccm of PH_3 and 13sccm of SiH_4. The end process is the same as for the p-channel devices.

6.1.2 Characteristics of Vertical n-channel MOSFET's

The long channel nMOS has well-behaved on current. Fig. 6.2 shows the drain current and the subthreshold characteristics of a vertical n-channel MOSFET with a 0.5μm channel length and a wide mesa. No SiGeC layers are introduced in this device. The low current at the linear region on the drain current-voltage plot may be due to the insufficient source/drain doping level. The subthreshold leakage current is around 5nA/cm and the

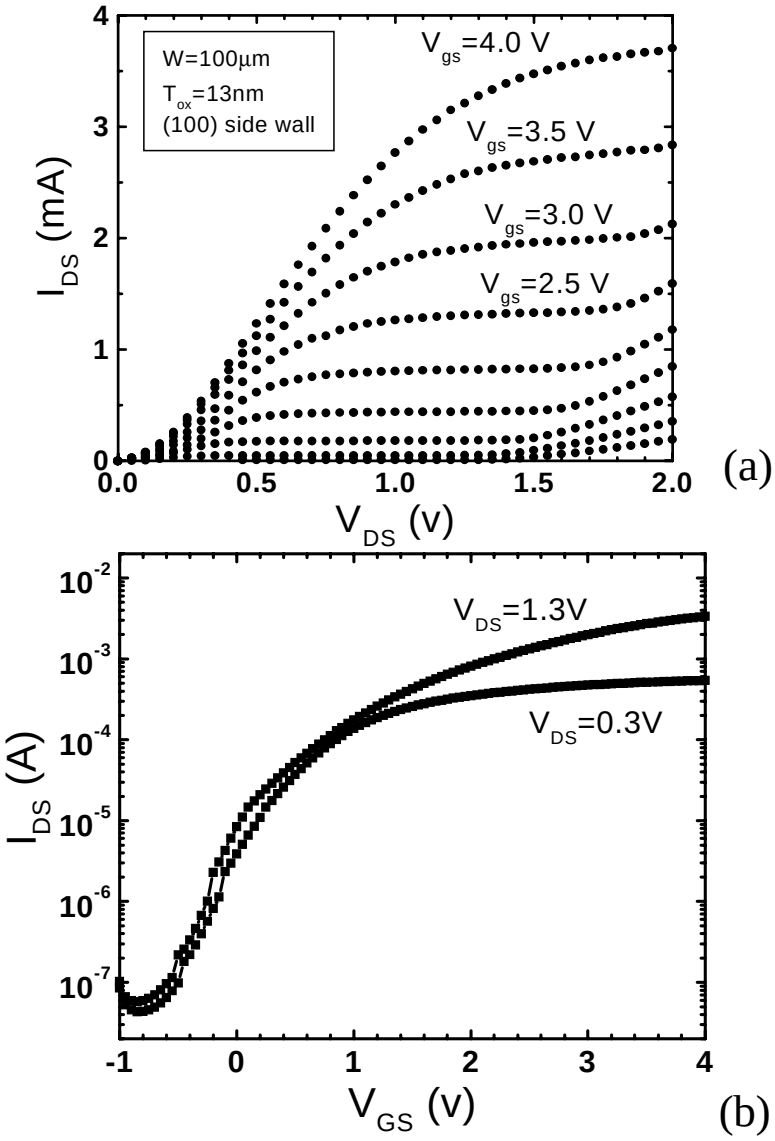


Figure 6.2: (a) Drain current-voltage and (b) subthreshold characteristics of a vertical n-channel MOSFET with Si epitaxial layers only. The channel length is about 0.5μm.

subthreshold slope is 0.2V/decade due to the thick gate oxide and high channel doping. Assuming a negligible interface density, the subthreshold slope calculated from Eqn. 2.5 is 0.18V/decade for the same structure. In the future, higher source/drain dopings should be used to reduce the series resistance and thinner gate oxides should be used to reduce the subthreshold slope. Phosphorus ion implantation after the mesa RIE may be used to increase the doping level. The consequent transient-enhance-diffusion of phosphorus during the high temperature annealing after implantation may be suppressed by introducing SiGeC layers, and will be further discussed in the next section.

6.1.3 Oxidation-Enhanced-Diffusion of Phosphorus

To achieve vertical n-channel MOSFET's with sub-100nm channel lengths, phosphorus dopant diffusion has to be controlled during the gate oxidation or ion implantation. Phosphorus, like boron, diffuses by a self-interstitial mechanism [183]. Thus, phosphorus diffusion is also greatly enhanced during oxidation (OED) [223] and implantation/annealing (TED) [190]. For the previously demonstrated vertical n-channel MOSFET's using a similar approach, the channel lengths were not under control, especially for the devices with sub-100nm final channel lengths. That is, the channel length was 170nm in the as-grown structure in order to obtain a 70nm channel length after processing [77]. Fig. 6.3 shows the phosphorus doping profile in a vertical nMOS device before and after gate oxidation, predicted by a Tsuprem-4 [126] simulation. The sacrificial and gate oxidation are both at 750^oC in wet oxygen for 20min. After oxidation, a 15min nitrogen annealing was done at the same temperature. Assuming a channel doping of 10^{18}cm^{-3}, the distance between the two pn channel junctions is reduced from 110nm to 65nm. Similar to the boron diffusion, the phosphorus profile remains the same as that from the as-grown sample if there is no oxidation-enhanced-diffusion effect.

In the present work, SiGeC layers are also introduced in the source/drain to suppress phosphorus oxidation enhanced diffusion, as was done for boron in the vertical p-channel MOSFET's. Fig. 6.4 gives the SIMS measurements of the dopant profiles in a L=50nm vertical n-channel MOSFET before and after gate oxidation. No significant phosphorus

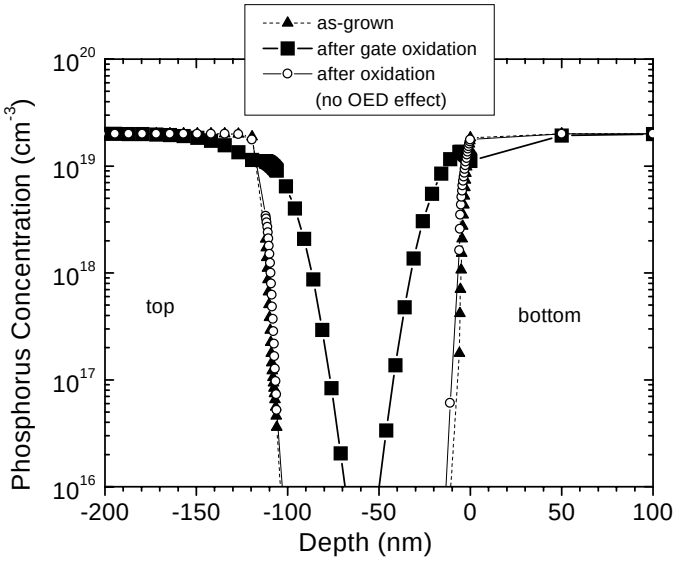


Figure 6.3: Phosphorus profile of an n-channel vertical MOSFET simulated by Tsuprem-4 before and after the sacrificial and gate oxidation. The oxidation were performed at 750^{o}C in wet O_2 for 20min, and then annealed in N_2 for 15min.

diffusion is observed. In contrast, phosphorus diffusion in all Si devices is observed, shown in Fig. 6.5. Sub-100nm vertical n-channel MOSFET's with SiGeC layers are currently under investigation.

6.1.4 Floating-body Effect

For the wide mesa structure, the center is far from the gates. As such, the punch-through problem was found to occur in the vertical p-channel MOSFET's with L=25nm. Therefore higher channel doping is necessary. This problem will also affect n-channel MOSFET's. Furthermore, parasitic lateral bipolar transistors will also enhance the leakage current at ultra-short channel lengths [224]. However, for vertical n-channel MOSFET's, shown in Fig. 6.6, anomalous subthreshold characteristics are observed even for L=0.5μm. When the drain bias is raised above 1.5V, the subthreshold slope decreases as the drain bias increases, which is the opposite behavior of the short-channel effect. When the drain bias reaches 2.2V, the slope is abnormally sharp (20mV/decade). A similar problem has also been observed in partially-depleted SOI MOSFET's [225, 226] and is attributed to the floating

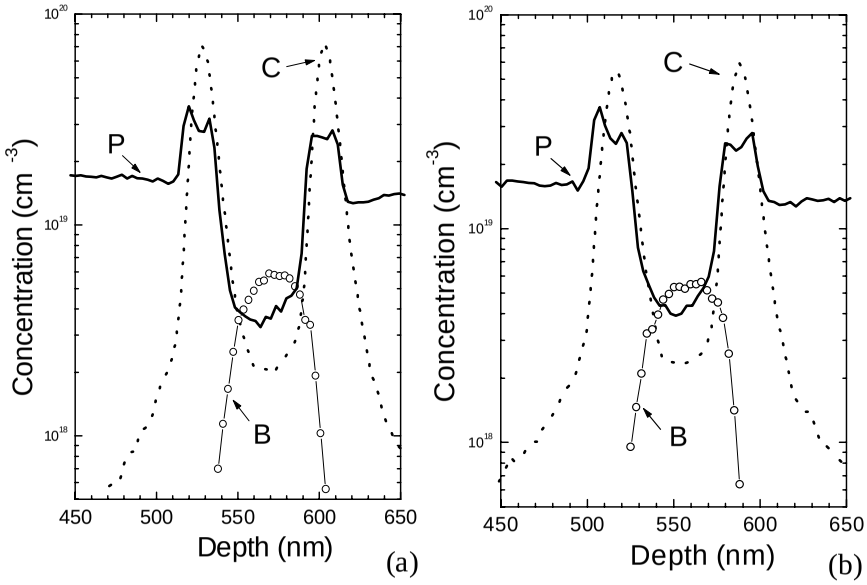


Figure 6.4: Dopant profiles of a vertical n-channel MOSFET with SiGeC layers in the source/drain, measured by SIMS (a) before and (b) after gate oxidation. The carbon signal is the mark of SiGeC layers.

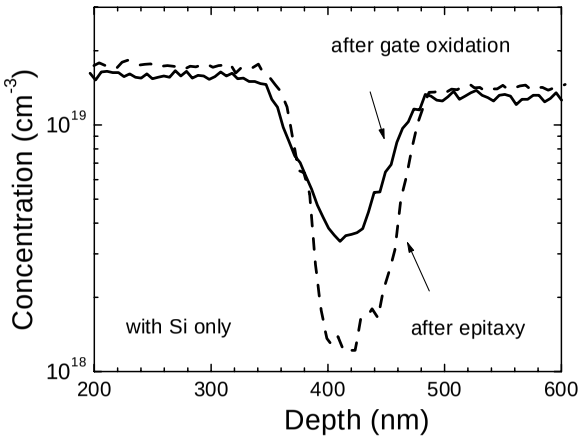


Figure 6.5: Phosphorus profiles before and after oxidation for a vertical n-channel MOSFET with Si only.

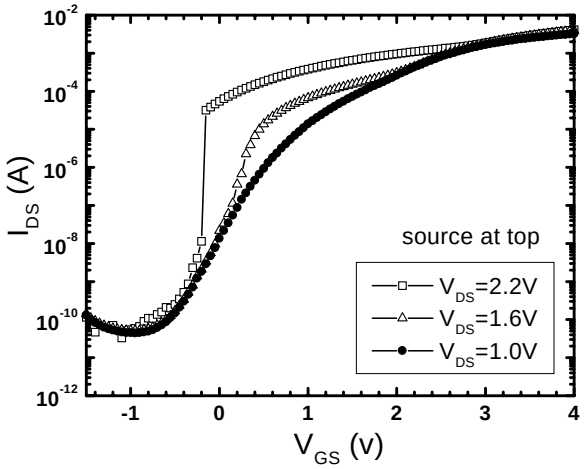


Figure 6.6: Subthreshold characteristics of the vertical n-channel MOSFET's shown in Fig. 6.2 under larger drain biases, illustrating floating body effects.

body effect. It has been reported that a large number of electron-hole pairs are generated by electron impact ionization even when the drain is well below 1V [227]. The generated holes are drifted by the electrical field and accumulate in the channel region, near the source. The built-up charge then lowers the barrier height, leading to premature turn-on of the n-channel MOSFET. Increasing drain voltage causes larger charge accumulation due to the impact ionization, thus resulting in earlier turn-on. If the voltage drop near the source is close to 0.6V due to the built-up charge, the leakage current is dramatically increased by positive feed-back, and the device subsequently breaks down. This anomalous subthreshold behavior is not so severe in the vertical p-channel MOSFET's, as the hole-impact ionization coefficient in silicon is much lower than that for electron. In this work, no floating body effect on the vertical p-channel MOSFET's has been observed.

Various methods have been proposed to solve the floating body problem in SOI MOSFET's, such as use of lightly doped drain (LDD) or lightly doped source (LDS) structures [228], body contact[229], source-tie [230], lifetime killer [231, 232, 233], field shield [234], and bandgap engineering. The body contact method provides a simple and effective solution, but the breakdown voltage rapidly decreases as the channel width increases [235]. The same problem occurs in the field shield method. LDD or LDS structures sacrifice the device

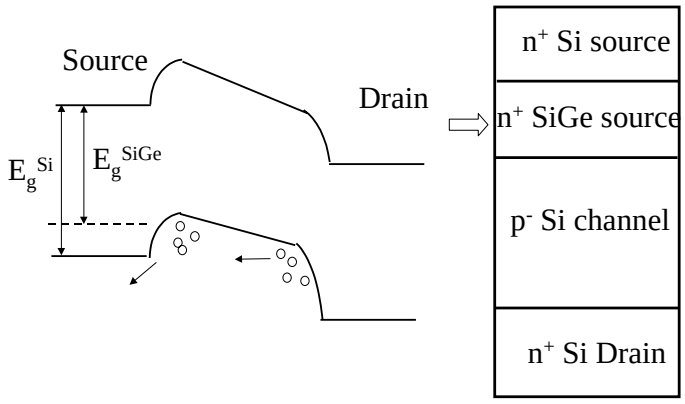


Figure 6.7: (a) Schematic band diagram to illustrate the floating body effect for vertical n-channel MOSFET's. (b) SiGe source materials are proposed in vertical MOSFET's to suppress the floating body effect.

drivability. The most promising method of all is bandgap engineering which, uses narrower bandgap material (such as SiGe) at the source, thus enhancing the hole flow into the source [219, 235, 236, 237, 238, 239]. This is illustrated in Fig. 6.7. The increased hole flow to the source reduces the current gain of parasitic bipolar transistors (opposite of the well-known heterojunction bipolar transistor device). For lateral SOI MOSFET's, Ge implantation has been used to create a SiGe source [235, 238, 237, 219]. In vertical n-channel MOSFET's, a SiGe source is very easy to achieve by using epitaxy. In our work, thin SiGeC layers have been added in the source for both p-channel and n-channel MOSFET's to suppress dopant diffusion. Determination as to whether or not these SiGeC layers suppress the floating body effect requires further study.

6.2 Thermal Stability of Vertical MOSFET's

Vertical p-channel and n-channel MOSFET's have been demonstrated in the previous chapter and the above section. In order to integrate vertical MOSFET's into advanced CMOS technology and/or enable a second layer of devices in the stacking structure for increasing packing density, the first device layer has to sustain the high temperatures used in the subsequent processing. To test the vertical MOSFET's thermal stability, nitrogen

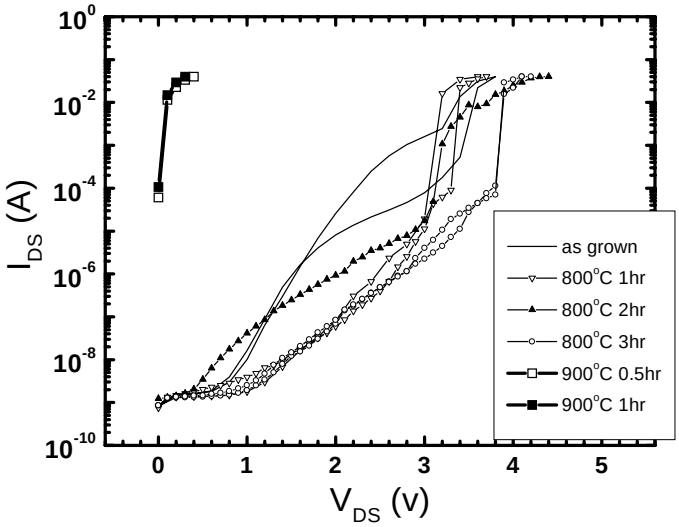


Figure 6.8: Drain current vs. drain voltage for vertical p-channel MOSFET's with L=0.12μm and SiGeC source/drain after various annealing conditions. The devices show good thermal stability for up to 800^{o}C annealing for 3hours in N_2.

annealing has been performed on the p-channel devices. For the device with a channel length of ~0.12μm, with doped SiGeC layers in the source and drain, the source and drain are shorted after 900^{o}C annealing for 0.5hr, but still have low leakage current after 800^{o}C annealing for 3 hrs. The drain current vs. drain voltage curves are shown in Fig. 6.8.

The dopant profiles, measured by SIMS, in the device after 800^{o}C 3hrs annealing are given in Fig. 6.9a. Compared with Fig. 5.11ba (as grown), the boron doping profile is not changed after the annealing. For a similar device with L=100nm and all silicon epitaxy layers, the source and drain are shorted after 800^{o}C 3hr annealing, confirmed by SIMS measurement (shown in Fig. 6.9b). Compared with Fig. 5.3a, there is significant boron diffusion from the source and drain into the channel after the annealing. Further experiments are needed to study the differences in the thermal diffusion between devices with Si only and with SiGeC in the source/drain, in the absence of oxygen.

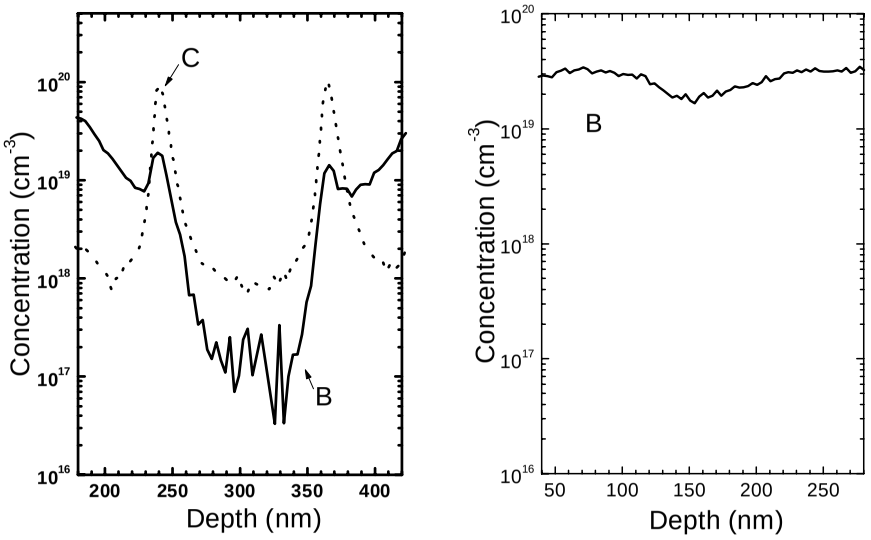


Figure 6.9: SIMS measurements of dopant concentrations of vertical p-channel MOSFET's after 800^{o}C nitrogen annealing for 3hrs. (a) L=0.12μm with SiGeC layers in the source/drain. (b) L=100nm with Si only.

6.3 Heterojunction MOSFET's

Using mature epitaxy technology, vertical structure can serve an alternative geometry for the heterojunction MOSFET's. As shown in Fig. 6.10a, hole mobility may be enhanced in the strained SiGe channel. A SiGe strained layer may also be used as the source instead of the channel, as shown in Fig. 6.10b. The narrower SiGe bandgap may help to reduce the floating body effect in n-channel MOSFET's, as discussed in the previous section. Using a SiGe source in a p-channel device, the barrier between the source and channel is material-defined and may reduce the DIBL effect for short channel lengths[80]. Using epitaxy re-growth after defining the pillar structure, strained Si n-channel MOSFET's can be fabricated (Fig. 6.10c). It is well known that electron mobility is enhanced in a tensile-strained Si layer [4]. In a conventional lateral structure, a relaxed SiGe buffer is required to obtain tensile strained Si. However, it is very difficult to grow high quality silicon layers on top of a relaxed SiGe buffer due to the mismatching dislocations. Using the vertical structure, tensile-strained Si channel may be obtained on the sidewall of fully-strained SiGe layer. Furthermore, Possion's relation gives a larger lattice displacement along the vertical

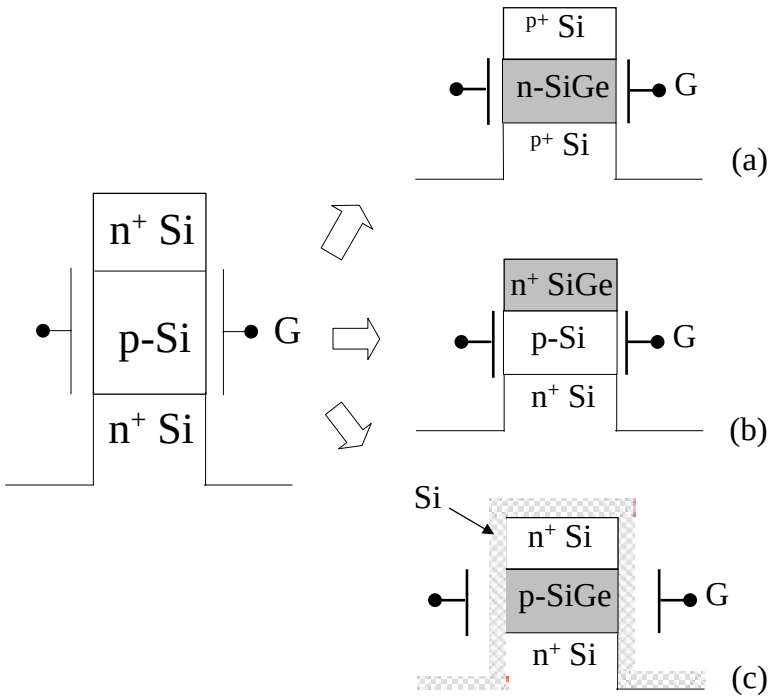


Figure 6.10: Schematic structure of vertical MOSFET's with heterojunctions: using (a) graded SiGe channel, (b) SiGe source, (c) strained-Si channel on the sidewall.

direction than the lateral displacement. Therefore, larger tensile strain may be achieved in the sidewall silicon layer for a given Ge concentration than on a lateral Si layer on top of the relaxed SiGe buffer. A similar structure has been reported by Liu *et al.* [81], but more experiments are needed to prove the advantages mentioned above. Using the facilities at Princeton, it is possible that highly improved device performance for heterojunction devices may be achieved, as high quality SiGe and Si epitaxial layers have been grown on both planar silicon substrates and vertical structure sidewalls.

6.4 Final Remarks

Vertical p-channel MOSFET's with record channel lengths and vertical n-channel MOSFET's with $\sim$0.5μm have been demonstrated in the present work. Many areas in the development of vertical MOSFET's are still waiting to be investigated thoroughly. They are,

for example, sub-100nm n-channel MOSFET's, vertical device thermal stability, heterojunction devices, and most important of all vertical double-gate MOSFET's on ultra-thin pillars (d <100nm), which is our ultimate goal. The vertical double-gate (surrounding-gate) MOSFET (Chapter 2 & 3) is a very promising structure. It may provide high packing density and high short-channel immunity, enabling the continuous development of CMOS technology. It may also lead the current 2D-layered CMOS technology to advance into the realm of full 3D integration, either through transistors on top of trench capacitors, or through two-level CMOS (one SOI device layer formed on top of an existing one) given the thermal stability of the first layer.

Chapter 7

Calculation of Band Alignments and Quantum Confinement Effects in Zero- and One-Dimensional Pseudomorphic Structures

The strain field distributions and band lineups of zero-dimensional (0-D) and one-dimensional (1-D) strained pseudomorphic semiconductor particles inside a three-dimensional (3-D) matrix of another semiconductor have been studied. The resulting strain in the particle and the matrix leads to band alignments considerably different than those in the conventional 2-D pseudomorphic growth case. The models are then applied to ideal spherical and cylindrical $Si_{1-x}Ge_x$ particles in a large Si matrix. In contrast to the 2-D case, the band alignments for both structures are predicted to be strongly type II, where the conduction band edge and the valence band edge of the Si matrix are both significantly lower than those in the $Si_{1-x}Ge_x$ inclusion respectively. Band lineups and the lowest electron-heavy-hole transition energies of a pseudomorphic V-groove $Si_{1-x}Ge_x$ quantum wire inside a large Si matrix have been calculated numerically for different size structures. The photoluminescence energies of large $Si_{1-x}Ge_x$ V-groove structures on Si will be lower than those of conventional 2-D strained $Si_{1-x}Ge_x$ for similar Ge contents.

7.1 Introduction

There has recently been an increasing interest in zero-dimensional (0-D) "quantum dots" and one-dimensional (1-D) "quantum wires" consisting of a pseudomorphically strained epitaxial semiconductor surrounded by a matrix of a second semiconductor. Such material systems include $Si_{1-x}Ge_x$ on Si [240, 241, 242, 243, 244, 245, 246, 247], $Si_{1-x-y}Ge_xC_y$ on Si [248], and $In_xGa_{1-x}As$ on GaAs [249, 250, 251, 252, 253, 254, 255]. While the effect of uniform strain in biaxially-strained pseudomorphic two-dimensional layers on planar substrates is well known [256, 257], the effect of strain on band alignments in pseudomorphic 0-D and 1-D particles has not generally been explored.

In this chapter we first calculate the spatially varying strain fields and resulting band alignments for ideal spherical and cylindrical pseudomorphic inclusions in an infinite matrix, and apply the results to $Si_{1-x}Ge_x$ in Si, assuming the materials are isotropic. The results are very different from those in a uniform biaxially-strained 2-D layer, and the type of band offset (Type I vs. Type II) can be changed. The finite element method is then used to investigate the strain distribution in and around a single V-groove $Si_{1-x}Ge_x$ quantum wire buried inside a large Si matrix. The electron and hole energy levels are obtained in order to compare with experimental photoluminescence values.

In vertical MOSFET's, pseudomorphic SiGeC epitaxial-layers have been introduced to suppress dopant diffusion (Chapter 5), and SiGe layers have been proposed (Chapter 6) for novel heterojunction devices. For the vertical double-gate MOSFET's with ultra-thin pillars, the strain in the SiGe and SiGeC layers will be significantly affected by the three-dimensional effect. A similar method to that presented in this chapter can also be used to calculate the strain and band lineups in SiGe and SiGeC layers in these thin pillars.

In the following section we will first discuss analytical strain distributions for the ideal symmetry structures, i.e. pseudomorphic 0-D spheres and 1-D cylinders made up of isotropic materials. In Sec. 7.3 we will present an approach to calculate band alignments from the strain distributions following *model-solid approach* of Van de Walle and Martin [256, 257] and Pollak and Cardona [258]. The results for pseudomorphic $Si_{1-x}Ge_x$ inside a Si

matrix using analytic models are given in Sec. 7.4. The analytic results are also compared with results where the strain is calculated numerically using the finite element approach taking anisotropies into account. Numerical results are derived in Sec. 7.5 for a V-groove $Si_{1-x}Ge_x$ quantum-wire, considering the anisotropic elastic properties of $Si_{1-x}Ge_x$ material. A perturbation approach is used to get the quantum confinement energy in the small V-grooves.

7.2 Strain Distribution of Ideal Structures

In order to determine the band alignments of a system, the strain distributions in the materials are required. For the purposes of analytical calculation it is assumed at first that the elastic properties of Si and Ge are isotropic. The results will be compared with the anisotropic case later. We also only consider an ideal pseudomorphic interface.

7.2.1 Spheres

Conceptually, a pseudomorphic 0-D dot can be formed by replacing atoms in a sphere of radius R in a matrix of a semiconductor with atoms of a second semiconductor of different lattice constant, shown in Fig. 7.1. If the lattice constant of the relaxed inclusion a_i is larger (smaller) than that of the matrix a_m, both materials are under compressive (tensile) stress. This was modeled using continuum linear elastic theory assuming no defects or plastic deformation. While the solution of a spherical inclusion inside an infinite matrix can be found in the literature [259, 260], a more straightforward way to derive the analytical expressions for a more general case is presented here. For simplicity we only consider first order solutions of the lattice mismatch between the inclusion and the matrix $\epsilon_m = a_i/a_m - 1$.

On account of the spherical symmetry, there are two tangential stress components σ_t, and one radial component σ_r. They must satisfy the equilibrium equation (Ref.[261], p395):

$$\frac{d\sigma_r}{dr} + \frac{2}{r}(\sigma_r - \sigma_\tau) = 0 \tag{7.1}$$

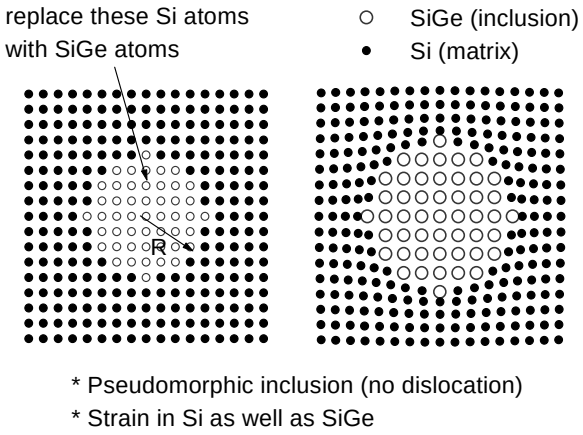


Figure 7.1: Schematic picture of strain distribution of a SiGe alloy inside a Si matrix. (a) a Si matrix , (b) replacing the center Si atoms with SiGe atoms. Since lattice constant $a_{SiGe} > a_{Si}$, both materials are under compressive strain.

In spherical coordinates, the relation between stress and strain can be written as

$$\sigma_r = \frac{E}{(1+\nu)(1-2\nu)}[(1-\nu)\varepsilon_r + 2\nu\varepsilon_\tau], \tag{7.2}$$

$$\sigma_\tau = \frac{E}{(1+\nu)(1-2\nu)}(\varepsilon_\tau + \nu\varepsilon_r), \tag{7.3}$$

and the relation between strain and radial displacement u can be expressed by

$$\varepsilon_r = \frac{du}{dr} \tag{7.4}$$

$$\varepsilon_\tau = \frac{u}{r} \tag{7.5}$$

where E is the modulus of elasticity (Young's modulus) and ν Poisson's ratio. Substituting Eqns. (7.2-7.5) into Eqn. (7.1), we find the differential equation for u to be

$$\frac{d}{dr}(\frac{1}{r^2}\frac{d}{dr}(ru^2)) = 0$$

Its solution is

$$u = C_1 r + \frac{C_2}{r^2} \tag{7.6}$$

where C_1 and C_2 are constants to be determined from boundary conditions.

A. Infinite Matrix

First let us consider an infinitely large matrix. These results will be compared with a finite matrix in the next section. To satisfy the following requirements

$$u_i \to 0 \quad when \quad r \to 0$$
$$u_m \to 0 \quad when \quad r \to \infty$$

for an infinite matrix, the displacement of the atoms inside and outside the sphere can only have the form of

$$\begin{aligned} u_i &= C_i r \\ u_m &= \frac{C_m}{r^2}. \end{aligned}$$

From Eqns. (7.4, 7.5), the strain inside the sphere (ε_{in}) and outside in the matrix (ε_r and ε_τ) are

$$\varepsilon_{in} = C_i \qquad (r < R) \tag{7.7}$$

$$\left.\begin{aligned} \varepsilon_r &= -\tfrac{2C_m}{r^3} \\ \varepsilon_\tau &= \tfrac{C_m}{r^3} \end{aligned}\right\} \quad (r > R). \tag{7.8}$$

Note that in the inclusion only a uniform hydrostatic strain exits, and that in the matrix only "normal" (no shear or hydrostatic) strains exist.

Using the following boundary conditions (7.9 and 7.10), the coefficients C_i and C_m can be determined,

$$u_i|_R - u_m|_R = -\epsilon_m R \tag{7.9}$$

$$\sigma_r^m = \sigma_r^i \tag{7.10}$$

$$\Rightarrow \left\{ \begin{aligned} C_m &= \tfrac{\epsilon_m R^3}{\gamma} \\ C_i &= \epsilon_m(\tfrac{1}{\gamma} - 1) \end{aligned} \right.$$

where the constant γ is defined as

$$\gamma = 1 + \frac{4\mu_m}{3\kappa_i} = 1 + \frac{2\kappa_m(1-2\nu_m)}{\kappa_i(1+\nu_m)} \tag{7.11}$$

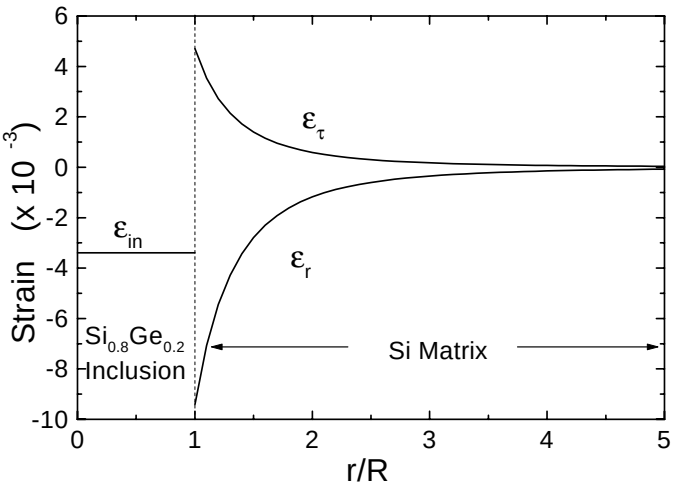


Figure 7.2: Strain distribution vs. r/R (ratio of the radial location vs. the radius of the sphere) for the structure of a $Si_{0.8}Ge_{0.2}$ sphere inside a Si matrix. ϵ_τ and ϵ_r are the tangential and radial strain components. The strain inside the SiGe is uniform and hydrostatic.

and where κ and μ are the bulk modulus and the modulus of rigidity, respectively. Their relationship with E and ν are

$$\mu = \frac{E}{2(1+\nu)}, \qquad E = 3\kappa(1-2\nu).$$

Thus the strain inside the sphere are:

$$\varepsilon_{in} = \epsilon_m(\frac{1}{\gamma} - 1) \tag{7.12}$$

and the strain components in the matrix is:

$$\varepsilon_r = -2\frac{\epsilon_m}{\gamma}(\frac{R}{r})^3 \tag{7.13}$$

$$\varepsilon_\tau = \frac{\epsilon_m}{\gamma}(\frac{R}{r})^3. \tag{7.14}$$

The strain in the sphere is uniform and hydrostatic, which means the shape (spherical) of the inclusion will not change under the stress. The strain in the matrix has no hydrostatic component; its magnitude is independent of the absolute size of the sphere, but only related to r/R, the ratio of the distance from the center to the radius of the sphere. Note that the result pertains only to isolated spheres, not an interacting array of spheres.

The strain components ε_r and ε_τ are plotted in Fig. 7.2 for a $Si_{0.8}Ge_{0.2}$ sphere inside an infinite Si matrix. The uniformly distributed hydrostatic strain inside the sphere is -3.4×10^{-3}, and in the matrix around the sphere, the radial and tangential strain components would be -9.4×10^{-3} and 4.7×10^{-3} respectively.

B. Finite Matrix

In the case of a finite spherical matrix, the strain field may also be solved analytically, given an assumption of isotropic elastic properties of the materials.

For a matrix with radius R_m (Fig. 7.3), the displacement of atoms in the matrix under a given internal pressure p_0 is [261]

$$u_m = \frac{p_0 \frac{R^3}{R_m^3}}{3\kappa_m(1-\frac{R^3}{R_m^3})} r + \frac{p_0 R^3}{4\mu_m(1-\frac{R^3}{R_m^3})} \frac{1}{r^2}, \tag{7.15}$$

and the displacement of atoms in the sphere is

$$u_i = \frac{-p_0}{3\kappa_i} r. \tag{7.16}$$

Thus from Eqns. (7.4, 7.5), the strain component inside the sphere can be written as

$$\varepsilon_{in} = \frac{-p_0}{3\kappa_i}, \tag{7.17}$$

and in the matrix as

$$\varepsilon_r = \frac{p_0 \frac{R^3}{R_m^3}}{3\kappa_m(1-\frac{R^3}{R_m^3})} - \frac{2p_0 R^3}{4\mu_m(1-\frac{R^3}{R_m^3})} \frac{1}{r^3} \tag{7.18}$$

$$\varepsilon_\tau = \frac{p_0 \frac{R^3}{R_m^3}}{3\kappa_m(1-\frac{R^3}{R_m^3})} + \frac{p_0 R^3}{4\mu_m(1-\frac{R^3}{R_m^3})} \frac{1}{r^3}. \tag{7.19}$$

The parameter p_0 can be determined by the boundary condition

$$u_i|_R - u_m|_R = -\epsilon_m R. \tag{7.20}$$

Inserting Eqns. (7.15) and (7.16) into Eqn. (7.20), we can get an expression of p_0 as:

$$\frac{\epsilon_m}{p_0} = \frac{1}{3\gamma_1} + \frac{1}{(1-\frac{R^3}{R_m^3})\gamma_2} \tag{7.21}$$

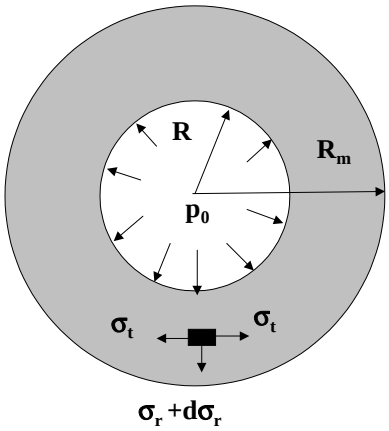


Figure 7.3: Schematic of a sphere inside a matrix with finite size.

where

$$\frac{1}{\gamma_1} = \frac{1}{\kappa_i} - \frac{1}{\kappa_m}, \qquad \frac{1}{\gamma_2} = \frac{1}{3\kappa_m} + \frac{1}{4\mu_m}.$$

From Eqns. (7.17 - 7.19) and (7.21), the strain distribution of a sphere inside an finite matrix can be found.

Fig. 7.4 gives the value of the hydrostatic strain inside the $Si_{0.8}Ge_{0.2}$ inclusion as a function of the ratio between the radius of the Si matrix and the SiGe inclusion R_{Si} / R_{SiGe}. The strain inside the SiGe decreases as the size of the matrix decreases. But at R_{Si} / R_{SiGe}=3, the strain inside the sphere is already 97% of the value of the infinite model. Therefore the magnitude of the strain distribution can be estimated using an infinite matrix, as long as the radius of the matrix (R_{Si}) is several times larger than the radius of the SiGe sphere (R_{SiGe}).

7.2.2 Cylinders

To model a 1-D structure, an infinitely long (in the z direction) cylindrical shaped inclusion with radius R is inserted in an infinite matrix of smaller (larger) lattice constant (a_m) (Fig. 7.5). For a pseudomorphic structure, the axial strain in the matrix is

$$\varepsilon_{zz} = 0, \tag{7.22}$$

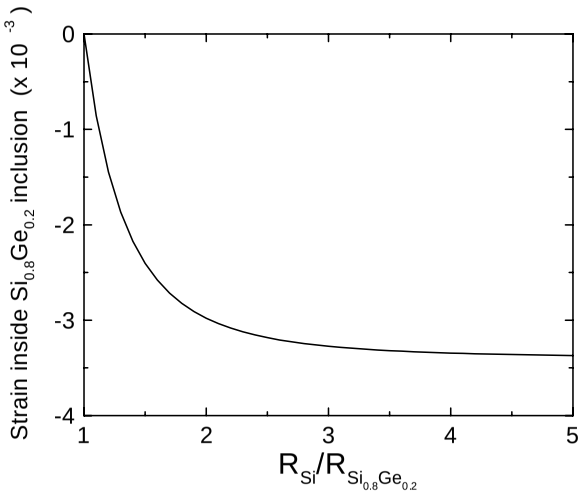


Figure 7.4: Strain inside a $Si_{0.8}Ge_{0.2}$ sphere as a function of $R_{Si}/R_{Si_{0.8}Ge_{0.2}}$ (the ratio of the radius of the Si matrix over that of the SiGe sphere). The infinite matrix approximation is good for R_{Si} several times larger than R_{SiGe}.

and in the cylinder is

$$\varepsilon_{zz} \approx -\epsilon_m. \tag{7.23}$$

Due to the cylindrical symmetry, the stress σ_r and σ_θ satisfy equation (Ref. [261] p442):

$$\frac{d\sigma_r}{dr} + \frac{\sigma_r - \sigma_\theta}{r} = 0 \tag{7.24}$$

If u denotes the radial displacement, we have

$$\varepsilon_r = \frac{du}{dr}, \qquad \varepsilon_\theta = \frac{u}{r}. \tag{7.25}$$

For cylindrical symmetry, the relationships between strain and stress are:

$$\varepsilon_r = \frac{1}{E}[\sigma_r - \nu(\sigma_\theta + \sigma_z)] \tag{7.26}$$

$$\varepsilon_\theta = \frac{1}{E}[\sigma_\theta - \nu(\sigma_r + \sigma_z)] \tag{7.27}$$

$$\varepsilon_z = \frac{1}{E}[\sigma_z - \nu(\sigma_r + \sigma_\theta)]. \tag{7.28}$$

Inserting Eqns. (7.25- 7.28) into Eqns. (7.24), we get

$$\frac{d}{dr}[\frac{1}{r}\frac{d(ru)}{dr}] = 0.$$

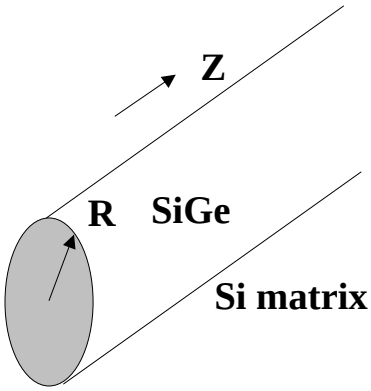


Figure 7.5: Schematic of a SiGe wire inside a Si matrix

The solution of the above equation is

$$u = C_1 r + \frac{C_2}{r},$$

where C_1 and C_2 are constants to be determined by the boundary conditions. In an infinite matrix, the radial displacement can only take the form of

$$u_m = \frac{C_2}{r},$$

and for the inclusion

$$u_i = C_1 r.$$

Evaluating the above equations at the boundary conditions:

$$\begin{aligned} \sigma_r^i|_R &= \sigma_r^m|_R \\ u_m|_R - u_i|_R &= \epsilon_m R. \end{aligned}$$

We thus obtain the strain distribution of an infinite long cylinder inside an infinite matrix as

$$r > R, \begin{cases} \varepsilon_r &= -\frac{\epsilon_m}{\gamma'}(\frac{R}{r})^2 \\ \varepsilon_\tau &= \frac{\epsilon_m}{\gamma'}(\frac{R}{r})^2 \\ \varepsilon_{zz} &= 0 \end{cases}$$

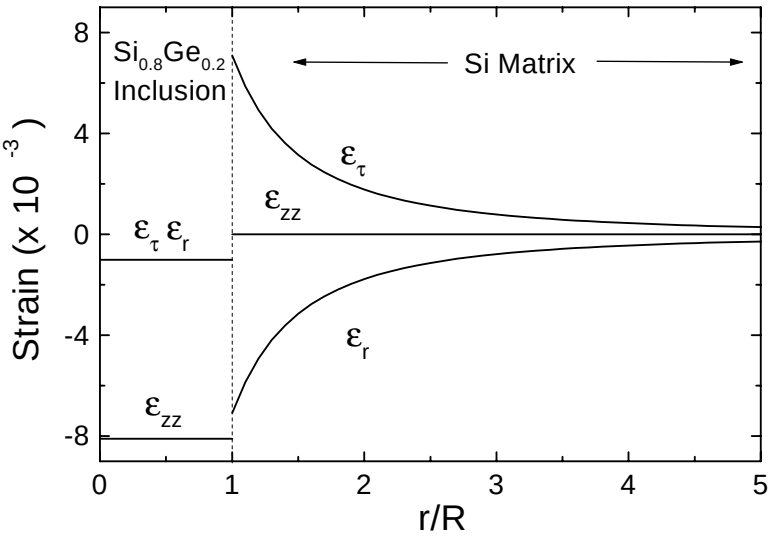


Figure 7.6: Strain distribution vs. r/R (ratio of the radial location vs. the radius of the cylinder) for a $Si_{0.8}Ge_{0.2}$ cylinder inside a Si matrix. ϵ_τ and ϵ_r are the tangential and radial strain components in the polar plane. ϵ_{zz} is the axial strain.

$$r < R, \begin{cases} \varepsilon_{in} &= \varepsilon_r = \varepsilon_\tau = \epsilon_m(\frac{1}{\gamma'} - 1) \\ \varepsilon_{zz} &= -\epsilon_m \end{cases}$$

where

$$\gamma' = \frac{1}{1+\nu_i} + \frac{\kappa_m}{\kappa_i}\frac{1-2\nu_m}{1+\nu_m}.$$

For a $Si_{0.8}Ge_{0.2}$ cylinder inside a Si matrix, the strain components are plotted in Fig. 7.6. The strains ε_r and ε_τ inside the cylinder would be -1.01×10^{-3} with a lattice mismatch of -8.1×10^{-3} in z direction. In the matrix, ε_r and ε_τ would be -7.1×10^{-3} and 7.1×10^{-3}, respectively, at the boundary.

7.3 Calculation of Band Alignments for Strain Distribution

7.3.1 Valence Band

To determine the effect of strain on band alignments, we first define the *xyz* axis for our analysis in the usual [100], [010], and [001] crystal directions. In a general case, a stress

tensor can be written as:

$$\boldsymbol{\varepsilon} = \begin{bmatrix} \varepsilon_{xx} & \varepsilon_{xy} & \varepsilon_{xz} \\ \varepsilon_{xy} & \varepsilon_{yy} & \varepsilon_{yz} \\ \varepsilon_{xz} & \varepsilon_{yz} & \varepsilon_{zz} \end{bmatrix}.$$

The procedure for obtaining the lineups follows the *model-solid approach* of Van de Walle and Martin [256, 257]. In this theory the average energy of the highest valence bands at the Γ point ($E^0_{v,av}$) is set on an absolute scale for bulk relaxed material. The effects of spin-orbit coupling ($H_{s,o}$, assumed independent of strain) and the effects of strain (H_ε) are then added to this starting point to get the position of an individual valence band maximum

$$E_v = E^0_{v,av} + < J, m_J | H_{s,o} + H_\varepsilon | J, m_J > . \tag{7.29}$$

Without spin-orbit splitting, the valence band maxima of unstrained Si, Ge, and $Si_{1-x}Ge_x$ alloy at $\mathbf{k}$=0 is a six-fold degenerate multiplet with orbital symmetry $\mathbf{\Gamma}_{25'}$. The spin-orbit interaction lifts this degeneracy into a four-fold $p_{3/2}$ multiplet ($J = \frac{3}{2}, m_J = \pm\frac{3}{2}, \pm\frac{1}{2}$ in spherical notation) and a two-fold $p_{1/2}$ multiplet ($J = \frac{1}{2}, m_J = \pm\frac{1}{2}$). In the $|J, m_J >$ representation, the spin-orbit interaction Hamiltonian has a diagonal form, and reads:

$$H_{s,o} = \begin{bmatrix} |\frac{3}{2},\frac{3}{2}> & |\frac{3}{2},\frac{1}{2}> & |\frac{3}{2},-\frac{1}{2}> & |\frac{3}{2},-\frac{3}{2}> & |\frac{1}{2},\frac{1}{2}> & |\frac{1}{2},-\frac{1}{2}> \\ \frac{\Delta_0}{3} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{\Delta_0}{3} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{\Delta_0}{3} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{\Delta_0}{3} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{2\Delta_0}{3} & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{2\Delta_0}{3} \end{bmatrix}$$

where Δ_0 is the spin-orbit splitting of the valence bands at the Γ point (0.3eV for Ge and 0.04eV for Si).

It has been shown that the orbital-strain Hamiltonian H_ε for a given band at $\mathbf{k}$=0 can be written as [262, 263, 264, 265, 266, 267, 268]

$$H_\varepsilon = a_v(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) - 3b[(L_x^2 - \frac{1}{3}\mathbf{L}^2)\varepsilon_{xx} + c.p.] - \frac{6}{\sqrt{3}}d[\{L_x L_y\}\varepsilon_{xy} + c.p.] \tag{7.30}$$

where **L** is the angular-momentum operator, c.p. denotes cyclic permutations with respect to the indices, x, y, and z, and the quantities in the curly brackets indicate the symmetrized product: $\{L_xL_y\} = \frac{1}{2}(L_xL_y + L_yL_x)$. The parameter a_v is the hydrostatic pressure-deformation potential for valence band. The quantities b and d are uniaxial deformation potentials. The orbital-strain Hamiltonian can be re-written as

$$\begin{aligned} H_\varepsilon &= a_v(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}) - 3b[\frac{L_+^2+L_-^2}{4}(\varepsilon_{xx}-\varepsilon_{yy}) + \frac{L^2-3L_z^2}{6}(\varepsilon_{xx}+\varepsilon_{yy}-2\varepsilon_{zz})] \\ &\quad -\sqrt{3}d[\frac{1}{2i}(L_+^2-L_-^2)\varepsilon_{xy} + \frac{1}{2}(L_+L_z+L_zL_+)(\varepsilon_{xz}-i\varepsilon_{yz}) \\ &\quad +\frac{1}{2}(L_-L_z+L_zL_-)(\varepsilon_{xz}+i\varepsilon_{yz})]. \end{aligned}$$

The wave function for the valence band states will be taken in the $|J, m_J>$ representations in which $H_{s,o}$ is diagonal:

$$\begin{cases} |\frac{3}{2},\frac{3}{2}> &= Y_{11}\uparrow \\ |\frac{3}{2},\frac{1}{2}> &= \sqrt{\frac{1}{3}}Y_{11}\downarrow + \sqrt{\frac{2}{3}}Y_{10}\uparrow \\ |\frac{3}{2},-\frac{1}{2}> &= \sqrt{\frac{2}{3}}Y_{10}\downarrow + \sqrt{\frac{1}{3}}Y_{1-1}\uparrow \\ |\frac{3}{2},-\frac{3}{2}> &= Y_{1-1}\downarrow \\ |\frac{1}{2},\frac{1}{2}> &= \sqrt{\frac{2}{3}}Y_{11}\downarrow - \sqrt{\frac{1}{3}}Y_{10}\uparrow \\ |\frac{1}{2},-\frac{1}{2}> &= \sqrt{\frac{1}{3}}Y_{10}\downarrow - \sqrt{\frac{2}{3}}Y_{1-1}\uparrow \end{cases}$$

where $\uparrow$ and $\downarrow$ indicate spin up and down. If we denote

$$\begin{aligned} Y_1 &= a_v(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}) - b(\varepsilon_{xx}+\varepsilon_{yy}-2\varepsilon_{zz}) \\ Y_2 &= a_v(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}) + \frac{b}{2}(\varepsilon_{xx}+\varepsilon_{yy}-2\varepsilon_{zz}) \\ Y_3 &= \sqrt{\frac{3}{2}}d\varepsilon_{xz} \\ Y_4 &= -\sqrt{\frac{3}{2}}d\varepsilon_{yz} \\ Y_5 &= \frac{3}{2}b(\varepsilon_{yy}-\varepsilon_{xx}) \\ Y_6 &= \sqrt{3}d\varepsilon_{xy} \end{aligned}$$

then

$$< Y_{11}|H_\varepsilon|Y_{11} > = Y_2$$

$$
\begin{aligned}
< Y_{11}|H_\varepsilon|Y_{10} > &= -(Y_3 + iY_4) \\
< Y_{10}|H_\varepsilon|Y_{10} > &= Y_1 \\
< Y_{10}|H_\varepsilon|Y_{1-1} > &= Y_3 + iY_4 \\
< Y_{11}|H_\varepsilon|Y_{1-1} > &= Y_5 + iY_6 \\
< Y_{1-1}|H_\varepsilon|Y_{1-1} > &= Y_2.
\end{aligned}
$$

Using the above wave functions, the Hamiltonian matrix of Eqn. (7.29) can be evaluated to yield:

$$
\begin{bmatrix}
\frac{\Delta}{3} + Y_2 & -\sqrt{\frac{2}{3}}(Y_3 + iY_4) & \sqrt{\frac{1}{3}}(Y_5 + iY6) & 0 & \sqrt{\frac{1}{3}}(Y_3 + iY4) & -\sqrt{\frac{2}{3}}(Y_5 + iY_6) \\
-\sqrt{\frac{2}{3}}(Y_3 - iY_4) & \frac{\Delta}{3} + \frac{1}{3}Y_2 + \frac{2}{3}Y_1 & 0 & \sqrt{\frac{1}{3}}(Y_5 + iY6) & \frac{\sqrt{2}}{3}(Y_2 - Y1) & -Y_3 - iY_4 \\
\sqrt{\frac{1}{3}}(Y_5 - iY_6) & 0 & \frac{\Delta}{3} + \frac{2}{3}Y_1 + \frac{1}{3}Y_2 & \sqrt{\frac{2}{3}}(Y_3 + iY_4) & -Y_3 + iY_4 & \frac{\sqrt{2}}{3}(Y_1 - Y2) \\
0 & \sqrt{\frac{1}{3}}(Y_5 - iY_6) & \sqrt{\frac{2}{3}}(Y_3 - iY_4) & \frac{\Delta}{3} + Y_2 & \sqrt{\frac{2}{3}}(Y_5 - iY_6) & \sqrt{\frac{1}{3}}(Y_3 - iY_4) \\
\sqrt{\frac{1}{3}}(Y_3 - iY_4) & \frac{\sqrt{2}}{3}(Y_2 - Y1) & -Y_3 - iY_4 & \sqrt{\frac{2}{3}}(Y_5 + iY_6) & -\frac{2\Delta}{3} + \frac{2}{3}Y_2 + \frac{1}{3}Y_1 & 0 \\
-\sqrt{\frac{2}{3}}(Y_5 + iY_6) & -Y_3 + iY_4 & \frac{\sqrt{2}}{3}(Y_1 - Y2) & \sqrt{\frac{1}{3}}(Y_3 + iY_4) & 0 & -\frac{2\Delta}{3} + \frac{1}{3}Y_1 + \frac{2}{3}Y_2
\end{bmatrix}. \tag{7.31}
$$

The eigenvalues of the Hamiltonian matrix will give the energy band shift under stress. In a general case, m_J is not a good number. The valence bands will split into three two-fold levels, which are the mixing of the J=3/2 and J=1/2 states. Note that strain might shift the average valence band position ($E^0_{v,av}$ is for unstrained material).

7.3.2 Conduction Band

For the conduction band, the absolute energy of the minimum of the conduction band valley j of type Δ, L, or Γ (represented by α), $E^j_{c,\alpha}$, is determined by adding the shift of the minimum due to strain $\Delta E^j_{c,\alpha}$, to the position of the conduction band minimum in the bulk material $E^0_{\alpha,av}$, where

$$E^0_{\alpha,av} = E^0_{g,\alpha} + \frac{\Delta_0}{3} + E^0_{v,av} \tag{7.32}$$

and

$$E^j_{c,\alpha} = \Delta E^j_{c,\alpha} + E^0_{\alpha,av}. \tag{7.33}$$

$E^0_{g,\alpha}$ is the distance from the valence band maximum to the minimum of the conduction band of type α in relaxed bulk material. Following the notation of Herring and Vogt, $\Delta E^j_{c,\alpha}$

can be written as [269, 270]

$$\Delta E^{j}_{c,\alpha} = [\Xi^{\alpha}_{d}\mathbf{1} + \Xi^{\alpha}_{u}\{\hat{\mathbf{a}}_j\hat{\mathbf{a}}_j\}] : \boldsymbol{\varepsilon} \tag{7.34}$$

where $\mathbf{1}$ is the unit tensor, $\hat{\mathbf{a}}_j$ is the unit vector to the valley j, $\{\}$ denotes a dyadic product, $\boldsymbol{\varepsilon}$ is the strain tensor, and Ξ^{α}_{d} and Ξ^{α}_{u} are the deformation potentials for the conduction band α. The quantity $(\Xi^{\alpha}_{d} + \frac{1}{3}\Xi^{\alpha}_{u})$ sometimes is also denoted as a^{α}_{c}, the hydrostatic deformation potential for the conduction band α. The degeneracies of the conduction band minima not at Γ (e.g. Δ and L) are usually split by non-hydrostatic strain; conduction band minima at Γ are only subject to hydrostatic strain shifts (the second term on the right in Eqn. (7.34) vanishes).

We shall first consider the conduction band minima at Δ, near the X-points. The unit vector $\hat{\mathbf{a}}_{\Delta} = \{001\}$, and

$$\Delta E^{100,\bar{1}00}_{c,\Delta} = \Xi_d(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + \Xi_u\varepsilon_{xx} \tag{7.35}$$

$$\Delta E^{010,0\bar{1}0}_{c,\Delta} = \Xi_d(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + \Xi_u\varepsilon_{yy} \tag{7.36}$$

$$\Delta E^{001,00\bar{1}}_{c,\Delta} = \Xi_d(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + \Xi_u\varepsilon_{zz}. \tag{7.37}$$

For the conduction bands at L, the unit vector $\hat{\mathbf{a}}_L = \frac{1}{3}\{111\}$, and

$$\Delta E^{111,\overline{\bar{1}\bar{1}\bar{1}}}_{c,L} = (\Xi_d + \frac{1}{3}\Xi_u)(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + \frac{2}{3}\Xi_u(\varepsilon_{xy} + \varepsilon_{yz} + \varepsilon_{xz}) \tag{7.38}$$

$$\Delta E^{\bar{1}11,1\bar{1}\bar{1}}_{c,L} = (\Xi_d + \frac{1}{3}\Xi_u)(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + \frac{2}{3}\Xi_u(-\varepsilon_{xy} + \varepsilon_{yz} - \varepsilon_{xz}) \tag{7.39}$$

$$\Delta E^{1\bar{1}1,\bar{1}1\bar{1}}_{c,L} = (\Xi_d + \frac{1}{3}\Xi_u)(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + \frac{2}{3}\Xi_u(-\varepsilon_{xy} - \varepsilon_{yz} + \varepsilon_{xz}) \tag{7.40}$$

$$\Delta E^{11\bar{1},\bar{1}\bar{1}1}_{c,L} = (\Xi_d + \frac{1}{3}\Xi_u)(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + \frac{2}{3}\Xi_u(\varepsilon_{xy} - \varepsilon_{yz} - \varepsilon_{xz}). \tag{7.41}$$

Note that if the stress is an uniaxial stress along the [001] direction, i.e. $\varepsilon_{xy} = \varepsilon_{xz} = \varepsilon_{yz} = 0$, the L band will only shift its weighted average by the hydrostatic strain component and remain 4-fold degenerate. Similarly, if the uniaxial stress is along [111] directions ($\varepsilon_{xx} = \varepsilon_{yy} = \varepsilon_{zz}$), the Δ band minima will remain 3-fold degenerate. Only their weighted average changes in proportion to the hydrostatic strain component.

	a	c11	c12	c44	$E^0_{g,\Gamma}$	$E^0_{g,\Delta}$	$E^0_{g,L}$	Δ_0	$E^0_{v,av}$	c_Γ
	a_v	b	d	Ξ^Δ_u	Ξ^L_u	Ξ^Δ_d	Ξ^L_d	Ξ^Γ_d	c_L	c_Δ
Si	5.43	1.675	0.650	0.801	3.37	1.17	2.06	0.04	-7.03	–
	2.46	-2.35	-5.32	9.16	16.14	1.127	-6.04	1.98	0.0[a]	0.206[a]
Ge	5.65	1.315	0.494	0.684	0.89	0.96	0.74	0.3	-6.35	–
	1.24	-2.55	-5.50	9.42	15.13	-0.59	-6.58	−8.24	0.0[a]	0.206[a]

[a] from Ref. [271]

Table 7.1: Lattice Constant a (in Å), elastic constants c_{11}, c_{12}, and c_{44} (in 10^{12} dyn/cm^2), spin-orbit splitting Δ_0, average valence band $E^0_{v,av}$, band gaps $E^0_{g,\Delta}$, $E^0_{g,L}$ and $E^0_{g,\Gamma}$, and deformation potentials a_v, b, d, Ξ^Δ_u, Ξ^L_u, Ξ^Δ_d, Ξ^L_d and Ξ^Γ_d (all in eV) used in this work (Ref. [256, 257] except where noted).

7.4 Ideal Symmetric Structures of $Si_{1-x}Ge_x$/Si

We now apply these formulae to the case of a single $Si_{1-x}Ge_x$ sphere and cylinder inside of a Si matrix. The parameters used are listed in Table 7.1. All were linearly interpolated for the alloys except $E^0_{v,av}$ and $E^0_{g,\alpha}$ in this work. In an alloy $A_{1-x}B_x$ with lattice constants a_A and a_B mismatched, $E^0_{v,av}$ should be given by [256]:

$$E^0_{v,av}(x) = xE^0_{v,av,B} + (1-x)E^0_{v,av,A} + 3x(1-x)[-a^B_v + a^A_v]\frac{a_B - a_A}{a_{AB}} \tag{7.42}$$

where the alloy lattice constant $a_{AB} = a_A(1-x) + a_B x$. The bandgaps of the bulk relaxed alloys were fit with a quadratic as

$$E^0_{g,\alpha}(x) = (1-x)E^0_{g,\alpha,A} + xE^0_{g,\alpha,B} - c_\alpha x(1-x) \tag{7.43}$$

where α refers to the type of conduction band minimum and c_α is a "bowing" parameter.

7.4.1 $Si_{1-x}Ge_x$ Quantum-wires and Quantum-dots

For the case of a $Si_{0.8}Ge_{0.2}$ sphere in a Si matrix, Fig. 7.7(a) gives the band extreme positions as a function of r/R in the [100] real-space direction, which has the lowest conduction band. (Note the [100], [010], and [001] directions are equivalent in this spherical inclusion

case.) The energies are relative to the top of the valence band edge in relaxed Si material. Only Δ conduction bands are plotted as L bands lie higher in energy for all Ge concentrations (unlike the relaxed alloy), assuming an L bandgap in bulk Si of 2.06 eV. Inside the sphere, the band edges of the SiGe are uniform due to the uniform strain distribution. As the stress in the sphere is hydrostatic, the conduction band and the valence band edges remain degenerate except for the spin-orbit splitting of the valence band, although both bands are dropped from their relaxed positions. In the Si matrix, the 4-fold degenerate conduction band Δ_4 is lifted up by 0.045 eV and the 2-fold degenerate conduction band Δ_2 (valleys in the [100] and [$\bar{1}$00] k-space directions for the [100] real-space direction) drops by 0.09 eV to form the conduction band minimum. As there is no hydrostatic strain in the matrix, the weighted average of these bands does not change. At the boundary, the conduction band edge in the matrix is 0.15 eV lower than that inside the sphere and the valence band edge in the sphere lies 0.10 eV higher than that outside the sphere. Although it is well known that for biaxially strained planar $Si_{1-x}Ge_x$ on Si (100) substrates the conduction band offset is negligibly small with a large valence band offset [256, 272], in this case of a commensurately strained sphere, the predicted band lineup is clearly type II, with significant offset in both bands. For example, for Ge concentration x=0.2 in the 2-D case (SiGe planar layer on top of Si(001) substrate), the conduction band offset calculated by the same approach is 0.01 eV, less than that caused by uncertainty in the parameters (0.02 eV).

As the direction of stress affects the band alignment for the conduction bands not at Γ, the energy bands of the matrix vary with direction and are plotted in Fig. 7.7(b) at the spherical boundary r=R, from [001] to [111], from [111] to [110], and from [110] to [010] real-space directions. Along the [111] direction the conduction bands remain degenerate in their bulk positions, and are 0.09 eV higher than the minima along the [100]-like directions, but are still lower than those inside the sphere (which are independent of real-space direction because of the hydrostatic strain inside the sphere). The valence bands change comparatively less with orientation compared with the conduction bands. The valence band maximum in the matrix is highest in the [111] real-space direction (0.02 eV more than in

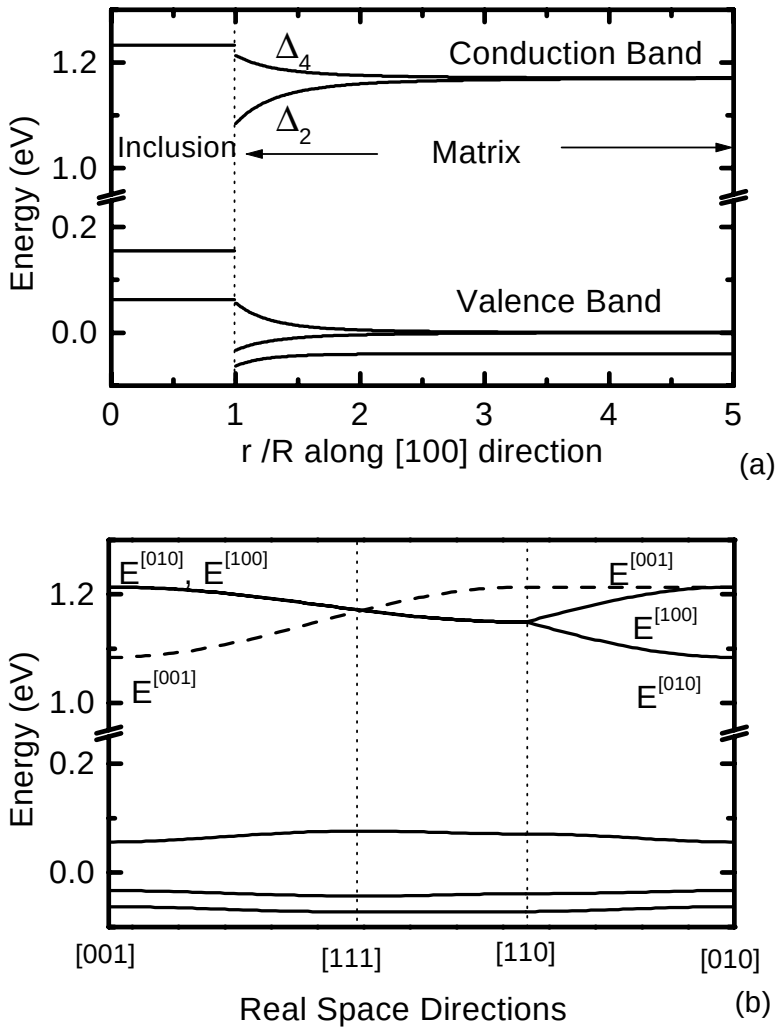


Figure 7.7: (a) Band positions vs. r/R in the [100] direction for a 0-D system: a $Si_{0.8}Ge_{0.2}$ sphere inside a Si matrix. All energies are referred to the top of the valence band in Si bulk material. Only the Δ conduction band is plotted here. (b) Energy bands vs. real space direction in the matrix at r=R.

the [100] direction), so that the conduction band and valence band extreme in the matrix lie in different positions in real space. The band gap of the matrix has a minimum at the interface in the [100] direction with a value of 1.03 eV, which is less than that inside the sphere (1.08 eV). The band gap reaches a maximum in the [111] direction in the matrix and is 0.07 eV larger than that along [100] direction.

Qualitatively similar results are obtained for a long $Si_{0.8}Ge_{0.2}$ cylinder (with its axis along [001] direction) inside a Si matrix. Fig. 7.8(a) is the band alignment along the [100] real-space direction. Inside the cylinder the energy bands are spatially uniform, but split due to the non-hydrostatic strain. The two conduction band minima in the [100] k-space directions are 0.06 eV lower in energy than the four in the [010] and [001] k-space directions. The band alignment is type II, with 0.08 eV conduction band offset, and 0.14 eV valence band offset. The energies of the bands in the matrix vary along different directions in the polar plane in real space, which is given in Fig. 7.8(b). The six conduction band minima split into three non-degenerate pairs; bands are only degenerate in the [110] direction. The [100] and [010] directions in real space have the lowest conduction bands ([100] and [010] directions in k-space respectively), which are 0.06 eV lower than that of [110] direction at the interface r=R. The conduction band edges in the matrix in all real space directions are lower than that inside the cylinder. Changes for the valence bands in different directions in the matrix are small. The valence band offset between [100] and [110] direction in the matrix is 0.02 eV.

A similar analysis was performed for a $Si_{0.8}Ge_{0.2}$ cylinder with its axis along the [011] direction (Fig. 7.9(a)). (The [011] and $[0\bar{1}1]$ are the directions of straight lines usually defined by lithography on (100)-oriented wafers.) Again the bands are spatially uniform inside the cylinder, but four conduction band minima in k-space in the plane of the cylinder lie lower than the other two minima (along [100] direction) rather than higher. In the matrix, the relative alignment of the six conduction band minima are also different as shown in Fig. 7.9(b). The overall alignment between the inclusion (cylinder) and matrix is again type II, with a 0.11 eV conduction band offset and 0.14 eV valence band offset along $[1\bar{1}1]$. The largest energy offset between the cylinder and matrix for different directions are

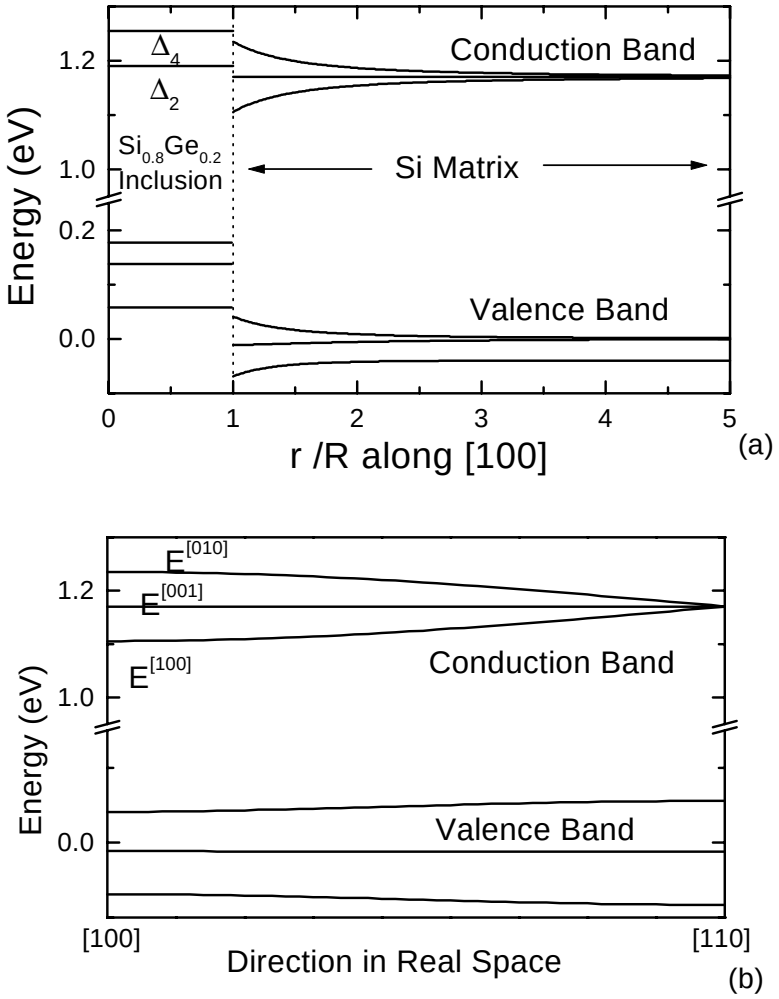


Figure 7.8: (a) Band alignments vs. r/R in the [100] direction for a 1-D system: a $Si_{0.8}Ge_{0.2}$ cylinder inside a Si matrix. The direction of the z-axis is along [001] crystal direction. All energies are plotted the same way as in Fig. 7.7. (b) Energy bands vs. real space direction in the matrix at r=R.

0.06 eV for the conduction band and 0.01 eV for valence band as plotted in Fig. 7.9(b).

To summarize these results of band extreme and offsets, Fig. 7.10 shows the conduction band and valence band positions in the $Si_{1-x}Ge_x$ inclusion and in the Si matrix (at r=R in the [100] real-space direction) as a function of Ge concentration in the sphere and cylinder (z-axis along [001] direction) structures. Also shown for comparison are the band edges of a conventional 2-D biaxially-strained $Si_{1-x}Ge_x$ layer on a Si (100) substrate (as in Ref. [257]) calculated with the parameters in Table 7.1. (The [100] real space direction represents the conduction band minimum in the Si matrix at r=R. Because of the uniform strain in the SiGe in all three structures, there is no dependence of conduction band minimum on real space direction in the SiGe in all the cases). For both 1-D and 0-D cases, the Δ conduction band minimum decreases in the matrix and increases in the inclusion, while the valence band edge increases in the inclusion faster than in the matrix as Ge concentration increases, in both cases leading to a Type II band alignment. The valence band maximum in the matrix lies marginally higher in other directions in the 0-D and 1-D particles as discussed earlier, but not enough to affect the sign of band offset. For a pure Ge pseudomorphic particle inside a Si matrix, the conduction band offsets are 0.80 eV and 0.51 eV and the valence band offsets are 0.41 eV and 0.60 eV in the [100] real-space direction for 0-D and 1-D respectively. In the conventional 2-D case the valence band is higher in the SiGe, as in the 0-D and 1-D cases. The lack of dependence of the conduction band on the Ge concentration in the 2-D case leads to a much smaller conduction band offset in the 2-D case compared with the 0-D and 1-D cases, however. While the exact band distribution will depend on the exact shape of the 0-D and 1-D inclusions, the model sphere and cylinder systems chosen here clearly show that care must be taken when directly relating photoluminescence energies to the bandgap of the inclusions, as the band type in these structures can be strongly Type II.

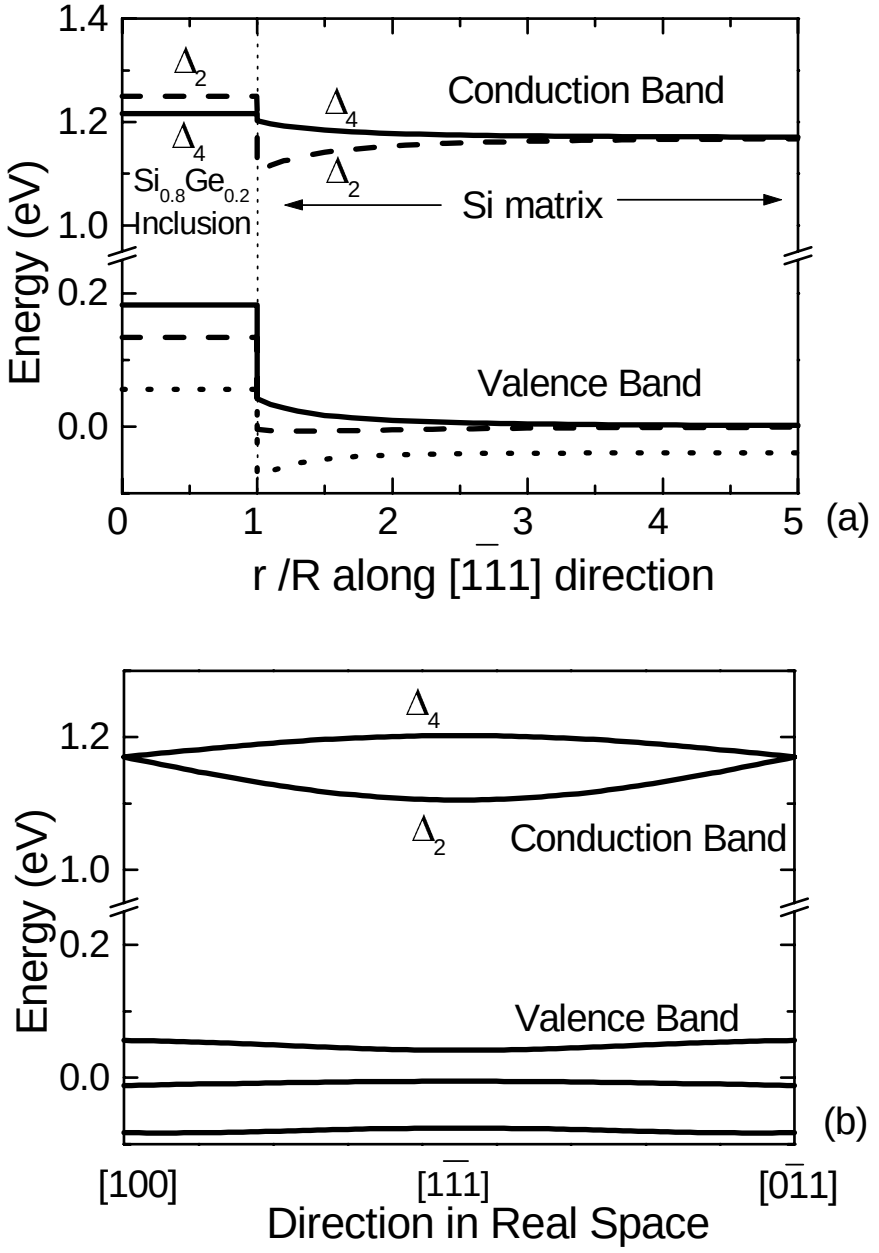


Figure 7.9: (a) Band alignments along the [1$\bar{1}$1] real space direction for a $Si_{0.8}Ge_{0.2}$ cylinder with z-axis in the [011] direction. All energies are plotted the same way as in Fig. 7.7. (b) Energy bands vs. real space direction in the matrix at r=R.

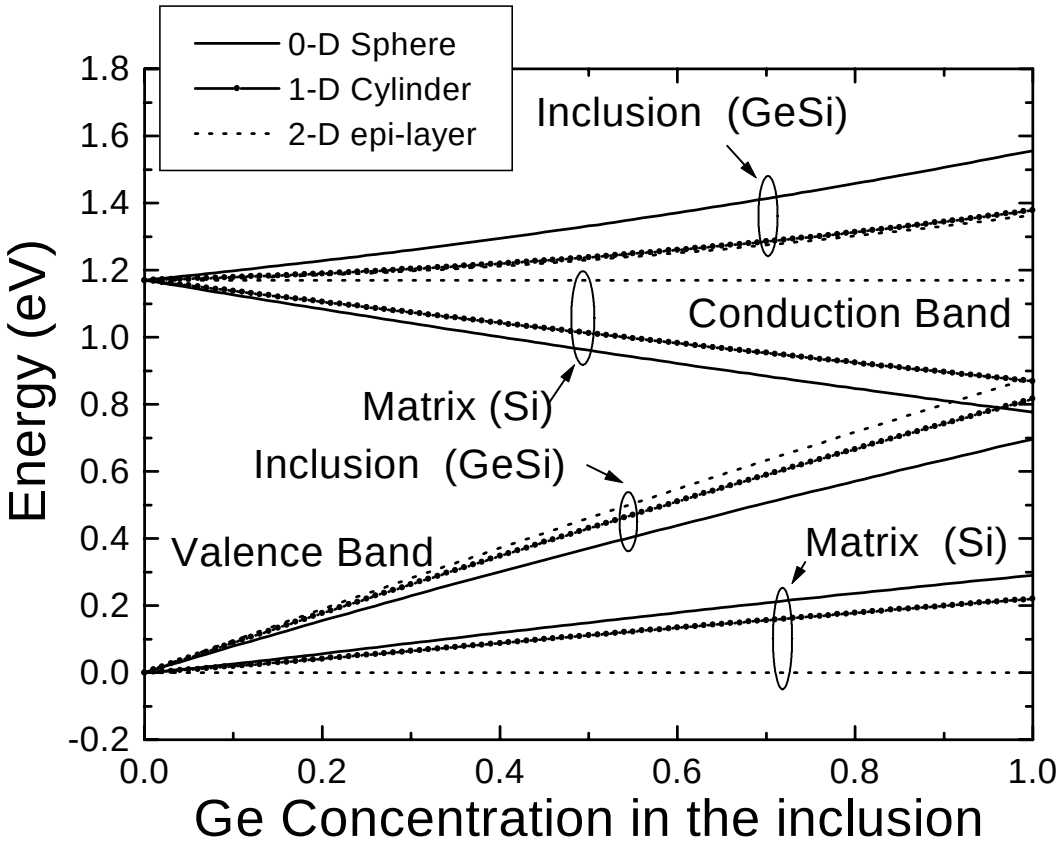


Figure 7.10: Valence and conduction band edges in a $Si_{1-x}Ge_x$ inclusion and in the Si matrix as a function of the Ge concentration for 1-D cylinder (axis in [001] direction) and 0-D sphere structures at the [100] real space boundary between matrix and inclusion (r=R). The conduction and valence bands of a conventional 2-D $Si_{1-x}Ge_x$ strained layer on a Si (100) substrate are also shown.

7.4.2 Anisotropy and Finite Element Modeling

In the above calculations, we assumed that the elastic properties of the semiconductors are isotropic, i.e. $c_{11} - c_{12} - 2c_{44} = 0$ in the compliance matrix of a cubic crystal:

$$\begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{xy} \\ \sigma_{xz} \\ \sigma_{yz} \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{44} \end{bmatrix} \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{xy} \\ \varepsilon_{xz} \\ \varepsilon_{yz} \end{bmatrix}$$

Under this isotropic assumption, we used the bulk modulus $\kappa = (c_{11}+2c_{12})/3$, Poisson's ratio $\nu = \frac{c_{12}}{c_{11}+c_{12}}$, and Young's modulus $E = \frac{(c_{11}-c_{12})(c_{11}+2c_{12})}{c_{11}+c_{12}}$ so that the strain was only a function of r/R. But actual cubic crystal materials (e.g. Si and Ge) are anisotropic, i.e. $c_{11} - c_{12} - 2c_{44} \neq 0$ [273, 274]. The Si anisotropy factor $\frac{2c_{44}}{c_{11}-c_{12}} = 1.56$. Its Young's modulus is maximum in the $< 111 >$ directions and minimum in the $< 100 >$ directions.

To examine whether the isotropic assumption will affect the strain results, we then used finite element analysis to calculate the strain in the anisotropic case using the commercially available program "DYNAFLOW" [275]. The results indicate that there is only a small change of the strain and energy levels from the isotropic results. The energy bands of 1-D and 0-D $Si_{0.8}Ge_{0.2}$/Si structures shift less than 0.01 eV, which indicates the isotropic elasticity assumption is good to first order. The results of the strain distribution can not be simply added to the plots in Fig. 7.2 and Fig. 7.4, because in the anisotropic structures strain can not be reduced to two normal components: tangential (ε_τ) and radial (ε_r).

7.5 $Si_{1-x}Ge_x$/ Si V-groove Structures

Recently the growth and photoluminescence measurements of $Si_{1-x}Ge_x$ quantum wires on a Si substrate with etched V-grooves have been reported[276, 277]. Strain distributions of a single wire [278] and an array [279] of wires were calculated assuming the materials are

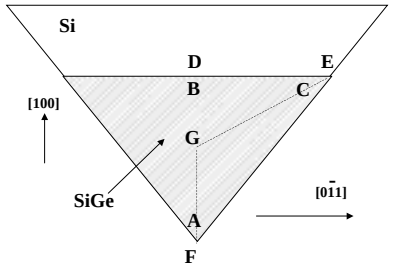


Figure 7.11: Cross-section of a SiGe epitaxial layer with Si cap on a V-grooved Si (100) substrate.

isotropic. Ref. [279] also analytically calculated the effect of strain on the overall bandgap in wires, but the effect on the individual band-edges and electron and hole confinement energies were not reported. In this work we numerically model the strain in quantum wire structures, fully considering anisotropic material properties, and present effects individually on both conduction and valence bands. We then calculate quantum confinement energies of carries in their wires as the wire dimensions become small, and relate the results to photoluminescence experiments.

We model the V-groove structure as a long wire with a triangular cross-section buried in an infinite matrix as shown in Fig. 7.11. After the Si is etched, a sharp corner between two {111} planes is formed. $Si_{1-x}Ge_x$ is selectively grown on the bottom of the V-groove and capped by a Si epitaxial layer. The growth direction is [100] and the axis of the quantum wire is in the [011] direction, forming an approximately triangular cross-section with its width $\sqrt{2}$ larger than its depth. We assume that the interface is free from any defects and dislocations. The alloy segregation effect, which might cause the alloy to be non-uniform throughout the triangle, is also neglected. Using finite element analysis [275], we calculated the strain distribution. Note that the strain distribution relies only on the shape of the cross-section. Once the strain distribution is known, the band alignments are derived from the same methods discussed before. The conduction band minimum is the two-fold Δ_2 band (in the [100] k-space direction) lying in the $Si_{1-x}Ge_x$ near the bottom of the V-groove (point A) and the valence band maximum is the heavy-hole band in the $Si_{1-x}Ge_x$ at the corner of the top interface (point C). Band lineups of the points along the SiGe/Si interface and along

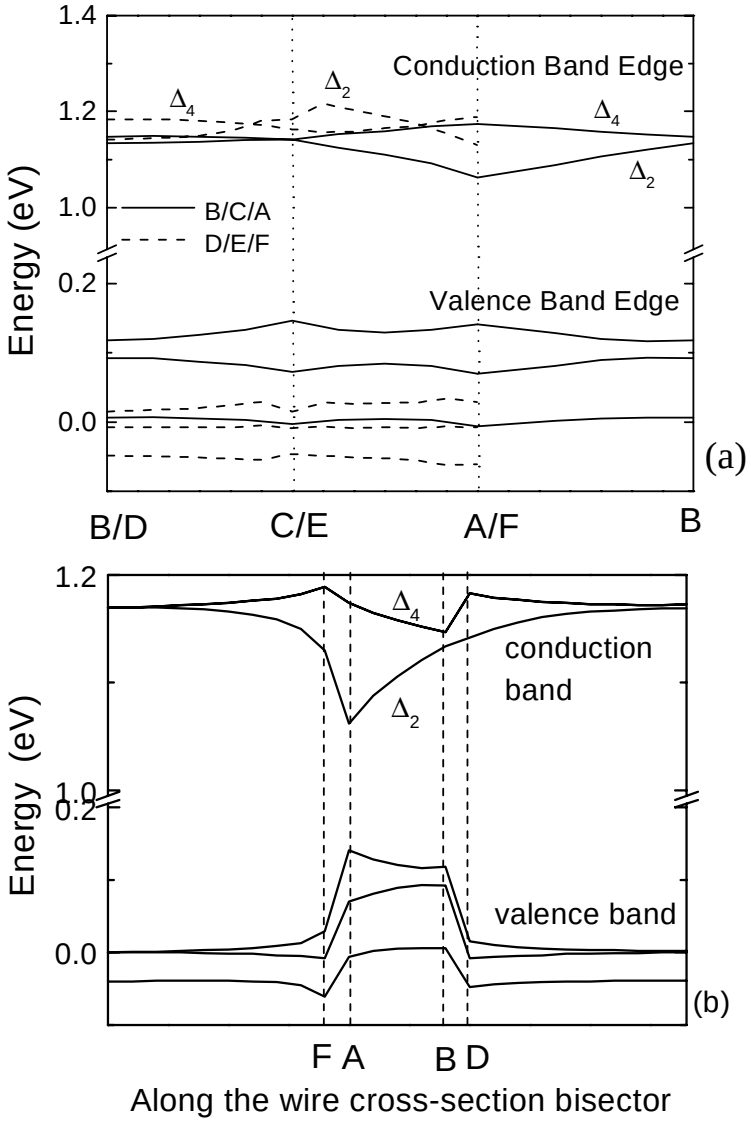


Figure 7.12: The Δ conduction bands and valence bands (a) along the $Si/Si_{0.8}Ge_{0.2}$ interface of the V-groove structure, and (b) along the vertical wire cross-section bisector. In (a) the solid lines are for points inside the SiGe and the dashed lines in Si.

the wire cross-section bisector are shown in Fig. 7.12. The reference energy point is the valence band edge in the Si far from $Si_{1-x}Ge_x$ interface. Far from the SiGe, the conduction band edge in the Si is 1.17eV. At point A in the SiGe, the Δ_2 conduction band is 0.07eV lower than the lowest conduction band point in the Si which occurs in the Δ_2 band at point F. At point C, the valence band edge in the $Si_{1-x}Ge_x$ is 0.13eV higher than point E in the Si. A 3-dimensional map of the Δ_2 conduction band and the valence band edge for $Si_{0.8}Ge_{0.2}$ in Si are plotted in Fig. 7.13 and Fig. 7.14 respectively. In SiGe the Δ_2 bands are lower and the valence band edges are higher than in Si. Note that as in the case of a symmetric cylinder, holes are confined to the SiGe. However, while in the symmetric cylinder case the conduction band minimum is in the Si matrix, for V-groove structure the lower conduction band is in the SiGe (at point A). This results from the shape of the structure, which causes a large non-hydrostatic strain at point A which splits conduction bands more strongly in the SiGe than in any of the other cases discussed in this work. This result is the only one in which electrons are strongly confined to SiGe. The conduction bands at point C are not significantly split in the SiGe compared with those at point A because the bisector of the triangle vector at point C (G-C) has a different crystalline orientation than that for the vector at point A (G-A), and because of the six-fold symmetry of the conduction band minima.

To consider the quantum confinement effects of a small wire cross-section on the electron and hole ground state energies, the electron and hole confinement energies are estimated using the perturbation approach discussed in Ref. [253] from the 2-D potential profiles we calculated from the strain fields. Here electric field and strain effects on the coupling between upper valence bands are neglected. First the 1-D Schrödinger equation was solved in the [100] direction using a Si longitudinal electron effective mass 0.98 (for the Δ_2 conduction band in [100] k-direction) and a heavy hole effective mass 0.49 at a given position in the $[0\bar{1}1]$ direction. The resulting potential profiles as a function of positions in the $[0\bar{1}1]$ direction were then solved using the 1-D Schrödinger equation (using a Si transverse electron effective mass of 0.19 and heavy hole effective mass of 0.49) to get the approximate energies of the ground states. The effect of Ge on the masses was second order and not considered.

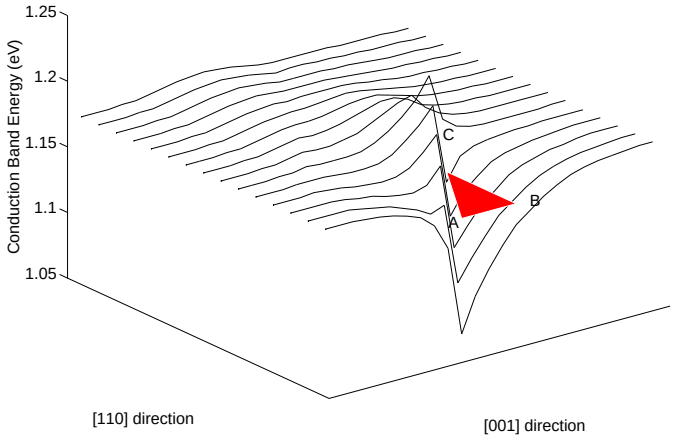


Figure 7.13: Δ_2 conduction band edge of the structure drawn in Fig. 7.11. The filled triangle shows the area of the $Si_{0.8}Ge_{0.2}$ region. Note the x and y axes are drawn on different scales.

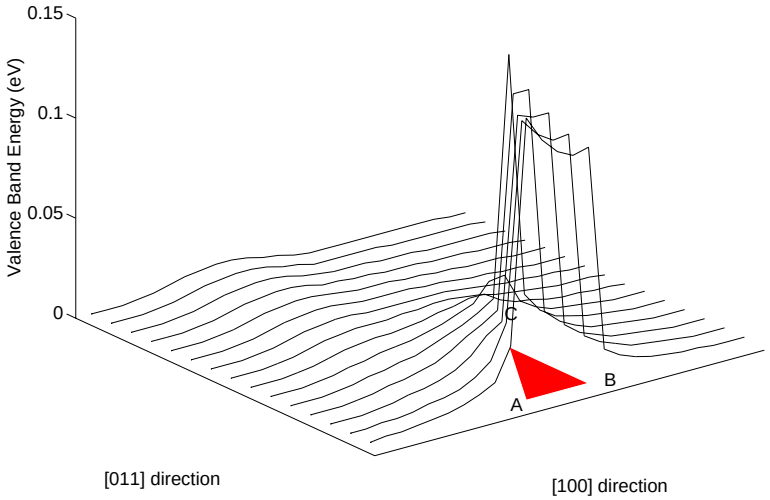


Figure 7.14: Valence band edge of the structure drawn in Fig. 7.11. The triangle shows the $Si_{0.8}Ge_{0.2}$ region. Note the x and y axes are drawn on different scales.

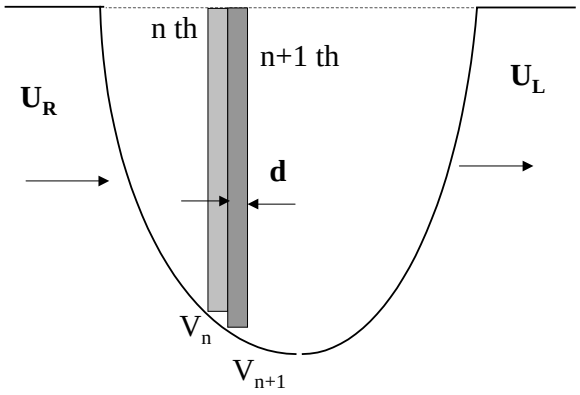


Figure 7.15: Potential is divided into step functions in small segments to calculate the eigenvalues of the Schrödinger equation using a *transfer matrix method*.

A transfer matrix method is applied to calculate the Schrödinger equation with an arbitrary potential profile [280]. The potential is divided into step-like functions in small segments (Fig. 7.15). For the nth segment, the wavefunction can be written as:

$$\varphi_n = a_n^+ e^{ik_n y} + a_n^- e^{-ik_n y},$$

or in the form of matrix as:

$$\varphi_n = \begin{pmatrix} a_n^+ \\ a_n^- \end{pmatrix}$$

where $k_n = \sqrt{\frac{\hbar^2}{2m^*}(E - V_n)}$. E is the eigen-energy and V_n is the potential of the nth segment. If $E < k_n$, then k_n is imaginary. The wave function in the (n+1)th segment has a relation to that of the nth through a transfer matrix T_n:

$$\varphi_{n+1} = T_n \varphi_n$$

where

$$T_n = \begin{pmatrix} 1 + \frac{k_n}{k_{n+1}} & 1 - \frac{k_n}{k_{n+1}} \\ 1 - \frac{k_n}{k_{n+1}} & 1 + \frac{k_n}{k_{n+1}} \end{pmatrix} \begin{pmatrix} e^{ik_n d_n} & 0 \\ 0 & e^{-ik_n d_n} \end{pmatrix} \tag{7.44}$$

where d_n is the width of the nth segment. Repeating the method, from right to left, the wave function thus has

$$\begin{pmatrix} a_R^+ \\ a_R^- \end{pmatrix} = T \begin{pmatrix} a_L^+ \\ a_L^- \end{pmatrix}, \quad T = T_N \cdot T_{N-1} \cdots T_1 \cdot T_0. \tag{7.45}$$

For a bound state,

$$a_L^+ = 0, a_R^- = 0,$$

e.g.

$$T_{22} = 0. \tag{7.46}$$

From Eqns. (7.44-7.46), the eigen-energy of the Schrödinger equation can be found.

The electron and hole confinement energies (energy difference from the ground state of large size) for $Si_{0.8}Ge_{0.2}$, $Si_{0.6}Ge_{0.4}$, and $Si_{0.4}Ge_{0.6}$ quantum wires are shown in Fig. 7.16. The quantum effect is significant when the height of the SiGe is less than 10nm. For a 5nm high $Si_{0.8}Ge_{0.2}$ triangle, the confinement energies of the electron and heavy-hole are about 0.07eV and 0.05eV. The confinement energies (size effect) of the electron and hole increase as Ge concentration increases. For 5nm high $Si_{0.6}Ge_{0.4}$ and $Si_{0.4}Ge_{0.6}$ triangles, the electron (heavy-hole) confinement energies increase to 0.12eV (0.08eV) and 0.18eV (0.12eV) respectively. These calculations can be used to predict the photoluminescence energies of the V-grooves. The differences between the energies of the lowest electron and highest hole (heavy hole in this case) states are given in Fig. 7.17 to the first order for different $Si_{1-x}Ge_x$ sizes and x values (0.2, 0.4, 0.6). Although the electron and hole wavefunctions will have their maxima in different locations within the SiGe, we neglect any possible resulting electric field effects on the transition energy. Any exciton effects are also neglected. First notice that for large SiGe regions, when only strain and not quantum effects are relevant, the transition energies are smaller than those predicted for planar pseudomorphic SiGe layers on Si (100) with the same x (shown for reference as dashed lines). For example, the transition energy is 0.94eV for a $Si_{0.8}Ge_{0.2}$/Si V-groove structure with a height of 50nm, compared with the 1.09eV $Si_{0.8}Ge_{0.2}$ bulk value and 0.99eV for the 2-D strained $Si_{0.8}Ge_{0.2}$ epitaxial layer. This larger decrease in transition energy in V-groove structures is mostly due to a significantly lower conduction band and higher valence band with SiGe in the V-groove. Such an effect does not occur in 2-D structures. When the size decreases, the transition energy increases. For x=20%, the transition energy of a triangle less than 7nm high is predicted to be larger than that of a 2-D conventional structure.

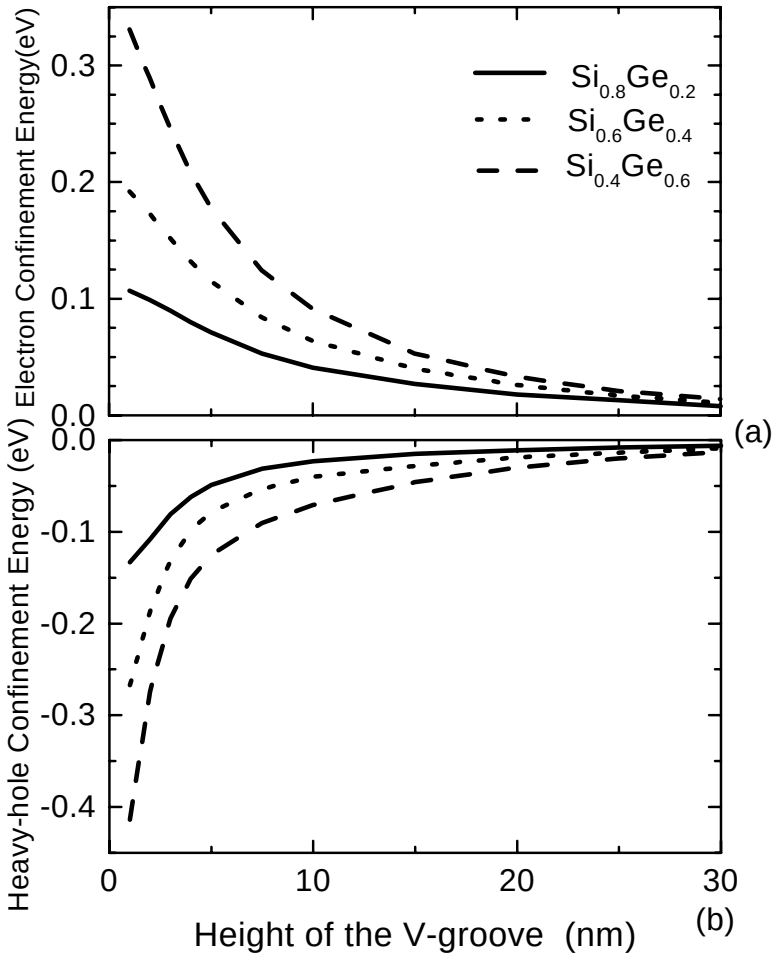


Figure 7.16: The confinement energies (energy difference from the ground state of large size structure) of electrons (a) and heavy-holes (b) as a function of the height of the SiGe V-groove structure with Ge concentrations of 20%, 40%, and 60%.

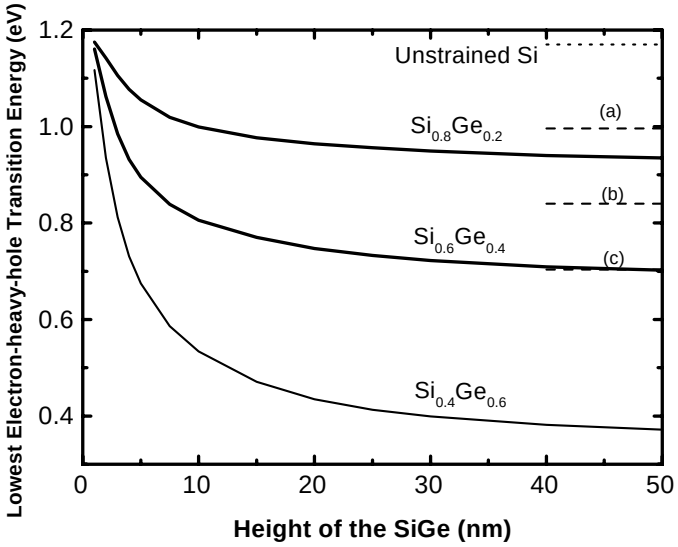


Figure 7.17: The lowest transition energies from electron to heavy-hole as a function of the height of the V-groove $Si_{1-x}Ge_x$ quantum-wire with x=20%, 40%, and 60%. The dashed lines show the photoluminescence energies from the 2-D conventional $Si_{1-x}Ge_x$ biaxially strained-layer with (a) x=20%, (b) x=40%, and (c) x=60%.

7.6 Summary

In summary, we have calculated the band lineups of 1-D and 0-D structures: a sphere, a long cylinder, and a V-groove filled with SiGe inside of an infinite Si matrix. The methodology used in this chapter is also relevant to vertical MOSFET's. Using ultra-thin pillar structures for double-gate MOSFET's, the strain of pseudomorphic SiGe and SiGeC layers will be different from that of planar epitaxial layers. The special structures presented in this chapter will assist the understanding of strain in other three-dimensional cases and the method used in this Chapter can be applied to the case of ultra-thin pillar with SiGeC layers.

For $Si_{1-x}Ge_x$ inside of a Si matrix, the band alignments are strongly type II for the both the sphere and cylinder cases. The conduction band minima lie in the Si matrix and the valence band maxima lie inside the $Si_{1-x}Ge_x$ inclusion. For the V-groove SiGe one-dimensional structure, the conduction band minimum and the valence band maximum are both in SiGe but at different points in real space. The transition energies from the

lowest electron state to the highest heavy hole state are estimated by considering quantum effects. This work demonstrates the importance of accurately accounting for the effects of 3-D strain distributions in strained-layer nanostructures, and that the relationship of photoluminescence energies to particle compositions may in some cases not be straightforward.

Chapter 8

The Effect of Carbon on Band Alignments and Band Gaps in $Si_{1-x-y}Ge_xC_y$ /Si (001) Structures

As $Si_{1-x-y}Ge_xC_y$ pseudomorphic layers have been introduced into vertical MOSFET's in Chapter 5, further study of the band alignment of the SiGeC/Si (001) heterojunction is necessary for better understanding of carrier transport in these MOSFET's. Three-dimensional effects on the strain and band alignments in the alloy layers have been discussed in the previous chapter. In this chapter, the roles of substitutional carbon atoms on the strain and band alignments of crystalline silicon or silicon-germanium alloys are studied in two aspects: the intrinsic effect of carbon and the change in strain induced in pseudomorphic epitaxial layers. A model based on the "*model-solid theory*" is presented to calculate the dependence of the band gap and band alignments of $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ alloys commensurate on Si (100) substrates on carbon concentration for germanium fractions less than 40% and carbon fractions less than 3%. The model separates the effects of strain and the intrinsic effects of carbon and treats them independently. The model results are in good agreement with nearly all available experimentally-measured effects of carbon on band gap, valance band offset, and conduction band offset for compressive- and tensile-strained $Si_{1-x-y}Ge_xC_y$ alloys as well as tensile-strained $Si_{1-y}C_y$ alloys.

The work in this chapter is based on the work first presented in a rough form in the Ph.D. thesis of Chia-Lin Chang (Princeton University). In this chapter this past work is extended to new ranges and compared to the available experimental data.

8.1 Introduction

In recent years, tremendous developments have occurred in the field of semiconductor heterojunctions and superlattices and their applications in electronic devices. The introduction and improvement of novel growth techniques (i.e. molecular-beam epitaxy and chemical vapor deposition) have made it possible to produce extremely high-quality epitaxial interfaces, not only between lattice-matched semiconductors, but also between lattice-mismatched semiconductors. For example, between Si and Ge, the lattice mismatched is 4%. Lattice-mismatched heterostructures can be grown with essentially no misfit defect generation if the layers are sufficiently thin; the mismatch is then completely accommodated by uniform lattice strain [281, 282]. The resulting so-called "pseudomorphic" interface is characterized by an in-plane lattice constant of the same value throughout the structure. In the late 1980's, high quality strained $Si_{1-x}Ge_x$ alloys were reported. Novel devices based on heterostructures have been demonstrated with superior electrical [283, 284] and optical [285, 286, 287] properties. However the benefit of band engineering in these devices is limited by the "critical thickness". Only below this thickness are the epitaxial layers pseudomorphic and defect-free. Fig. 8.1 shows the critical thickness for $Si_{1-x}Ge_x$ alloy grown on Si (001) substrates as a function of Ge concentration at thermal equilibrium [288]. If 50% Ge is needed in a SiGe/Si heterostructure to give a sufficiently large band-offset, the thickness of the SiGe alloy has to be less than 50 Å. Furthermore, the conduction band offset between a SiGe epitaxial layer and a Si (001) substrate is essentially zero [289, 290, 291, 256], making it difficult to achieve high electron mobility by n-type modulation doping.

The technological interest in $Si_{1-x-y}Ge_xC_y$ (beyond that of $Si_{1-x}Ge_x$ layers) is driven by two basic capabilities enabled by the addition of carbon: the ability to engineer the strain (and thus band gaps) to a degree impossible with $Si_{1-x}Ge_x$ alone, and the ability

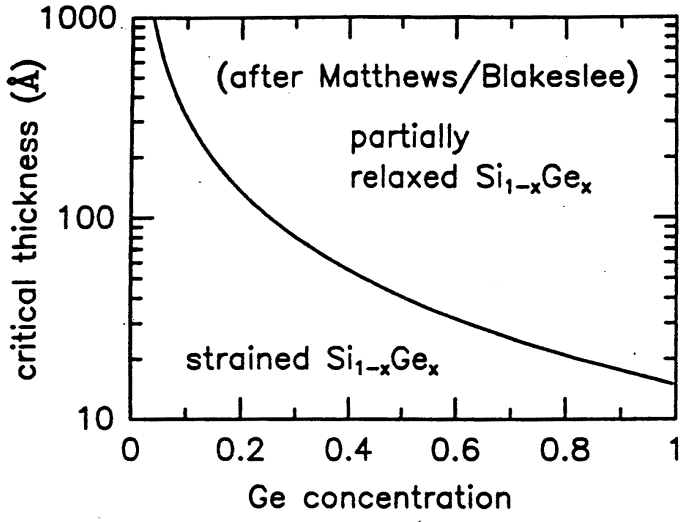


Figure 8.1: Equilibrium critical thickness of strained $Si_{1-x}Ge_x$ films on (001) silicon substrates as a function of Ge fraction. From Ref. [288].

to control the diffusion of dopants. Due to the small size of the carbon atom, adding carbon to compressively stressed $Si_{1-x}Ge_x$ commensurate on Si(100) reduces the stress, with one substitutional carbon atom compensating for the stress induced by 8-10 germanium atoms. Layers with at least 1% substitutional carbon have been demonstrated at low growth temperature (400-600^{o}C) by remote plasma-enhanced chemical vapor deposition [292], molecular beam epitaxy [293, 294], and chemical vapor deposition [295, 296, 204]. Adding carbon to such commensurate strained films slowly increases the band gap (20-25 meV/%C) [297, 298, 299, 218], but less than that which would occur if the stress were reduced solely by reducing the Ge fraction, leading to an increased critical thickness for a given band gap (Fig. 8.2) [205]. This might be useful for heterojunction bipolar transistors (HBT's) [299]. Further, if carbon is added to silicon without germanium to form a $Si_{1-y}C_y$ alloy on Si(100), the tensile stress causes the layer to have a conduction band substantially lower than that in silicon. Thus for the first time, modulation doping to achieve high mobility electrons could be achieved in a structure commensurate to a silicon (100) substrate without relaxed buffer layers [300].

The second driving force for the study of substitutional carbon is the reduction of

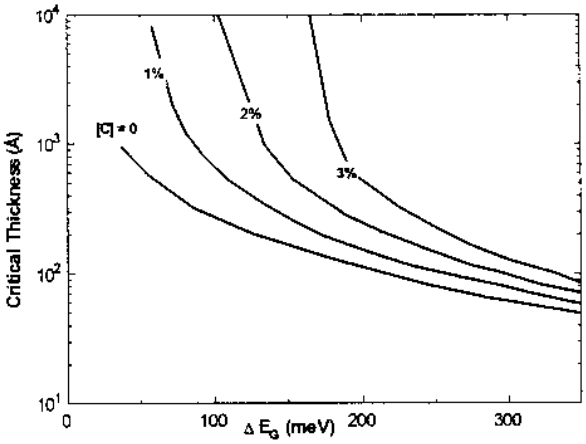


Figure 8.2: Comparison of the critical thickness/bandgap trade-off for $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ on Si (001) substrates. The critical thickness is from the Matthews-Blakeslee equilibrium model, assuming that the elastic properties of $Si_{1-x-y}Ge_xC_y$ are the same as those of SiGe (after Ref.[205]).

dopant diffusion caused by OED or TED, especially boron, in $Si_{1-y}C_y$ or $Si_{1-x-y}Ge_xC_y$ layers and in nearby silicon regions, due to the reduction in the local interstitial populations [191, 188, 301, 186]. This has been applied in devices including HBT's [191, 212] and vertical MOSFET's as demonstrated in Chapter 5 and Chapter 6. Close examination of this effect is important because dopant diffusion in process integration steps (oxidation, ion implantation) may disturb device profiles requiring nm-precision and thus degrade device performance. Several review papers have been published on the SiGeC material system [302, 303].

With the increasing importance of $Si_{1-x-y}Ge_xC_y$ commensurate to Si(100), there is a need to determine the band alignments and the band gaps as a function of Ge and C composition. As such there have been extensive experiments to date. Band-edge photoluminescence is a direct measurement of band gap and has been used by many groups to determine the carbon and germanium effects on the band gaps of $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ alloys [297, 298, 304, 305, 306, 307, 197, 308, 309]. Lanzerotti *et al.* demonstrated a carbon effect on band gap through the temperature dependence of heterojunction bipolar

transistor collector current [299]. Band alignments have been extracted from metal-oxide-semiconductor capacitance measurements on $Si_{1-x-y}Ge_xC_y$ /Si and $Si_{1-y}C_y$/Si heterostructures [310, 221, 311]. Admittance spectroscopy has been used by Stein *et al.* [312] and Singh *et al.* [313] for the band alignments. The effect of carbon on the valance band offset of $Si_{1-x-y}Ge_xC_y$ has been reported by Chang *et al.* using capacitance-voltage measurements on p^+-$Si_{1-x-y}Ge_xC_y/p^-Si(100)$ unipolar diodes [218]. Chang *et al.* also performed internal photoemission measurements on p^+-$Si_{1-x-y}Ge_xC_y/p^-Si(100)$ heterojunctions to study the carbon effect on the valance band offset [314]. Kim *et al.* measured X-ray photoelectron spectroscopy for the valance band offsets [216]. Using the saturation carrier concentration at low temperature, the conduction band offset has also been extracted from modulation-doped $Si/Si_{1-y}C_y/Si$ [300].

Interpretation of the results is complicated by the fact that the alignments are expected to depend on both the film composition and the strain, both of which often are changing in the course of a given experiments. In this chapter we will use the "*model-solid theory*" [256, 257] to systematically calculate the effect of carbon on the band alignments and band gaps in $Si_{1-x-y}Ge_xC_y$/Si heterostructures commensurate to Si (001) substrates. We will focus only on the states near the band edges and not discuss upper band transitions. The model has only two adjustable parameters, but gives good agreement with experiments under at least four different experimental conditions.

8.2 General Approach on Band Alignment

In this chapter, the band alignments in the $Si_{1-x-y}Ge_xC_y/Si(001)$ material system for low Ge ($x<0.4$) and C ($y<0.03$) fractions are modeled using three basic premises:

(i) The position of any energy band i (or band gap E_i^{total}) can be modeled as the independent contribution of an "intrinsic" (chemical) effect due to the chemical composition of the alloy ($E_i^{int.}$) plus the effect of strain which causes a change in this band position

from its position without strain (ΔE_i^{strain})

$$E_i^{total} = E_i^{int.} + \Delta E_i^{strain}. \tag{8.1}$$

(ii) The intrinsic effects on band positions can be modeled as linear in both the Ge and C fractions x and y, respectively:

$$E_i^{int.} = (1-x-y)E_i^{int.,Si} + xE_i^{int.,Ge} + yE_i^{int.,C}. \tag{8.2}$$

$E_i^{int.,C}$, $E_i^{int.,Ge}$ should be viewed only as fitting parameters and not the band position in diamond or bulk Ge.

(iii) The changes in position of band edge i or band gap in a layer due to strain (ΔE_i^{strain}) may be described solely by deformation potentials and the macroscopic strain in the layer. This effect is the independent of the layer composition.

We next formally develop this approach to first calculate the positions of the bands due to intrinsic effects, and then to develop the strain effects. Finally, the results are compared to experimental data. A similar model with slightly different parameters and assumptions has also recently been published [315], and will be contrasted with our results.

8.3 Intrinsic C and Ge Effects

We assume that bulk unstrained $Si_{1-x-y}Ge_xC_y$ alloys (with small x and y) have Si-like band structures. There are six minima in the conduction band along the [001], [010], and [100] directions (Δ_2 and Δ_4), all of which are degenerate and equal to their weighted average $E_{C,av}^{int.}$.

$$E_{C,av}^{int.} = E_{C,\Delta_2}^{int.} = E_{C,\Delta_4}^{int.} \tag{8.3}$$

The topmost valance band at the Γ point would be threefold degenerate in the absence of spin-orbit splitting. In an unstrained layer, the spin-orbit interaction lifts the degeneracy and splits the bands by an amount Δ_0. With respect to the weighted average of the valance band edges $E_{V,av}^{int.}$, two bands (the heavy hole and light hole denoted as HH and LH) are

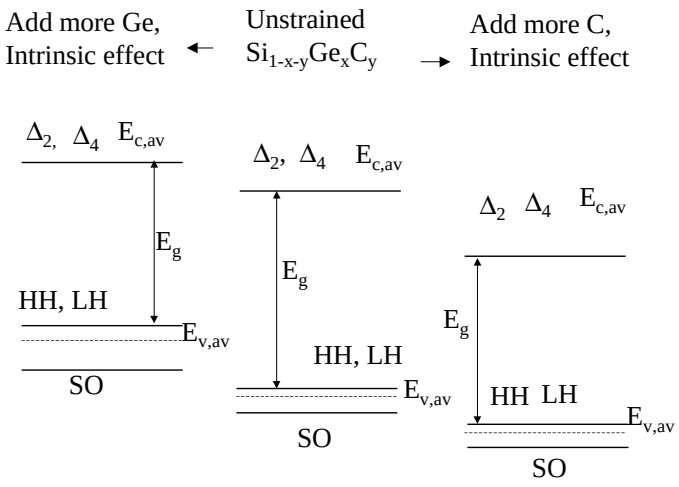


Figure 8.3: Schematic of Ge and C intrinsic effect on unstrained $Si_{1-x-y}Ge_xC_y$ material.

shifted up by $\Delta_0/3$ and one band (denoted as SO) is shifted down by $2\Delta_0/3$, as shown in Fig. 8.3.

$$E^{int.}_{V,LH} = E^{int.}_{V,HH} = E^{int.}_{V,av} + \frac{1}{3}\Delta_0 \tag{8.4}$$

$$E^{int.}_{V,SO} = E^{int.}_{V,av} - \frac{2}{3}\Delta_0 \tag{8.5}$$

The band gap of the unstrained material is

$$E^{int.}_{g} = E^{int.}_{C,av} - E^{int.}_{V,av} - \frac{1}{3}\Delta_0 \tag{8.6}$$

Thus to determine all the relevant positions of the band edges in the unstrained layers, one needs to know four fundamental band position parameters for any layer ($E^{int.}_{V,av}$, Δ_0, $E^{int.}_{g}$, and $E^{int.}_{C,av}$), only three of which are independent. According to the basic premise of the model, each of these parameters is linearly dependent upon Ge and C fractions x and y, [Eqn (8.2)]. Thus there are three independent parameters one must know, for each of Si, Ge and C, for a total of nine parameters.

For Si and Ge, these parameters are given in Table 8.1. The vacuum level is used as the reference energy for the band edge positions. For Ge, $E^{int.}_{V,av}$ and Δ_0 are chosen as their

Parameters (eV)	Materials			
	Si	Ge	C	$Si_{-x-y}Ge_xC_y$
$E_{V,av}^{int.}$	-7.03	-6.35	-9.32	-7.03+0.68x-2.20y
Δ_0	0.04	0.3	0	0.04+0.26x-0.04y
$E_{V,HH}^{int.} = E_{V,LH}^{int.}$	-7.02	-6.25	-9.23	-7.02+0.77x-2.21y
$E_{V,SO}^{int.}$	-7.06	-6.55	-9.23	-7.06+0.51x-2.17y
$E_g^{int.}$	1.12	0.69	-0.71	1.12-0.43x-1.83y
$E_{C,av}^{int.} = E_{C,\Delta_2}^{int.} = E_{C,\Delta_4}^{int.}$	-5.90	-5.56	-9.94	-5.90+0.34x-4.04y

Table 8.1: Values of parameters used in the calculation of the intrinsic effect on the band structure. Note that some parameters do not have physical meaning, but are only used for fitting $Si_{1-x-y}Ge_xC_y$ ($x \leq 0.4$, $y \leq 3\%$) data. Values for Si are from Ref.[257], and relaxed $Si_{1-x}Ge_x$ band gaps from Ref.[271] (the linear relation with x is valid only for Ge compositions where $x \leq 0.4$).

bulk values [312, 313]. Linear interpolation between the Si and Ge bulk values yields those for $Si_{1-x}Ge_x$ alloys, in accordance with Ref. [256, 257]. $E_{C,av}^{int.}$ and $E_g^{int.}$ of Ge are extracted from the fitting of band gaps of $Si_{1-x}Ge_x$ alloys with $x<0.4$, and are not equal to their bulk values, because of the "bowing" of the $Si_{1-x}Ge_x$ band gap when $x>0.4$ [271].

The intrinsic effect of C on the band gap of $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ random alloys has been calculated or modeled by several groups [316, 317, 318, 319]. Logarithmic interpolation between Si and SiC (or diamond) yields a predicted intrinsic effect on the band gap of 17 meV/%C for initial amounts of C added to Si or $Si_{1-x}Ge_x$[316]. This interpolation is not appropriate for modeling the initial effects of carbon, due to an experimentally observed negative "bowing" of the band gap vs. composition. Other studies have calculated the effect of C in $Si_{1-y}C_y$ structures from first principles and found that initial levels of C should actually decrease the band gap, with effects as large as 100 meV/%C [318, 319].

Here we will treat the effect of C on the band positions, $E_i^{int.,C}$, solely as a fitting parameter adjusted to reproduce experimental data. We will assume the spin-orbit split-off energy of carbon $\Delta_0^{int.,C}$ to be zero. Due to the small amount of carbon (<3%) incorporated in Si or SiGe, this has a negligible effect. The remaining two independent parameters are

taken to be:

$$E_{V,av}^{int.,C} = -9.23eV \tag{8.7}$$

$$E_{C,av}^{int.,C} = -9.94eV. \tag{8.8}$$

The effects of adding Ge or C to fully relaxed alloys [not commensurate on a Si(001) or other substrates] is summarized in Table 8.1 and plotted in Fig. 8.3. As Ge is added, the valance band maxima (HH and LH) move up, and the six-fold degenerate conduction band minima move up at a slower rate than the valance band. These effects combine to yield a net band gap reduction. As C is added to a fully relaxed alloy, the initial amount of C lowers the level of the valance band edge as well as the conduction band edge, with the net result of decreasing the band gap at -18 meV/%C. Later in the chapter the implications of these parameters will be compared with experimental data, and shown to give good agreement under many different strain conditions.

8.4 Strain Effects

For pseudomorphic epitaxy on a Si (001) substrate, strain arises in the $Si_{1-x-y}Ge_xC_y$ layer because the in-plane lattice constant of $Si_{1-x-y}Ge_xC_y$ is changed to that of the substrate, causing strain along the axes parallel ($\varepsilon_{||}$) to the interface and simultaneously introducing strain in the perpendicular direction ($\varepsilon_{\perp}$):

$$\varepsilon_{||} = \frac{a_{Si} - a_*^{relaxed}}{a_*^{relaxed}} \approx \frac{a_{Si} - a_*^{relaxed}}{a_{Si}}, \tag{8.9}$$

$$\varepsilon_{\perp} = -2\frac{c_{12}}{c_{11}}\varepsilon_{||}, \tag{8.10}$$

where the unstrained $Si_{1-x-y}Ge_xC_y$ lattice constant $a_*^{relaxed}$ is estimated through a linear interpolation of Si, Ge, and diamond:

$$a_*^{relaxed} = (1-x-y)a_{Si} + xa_{Ge} + ya_C. \tag{8.11}$$

Application of Vegard's law [Eqn. (8.11)] for calculation of the relaxed lattice constant of $Si_{1-x-y}Ge_xC_y$ is still under debate[320, 321, 322], but in this work we assume a fixed

Parameter	a_{Si}	a_{Ge}	$a_{diamond}$	C_{11}	C_{12}	a_v^Γ	a_c^Δ	b	Ξ_u^Δ
	5.431 Å	5.657 Å	3.567 Å	1.675 Mbar	0.650 Mbar	2.46 eV	4.18 eV	-2.35 eV	9.16 eV

Table 8.2: Values of parameters used in the calculation of the strain effects on the band structure. All deformation potential values are based on Ref.[257], except a_c^Δ, which is from Ref.[316]. Lattice constants are from Ref.[324].

Ge/C strain compensation ratio of 8.3 [303]. Constants c_{11} and c_{12} of $Si_{1-x-y}Ge_xC_y$ are replaced by those of Si in this work for simplicity, so that band gap and band offsets are first-order expressions in x and y.

Strain has two main effects on the band structure of a semiconductor. Hydrostatic strain shifts the weighted averages of the conduction band $E_{C,av}$ and the valance band $E_{V,av}$, and uniaxial strain splits degenerate band edges. The effect of hydrostatic and uniaxial strains on the valance band and conduction band is expressed via deformation potentials. Deformation potentials for hydrostatic strains will be denoted by the symbols a_v^Γ and a_c^Δ for the valance and conduction bands respectively; deformation potentials for uniaxial strains are denoted by b (valance band) and Ξ_u^Δ (conduction band). These deformation potentials have been determined experimentally and theoretically for Si and Ge [256, 257, 323] and are listed in Table 8.2. However, in this work we use the deformation potentials of Si for $Si_{1-x-y}Ge_xC_y$, a valid approximation if the amounts of Ge and C are small, again so that final results are linear with x and y.

The hydrostatic strain, corresponding to the fractional volume change, is given by the trace of the strain tensor: $2\varepsilon_{||} + \varepsilon_\perp$. The positions of $E_{V,av}$ and $E_{C,av}$ shift only when a hydrostatic strain is applied:

$$\Delta E_{V,av}^{strain} = a_v^\Gamma(2\varepsilon_{||} + \varepsilon_\perp) \quad (8.12)$$

$$\Delta E_{C,av}^{strain} = a_c^\Delta(2\varepsilon_{||} + \varepsilon_\perp). \quad (8.13)$$

Since the deformation potentials a_v^Γ and a_c^Δ are positive in our model, $E_{V,av}$ and $E_{C,av}$ will shift up under tensile strain (positive hydrostatic strain), and will shift down under

compressive strain (negative hydrostatic strain), as shown in Fig. 8.4. Note $|\Delta E_{C,av}^{strain}|$ is greater than $|\Delta E_{V,av}^{strain}|$, as a_c^{Δ} is greater than a_v^{Γ}.

The uniaxial strain ($\varepsilon_{\perp} - \varepsilon_{||}$) leads to a splitting of the valance bands (in addition to that due to the spin-orbit interaction), removing the degeneracy of the HH and LH bands. In this special case, the general Hamiltonian matrix (7.31) can be diagnoalized as

$$\begin{bmatrix} |\frac{3}{2},\frac{3}{2}>_{001} & |\frac{3}{2},\frac{1}{2}>_{001} & |\frac{1}{2},\frac{1}{2}>_{001} \\ \frac{\Delta}{3} - \delta E_H - \frac{1}{2}\delta E_{001} & 0 & 0 \\ 0 & \frac{\Delta}{3} - \delta E_H + \frac{1}{2}\delta E_{001} & \frac{\sqrt{2}}{2}\delta E_{001} \\ 0 & \frac{\sqrt{2}}{2}\delta E_{001} & -\frac{2\Delta}{3} - \delta E_H \end{bmatrix}.$$

Thus the splitting of the bands for strained layers of fixed composition (excluding the hydrostatic part) is:

$$E_{V,LH} - E_{V,av} = -\frac{1}{6}\Delta_0 + \frac{1}{4}\delta E_{001} + \frac{1}{2}[\frac{9}{4}(\delta E_{001})^2 + \Delta_0^2 + \delta E_{001}\Delta_0]^{1/2} \tag{8.14}$$

$$E_{V,HH} - E_{V,av} = \frac{1}{3}\Delta_0 - \frac{1}{2}\delta E_{001} \tag{8.15}$$

$$E_{V,SO} - E_{V,av} = -\frac{1}{6}\Delta_0 + \frac{1}{4}\delta E_{001} - \frac{1}{2}[\frac{9}{4}(\delta E_{001})^2 + \Delta_0^2 + \delta E_{001}\Delta_0]^{1/2} \tag{8.16}$$

where $\delta E_{001} = 2b(\varepsilon_{\perp} - \varepsilon_{||})$. We assume that strain has no effect on the spin-orbit splitting, since it is of atomic origin. Note that under compressive strain, the HH band is the uppermost valance band; under tensile strain, the LH band is the uppermost one (Fig. 8.4).

The square-root terms in Eqns. (8.14) and (8.16) for the LH and SO bands give terms which are not linear with carbon and germanium compositions. However, the LH band is relevant for the band edge in tensile strain only. In this case, when $\varepsilon_{||} < 0.5\%$ (corresponding to less than 1.4% C in pure Si as in most of the reported experiments), the term $\frac{\delta E_{001}}{\Delta_0} < 1$. We can linearize Eqns. (8.14) and (8.16) to yield:

$$E_{V,LH} - E_{V,av} \approx \frac{1}{3}\Delta_0 + \frac{1}{2}\delta E_{001} \tag{8.17}$$

$$E_{V,SO} - E_{V,av} \approx -\frac{2}{3}\Delta_0. \tag{8.18}$$

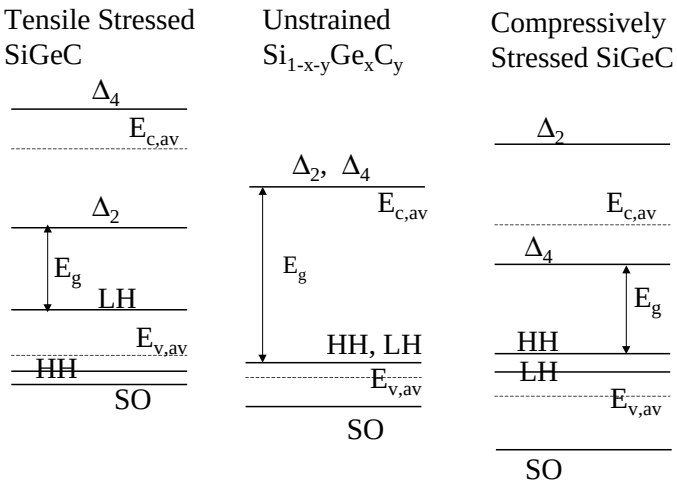


Figure 8.4: Schematic of energy band shift in $Si_{1-x-y}Ge_xC_y$ under compressive and tensile stresses (along [100] and [010] directions) with respect to the unstrained $Si_{1-x-y}Ge_xC_y$. The strain can be expressed by two parts: hydrostatic strain which shifts the weighted averages $E_{V,av}$ and $E_{C,av}$; and uniaxial strain which splits degenerated energy bands.

Under uniaxial strain, the $Si_{1-x-y}Ge_xC_y$ conduction bands will split into the 2-fold degenerate Δ_2 bands (along [001]) and the four-fold degenerate Δ_4 bands (along [010] and [100]). Inserting into Eqns. (7.35-7.37) that $\varepsilon_{xx} = \varepsilon_{yy} = \varepsilon_{||}$ and $\varepsilon_{zz} = \varepsilon_{\perp}$, the shifts of the conduction bands with respect to $E_{C,av}$ are

$$E_{C,\Delta 4} - E_{C,av} = -\frac{1}{3}\Xi_u^{\Delta}(\varepsilon_{\perp} - \varepsilon_{||}), \tag{8.19}$$

$$E_{C,\Delta 2} - E_{C,av} = \frac{2}{3}\Xi_u^{\Delta}(\varepsilon_{\perp} - \varepsilon_{||}). \tag{8.20}$$

Note that the strain-induced conduction band splitting offers the particular advantage that depending on whether the stress is compressive or tensile, different conduction band valleys become lower in energy, allowing one to pick carriers with a particular effective mass (longitudinal or transverse) and a particular direction of transport. Because the uniaxial deformation potential of the conduction band of Si, Ξ_u^{Δ}, is much larger than the hydrostatic deformation potentials, both compressive and tensile stresses lead to smaller band gaps with respect to the unstressed material (Fig. 8.4).

Table 8.2 lists values for all parameters required to evaluate the effects of strain on the conduction band and valance band in $Si_{1-x-y}Ge_xC_y$. Thus for the conduction and valance

bands, the strain effects are:

$$\Delta E_{V,LH}^{strain} \approx \frac{1}{2}\delta E_{001} + a_v^{\Gamma}(2\varepsilon_{||} + \varepsilon_{\perp}) \tag{8.21}$$

$$\Delta E_{V,HH}^{strain} = -\frac{1}{2}\delta E_{001} + a_v^{\Gamma}(2\varepsilon_{||} + \varepsilon_{\perp}) \tag{8.22}$$

$$\Delta E_{V,SO}^{strain} \approx a_v^{\Gamma}(2\varepsilon_{||} + \varepsilon_{\perp}) \tag{8.23}$$

$$\Delta E_{\Delta 4}^{strain} = -\frac{1}{3}\Xi_u^{\Delta}(\varepsilon_{\perp} - \varepsilon_{||}) + a_c^{\Delta}(2\varepsilon_{||} + \varepsilon_{\perp}) \tag{8.24}$$

$$\Delta E_{\Delta 2}^{strain} = \frac{2}{3}\Xi_u^{\Delta}(\varepsilon_{\perp} - \varepsilon_{||}) + a_c^{\Delta}(2\varepsilon_{||} + \varepsilon_{\perp}). \tag{8.25}$$

Using Eqns. (8.9-8.11) to compute the strains, one can then use Eqns. (8.21, 8.22-8.25) to determine all strain effects on the various bands, which are summarized in Table 8.3.

8.5 Commensurate Strained $Si_{1-x-y}Ge_xC_y$ Alloys on Si (001) Substrates

Figure 8.5 combines the intrinsic and strain effects in a single figure, showing what happens to the different band offsets as C or Ge is added to a $Si_{1-x-y}Ge_xC_y$ alloy layer commensurate on a Si (001) substrate, as predicted by the Eqns. (8.12-8.16) and (8.19, 8.20) (without the small-strain approximation). The data is plotted as energy bands vs. composition, as indicated where appropriate on the ordinate axes. First, as Ge is added to Si to form a compressive stressed $Si_{1-x}Ge_x$ layer, the valance band edge (HH) rises and the conduction band edge (Δ_4) is nearly flat, leading to a decreasing band gap, as is well known. Now consider adding C to this layer, shown in the figure as starting from a layer of $Si_{0.8}Ge_{0.2}$ for the purposes of illustration, to form a $Si_{0.8-y}Ge_{0.2}C_y$ alloy. Adding C decreases the compressive stress, and causes little change in the conduction band edge, but lowers the valance band edge from that of SiGe. Thus the band gap is increased compared to a SiGe alloy with the same Ge concentration (as shown).

The present model is compared to experimental results below. Experiments measuring band gaps and band offsets are generally of two types: those where the carbon level is varied systematically with fixed Ge content, so that the effect of carbon may be reported as a slope

Energy bands in $Si_{1-x-y}Ge_xC_y$ (eV)	Intrinsic Effect $E_i^{int.}$ (from Table 8.1)	Strain Effect ΔE_i^{strain}		Total effect E_i^{total}
		in terms of strain $\varepsilon_{\|\|}$	in terms of x,y	
$E_{C,av}$	-5.90+0.337x-4.04y	$5.11\varepsilon_{\|\|}$	-0.207(x-8.3y)	-5.90+0.13x-2.32y
E_{C,Δ_4}	-5.90+0.337x-4.04y	$10.52\varepsilon_{\|\|}$	-0.426(x-8.3y)	-5.90-0.09x-0.50y
E_{C,Δ_2}	-5.90+0.337x-4.04y	$-5.37\varepsilon_{\|\|}$	0.232(x-8.3y)	-5.90+0.57x-5.96y
$E_{V,av}$	-7.03+0.680x-2.20y	$3.01\varepsilon_{\|\|}$	-0.122(x-8.3y)	-7.03+0.56x-1.19y
$E_{V,HH}$	-7.02+0.767x-2.12y	$-1.16\varepsilon_{\|\|}$	0.047(-8.3y)	-7.02+0.81x-2.60y
$E_{V,LH}$	-7.02+0.767x-2.12y	$7.18\varepsilon_{\|\|}^*$	-0.291(x-8.3y)*	-7.02+0.48x+0.205y *
$E_{V,SO}$	-7.06+0.51x-2.17y	$3.01\varepsilon_{\|\|}^*$	-0.122(x-8.3y)*	-7.06+0.39x-1.16y*
E_g(tensile) =E_{C,Δ_2}-$E_{V,LH}$	1.12-0.43x-1.83y	$-12.91\varepsilon_{\|\|}$	0.523(x-8.3y)	1.12+0.093x-6.17y*
E_g(compressive) =E_{C,Δ_4}-$E_{V,HH}$	1.12-0.43x-1.83y	$11.68\varepsilon_{\|\|}$	-0.473(x-8.3y)	1.12-0.90+ 2.13y

* Linear approximation for small strain case.

Table 8.3: Effect of Ge and C incorporation on the band structure of $Si_{1-x-y}Ge_xC_y$/Si(001). For tensile stress, the band gap is determined by $E_{V,LH}$ and E_{C,Δ_2}; for compressive stress, the band gap is determined by $E_{V,HH}$ and E_{C,Δ_4}. ($E_{V,LH}$ and $E_{V,SO}$ are valid under the small strain approximation.)

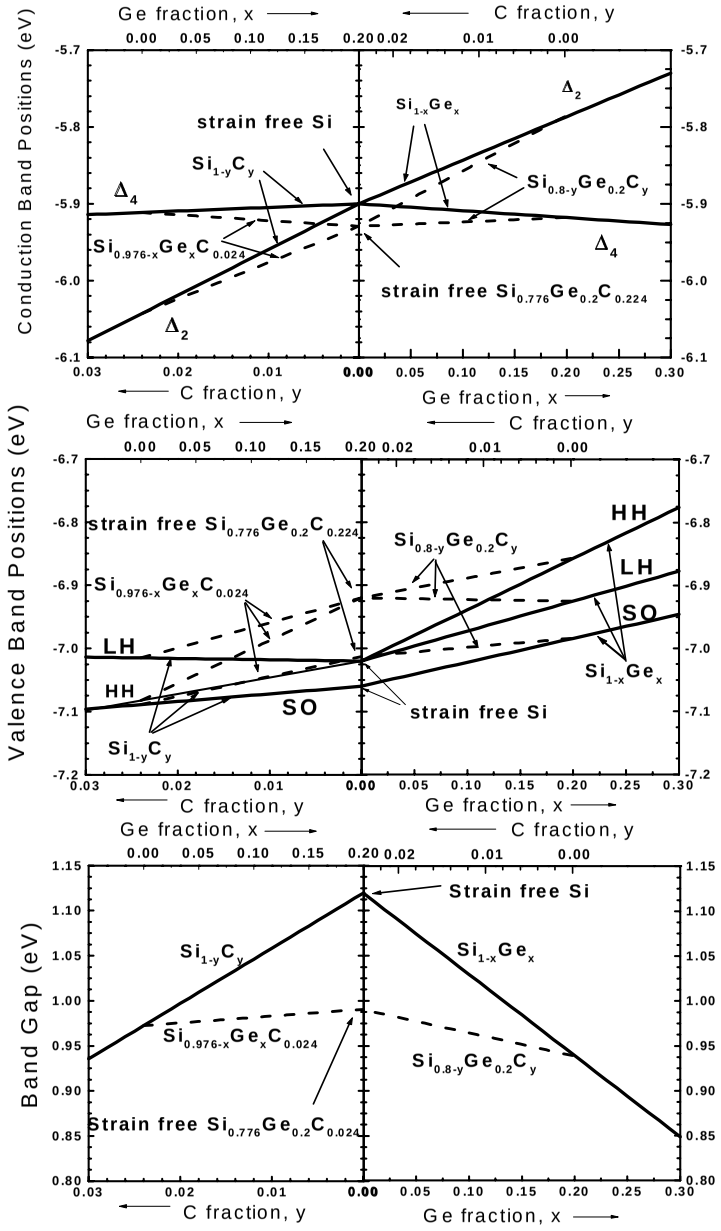


Figure 8.5: Combined intrinsic and strain effects on the conduction band and valance band positions as well as the band gap as a result of adding Ge into tensile-stressed $Si_{0.976}Ge_xC_{0.024}$/Si (001) and C into compressively-stressed $Si_{0.8-y}Ge_{0.2}C_y$/Si(001). Energy bands for tensile-stressed $Si_{1-y}C_y$/Si(001) and compressively-stressed $Si_{1-x}Ge_x$/Si (001) are also plotted.

of meV/% C, and those where the band position of a single $Si_{1-x-y}Ge_xC_y$ sample (i.e. the band offset in a single $Si_{1-x-y}Ge_xC_y$/Si heterojunction) is measured. Although we list both types of experiments in Table 8.4-8.6 for completeness, we discuss only those in which the carbon level was systematically varied. This is because measurements of the band offset of a single sample are prone to error because of uncertainty in the Ge and/or C concentration, inherent difficulties in measuring the absolute level of an offset (vs. a difference in offsets from sample to sample), etc. In Tables 8.4-8.6, we report the data as the difference in valance band position, conduction band position, and band gap in $Si_{1-x-y}Ge_xC_y$ commensurate on Si(100) substrates from those in bulk Si.

For compressive-stressed $Si_{1-x-y}Ge_xC_y$ on Si(100), there are at least three systematic measurements of the band gap vs. carbon level. For the band gap, an increase of 21 meV/%C is predicted by our model, and values from 21-26 meV/%C have been measured by both photoluminescence [297, 298] and temperature dependent transport [299], in good agreement with the model. In contrast, the model of Ref.[315] predicts a slight decrease of band gap as carbon is added in this case. This is due to a different assumption in their model, i.e. that the intrinsic effect of germanium on the conduction band is zero. For the valance band offset, there are at least three systematic studies on carbon concentration by: internal photoemission (-26 ± 1 meV/%C) [314], capacitance-voltage of unipolar diodes (-23 ± 3 meV/%C)[218], and MOS capacitance-voltage measurements [311] (-33 meV/%C found by fitting the data points given in Fig. 6 in the reference). Other isolated points have been measured by X-ray photoelectron spectroscopy [216] and admittance spectroscopy [312]. A decrease of -26 meV/%C is predicted, again in good agreement with experimental observations. For the conduction band position in $Si_{1-x-y}Ge_xC_y$, the model predicts a lowering of -5meV/%C, while there is a single report of -33 ± 22 meV/%C by the indirect method of fitting the admittance of Si/$Si_{1-x-y}Ge_xC_y$/Si Schottky diodes[313]. Metal-oxide-semiconductor capacitance measurements showed that the change in the conduction band offset after adding 1.3%C to $Si_{0.8}Ge_{0.2}$ is negligible to within the experimental error (±30 meV)[310].

On the other side of Fig. 8.5, one can add C to Si to form a tensile-stressed $Si_{1-y}C_y$

Difference of band energy vs. bulk Si ΔE_i		Predicted ΔE_i (eV)	Dependence of ΔE_i on C level	Experimental Data	
				Results	ref.
Compressive -stress	$\Delta E_C = \Delta E_{C,\Delta_4} = E^{SiGeC}_{C,\Delta_4} - E^{Si}_{C,\Delta_4}$	-0.09x -0.50y	-5meV/%C	-33 ±22meV/%C	[313]
			-70meV	$\Delta E_C(Si_{0.82}Ge_{0.17}C_{0.11})$=-100meV (with interstitutional C)	[312]
			-24meV	<abs(-30meV) ($Si_{0.787}Ge_{0.2}C_{0.013}$)	[310]
	$\Delta E_V = \Delta E_{V,HH} = E^{SiGeC}_{V,HH} - E^{Si}_{V,HH}$	0.81x-2.60y	-26meV/%C	-26±1 meV/%C	[314]
				-23±3 meV/%C	[218]
				-33meV/%C	[311]
			156meV	$\Delta E_V(Si_{0.79}Ge_{0.206}C_{0.004})$ =118±12meV	[312]
			290meV	$\Delta E_V(Si_{0.595}Ge_{0.394}C_{0.011})$ =223±20meV	
			143meV	$\Delta E_V(Si_{0.727}Ge_{0.25}C_{0.023})$= 210±30meV	[325]
	$\Delta E_g = E^{SiGeC}_g - E^{Si}_g$	-0.90x+ 2.13y	21meV/%C	ΔE_g=26meV/%C	[299]
				ΔE_g=21meV/%C	[298]
				ΔE_g=23.65meV/%C	[297]
			8.5meV	$E_g(Si_{0.936}Ge_{0.06}C_{0.004})$- $E_g(Si_{0.94}Ge_{0.06})$= 17meV (45 Å quantum well)	[306]

Table 8.4: Comparison of model predictions and reported experimental results for the dependence on carbon level of the difference of valance band position, conduction band position, and band gap in *compressively-stressed* $Si_{1-x-y}Ge_xC_y$ commensurate on Si(100) substrates from those in bulk Si. The second column defines the sign of the given ΔE_i.

Difference of band energy vs. bulk Si ΔE_i		Predicted ΔE_i (eV)	Dependence of ΔE_i on C level	Experimental Data	
				Results	ref.
tensile stress	$\Delta E_C = \Delta E_{C,\Delta_2} = E^{SiGeC}_{C,\Delta_2} - E^{Si}_{C,\Delta_2}$	0.57x-5.96y	-60meV/%C	-65meV/%C($Si_{1-y}C_y$)	[310, 221]
			-48meV	$\Delta E_C(Si_{0.992}C_{0.008})$= -70meV	[311]
			-120meV	$\Delta E_C(Si_{0.98}C_{0.02})$= -150meV(at 4K)	[300]
			-57meV	-55±25meV (admittance) & -48±10meV (C-V) for $Si_{0.9905}C_{0.0095}$	[313]
			-60meV	$\Delta E_C(Si_{0.09}C_{0.01})$= -65meV	[304]
	$\Delta E_V = \Delta E_{V,LH} = E^{SiGeC}_{V,LH} - E^{Si}_{V,LH}$	0.48x+0.205y*	5meV	$\Delta E_V(Si_{0.977}C_{0.023})$ =-10±30meV	[325]
	$\Delta E_g = E^{SiGeC}_g - E^{Si}_g$	0.093x -6.17y*	-62meV/%C	-65meV/%C ($Si_{1-y}C_y$)	[307, 197]
			-31meV/%C	$E_g(Si_{0.99}C_{0.005})$ -E_g(Si)=-38meV	[304]
			-62meV	$E_g(Si_{0.99}C_{0.01})$ -E_g(Si)= -65meV	(52 Å QW) [304]
			-105meV	$E_g(Si_{0.983}C_{0.017})$-E_g(Si) =-122meV	
			-56meV	$E_g(Si_{0.936}Ge_{0.06}C_{0.01})$-$E_g$(Si) =-35meV (45 Å multi-quantum-wells)	[306]

** Valid for small strain case*

Table 8.5: Comparison of model predictions and reported experimental results for the dependence on carbon level of the difference of valance band position, conduction band position, and band gap in *tensile-stained* $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ commensurate on Si(100) substrates from those in bulk Si. The second column defines the sign of the given ΔE_i.

alloy. In this case, the valance band goes up, while the conduction band goes down, and thus the band gap goes down as a $Si_{1-y}C_y$ alloy is formed. Experimentally, the conduction band offset of $Si_{1-y}C_y$/Si (001) has been measured to be -65 meV/%C by MOS capacitance [310, 221], which agrees well with the model prediction of -60 meV/%C. A band gap reduction of -65 meV/%C [307, 197] was also observed from photoluminescence measurement, which agrees with our prediction (-62 meV/%C). The valance band offset between strained $Si_{1-y}C_y$ and the Si substrate is predicted to be very small (5 meV/%C), in agreement with the X-ray photoelectron spectroscopy result of -10 ± 30 meV for 2.3%C [216]. Adding Ge in $Si_{1-y}C_y$ reduces the tensile stress, as plotted on the left side in Fig. 8.5 for $Si_{0.976-x}Ge_xC_{0.024}$. The conduction and valance band edges both rise from that of $Si_{0.976}C_{0.024}$, and the band gap increases slightly. There is no systematic experimental data for tensile-stressed $Si_{1-x-y}Ge_xC_y$, however, photoluminescence from 4.5 nm multi-quantum wells gives a band gap of 35 meV less than Si for a composition of 1%C and 6%Ge [306], while our calculated energy is 56 meV (quantum confinement will cause the experimental value to be smaller).

For a Ge/C ratio of about 8.3, a $Si_{1-x-y}Ge_xC_y$ layer commensurate on Si (001) will be strain-free, with degenerate band edges. Band offsets will be induced solely by the intrinsic effects of Ge and C. This is illustrated in Fig. 8.5 for a composition of $Si_{0.776}Ge_{0.2}C_{0.024}$. Note that a substantial valance band offset (42 meV/%C) and a negligible conduction band offset (-12 meV/%C) is predicted. While the individual band edge positions in such structures have not been measured, there is limited data on the gap of such strain free alloys by photoluminescence. The measured rate of the band gap decrease is -68 meV/%C, while our model predicts a band gap decrease at a rate of -54 meV/%C.

8.6 Summary

The model presented here for prediction of the effect of carbon on band gaps and band alignments has only two independently adjustable parameters ($E_{V,av}^{int.,C}$ and $E_{C,av}^{int.,C}$). The model has been shown to give good agreement with the dependence of the band positions

Difference of band energy vs. bulk Si ΔE_i		Predicted ΔE_i (eV)	Dependence of ΔE_i on C level	Experimental Data	
				Results	ref.
strain-free (x=8.3y)	ΔE_C	-1.23y	-12meV/%C		
	ΔE_V	4.19y	41meV/%C		
	$\Delta E_g = E_g^{SiGeC} - E_g^{Si}$	-5.40y	-54meV/%C	-68meV/%C (87Å quantum wells)	[305]
			-38meV	$E_g(Si_{0.936}Ge_{0.06}C_{0.007})$-$E_g$(Si)= -28meV (45 Å multi-quantum wells)	[306]

Table 8.6: Comparison of model predictions and reported experimental results for the dependence on carbon level of the difference of valance band position, conduction band position, and band gap in *strain fully-compensated* $Si_{1-x-y}Ge_xC_y$ commensurate on Si(100) substrates from those in bulk Si. The second column defines the sign of the given ΔE_i.

on carbon levels measured in at least four different physical cases. This agreement with the many different cases gives confidence that the approach of the model and the chosen parameters reasonably represents the effects of carbon on band positions in $Si_{1-x-y}Ge_xC_y$ alloys which are commensurately strained on Si (001) substrates. For example, it does appear that one can separate the intrinsic effects of Ge and C on the band gap from those induced by the resulting strain. It also appears that the effects are linear with C levels, for C levels on the order of 1%. Further work is needed to incorporate the effects of a deviation in lattice constants from Vegard's law, include deformation potentials and elastic constants which vary with composition, examine layers lattice-matched to other substrates, and to reconcile the few reported experimental conditions which are not consistent with the picture presented in this chapter.

Chapter 9

Summary

By introducing the $Si_{1-x-y}Ge_xC_y$ layers into the structure of a vertical p-channel MOSFET, boron diffusion from the source and drain has been suppressed for the first time. The tradeoff between doped and undoped $Si_{1-x-y}Ge_xC_y$ layers has been studied. It has been found that by using highly doped $Si_{1-x-y}Ge_xC_y$ layers inside the source/drain region, deleterious effects from the alloy or alloy/gate oxide interface can be eliminated. No excess leakage current is introduced by the use of thin SiGeC layers.

Phosphorus doping in Si and SiGe epitaxial layers grown by RTCVD has been studied, using dichlorosilane as a silicon source and phosphine as a phosphorus source. To improve phosphorus doping in silicon epitaxy, the growth is interrupted after n^+ epitaxy and the wafer is subsequently removed from the reactor for the *ex-situ processing*. A 20$\sim$50Å layer is etched away from the silicon surface and a SiGe sacrificial wafer is grown during the interruption. After reloading the device wafer, an 800^oC *in situ* cleaning is performed in hydrogen and then the subsequent layer is grown. An ultra-sharp phosphorus doping profile (13nm/decade) has been achieved for the first time. No oxygen or carbon contamination is observed at the interruption interface.

Vertical p-channel MOSFET's with sub-100nm channel lengths are demonstrated for the first time on the side-walls of a wide mesa, using SiGeC to control the boron doping profile in the source and drain, and using the interrupt-growth technique to improve the phosphorus doping profile in the channel. Devices with 25nm channel lengths have been fabricated. No excess leakage current introduced by either of the two newly developed

technologies was observed. Vertical n-channel MOSFET's of 0.5μm channel lengths have also been fabricated on a wide mesa structure.

Vertical double-gate MOSFET's have been proposed. A selective epitaxy approach would be used to grow the ultra-thin channel and to form self-aligned poly-silicon gates. Key technologies necessary for the fabrication of such a device have been developed.

Calculations have also been performed for the band gap and band alignments for a strained $Si_{1-x-y}Ge_xC_y$ alloy layer on a planar silicon (100) substrate, and a SiGe quantum dot and quantum wire buried in a Si matrix. The band structure of V-grooved SiGe quantum wires have been numerically calculated.

Appendix A

Growth Sequence of Vertical p-channel MOSFET's with L=80nm

The following growth sequence was used to grow a vertical p-channel MOSFET with channel length of 80nm after processing. The structure of this sample is shown in Fig. 5.12c, and its I-V and subthreshold characteristics are shown in Fig. 5.17. 20nm heavily doped $Si_{0.796}Ge_{0.2}C_{0.004}$ layers were used to suppress boron diffusion from the source/drain into the channel region during gate oxidation. The interrupt-growth technique was used to achieve ultra-sharp phosphorus doping profiles in the channel. Dopant profiles after all high temperature processing are shown in Fig. 5.16. The entire sequence is divided into three parts. First the bottom p^+ Si and n-type channel were grown. Then sample was removed from the reactor to etch away a thin layer of the silicon surface. Finally the sample was reloaded, and the channel and top p^+ Si layers were grown.

Bottom contact and n-type channel

Sequencer Table #0← ··· initializing the system

Step #	Action	Comment
0	Control On&	Turn on Control
1	Scan On(0.3)	and Scan simultaneously
2	SET(SP7,0)&	override power to zero
3	SET(SP4,0)&	turn off PID control
4	SET(SP0,0.6)	zero loop control
5	SET(DO0,1)&	N_2 off
6	SET(DO1,0)&	H_2 off
7	SET(DO2,0)&	GeH_4 select valve off
8	SET(DO3,0)&	SiH_4 select valve off
9	SET(DO4,0)&	B_2H_6 select valve off
10	SET(DO5,0)&	PH_3 select valve off
11	SET(DO6,0)&	HCl select valve off
12	SET(DO7,0)&	DCS select off
13	SET(DO8,0)	$SiCH_6$ select off
14	SET(DO9,0)&	GeH_4 inject off
15	SET(DO10,0)&	SiH_4 inject off
16	SET(DO11,0)&	B_2H_6 inject off
17	SET(DO12,0)&	PH_3 inject off
18	SET(DO13,0)	DCS inject off
19	SET(AO0,0.21)	H_2 MFC 1lpm
20	SET(DO15,1)	open vacuum valve
21	SET(DO1,1)&	inject H_2
22	SET(AO1,0)&	set GeH_4 MFC=0
23	SET(AO2,0)&	set SiH_4 MFC=0
24	SET(AO3,0)&	set B_2H_6 MFC=0
25	SET(AO4,0)&	set PH_3 High MFC=0
26	SET(AO5,0)&	set PH_3 Low MFC=0
27	SET(AO6,0)&	set DCS MFC=0
28	SET(AO7,0)	set $SiCH_6$ MFC=0
29	SET(AO8,0)	set pressure=0
30	SEQUENCER ON(0.3,1,0)	call sequencer #1

Sequencer Table #1 ← ···main program

Step #	Action	Comment
1	SET(SP2,0)&	
2	SEQUENCER ON(0.3,6,0)	call sequencer #6
3	WAITUNTIL(SP2>0.5)	
4	SET(SP2,0)&	
5	SEQUENCER ON(0.3,5,0)	call sequencer #5
6	WAITUNITL(SP2>0.5)	
7	SET(SP5, 4.304)	set T=750C
8	SET(SP4,1.0)	set loop control
9	SET(SP2,0)&	
10	SEQUENCER ON(0.3,4,0)	call sequencer #4
11	WAITUNTIL(SP2>0.5)	
12	SET(SP2,0)	
13	SET(SP4,0)&	
14	RAMPL(SP7, -0.4, 0)	turn off lamp
15	SEQUENCER ON(0.3, 7, 0)	call sequencer #7

Sequencer Table #6

Step #	Action	Comment
1	WAITUNTIL(AI24>0.5)	press GO for high pressure
2	SET(AO11,0)&	set high P select
3	SET(AO8,0.250)&	set P=250torr
4	SET(AO0,0.817)&	set H_2=4lpm
5	WAITUNTIL(AI29>250)	wait for P stable
6	SET(AO3,0.2)	B_2H_6=100sccm
7	SET(DO4,1)	B_2H_6 select on
8	SET(AO6, 0.534)	DCS=26sccm
9	SET(DO7, 1)	DCS select on
10	RAMP(SP7, 0.4, 0.30)	ramp to 30% lamp power
11	WAIT(120)	bake 2min
12	SET(AO8,0.18)	
13	WAIT(10)	
14	SET(AO8,0.1)	
15	WAIT(10)	
16	SET(AO8,0)&	pump out
17	SET(AO0, 0.617)&	
18	SET(AO5, 0.7)&	
19	SET(DO5,1)&	
20	SET(SP2,1)	

Sequencer Table #5

Step #	Action	Comment
1	WAITUNTIL(AI29<10)	
2	WAITUNTIL(AI24>0.5)	press GO for buffer layer
3	SET(AO11,1)&	select low P
4	WAITUNTIL(AI28<5.5)	pump out
5	SET(AO8,0.6)&	set P=6torr
6	WAITUNTIL(AI28>5.5)	wait P stable
7	SET(DO11,1)&	inject B_2H_6
8	SET(DO13,1)	inject DCS
9	WAIT(600)	10min
10	SET(DO13,0)&	
11	SET(DO11,0)	
12	RAMP(SP7, -0.4,0)	cool down
13	SET(AO1,0.214)	GeH_4=100sccm
14	SET(DO2,1)	select GeH_4
15	WAITUNTIL(AI24>0.5)	press Go for cold value
16	SET(SP3,1)	
17	WAIT(1)	take cold value
18	SET(SP3,0)	
19	RAMP(SP7, 0.4, 0.23)	reheat sample
20	WAIT(20)	
21	SET(SP2,1.0)	

Sequencer Table #4

Step #	Action	Comment
1	SET(DO13,1)&	inject DCS
2	SET(DO11,1)	inject B_2H_6
3	WAIT(300)	5min
4	SET(AO3,0.025)	change B_2H_6=12.5sccm
5	WAIT(300)	5min
6	SET(SP5,3.56)	set T=700C
7	WAIT(30)	
8	SET(SP5, 2.952)	set T=625C
9	WAIT(30)	
10	SET(DO13,0)	
11	WAIT(10)	
12	SET(DO13,1)&	
13	SET(DO9,1)	
14	WAIT(150)	SiGeC layer 20nm
15	SET(DO9,0)	
16	WAIT(30)	
17	SET(SP5, 3.56)	set T=700C
18	WAIT(200)	
19	SET(DO11,0)	B_2H_6 off
20	WAIT(560)	
21	SET(SP5, 2.952)	set T=625C
22	WAIT(30)	
23	SET(DO12,1)	inject PH_3
24	WAIT(1200)	20min
25	SET(SP5,3.56)	set T=700C
26	WAIT(1000)	n-type channel
27	SET(DO12,0)&	
28	SET(DO13,0)	
29	SET(SP2,1.0)	

Sequencer Table #7 ← ·shut off system

Step #	Action	Comment
1	SET(SP7,0)	set lamp off
2	SET(DO13,0)&	DCS inject off
3	SET(DO12,0)&	PH_3 inject off
4	SET(DO11,0)&	B_2H_6 inject off
5	SET(DO10,0)&	SiH_4 inject off
6	SET(DO9,0)&	GeH_4 inject off
7	SET(DO7,0)&	DCS select off
8	SET(DO5,0)&	PH_3 select off
9	SET(DO4,0)&	B_2H_6 select off
10	SET(DO3,0)&	SiH_4 select off
11	SET(DO2,0)&	GeH_4 select off
12	SET(DO1,0)	H_2 off
13	SET(AO8,0)	pressure=0
14	SET(AO7,0)&	$SiCH_6$ MFC=0
15	SET(AO6,0)&	DCS MFC=0
16	SET(AO5,0)&	PH_3 low MFC=0
17	SET(AO4,0)&	PH_3 high MFC=0
18	SET(AO3,0)&	B_2H_6 MFC=0
19	SET(AO2,0)&	SiH_4 MFC=0
20	SET(AO1,0)&	GeH_4 MFC=0
21	SET(AO0,0)	H_2 MFC=0
22	WAITUNTIL(AI28<0.5)	pump out
23	SET(DO15,0)	vacuum valve off
24	SEQUENCER OFF(0)	
25	SEQUENCER OFF(1)	
26	SEQUENCER OFF(2)	
27	SEQUENCER OFF(3)	
28	SEQUENCER OFF(4)	
29	SEQUENCER OFF(5)	
30	SEQUENCER OFF(6)	

Channel and top contact

Sequencer #0 and #7 are the same as the previous program

Sequencer Table #1 ← ·main program

Step #	Action	Comment
1	SET(SP2,0)&	
2	SEQUENCER ON(0.3,6,0)	call sequencer #6
3	WAITUNTIL(SP2>0.5)	
4	SET(SP2,0)&	
5	SEQUENCER ON(0.3,5,0)	call sequencer #5
6	WAITUNTIL(SP2>0.5)	
7	SET(SP2,0)	
8	SEQUENCER ON(0.3,4,0)	call sequener #4
9	WAITUNTIL(SP2>0.5)	
10	SET(SP2,0)	
11	SET(SP4,0)&	
12	RAMP(SP7,-0.4,0)	ramp lamp down
13	SEQUENCER ON (0.3,7,0)	

Sequencer Table #6

Step #	Action	Comment
1	SET(AO0,0.1)	H_2 MFC=0.5lpm
2	SET(DO1,1)	H_2 on
3	SET(AO1,0.214)	GeH_4=100sccm
4	SET(DO2,1)	select GeH_4
5	SET(AO6,0.534)	DCS=26sccm
6	SET(DO7,1)	select DCS
7	SET(AO3,0.2)	B_2H_6 MFC=100sccm
8	SET(DO4,1)	select B_2H_6
9	WAITUNTIL(AI24>0.5)	press Go for cold value
10	SET(SP3,1)	
11	WAIT(1)	take cold value
12	SET(SP3,0)	
13	SET(AO0,0.618)	H_2 MFC=3lpm
14	RAMP(SP7,0.4,0.23)	heat up
15	WAIT(30)	
16	SET(AO3,0.025)	B_2H_6 MFC=12sccm
17	SET(SP2,1)	

Sequencer Table #5

Step #	Action	Comment
1	WAITUNTIL(AI24>0.5)	press GO for low P
2	SET(AO11,1)&	Low P select
3	SET(AO8,1)&	P=10torr
4	SET(SP5,5.569)	T=800C
5	SET(SP4,1)	
6	WAIT(60)	bake for 1min
7	SET(SP5, 3.56)	T=700C
8	SET(AO8,0.6)	P=6torr
9	SET(DO13,1)	inject DCS
10	WAIT(30)	
11	SET(SP5,2.952)	T=625C
12	WAIT(1200)	20min
13	SET(SP5,3.56)	T=700C
14	WAIT(1200)	20min
15	SET(DO11,1)	inject B_2H_6
16	WAIT(200)	
17	SET(SP5,2.952)	T=625C
18	WAIT(30)	
19	SET(DO13,0)	
20	WAIT(10)	
21	SET(DO13,1)&	
22	SET(DO9,1)&	
23	WAIT(150)	SiGeC 20nm
24	SET(DO9,0)	
25	WAIT(30)	
26	SET(SP5,3.56)	T=700C
27	WAIT(30)	
28	SET(SP2,1.0)	

Sequencer Table #4

Step #	Action	Comment
1	SET(SP5,4.304)	T=750C
2	WAIT(300)	
3	SET(AO3,0.2)	B_2H_6 MFC=100sccm
4	WAIT(1020)	
5	SET(DO13,0)&	
6	SET(DO11,0)	
7	SET(SP2,1)	

Appendix B

Growth Sequence of p^+ Polysilicon Gate for Vertical p-channel MOSFET's

The following sequence was used to grow p^+ polysilicon gates for vertical p-channel MOSFET's presented in this thesis. The experiments were performed on the RTCVD system at Princeton. The growth temperature was 700^oC and pressure was 6Torr. 100sccm SiH_4 (diluted to 10% in Ar) was used as the silicon source. The B_2H_6 (diluted to 126ppm in H_2) flow rate was 450sccm. 3slpm H_2 was used as carrier gas. Growth rate is about 200nm/30min. The same sequence can be used for n^+ polysilicon. Note that for 450sccm PH_3 (diluted to 70ppm in H_2), the growth rate is about 200nm/50min.

Sequencer #0 and #7 are the same as the previous program

Sequencer Table #1← ···main program

Step #	Action	Comment
1	SET(SP2,0)&	
2	SEQUENCER ON(0.3,6,0)	call sequencer #6
3	WAITUNTIL(SP2>0.5)	
4	SET(SP2,0)&	
5	SEQUENCER ON(0.3,5,0)	call sequencer #5
6	WAITUNITL(SP2>0.5)	
7	SET(SP5, 3.56)	set T=700C
8	SET(SP4,1.0)	set loop control
9	WAIT(60)	
10	SET(SP2,0)&	
11	SEQUENCER ON(0.3,4,0)	call sequencer #4
12	WAITUNTIL(SP2>0.5)	
13	SET(SP2,0)	
14	SET(SP4,0)&	
15	RAMPL(SP7, -0.4, 0)	turn off lamp
16	SEQUENCER ON(0.3, 7, 0)	call sequencer #7

Sequencer Table #5

Step #	Action	Comment
1	WAITUNTIL(AI29<10)	
2	WAITUNTIL(AI24>0.5)	press GO for buffer layer
3	SET(AO11,1)&	select low P
4	WAITUNTIL(AI28<5.5)	pump out
5	SET(AO8,0.6)&	set P=6torr
6	WAITUNTIL(AI28>5.5)	wait P stable
7	RAMP(SP7, 0.4, 0.23)	reheat sample
8	WAIT(40)	
9	RAMP(SP7,0.4,0.19)	
10	WAIT(10)	
11	SET(SP2,1.0)	

Sequencer Table #6

Step #	Action	Comment
1	WAITUNTIL(AI24>0.5)	press Go for cold value
2	SET(SP3,1)	
3	WAIT(1)	take cold value
4	SET(SP3,0)	
5	SET(AO0, 0.817)	H_2 MFC=4lpm
6	SET(AO3,0.2)	
7	SET(AO2,0.214)	
8	SET(DO3,1)	
9	SET(DO4,1)	
10	WAITUNTIL(AI24>0.5)	
11	SET(AO11,0) &	
12	SET(AO8,0.250)	
13	WAITUNTIL(AI29>250)	
14	WAIT(60)	
15	SET(AO8, 0.2)	
16	WAIT(10)	
17	SET(AO8,0.15)	
18	WAIT(10)	
19	SET(AO8,0.10)	
20	WAIT(10)	
21	SET(AO8,0.05)	
22	WAIT(10)	
23	SET(AO8,0)&	
24	SET(AO0,0.617)&	H_2 MFC=3lpm
25	SET(SP2,1)	

Sequencer Table #4

Step #	Action	Comment
1	SET(DO10,1)&	inject SiH_4
2	SET(DO11,1)	inject B_2H_6
3	WAIT(1800)	30min
4	SET(DO10,0)	
5	SET(DO11,0)	
6	SET(SP2,1)	

Appendix C

Publications and Presentations Resulting from This Thesis

JOURNAL PUBLICATIONS

1. M. Yang, M. Carroll, and J. C. Sturm, "Extremely sharp phosphorus doping profiles in silicon epitaxy by rapid thermal chemical vapor deposition", J. Electrochem. Soc. (to be published).

2. M. Yang, and J. C. Sturm, "Doped vs. undoped SiGeC layers in sub-100nm vertical p-channel MOSFET's", Thin Solid Films (to be published).

3. M. Yang, C.-L. Chang, and J. C. Sturm, "The effect of carbon on band alignments and band gaps in Si1-x-yGexCy/Si (001) structures" in "SiGeC alloys and their applications", edited by S. Zollner and S. T. Pantelides (to be published).

4. M. Yang, and J. C. Sturm, "SiGeC source and drain in Sub-100nm vertical p-channel MOSFET's", submitted to IEEE Transactions on Electronic Devices, 1999.

5. M. Yang, C.-L. Chang, M. Carroll, and J. Sturm, "25nm p-channel vertical MOSFET's with SiGeC sources/drains", IEEE Electron Device Letters 20, 301 (1999).

6. M. Yang, J. C. Sturm, and J. Prevost, "Calculation of band alignments and quantum confinement effects in zero- and one-dimensional pseudomorphic structures". Phys.

Rev. B 56, 1973 (1997).

CONFERENCE PAPERS

1. J. C. Sturm, M. S. Carroll, M. Yang, E. Stewart, and J. Gray "Mechanisms and applications of the control of dopant profiles in silicon using SiGeC layers grown by RTCVD", to be presented at the 197th Electrochemical Society Meeting, Toronto, May 2000.

2. M. Yang, and J. C. Sturm, "Doped vs. undoped SiGeC layers in sub-100nm vertical p-channel MOSFET's", International Joint Conference on Silicon Epitaxy and Heterostructures, Miyagi, Japan, September, 1999.

3. (Invited) J. C. Sturm, M. Yang, and M. Carroll, "Doped and undoped SiGeC layers for dopant profile control in sub-100nm vertical MOSFET's", Silicon Nanoelectronics Workshop, June 12-13, 1999, Kyoto, Japan.

4. M. Carroll, M. Yang, and J. C. Sturm, "Suppressed phosphorus auto-doping in silicon epitaxy for ultra-sharp phosphorus profiles by low temperature rapid thermal chemical vapor deposition", 195th Electrochemical Society Meeting, Seattle, Washington, May 1999.

5. M. Yang, C.-L. Chang, M. Carroll, and J. Sturm, "40nm p-channel vertical MOSFET's with SiGeC sources/drains", Device Research Conference, Virginia, 1998.

6. (Invited) J. C. Sturm, M. Yang, M. Carroll, and C.-L. Chang, "SiGeC alloys: an enabling technology for scaled high performance silicon-based heterojunction devices", IEEE MTT-S: Silicon Monolithic Integrated Circuits in RF Systems Symposium, Michigan, 1998.

7. (Invited) J. C. Sturm, M. Yang, C.-L. Chang, and M. S. Carroll, "Novel applications of rapid thermal chemical vapor deposition for nanoscale MOSFET's". Materials Research Society Spring Symposium, San Francisco, 1998.

8. M. Yang, J. C Sturm, and J. Prevost, "Strain-field effects on band gap and band alignment in pseudomorphic zero- and one-dimensional structures", Electronic Materials Conference, Santa Barbara, 1996.

Bibliography

[1] N. Kistler and J. Woo, *IEDM Tech. Dig.*, p. 727, 1993.

[2] T. J. King, J. R. Pfiester, and K.Saraswat, *IEEE Electro Device Lett.*, vol. 12, p. 533, 1993.

[3] W. C. Lee, T. J. King, and C. Hu, *Symp. VLSI Tech. Dig.*, p. 190, 1998.

[4] K. Ismail, J. O. Chu, K. L. Saenger, and B. S. Meyerson, *Appl. Phys. Lett.*, vol. 65, p. 1248, 1994.

[5] K. Ismail, J. O. Chu, and B. S. Meyerson, *Appl. Phys. Lett.*, vol. 64, p. 3124, 1994.

[6] K. Ismail, *IEDM Tech. Dig.*, p. 509, 1995.

[7] G. A. Sai-Halasz, M. R. Wordeman, D. P. Kern, E. Ganin, S. Rishton, D. S. Zicherman, H. Schmid, M. R. Polcari, H. Y. Ng, P. J. Restle, T. H. P. Chang, and R. H. Dennard, *IEEE Electron Device Lett.*, vol. 8, no. 10, p. 463, Oct. 1987.

[8] G. Timp, A. Agarwal, K. K. Bourdelle, J. E. Bower, T. Boone, A. Ghetti, M. Green, J. Garno, H. Gossmann, D. Jacobson, R. Kleiman, A. Kornblit, F. Klemens, S. Moccio, M. O'Malley, L. Ocola, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, W. Timp, and D. Tennet, *IEDM Tech. Dig.*, p. 1041, 1998.

[9] G. Timp, A. Agarwal, F. H. Baumann, T. Boone, M. Buonanno, R. Cirelli, V. Donnelly, M. Foad, D. Grant, M. Green, H. Gossmann, S. Hillenius, J. Jackson, D. Jacobson, R. Kleiman, A. Kornblit, F. Klemens, J. T. C. Lee, W. Mansfield, S. Moccio,

A. Murrell, M. O'Malley, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, W. W. Tai, D. Tennant, H. Vuong, and B. Weir, *IEDM Tech. Dig.*, p. 930, 1997.

[10] A. Hori, H. Nakaoka, H. Umimoto, K. Yamashita, M. Takase, N. Shimizu, B. Mizuno, and S. Odanaka, *IEDM Tech. Dig.*, p. 485, 1994.

[11] H. Kawaura, T. Sakamoto, T. Baba, Y. Ochiai, J. Fujita, S. Matsui, and J. Sone, *IEEE Electron Device Lett.*, vol. 19, no. 3, p. 74, Mar. 1998.

[12] M. Rodder, M. Hanratty, D. Rogers, T. Laaksonen, J. C. Hu, S. M. adn C. P. Chao, S. Hattangady, S. Aur, A. Amerasekera, and I. C. Chen, *IEDM Tech. Dig.*, p. 223, 1997.

[13] M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, T. O. H. S. Momose, and H. Iwai, *J. Vac. Sci. Technol. B*, vol. 13, no. 4, p. 1740, Jul/Aug. 1995.

[14] Y. Taur, S. Cohen, S. Wind, T. Lii, C. Hsu, D. Quinlan, C. Chang, D. Buchanan, P. Agnello, Y. Mii, C. Reeves, A. Acovic, and V. Kesan, *IEDM Tech. Dig.*, p. 901, 1992.

[15] Y. Mii, S. Rishton, Y. Taur, D. Kern, T. Lii, K. Lee, K. A. Jenkins, D. Quinlan, T. B. Jr., D. Danner, F. Sewell, and M. Polcari, *IEEE Electron Device Lett.*, vol. 15, no. 1, p. 28, Jan. 1994.

[16] C. Hu, *Semiconductor International*, p. 105, Jun. 1994.

[17] S. I. A. (SIA), "International technology roadmap for semiconductors," 1998.

[18] M. Kakumu, *IEDM Short Course*, 1997.

[19] R. Yan, A. Ourmazd, and K. F. Lee, *IEEE Tran. Electron Devices*, vol. 39, p. 1704, 1992.

[20] C. Fiegna, H. Iwai, T. Wada, M. Saito, E. Sangiorgi, and b. Riccó, *IEEE Trans. Electron Devices*, vol. 41, no. 6, p. 941, Jun. 1994.

[21] S. Kohyama, *Symposium on VLSI Tech. Dig.*, p. 5, 1994.

[22] Y. Taur, Y. J. Mii, D. J. Frank, H. S. Wong, D. A. Buchanan, S. J. Wind, S. A. Rishton, G. A. Sai-Halasz, and E. J. Nowak, *IBM J. Res. Develop.*, vol. 39, no. 1/2, p. 245, Jan./Mar. 1995.

[23] P. K. Chatterjee and R. R. Doering, *Symposium on VLSI Tech. Dig.*, p. 53, 1995.

[24] Y. Taur, D. A. Duchanan, W. Chen, D. J. Frank, K. E. Ismail, S. H. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H. J. C. Wann, S. J. Wind, and H. S. Wong, *Proceedings of the IEEE*, vol. 85, no. 4, p. 486, Apr. 1997.

[25] H. S. P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wann, and J. J. Welser, *Proceedings of the IEEE*, vol. 87, no. 4, p. 537, Apr. 1999.

[26] S. Tiwari, P. M. Solomon, J. J. Welser, E. C. Jones, F. R. McFeely, and E. Cartier, *Mircoelectronic Engineering*, vol. 46, p. 3, 1999.

[27] R. R. Troutman, *IEEE J. Solid-State Circuits*, vol. 14, no. 2, p. 383, Apr. 1979.

[28] M. Yoshimi, H. Hazama, M. Takahashi, S. K. T. Wada, K. Kato, and H. Tango, *IEEE Trans. Electron Devices*, vol. 36, no. 3, p. 493, Mar. 1989.

[29] P. Richman, *MOSFET's and Integrated Circuits.* New York: Wiley, 1973.

[30] R. R. Troutman, *J. Solid-State Circuits*, vol. SC-9, p. 55, Apr. 1974.

[31] D. Burnett and S. W. Sun, *Proc. SPIE*, vol. 2636, p. 83, 1995.

[32] H. S. Wong, Y. Taur, and D. Frank, *Microelectronic Reliability*, vol. 38, no. 9, p. 1447, 1998.

[33] B. Hoeneisen and C. A. Mead, *Solid State Electron.*, vol. 15, p. 819, 1972.

[34] R. W. Keyes, *IEEE J. Solid-State Circuits*, vol. SC-10, p. 245, 1975.

[35] H. S. Wong and Y. Taur, *IEDM Tech. Dig.*, p. 705, 1993.

[36] T. Mizuno, J. Okamura, and A. Toriumi, *1993 IEEE symposium on VLSI Technology Digest of Technical Papers*, p. 41, 1993.

[37] V. De, X. Tang, and J. Meindl, *Proc. VLSI Symp.*, p. 198, 1996.

[38] F. H. Gaensslen, V. L. Rideout, E. J. Walker, and J. J. Walker, *IEEE Trans. Electron Devices*, vol. ED-24, p. 218, 1977.

[39] J. Y. C. Sun, Y. Taur, R. H. Dennard, and S. P. Klepner, *IEEE Trans. Electron Devices*, vol. ED-34, p. 19, 1987.

[40] Y. Taur, S. Cohen, S. Wind, T. Lii, C. Hsu, D. Quinlan, C. Chang, D. Buchanan, P. Agnello, Y. Mii, C. Reeves, A. Acovic, and V. Kesan, *IEEE Electron Device Lett.*, vol. 14, p. 304, 1993.

[41] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu, *IEDM Tech. Dig.*, p. 809, 1994.

[42] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Boker, P. K. Ko, and C. Hu, *IEEE Trans. Electron Devices*, vol. 44, no. 3, p. 414, Dec. 1994.

[43] D. J. Frank, S. E. Laux, and M. V. Fischetti, *IEDM Tech. Dig.*, p. 553, 1992.

[44] C. Fiegna, H. Iwai, T. Wada, T. Saito, E. Sangiorgi, and B. Riccò, *Symp. VLSI Tech.*, p. 33, 1993.

[45] T. Sekigawa and Y. Hayashi, *Solid-State Electronics*, vol. 27, no. 8, p. 827, 1984.

[46] H. S. P. Wong, D. J. Frank, and P. M. Solomon, *IEDM Tech. Dig.*, p. 407, 1998.

[47] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, *IEEE Trans. Electron Devices*, vol. 40, no. 12, p. 2326, Dec. 1993.

[48] P. Francis, A. Terao, d. Flandre, and F. V. de Walle, *IEEE Trans. Electron Devices*, vol. 41, no. 5, p. 715, May 1994.

[49] Y. Tosaka and K. Suzuki, *IEEE Electron Device Lett.*, vol. 15, no. 11, p. 466, Nov. 1994.

[50] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, Y. Arimoto, and T. Itoh, *Solid-State Electronics*, vol. 37, no. 2, p. 327, 1994.

[51] B. Majkusiak, T. Janik, and J. Walczak, *IEEE Trans. Electron Devices*, vol. 45, no. 5, p. 1127, May 1998.

[52] S. S. Chen and J. B. Kuo, *IEEE Trans. Electron Devices*, vol. 43, no. 9, p. 1387, Sep 1996.

[53] L. Wei, Z. Chen, and K. Roy, *Proceedings 1998 IEEE International SOI conference*, p. 69, 1998.

[54] T. M. Associates, *TMA Medici: Two-Dimensional Device Simulator Program*, 1996.

[55] J. M. Hwang and G. Pollack, *IEDM Tech. Dig.*, p. 345, 1992.

[56] H. S. P. Wong, K. K. Chan, and Y. Taur, *IEDM Tech. Dig.*, p. 427, 1997.

[57] T. Tanaka, K. Suzuki, H. Horie, and T. Sugii, *Symp. VLSI Tech. Dig.*, p. 11, 1994.

[58] T. Tanaka, H. Horie, S. Ando, and S. Hijiya, *IEDM Tech. Dig.*, p. 683, 1991.

[59] J. P. Denton and G. W. Neudeck, *IEEE Electron Device Lett.*, vol. 17, no. 11, p. 509, 1996.

[60] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, *IEEE Electron Device Lett.*, vol. 8, no. 9, p. 410, Sep. 1987.

[61] J. P. Colinge, M. H. Gao, A. Romano-Rodríguez, H. Maes, and C. Claeys, *IEDM Tech. Dig.*, p. 595, 1990.

[62] E. Leobandung, J. Gu, L. Guo, and S. Y. Chou, *J. Vac. Sci. Technol. B*, vol. 15, no. 6, p. 2791, 1997.

[63] D. Hisamoto, T. Kaga, and E. Takeda, *IEEE Trans. Electron Devices*, vol. 38, no. 6, p. 1419, Jun. 1991.

[64] H. S. Wong, D. J. Frank, Y. Taur, and J. M. C. Stork, *IEDM Tech. Dig.*, p. 747, 1994.

[65] H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, F. Horiguchi, and F. Masuoka, *IEEE Trans. Electron Devices*, vol. 38, p. 573, Mar. 1991.

[66] W. F. Richardson, D. M. Bordelon, G. P. Pollack, A. H. Shah, S. D. S. Malhi, H. Shichijo, S. K. Banerjee, M. Elahy, R. H. Womack, C. P. Wang, J. Gallia, H. E. Davis, and P. K. Chatterjee, *IEDM Tech. Dig.*, p. 714, 1985.

[67] K. Sunouchi, H. Takato, N. Okabe, T. Yamada, T. Ozaki, S. Inoue, K. Hashimoto, K. Hieda, A. Nitayama, F. Horiguchi, and F. Masuoka, *IEDM Tech. Dig.*, p. 23, 1989.

[68] A. Nitayama, H. Takato, N. Okabe, K. Sunouchi, K. Hieda, F. Horiguchi, and F. Masuoka, *IEEE Trans. Electron Devices*, vol. 38, no. 3, p. 579, Mar. 1991.

[69] B. Goebel, E. Bertagnolli, and F. Koch, *IEDM Tech. Dig.*, p. 939, 1998.

[70] K. Liu, S. Ray, S. Oswal, and S. Banerjee, *IEEE Electron Device Letter*, vol. 19, p. 13, 1998.

[71] X. Zheng, M. Pak, J. Huang, S. Choi, and K. L. Wang, in *Proceeding of 56th Device Research Conference*, (Charlottesville, Virginia), p. 70, 1998.

[72] C. Auth and J. Plummer, in *Proceeding of 54th Device Research Conference*, (Santa Barbara, California), p. 108, 1996.

[73] W. Kiunke, E. Hammerl, and I. Eisele, *J. Crystal Growth*, vol. 127, p. 73, 1993.

[74] H. Gossner, I. Eisele, and L. Risch, *Jpn. J. Appl. Phys.*, vol. 33, p. 2423, 1994.

[75] H. Gossner, F. Wittmann, I. Eisele, T. Grabolla, and D. Behammer, *Electronics Lett.*, vol. 31, no. 16, p. 1394, Aug. 1995.

[76] A. Strass, *Solid State Technology*, p. 65, Jan. 1996.

[77] L. Risch, W. Krautschneider, F. Hofmann, H. Schafer, T. Aeugle, and W. Ronser, *IEEE Trans. Electron Devices*, vol. 43, p. 1495, Sep. 1996.

[78] V. R. Rao, F. Wittmann, H. Gossner, and I. Eisele, *IEEE Trans. Electron Devices*, vol. 43, p. 973, Jun. 1996.

[79] D. Behammer, L. Vescan, R. Loo, J. Moers, A. Mück, H. Lüth, and T. Grabolla, *Electronics Letters*, vol. 32, p. 406, 1996.

[80] K. D. Meyer, M. Caymax, N. Collaert, R. Loo, and P. Verheyen, *Thin Solid Films*, vol. 336, p. 299, 1998.

[81] K. C. Liu, X. Wang, E. Quinones, X. Chen, X. D. Chen, D. Kencke, B. Anantharam, S. K. Ray, S. K. Oswal, and S. K. Banerjee, in *Proceedings of 57th Device Research Conference*, (Santa Barbara, CA), p. 180, 1999.

[82] W. Hansch, V. R. Rao, C. Fink, F. Kaesen, and I. Eisele, *Thin Solid Films*, vol. 206, p. 206, 1998.

[83] F. Kaesen, C. Fink, K. G. Anil, W. Hansch, T. Doll, T. Grabolla, H. Schreiber, and I. Eisele, *Thin Solid Films*, vol. 336, p. 309, 1998.

[84] D. Behammer, M. Zeuner, T. Hackbarth, J. Herzog, M. Schafer, and T. Grabolla, *Thin Solid Films*, vol. 336, p. 313, 1998.

[85] P. Verheyen, N. Collaert, M. Caymax, R. Loo, K. D. Meyer, and M. V. Rossum, in *Proceedings of Nanoelectronics Workshop*, (Kyoto, Japan), 1999.

[86] J. M. Hergenrother, D. P. Monroe, F. P. Klemens, A. Kornblit, G. R. Weber, W. M. Mansfield, M. R. Baker, F. H. Baumann, K. J. Bolan, J. E. Bower, N. A. Ciampa, R. A. Cirelli, J. I. Colonell, D. J. Eaglesham, J. Frackoviak, H. J. Gossmann, M. L. Green, S. J. Hillenius, C. A. King, R. N. Kleiman, W. Y. C. Lai, J. T. C. Lee, R. C.

Liu, H. L. Maynard, M. D. Morris, C. S. Pai, C. S. Rafferty, J. M. Rosamilia, T. W. Sorsch, and H. H. Vuong, *IEDM Tech. Dig.*, p. to be published, 1999.

[87] C. Auth and J. Plummer, *IEEE Electron Device Letters*, vol. 18, p. 74, Feb. 1997.

[88] C. P. Auth and J. D. Plummer, *IEEE Trans. Electron Devices*, vol. 45, no. 11, p. 2381, Nov. 1998.

[89] S. Maeda, S. Maegawa, T. Ipposhi, H. Nishimura, H. Kuriyama, O. Tanina, Y. Inoue, T. Nishimura, and N. Tsubouchi, *IEEE Trans. Electron Devices*, vol. 42, no. 12, p. 2117, Dec. 1995.

[90] S. Watanabe, K. Tsuchida, D. Takashima, Y. Oowaki, A. Nitayama, K. Hieda, H. Takato, K. Sunouchi, F. Horiguchi, F. M. K. Ohuchi, and H. Hara, *IEEE J. Solid-State Circuits*, vol. 30, no. 9, p. 960, 1995.

[91] T. Inaba, D. Takashima, Y. Oowaki, T. Ozaki, S. Watanabe, and K. Ohuchi, *Symp. VLSI Circuits Tech. Dig.*, p. 99, 1995.

[92] S. Maeda, S. Maegawa, T. Ipposhi, H. Nishimura, H. Kuriyama, O. Tanina, Y. Inoue, T. Nishimura, and N. Tsubouchi, *Symposium on VLSI Tech. Dig.*, p. 133, 1994.

[93] H. Nakano, D. Takashima, K. Tsuchida, S. Shiratake, T. Inaba, M. Ohta, Y. Oowaki, S. Watanabe, K. Ohuchi, and J. Matsunaga, *IEEE Symp. VLSI Circuits Tech. Dig.*, p. 190, 1996.

[94] H. J. Cho, F. Nemati, P. B. Griffin, and J. D. Plummer, *Symposium on VLSI Tech. Dig.*, p. 38, 1998.

[95] J. J. Welser, A. Kumar, T. Furukawa, T. S. Kanarsky, S. J. Holmes, D. V. Horak, N. King, A. Knorr, P. C. Jamison, U. Gruening, C. Radens, J. A. Mandelman, G. B. Bronner, S. Tiwari, and M. Hakey, in *57th Device Research Conference*, (Santa Barbara, CA), 1999.

[96] U. Gruening, C. J. Radens, J. A. Mandelman, A. Michaelis, M. Seitz, N. Arnold, D. Lea, D. Casarotto, A. Knorr, S. Halle, T. H. Ivers, L. Economikos, S. Kudelka, S. Rahn, H. Tews, H. Lee, R. Divakaruni, J. J. Welser, T. Furukawa, T. S. Kanarsky, J. Alsmeier, and G. B. Bronner, *IEDM Tech. Digest*, p. 25, 1999.

[97] E. Bertagnolli, F. Hofmann, J. Willer, R. Maly, F. Lau, P. W. V. Basse, M. Bollu, R. Thewes, U. Kollmer, U. Zimmermann, M. Hain, W. H. Krautschneider, A. Rusch, B. Hasler, A. Kohlhase, and H. Klose, *Symposium on VLSI Tech. Dig.*, p. 58, 1996.

[98] H. Pein and J. D. Plummer, *IEEE Electron Device Lett.*, vol. 14, no. 8, p. 415, Aug. 1993.

[99] H. I. Hanafi, S. Tiwari, S. Burns, W. Kocon, A. Thomas, N. Garg, and K. Matsushita, *IEDM Tech. Dig.*, p. 657, 1995.

[100] H. B. Pein and J. D. Plummer, *IEDM Tech. Dig.*, p. 11, 1993.

[101] D. S. Kuo, M. Simpson, L. Tsou, and S. Mukherjee, *Symposium on VLSI Tech. Dig.*, p. 51, 1994.

[102] T. Endoh, K. Shinmei, H. Sakuraba, and F. Masuoka, *IEIC Trans. Electron.*, vol. E81-C, no. 9, p. 1491, Sep. 1998.

[103] T. Endoh, K. Shinmei, H. Sakuraba, and F. Masuoka, *IEEE J. of Soild-State Circuits*, vol. 34, no. 4, p. 476, Apr. 1999.

[104] F. Nemati and J. D. Plummer, *Symposium on VLSI Tech. Dig.*, p. 66, 1998.

[105] R. Zingg and B. Höfflinger, *IEDM Tech. Dig.*, p. 909, 1989.

[106] J. Moers, D. Klaes, A. Tönnesmann, L. Vescan, S. Wickenhäuser, M. Marso, P. Kordoš, and H. Lüth, *Electronics Lett.*, vol. 35, no. 3, p. 239, Feb 1999.

[107] F. C. Eversteyn and B. H. Put, *J. Electrochem. Soc.*, vol. 120, p. 106, 1973.

[108] B. Ricco, R. Versari, and D. Esseni, *IEEE Electron Device Letters*, vol. 17, p. 103, 1996.

[109] K. Pangal, S. Firebaugh, and J. C. Sturm, *Appl. Phys. Lett.*, vol. 69, p. 1471, 1996.

[110] S. Fang and J. P. McVittie, *IEEE Electron Device Lett.*, vol. 13, no. 5, p. 288, 1992.

[111] C. T. Gabriel and J. P. McVittie, *Solid State Technol.*, vol. 35, p. 81, June 1992.

[112] H. C. Shin and C. Hu, *Semicond. Sci. Technol.*, vol. 11, p. 463, 1996.

[113] C. T. Gabriel, *J. Vac. Sci. Technol. B*, vol. 9, p. 370, 1991.

[114] K. Arita and T. Asano, *Jpn. J. Appl. Phys.*, vol. 35, p. 6534, 1996.

[115] J. C. King and C. Hu, *IEEE Electron Device Lett.*, vol. 15, no. 11, p. 475, 1994.

[116] J. Li and J. W. McConkey, *J. Vac. Sci. Technol. A*, vol. 14, no. 4, p. 2102, 1996.

[117] K. Lai, K. Kumar, A. Chou, and J. C. Lee, *IEDM Tech. Dig.*, p. 319, 1995.

[118] D. D. Lee, J. H. Kim, K. S. Shin, H. S. Park, and S. H. Choi, *J. Vac. Sci. Technol. B*, vol. 13, no. 2, p. 396, 1995.

[119] V. M. Donnelly, *Plasma Diagnostics, Discharge Parameters and Chemistry.* New York: Academic, 1989. edited by O. Auciello and D. L. Flamm.

[120] H. H. Busta, R. E. Lajos, and D. A. Keiwit, *Solid State Technol.*, vol. 22, p. 61, 1979.

[121] T. R. Hayes, P. A. Heimann, V. M. Donnelly, and K. E. Strege, *Appl. Phys. Lett.*, vol. 57, p. 2817, 1990.

[122] R. Braunstein, A. R. Moore, and F. Herman, *Phys. Rev.*, vol. 109, no. 3, p. 695, Feb. 1958.

[123] V. A. Yunkin, I. W. Rangelow, J. A. Schaefer, D. Fischer, E. Voges, and S. Sloboshanin, *Microelectronic Engineering*, vol. 23, p. 361, 1994.

[124] J. C. Sturm, P. V. Schwartz, E. J. Prinz, and H. Manoharan, *J. Vac. Sci. Technol. B*, vol. 9, p. 2011, 1991.

[125] J. C. Sturm, P. V. Schwartz, and P. M. Garone, *Appl. Phys. Lett.*, vol. 56, p. 961, 1990.

[126] T. M. Associates, "TMA Tsuprem-4: Two-dimensional process simulation program," 1993.

[127] E. A. Irene, H. Z. Massoud, and E. Tierney, *J. Electrochem. Soc.*, vol. 133, p. 1253, 1986.

[128] S. Theise. private communication.

[129] V. S. Ban and S. L. Gilbert, *J. Electrochem. Soc.*, vol. 122, p. 1382, 1975.

[130] W. A. P. Claassen and J. Bloem, *J. Cryst. Growth*, vol. 50, p. 807, 1980.

[131] J. T. Fitch, *J. Electrochem. Soc.*, vol. 141, no. 4, p. 1046, Apr. 1994.

[132] M. R. Goulding, *Materials Science and Engineering*, vol. B17, p. 47, 1993.

[133] C. G. Tuppen, C. J. Gibbings, and M. Hockly, *J. Crystal Growth*, vol. 94, p. 392, 1989.

[134] R. A. H. Heinecke, *Solid State Electron.*, vol. 18, p. 1146, 1975.

[135] H. W. Lehmann and R. Widmer, *Appl. Phys. Lett.*, vol. 32, no. 3, p. 163, 1978.

[136] L. M. Ephrath, *J. Electrochem. Soc.*, vol. 126, no. 8, p. 1419, 1979.

[137] G. S. Oehrlein and H. L. Williams, *J. Appl. Phys.*, vol. 62, no. 2, p. 662, July 1987.

[138] K. Maruyama, K. Ohkouchi, and T. Goto, *Jpn. J. Appl. Phys.*, vol. 35, Pt.1, no. 7, p. 4088, 1996.

[139] P. Studenkov. private communication.

[140] J. Moers, D. Klaes, A. Tönnesmann, L. Vescan, S. Wickenhäuser, T. Grabolla, M. Marso, P. Kordoš, and H. Lüth, *Solid-State Electronics*, vol. 43, p. 529, 1999.

[141] D. Klaes, J. Moers, A. Tönnesmann, S. Wickenhäuser, L. Vescan, M. Marso, T. Graboll, M. Grimm, and H. Lüth, *Thin Solid Films*, vol. 332, p. 1, 1998.

[142] B. S. Meyerson, F. K. LeGoues, T. N. Nguyen, and D. L. Harame, *Appl. Phys. Lett.*, vol. 50, p. 113, 1987.

[143] P. J. Roksnoer, J. W. F. M. Maes, A. T. Vink, C. J. Vriezema, and P. C. Zalm, *Appl. Phys. Lett.*, vol. 58, p. 711, Feb. 1991.

[144] D. W. Greve, *Materials Science and Engineering*, vol. B18, p. 22, 1993.

[145] B. S. Meyerson and M. L. Yu, *J. Electrochem. Soc.*, vol. 131, p. 2366, 1984.

[146] D. W. Greve and M. Racanelli, *J. Electrochem. Soc.*, vol. 138, p. 1744, 1991.

[147] L. D. Madsen and L. Weaver, *J. Electrochem. Soc.*, vol. 137, p. 2246, 1990.

[148] H. Kurokawa, *J. Electrochem. Soc.*, vol. 129, p. 2620, 1982.

[149] J. H. Comfort and R. Reif, *J. Appl. Phys.*, vol. 65, p. 1053, 1989.

[150] A. J. Learn and D. W. Foster, *J. Appl. Phys.*, vol. 61, p. 1898, 1987.

[151] W. Ahmed and D. B. Meakin, *J. Cryst. Growth*, vol. 79, p. 394, 1986.

[152] L. P. Chen, G. W. Huang, and C. Y. Chang, *Appl. Phys. Lett.*, vol. 68, p. 1498, 1996.

[153] T. O. Sedgwick, P. D. Agnello, D. N. Ngoc, T. S. Kuan, and G. Scilla, *Appl. Phys. Lett.*, vol. 58, p. 1896, 1991.

[154] P. D. Agnello, T. O. Sedgwick, M. S. Goorsky, and J. Cotte, *Appl. Phys. Lett.*, vol. 60, p. 454, 1992.

[155] T. Y. Hsieh, H. G. Chun, and D. L. Kwong, *Appl. Phys. Lett.*, vol. 55, p. 2408, 1989.

[156] Y. Ohshita and H. Kitajima, *J. Appl. Phys.*, vol. 70, p. 1871, 1991.

[157] T. I. Kamins and D. Lefforge, *J. Electrochem. Soc.*, vol. 144, no. 2, p. 674, 1997.

[158] A. C. Churchill, D. J. Robbins, D. J. Wallis, N. Griffin, D. J. Paul, and A. J. Pidduck, *Semicond. Sci. Technol.*, vol. 12, p. 943, 1997.

[159] B. Tillack, D. Krüger, P. Gaworzewski, and G. Ritter, *Thin Solid Films*, vol. 294, p. 15, 1997.

[160] K. Ismail, S. Rishton, J. O. Chu, K. Chan, and B. S. Meyerson, *IEEE Electron Device Lett.*, vol. 14, p. 348, 1993.

[161] J. O. Chu, K. Ismail, and S. Koester, *40th Electronic Materials Conference, Virginia*, 1998.

[162] B. S. Meyerson and W. Olbricht, *J. Electrochem. Soc.*, vol. 131, p. 2361, 1984.

[163] J. A. del Alamo and R. M. Swanson, *J. Electrochem. Soc.*, vol. 132, no. 12, p. 3011, 1985.

[164] S. M. Jang, K. Liao, and R. Reif, *Appl. Phys. Lett.*, vol. 63, p. 1675, 1993.

[165] A. Baudrant and M. Sacalotti, *J. Electrochem. Soc.*, vol. 129, p. 1109, 1982.

[166] M. L. Hitchman and W. Ahmed, *Vacuum*, vol. 34, p. 979, 1984.

[167] R. F. C. Farrow, *J. Electrochem. Soc.*, vol. 121, p. 899, 1974.

[168] C. A. Chang, *J. Electrochem. Soc.*, vol. 123, p. 1245, 1976.

[169] R. Malik, E. Gulari, P. Bhattacharya, K. K. Linder, and J. S. Rieh, *Appl. Phys. Lett.*, vol. 70, no. 9, p. 1149, Mar. 1997.

[170] N. Maity, L. Q. Xia, and J. R. Engstrom, *Appl. Phys. Lett.*, vol. 66, p. 1909, 1995.

[171] M. L. Yu, D. J. Vitkavage, and B. S. Meyerson, *J. Appl. Phys.*, vol. 59, p. 4032, 1986.

[172] Y. Wang, X. Chen, and R. J. Hamers, *Phys. Rev. B*, vol. 50, no. 7, p. 4534, 1994.

[173] J. Bloem, *J. Cryst. Growth*, vol. 31, p. 256, 1975.

[174] J. Bloem, L. J. Giling, and M. W. M. Graef, *J. Electrochem. Soc.*, vol. 121, no. 10, p. 1354, 1974.

[175] R. Reif, *J. Electrochem. Soc.*, vol. 129, no. 8, p. 1122, 1982.

[176] P. M. Garone, J. C. Sturm, P. V. Schwartz, S. A. Schwarz, and B. J. Wilkens, *Appl. Phys. Lett.*, vol. 56, p. 1275, 1990.

[177] R. Bashir, A. E. Kabir, and P. Westrom, *Appl. Phys. Lett.*, vol. 75, no. 6, p. 796, 1999.

[178] K. Ismail, J. O. Chu, K. L. Saenger, and B. S. Meyerson, *Appl. Phys. Lett.*, vol. 65, p. 1248, 1994.

[179] M. Carroll, M. Yang, and J. C. Sturm, *195th Electrochemical Society Meeting, Seattle Washington*, p. 523, May 1999.

[180] M. Yang, C. Chang, M. Carroll, and J. C. Sturm, *IEEE Electronic Device Letters*, vol. 20, p. 301, 1999.

[181] L. Lanzerotti, *Carbon in $Si_{1-x}Ge_x$ Heterojunction Bipolar Transistors.* Ph.d thesis, Princeton University, 1998.

[182] P. J. Drevinsky, C. E. Caefer, S. P. Tobin, J. C. Mikkelsen, and L. C. Kimerling, *Mater. Res. Soc. Symp. Proc.*, vol. 104, p. 167, 1988.

[183] P. M. Fahey, P. B. Griffin, and J. D. Plummer, *Rev. Mod. Phys.*, vol. 61, p. 289, 1989.

[184] N. E. B. Cowern, A. Cacciato, J. S. Custer, F. W. Saris, and W. Vandervorst, *Appl. Phys. Lett.*, vol. 68, p. 1150, 1996.

[185] J. M. Poate, D. J. Eaglesham, G. H. Gilmer, H. J. Gossman, M. Jaraiz, C. S. Rafferty, and P. A. Stolk, *IEDM Tech. Dig.*, p. 77, 1995.

[186] P. A. Stolk, D. J. Eaglesham, H. J. Gossmann, and J. M. Poate, *Appl. Phys. Lett.*, vol. 66, p. 1370, 1995.

[187] G. Davies, K. T. Kun, and T. Reade, *Phys. Rev. B*, vol. 44, no. 22, p. 12146, 1991.

[188] H. Rücker, B. Heinemann, W. Ropke, R. Kurps, D. Krüger, G. Lippert, and H. J. Osten, *Appl. Phys. Lett.*, vol. 73, p. 1682, 1998.

[189] M. S. Carroll, C. L. Chang, and J. C. Sturm, *Appl. Phys. Lett.*, vol. 73, p. 3695, 1998.

[190] P. A. Stolk, H. J. Gossmann, D. J. Eaglesham, D. C. Jacobson, C. S. Rafferty, G. H. Gilmer, M. Jaraíz, and J. M. Poate, *J. Appl. Phys.*, vol. 81, no. 9, p. 6031, 1997.

[191] L. Lanzerotti, J. Sturm, E. Stach, R. Hull, T. Buyuklimanli, and C. Magee, *Appl. Phys. Lett.*, vol. 70, p. 3125, 1997.

[192] M. Carroll, L. Lanzerotti, and J. C. Sturm, *Mat. Res. Soc. Symp. Proc.*, vol. 527, p. 417, 1998.

[193] P. Kuo, J. Hoyt, J. Gibbons, J. Turner, R. Jacowitz, and T. Kamins, *Appl. Phys. Lett.*, vol. 62, p. 612, 1993.

[194] O. Madelung, *Semiconductors: Group IV elements and III-V compounds.* Berlin, Heidelberg: Springer-Verlag, 1991.

[195] J. W. Strane, H. J. Stein, S. R. Lee, S. T. Picraux, J. K. Watanabe, and J. W. Mayer, *J. Appl. Phys.*, vol. 76, p. 3656, 1994.

[196] G. Davies and R. C. Newman, *Handbook on Semiconductors*, vol. 3. New York: Elsevier Science, 1994.

[197] K. Brunner, K. Eberl, and W. Winter, *Phys. Rev. Lett.*, vol. 76, p. 303, 1996.

[198] T. O. Mitchell, J. L. Hoyt, and J. F. Gibbons, *Appl. Phys. Lett.*, vol. 71, p. 1688, 1997.

[199] J. Mi, P. Warren, P. Letourneau, M. Judelewicz, M. Galihanou, M. Dutoit, C. Dubois, and J. C. Dupuy, *Appl. Phys. Lett.*, vol. 67, p. 259, 1995.

[200] P. C. Kelires and J. Tersoff, *Phys. Rev. Lett.*, vol. 63, p. 1164, 1989.

[201] H. J. Osten, *Mat. Sci. Eng. B*, vol. 36, p. 268, 1996.

[202] H. J. Osten, M. Kim, K. Pressel, and P. Zaumseil, *J. Appl. Phys.*, vol. 80, p. 6711, 1996.

[203] C. L. Chang, *Ph.D thesis, Princeton University*, 1998. unpublished.

[204] C. W. Liu, A. S. Amour, J. C. Sturm, Y. R. J. Lacroix, M. L. W. Thewalt, C. W. Magee, and D. Eaglesham, *J. Appl. Phys.*, vol. 80, p. 3043, 1996.

[205] C. L. Chang, A. S. Amour, and J. C. Sturm, *IEDM Tech. Dig.*, p. 257, 1996.

[206] F. S. Johnson, D. S. Miles, D. T. Grider, and J. J. Wortman, *J. Electronic Materials*, vol. 21, p. 805, 1992.

[207] F. K. LeGoues, R. Rosenberg, T. Nguyen, and B. S. Meyerson, *Mater. Res. Soc. Symp. Proc.*, vol. 105, p. 313, 1988.

[208] S. S. Iyer, P. M. Solomon, V. P. Kesan, A. A. Bright, J. L. Freeouf, T. N. Nguyen, and A. C. Warren, *IEEE Electron Device Letters*, vol. 12, p. 246, 1991.

[209] S. S. Jain and P. Balk, *Thin Solid films*, vol. 223, p. 348, 1993.

[210] J. Xiang, N. Herbots, H. Jacobsson, P. Ye, S. Hearne, and S. Whaley, *IEEE Tran. Electron Devices*, vol. 39, p. 1704, 1992.

[211] Z. Atzmon, A. E. Bair, T. L. Alford, D. Chandrasekhar, D. J. Smith, and J. W. Mayer, *Appl. Phys. Lett.*, vol. 66, p. 2244, 1995.

[212] H. J. Osten, B. Heinemann, D. Knoll, G. Lippert, and H. Rücker, *J. Vac. Sci. Technol. B*, vol. 16, p. 1750, 1998.

[213] I. Ban, M. Öztürk, and E. Demirlioglu, *IEEE Trans. Electron Devices*, vol. 44, p. 1544, 1997.

[214] H. J. Gossmann, C. S. Rafferty, G. Hobler, H. H. Vuong, D. C. Jacobson, and M. Frei, *IEDM Tech. Dig.*, p. 725, 1998.

[215] K. Pressel, G. G. Fischer, P. Zaumseil, M. Kim, and H. J. Osten, *Thin Solid Films*, vol. 294, p. 133, 1997.

[216] H. J. Osten, G. Lippert, P. Gaworzewski, and R. Sorge, *Appl. Phys. Lett.*, vol. 71, p. 1522, 1997.

[217] C. L. Chang, S. P. Shukla, W. Pan, V. Venkataraman, J. C. Sturm, and M. Shayegan, *Thin Solid Films*, vol. 321, p. 51, 1998.

[218] C. L. Chang, A. S. Amour, and J. C. Sturm, *Appl. Phys. Lett.*, vol. 70, p. 1557, 1997.

[219] A. Nishiyama, O. Arisumi, and M. Yoshimi, *IEEE Trans. Electron Devices*, vol. 44, p. 2187, Dec. 1997.

[220] P. A. Stolk, H.-J. Gossmann, D. J. Eaglesham, and J. M. Poate, *Materials Science and Engineering*, vol. B36, p. 275, 1996.

[221] K. Rim, T. O. Mitchell, D. V. Singh, J. L. Hoyt, and J. F. Gibbons, *Appl. Phys. Lett.*, vol. 72, p. 2286, 1998.

[222] K. Pressel, M. Franz, D. Krüger, H. J. Osten, B. Garrido, and J. R. Morante, *J. Vac. Sci. Technol. B*, vol. 16, p. 1757, 1998.

[223] A. Ural, P. B. Griffin, and J. D. Plummer, *Appl. Phys. Lett.*, vol. 73, no. 12, p. 1706, 1998.

[224] J. P. Colinge, *IEEE Trans. Electron Devices*, vol. ED-34, p. 845, 1987.

[225] J. R. Davis, A. E. Glaccum, K. Reeson, and P. L. F. Hemment, *IEEE Electron Device Lett.*, vol. EDL-7, p. 570, 1986.

[226] J. G. Fossum, R. Sundaresan, and M. Matloubian, *IEEE Electron Device Lett.*, vol. 8, no. 11, p. 544, Nov. 1987.

[227] T. Mizuno, A. Toriumi, M. Iwase, M. Takahashi, H. Niiyama, M. Fukumoto, and M. Yoshimi, *IEDM Tech. Dig.*, p. 695, 1992.

[228] J. Y. Choi and J. G. Fossum, *IEEE Trans. Electron Devices*, vol. 38, p. 1384, Jun. 1991.

[229] W. Chen, Y. Taur, D. Sadana, K. A. Jenkins, J. Sun, and S. Cohen, *Symp. VLSI Tech. Dig.*, p. 92, 1996.

[230] E. P. V. Ploeg, T. Watanabe, N. A. Kistler, J. C. S. Woo, and J. D. Plummer, *IEDM Tech. Dig.*, p. 337, 1992.

[231] T. Ohno, M. Takahashi, Y. Kado, and T. Tsuchiya, *IEEE Trans. Electron Devices*, vol. 45, no. 5, p. 1071, May 1998.

[232] A. C. Ipri, G. M. Dolny, D. P. Vu, and M. W. Batty, *Proc. 1992 IEEE Int. SOI Conf.*, p. 34, 1992.

[233] M. Horiuchi and M. Tamura, *IEEE Tran. Electron Devices*, vol. 45, no. 5, p. 1077, May 1998.

[234] T. Eimori, T. Oashi, H. Kimura, Y. Yamaguchi, T. Iwamatsu, T. Tsurada, K. Suma, H. Hidaka, Y. Inoue, T. Nishimura, S. Satoh, and H. Miyoshi, *IEDM Tech. Dig.*, p. 45, 1993.

[235] M. Yoshimi, M. Terauchi, A. Murakoshi, M. Takahashi, K. Matsuzawa, N. Shigyo, and Y. Ushiku, *IEDM Tech. Dig.*, p. 429, 1994.

[236] R. Koh and H. Matsumoto, *Jpn. J. Appl. Phys.*, vol. 36, Part 1, no. 3B, p. 1563, Mar. 1997.

[237] M. Yoshimi, M. Terauchi, A. Nishiyama, O. Arisumi, A. Murakoshi, K. Matsuzawa, N. Shigyo, S. Takeno, M. Tomita, K. Suzuki, Y. Ushiku, and H. Tango, *IEEE Trans. Electron Devices*, vol. 44, p. 423, Mar. 1997.

[238] M. Terauchi, M. Yoshimi, A. Murakoshi, and Y. Ushiku, *Symp. VLSI Tech. Dig.*, p. 35, 1995.

[239] J. H. Sim, C. H. Choi, and K. Kim, *IEEE Trans. Electron Devices*, vol. 42, p. 1495, 1995.

[240] P. Schittenhelm, M. Gail, J. Brunner, J. Nützel, and G. Abstreiter, *Appl. Phys. Lett.*, vol. 67, p. 1292, 1995.

[241] H. Sunamura, S. Fukatsu, and Y. Shiraki, *J. Cryst. Growth*, vol. 150, p. 1038, 1995.

[242] J. Tersoff, C. Teichert, and M. G. Lagally, *Phys. Rev. Lett.*, vol. 76, p. 1675, 1996.

[243] Y. H. Xie, S. B. Samavedam, M. Bulsara, T. A. Langdo, and E. A. Fitzgerald, *Appl. Phys. Lett.*, vol. 71, no. 24, p. 3567, 1997.

[244] M. Goryll, L. Vescan, K. Schmidt, S. Mesters, H. Lüth, and K. Szot, *Appl. Phys. Lett.*, vol. 71, no. 3, p. 410, 1997.

[245] D. J. Eaglesham and M. Cerullo, *Phys. Rev. Lett.*, vol. 64, no. 16, p. 1943, 1990.

[246] P. Boucaud, V. L. Thanh, S. Sauvage, D. Débarre, and D. Bouchier, *Appl. Phys. Lett.*, vol. 74, no. 3, p. 401, 1999.

[247] J. L. Liu, W. G. Wu, A. Balandin, G. Jin, Y. H. Luo, S. G. Thomas, Y. Lu, and K. L. Wang, *Appl. Phys. Lett.*, vol. 75, no. 12, p. 1745, 1999.

[248] O. G. Schmidt, C. Lange, K. Eberl, O. Kienzle, and F. Ernst, *Appl. Phys. Lett.*, vol. 71, p. 2340, 1997.

[249] D. Leonard, M. Krishnamurthy, C. Reaves, S. Denbaars, and P. Petroff, *Appl. Phys. Lett.*, vol. 63, p. 3203, 1993.

[250] J.-Y. Marzin, J.-M. Gérard, A. Izraël, D. Barrier, and G. Bastard, *Phys. Rev. Lett.*, vol. 73, p. 716, 1994.

[251] M. Grundmann, O. Stier, and D. Bimberg, *Phys. Rev. B*, vol. 52, p. 11969, 1995.

[252] M. Grundmann, O. Stier, and D. Bimberg, *Phys. Rev. B*, vol. 50, p. 14187, 1994.

[253] E. Kapon, D. M. Hwang, and R. Bhat, *Phys. Rev. Lett.*, vol. 63, p. 430, 1989.

[254] A. Wankerl, A. T. Schremer, and J. R. Shealy, *Appl. Phys. Lett.*, vol. 72, no. 25, p. 3332, 1998.

[255] I. Mukhametzhanov, Z. Wei, R. Heitz, and A. Madhukar, *Appl. Phys. Lett.*, vol. 75, no. 1, p. 85, 1999.

[256] C. G. V. de Walle and R. M. Martin, *Phys. Rev. B*, vol. 34, p. 5621, 1986.

[257] C. G. V. de Walle, *Phys. Rev. B*, vol. 39, p. 1871, 1989.

[258] F. H. Pollak and M. Cardona, *Phys. Rev.*, vol. 172, p. 816, 1968.

[259] J. Eshelby, *J. Appl. Phys.*, vol. 25, p. 255, 1954.

[260] J. Eshelby, *Solid State Physics*, vol. 3, p. 79, 1956.

[261] S. Timoshenko and J. Goodier, *Theory of Elasticity.* New York: McGraw-Hill, 1970.

[262] G. E. Picus and G. L. Bir, *Soviet Phys. –Solid State*, vol. 1, p. 136, 1959.

[263] G. E. Picus and G. L. Bir, *Soviet Phys. –Solid State*, vol. 1, p. 1502, 1960.

[264] G. E. Picus, *Soviet Phys. –Solid State*, vol. 6, p. 261, 1964.

[265] G. E. Picus and Z. Eksperim, *Soviet Phys. –JETP*, vol. 14, p. 1075, 1962.

[266] G. L. Bir and G. E. Pikus, *Symmetry and Strain-Induced Effects in Semiconductors.* John Wiley & Sons, 1974.

[267] H. Hasegawa, *Phys. Rev.*, vol. 129, p. 1029, 1963.

[268] J. C. Hensel and G. Feher, *Phys. Rev.*, vol. 129, no. 3, p. 1041, Feb. 1963.

[269] C. Herring and E. Vogt, *Phys. Rev.*, vol. 101, p. 944, 1956.

[270] I. Balslev, *Phys. Rev.*, vol. 143, p. 636, 1966.

[271] J. Weber and M. I. Alonso, *Phys. Rev. B*, vol. 40, p. 5683, 1989.

[272] D. C. Houghton, G.C.Aers, S.-R. Yang, E.Wang, and N.L.Rowell, *Phys. Rev. Lett.*, vol. 75, p. 866, 1995.

[273] J. J. Wortman and R. A. Evans, *J. Appl. Phys.*, vol. 36, no. 1, p. 153, Jan. 1965.

[274] W. P. Mason, *Physical Acoustics and the Properties of Solids*. Princeton, New Jersey: D. Van Nostrand Company, Inc., 1958.

[275] J. H. Prevost, "Dynaflow: a nonlinear transient finite element analysis program," tech. rep., Dept of Civil Eng. and Op. Research, Princeton University, 1981. last update 1996.

[276] A. Hartmann, L. Vescan, C. Dieker, and H. Lüth, *J. Appl. Phys.*, vol. 77, p. 1959, 1995.

[277] N. Usami, T. Mine, S. Fukatsu, and Y. Shiraki, *Appl. Phys. Lett.*, vol. 64, p. 1126, 1994.

[278] T. Gosling and J. Willis, *J. Appl. Phys.*, vol. 77, p. 5601, 1995.

[279] D. Faux, J. Downes, and E. O'Reilly, *J. Appl. Phys.*, vol. 80, p. 2515, 1996.

[280] G. Z. Xu, M. Yang, and P. Jiang, *J. Appl. Phys.*, vol. 74, no. 11, p. 6747, Dec. 1993.

[281] F. C. Frank and J. V. der Merwe, in *Proc. R. Soc. A*, vol. 198, p. 216, 1949.

[282] G. C. Osbourn, *J. Appl. Phys.*, vol. 53, p. 1586, 1982.

[283] R. People, *IEEE J. Quantum Electron*, vol. 22, p. 1696, 1986.

[284] F. Schäffler, *Properties of strained and relaxed SiGe*, p. 135. London: INSPEC, E. Kasper (ed.) ed., 1995.

[285] T. L. Lin and J. Maserjian, *Appl. Phys. Lett.*, vol. 57, no. 14, p. 1422, 1990.

[286] J. S. Park, T. L. Lin, E. W. Jones, H. M. D. Castillo, and S. D. Gunapala, *Appl. Phys. Lett.*, vol. 64, no. 18, p. 2370, May 1994.

[287] R. P. G. Karunasiri, J. S. Park, and K. L. Wang, *Appl. Phys. Lett.*, vol. 61, no. 20, p. 2434, 1992.

[288] J. Matthews and A. Blakeslee, *J. Crystal Growth*, vol. 27, p. 118, 1974.

[289] R. People, J. C. Bean, D. V. Lang, A. M. Sergent, H. L. Störmer, K. W. Wecht, R. T. Lynch, and K. Baldwin, *Appl. Phys. Lett.*, vol. 45, p. 1231, 1984.

[290] R. People, J. C. Bean, and D. V. Lang, *J. Vac. Sci. Technol. A*, vol. 3, p. 846, 1985.

[291] R. People and J. C. Bean, *Appl. Phys. Lett.*, vol. 48, no. 8, p. 538, Feb. 1986.

[292] J. B. Posthill, R. A. Rudder, S. V. Hattangaddy, C. G. Fountain, and R. J. Markunas, *Appl. Phys. Lett.*, vol. 56, p. 734, 1990.

[293] S. S. Iyer, K. Eberl, F. K. LeGoues, J. C. Tsang, and F. Cardone, *Appl. Phys. Lett.*, vol. 60, p. 356, 1992.

[294] K. Eberl, S. S. Iyer, S. Zollner, J. C. Tsang, and F. K. LeGoues, *Appl. Phys. Lett.*, vol. 60, p. 3033, 1992.

[295] M. Hiroi, K. Miyanaga, and T. Tatsumi, *Ext. Abs. 1993 Conf. Solid State Dev. Mater. (Japan Society of Applied Physics, Makuhari)*, p. 934, 1993.

[296] J. L. Regolini, F. Gisbert, G. Dolino, and P. Boucaud, *Mater. Lett.*, vol. 18, p. 57, 1993.

[297] P. Boucaud, C. Francis, F. H. Julien, J.-M. Lourtioz, and D. Bouchier, *Appl. Phys. Lett.*, vol. 64, p. 875, 1994.

[298] A. S. Amour, C. W. Liu, J. C. Sturm, Y. Lacroix, and M. L. W. Thewalt, *Appl. Phys. Lett.*, vol. 67, p. 3915, 1995.

[299] L. Lanzerotti, A. S. Amour, C. W. Liu, J. Sturm, J. K. Watanabe, and N. D. Theodore, *IEEE Electron Device Letters*, vol. 17, p. 334, 1996.

[300] W. Faschinger, S. Zerlauth, G. Bauer, and L. Palmetshofer, *Appl. Phys. Lett.*, vol. 67, p. 3933, 1995.

[301] C. L. Chang and J. C. Sturm, *Appl. Phys. Lett.*, vol. 74, p. 2501, 1999.

[302] J. C. Sturm, *Material Research Society Bulletin*, vol. 23, p. 60, April 1998.

[303] S. C. Jain, H. J. Osten, B. Dietrich, and H. Rücker, *Semincond. Sci. Technol.*, vol. 10, p. 1289, 1995.

[304] D. C. Houghton, G. C. Aers, N. L. Rowell, K. Brunner, W. Winter, and K. Eberl, *Phys. Rev. Lett.*, vol. 78, p. 2441, 1997.

[305] O. G. Schmidt and K. Eberl, *Phys. Rev. Lett.*, vol. 80, p. 3396, 1998.

[306] R. Hartmann, U. Gennser, H. Sigg, D. Grützmacher, and K. Ensslin, *Appl. Phys. Lett.*, vol. 73, p. 1257, 1998.

[307] K. Brunner, O. G. Schmidt, W. Winter, K. Eberl, M. Glück, and U. König, *J. Vac. Sci. Technol. B*, vol. 16, p. 1701, 1998.

[308] R. L. Williams, G. C. Aers, N. L. Rowell, K. Brunner, W. Winter, and K. Eberl, *Appl. Phys. Lett.*, vol. 72, p. 1320, 1998.

[309] A. S. Amour, L. D. Lanzerotti, C. L. Chang, and J. C. Sturm, *Thin Solid Film*, vol. 294, p. 112, 1997.

[310] D. V. Singh, K. Rim, T. O. Mitchell, J. L. Hoyt, and J. F. Gibbons, *J. Appl. Phys.*, vol. 85, p. 978, 1999.

[311] J. L. Hoyt, T. O. Mitchell, K. Rim, D. V. Singh, and J. F. Gibbons, *Thin Solid Films*, vol. 321, p. 41, 1998.

[312] B. L. Stein, E. T. Yu, E. T. Croke, A. T. Hunter, T. Laursen, A. E. Bair, J. W. Mayer, and C. C. Ahn, *Appl. Phys. Lett.*, vol. 70, p. 3413, 1997.

[313] D. V. Singh, K. Rim, T. O. Mitchell, J. L. Hoyt, and J. F. Gibbons, *J. Appl. Phys.*, vol. 85, p. 985, 1999.

[314] C. L. Chang, L. P. Rokhinson, and J. C. Sturm, *Appl. Phys. Lett.*, vol. 73, p. 3568, 1998.

[315] H. J. Osten, *J. Appl. Phys.*, vol. 84, p. 2716, 1998.

[316] R. A. Soref, *J. Appl. Phys.*, vol. 70, p. 2470, 1991.

[317] Y. Fu, M. Willander, P. Han, T. Matsuura, and J. Murota, *Phys. Rev. B*, vol. 58, p. 7717, 1998.

[318] A. A. Demkov and O. f. Sankey, *Phys. Rev. B*, vol. 48, p. 2207, 1993.

[319] J. Xie, K. Zhang, and X. Xie, *J. Appl. Phys.*, vol. 77, p. 3868, 1995.

[320] P. C. Kelires, *Phys. Rev. B*, vol. 75, p. 8785, 1997.

[321] P. C. Kelires, *Phys. Rev. Lett.*, vol. 75, p. 1114, 1995.

[322] J. L. Martins and A. Zunger, *Phys. Rev. Lett.*, vol. 56, p. 1400, 1986.

[323] U. Schmid, N. E. Christensen, and M. Cardona, *Solid State Communications*, vol. 75, p. 39, 1990.

[324] E. Kasper and F. Schäffler, *Group IV Compounds Semiconductors and Semimetals*, vol. 83. New York: Academic, 1991. edited by T. P. Pearsall.

[325] M. Kim and H. J. Osten, *Appl. Phys. Lett.*, vol. 70, p. 2702, 1997.