3.6 SUMMARY

Room temperature exposure to a RF hydrogen plasma can dramatically reduce the thermal budget for the crystallization of PECVD *a*-Si:H films. The hydrogen plasma treatment changes the microstructure of the *a*-Si:H at the surface, and depletes hydrogen from the surface of the film. The plasma treatment creates seed nuclei of microcrystalline silicon at the surface (30-40 nm) of the *a*-Si:H film which are characterized by Si-H_2 bonds at the surfaces of the crystallites. During the subsequent anneal at 600 °C, these crystallites grow till the grains touch each other leading to complete crystallization. The plasma treatment thereby enhances the overall crystallization rate as the nucleation step is bypassed in this case. In spite of the enhanced nucleation density due the plasma treatment, the grain size of the blanket hydrogen-plasma-treated films was comparable to that of the untreated films.

This technique can be used to reduce the thermal budget for the fabrication of polysilicon thin-film transistors as discussed in the next chapter. This effect can also be controlled spatially resulting in polycrystalline silicon and amorphous silicon areas on the same substrate and in chapter 5 we will discuss the fabrication of integrated amorphous and polycrystalline transistors. In addition, by this technique of masking, the nucleation in the amorphous films can be controlled so that the location of the grain boundaries in the final polysilicon film can be controlled and larger grains can be realized. In the next chapter we will discuss the use of this property in improving the performance of thin-film transistors.

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Chapter 4

POLYCRYSTALLINE SILICON THIN-FILM TRANSISTORS

4.1 INTRODUCTION

The technology used to fabricate thin-film transistors (TFTs) in polycrystalline silicon (polysilicon) layers is similar to that used for fabrication of metal-oxide-semiconductor field-effect transistors (MOSFETs) in bulk silicon substrates. Conventional integrated circuits fabricated in bulk Si requires isolation between devices, which is usually achieved by growing thick oxides or etching trenches between the active device regions. In addition, the capacitive coupling between the integrated-circuit devices through the high-relative-permittivity silicon substrate can degrade circuit performance. Charge injected at one node of a circuit may travel to an another node through the substrate, changing the charge state of dynamic memory elements. Also charge generation in the substrate also makes bulk-silicon integrated circuits sensitive to radiation. Building transistors in thin polysilicon films isolated from the substrate by the oxide reduces all these limitations.

Restricting integrated circuits to a single plane of devices at the surface of a bulk silicon wafer limits the type of devices and circuits that can be realized. The ability to use the third dimension by employing several layers of transistors would enable the

fabrication of novel device structures and the increase of the device density on the chip. This should also reduce the interconnection length between the devices, improving overall circuit speed. TFTs on large-area, preferably transparent substrates will also be useful for display applications, both for active-matrix transistor array and for addressing and other peripheral circuitry.

Although the shape of the polysilicon TFT characteristics is comparable to that of a bulk MOSFET, a large gate voltage must be applied before significant drain current can flow; the threshold voltage is high, and the transistor has a low transconductance. This is caused due the high concentration of traps, which arise from the crystalline defects in the polysilicon, especially at the grain boundaries, within the forbidden gap of the polysilicon. Much of the applied gate voltage is used to charge or discharge these traps, rather than inducing free carriers in an inversion layer, leading to higher threshold voltages [1].

As most of the traps are located near the grain boundaries, the transistor can be visualized as several transistors in series. Comparatively high-quality grains are separated from each other by highly defective grain boundaries. Consequently, the transistor over the central regions of the grain have a threshold voltage determined by normal transistor equations for single-crystal silicon, but the transistors over the grain boundaries have a much higher threshold voltage. A moderate gate voltage induces conducting channels over the central regions of the grains, but barriers still exist at the grain boundaries. A considerably higher gate voltage is therefore required to induce channels over the grain boundaries and form a continuous conducting path. Consequently, the observed threshold voltage is higher than expected from the dopant concentration in the polysilicon grains. Even after a continuous conducting channel is formed, the transistor characteristics are still limited by the traps at the surface. If the

trap density is high, the charge states of many traps need to be changed to increase the surface potential even slightly, and the field-effect mobility is low [1].

Because of the deleterious effect of grain boundaries, large grain size, defect-free polycrystalline silicon is therefore essential for high performance transistors. As discussed in chapter 2, solid phase crystallization (SPC) of amorphous silicon (*a*-Si) is the preferred technique to obtain polysilicon films with large grain size and smooth surface [2], and hence better transistor performance. Glass substrates, used in display applications, constrains the processing temperature of the transistors to below ~650 °C [3]. Also for 3-D IC integration, the process temperature should also be kept small so that the preexisting devices are not affected. However, because of this upper limit on the process temperature, SPC results in long anneal times [2] (about 20 h or higher), and hence makes the process unattractive for manufacturing. As we discussed in chapters 2, several methods of enhancing this crystallization process have been tried, and of these methods, the plasma-induced crystallization potentially introduces the least contamination to the films. We discussed in chapter 3, the effect of an RF hydrogen plasma exposure at room temperature on the crystallization time of hydrogenated amorphous silicon films. We found that the plasma treatment results in the reduction of crystallization time by nearly a factor of five compared to untreated films, and can be as short as 4 h at 600 °C [4]. We also found that the plasma treatment can be masked to realize polycrystalline and amorphous regions in a single silicon layer, and that this can also lead to lateral crystallization from the exposed to the unexposed regions.

In this chapter we discuss the performance of n-channel self-aligned thin-film transistors (TFTs) fabricated in such polysilicon films crystallized from plasma-enhanced chemical vapor deposited (PECVD) *a*-Si:H after a room-temperature RF hydrogen plasma treatment. TFTs with maximum process temperature of 600-625 °C

and 1000 °C are compared as function of channel length. The hydrogen plasma treatment is also then locally applied to the source/drain region of the TFTs to seed the lateral crystallization into the channel region. The process leads to larger grains in the channel region and a two-fold increase in the mobility at short channel length to ~75 cm^2/Vs for process temperature of 600 °C.

In Section 4.2 the deposition of the precursor *a*-Si:H film and subsequent crystallization anneal, and the material properties of the polysilicon film are described. Section 4.3 describes with the high-temperature TFTs, with thermally grown gate oxides. We discuss the low-temperature TFTs next in Section 4.4, with the effect of plasma treatment and anneal conditions on the TFT characteristic, examined in detail. The laterally-seeded TFTs will be discussed in Section 4.5, and we end with a summary in Section 4.6.

4.2 PRECURSOR SILICON FILM DEPOSITION AND CRYSTALLIZATION

The TFTs in this work were all fabricated in polysilicon films, which were first deposited as hydrogenated amorphous silicon (*a*-Si:H) by PECVD at 150 or 250 °C using pure silane, at pressure of 500 mtorr and RF power density of ~0.02 W/cm^2, with the thickness of the films being ~150 nm (see Appendix A for growth recipes). The substrates were either Corning 1737 or 7059 glass which were pre-annealed as discussed in Section 3.2.1, or silicon wafers coated with ~500 nm of SiO_2 deposited by PECVD at 250 °C, using SiH_4 and N_2O, pressure of 400 mtorr and RF power density of 0.1 W/cm^2. In all cases, the substrates were exposed to hydrogen plasma (Section 3.2.1) prior to *a*-Si:H deposition. In experiments with blanket seeding, the films were then exposed to a room-temperature RF hydrogen or oxygen plasma for one hour in Plasma Therm RIE chamber. Typical plasma conditions were; RF power density of 0.8 W/cm^2, pressure of 50 mtorr and flow rate of 50 sccm. The samples were usually placed on a

100-125 mm Si wafer during exposure to minimize aluminum contamination of the films as discussed previously in Section 3.4.1. The RIE chamber was also cleaned prior to loading the sample with an oxygen plasma at 0.8 W/cm^2 and pressure of 200 mtorr for ~10 min to oxidize any trace organic contamination present in the chamber from previous runs. Some films were not treated to plasma as controls.

After the plasma treatment the samples were cleaned by rinsing in dilute HF. Annealing at 600 or 625 °C in N_2 in a furnace, with the crystallization monitored by UV reflectance measurement (Section 3.2.1), then crystallized the samples. The typical grain size for plasma-treated or untreated control polycrystalline films as observed by TEM is ~0.5 μm (Fig. 3.12 (a)). The grains of the completely crystallized polysilicon film are predominantly oriented in the [111] direction normal to the substrate surface (Fig. 3.11), irrespective of prior treatment.

4.3 HIGH-TEMPERATURE TRANSISTORS (≤ 1000 °C)

Transistors were first made using a conventional self-aligned n-channel high-temperature process flow with a thermally grown gate oxide. These devices are also important for use in high-resolution projection displays, with poly-Si TFTs used in pixel switching circuits and in driver circuits, which are fabricated on high-temperature resistant quartz substrates.

4.3.1 Fabrication details

Plasma treatment and anneal

Transistors were first fabricated after the 600-°C crystallization anneal by a high-temperature process with thermally-grown gate oxide. 150 nm of *a*-Si:H was deposited at substrate temperature (set point) of 150 °C on SiO_2 covered silicon substrates. A polysilicon top-gate self-aligned process was then used to make n-channel

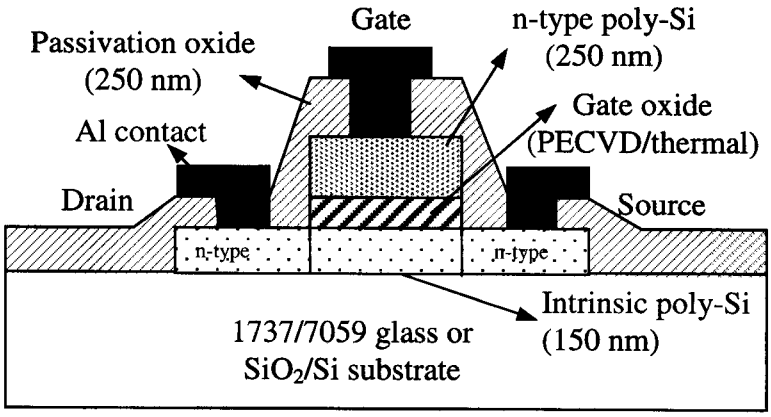


Figure 4.1. Simplified self-aligned TFT cross section for the low-temperature and high-temperature process.

TFTs (Fig. 4.1). The films were either not exposed to a plasma before crystallization (anneal time of 20 h) or exposed to a hydrogen plasma (anneal time 4 h) before crystallization. During the plasma treatment, the samples were placed on a large silicon wafer to eliminate the aluminum contamination form the Al_2O_3 electrode [4].

Device island patterning

After crystallization at 600 °C in N_2, device islands were patterned by dry etching with SF_6/CCl_2F_2 plasma at RF power density of 0.16 W/cm^2 and pressure of 100 mtorr and SF_6 flow of ~25 sccm and CCl_2F_2 flow of 1.6 sccm corresponding to set-point of 80 % and 12.5 % on the flow control potentiometers, respectively [5]. The etch was carried out in Plasma Technology RIE chamber. The etch rate of polysilicon was ~400 nm/min. This etch recipe is also quite selective with respect to either SiO_2 or glass, the ratio of etch rates of Si vs. SiO_2 being >30 [5]. The etching was also monitored by measuring the interference of the reflected He-Ne laser beam from the surface being etched as a function of time. This technique is useful to detect end-point of etching accurately.

Gate Oxidation

Before the gate oxidation, the sample was cleaned by rinsing in hydrogen peroxide and sulfuric acid mixture for ~10 min, and subsequent rinse in dilute HF. The samples were then loaded in the furnace, with N_2 flowing in the furnace tube and the furnace temperature set to 1000 °C. After ~5 min (for the sample to reach the furnace temperature), the N_2 flow was stopped and O_2 flow was started. Oxidation was done for ~20 min and then the samples were annealed in N_2 at the same temperature for ~20 min. To measure the thickness of the oxide, a bare Si lightly doped (~50 Ω-cm) wafer with (100) orientation was loaded along with the polysilicon samples. The thickness of oxide on the bare Si wafer was easily measured with an Ellipsometer or a Nanospec. The thickness of oxide on the polysilicon film was then estimated from this value, knowing that the polysilicon was predominantly (111) oriented and the ratio of oxide thickness of (111) and (100) oriented surfaces is ~1.75 at 1000 °C in the linear regime of growth [6]. The thickness of oxide on the polysilicon samples was then estimated to be ~35 nm.

Gate layer deposition, etch and ion implantation

The n^+ *a*-Si:H gate, ~250 nm thick, was deposited by PECVD in the p-chamber of the S900 plasma deposition system at ~300 °C using SiH_4, PH_3 and H_2, at RF power density of ~0.02 W/cm^2, and pressure of 500 mtorr (see Appendix A for growth sequence). The gate was then patterned by dry etching in SF_6/CCl_2F_2 plasma with the plasma conditions being the same as those used for active island etching except the RF power, which was increased to 0.32 W/cm^2. Once again laser interferometry was used for end-point detection. The endpoint detection ensures that overetch time is minimized so the damage to gate oxide (exposed to plasma at the edges of the gate) is minimal. The gate oxide was then etched in dilute HF to expose the source/drain regions for ion implantation. Care was taken during this step not to overetch as that would result in

transistors with significant gate leakage through the thinned gate oxide at the edge of the device. The thickness of the oxide was also estimated from the surface profile measurement (Dektak) of the sample before and after etching the gate oxide. For ion implantation the small sample pieces were taped on a 100-mm Si wafer and were sent out to a vendor. The source and drain implant was phosphorus at 60 keV and dose of $2x10^{15}$ cm^{-2}.

Implant anneal and hydrogenation

After the ion implantation the samples were annealed at 850 °C in N_2 for ~30 min to anneal the damage. Once again the samples were cleaned by rinsing in hydrogen peroxide and sulfuric acid mixture for ~10 min, and subsequent rinse in dilute HF, before loading in the furnace. After the 850-°C anneal, an RF hydrogenation step was performed to passivate the grain boundaries in the polysilicon film [7]. It has been reported that the hydrogenation is most effective at higher substrate temperature of 300-350 °C, due to enhanced diffusion of hydrogen through the bulk of the film [7]. The RF hydrogenation was done in the i-chamber of the S900 plasma deposition system. The PECVD system was chosen, as the RIE chamber (Plasma Therm), wherein the hydrogen or oxygen plasma-seeding treatments to enhance crystallization were performed, did not have any heaters to control the substrate temperature. The i-chamber was chosen instead of the p-chamber to minimize contamination during the hydrogenation from dopants. The n-chamber is used exclusively for SiN_x deposition as mentioned earlier in Section 3.2.1. We will discuss the effect of hydrogenation on the characteristics of the TFTs in the next section.

To avoid confusion between the various hydrogen plasma treatments used in this work, henceforth, we will refer all plasma treatments to enhance crystallization of *a*-

Si:H films as hydrogen or oxygen plasma *seeding* treatment, and hydrogen plasma treatment to passivate defects will be referred to as hydrogenation.

In some cases, a 250-nm thick passivation oxide was deposited by PECVD at 250 °C after the hydrogenation step in the plasma deposition system (Plasma Therm) using 35 sccm of SiH_4 and 160 sccm N_2O at RF power density of 0.1 W/cm^2 and pressure of 400 mtorr. Etching in buffered HF opened contact holes.

Finally aluminum metal was thermally evaporated on the samples and patterned to form gate, source and drain contacts (Fig. 4.1). To ensure good electrical ohmic contact between the Al layer and the Si film, the sample was rinsed in very dilute HF before the metal deposition to remove any native oxide at the surface. However, care must be taken so that the gate oxide is not etched. The contacts were then annealed in forming gas (mixture of 10% H_2 in N_2) at ~250 °C for ~90 s in AGA associates rapid thermal annealer. The schematic cross-section of the final device is shown in Fig. 4.1.

No significant differences in the characteristics of the transistors were observed by including the passivation oxide step in the process flow. The drawback is the increase in the number of process steps (1 additional mask). On the other hand, this step increases the lifetime of the transistor as the gate oxide (near the edges) is no longer exposed to the atmosphere (Fig. 4.1), and there is no danger of etching the gate oxide as earlier, as the gate region is masked during the contact hole definition step.

The hydrogenation could also be done after the metal step, but we chose this sequence of steps for two reasons. The primary concern was to minimize the antenna effect during the hydrogenation. The antenna effect occurs when large metal areas over either the field-oxide in case of regular ICs in bulk Si, or over the underlying glass or SiO_2 in case of ICs in SOI layers, act as charge collectors [8]. This collected charge is then applied on the gate of the transistor. The current stress through the small area with

the gate oxide is therefore increased by the antenna ratio which is the area of the metal connected to the gate divided by the area of the transistor (see Section 7.2 for more details). The second reason is that the i-chamber can no longer be used for hydrogenation after the metal step (to avoid contamination of the chamber) and therefore the hydrogenation has to be done in the p-chamber, increasing the chance of contamination (p-chamber is where doped films are grown). The transistors were then tested on a Hewlett Packard 4155A Parameter Analyzer.

4.3.2 Results and discussion

For all the TFTs discussed in this chapter, the field-effect mobility was calculated from the maximum value of the transconductance (dI_{DS}/dV_{GS}) at V_{DS} = 0.1 V. The effective channel length was used in the calculation, which was derived from difference between the drawn channel length and the x-intercept of the straight line fit to $1/I_{DS}$ vs. drawn channel length for fixed [$V_{GS} - V_{TH}$]. As the threshold voltage (V_{TH}) can vary with channel length, the value of V_{GS} was varied for the different channel length transistors such that the [$V_{GS} - V_{TH}$] is fixed. The straight-line fit assumed a constant mobility and was done for L>5 μm, since for short L an increase in mobility was observed. The threshold voltage was deduced from the x-intercept of the straight line fit to I_{DS} vs. V_{GS} for V_{DS} = 0.1 V. I_{OFF} is the minimum value of I_{DS} when V_{DS} = 5 V, and I_{ON} is the maximum value of I_{DS} when V_{DS} = 5 V and V_{GS} is scanned from –10 to 20 V.

Effect of RF hydrogenation

During the hydrogenation, the hydrogen plasma etches *a*-Si:H but not poly-Si, hence complete crystallization of the n^+ *a*-Si:H gate layer must be ensured before loading the samples for the hydrogenation step. Significant etching and sputtering of the *a*-Si:H deposited on the walls of the chamber or on the sample holder occurs during the

hydrogenation step, and this *a*-Si:H is deposited on the transistor samples. To prevent this unwanted deposition, the chamber was first cleaned with a hydrogen plasma under the same conditions for ~20 min prior to loading the samples.

Addition of argon (~50 %) is known to increase the ionization efficiency of the plasma and thereby increase the hydrogen ion density [9]. But this led to significant etching of poly-Si too during the plasma treatment. So in our work we used pure hydrogen plasma to passivate the defects in the polysilicon films. The chamber pressure during hydrogenation was high (1 torr) as we could not strike plasma at lower pressures. Higher pressure leads to higher density of hydrogen ions and radicals thereby improving the hydrogenation efficiency. The hydrogenation condition (RF power density and exposure time) was then optimized to realize maximum field-effect mobility and minimum leakage current (Figs. 4.2 (a) and (b)). The field-effect mobility of the transistors increased as the RF power density during hydrogenation was raised (Fig. 4.2(a)). Higher RF power densities leads to increased hydrogen ion density and larger number of hydrogen atoms in the plasma and hence better defect passivation. The ON/OFF current ratio of the TFTs also increased for longer hydrogenation. The ON current increases as the number of defect states, which act as carrier scattering sites decreases. The leakage current decreases as the number of defect states in the band-gap that act as generation sites contributing to source/drain junction leakage, decreases. However, prolonged exposure to hydrogen plasma led to decrease in the ON/OFF current ratio (Fig. 4.2(b)). This is primarily due to increase in leakage currents, the ON currents in fact increased slightly. The increase in leakage current might be due to increasing damage during the plasma exposure from the UV photons and the surface charging (from the ions and electrons flux) leading to degradation of the gate dielectric [10]. We will discuss the plasma-induced damage mechanisms and the techniques to

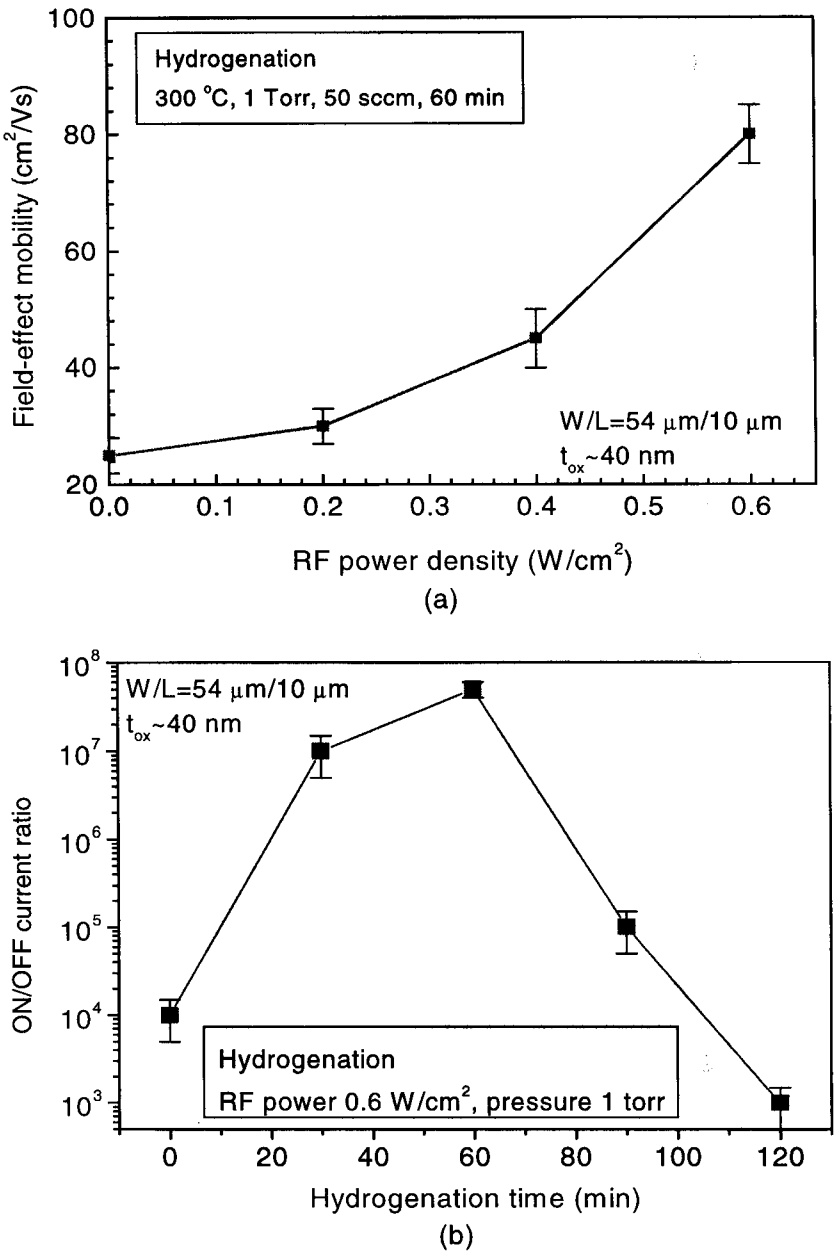


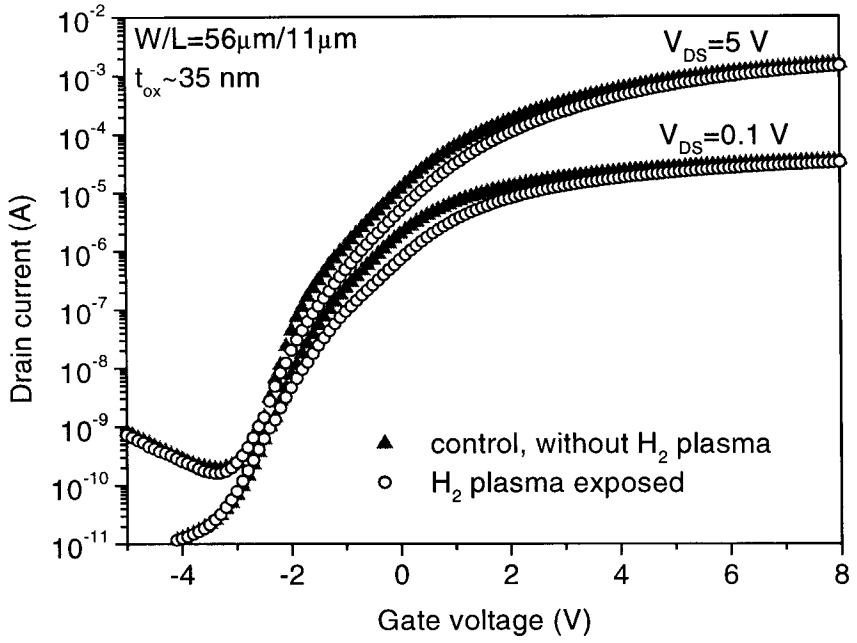
Figure 4.2. Effect of hydrogenation on the high-temperature TFT characteristics, (a) field-effect mobility of the TFTs as a function of the RF power during hydrogenation, and (b) ON/OFF current ratio of the TFTs as a function of exposure time during hydrogenation.

determine the damage in more detail later in Chapter 7. The optimum conditions in terms of field-effect mobility and leakage current were found to be substrate temperature (set point) of 350 °C, RF power density of 0.6 W/cm^2, pressure of 1 torr, hydrogen flow of 50 sccm, and exposure time of 60 min.

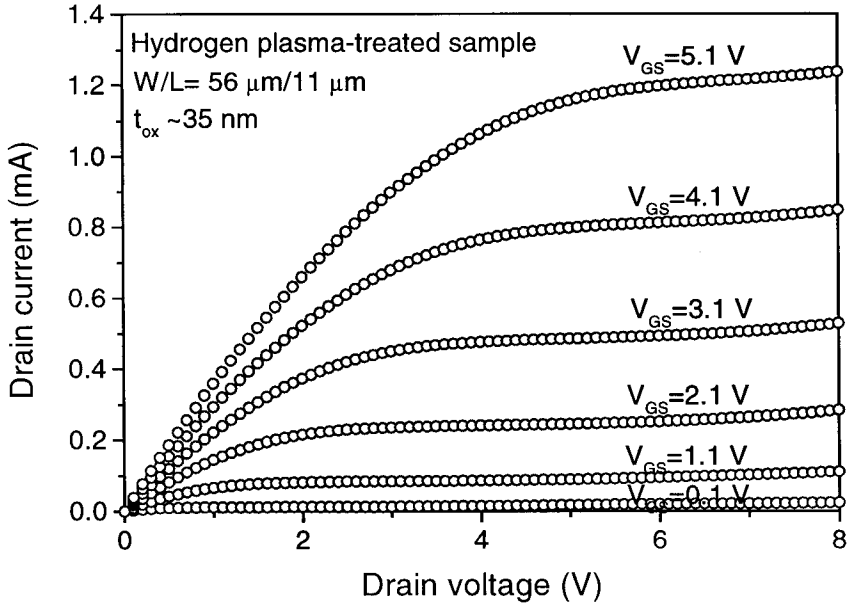
Effect of hydrogen-plasma-seeding treatment

Fig. 4.3 shows typical TFT characteristics after optimum hydrogenation, which were similar and well behaved for devices in films both with and without the hydrogen-plasma-seeding treatment, with no significant difference between two kinds of devices. The threshold voltage was ~0.1 V, the subthreshold slope was ~0.5 V/decade and the ON/OFF current ratio was in excess of 10^7, for both the control and the hydrogen-plasma-treated samples.

Within experimental error, the control and hydrogen-plasma-seeded samples had similar linear region field-effect mobilities. They were ~75 cm^2/Vs at long channel length, but rose up to ~100 cm^2/Vs at channel length of ~2 μm (Fig. 4.4). Others have observed an increase in mobility at short channel lengths in polysilicon TFTs [11, 12]. It has been attributed to grain sizes on the order of a channel length, leading to large portion of the channel with no grain boundaries obstructing the motion of electrons from the source to the drain. Thus our results imply a grain size of few microns, much larger than the as-crystallized film. The apparent increase in grain size over that after the 600-°C crystallization, might result from a grain ripening effect during the high-temperature oxidation and the ion implantation anneal steps, during which the grains oriented in the minimum energy configuration grow at the expense of others [13]. High-temperature processing might also result in the annealing of the structural defects within the grains



(a)



(b)

Figure 4.3. (a) Drain current vs. gate voltage characteristics, and (b) drain current vs. drain voltage of high-temperature poly-Si TFTs made of films annealed at 600°C with and without H_2 plasma-seeding treatment prior to anneal with thermal oxide grown at 1000 °C. Anneal times at 600 °C is 4 h for H_2-plasma-treated sample and ~20 h for untreated sample.

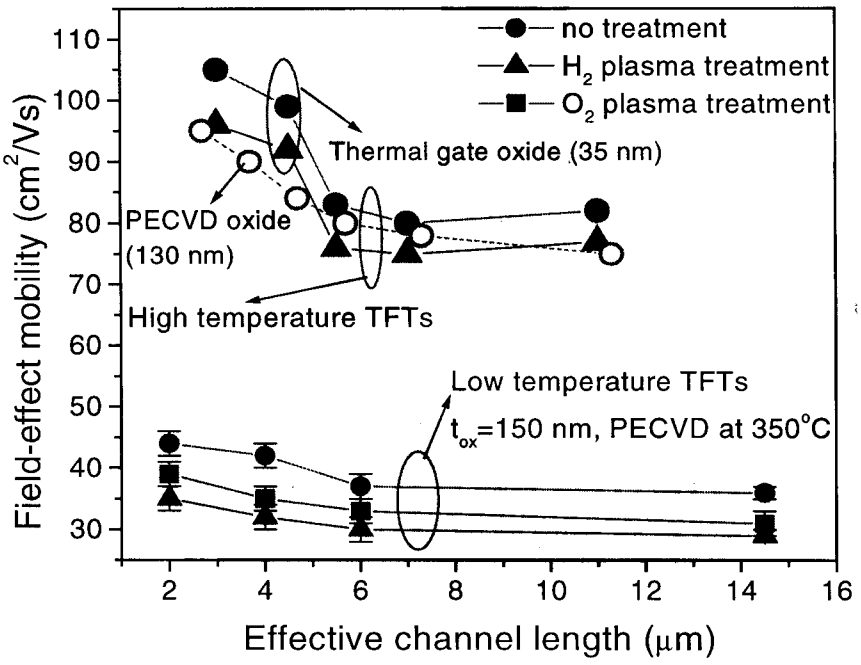


Figure 4.4. Field-effect mobility of high-temperature TFTs as a function of channel length, for untreated (with thermal oxide and PECVD oxide) and plasma-treated (blanket-seeded) films. Field-effect mobility of samples 5, 6 and 7 (Table 4.1) fabricated with low-temperature PECVD oxide also shown for comparison.

of the polysilicon [14], or else some grain boundaries are electrically inactive after the high-temperature anneal, leading to improved performance of the TFTs.

4.4 LOW-TEMPERATURE TRANSISTORS (≤ 600 °C)

4.4.1 Fabrication details

Low-temperature TFTs were made in polycrystalline films on glass substrates not exposed to a plasma before crystallization (anneal time of 13 or 20 h depending on the growth temperature of the initial *a*-Si:H films), and in films exposed to an oxygen (typical anneal time 7 h) or hydrogen (typical anneal time 4 h) plasma before crystallization, with all crystallization done at 600 °C [15]. Table 1 lists the different process conditions for different samples. After the crystallization, n-channel TFTs were fabricated by a standard self-aligned top-gate process, similar to that for the high-

temperature TFTs, except for the low process temperature. After the films were completely crystallized at 600 °C, the active area was defined by dry etching as described in Section 4.3.1.

Gate oxide deposition

Next ~150 nm gate oxide was deposited by PECVD in the Plasma Therm RF plasma deposition chamber. The sample was rinsed in dilute HF to remove any native oxide on the polysilicon surface prior to the deposition. The PECVD chamber was first cleaned with a CF_4 plasma (0.8 W/cm^2, 200 mtorr) for ~15 min. After the etching step, a thin ~100 nm of SiN_x was then deposited to minimize flakes (etch residue) from the chamber walls depositing on the sample during the normal gate oxide deposition. After these chamber-preparation steps, the samples were loaded in the chamber on a 100 mm Si wafer (for uniformity of oxide deposition), and SiO_2 was deposited on them. The conditions during SiO_2 deposition were substrate temperature (set point) of 350 °C or 250 °C, flow of 35 sccm of SiH_4, and 160 sccm of N_2O, pressure of 400 mtorr, and RF power of 0.1 W/cm^2. The gate oxide was then annealed for ~2 h in O_2 at 600 °C in some cases. A few samples had gate oxide deposited by magnetron PECVD at 250 °C at Lawrence Livermore National Laboratory, courtesy of Dr. Steven Theiss.

About 250 nm *a*-Si:H layer doped in-situ with phosphorus (~10^{20} cm^{-3}) was deposited by PECVD in the p-chamber of the multi-chamber S900 system at ~300 °C using 44 sccm of SiH_4, 6 sccm of PH_3 and at a chamber pressure of 500 mtorr and RF power of ~0.02 W/cm^2 to form the gate (see Appendix A for details). Phosphorus doping in the *a*-Si:H films increases the crystallization time as discussed previously in Section 3.3.6. Therefore we tried increasing the deposition temperature of the n$^+$ *a*-Si:H gate layer to ~350 °C to reduce the crystallization time. But this led to significant peeling of the layer during deposition itself. A substrate temperature of ~300 °C was

found to be good trade-off. After the gate was patterned by dry etching in SF_6 and CCl_2F_2 plasma (RF power ~0.3 W/cm^2, pressure of 100 mtorr) the source and drain were implanted with phosphorus at 50 keV and a dose of $2x10^{15}$ cm^{-2}. The anneal of implant damage in the source/drain and crystallization of the gate was done simultaneously by annealing at 600 °C in N_2 for ~6 h, with the rate limiting step being the complete crystallization of the gate. As discussed previously in Section 4.3.1, complete crystallization of the gate is essential so that the gate is not etched during the subsequent hydrogenation step. Note that the maximum process temperature is limited to 600 °C. An RF hydrogenation step was performed to passivate the grain boundaries in the polysilicon film as in the case of the high-temperature TFTs at substrate temperature (set point) of 350 °C, RF power density of 0.6 W/cm^2, pressure of 1 torr, hydrogen flow of 50 sccm, and exposure time of 60 min. (section 4.3.1). A passivation-250-nm thick SiO_2 was deposited in some cases by PECVD as described previously in Section 4.3.1. Etching in buffered HF opened contact holes. Finally aluminum contacts were evaporated and patterned and the metal contacts were annealed as before in forming gas at 250 °C for 90 s in the RTA chamber. All I-V data were measured as before on the HP 4155A Parameter Analyzer.

4.4.2 Results and discussion

Well-behaved characteristics were obtained in all cases as can be seen from Table 4.1. Typical characteristics of drain current vs. gate voltage and vs. drain voltage are shown in Figs. 4.5(a) and 4.5(b) respectively, for a device in a film treated with a hydrogen plasma before a 4-h 600-°C crystallization step (sample 7 in Table 4.1). Typical results are mobilities in the range of 30-40 cm^2/Vs, subthreshold slopes from 1 to 2 V/decade, and ON/OFF current ratios from 10^5 to 10^6. In the subsequent sections, the effects of annealing time and plasma treatment, the effect of the channel length, the

S. No	*a*-Si:H growth temp (°C)	Plasma pre-treatment		Anneal at 600 °C (h)		Gate oxide		TFT characteristics (L_{eff} ~ 3.5 μm)			
		Type	On Si wafer	Cryst. time	Imp. ann.	Temp (°C)	Anneal in O_2	μ_{linear} (cm^2/Vs)	V_{TH} (V)	S (V/dec)	I_{ON}/I_{OFF}
Standard deviation of the data								± 1.5	± 0.3	± 0.2	2x
1	150	-	-	20	6	250	No	38	0.8	1.6	10^6
2	150	H_2	Yes	4	6	250	No	33	-7.5	1.7	10^6
3	150	H_2	Yes	20	6	250	No	33	0.8	1.4	10^6
4	150	-	-	20	45	250	No	37	-6	2.4	10^6
5	250	-	-	12	6	350	Yes	42	0.2	2.6	$2x10^5$
6	250	O_2	No	8	6	350	Yes	38	3.4	1.4	$4x10^5$
7	250	H_2	No	5	6	350	Yes	35	3.2	1.6	$7x10^5$
8	250	-	-	12	6	250	No	30	0.1	2.0	$3x10^5$
9	250	H_2	Yes	5	6	250	No	24	-7	1.8	$5x10^5$
10	250	H_2	Yes	8	6	250	No	24	-0.8	1.6	$5x10^5$
11	150	-	-	20	6	Livermore ox.		32	-4.5	2.5	10^5

Table 4.1. Process conditions and TFT results for devices fabricated with blanket plasma treatment, with maximum process temperature of 600 °C. Except for devices 3, 4 and 10, the crystallization times are the minimum required to saturate the change in UV reflectance (measure of degree of crystallization).

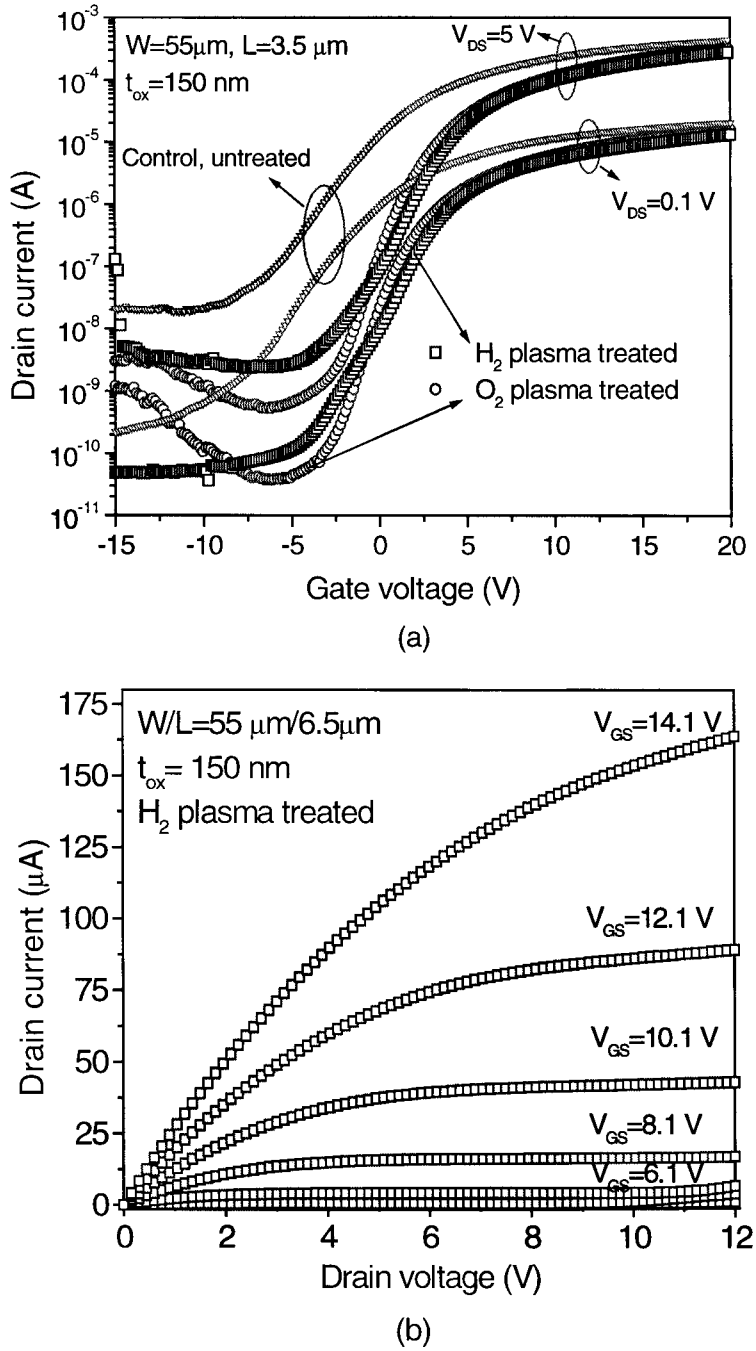


Figure 4.5. (a) Drain current vs. gate voltage, and (b) drain current vs. drain voltage for TFTs in polysilicon films with and without plasma treatment prior to anneal. (samples 5, 6 and 7 in Table 4.1).

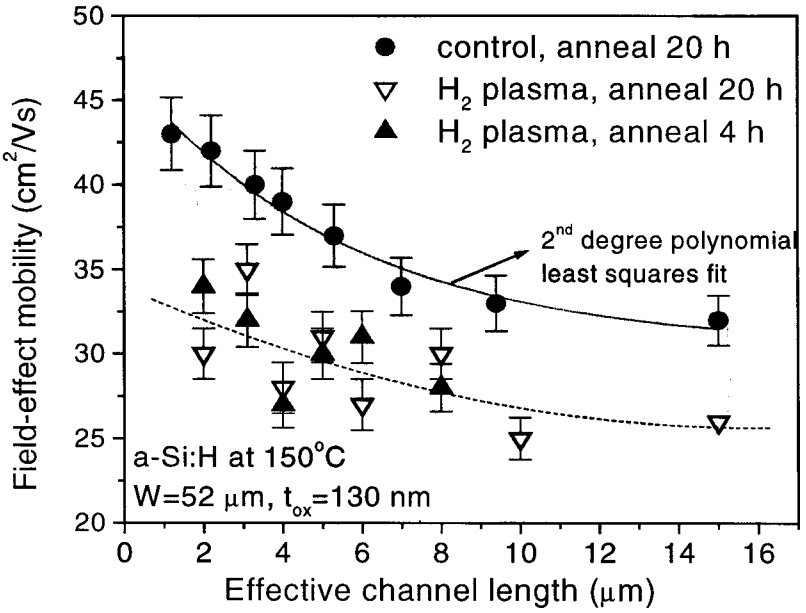


Figure 4.6. Field-effect mobility of polysilicon TFTs in hydrogen-plasma-treated films annealed for 4 h and 20 h (sample 2 and 3), and control untreated film annealed for 20 h (sample 1) at 600 °C, for different channel lengths.

effect of growth temperature of the precursor *a*-Si:H film, and the effect of the gate oxide on device performance will be examined.

Effect of hydrogen-plasma-seeding treatment and anneal time on mobility

The hydrogen-plasma-seeding treatment resulted in slight reduction of field-effect mobility at channel length (L) of ~3.5 μm of the TFT from ~38 cm^2/Vs for the untreated sample (sample 1, Table 4.1) to ~33 cm^2/Vs for the hydrogen-plasma-treated sample (samples 2, Table 4.1). The subthreshold slope was ~1.7 V/decade and the ON/OFF current ratio was ~10^6 for both the hydrogen-plasma-treated and untreated samples. From point of view of these parameters, no significant penalty in TFT performance was seen when using 4-h-hydrogen-plasma-treated anneal vs. 20-h anneal for the untreated case.

To ensure that the field-effect mobility in the case of the hydrogen-plasma-treated sample was not smaller due to the shorter anneal time and to discern the effect of anneal time on threshold voltage, transistors were also fabricated in films annealed at 600 °C in N_2 for various anneal times. Samples 2 and 3 were hydrogen-plasma-treated before and annealed for 4 h and for 20 h at 600 °C, respectively. Samples 1 and 4 were untreated and annealed later for a total of 20 h and 60 h at 600 °C, respectively. All the samples were placed on a 125-mm Si wafer during the hydrogen plasma treatment to reduce the effect of aluminum sputtering onto the sample (as discussed previously in Section 3.4.2). The gate insulator in this case was PECVD SiO_2 deposited at 250 °C. The field-effect mobility of the transistors from hydrogen-plasma-seeded films (2 and 3) was independent of the annealing time, with both samples having a mobility of ~30 cm^2/Vs at L ~ 3.5 μm, and was smaller than the field-effect mobility of the control untreated samples (annealed for ~20 h) at all channel lengths (Fig. 4.6). The very long anneal in the case of sample 4 (~20 h crystallization anneal and ~45 h implant damage anneal after the ion implantation step at 600 °C) also did not result in any change in field-effect mobility (Table 4.1).

The field-effect mobility of the low-temperature TFTs in polysilicon films with or without plasma treatment did not change appreciably as the channel length was reduced (Figs. 4.4 and 4.6). There was a gradual ~20 % increase in field-effect mobility as the channel length was reduced from ~15 μm to ~2 μm. In case of the high-temperature TFTs, however, the increase is higher (>30 %) and it saturates below channel length of ~3 μm, indicating that the grains in the high-temperature case are about 3 μm or larger in size. However, the grain sizes in the low-temperature case are much less than 2 μm, (which was the smallest channel length) as was confirmed by

TEM measurement. The higher values of field-effect mobilities of the high-temperature TFTs might be due to larger grains [13] and lower number of intra-grain defects due to the high-temperature anneal [14], and due to lower interface-state density for the thermal gate oxide (confirmed by C-V measurements of MOS capacitors). The subthreshold slope and the ON/OFF current ratio of the low-temperature TFTs did not change significantly when the channel length was changed from 10 μm to 2 μm.

Effect of hydrogen-plasma-seeding treatment and anneal time on V_{TH}

Threshold voltages were affected by the plasma treatment, with the hydrogen-plasma-treated sample having a threshold voltage of -7.5 V compared to 0.8 V at L ~ 3.5 μm in case of the untreated control sample. As in the case of the high-temperature TFTs, the samples were placed on a Si wafer during the hydrogen-plasma-seeding step to minimize the aluminum contamination in the films, hence the threshold voltage shift is not due to aluminum sputter effect.

The threshold voltage (V_{TH}) did depend strongly on the annealing time for the hydrogen-plasma-treated samples, with the V_{TH} for the long-channel TFTs increasing from -1 V to 4 V (L>10 μm) when the annealing time increased from 4 h to 20 h (Fig. 4.7). But the threshold voltages for samples 1 and 3, which were both annealed for 20 h, are nearly the same (Fig. 4.7). This indicates that the plasma treatment, with the sample placed on a Si wafer during exposure, itself does not affect the threshold voltage of the TFTs and that V_{TH} depends strongly on the annealing time of the films for the same gate oxide. All the *a*-Si:H films deposited by PECVD have high oxygen content of $3\text{-}4\times10^{18}$ cm^{-3} (as measured by SIMS) [4] and even at the crystallization temperature of 600 °C, enough oxygen related thermal donors might be created to dope the polysilicon films slightly n-type [16]. This would lead to negative threshold voltages making it difficult to

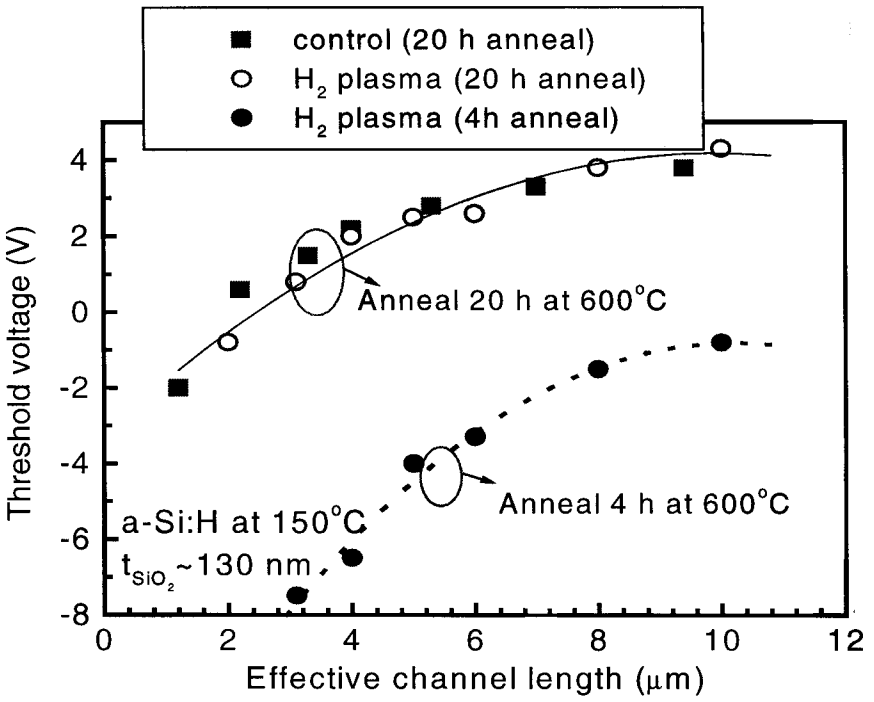


Figure 4.7. Threshold voltage of polysilicon TFTs in hydrogen-plasma-seeded films annealed for 4 h and 20 h (sample 2 and 3, Table 4.1) and control untreated film annealed for 20 h (sample 1, Table 4.1) for different channel lengths.

turn the transistors off. Long annealing (e.g. 20 h in sample 1) might reduce the doping effect of the oxygen in the film due to dissolution of the thermal donors [16, 17], and hence change the TFTs characteristics from normally ON to normally OFF. The fairly high negative threshold voltage in the case of sample 4 (-6 V) might be due to dopant diffusion into the channel region during the long implant (~45 h at 600 °C) damage anneal. This could lead to the channel being doped slightly n-type and hence result in large negative threshold voltage.

Some of the plasma-treated samples (samples 5 and 6, Table 4.1) show higher threshold voltages of ~3 V than the 0.2 V for the sample without the plasma treatment (sample 7, Table 4.1). We believe that the higher threshold voltage is a result of the sputtering of aluminum from the aluminum oxide coated electrode on to the sample

during the plasma exposure, which we found to dope the channel region p-type (N_{Al} ~$5x10^{18}$ cm^{-3} as measured by SIMS [4, 15]). Placing the samples on a Si wafer during the plasma treatment reduced the aluminum contamination effect, and the TFTs made in these films did not show the positive threshold voltage shift.

The threshold voltage of the TFTs dropped by ~5 V as the channel length was reduced to 2 μm from 10 μm in case of both the plasma-treated and untreated samples annealed for either 4 h or 20 h at 600 °C (Fig. 4.4). This reduction in threshold voltage might be due to short channel effects, and due to the lateral diffusion of dopants from the source/drain regions into the channel region during the implant damage anneal, which also causes reduction of effective channel length from drawn channel length. The lateral diffusion of dopants in polysilicon is enhanced due the presence of grain boundaries and can be as much as 2 μm for phosphorus annealed at 900 °C for 60 min [18]. This dopant diffusion might lead to the channel being doped slightly n type and hence result in large negative threshold voltages in case of the short channel TFTs. At long channel lengths, the central part of the channel is not affected due to slight lateral dopant diffusion.

Effect of growth temperature of original *a*-Si:H on mobility and V_{TH}

The field-effect mobility of the TFTs from control untreated films (samples 1 and 8, Table 4.1) was reduced to ~30 cm^2/Vs from ~38 cm^2/Vs for channel length of 3.5 μm, when the growth temperature of the original *a*-Si:H film was changed from 150 °C to 250 °C. All the TFTs had gate oxides deposited by PECVD at 250 °C, with no annealing of the SiO_2 at 600 °C. As the growth temperature for *a*-Si:H is lowered, the hydrogen content in the *a*-Si:H film is increased and the crystallization time increases[15], suggesting that the grain sizes become larger [19]. Larger grain size implies fewer grain

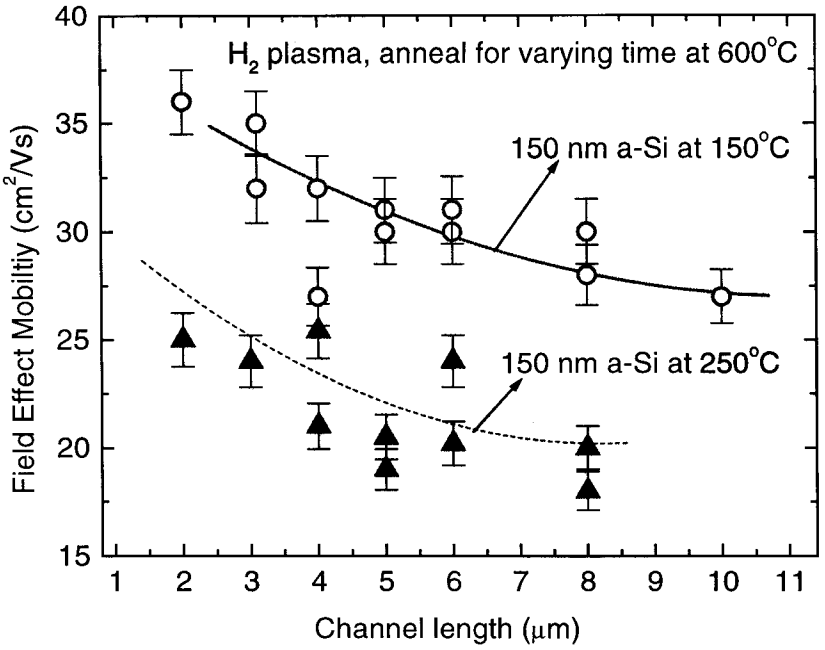


Figure 4.8. Field-effect mobility of polysilicon TFTs in hydrogen-plasma-treated films annealed for various times at 600 °C as a function of channel length. For *a*-Si:H growth temperature of 150 °C and 250 °C, samples 1 and 8, respectively.

boundaries in the channel. Therefore we expect larger field-effect mobility for the TFTs with polysilicon films from *a*-Si:H deposited at lower temperatures. A similar trend was seen for the hydrogen-plasma-seeded samples (Fig. 4.8), in which the field-effect mobility reduced to ~25 cm^2/Vs from ~33 cm^2/Vs for channel length of 3.5 μm (samples 2 and 9, Table 4.1) when the growth temperature was raised from 150 °C to 250 °C. There was no significant change in threshold voltage in either case. The hydrogen plasma treatment is more efficient in creating seed nuclei in films deposited at lower temperature [4]: the crystallization time at 600 °C was reduced to ~4 h from ~5 h when the growth temperature was lowered to 150 °C from 250 °C (as we discussed in Section 3.3.4). But it is not clear why the field-effect mobility of the hydrogen-plasma-

treated TFTs should decrease as the growth temperature of the precursor *a*-Si:H films is raised.

Effect of gate oxide and high-temperature anneal after crystallization

The gate oxide plays an important role in determining the TFTs characteristics. Nearly all the TFTs fabricated in this section used PECVD gate oxide. The temperature of deposition of the PECVD oxide also affects the properties of the oxide and therefore the characteristics of the TFTs. The field-effect mobility of the TFTs increased from ~30 cm^2/Vs to ~42 cm^2/Vs for the control samples (samples 8 and 5, Table 4.1), and from ~24 cm^2/Vs to ~35 cm^2/Vs for the hydrogen-plasma-treated samples (samples 9 and 7, Table 4.1), when the deposition temperature of the PECVD oxide was changed from 250 °C to 350 °C, and a 2-h 600-°C anneal in O_2 was added after the gate deposition. These are the highest mobilities found in both the control and the hydrogen-plasma-treated cases. The threshold voltage of the TFTs increased slightly from 0.1 V to 0.2 V (samples 8 and 5, Table 4.1) when the gate oxide growth temperature was increased to 350 °C and annealed in O_2 subsequently. The PECVD gate oxide has a high fixed charge density of ~10^{12} cm^{-2} and a high interface-state density ~10^{12} $cm^{-2}eV^{-1}$, as deduced from C-V measurement of MOS capacitors on crystalline Si substrates made using the same gate oxide. Subsequent anneal of the oxide at 600 °C in O_2 did not affect the interface-state densities appreciably, though the fixed positive charge density was slightly reduced from ~$6x10^{11}$ cm^{-2} to ~$3x10^{11}$ cm^{-2} after ~2 h of anneal, which might explain the small increase in threshold voltage of the n-channel TFTs with the gate oxide anneal in O_2.

The TFT performance with gate oxide deposited by magnetron plasma-enhanced CVD at Lawrence Livermore National Laboratory by Dr. Steven Theiss was also examined. The field-effect mobility of an untreated control sample with a magnetron-

PECVD oxide deposited at 250 °C was ~32 cm^2/Vs (sample 11, Table 4.1) as compared to ~38 cm^2/Vs for the control sample (sample 1, Table 4.1) with normal PECVD oxide at L=3.5 μm. The subthreshold slope of the TFTs with magnetron-PECVD oxide was ~2.5 V/decade as compared to ~1.6 V/decade for the TFTs with the regular-PECVD oxide. The lower mobility and poorer subthreshold slope in case of the TFTs with the magnetron-PECVD oxide suggests that the interface-state density is higher for the gate oxide deposited by magnetron-PECVD. The threshold voltage of the magnetron-PECVD device was -4.5 V compared to 0.8 V for the normal PECVD device at L=3.5 μm. The large negative threshold in the former case might be due to the higher fixed oxide charge, which is typically positive, in the magnetron-PECVD oxide.

As discussed previously, the higher value of mobility in case of the high-temperature process compared to the low-temperature case, might be due to the increase in grain size [13] and lower number of defect states within the grain [14], and/or reduction in interface-state density for the dry thermal oxide. To find out the dominant effect, TFTs were made in polysilicon films annealed at 1000 °C after the 600 °C crystallization anneal with PECVD gate oxide, and compared with TFTs with thermal gate oxide grown at 1000 °C. The field-effect mobility of the transistors with PECVD oxide and a high-temperature anneal was ~75 cm^2/Vs vs. ~82 cm^2/Vs for the TFTs with thermal gate oxide at long channel lengths. The field-effect mobility also shows similar dependence on channel length in both cases, indicating increased grain size of a few microns due to the high-temperature anneal (Fig. 4.4). The subthreshold slope, which is proportional to gate oxide thickness when the sum of polysilicon space-charge capacitance and the interface-state capacitance is much greater than the gate oxide capacitance, is ~1.8 V/decade for the 130 nm PECVD oxide vs. 0.5 V/decade for the 35 nm thermal oxide. But the ON/OFF current ratio (10^6 vs. 10^7) is poorer in case of the

PECVD gate oxide TFTs due to higher leakage current. This data clearly indicates that mobility of high-temperature TFT is predominantly affected by the high-temperature anneal leading to increased grain size, and not by the gate oxide quality. The thermal oxide with the lower interface-state density results in lower leakage currents compared to the PECVD oxide and only marginal improvement in field-effect mobility. This leads us to the conclusion that overall TFT performance can be improved with large-grain polysilicon and higher-quality gate oxides like thermal oxide or ECR oxide [20].

Non-self-aligned n-channel TFTs fabricated in polysilicon films crystallized after an ECR oxygen plasma treatment at 400 °C, with a maximum process temperature of 600 °C, have also been reported [21]. The process details were, however, not reported. The TFTs had a field-effect mobility of 35 cm^2/Vs and ON/OFF current ratio of ~10^6, which are similar to the values in this work.

4.5 LATERALLY-SEEDED LOW-TEMPERATURE TRANSISTORS

4.5.1 Device Concept

In the previous section we found that the field-effect mobility of high-temperature long-channel (>10 μm) TFTs is ~75 cm^2/Vs, compared to ~35 cm^2/Vs for the low-temperature long channel TFTs. The field-effect mobilities of theses transistors are primarily limited by the grain size, due to scattering of carriers at the grain boundaries. Our aim is to increase the mobility in polycrystalline silicon low-temperature (≤ 600 °C) transistors by increasing grain sizes, within a reasonable thermal budget. If the grain boundary locations can be controlled, transistors can then be fabricated within a grain, eliminating the grain boundary effect altogether.

A large grain size can be achieved by a very high-temperature anneal (~1000 °C), after the polysilicon is first formed, so that the large grains grow at the expense of

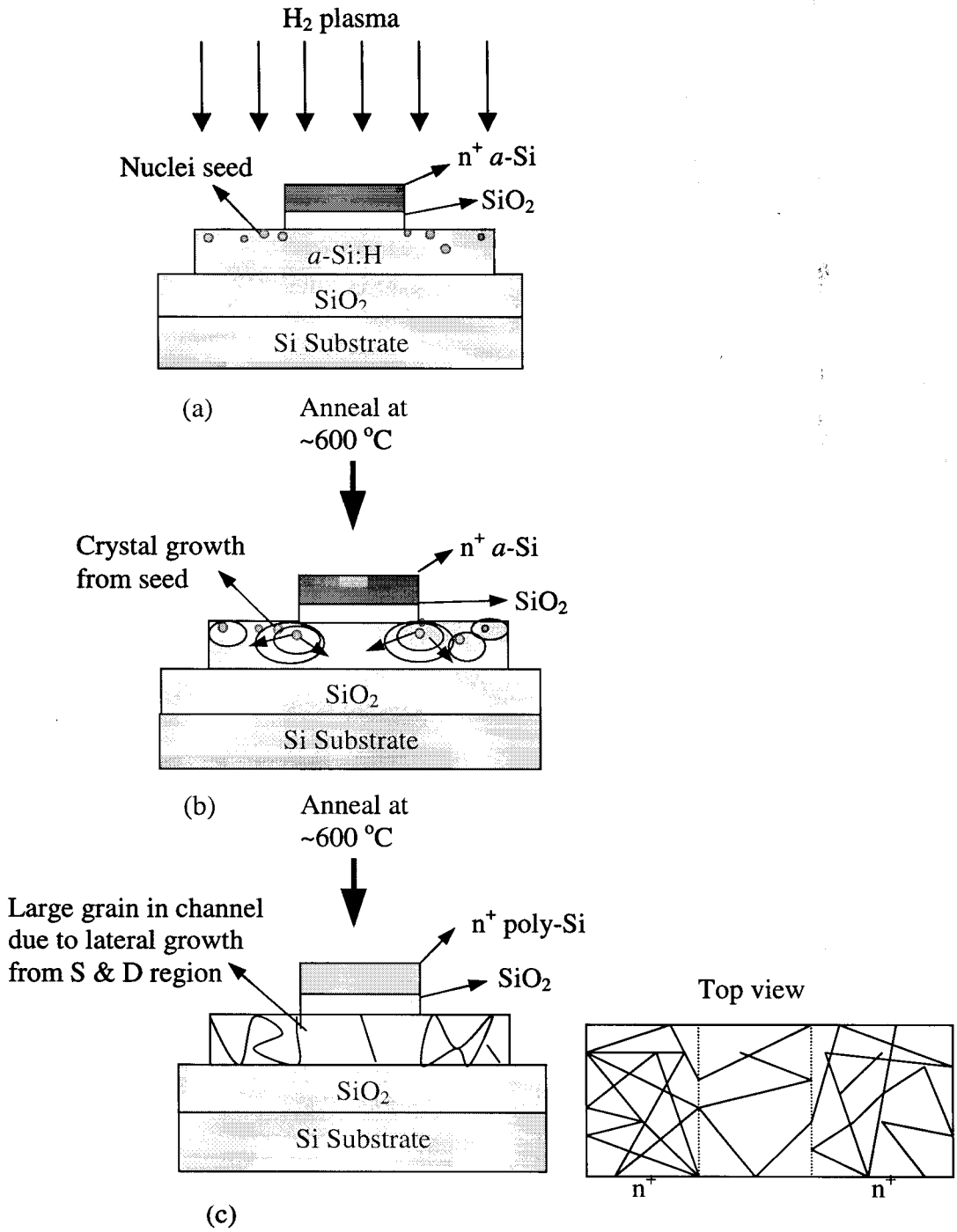


Figure 4.9. Schematic cross-section of the laterally hydrogen-plasma-seeded TFT fabrication sequence. (a) Hydrogen plasma seeding in source/drain and gate regions after ion implantation and gate/device island definition steps. (b) Crystallization and implant damage anneal at ~600 °C. (c) Cross-sectional view and top view of device after complete crystallization.

the small leading to an overall increase in grain sizes [13] and mobility in the 1000-°C process vs. the 600-°C process (discussed in detail in Section 6.2.4). An alternative is the lateral grain growth of polysilicon from the source and drain regions into the adjacent *a*-Si:H channel region to directly form large-grain polysilicon in the channel at 600 °C. This process has the added advantage that the grain boundary location is controlled, i.e. for the right channel length, the number of grain boundaries in the channel can be reduced to just one at the center of the channel (dual seeding). This technique involves selective seeding by hydrogen plasma treatment of the source and drain regions masked by the gate as illustrated in Fig. 4.9. To eliminate the single grain boundary at the center of the channel, seeding has to be done only at the one end (either drain or source). This, however, leads to increased masks and aligning steps, as the seeding will now have to be done earlier and the transistor fabricated subsequently, such that the channel is in the laterally crystallized region [12].

Note, other groups have done similar lateral crystallization using metals like Ni [22], or germanium [12], leading to either Ni or Ge contamination in the channel regions, respectively. Patterned light absorption masks were also used to fabricate laterally crystallized polysilicon TFTs [11], but this technique requires transparent substrates and the crystallization anneal was done at high-temperature of 850 °C. We will discuss these techniques in further detail in chapter 6.

4.5.2 Selective crystallization

Selective crystallization with plasma seeding can be done by masking against the plasma with an oxide [21, 23]. As discussed in Section 3.3.7, 100 nm of SiO_2 was deposited by electron-beam evaporation on top of 150 nm of *a*-Si:H film deposited at 150 °C. The SiO_2 was then patterned and the samples were exposed to hydrogen plasma. Then all the remaining SiO_2 was stripped and the samples were annealed in the furnace

for ~4 h at 600 °C. The exposed areas crystallized completely as expected, while the unexposed areas remain amorphous [4]. The amorphous/polycrystalline difference of the two regions was also confirmed by UV reflectance measurements. Note that the size of the crystalline area increases with time. This shows that the crystalline/amorphous interface front moves out of the seeded areas to the unexposed areas, with the lateral crystalline growth rate being ~0.5 μm/hr at 600 °C [4]. The lack of crystalline grain nucleation in the unexposed area, which is a result of the higher activation energy for nucleation than the activation energy of crystal growth, leads to larger silicon grains in the lateral growth area than in the plasma-seeded areas. This was confirmed by plan-view transmission electron microscopy (TEM) measurements of the films, which shows that the lateral grain growth from seeded regions results in grains as large as ~3 μm (Fig. 3.12 (b)). The grains in the seeded regions themselves, as in case of the blanket crystallization, are only ~0.5 μm in size (Fig. 3.12 (a)). The TEM sample preparation involved chemically etching a hole in the substrate to realize an electron-transparent film at the edge of the hole (see Section 3.2.3 for further details on TEM sample preparation).

4.5.3 Fabrication of laterally-seeded transistors

We used the hydrogen-plasma seeding technique to fabricate laterally-seeded TFTs with higher mobility. The source/drain regions were used as the seeded regions to promote lateral crystal growth in the channel. No additional lithography steps were required because the patterned gate was used as the mask for the hydrogen plasma seeding treatment as illustrated in Fig. 4.9. The transistors were fabricated using a 150 nm *a*-Si:H layer deposited at a substrate temperature of 150 °C. The active islands were then patterned by dry etching in SF_6/CCl_2F_2 plasma as described earlier. The gate

insulator used was PECVD SiO_2 deposited at a substrate temperature of 250 °C. Note that the gate oxide is deposited on *a*-Si:H and the crystallization anneal is done with the gate oxide covering the channel regions. This is in contrast to the low-temperature TFTs discussed in Section 4.4.1 where, the gate oxide was deposited after the amorphous film was completely crystallized.

A 250-nm thick phosphorus-doped *a*-Si:H film was then grown for the gate (see Appendix A for growth recipe). After patterning the gate, the samples were implanted with phosphorus to form the source and drain contacts. A few samples were then exposed to hydrogen plasma (seeded) to create seed nuclei in the exposed source and drain and gate electrode regions and annealed at 600 °C and 625 °C along with unseeded control samples. Both the crystallization and the implant anneal were done simultaneously. The anneal time of ~20 h at 600 °C and ~6 h at 625 °C was chosen such that the channel region of the longest channel (~15 μm) TFTs and the n^+ *a*-Si:H gate layer was completely crystallized, considering the crystal growth velocity is ~0.5 μm/h at 600 °C [4] and that phosphorus-doped source/drain regions and gate take longer time to crystallize [24]. The hydrogen plasma seeding reduced the crystallization time for the crystallization of the phosphorus-doped gate [4]. Transistors were also fabricated with the lateral crystallization anneal of the channel done prior to the ion implantation step. This involved two 600-°C steps, one to crystallize the channel and another to anneal the implant damage, and therefore a higher thermal budget. RF hydrogenation was done after the crystallization/implant-damage anneal as in case of the low and high-temperature TFTs discussed previously. The back-end processing was the same with passivation oxide deposition, etching contact holes, deposition of aluminum, patterning contacts and annealing the contact in forming gas, all done as previously described in Section 4.3.2.

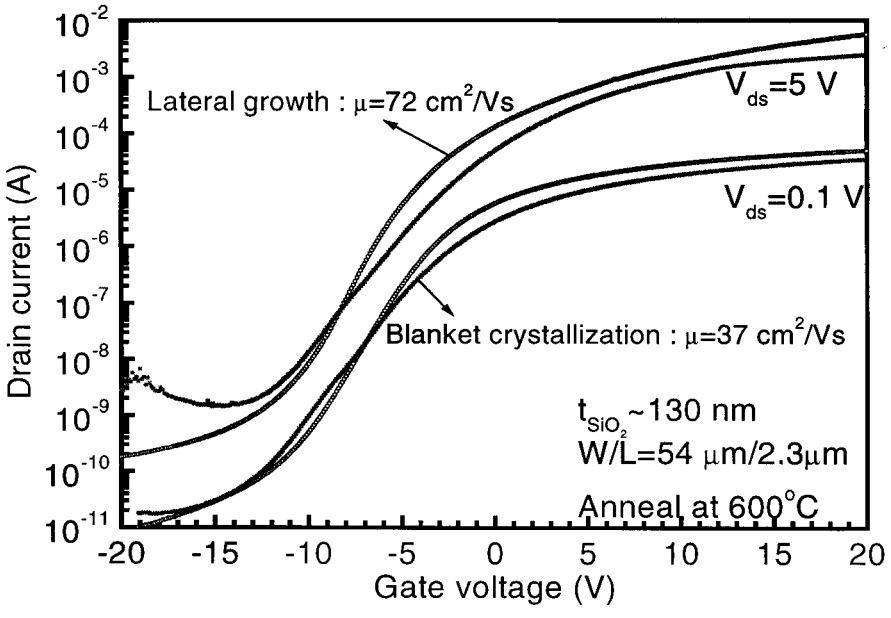
S. No.	*a*-Si:H growth temp (°C)	Plasma pre-treatment		PECVD Gate Oxide		Anneal temp (°C)/ time (h)	TFT characteristics (L_{eff} ~ 2 μm)			
		Seed	After ion implant	N_2O plasma	Magnet ron		μ_{linear} (cm^2/Vs)	V_{TH} (V)	S (V/ dec)	I_{ON}/I_{OFF}
Standard deviation of data							± 3	± 0.5	± 0.2	2x
12	150	Yes	Yes	No	No	600/20	72	-4	1.6	10^7
13	150	No	Yes	No	No	600/20	37	-4	1.7	$2x10^6$
14	150	Yes	Yes	No	No	625/5	68	-4	1.6	10^7
15	150	No	Yes	No	No	625/5	30	-4	1.7	$3x10^6$
16	150	Yes	Yes	No	Yes	600/20	50	2.4	1.5	$3x10^6$
17	150	Yes	Yes	No	Yes	600/60	48	2.3	1.6	10^6
18	150	Yes	No	No	No	600/25	44	-5	2.0	$4x10^6$
19	150	No	No	No	No	600/25	32	-5	2.4	$8x10^5$
20	250	Yes	Yes	Yes	No	600/12	28	-2	2.6	10^4
21	250	No	Yes	Yes	No	600/12	27	-1.5	2.6	10^4
22	150	Yes	Yes	Yes	No	600/20	74	-2.5	2.3	10^4

Table 2. Laterally-seeded low-temperature TFT characteristics for various growth, anneal and process conditions. The column, "after ion implantation" refers to whether the H_2 seeding treatment and lateral crystallization, was done before or after the S & D ion implantation step. The column, "N_2O plasma" refers to whether the gate PECVD oxide was treated to N_2O plasma after deposition. See text for further details.

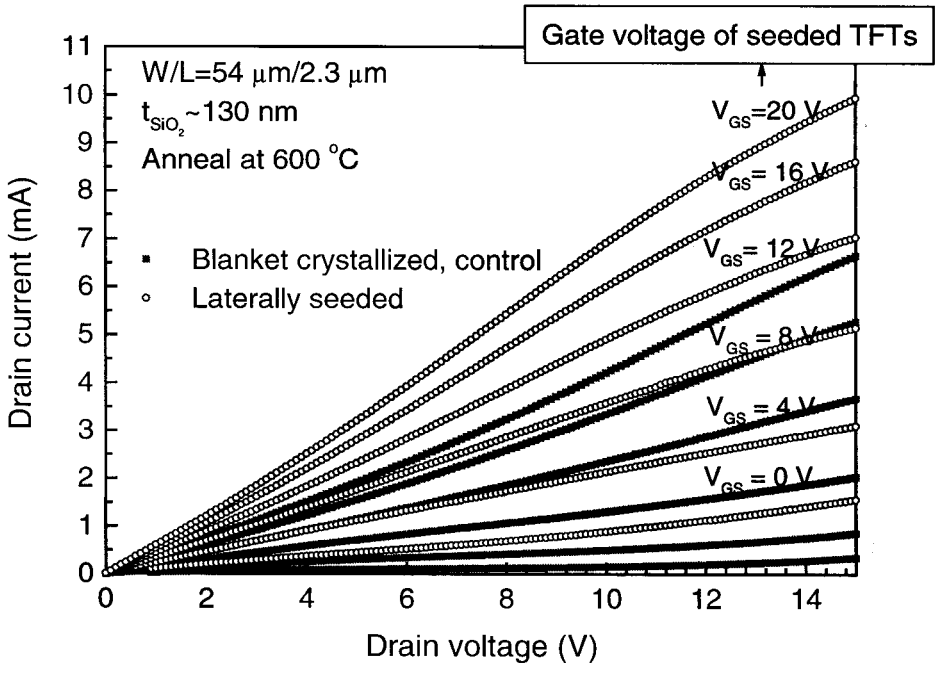
4.5.4 Results and discussion

Table 4.2 lists the characteristics of the laterally-seeded TFTs under various process conditions, with the measurement conditions being the same as those mentioned in Section 4.4.2. The laterally-seeded transistor (sample 12) showed excellent characteristics as can be seen in Fig. 4.10 with ON/OFF current ratios of ~10^7 and subthreshold slopes of about 1.7 V/decade. The threshold voltages of the TFTs decreases as the channel length is reduced because of the short-channel effect as discussed previously, with the threshold voltage of both the unseeded and seeded TFTs equal to -4 V at L ~ 2μm (Fig. 4.11(a)). The threshold voltages are more negative compared to the low-temperature TFTs discussed in Section 4.4.2, with the shift in threshold voltage being ~ -2 V. The negative shift in the threshold voltage in case of the unseeded or seeded TFTs fabricated in this manner might be due to the long anneal at 600 °C after implantation. Long anneal times were necessary in this case as the crystallization of the amorphous active layer and the implant damage anneal were done simultaneously. We saw similar large negative threshold voltages in case of the low-temperature TFTs that were annealed for long duration after the ion implantation step (sample 4, Table 4.1). The large negative threshold could also be due to the higher fixed charge density in the PECVD oxide, as in this case the oxide was deposited on the *a*-Si:H layer prior to the crystallization anneal in contrast to after the crystallization anneal for the low-temperature TFTs discussed previously in Section 4.4.

The dopant diffusion during the long anneal (~20 h at 600 °C) could lead to shorter effective channel length and therefore result in an apparent increase in field-effect mobility as deduced from the drawn channel length. Therefore the effective channel length was calculated by plotting $1/I_{DS}$ as a function of the drawn channel length for various $|V_{GS} - V_{TH}|$ values and finding the x-intercept of the straight line



(a)



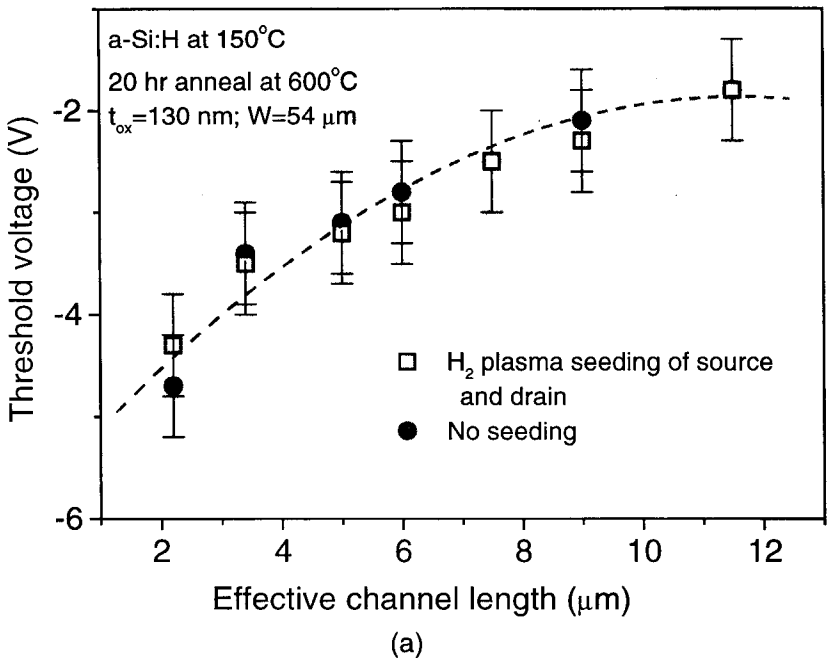
(b)

Figure 4.10. (a) Drain current vs. gate voltage, and (b) drain current vs. drain voltage of the seeded and unseeded control poly-Si TFTs (sample 12 and 13) with maximum processing temperature of 600 °C.

(Figs. 4.12(a) and 4.12(b)) with V_{TH} calculated for each channel length (as discussed previously in Section 4.3.2). For fixed values of field-effect mobility, $1/I_{DS}$ varies linearly with channel length and in ideal situation it goes to zero when the channel length goes to zero. Hence, the x-intercept is ΔL and $L_{effective} = L_{drawn} - \Delta L$. But as the field-effect mobility is not expected to be constant for all the channel lengths in this case, the straight line fit is limited to $L_{drawn} > 5$ μm and extrapolated to yield the effective channel length. The ΔL values are nearly the same (0.2-0.4 μm) for both the seeded and the unseeded TFTs.

The mobility of the transistor for different channel lengths is shown in Fig. 4.11 (b). At long channel lengths, the field-effect mobilities of the laterally-seeded TFTs are ~ 37 cm^2/Vs, slightly higher than in the unseeded process. Not known if significant. At short channel lengths, < 5 μm, the control devices show negligible change in mobility, but the laterally-seeded devices show a large increase in mobility up to ~72 cm^2/Vs. This is attributed to the larger grain size in the channel region of the laterally-seeded transistor. The negligible change in mobility as channel length is reduced in the control devices means that the effective grain size is much smaller than the smallest channel length (2 μm) as seen in Section 4.4.2.

The leakage current (minimum drain current in the OFF state) of the laterally-seeded TFTs is ~3 pA/μm compared to ~35 pA/μm for the unseeded control devices. The large grains in case of the laterally-seeded devices means fewer grain boundaries in the channel region and hence fewer number of trap states, leading to lower leakage current. This dependence of leakage current of polysilicon TFTs on the grain size of the polysilicon has also been reported elsewhere [25].



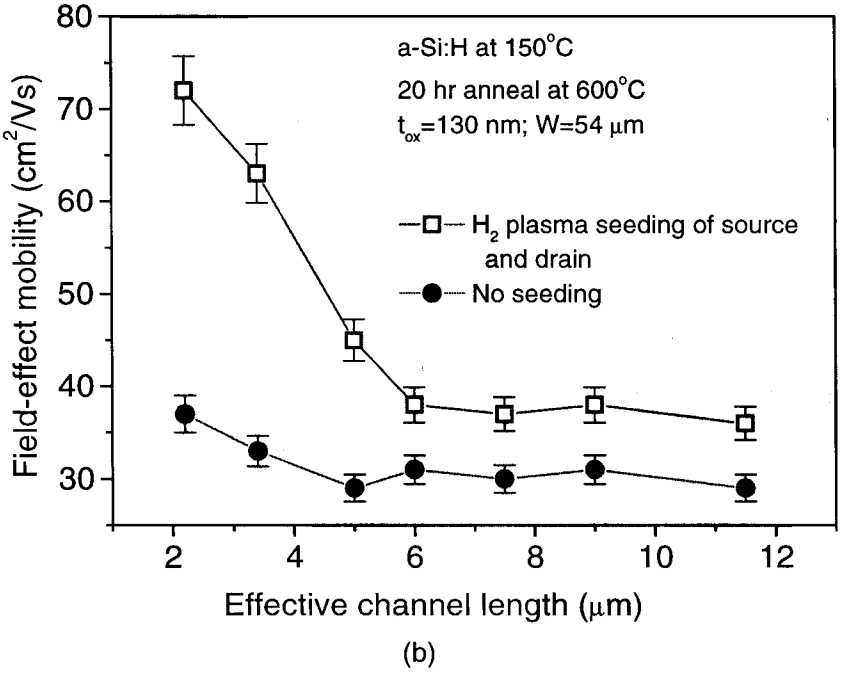
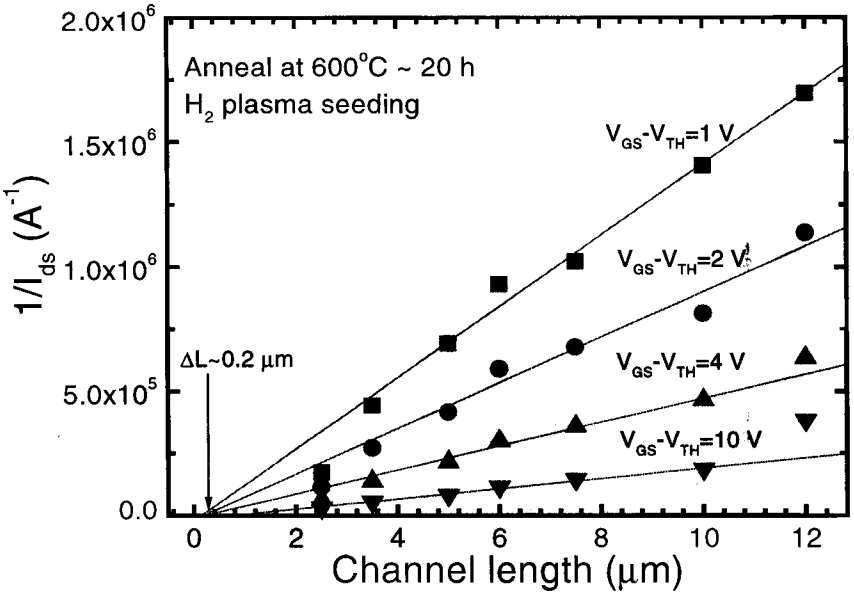
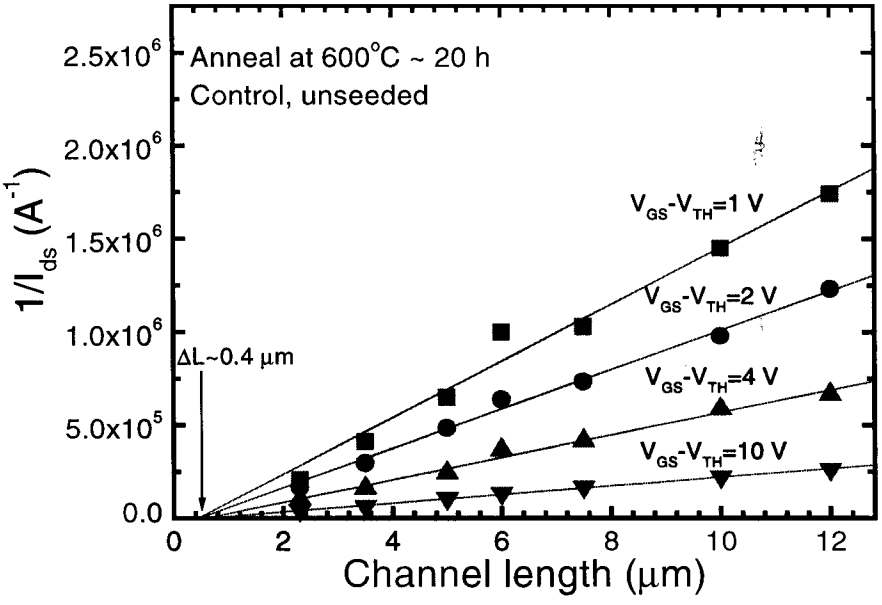


Figure 4.11. (a) Threshold voltage calculated from the x-intercept of the straight line fit to drain current vs. gate voltage at V_{DS} = 0.1V for different channel lengths in seeded and unseeded TFTs. (b) Field-effect mobility calculated at V_{DS}=0.1 V as a function of effective channel length in the seeded and unseeded TFTs.



(a)



(b)

Figure 4.12. Plot of $1/I_{DS}$ as a function drawn channel length for various values of $|V_{GS} - V_{TH}|$ to extract the effective channel length for (a) the laterally-seeded TFTs, and (b) unseeded, control TFTs. Note the straight line is fitted for the longer channel lengths as the method implicitly assumes fixed field-effect mobility, and V_{TH} is calculated for each channel length.

In the subsequent section, the effects of crystallization anneal temperature and length of anneal, effect of lateral crystallization done before or after the ion implantation step, effect of the growth temperature of the precursor *a*-Si:H film, and the effect of N_2O plasma treatment of the gate oxide will be studied. The process conditions to realize optimum laterally-seeded transistor performance will then become clear.

Effect of annealing temperature and time

We studied the effect of annealing temperature (samples 14 and 15 vs. 12 and 13, Table 4.2) on the grain size and hence on the electron mobility. The annealing temperature was changed to 625 °C, from the 600 °C used in the previous experiments. We found that the time taken to crystallize untreated films was reduced from ~20 h to ~5 h and the lateral crystal growth rate was enhanced. However, the mobility became smaller in the control samples (sample 15 vs. sample 13), probably because of an increase in nucleation density at higher anneal temperature, leading to smaller grains [2]. Fig. 4.13 shows the linear field-effect mobilities in the seeded and the unseeded transistors (samples 14 and 15) sample with the crystallization temperature of 625°C. The mobility in the control sample is ~25 cm^2/Vs when annealed at 625 °C, compared to ~35 cm^2/Vs when annealed at 600°C at L>5 μm. But the seeded TFTs have nearly the same mobility irrespective of the annealing temperature. The advantage of using higher temperature (625°C vs. 600°C) is that the annealing time is reduced but the disadvantage is that one has to use more expensive glass substrates (for display applications) with higher strain point temperatures [3].

A few of the samples were also annealed for longer times up to 60 h at 600 °C (sample 17, Table 4.2). These samples had gate oxide deposited by magnetron PECVD at 250 °C. The longer anneal did not result in any significant change in any of the TFTs characteristics, in fact the mobility of the TFTs reduced slightly to ~48 cm^2/Vs

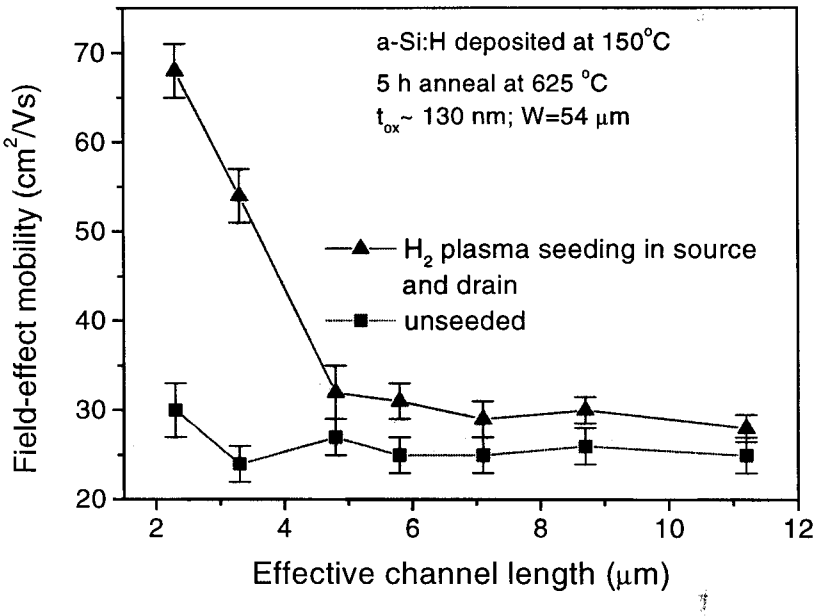


Figure 4.13. Linear regime mobility calculated at V_{DS} = 0.1 V as a function of channel length in seeded and unseeded TFTs. The crystallization temperature was 625°C.

compared to ~50 cm^2/Vs for the sample annealed for 20 h at 600 °C (sample 16 vs. 17, Table 4.2). The laterally-seeded TFT annealed for 20 h at 600 °C had mobility of ~50 cm^2/Vs when the gate oxide was deposited by magnetron PECVD, compared to ~72 cm^2/Vs for the laterally-seeded TFT with regular PECVD oxide. This reduction in mobility was also seen in case of the TFTs made in blanket crystallized films discussed in Section 4.4.2.

The subthreshold slope of the laterally-seeded TFTs was ~1.6 V/decade, and was the nearly the same for both magnetron PECVD or regular PECVD oxide. Both, the laterally-seeded and control TFTs, with the magnetron oxide have fairly high threshold voltages of ~2.5 V irrespective of the annealing time, while the TFTs with the PECVD oxide (sample 12, Table 4.1) have fairly negative threshold voltage of -4 V at L = 2 μm. However, the opposite effect was seen in the case of the low-temperature TFTs in Section 4.4.2, with the threshold voltage shift being positive and subthreshold slope

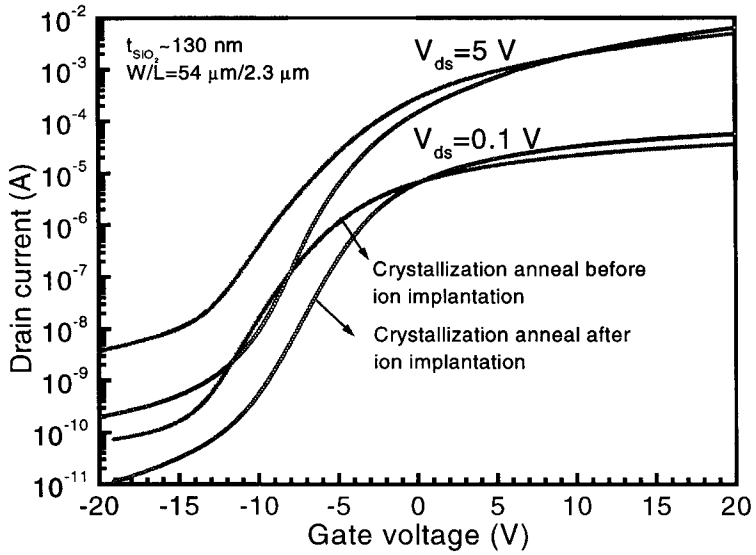


Figure 4.14. Drain current vs. gate voltage of laterally-seeded TFTs with lateral crystallization done before and after the source/drain ion implantation step (samples 18 and 12, Table 4.2).

decreasing when magnetron PECVD oxide was used instead of regular PECVD oxide. The reason for this discrepancy is not clear. But, the one significant difference between the two types of TFTs is that, the gate oxide was deposited after the *a*-Si:H film was completely crystallized in case of TFTs in Section 4.4.2, while in this case the crystallization anneal was done after the gate oxide was deposited.

Effect of lateral crystallization before source/drain ion implantation

The effect of crystallization anneal before ion implantation (samples 18 and 19, Table 4.2) on the performance of the TFTs was also examined. In addition to increasing the number of annealing steps, this did not lead to as large an increase in the mobility of the seeded transistor as in the case of crystallization after the ion implantation. For example, the field-effect mobility was reduced to ~44 cm^2/Vs at a channel length of ~2 μm compared to ~72 cm^2/Vs in the single-step anneal (sample 18 vs. 12, Table 4.2), for annealing at 600 °C. The leakage current was also higher with the ON/OFF current ratio

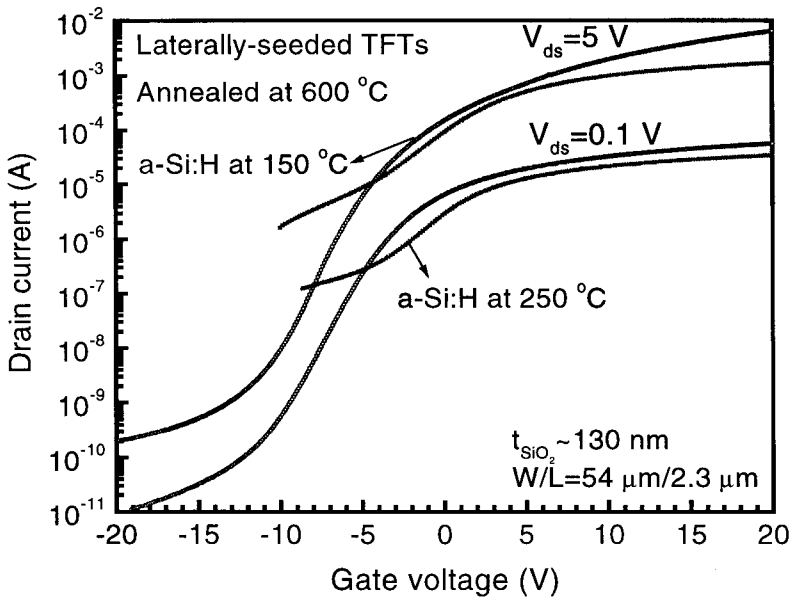


Figure 4.15. Drain current vs. drain voltage for the laterally-seeded TFTs from crystallization at 600 °C of *a*-Si:H films deposited at 250 °C and 150 °C (samples 20 and 12).

being ~10^6 for TFTs with lateral crystallization anneal done before the ion implantation, compared to ~10^7 for the single-step anneal TFTs (Fig. 4.14). The source/drain ion implantation amorphizes the exposed regions. But its effect on the preexisting crystalline grains in the channel during the subsequent implant damage anneal is not clear.

Effect of growth temperature of *a*-Si:H

The deposition temperature of the precursor *a*-Si:H film also affects the performance of the laterally-seeded TFTs. When the growth temperature of the *a*-Si:H film was changed to 250 °C (samples 20 and 21 Table 4.2) from 150 °C (samples 12 and 13, Table 4.2), the amount of hydrogen in the film was reduced and the incubation time for thermal generation of seed nuclei also dropped [4, 19]. During the crystallization after the hydrogen-plasma seeding in the exposed source and drain regions, spontaneous

nucleation might occur in the unexposed channel regions before the lateral crystal growth from the seeded regions can crystallize the whole channel. Therefore, the grain size in the channel region may not be enhanced. This was indeed the case, and the field-effect mobility of the TFTs was ~28 cm^2/Vs for both the laterally-seeded sample and the unseeded control sample for all channel lengths compared to the nearly two-fold increase in field-effect mobility in case laterally-seeded TFTs made from *a*-Si:H deposited at 150 °C (Fig. 4.15). Hence, the deposition temperature of the precursor *a*-Si:H film has to be chosen such that, the incubation time for nucleation of seeds is the longest, for the lateral seeding to work effectively.

Effect of N_2O plasma treatment on PECVD gate oxide

It had been reported earlier that N_2O plasma treatment of the gate oxide leads to improvement in the interface-state density and reliability of the oxide due to increased nitrogen at the poly-Si/SiO_2 interface, and hence leads to improved performance of the TFTs [26]. The N_2O plasma treatment, in our experiments, was optimized to minimize the interface-state density (Fig. 4.16 (a)), as inferred from C-V measurement of MOS capacitors (see Section 7.4.2 for details on C-V measurement). As the data indicates, the N_2O plasma treatment did lead to significant change in the interface-trap density. Laterally-seeded and unseeded control TFTs were then fabricated with the gate oxide treated with a N_2O plasma treatment at 75 W for 30 min directly after deposition of the gate oxide (sample 22, Table 4.2). The field-effect mobility of the laterally-seeded TFTs was ~74 cm^2/Vs with the N_2O plasma treatment, which was the same as that obtained from TFTs without the N_2O plasma treatment (sample 12, Table 4.2). But, the leakage current in the N_2O-plasma-treated samples increased by nearly three orders of magnitude and the ON/OFF current ratio was only ~10^4 compared to ~10^7 without the N_2O plasma treatment of the gate oxide for the laterally-seeded TFTs (Fig. 4.16 (b)).

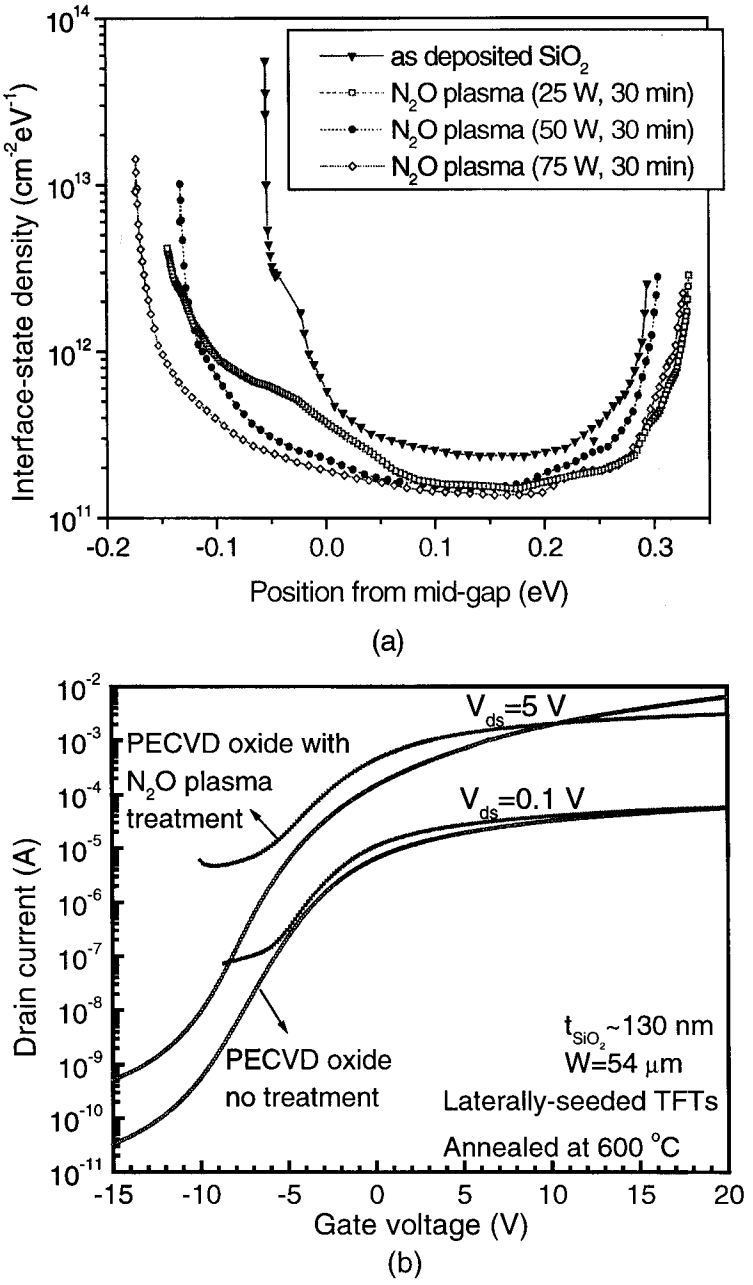


Figure 4.16. Effect of N_2O plasma treatment on PECVD gate oxide; (a) Interface-state density inferred from C-V measurements of MOS capacitors for different N_2O plasma treatments, and (b) drain current vs. gate voltage for the laterally-seeded TFTs with and without N_2O plasma treatment a 75 W for 30 min of the PECVD gate oxide (sample 22 and 12, Table 4.2).

The reason for this increase in leakage current of the TFTs, and lack of field-effect mobility improvement in contrast to previous reported work due the N_2O plasma treatment is not clear.

4.6 SUMMARY

TFTs with excellent characteristics with both high and low thermal budgets were fabricated in polycrystalline silicon films, which were crystallized from *a*-Si:H using a hydrogen-plasma-seeding technique. The method is very attractive for high performance circuits on large-area glass substrates. Selective seeding by hydrogen plasma treatment can be applied to growing crystal grains laterally from the seeded regions into the unexposed regions. This produces large grains in the lateral growth region. We have fabricated poly-Si TFTs with mobilities as high as 75 cm^2/Vs at a maximum process temperature of 600 °C, utilizing this lateral crystallization effect without laser processing. The dominant factor in determining the field-effect mobility in all cases was the grain size of the polycrystalline silicon, and not the gate oxide growth/deposition conditions. Significant increases in mobility are observed when the grain size is on order of the channel length. However, the gate oxide plays an important role in determining the subthreshold slope and the leakage current of the TFTs.

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Chapter 5

INTEGRATED AMORPHOUS AND POLYCRYSTALLINE SILICON TRANSISTORS

5.1 INTRODUCTION

For large area electronics, such as flat panel displays, there has been considerable interest to integrate both amorphous silicon (*a*-Si:H) thin-film transistors (TFTs), for low leakage in the OFF state, and polycrystalline silicon (poly-Si, polysilicon) TFTs, for high drive currents, on the same substrate. This might be done to integrate polysilicon drivers in flat panel displays using *a*-Si:H TFTs in pixels. In this chapter we describe the use of selective crystallization using hydrogen plasma treatment of *a*-Si:H, discussed in chapter 3, to achieve this aim.

Integration of *a*-Si:H and poly-Si TFTs is difficult for three reasons. First, the conventional *a*-Si:H TFT fabrication process is a low-temperature process (<300 °C) [1], while the poly-Si TFT fabrication requires a 600 °C anneal starting from *a*-Si:H if laser processing is not used. Second, one would like to deposit only a single Si layer instead of two (*a*-Si:H and poly-Si) to save cost, and third, the structure and fabrication sequence of conventional *a*-Si:H TFTs and poly-Si TFTs are very different (bottom gate vs. top gate process), so that few process steps can be shared.

Various techniques have been tried to integrate *a*-Si:H and poly-Si TFTs on the same substrate. One method is excimer laser annealing to crystallize the chemical vapor deposited (CVD) deposited *a*-Si selectively and fabricate bottom-gate transistors in both the amorphous and polycrystalline regions [2-4]. Another method uses crystallization of a thin (20 nm) *a*-Si:H layer deposited by plasma-enhanced CVD (PECVD) using Ar and XeCl (300 mJ/cm^2) lasers, and subsequent deposition of a thick (200 nm) *a*-Si:H layer and patterning the *a*-Si:H to realize staggered layers of poly-Si and *a*-Si:H. Bottom-gate TFTs were then fabricated in the two regions [5]. Both of these methods involve laser processing which has relatively low throughput and also can lead to variable film quality due to variations in laser beam power and width. Also, the latter method involves fabrication of TFTs in staggered layers, i.e., the transistors are not in a single silicon layer.

Our work is based on the masking of hydrogen plasma seeding treatment of *a*-Si:H and subsequent crystallization anneal as discussed in Section 3.3.7. In this chapter, the method for integrating *a*-Si:H and poly-Si transistors together starting with a single Si layer is described. The approach shares all fabrication steps between the two transistors, except for the one initial step, which defines the regions to be selectively crystallized. The fabrication involves no laser processing.

In this process we have three key steps:

1) Selective hydrogen-plasma-enhanced crystallization of *a*-Si:H.

2) SiN_x cap layer on the *a*-Si:H region to prevent the hydrogen-plasma-induced nucleation and also to reduce hydrogen effusion from the amorphous region during subsequent annealing at 600 °C.

3) Rehydrogenation of the amorphous region after the 600 °C anneal to obtain device quality *a*-Si:H.

5.2 EXPERIMENTAL PROCEDURE AND MEASUREMENT TECHNIQUES

5.2.1 Sample growth and selective crystallization

Hydrogenated amorphous silicon (*a*-Si:H) films of 150 nm thickness were deposited by plasma-enhanced chemical vapor deposition (PECVD) using pure silane, on Corning 1737 glass substrates at a substrate temperature (set point) of 150 or 250 °C and RF power of ~0.02 W/cm^2 in the i-chamber of the S900 plasma deposition system (see Appendix A for growth sequence). Our usual process for growth of *a*-Si:H for TFT fabrication is the same but the substrate temperature is 250 °C [1]. We lowered the substrate temperature to 150 °C to raise the hydrogen content of the *a*-Si:H to 15 at. %, which facilitates the subsequent anneal [6, 7].

As in Section 3.3.7, the principle of area-selective crystallization is to protect selected areas of the *a*-Si:H precursor film from the plasma exposure by masking [6, 8, 9]. A 120 nm thick SiN_X mask film was deposited by PECVD in the n-chamber of the S900 multi-chamber plasma deposition system using SiH_4, H_2 and NH_3, at a substrate temperature (set point) of 200 °C and RF power density of ~ 0.09 W/cm^2 (see Appendix A for growth recipe) [10], on a 150 nm thick *a*-Si:H precursor layer deposited at 150 °C on Corning 1737 glass substrate. The SiN_X was patterned by etching in dilute hydrofluoric acid (HF). To promote nucleation, the films were then exposed to atomic hydrogen in Plasma Therm RIE chamber at room temperature. The RF power density was 0.8 W/cm^2, RF frequency was 13.56 MHz, the chamber pressure was 50 mtorr, and the exposure time was 60 min. The sample was placed on a 125-mm Si wafer during the exposure to minimize aluminum contamination due to aluminum sputtered from the electrode onto the sample surface as described previously in Section 3.4. The films were then crystallized by annealing in a furnace at 600 °C in N_2. The crystallization process

was monitored by UV reflectance measurement [11]. The patterned SiN_x film prevents nucleation and caps the *a*-Si regions to minimize the loss of hydrogen during the anneal. After ~4 h of anneal the portion of the *a*-Si:H film that had been exposed to the hydrogen plasma was completely crystallized (confirmed by UV reflectance measurement), while the unexposed regions were still amorphous. The SiN_x-cap layer was then removed by etching in dilute HF. Thus both amorphous and polycrystalline silicon were obtained in a single silicon layer [6, 8].

5.2.2 Measurement techniques

Infrared transmission

For this work, we needed to determine the hydrogen content in the amorphous films after the high-temperature (600 °C) anneal and the effect of subsequent rehydrogenation on the properties of the amorphous silicon. The net hydrogen content in the *a*-Si:H films can be easily determined from the integrated absorption coefficient (α) at 630 cm^{-1} which arises due to wagging modes of Si-H and $Si-H_2$ bonds [12-14] (see Appendix B for details).

For infrared transmission measurement, *a*-Si:H films are usually deposited on single-crystal Si substrates as discussed in Section 3.2.1 and Appendix B, as glass substrates are not transparent in the infrared. If, however, the *a*-Si:H film is deposited directly on the single-crystal Si substrate, during the 4 h 600 °C anneal to selectively crystallize the amorphous silicon, even the amorphous silicon not exposed to hydrogen plasma will crystallize. The single-crystal Si acts as the seed for nucleation during the anneal, thereby reducing the crystallization time. Hence, 250-nm thick *a*-Si:H deposited on SiO_2 covered Si substrates were used for the transmission measurements. The thickness of the SiO_2 was ~200 nm to prevent peeling of the film during the anneal (see Section 3.2.1 for details on techniques to minimize peeling of *a*-Si:H films during

anneal). The transmittance of *a*-Si:H/SiO_2/Si (T_1) sample and the transmittance of the SiO_2/Si substrate (T_2) were measured, and the transmittance of the *a*-Si:H film was then determined from T_1/T_2.

Absorption coefficient of *a*-Si:H

To determine the optical absorption and optical bandgap (Tauc gap) of the films, optical transmission of *a*-Si:H films deposited on glass substrates was measured. A Hitachi H-3410 spectrophotometer was used for the optical transmission measurement, and the range of wavelengths measured was from 300-2500 nm. The absorption coefficient (α) in the strongly absorbing region, was then determined by deconvoluting the transmission data following the Swanepoel method [15]. See Appendix B for details.

The optical transmission measurement, however, cannot be used to determine the absorption coefficient with any accuracy when it is very small, i.e. in the weakly absorbing or transparent regions. Therefore photo-thermal deflection spectroscopy (PDS) was used to measure small α (see Appendix B for more explanation). In order to obtain the absorption coefficient from energies of ~1 eV to over 2 eV, the data from these optical transmission and PDS were combined. The absorption coefficient at low photon energies gives us information about defect states in the mobility-gap of the material. A large number of defect states corresponding to a large sub-bandgap absorption means a poor device quality material.

Dark conductivity

Current flow in amorphous layers can occur through either carrier conduction in the extended states of the *a*-Si:H film or hopping conduction from one defect site to the other. To determine the conduction mechanism and hence determine the electrical characteristics of the layer, dark conductivity measurement was performed. This was done by thermally evaporating coplanar aluminum contacts onto the thin film and

measuring the current for applied bias at given temperature. A straight line was fit to the logarithmic plot of conductivity vs. 1/kT to obtain the activation energy of the material's conductivity. See Appendix B for further details on the technique.

5.3 HYDROGEN EFFUSION DURING ANNEAL AND REHYDROGENATION

A critical issue for the fabrication of *a*-Si:H TFTs in such a process is the loss of hydrogen from the amorphous regions during the 600 °C anneal to crystallize the plasma exposed regions. Loss of hydrogen from the layer leads to increase in number of unpassivated dangling bonds. This results in higher defect state density and hence poor devices. The SiN_x layer is a good diffusion barrier, but nevertheless most of the hydrogen is lost. In this section, we examine the loss of hydrogen from the *a*-Si:H layers during the high-temperature anneal and ways to put it back.

The atomic hydrogen content in the films was deduced from the integrated infrared absorption near 630 cm^{-1}, which is due to the Si-H and $Si-H_2$ wagging modes [14]. A conversion factor of $2.1x10^{19}$ $cm^{-2}/5x10^{22}$ cm^{-3} was used to estimate the hydrogen content in the films in atomic % [16]. The atomic hydrogen content in the as-grown *a*-Si:H was ~15 at. %, which after annealing had dropped to about ~0.3 at. % (Fig. 5.1). A similar loss of hydrogen is evident in the Si-H stretching mode absorption at ~2000 cm^{-1} (Fig. 5.2). The midgap defect state density increased from < $6x10^{17}$ cm^{-3} to ~$4x10^{19}$ cm^{-3} after the anneal, as deduced from the absorption coefficient at 1.3 eV measured by photo-thermal deflection spectroscopy (PDS) (Fig. 5.3) [17]. The dangling bond densities as measured by PDS is rather high in this case as the films used were only 300 nm thick and the measurement is sensitive to presence of surface states as discussed in Appendix B. The *a*-Si:H top-gate transistors made with this film had electron mobilities of only 0.01 cm^2/Vs with an ON/OFF current ratio of only ~10^4.

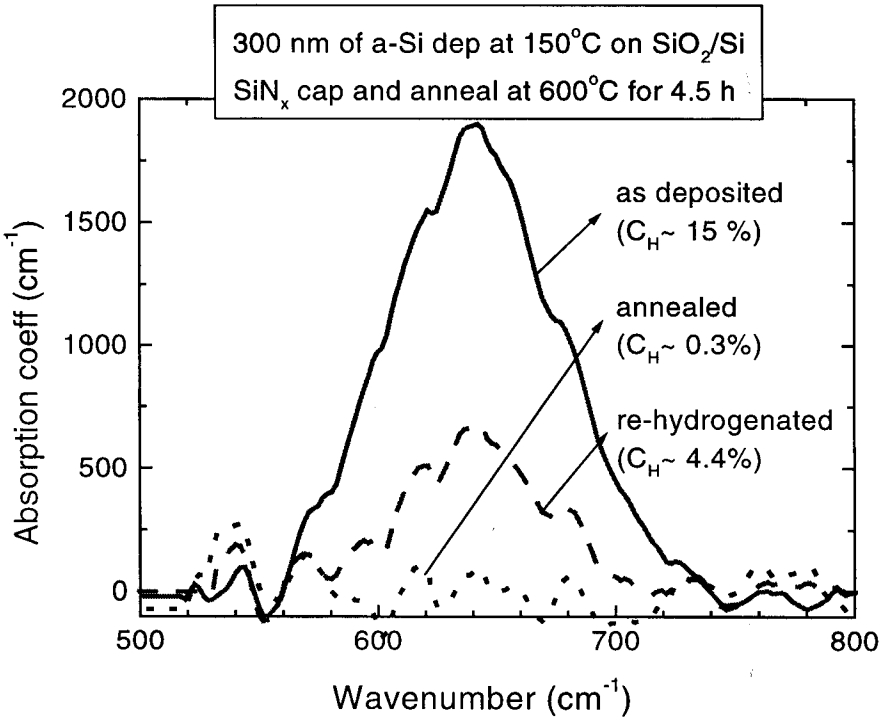


Figure 5.1. Absorption coefficient at 630 cm^{-1} corresponding to wagging modes of Si-H and Si-H_2 bonds, which is a measure of net hydrogen in the *a*-Si:H films. The effect of high-temperature anneal and subsequent rehydrogenation on the hydrogen content in the film is highlighted. Growth temperature of precursor *a*-Si:H film was 150 °C.

Rehydrogenation is necessary to reduce the defect state density in both the amorphous and polycrystalline regions of the film. This was done after stripping the patterned SiN_x-cap layer with dilute HF (1:10 deionized water). The hydrogen plasma conditions were chosen such that hydrogen abstraction and etching are minimal and hydrogen insertion is the dominant mechanism, knowing that hydrogen ion energy determines the dominant reaction to a certain extent (Section 3.4.3). In a plasma deposition system the sample is on the grounded electrode with the chamber walls also grounded, while the RF power is fed to the other electrode with a smaller area. Since the DC voltage across the sheath (which is the accelerating voltage for the ions), is inversely proportional to the electrode areas, the ion energies in a plasma deposition

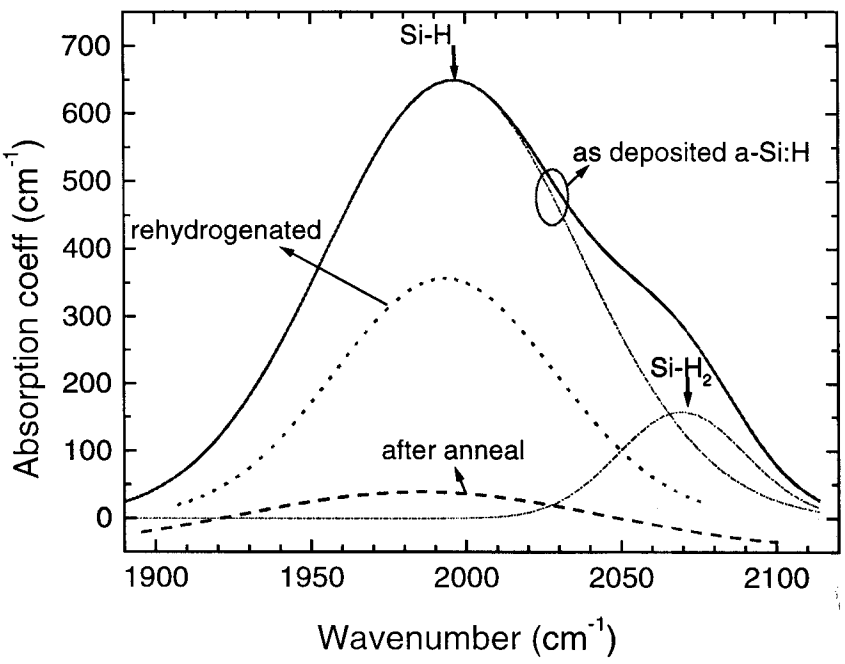


Figure 5.2. Infrared absorption spectrum of the *a*-Si:H films around 2000 cm^{-1} (Si-H stretch vibration) to illustrating that rehydrogenation results in increase of Si-H rather than $Si-H_2$. The spectrum of the as-grown film is decomposed into the Si-H and $Si-H_2$ components. Growth temperature of precursor *a*-Si:H film was 150 °C.

system are lower compared to RIE system, wherein the sample sits on the powered electrode with the smaller area (see chapter 7 for more details about plasma physics). The rehydrogenation was therefore done in the i-chamber of the S900 multi-chamber plasma deposition system (described previously in Section 3.2.1), instead of the RIE system (used earlier for the hydrogen plasma seeding treatment) so as to reduce the hydrogen ion energies. The rehydrogenation was done in the i-chamber, as it is the cleanest of the three chambers. As we discussed previously in Section 4.3.1, the hydrogenation was done at an elevated substrate temperature (set point) of 350 °C so that hydrogen diffuses throughout the bulk of the film. The plasma power density was lowered to ~0.2 W/cm^2 and the chamber pressure was increased to 1 torr, so that the hydrogen ion energies are small (<30 eV), as compared to 0.8 W/cm^2 and 50 mtorr

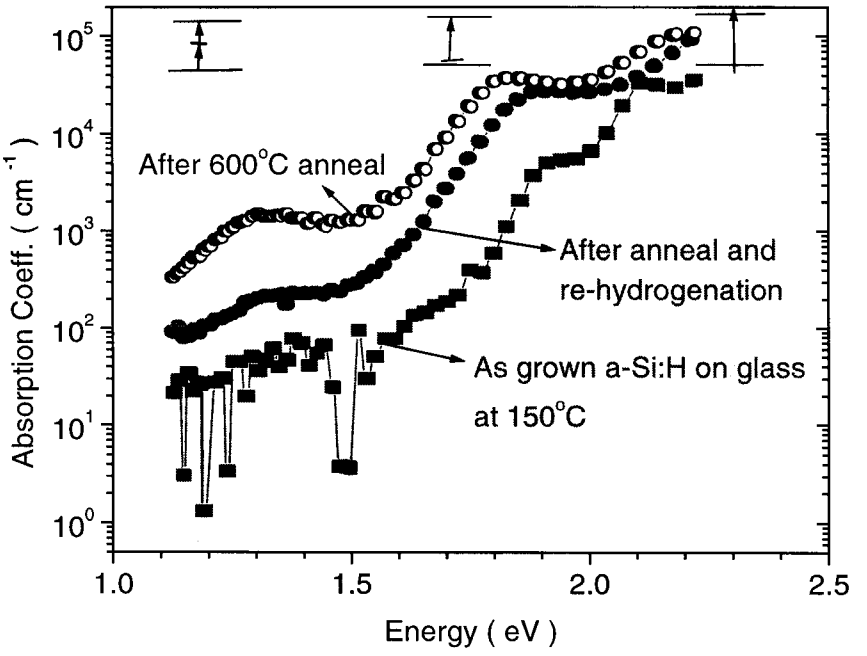


Figure 5.3. Photo-thermal deflection spectra of the optical absorption coefficient of *a*-Si:H films in the as-deposited, annealed with SiN_x cap layer at 600 °C, and re-hydrogenated states. The inset shows the relevant transitions at different energies in a band diagram. Growth temperature of precursor *a*-Si:H film was 150 °C.

resulting in hydrogen ion energy of ~500 eV during the hydrogen-plasma-seeding treatment. We will discuss the rehydrogenation in further detail later in Section 5.4.3.

Rehydrogenation for 75 min increased the hydrogen content of the film to ~4.4 at. % as measured by the IR absorption at 630 cm^{-1} (Fig. 5.1). The increase in hydrogen content resulted in the passivation of the Si dangling bonds to ~$6x10^{18}$ cm^{-3} and therefore led to a decrease in sub-gap absorption to as can be seen in Fig. 5.3.

Note, however, that hydrogen content in the rehydrogenated films was not raised as far as the initial level of ~15 at. %. This might be partly due to fact that the rehydrogenation was performed at higher temperature (~350 °C) compared to growth temperature of 150 °C of the initial precursor *a*-Si:H film. The hydrogen content in the film is a strong function (nearly linear dependence) of the growth temperature of the *a*-

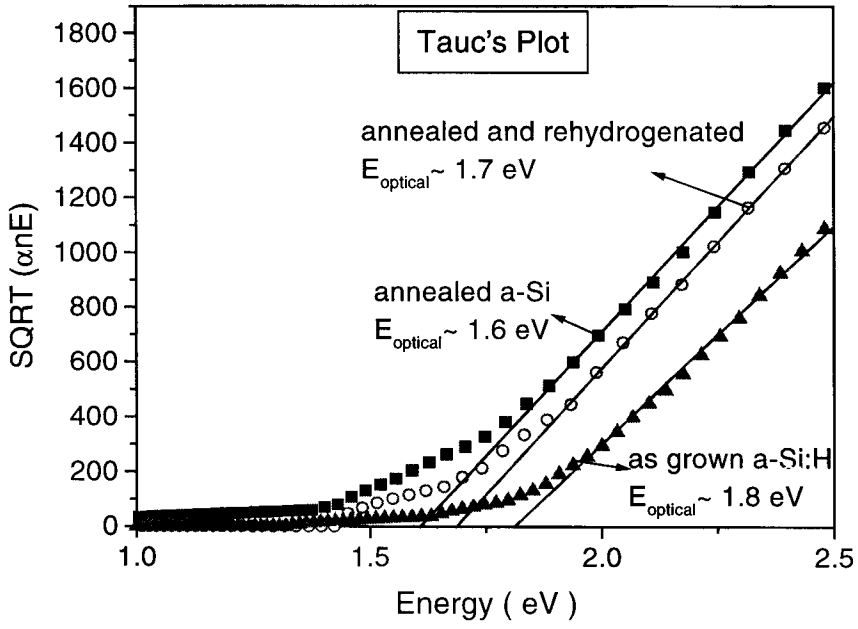


Figure 5.4. Tauc's plot of $(\alpha nE)^{1/2}$ vs. photon energy of as-grown, annealed, and re-hydrogenated films as determined from optical transmission data.

Si:H as we saw earlier in Section 3.3.4. The amount of hydrogen in the film is determined by the growth temperature of the film with *a*-Si:H grown at 350 °C having a hydrogen content of ~8 at. %. But the hydrogen content in the rehydrogenated films with rehydrogenation done at ~350 °C is considerably lower than hydrogen content in *a*-Si:H deposited at the same temperature. We are not sure if this is a kinetics problem, related to difficulty in getting hydrogen into the film, or a more fundamental problem, due to the Si dangling bonds sites reconstructing in some way after the high-temperature anneal so that the amount of hydrogen that can be accommodated in the film is lowered.

Rehydrogenation, in addition to increasing the hydrogen content of the *a*-Si:H, improves the electrical characteristics of the film. Rehydrogenation is expected to improve its stability as the hydrogen predominantly bonds in the form of Si-H, in

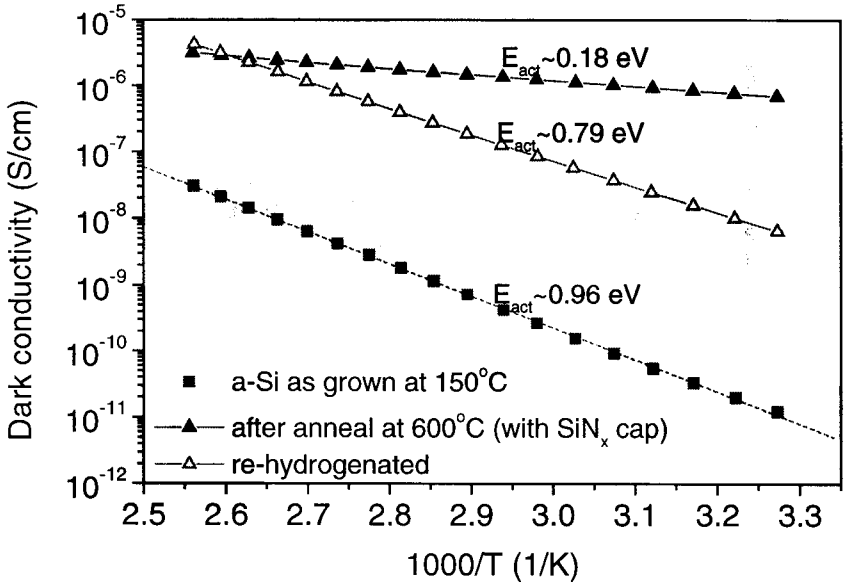


Figure 5.5. Dark conductivity measurement of the *a*-Si:H samples. A high activation energy reflects conduction above the mobility edge of low-defect density *a*-Si:H. Low activation energies reflect activated hopping through a high density of defect states.

contrast to the as-grown *a*-Si:H film deposited at 150 °C, which had a considerable Si-H_2 content (Fig. 5.2). The Tauc optical gaps (E_{opt}) calculated from the optical transmission spectra above the band-gap show that the E_{opt} drops to 1.6 eV from 1.8 eV during annealing and that rehydrogenation raises E_{opt} to 1.7 eV (Fig. 5.4). Dark conductivity (σ_d) measurement shows that σ_d of the *a*-Si:H film increases after the anneal and that σ_d has a low thermal activation energies, indicating conduction through defect states (Fig. 5.5). Rehydrogenation brings the activation energy of the film closer to $E_g/2$ indicating a reduced defect density. But σ_d still is not as small as that of the as-grown *a*-Si:H and suggests conduction in a heterogeneous material, which may explain the slightly higher leakage currents of the transistors (Fig. 5.14). Overall, the data show that the capped *a*-Si:H film remains largely amorphous after the anneal, and that rehydrogenation results in *a*-Si:H film which may be suitable for devices.

5.4 TRANSISTOR PERFORMANCE AND OPTIMIZATION

5.4.1 Fabrication details

Non-self-aligned n-channel top-gate transistors were fabricated in both the amorphous and polycrystalline silicon regions. Fig. 5.6 shows the process sequence of the transistor fabrication. A 120-nm thick SiN_X was deposited by PECVD at 200 °C (set point) as described earlier in Section 5.2.1, on a 150-nm thick *a*-Si:H layer deposited at 150 °C on Corning 1737 glass substrate. After patterning of the SiN_X by etching with dilute HF (1:10 deionized water), the sample was then exposed to the RF hydrogen plasma in the RIE system as described earlier. Subsequent annealing was done in a furnace at a temperature of 600°C in a N_2 ambient with the SiN_x cap selected *a*-Si regions. After ~4 h of anneal the region exposed to hydrogen plasma was completely crystallized, while the unexposed areas remain amorphous. The remaining SiN_x mask layer was then removed by etching in dilute HF, leaving behind both amorphous and polycrystalline silicon in a single silicon layer.

Rehydrogenation of the film is essential to improve the TFT performance as discussed earlier. This was done by exposing the sample to hydrogen plasma at the RF power of 0.2 W/cm^2 at substrate temperature of 350 °C (set point) and pressure of 1 torr for ~75 min as discussed in Section 5.3. Details on the rehydrogenation and its effect on the amorphous silicon TFT characteristics will be discussed subsequently.

After the rehydrogenation step, ~50 nm of n^+ microcrystalline (μc-Si:H) silicon was deposited by PECVD (in the p-chamber of the S900 multi-chamber PECVD system) using SiH_4, H_2 and PH_3, at a pressure of 900 mtorr, RF power of ~0.3 W/cm^2, and at a substrate temperature of 340 °C [18] (Fig. 5.6 (a)), see Appendix A for the growth recipe. Device islands were then defined by dry etching in a SF_6 and CCl_2F_2 plasma at

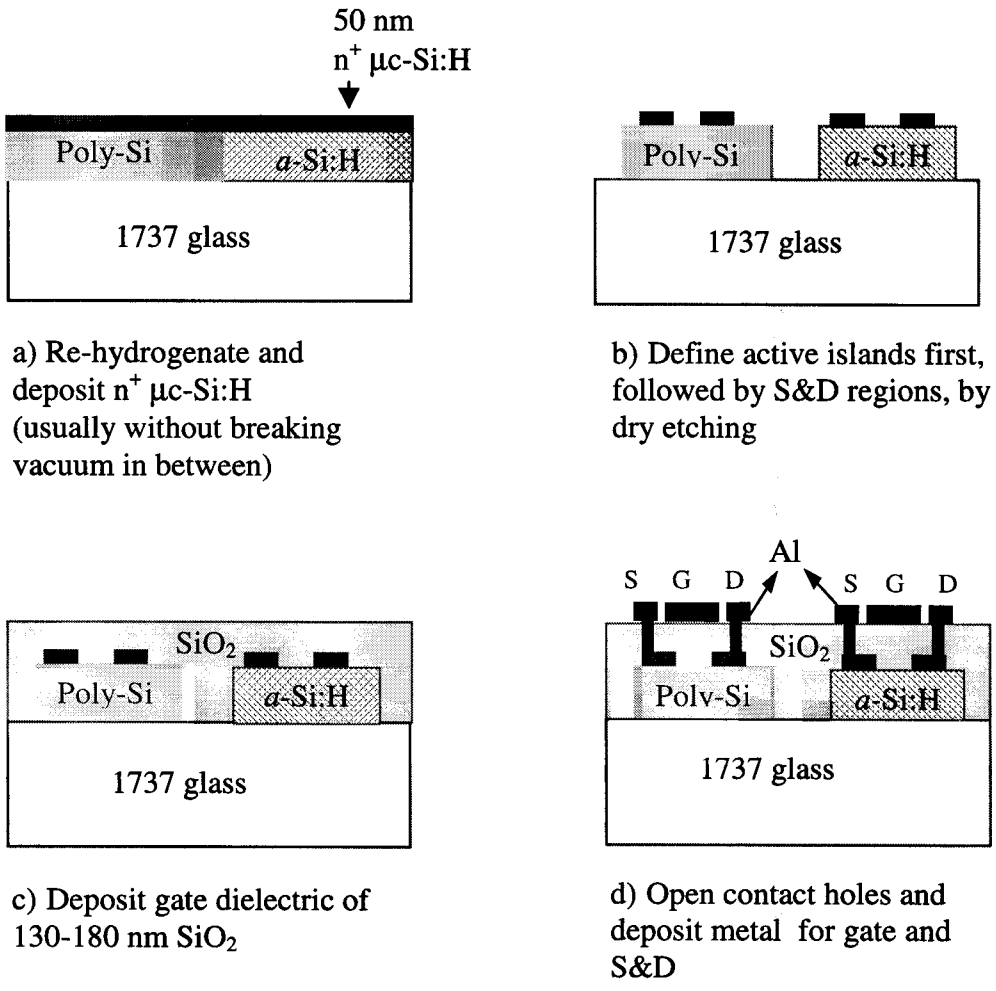
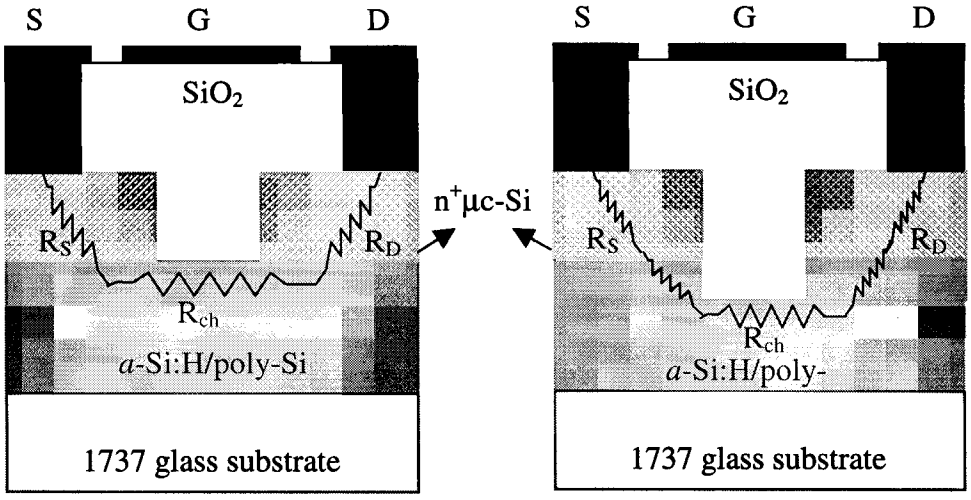


Figure 5.6. Amorphous and polycrystalline silicon top-gate non-self-aligned transistor fabrication steps. The steps after the selective crystallization step are shown. The process required four masks for the TFT fabrication and an additional mask to define the polycrystalline and amorphous regions.



a) Non-coplanar S/D contacts resulting in source/drain resistance

b) Overetching during channel definition leading to increased source/drain resistance

Figure 5.7. Exaggerated cross-section of the *a*-Si:H/poly-Si TFT showing the (a) effect of non-coplanar source/drain contacts on source/drain resistance, and (b) effect of overetch during channel definition on source/drain resistance.

an RF power of ~0.3 W/cm^2 and pressure of 100 mtorr (similar to the etch recipe used to etch device islands in the self-aligned TFT process discussed in Section 4.3.2). The future channel regions were defined by dry etching just the n^+ μc-Si:H layer in a separate etching step using a CCl_2F_2 and O_2 plasma at an RF power of 0.08 W/cm^2 and pressure of 100 mtorr with CCl_2F_2 flow rate of 9 sccm and O_2 flow rate of 5 sccm (Fig. 5.6 (b)). The n^+ μc-Si:H and device-island etching were both done in the Plasma Technology RIE chamber.

During the etching step, laser interferometry (see Section 4.3.1) is used to detect endpoint and accurately determine the thickness of the layer etched. But during the channel-definition step, the layer (n^+ μc-Si) thickness to be etched is only ~50 nm and we need to stop when the intrinsic layer is reached. The laser interferometry technique is powerful when the layer to be etched is silicon on an insulator, so that endpoint can

be detected once the signal is flat with no interference fringes. The technique is also helpful if the Si layer to be etched is at least 80-nm thick, as the difference between two maxima or minima ($\Delta d = \lambda/2n$) corresponds to Si thickness of ~80 nm for He-Ne laser. Due to these reasons, the sample can get overetched during the channel-definition step resulting in damage at the channel surface and therefore increased source/drain resistance (Fig. 5.7). Some variations in the process sequence were tried to minimize this etching damage of the channel as discussed later in Section 5.4.2. The sample was then rinsed first with sulfuric acid and hydrogen peroxide solution and then dilute hydrofluoric (HF) acid to clean the surface. This also helps in smoothening the surface as rinsing in sulfuric acid peroxide mixture results in a thin oxide (~5 nm) which is subsequently etched during the HF rinse. The oxide also getters any impurities (like metals) from the sample surface and hence reduces the amount of contaminants at the channel surface.

The gate dielectric, 130-180 nm of SiN_x or SiO_2, was then deposited by PECVD at a substrate temperature of about 250 °C (Fig. 5.6(c)). Care was taken to change the recipes such that all processing after rehydrogenation was done at lower temperature than the rehydrogenation temperature so that no loss of hydrogen again occurs during the subsequent processing. The SiO_2 was deposited in the plasma deposition system (Plasma Therm) with the deposition conditions and the chamber preparation steps being that same as that described previously in Section 4.4.1 to fabricate the low-temperature self-aligned TFTs. The SiN_x was deposited in the n-chamber of the S900 multi-chamber PECVD system (see Appendix A for growth sequence). The growth temperature was 300 °C with a SiH_4 flow of 13 sccm, NH_3 flow of 130 sccm, and H_2 flow of 143 sccm. The chamber pressure was 500 mtorr and the RF power density was ~0.02 W/cm^2 during the SiN_x deposition. The typical growth temperature of SiN_x used as gate

dielectric for *a*-Si:H TFTs is ~350 °C [1, 19]. The deposition temperature was lowered in this case to ensure that no loss of hydrogen occurs due to processing done at temperature higher than or equal to the rehydrogenation temperature. Due to the lowered growth temperature the quality of the nitride films degrades due to increased porosity leading to poor electrical characteristics like gate leakage and breakdown voltage [20]. Hydrogen (50 %) was added during growth to improve the quality of the nitride layer [20].

Contact holes were then made to the source and drain regions by etching in dilute HF and aluminum was evaporated and patterned to form the gate, and source and drain contacts (Fig. 5.6(d)). The samples were then annealed at ~225 °C in forming gas (10% H_2 in N_2) for ~90 s in AGA associates rapid thermal annealer (RTA) to reduce contact resistance. Note this is not a self-aligned process. The process is similar to the inverted-staggered process typically used for *a*-Si:H TFTs in active matrix liquid crystal displays.

5.4.2 Techniques to minimize channel–etch damage

The transistor fabrication process described above involves a channel-definition step during which the deposited ~50 nm of n^+ μc-Si is etched to define the source/drain regions. Due to the inherent limitations of the laser interferometry as discussed previously overetching occurs and the etch leads to damage at the channel surface which is detrimental to both amorphous and polycrystalline transistor performance. The overetch also leads to increased source and drain resistance as can be seen from Fig. 5.9 and thereby degrades the performance of the TFTs, especially the polysilicon TFTs. Variations in the process flow were therefore tried to reduce this channel-etch damage as described next.

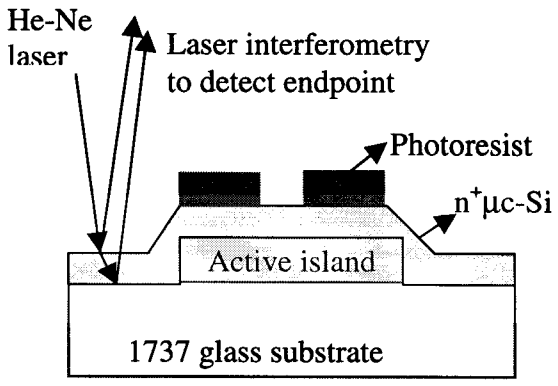


Figure 5.8. Schematic cross-section of sample during channel definition etch of n^+ μc-Si with the n^+ μc-Si deposited after the active islands (*a*-Si:H/poly-Si) were patterned.

n^+ μc-Si after active island patterning

The only change in this process compared to the regular process described earlier in Section 5.4.1, is that in this case the active islands were patterned after the rehydrogenation step before the n^+ μc-Si deposition step as seen in Fig. 5.8. During the channel-definition step involving the etch of n^+ μc-Si, laser interferometry can be used to accurately determine the end of etching (as the etch involves Si on insulator). This ensures that overetch and etch-related damage is minimized. Care should be taken, however, to clean the sample with dilute HF prior to the n^+ μc-Si deposition to ensure good electrical contact between the active layer and the n^+ μc-Si layer. This was not so crucial in the standard process as the n^+ μc-Si was deposited directly on the unpatterned active film after the rehydrogenation step without breaking vacuum. This variation still involves exposure of the channel surface to the plasma during the etching, but better endpoint detection ensures reduced damage and a more repeatable and hence a robust process. The effect on the TFT characteristics is primarily the reduction of the

source/drain resistance from 200-300 kΩ to <100 kΩ for polysilicon TFTs with channel width of ~200 μm.

n^+ μc-Si before active layer deposition

The process sequence is shown in Fig. 5.9. This process does not involve any etch step during which the channel surface is exposed during the etch. First ~50 nm of n^+ μc-Si is deposited on annealed Corning 1737 glass substrate and patterned by dry etching in CCl_2F_2/O_2 plasma (Fig 5.9(a)). Laser interferometry can be used to determine exact endpoint of etching as it involves etching of Si on an insulator. Next ~150 nm of intrinsic *a*-Si:H is deposited by PECVD at 150 °C and then ~120 nm of SiN_x cap layer is deposited at 200 °C. The SiN_x is patterned and the sample exposed to H_2 plasma to selectively seed the *a*-Si:H layer. The sample is then annealed at 600 °C to selectively crystallize the film (Fig. 5.9(c)). Active islands are patterned (again etching involves Si on insulator) and endpoint is detected accurately by laser interferometry (Fig. 5.9(d)). This is followed by gate nitride deposition, etching contact holes to the source/drain, and aluminum contact definition (Fig. 5.9(e)). Although the processing was easy and did not result in any channel-etch damage, the transistor characteristics were poor. The polysilicon TFT could not be turned OFF. The drain/source junction was extremely leaky and the channel was effectively resistor-like, with no gate control. This might be due to diffusion of dopants from the n^+ μc-Si layer into the intrinsic channel layer during the 600-°C crystallization anneal. For this reason almost all the TFTs were fabricated using the standard process with the variation described in the preceding section (n^+ μc-Si deposition after active-island patterning).

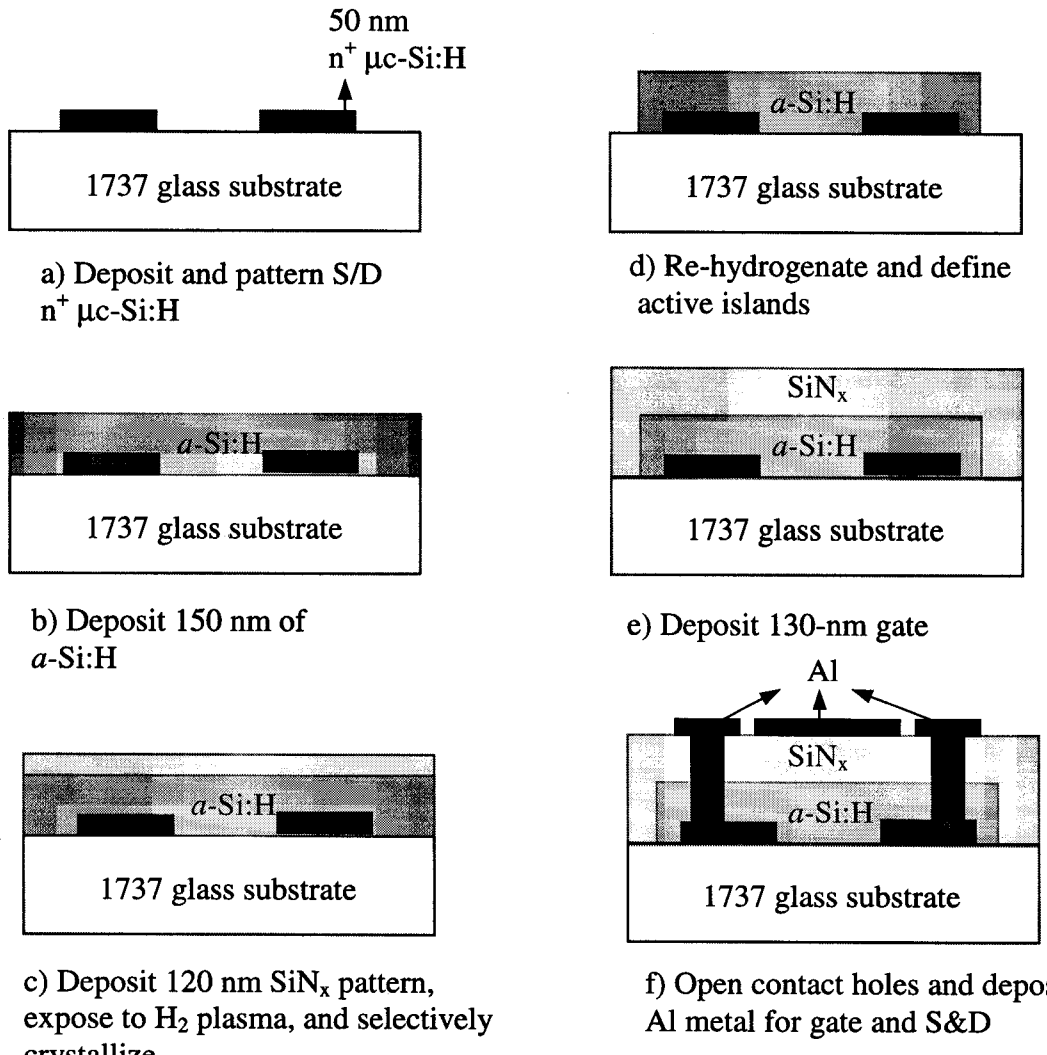


Figure 5.9. Fabrication sequence of TFTs with inverted source/drain contacts i.e., the n^+ μc-Si is deposited first followed by the intrinsic layer. The advantage of this process flow is that the channel does not suffer from etch-damage, although the channel and the source/drain are not co-planar. Furthermore, the n^+ layer to accumulation (for *a*-Si TFT) or inversion layer (for poly-Si TFT) layer contact area is at the very edge of the n^+ layer (although through the i-layer top to bottom), vs. all along under the n^+ layer in the conventional case (Fig. 5.7).

5.4.3 Results and discussion

Fabrication of the integrated TFTs required the careful optimization of many parameters on which the TFTs performance was strongly dependent. The process parameters optimized/studied primarily are -

1) Deposition temperature of the original PECVD *a*-Si:H

2) Thickness of the *a*-Si:H film

3) Type of cap layer used during selective plasma exposure and subsequent selective crystallization

4) Temperature of anneal during crystallization

5) Rehydrogenation condition

6) Gate dielectric, whether SiN_x or SiO_2

7) Post metal hydrogenation

The most important parameter is the rehydrogenation condition. Table 5.1 lists the poly-Si and *a*-Si:H TFTs characteristics as a function of the process parameters. We will refer to the sample numbers of Table 5.1 in the following discussion. The I_{OFF} in all cases was the minimum value of I_{DS} at V_{DS} = 10 V when V_{GS} was scanned from -10 to 20 V. I_{ON} was the maximum I_{DS} at V_{DS} = 10 V. As discussed earlier in Section 4.4.2, the electron field-effect mobility was calculated from the maximum transconductance value (dI_{DS}/dV_{GS}) at V_{DS} = 0.1 V, and threshold voltage was deduced from the intercept of the straight line fit to I_{DS} vs. V_{GS} at V_{DS} = 0.1 V in most cases.

In case of the polysilicon transistors, however, the effect of the source and drain contact resistance cannot be ignored, especially because this is not a self-aligned TFT and the source/drain contacts are not co-planar with the channel (Fig. 5.7). In the linear region (V_{DS} = 0.1 V) the drain to source current is given by

S. No	a-Si:H growth temp. (°C)	a-Si:H thick (nm)	Cap layer	Cryst. Temp (°C)/ Time (h)	Rehydrogenation.		Gate Dielec. (nm)	Post Met. Hydr	a-Si:H TFTs (L ~ 50 μm)				Poly-Si TFTs (L ~ 50 μm)				
					RF (W)	Time (min)			μ_{linear} (cm^2/Vs)	V_{TH} (V)	S (V/dec)	ON/ OFF	μ_{linear} (cm^2/Vs)		V_{TH} (V)	S (V/dec)	ON/ OFF
													No R_s	With R_s			
1	250	150	SiN_x	600/5	45	60	SiN_x/ 170	Yes	0.01	1.5	1.2	10^3	3	2.5	1.4	1.1	$2x10^5$
2	150	150	SiN_x	600/4	45	60	SiN_x/ 170	No	0.24	4	1.2	$4x10^4$	9	8	1.5	1.3	$<10^5$
								Yes	0.24	4.2	1.1	$4x10^5$	9	8	1.5	1.2	$<10^5$
3	150	75	SiN_x	600/5	20	60	SiN_x/ 170	Yes	0.01	5	1.2	$8x10^4$	2	1.5	4	1.2	$2x10^5$
4	150	150	SiN_x	600/4	20	60	SiN_x/ 170	Yes	0.05	5	1.3	10^5	6	5.5	3	1.5	$2x10^5$
5	150	300	SiN_x	600/4	45	75	SiO_2/ 180	Yes	0.6	6	0.95	$2x10^5$	12	10.5	1	1.2	10^4
6	150	150	SiN_x	600/4	45	60	SiO_2/ 130	Yes	0.5	5	1	10^5	14	12	1	1	10^5
7	150	150	SiN_x	625/1	45	60	SiO_2/ 130	Yes	0.7	4	1	10^5	8	7.2	0	0.9	$5x10^5$
8	150	150	SiN_x	600/4	0	0	SiN_x/ 170	Yes	0.02	6	2	$5x10^4$	7	6.4	3.3	1.3	$5x10^4$
9	150	150	SiN_x	600/4	90	60	SiN_x/ 170	Yes	0.02	3	1.3	10^5	8	7.3	1	1	$3x10^4$
10	150	150	SiN_x	600/4	45	30	SiO_2/ 170	Yes	0.05	5	1.3	$4x10^4$	2	1.6	1.5	1.2	$3x10^4$
11	**150**	**150**	**SiN_x**	**600/4**	**45**	**75**	**SiO_2/ 180**	**Yes**	**0.7**	**5**	**1**	**10^6**	**15**	**12.5**	**2**	**1**	**$2x10^5$**
12	150	150	SiN_x	625/1	45	75	SiO_2/ 130	Yes	1.2	6	0.4	10^6	9	8	1	1	10^5
13	150	150	SiN_x	600/4	45	90	SiO_2/ 120	Yes	0.1	1	0.7	$4x10^4$	14	12	0	2	$2x10^5$

Table 5.1. TFT characteristics for several combinations of processing conditions. The optimum condition is highlighted. The standard process flow shown in Fig. 5.6 was used for fabrication of the transistors. In almost all cases, the active device islands were patterned prior to n^+ μc-Si:H deposition. The column titled "Post Metal Hydr." refers to hydrogenation step after metal.

$$I_{DS} = \frac{\mu_{eff} C_{ox} W}{L}[V_{DS}(V_{GS} - V_{TH})] \qquad (5.1)$$

With contact resistance of R_D and R_S at the drain and source ends, and assuming a symmetric device with $R_D = R_S$, equation (5.1) can be rewritten as (ignoring second order terms)

$$I_{DS} \approx \frac{kV_{ds}(V_{GS} - V_{TH})}{1 + 2kR_S(V_{GS} - V_{TH}) + kR_S V_{DS}} \qquad (5.2)$$

where $k = \mu_{eff} C_{ox} W/L$ and R_S is the contact resistance at the source/drain. Equation (5.2) can be used to perform a least square fit of the data and the values of k, V_{TH} and R_S can be extracted for one device of one channel length. For polysilicon TFTs, R_S was found to be as high as 300 kΩ in some cases for channel width of ~200 μm, which means that equation (5.1) would have resulted in a pessimistic estimate of μ_{eff}. Table 5.1 lists the values of field-effect mobility for the poly-Si TFTs calculated from equation (5.2) under the column titled "No R_S", and from the maximum value of the transconductance under the column titled "With R_S", showing the effect of source/drain resistance on the extracted field-effect mobilities. For the *a*-Si:H TFTs, on the other hand, the effect of the source/drain resistance was negligible as the channel conductance and mobilities are much lower than for the poly-Si TFTs.

1) Deposition temperature

The *a*-Si:H TFTs fabricated in this fashion show greatly improved performance when the *a*-Si:H films are deposited at 150 °C instead of 250 °C, as can be seen for samples 1 and 2 in Table 5.1 and in Fig. 5.10. The crystallization time of hydrogen-plasma-treated *a*-Si:H films at 600 °C reduces from 5 h to 4 h for a reduction of *a*-Si:H deposition temperature from 250 °C to 150 °C as we discussed earlier in Section 3.3.4.

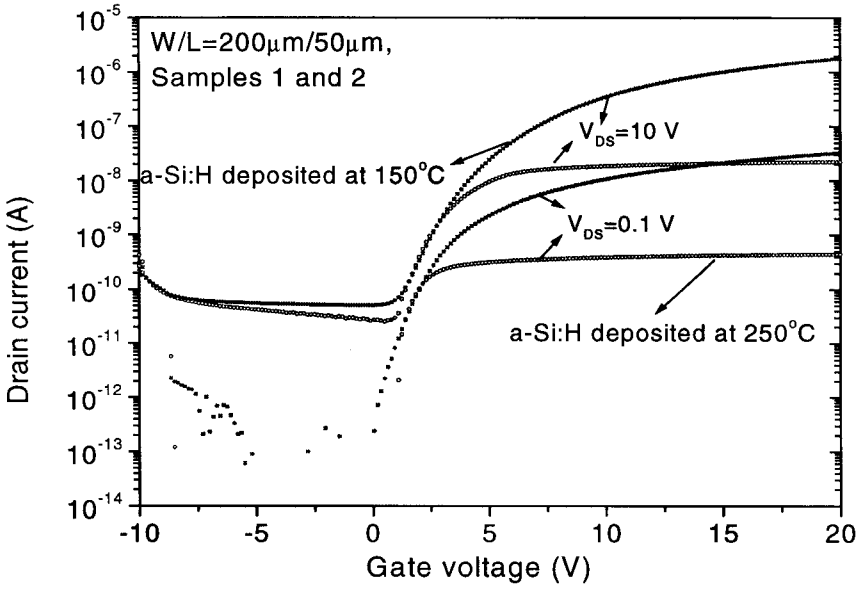


Figure 5.10. Subthreshold characteristics of *a*-Si:H TFTs for two different growth temperatures of the *a*-Si:H precursor film; 150 °C yielded improved I_{ON} and better I_{ON}/I_{OFF}. These are samples 1 and 2 of Table 5.1.

The longer anneal time for the *a*-Si:H deposited at 250 °C means increased hydrogen effusion during the selective crystallization anneal and hence larger defect-state density. This might explain the lower field-effect mobility of 0.01 cm^2/Vs for the 250-°C initial growth-temperature *a*-Si:H TFT compared to 0.24 cm^2/Vs for the 150-°C initial growth-temperature *a*-Si:H TFT as seen in Fig. 5.10. However, the difference is so dramatic that this needs to be investigated more thoroughly. It indicates that efficiency of rehydrogenation depends strongly on the structure of the precursor amorphous film. High-temperature 600-°C anneal might also lead to some kind of restructuring of the resulting Si dangling bonds (after the hydrogen in the film is lost). This might play a crucial role in the efficacy of rehydrogenation. Possibly the more porous structure of the *a*-Si:H deposited at 150 °C facilitates rehydrogenation. It has to be noted that, however, *a*-Si:H TFTs made by conventional inverted-staggered processing in *a*-Si:H films deposited either 150 °C or 250 °C had similar field-effect mobilities [1, 10].

The lower growth temperature also led to improved polysilicon TFT performance. The field-effect mobility (μ_n) of the polysilicon TFTs increased from 3 cm^2/Vs to 9 cm^2/Vs when the deposition temperature of the precursor *a*-Si:H film was reduced to 150 °C from 250 °C. The *a*-Si:H grown at 150 °C (sample 2) has higher hydrogen content than that grown at 250 °C (sample 1). The higher hydrogen content facilitates nucleation and growth of larger grains [7], which in turn led to the higher electron field-effect mobility for the poly-Si TFTs. A similar increase in μ_n was seen in case of the self-aligned n-channel TFTs discussed previously in chapter 4. All the TFTs in this case had SiN_x as the gate dielectric.

2) Thickness of intrinsic *a*-Si:H film

The crystallization time at 600 °C increases from 4 h to 5 h for the hydrogen-plasma-treated sample, as the *a*-Si:H film thickness is reduced from 150 nm (sample 4) to 75 nm (sample 3), with the growth temperature being 150°C. This might be due to film stress effect that decays from the *a*-Si:H/glass interface into the film [21] as discussed previously in Section 3.3.5. This increase in crystallization time may lead to increased outdiffusion of hydrogen from the amorphous regions during selective crystallization. This hypothesis is supported by the TFT characteristics of samples 4 and 3, with active layer thickness of 150 nm and 75 nm respectively. The OFF currents (I_{OFF}) of the poly-Si TFTs drop from ~20pA/μm to 2pA/μm at V_{DS} of 10 V, as the thickness of the i-layer is reduced from 150 nm to 75 nm, but μ_n also drops from ~6 cm^2/Vs to 2 cm^2/Vs. The μ_n of the *a*-Si:H TFT also fell from ~0.05 cm^2/Vs to ~0.01 cm^2/Vs as the i-layer thickness is reduced. Increasing the active layer thickness to 300 nm from 150 nm (samples 5 vs. 11) did not result in any significant change in I_{ON} but I_{OFF} increased to

~50 fA/μm from ~10 fA/μm for the *a*-Si:H TFTs, while the poly-Si TFT characteristics were unchanged. The optimum thickness of the active layer is therefore ~150 nm.

3) Cap layer for selective crystallization

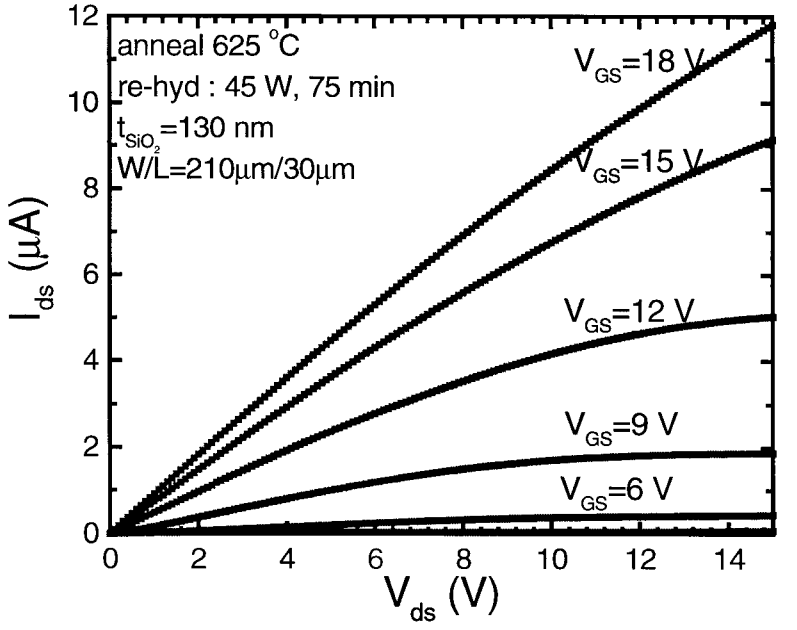
The cap layer plays a crucial role in this process. It has to provide a barrier against the hydrogen plasma, and a diffusion barrier against hydrogen outdiffusion during the high temperature (≥ 600 °C) anneal when the exposed regions crystallize. Silicon nitride is far superior in these respects to SiO_2. But the normal SiN_x growth temperature is ~300 °C or higher, which might alter the characteristics of the as-deposited *a*-Si:H film as the optimized growth temperature for the *a*-Si:H film was found to be 150 °C, and hydrogen in the *a*-Si:H begins to outdiffuse at a few degrees above the growth temperature [22, 23]. Therefore the SiN_x deposition recipe was changed to 200 °C, and hydrogen dilution was used during SiN_x growth make the film denser [10] and hence a better diffusion barrier. The recipe used for SiN_x deposition is spelt out in detail in Section 5.4.1.

SiN_x is also better than SiO_2 in another respect. Regions of *a*-Si:H film covered by the nitride film crystallize slower than those in which the nitride has been removed, whereas SiO_2 covered regions do not show this effect (crystallization time of >24 h with the SiN_x cap on vs. crystallization time of 15-20 h without the SiN_x-cap layer). The SiN_x has larger bond lengths than the *a*-Si:H and is deposited at higher temperature than the *a*-Si:H film (200 vs. 150 °C). This results in tensile stress in the thin *a*-Si:H films which inhibits nucleation during the subsequent crystallization anneal [24-26]. This would ensure that the regions covered by the nitride remain amorphous and lose comparatively less amount of hydrogen during the high temperature annealing. All samples shown in Table 5.1 had SiN_x-cap layer on the amorphous regions during the selective crystallization anneal.

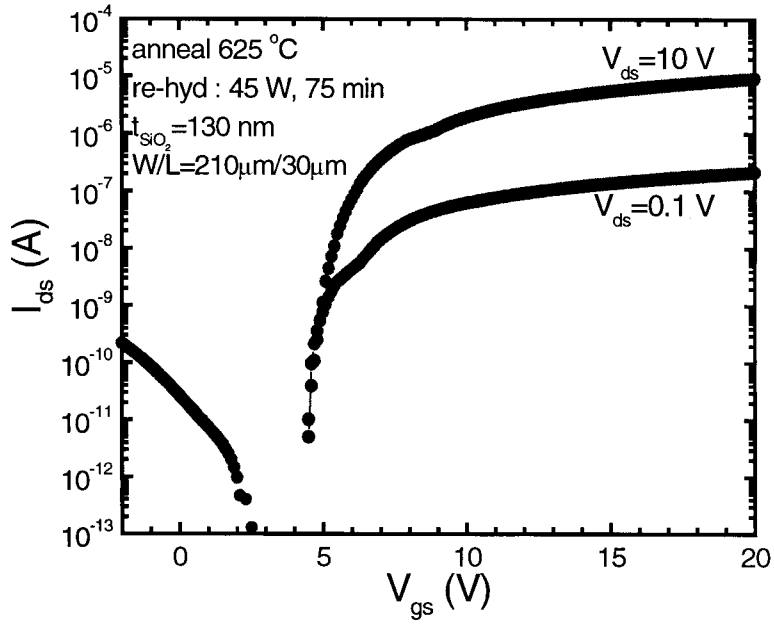
4) Temperature of annealing

Another process parameter, which can be changed easily, is the crystallization temperature. The *a*-Si:H TFTs mobility increased to 0.7 cm^2/Vs from 0.5 cm^2/Vs for samples 6 and 7, respectively, without change in I_{OFF} when the crystallization anneal temperature was increased to 625 °C from 600 °C. In fact, the higher temperature anneal led to better performance *a*-Si:H TFTs with field-effect mobility as high as 1.2 cm^2/Vs (Figs. 5.13 (a) and (b)) when the rehydrogenation time was increased to 75 min from 60 min for sample 12. As we discussed in Section 3.3.2, increasing the annealing temperature by 25 °C from 600 °C resulted in reduction of crystallization time of the hydrogen-plasma-treated region by nearly a factor of 4 from ~4 h to ~1 h. The reduced crystallization time during selective crystallization might lead to lower hydrogen loss from the amorphous regions. However, the crystallization time of the hydrogen-plasma-treated region has an activation energy of about 2.7 eV [6], and the diffusion of hydrogen from the *a*-Si:H films, which is also a thermally-activated process, has an activation energy of 1.6 to 2.8 eV [22, 23]. This would mean that in addition to faster crystallization rates at higher temperatures, the hydrogen effusion rate is also enhanced at higher temperatures. But, due to the slightly lower activation energies of the hydrogen effusion process, the amount of hydrogen lost during the 1-h 625-°C anneal might be less than that lost during the 4-h 600-°C anneal. This might explain the higher *a*-Si:H field-effect mobilities observed in case of the higher temperature anneal process.

On the other hand, the field-effect mobilities of the poly-Si TFTs decreased by a factor of nearly two from 14 cm^2/Vs to 8 cm^2/Vs for samples 6 and 7, respectively, as the temperature of anneal was increased from 600 to 625 °C. As the annealing temperature is raised the grain size in the polycrystalline regions is reduced because the higher nucleation rate leads to closely packed grains [27], which would explain the



(a)



(b)

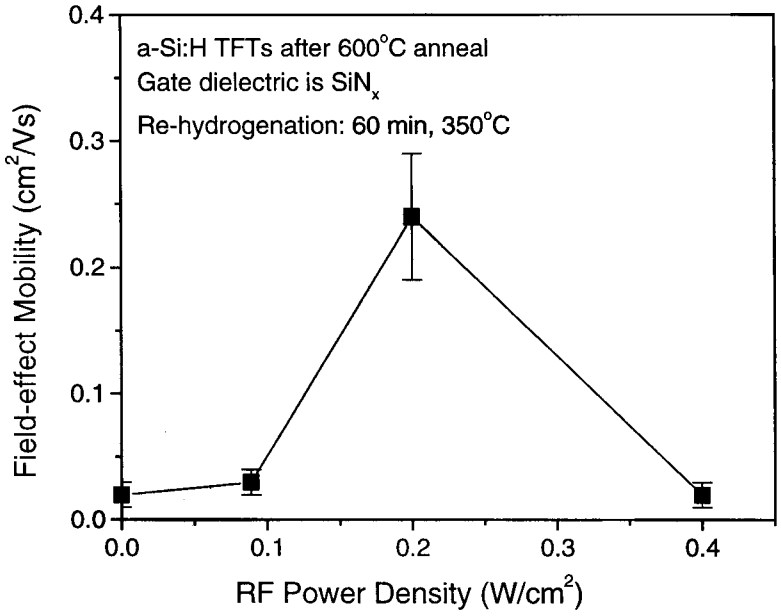
Figure 5.11. Best *a*-Si:H TFT characteristics for crystallization anneal at 625 °C and rehydrogenation at 0.2 W/cm^2 for 75 min, (a) linear characteristics, and (b) subthreshold characteristics.

smaller mobilities for the poly-Si TFTs annealed at higher temperature. A similar reduction in mobility with increase in annealing temperature was also seen in case of self-aligned polysilicon TFTs discussed previously in Section 4.5.3. Optimization of both poly-Si and *a*-Si:H TFTs will require more experiments with time-temperature programs for the crystallization anneal.

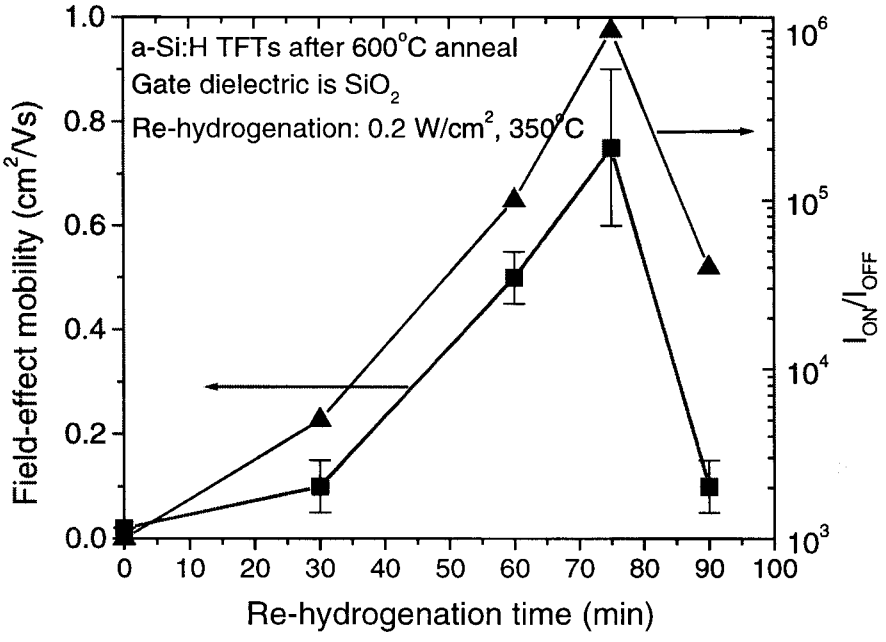
5) Rehydrogenation condition

Though SiN_x is used as a cap layer during the crystallization process, extensive hydrogen outdiffusion does occur (Section 5.3). The TFTs fabricated in *a*-Si directly after the crystallization anneal, without any rehydrogenation (sample 8), have poor mobilities of ~0.02 cm^2/Vs, while the poly-Si TFTs have mobilities of ~7 cm^2/Vs. Rehydrogenation is therefore required to passivate the dangling bonds in the amorphous region and thereby improve the electrical characteristics of the film. But rehydrogenation is a double-edged sword, as the hydrogen radicals abstract hydrogen from the *a*-Si:H layer and even etch the amorphous silicon layer by inserting themselves in Si-Si bonds and creating volatile SiH_4 [28, 29]. Therefore, the hydrogen plasma parameters, primarily the RF power and exposure time, have to be adjusted just right, so that the film is sufficiently hydrogenated but not etched. This requires that rehydrogenation be done at low RF power and high pressure to reduce the hydrogen ion energy, and that the substrate temperature be raised to accelerate the hydrogen diffusion into the bulk of the film. The optimum condition was found to be a hydrogen plasma at RF power density of 0.2 W/cm^2, chamber pressure of 1 torr, H_2 flow of 50 sccm, substrate temperature of 350 ^oC and exposure time of ~75 min. The effect of rehydrogenation on the materials properties of the annealed *a*-Si:H films has been discussed previously in Section 5.3.

In addition to setting the plasma conditions right so that etching of the *a*-Si:H is minimized, the chamber walls and the electrodes should also be prepared prior to the rehydrogenation step. As discussed in Section 4.3.2, hydrogenation for grain boundary passivation of the poly-Si TFTs requires that the chamber be prepared by striking a hydrogen plasma prior to loading the samples to remove any *a*-Si:H on the chamber walls or on the electrodes to minimize any *a*-Si:H deposition on the samples. However, in this case we had to deposit *a*-Si:H on dummy glass slides using the same sample holder as the one used for the actual rehydrogenation, to coat the chamber walls and the sample holder with *a*-Si:H film. This was done to minimize etching of the *a*-Si:H film during the subsequent rehydrogenation step. During the rehydrogenation step, the *a*-Si:H film deposited on the walls and the electrode is also etched, and thereby the etching of *a*-Si:H film on the sample substrate is minimal. This dummy coat of *a*-Si:H must be done at low temperatures (~150 °C), as the etch rate of *a*-Si:H in hydrogen plasma increases if the growth temperature of the film is lowered and this ensures that the dummy *a*-Si:H film is preferentially etched. The etching effect of the hydrogen plasma was most severe when the rehydrogenation was done after the active islands were patterned, which reduces the effective area of the *a*-Si film to be hydrogenated (reduced loading factor). Also, the previous history (runs) of the sample holder and the deposition chamber plays an important role. It was found that the etching of *a*-Si:H during rehydrogenation was minimized if the *a*-Si:H was deposited in the previous runs as compared to nitride or μc-Si:H films. Coating the sample holder prior to the actual rehydrogenation with ~300 nm of *a*-Si:H deposited at 150 °C minimizes this dependence on the previous history of the chamber and the substrate/sample holder. All this goes to prove that the rehydrogenation step is a very critical step and the most



(a)



(b)

Figure 5.12. Field effect mobility of the *a*-Si:H transistors for different rehydrogenation conditions, (a) as a function of RF power (samples 8, 4, 2 and 9), and (b) as a function of exposure time (samples 10, 7, 11 and 13).

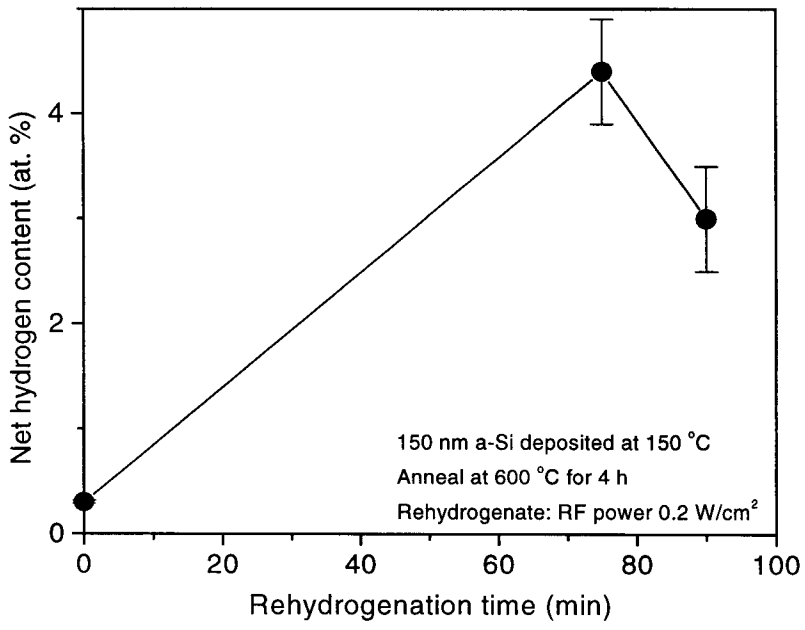


Figure 5.13. Net hydrogen content as estimated from the integrated IR absorption near 630 cm^{-1} in the *a*-Si:H films after rehydrogenation for various exposure times. The hydrogen plasma conditions were: RF power density of 0.2 W/cm^2, pressure of 1 torr, and hydrogen flow rate of 50 sccm. The growth temperature of the initial *a*-Si:H film was 150 °C, deposited on SiO_2/Si substrate for infrared absorption measurement.

demanding. See Appendix A for the actual rehydrogenation process sequence with the recipes for the dummy *a*-Si:H film and the rehydrogenation step.

Fig. 5.12(a) shows the effect of RF power (samples 8, 3, 2 and 9) and Fig. 5.12(b) illustrates the effect of plasma exposure time (samples 10, 7, 11 and 13) on μ_n and I_{ON}/I_{OFF} of the *a*-Si:H TFTs, respectively. Increasing the rehydrogenation time beyond 75 min led to significant etching of the *a*-Si:H film. When the exposure time was increased to 90 min from 75 min, the hydrogen content of the film fell (Fig. 5.13) from 4.4 at. % to ~3 at. % (as measured by IR absorption at 630 cm^{-1}) with a corresponding decrease in field-effect mobility of the *a*-Si:H TFTs (Fig. 5.12(b)). High RF power densities (>0.2 W/cm^2) led to etching in spite of all the chamber preparations

as discussed earlier, and above 0.4 W/cm^2 the *a*-Si:H film was completely etched. When the RF power was too low, the hydrogenation was not efficient, leading to poor field-effect mobility for the *a*-Si:H TFTs.

The poly-Si TFT characteristics, on the other hand, were essentially unchanged, as rehydrogenation was not a critical step for them. Any change observed in the poly-Si performance when only the RF hydrogen conditions were changed (e.g. between samples 6 and 10, Table 5.1) probably is due to a variation in the percentage of crystallinity of the film after the 4-h anneal at 600 °C, and not related to hydrogenation. This is in contrast to the effect of hydrogenation on the field-effect mobility observed earlier in case of the self-aligned polysilicon TFTs in chapter 4. This might be because the rehydrogenation was done at far lower RF power densities (~0.2 W/cm^2) during the integrated TFT processing (to minimize the *a*-Si:H film etching as discussed previously) compared to the RF power density (~0.6 W/cm^2) during hydrogenation for defect passivation for self-aligned poly-Si TFTs. In fact the improvement in field-effect mobility of the self-aligned poly-Si TFTs was minimal at low RF power densities, and significant improvement only occurred at RF power densities of 0.4 W/cm^2 or larger (Fig. 4.2). Another reason might be that the field-effect mobility of carriers in case of the non-self-aligned poly-Si TFTs is limited by carrier scattering at the poly-Si/SiO_2 interface, as the channel is etched during processing, rather than by carrier scattering at the grain boundaries. And since, hydrogenation does not reduce the surface roughness of the films, the field-effect mobility of the non-self-aligned poly-Si TFTs is not changed due to hydrogenation.

6) Gate dielectric

Traditionally *a*-Si:H TFTs have been fabricated with bottom gates and SiN_x gate dielectric to obtain the lowest interface-state density. This led to improved μ_n and higher

I_{ON}/I_{OFF} [19]. But poly-Si TFTs are fabricated usually with top gates and SiO_2 as the gate dielectric [30]. Hence a trade-off is required. We compared SiN_x and SiO_2 as the gate dielectric in the top gate configuration for both the *a*-Si:H and the poly-Si TFTs. With SiO_2 as the gate dielectric, deposited at 250 °C by PECVD, from SiH_4 and N_2O, and at RF power density of ~0.1 W/cm^2, the poly-Si TFTs had μ_n of ~14 cm^2/Vs (sample 11). On the other hand, TFTs with SiN_x as the gate dielectric, deposited at 300 °C by PECVD, using SiH_4, H_2 and NH_3, and at a RF power of ~0.09 W/cm^2 had μ_n of ~9 cm^2/Vs (sample 2). Although the SiO_2/*a*-Si:H interface-state densities are higher than that of the SiN_x/*a*-Si:H interface [31], the leakage currents were not significantly increased when SiO_2 was used as the gate dielectric instead of SiN_x for the *a*-Si:H TFTs. But, the I_{ON} and hence μ_n were also higher (0.5-1 cm^2/Vs compared to ~0.2 cm^2/Vs), with I_{OFF} of only ~10-50 fA/μm when SiO_2 was the gate dielectric instead of SiN_x. Therefore, overall best results for both *a*-Si:H and poly-Si TFTs were obtained with SiO_2 as the gate dielectric.

7) Post metal hydrogenation

All the transistors were annealed in forming gas (10% H_2 in N_2) at ~225 °C as mentioned earlier in Section 5.4.1 to reduce the contact resistance between the n^+ μc-Si:H source and drain layers and the aluminum prior to I-V measurement. In addition to this anneal, a further hydrogenation using a RF hydrogen plasma at RF power of 0.6 W/cm^2 and exposure time of 60 min substrate temperature of 250 °C and pressure of 1 torr (similar to the conditions used for hydrogenation of self-aligned poly-Si TFTs discussed in Section 4.3.1) reduced I_{OFF} from ~250 fA/μm to ~30 fA/μm for the *a*-Si:H TFTs (Fig. 5.14). But there was no change in μ_n of either the poly-Si or the *a*-Si:H TFTs (sample 2, Table 5.1). However, this step did not lead to such drastic reduction in I_{OFF}

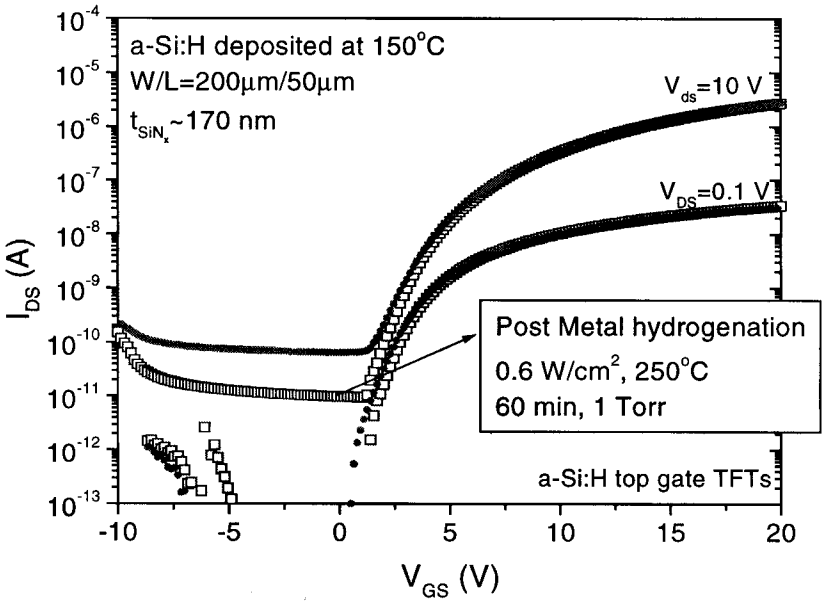


Figure 5.14. Drain current as a function of gate voltage plotted on log scale of *a*-Si:H TFTs before and after post-metal hydrogenation, showing the reduction in I_{OFF} , while I_{ON} remain the same for sample 2, Table 5.1.

of sample 11, which was rehydrogenated after the 600-°C anneal step under the optimized conditions as discussed previously, and therefore did not require any subsequent hydrogenation. The implication is that the post-metal hydrogenation step is essential only if the prior rehydrogenation was incomplete, i.e., not all the dangling bonds in the *a*-Si:H layer were passivated.

Overall optimization

The best performance of *a*-Si:H TFTs in this process flow was achieved when the selective crystallization anneal was done at 625 °C instead of the usual 600 °C. This process yielded *a*-Si:H TFTs with field-effect mobilities as high as 1.2 cm^2/Vs with ON/OFF current ratio > 10^6, subthreshold slope of 0.4 V/decade and threshold voltage of ~6 V. However, the field-effect mobility of the poly-Si TFTs was lowered to ~9 cm^2/Vs compared to ~14 cm^2/Vs for the poly-Si TFTs with the 600-°C crystallization anneal (sample 12, Table 5.1).

The best performance for the non-self-aligned poly-Si TFTs was achieved for the process with 600-°C crystallization anneal with SiO_2 as the gate dielectric and with the n^+ μc-Si:H deposited after the device islands have been patterned (to minimize overetching of the channel as discussed in 5.4.2). The field-effect mobility of these poly-Si TFTs was ~14 cm^2/Vs and the ON/current ratio was $>10^5$ (sample 11, Table 5.1). With the self-aligned process flow discussed in chapter 4, for the hydrogen-plasma-treated poly-Si TFTs, higher field-effect mobility (~33 cm^2/Vs) and better ON/OFF current ratios (~10^6) can be achieved (sample 2, Table 4.1). With the laterally-seeded process flow, the performance could be improved even further to achieve field-effect mobility as high as 75 cm^2/Vs and ON/OFF current ratio greater than 10^7 (sample 12, Table 4.2). The self-aligned process, however, requires an additional 6-h 600-°C-process step to anneal the source/drain implant damage (Section 4.4.1). This results in more complicated processing as the amorphous regions would have to be covered during this anneal to minimize loss of hydrogen, in addition to requiring another rehydrogenation step. Higher number of high-temperature steps leads to the increased degradation of *a*-Si:H TFT characteristics.

To achieve optimum performance for both poly-Si and *a*-Si:H TFTs with the same process flow, several trade-offs were required like, 600-°C anneal instead of 625-°C anneal, SiO_2 instead of SiN_x as the gate dielectric, and the use of non-self-aligned process with deposited n^+ μc-Si:H for source/drain contacts instead of self-aligned process with ion-implanted source/drain contacts. The optimum conditions for the fabrication of the integrated poly-Si and *a*-Si:H TFTs after selective crystallization by

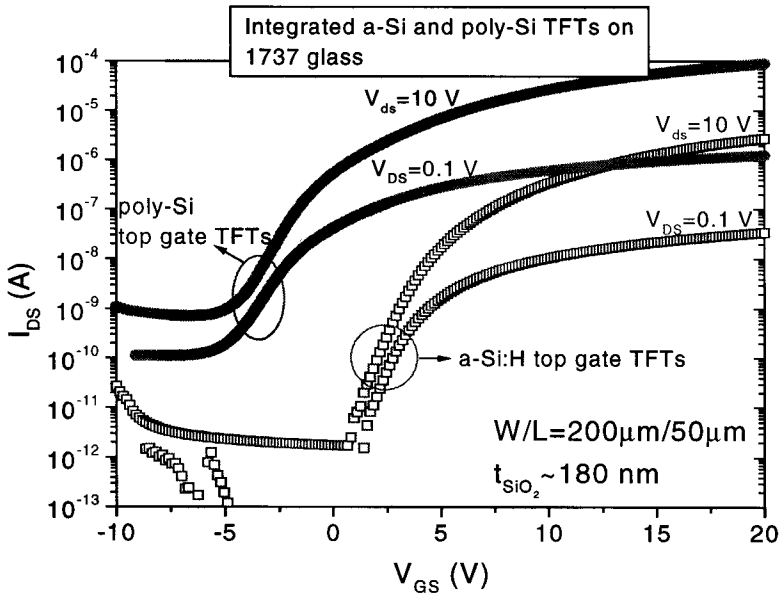


Figure 5.15. Drain current as a function of gate voltage plotted on a logarithmic scale of optimized *a*-Si:H and poly-Si TFTs made of the same *a*-Si:H precursor film on Corning 1737 glass substrate (sample 11). Poly-Si is obtained by the selective crystallization of hydrogen-plasma-seeded *a*-Si:H at 600 °C in N_2 for 4 h.

annealing at 600°C are those given for sample 11 in Table 5.1. The μ_n in the linear regime were ~0.7 and 15 cm^2/Vs for the *a*-Si:H and poly-Si TFTs, respectively, with SiO_2 as the gate dielectric. I_{OFF} of *a*-Si:H TFT is ~10 fA/μm and I_{ON} of the poly-Si TFT is ~1μA/μm, with I_{ON}/I_{OFF} of both types of devices $\geq 10^5$ (Fig. 5.15). These results compare favorably with work on integrating *a*-Si:H and poly-Si TFTs by laser processing, which resulted in *a*-Si TFTs with μ_n of ~0.9 cm^2/Vs and poly-Si TFTs with μ_n of ~20 cm^2/Vs [4]. These *a*-Si:H TFTs also compare favorably with conventional inverted-staggered TFTs, which have μ_n of ~1 cm^2/Vs and I_{ON}/I_{OFF} ~10^7 [1, 19]. A typical result for top-gate *a*-Si:H TFT with SiN_x as the gate dielectric, is field-effect mobility of ~0.4 cm^2/Vs and ON/OFF current ratio of ~10^5 [32]. Our results for *a*-Si:H top gate TFTs after a 600 or 625 °C annealing step are the best reported.

5.5 SUMMARY

A masked exposure to a RF hydrogen plasma can be used to spatially control the subsequent crystallization of *a*-Si:H to poly-Si, resulting in polycrystalline silicon and amorphous silicon areas on the same substrate. The selective crystallization effect has been used to fabricate TFTs in both the poly-Si and *a*-Si:H regions in a single layer of silicon for the first time with no laser processing. All the transistor fabrication steps for both *a*-Si:H and poly-Si were shared so as to minimize cost. The only additional mask required was to create the amorphous and polycrystalline regions in the single Si layer. Careful control of the rehydrogenation process achieved high field-effect mobility in the amorphous silicon after the 600-°C-crystallization process. Optimized transistor fabrication produced good TFT characteristics for both the poly-Si and *a*-Si:H TFTs. The poly-Si TFTs had an electron mobility of ~15 cm^2/Vs and the *a*-Si TFT had an electron mobility ~0.7 cm^2/Vs. In both cases the ON/OFF current ratio was $>10^5$. This technique can therefore be used to integrate *a*-Si:H TFT for pixel switching and poly-Si TFTs for row/column driver circuits in active-matrix liquid-crystal displays.

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Chapter 6

SOLID PHASE CRYSTALLIZATION: TECHNIQUES TO REALIZE SILICON-ON-INSULATOR STRUCTURES

6.1 INTRODUCTION

In chapter 2 we discussed the need for crystallization of precursor amorphous silicon (*a*-Si) films to obtain large grain polycrystalline silicon with smooth surfaces, and the various techniques that have been studied to realize it. One of the most prevalent and popular techniques that have gained lot of interest, especially for use in 3-D ICs and displays, in the recent years is the solid phase crystallization of amorphous silicon films by furnace annealing. There are several advantages of this technique, like, low cost, simplicity, excellent uniformity, reproducibility, high throughputs by batch annealing, ease of large area-substrate processing, and highly smooth surface morphologies [1]. In this chapter we will discuss in some detail, the various techniques that have been reported to achieve single-crystal like Si on insulating substrates (SOI) by solid phase crystallization of precursor *a*-Si films.

However, the major drawbacks of the technique especially for use in fabrication of silicon-on-insulator structures, are the long anneal time [2] typically required when glass substrates are employed, the fact that nucleation occurs randomly leading to

random distribution of grain boundaries with random grain orientation in the silicon film, and the presence of crystalline defects within the grains of SPC polysilicon films. The detrimental effect of grain boundaries due to carrier trapping on the electrical characteristics of the polycrystalline silicon film is well documented [3, 4]. The grain boundary effect can be reduced by increasing the grain size of the polysilicon films and by controlling the location of the grain boundaries.

Several techniques have been reported in the literature to increase the grain size of the *a*-Si films. As we discussed in chapter 2, the key is to increase the crystal growth rate and reduce the nucleation rate (equation 2.1). Due to the higher activation energy of nucleation compared to crystal growth [5], larger grains are most easily achieved by annealing at lower temperatures (<650 °C) [2]. Also, the nucleation rate is a strong function of the disorder in the precursor amorphous silicon films [6]. Therefore, one obvious technique to increase grain size of polysilicon is to increase the disorder in the precursor *a*-Si films by either reducing the growth temperature (Section 3.34), or increasing the growth rate [6]. Other techniques to increase the grain size involve a multiple-step anneal [7], suppressing nucleation at the *a*-Si/substrate interface through incorporation of oxygen [8] or growth of double layers of *a*-Si [9] or using Si_3N_4 coated glass substrates [10], a high-temperature anneal after complete crystallization leading to secondary grain growth [11, 12], and amorphization of polysilicon films by ion implantation such that a few small grains survive and during subsequent annealing these crystalline regions grow to yield larger grains [5, 13]. Section 6.2 discusses these grain-enhancement techniques.

Seeding selective regions of the *a*-Si film can control the location of grain boundaries. Subsequent lateral grain growth occurs in desired locations and transistors can be fabricated in these selective regions within a particular grain with characteristics

close to that obtained for transistors in single-crystal Si. Various nucleation enhancement and seeding techniques have been studied for selective nucleation of *a*-Si films and also to reduce the crystallization time (as nucleation of seeds is usually the rate-limiting step during SPC of *a*-Si) as discussed in chapter 2. In our work we studied the hydrogen-plasma-seeding effect, as it might be the cleanest of all the nucleation enhancement methods, introducing the least amount of contamination and damage in the resulting polysilicon films. We also discussed the effect of controlled hydrogen plasma seeding in the source/drain regions of the transistor to realize higher field-effect mobility due to reduced number of grain boundaries in the channel in chapter 4. In this chapter (Section 6.3) we will discuss in further detail the various seeding techniques that have been tried to control the locations of grain boundaries and to achieve larger grains through the lateral-crystallization effect.

In addition to controlling the location of grain boundaries and increasing the grain size, the defects within the grains should also be reduced (Section 6.4) and the grain orientation should be controlled (Section 6.5) to achieve ideally (100) vertical orientation, so as to realize single-crystal like behavior. In the following sections we will discuss these issues in some detail.

6.2 TECHNIQUES TO REALIZE LARGE GRAINS

Direct deposition of silicon on insulating substrates like SiO_2 gives rise to either amorphous films or polycrystalline films with small grains (grain size < 100 nm) and rough surfaces, due to the amorphous nature of the insulating substrate (either glass or SiO_2). As mentioned in the earlier section, solid phase crystallization of amorphous Si is preferred method for obtaining SOI films. However, small grains and random grain boundaries can lead to scattering of the charge carriers and hence poor device properties. Various techniques have been tried to increase the grain size by reducing

nucleation rates with respect to crystal growth rates. In the following sections we will discuss the several techniques that have been studied to achieve this.

6.2.1 Annealing temperature and effect of disorder in a-Si films

Annealing temperature

The final grain size of SPC annealed polysilicon films depends on the annealing temperature, and the deposition temperature and the deposition rate of the precursor amorphous films. Calculation of relation between the average grain size and the growth and nucleation rates is a relatively complex problem. However, after many simplifying assumptions, the average grain size (g) can be written as [2] (for thin films)

$$g = g_o e^{\left[\frac{E_n - E_g}{3kT}\right]} \qquad (6.1)$$

where g_o is independent of temperature, E_n and E_g are the activation energy of nucleation and grain growth rate, respectively. From equation (6.1) we see that the grain size will increase with decreasing annealing temperature provided that E_n is greater than E_g. The value of E_n-E_g is strongly dependent on the material properties of the precursor amorphous films with values of 0.25 eV for low pressure chemical vapor deposited (LPCVD) films and ~2 eV for e-beam-evaporated amorphous silicon [14, 15].

However, Koster [14] has speculated that as the annealing temperature increases, at very high temperatures (>900 °C) the nucleation rate reduces while the crystal growth rate keeps increasing. The crystal growth rate reduces near the melting point temperature of silicon. This means that large grains can also be obtained by annealing at very high temperature where the nucleation rate starts to decrease with temperature but a high growth rate can be maintained. Even under such conditions, the heating of the sample to that temperature range has to occur fast enough to avoid excessive nucleation during the temperature rise.

Effect of disorder in *a*-Si films

Large grains were also obtained for crystallization of *a*-Si films deposited at lower temperatures [6, 16, 17] and high growth rates [6]. Increasing the structural disorder of the silicon network in the amorphous films resulted in reduced nucleation rates and thereby increased grain size for the crystallized films. The disorder of the underlying silicon network can be increased by utilizing low deposition temperatures combined with high deposition rates. Both parameters influence the surface diffusion length, which is a measure of the surface mobility of the silicon adatoms (adsorbed atoms) during deposition [18]. As the deposition temperature decreases or the deposition rate increases the surface diffusion length reduces, resulting in the deposition of silicon films with higher structural disorder. The crystal growth rates were also found to be higher for more disordered structures, indicating a weaker bonding among the silicon atoms in the disordered structural matrix. The growth is probably enhanced due to the probability of atom rearrangement within a looser structure [6]. Therefore a combination of suppressed nucleation rate and enhanced crystal growth (equation 2.1) ensures larger grains for films crystallized from disordered amorphous films.

To illustrate this effect of disorder in the amorphous film on the final grain size of the crystallized films, consider the grain size of polysilicon obtained from crystallization of *a*-Si deposited by LPCVD using either silane or disilane. When silane is used in LPCVD the deposition rates are significantly reduced as the deposition temperature is reduced below 530 °C. Disilane, on the other hand, has been shown to result in the high deposition rates even at temperatures below 500 °C. Hence, films crystallized from *a*-Si obtained by the pyrolysis of disilane yielded larger grains [19].

Low anneal temperature (under normal circumstances) and increased disorder in the amorphous silicon film are key to any technique involving grain size enhancement.

6.2.2 Multiple-step anneal

Large-grain polysilicon was realized from multistep thermal annealing (MTA) utilizing the incubation time for nucleation due to the higher activation energy for nucleation [7]. According to this method, crystallization takes place in steps, via heating-cooling cycles. In each cycle the wafer is annealed for a period which is less than the incubation time for nucleation and then cooled to a low temperature for relaxation. During each annealing period at high temperature, the seed grains grow to a certain extent, while spontaneous nucleation does not occur. The annealing process could then be designed so that the seed grains will grow by steps until all the amorphous material is consumed, while nucleation is minimized or does not occur at all.

A multistep thermal anneal process with a short high-temperature step to nucleate the film followed by a low-temperature step to maximize grain has also been reported [20]. This requires the ability to detect nucleation so that the temperature can be lowered. An acoustic sensor was used to measure the temperature of the wafer, from the time of flight of acoustic waves through the wafer [21]. PZT transducers bonded to quartz pins are used to pulse ultrasonic Lamb waves through the sample. The measured delay exhibits a linear variation with temperature. The onset of nucleation was detected from the dip in temperature. The optical absorption coefficient of amorphous silicon film is reduced as it crystallizes. In rapid thermal annealing of films using tungsten halogen lamps (discussed previously in Section 2.2.2) using transparent substrates, this results in a reduction of heat absorption by the sample and therefore a reduction in substrate temperature. N-channel transistors made in such MTA films showed nearly 20 % increase in field-effect mobility with a corresponding increase of grain size compared to single-step-annealed films [20].

6.2.3 Suppress nucleation at the a-Si/substrate interface

As mentioned earlier, the key to increasing grain sizes of polysilicon films is to suppress nucleation rates so that the grain can grow larger without impinging on other grains. The interface of the precursor amorphous film/substrate (a-Si/SiO_2) is known to provide large number of nucleation sites [6, 22]. Several techniques have been tried to suppress this interface-nucleation involving either incorporation of oxygen at the interface [8] or growth of double-layers of a-Si films [9]. We will discuss these techniques in some detail next.

Incorporation of oxygen at the a-Si/SiO_2 interface

It has been known that oxygen retards the crystallization process of a-Si during the solid phase epitaxial regrowth of oxygen-implanted a-Si [23]. Oxygen was therefore incorporated at the a-Si/SiO_2 interface during growth of the a-Si film by introducing oxygen into the LPCVD chamber before commencement of growth [8]. This resulted in suppression of interface nucleation at the lower Si/SiO_2 and nucleation occurred at other sites, namely the top surface. These films had fewer crystalline defects like microtwins and stacking faults, unlike the typical interface-nucleated films. These crystalline defects are typically produced in interface-nucleated films to relieve the large magnitude of tensile stress at the vicinity of the a-Si/SiO_2 interface (also discussed in Section 3.3.5). The stress is formed by the phase transformation from amorphous to crystalline [24]. For the case of the top-surface nucleation, the defects are not formed at the nucleation step since the stress is relieved at the surface [8]. However, the stress gradually builds up at the growth front as the crystal grows, and when the stress increases above a critical level, defects are generated at the growth front. The surface-nucleated grains had equiaxial shape with {111}-orientation and grain size of 3-5 μm,

while conventional SPC polysilicon had elliptical grains with size of about 0.3-1μm [8]. No data on the electrical characteristics of such films was available.

Double layer of *a*-Si film

The other technique reported to suppress nucleation at the *a*-Si/SiO_2 interface involved deposition of double layers of amorphous silicon deposited at different temperatures [9]. The bottom *a*-Si layer was deposited at lower temperature (higher disorder) to suppress the nucleation, while the top layer was deposited at higher temperature and hence nucleate with smaller number of nucleation sites and maintains a high growth rate. The deposition temperature of the top layer determined the incubation time for nucleation and the total crystallization time. This means that one can get the larger grains realized from annealing of low-temperature deposited *a*-Si films without paying penalty of the longer crystallization time due to slower nucleation rate. The grain size of the double layer film sequentially deposited at 150 °C and 200 °C enhanced to 1.8 μm while that of the monolayer film deposited at 200 °C was 1.4 μm. In fact the grain size improved to 2.1 μm when double layers deposited sequentially at 65 and 200 °C, though at a penalty of longer crystallization time [9]. Further study is required to find the limits of this process and determine the effect of thickness of the individual layers on the final grain size.

6.2.4 Secondary grain growth

Grain growth in polycrystalline silicon thin films proceeds through two fundamentally different processes, namely normal grain growth and secondary grain growth [11]. When the initial grain size is smaller than the film thickness, normal grain growth leads to a continuous increase in the average grain size and the grain growth is three-dimensional. In this case the average grain size increases so that the total grain-