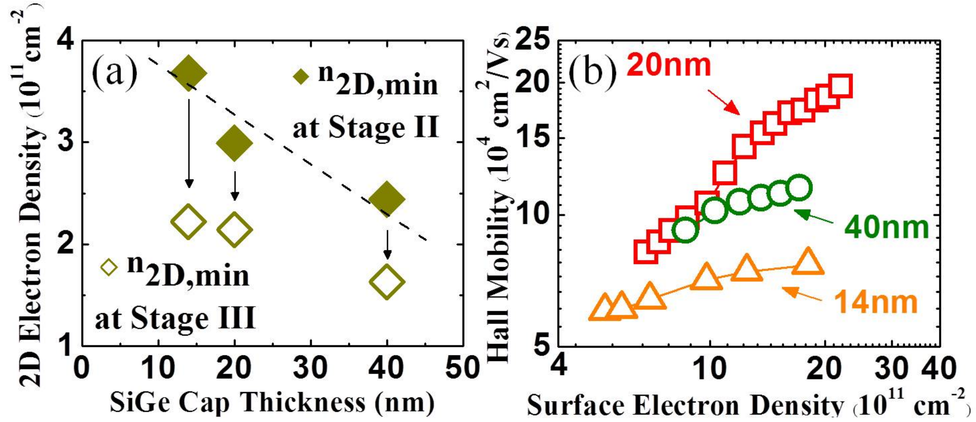


Figure 6.7: (a) The reduction in minimum n_{2D} due to the screening effect by the surface electron layer. (b) The increasing surface electron density screens the scattering from remote charges and thus enhances the buried electron mobility.

are shown in Fig. 6.7b. Here, the tunable $n_{surface}$ was calculated by starting with the change in electron density in the buried layer at the collapse voltage (adjusted for the slightly different gate capacitances from the gate to the buried versus the surface layers), and then scaling the value up by $C_{ox} \cdot \Delta V_G$ from that point. In stage III, the increase in gate voltage (2-3 V) results in a considerable increase in $n_{surface}$ from around 4.0×10^{11} cm^{-2} to over 1.0×10^{12} cm^{-2}, but only a marginal increase in n_{buried} ($<1.0\times10^{11}$ cm^{-2}). With the increases in $n_{surface}$, we do see the significant increase in Hall mobility (Fig. 6.7b). Here we note that we did look for a theory with the tunable shielding layer to fit, but so far we can not find one. Nevertheless, this result increases our confidence in attributing the enhancement in buried layer mobility to the strong screening by the surface electron layer.

6.3.3 Parallel Conduction in Stage IV

If we keep ramping up the bias in the equilibrium mode, a decrease in Hall mobility is eventually seen in all samples (stage IV in Fig. 6.6). Here we set the highest mobility as the boundary of stage III and IV. We calculated the surface electron mobility for

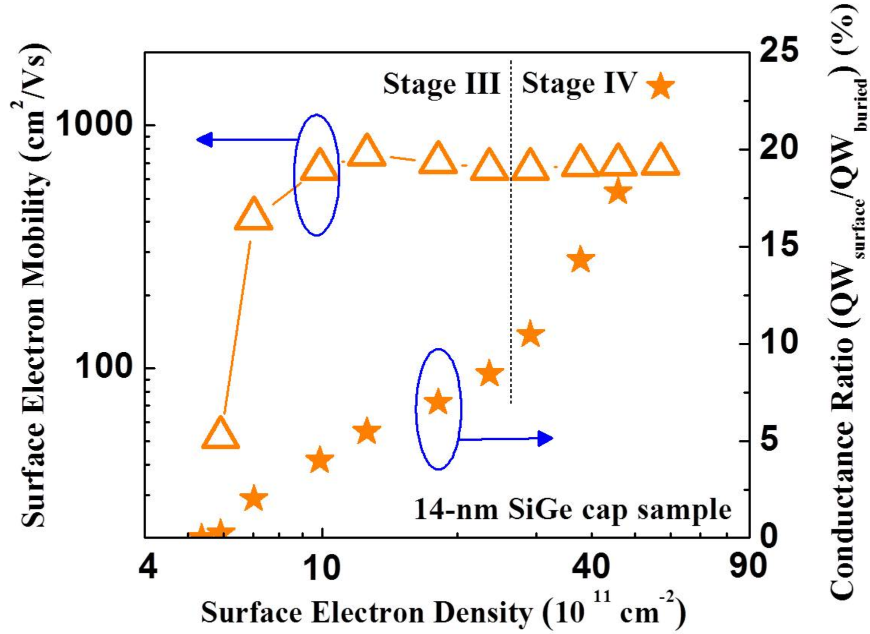


Figure 6.8: Surface electron mobility (calculated based on the parallel conduction model) versus the surface electron density (calculated in Sec. 6.3.2). The right Y axis shows the conductance ratio of the surface QW to the buried QW.

both stage III and stage IV (Take the 14-nm SiGe cap sample as an example again) based on the parallel conduction model described in [32], given n_{buried} is fixed at the lowest value after the density collapses. The relationship between surface electron mobility and $n_{surface}$ (calculated in Sec. 6.3.2) is then shown in Fig. 6.8, with the corresponding conductance ratio of the surface QW to the buried QW on the right Y axis. First, the increasing surface electron density leads to higher surface electron mobility in stages III as we expected. Similar to Hall electron mobility, surface electron mobility saturates with increasing $n_{surface}$ probably because of the interface roughness scattering. Second, due to the increases in both mobility and density, eventually the conductance in the surface layer becomes significant compared to that in the buried electron layer (<1% at the beginning of stage III to >10% in stage IV). Therefore, the Hall mobility (based on the total lateral conduction) is decreased as Hall electron density is increased [32].

6.3.4 Magneto-Resistance Transport Property at 0.3 K

In the previous discussions, the fundamental assumption we made is that the conduction of electrons in the surface QW is several orders of magnitude lower than that of electrons in the buried QW because electrons in the surface QW are too close to the unfavorable charged impurities at the interface. Hence, we believe the enhanced transport properties shown in stage III still represents the properties of the buried QW, even though measured $1/R_{xx}$ and $1/R_{xy}$ are the equivalent parallel conductivity, not the conductivity from a single layer. However, direct experimental evidence to show where the 2D electron layer is exactly located is still preferable. Therefore, several magneto-resistance transport measurements for samples shown in Fig. 6.6 were conducted under 0.3 K by Hao Deng in Prof. Shayegan′s group. In contrast to Hall measurements at 4.2 K, magneto-resistance transport measurements at 0.3 K were performed with much larger increment in gate biases due to the long scanning time to increase magnetic field up to 15 T. The data from two representative gate biases, 4 V in stage II and 9 V in stage III from the sample with a 20-nm SiGe cap, are highlighted in Fig. 6.9 in blue.

Clear Shubnikov-de Haas (SdH) oscillations in R_{xx} and quantum Hall plateaus in R_{xy} were observed at both 4 V and 9 V (Fig. 6.10). In stage II, the well-resolved and flat quantum Hall plateaus imply a good quality of the 2DEG. The SdH oscillation that touches zero several times and the single frequency extracted from a Fourier transform on R_{xx} at low field show a fact that no parallel conduction occurs at 4 V. The electron density extracted from the SdH oscillation at low field is ~3.87×10^{11} cm^{-2}.(Note that the saturation of the SdH oscillation peak at 12 T in Fig. 6.10a is an artifact.)

When the sample was biased in stage III, namely when the gate voltage was fixed at 9 V, a more ideal SdH oscillation and flatter quantum Hall plateaus at a lower density ~2.92×10^{11} cm^{-2} were observed (Fig. 6.10b). More filling factors with high

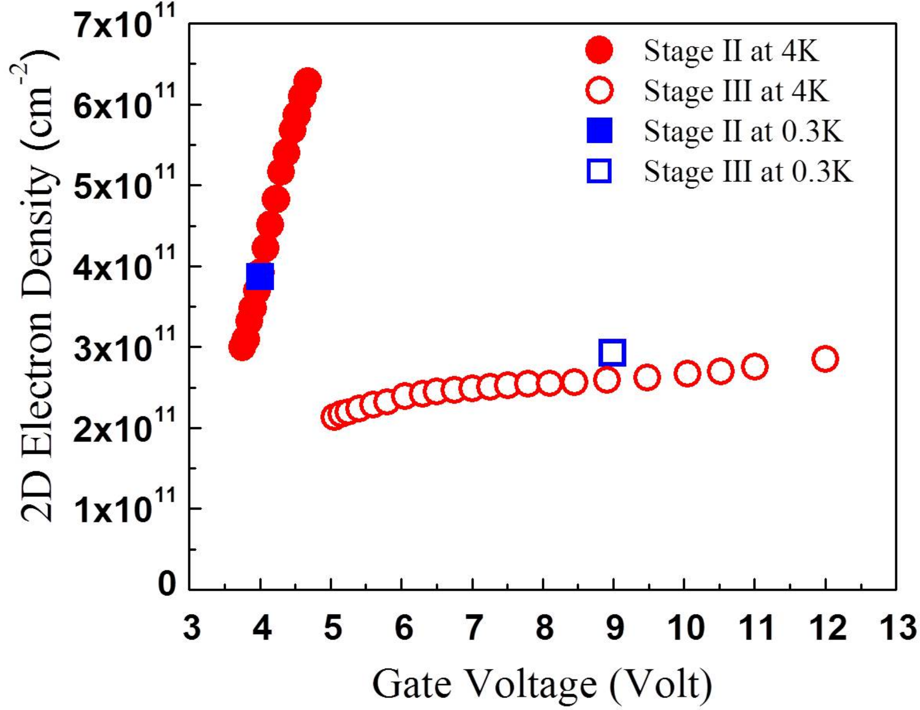
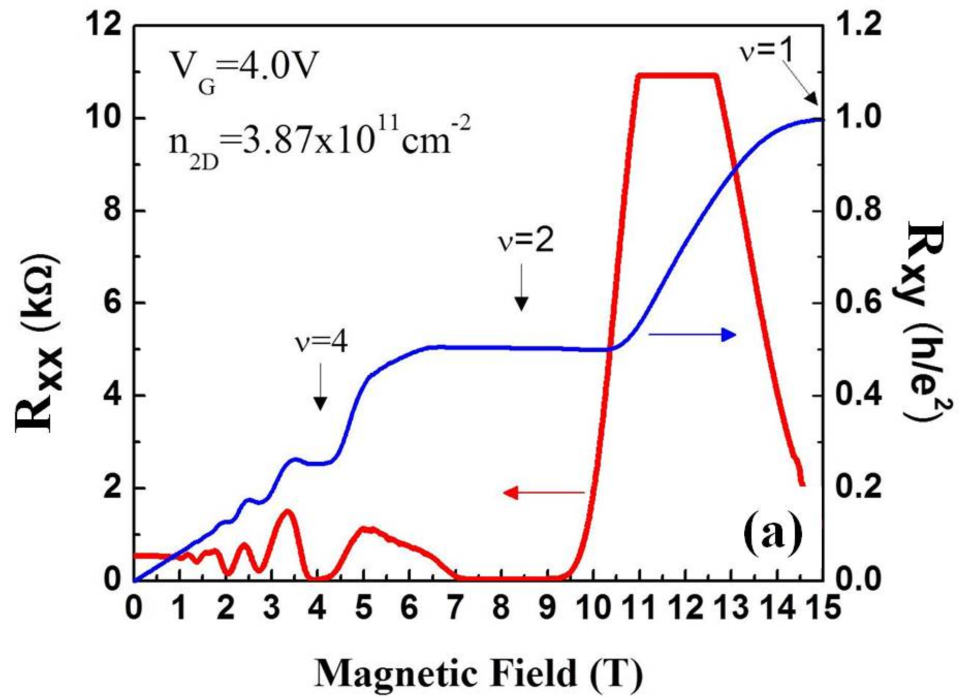


Figure 6.9: The four-stage behavior in density of the sample with a 20-nm SiGe cap measured by Hall measurement at 4.2 K (red). The sample was then dipped to 0.3 K for magneto-resistance transport measurement. Two representative gate biases used at 0.3 K were highlighted in blue.

orders were resolved at low magnetic field in both R_{xx} and R_{xy}. No overshoot in the left end of each plateau was observed as in the plateaus at 4 V. Furthermore, a fractional quantum Hall effect was identified at ν=4/3 between two large plateaus for ν=1 and ν=2. The above are all the signs that the 2DEG system at stage III becomes cleaner (because less influenced by scattering sites), most likely due to the screening effect we mentioned in previous sections. In addition, we also made a plot with R_{xx} v.s. 1/B from the sample with a 20-nm SiGe cap at low field (0.5 T-2.5 T) at 9 V (Fig. 6.11a). The frequency peaks with ratio of 1, 2 and 4 in the the Fourier transform on R_{xx} v.s. 1/B are observed (Fig. 6.11b).



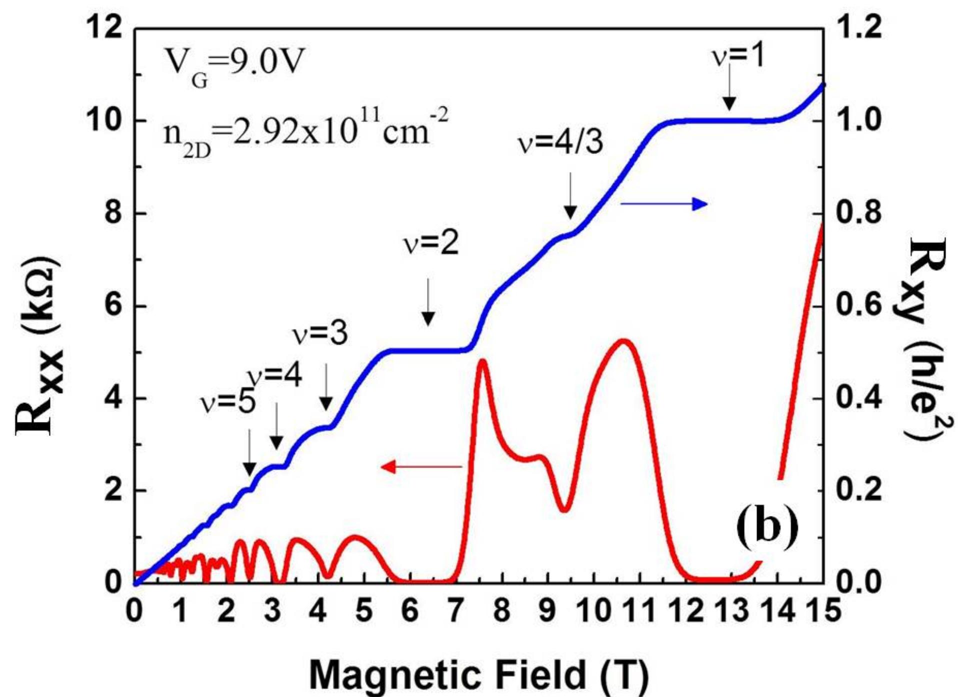


Figure 6.10: The magneto-resistance transport measurements at 0.3 K were shown versus magnetic field up to 15 T at (a) 4 V (stage II) and (b) 9 V (stage III).

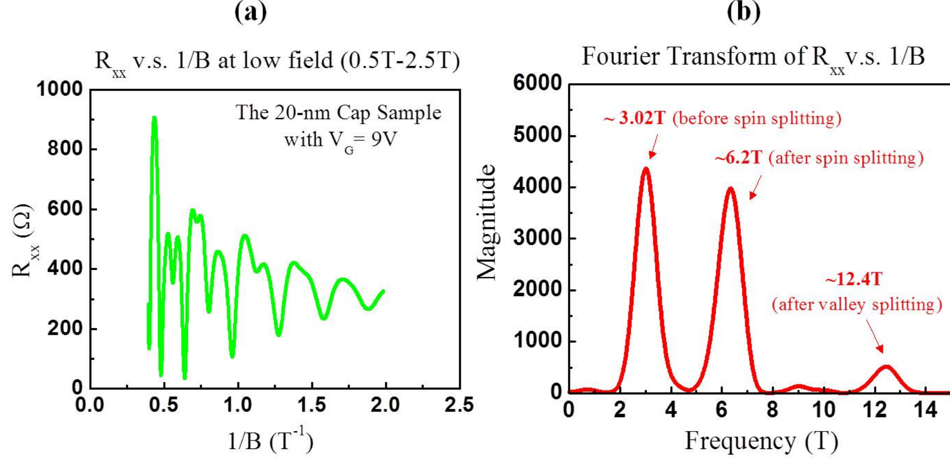


Figure 6.11: (a) R_{xx} versus the inverse of magnetic field from the sample with a 20-nm SiGe cap at 9 V in the range of 0.5 T to 2.5 T. (b) The Fourier transform of the curve in (a) shows three peaks. The ratio of frequencies show the different degeneracies, but they all represent the same conducting channel and a single electron density of 2.92×10^{11} cm^{-2}.

The peak at 3.02 T, 6.2 T and 12.4 T show 4 (2 spin degeneracies and 2 valley degeneracies), 2 (2 valley degeneracies), and 1 degeneracy (all degeneracies are split) at such magnetic fields, and a single electron density can be calculated by (e/h)×degeneracy×frequency, where e is the elementary charge and h is the Planck constant [32]. Therefore, all three peaks verify that only single significant lateral conducting path exists at stage III. In other words, our main assumption that Hall measurement data validly interprets transport property of the buried QW at stage III is proven correct. The best ambiguity in our theory can be finally ruled out.

6.3.5 Negligible Screening Effect in Thick-Cap 2DEGs

The exciting screening effect greatly improves the transport property of undoped 2DEGs with thin SiGe caps (<40 nm). In fact, an identical four stage behavior in density was also experimentally observed in 2DEGs with thicker SiGe caps (Fig. 6.12).

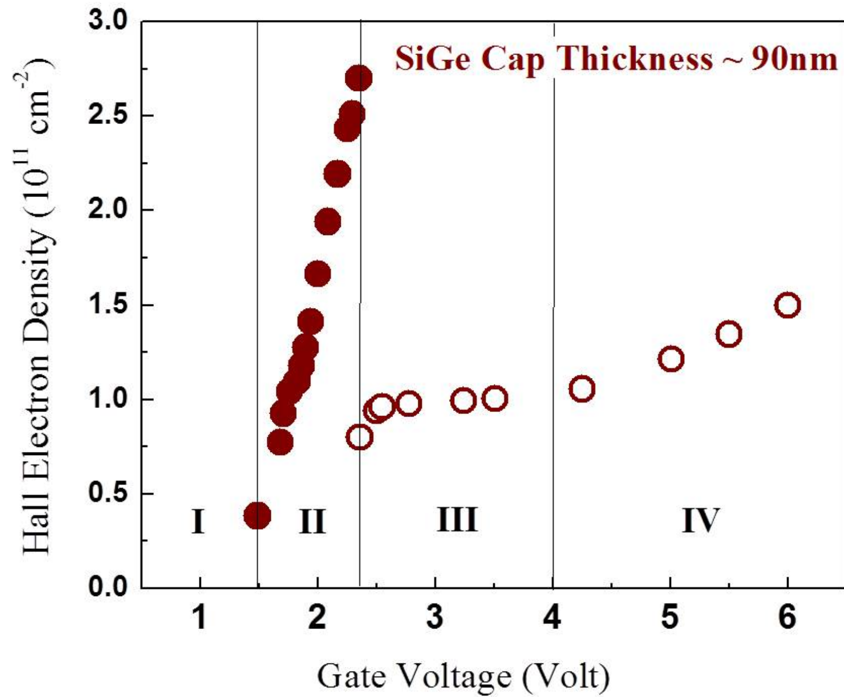


Figure 6.12: An identical four-stage behavior in density was also observed in samples with thicker SiGe caps (90 nm in this case).

However, the transport data from them were different from the thin cap samples: the significant improvement in mobility and critical density was not seen for these samples. As an example, mobility data at stage II (closed symbols) from a 2DEG with a 90-nm SiGe cap were plotted together with the data from stage III and IV (open symbols) in Fig. 6.13. In stage III, the increase in mobility with increasing density basically follows the data in stage II until it steps into the stage IV where the parallel conduction bends down the effective Hall mobility. An implicit message from the overlap between data in stage II and stage III is that the mobility-limiting mechanisms in undoped 2DEGs with thicker SiGe cap layers may not be remote scattering at the top surface anymore. As a result, the screening of remote charged impurities at the interface by the newly-formed surface electron layer is not effective to enhance electron mobility.

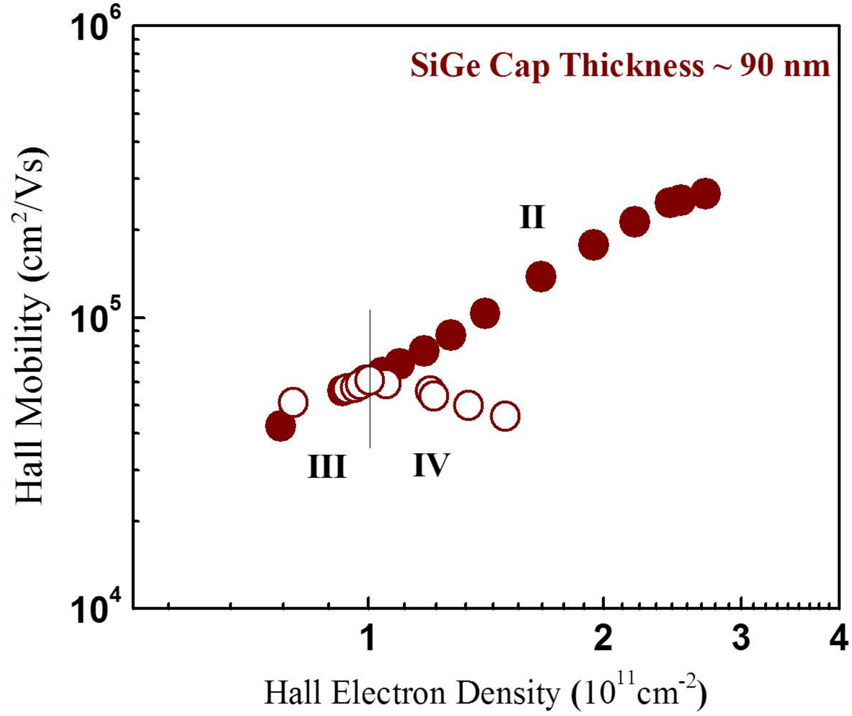


Figure 6.13: Mobility data of the 2DEG sample with a thick SiGe cap (90 nm). No significant screening effect was observed.

That surface potential fluctuations are not important in samples with thicker SiGe caps (big separation between the 2DEG and the surface) is in the end not surprising. However, the cap thicknesses of interests for quantum computing and other patterning 2DEG applications is under 60 nm, where our discovered tunable screening effect may play an important role.

6.4 Reverse V_G Scanning in Stage III

The unique four-stage behavior of densities in an enhancement-mode undoped 2DEG with thin SiGe cap (<40 nm) were analyzed in detail in Sec. 6.2. With the gate voltage ramping up, electrons start to accumulate in the buried QW until a critical electrical field is built up to trigger the whole positive feedback process. The density

collapses and then remains constant (to first order) even if the gate voltage increases couple volts when the system is in thermal equilibrium (stage III).

An interesting trial to reverse the gate voltage scanning direction has also been done in these 2DEGs with thin SiGe caps after reaching a high gate voltage in stage III. Here we take the 14-nm SiGe cap sample shown in Fig. 6.1 as an example again. When we scan the gate voltage down, n_{2D} basically remains the same level as we scan up until the gate voltage approaches the boundary between stage II and III. Near this boundary, a slight decrease in n_{2D} can be seen before the buried 2DEG became insulating again. We note that densities with the reverse bias scanning are not shown in this figure, but they are basically the same as those with the forward bias scanning in stage III.

A similar tendency under reverse bias scanning in stage III was observed in samples with thicker SiGe caps as well. The density data for both scanning directions from a 2DEG sample with a 75-nm SiGe cap are shown in Fig. 6.14 as an example. However, the extension of measurements under the gate voltages that are supposed to be classified into stage II was observed. Furthermore, when the gate voltage ramps down and passes the boundary of two stages, a linear decrease in n_{2D} occurs. The similar slopes extracted from this linear decrease at stage III (scan down) and the linear increase in n_{2D} at previous stage II (scan up) imply that we modulated the 2DEG in the buried QW in both scans.

The transport properties measured from this sample both under a regular voltage ramp-up at stage II (solid symbols) and a ramp-down at stage III (open symbols) are shown in Fig. 6.15. When ramping down, $n_{surface}$ decreases first and n_{buried} is constant, reversing the path in Fig. 6.3 (solid lines). Then, the surface layer becomes insulating, but with a higher density of electrons than the near zero amount when ramping up in stage II. Beyond this point, n_{buried} starts to decrease. However, there is now a screening layer trapped at the surface, so we expect improved transport

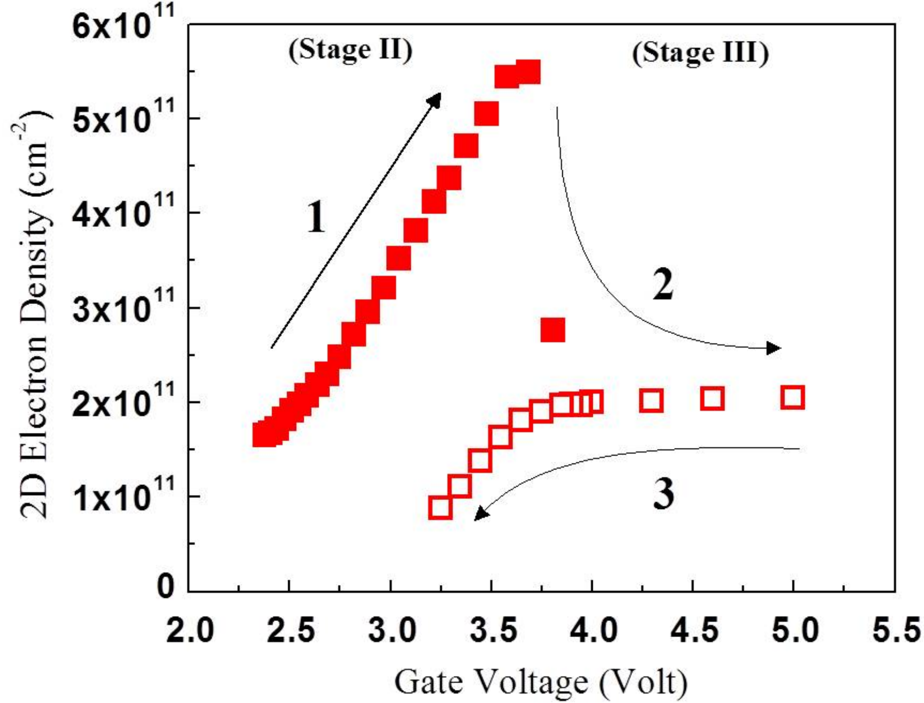


Figure 6.14: The modulation of electron density under two scanning directions of gate voltages. Electrons are first accumulated in the QW as the gate voltages ramp up at stage II (solid symbols, step 1) until a collapse occurs. The density then drops to a fixed value with further increasing biases (open symbols, step 2). Finally, the density remains constant as the gate voltages ramp down, followed by a linear decrease when the gate voltage crosses the boundary of two stages (open symbols, step 3). (This reference sample has a 75-nm SiGe cap layer and a 145-nm SiGe buffer)

properties. The lowest n_{2D} under a ramp-down at stage III (~8×10^{10} cm^{-2}) is about two times lower than that under a ramp-up at stage II (~1.6×10^{11} cm^{-2}).

For unknown reasons, the mobility is not improved during the downwards scan. This is not understood, but suggests again that different limiting factors may control minimum n_{2D} and mobility at high densities.

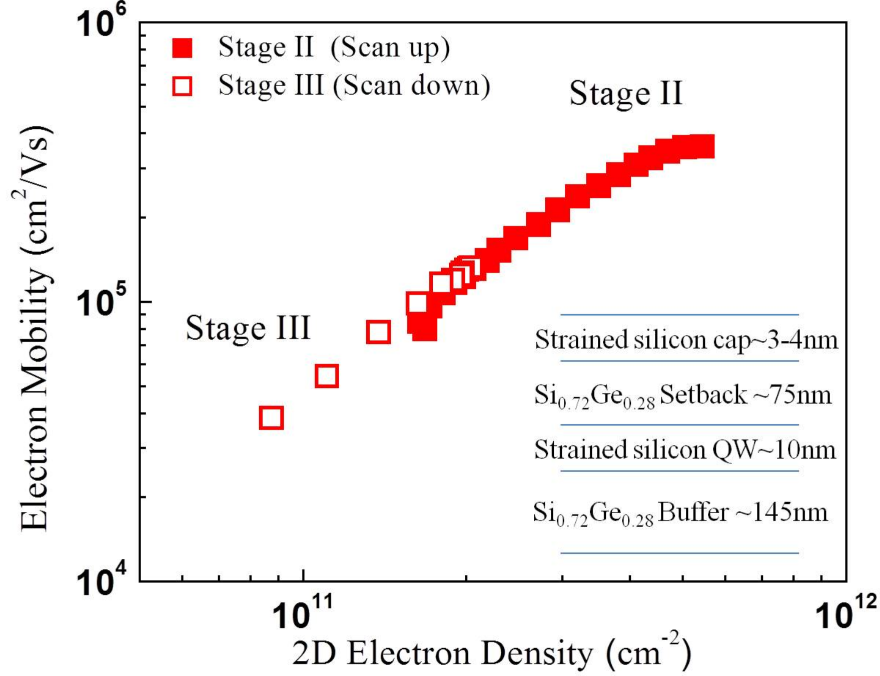


Figure 6.15: The transport property of a typical undoped 2DEG with a thick SiGe cap under a regular voltage ramp-up at stage II (solid symbols) and a voltage ramp-down at stage III (open symbols).

6.5 Summary

We have discovered a new physical effect: the strong screening of the remote charge scattering sites from the oxide/semiconductor interface in enhancement-mode undoped Si 2DEGs, by introducing a tunable shielding electron layer at the semiconductor surface. When a high density of electrons in the buried silicon quantum well exists, the tunneling of electrons from the buried layer to the surface quantum well can lead to the formation of a nearly immobile surface electron layer. The existence of this surface electron layer and the validity of Hall measurements under this circumstance have both been verified by magneto-resistance measurements at 0.3 K. The screening of the remote charges at the interface by this newly formed surface electron layer results in an increase in the mobility of the buried 2DEG. Furthermore,

a significant decrease in the minimum mobile electron density of the 2DEG occurs as well. Together, these effects can reduce the increased detrimental effect of interface charges as the cap distance for the 2DEG to the surface is reduced for improved lateral confinement by top gates. Finally, we have also showed the density data under both upwards and downwards bias scans. A 2× lower minimum n_{2D} was observed in stage III as the gate bias ramped down than that in stage II as the gate bias ramped up, while the mobility was not improved at the same time. This again concludes that the limiting mechanisms for minimum n_{2D} and mobility at high densities could be different.

Chapter 7

The Role of the Regrowth Interface on Undoped 2DEG Properties

7.1 Introduction

Because our experiments in Ch. 5 indicated possible remote scattering sites at the bottom interface (regrowth interface) in addition to that at the oxide/silicon interface, we began modeling the 2DEG densities for different pinning positions of the Fermi level at the substrate growth interface. The pinning of the Fermi level could be a reflection of a high number of defect states. Then, experimentally we varied the SiGe buffer thickness, which is the separation from the silicon channel to the regrowth interface, to examine its effect on 2DEG transport properties. A 2DEG with thick SiGe buffers (145 nm or greater) shows higher electron mobility and lower critical densities than that with thin SiGe buffers (70 nm or less). In addition, we also varied the baking condition of the regrowth interface before the epi-layer growth. The electron mobility is independent of the baking temperatures (or baking lamp powers), but a lower baking power reduces the critical density. The electron density of 3.2×10^{10} cm^{-2} measured from the sample with a 75-nm SiGe cap in stage III (scan

down) with a 18% baking power for 20 minutes was obtained, which is the lowest value over the published data with the similar SiGe cap thickness.

7.2 Fermi Level Pinning

7.2.1 Contamination at the Regrowth Interface

A high temperature baking (~1000 °C, or baking lamp power 23% with the new SCR power control unit) at 6 torr with 3 slpm hydrogen flow is necessary to remove the remnant oxide layer or other contamination on the surface of a silicon wafer before any epi-layer growth. However, cleaning the SiGe buffer before growth is always much more difficult mainly because high temperature cleaning (~1000 °C) may relax the SiGe graded buffer and introduce more defects into the substrate. Therefore, the common baking temperature for SiGe buffers before growth is controlled below 900 °C (18%-20% baking power, with the new SCR power control unit). Because of this lower baking temperature, high contamination levels are very common at the regrowth interface of typical undoped 2DEG samples grown in our lab by RTCVD (Fig. 7.1). At the regrowth interface, the oxygen and carbon concentrations are 1×10^{20} cm^{-3} and 5×10^{20} cm^{-3}, respectively, while those at the regrowth interface of a silicon wafer are typically below 1×10^{18} cm^{-3} (not shown here). The integral 2D densities of oxygen and carbon in Fig. 7.1 are 6×10^{13} cm^{-2} and 4×10^{14} cm^{-2}, respectively. Such high sheet densities very likely pin the Fermi level (E_F) at the regrowth interface, and affect the electron densities in the buried QW in thermal equilibrium. Here we note that P and B background concentrations are both below the SIMS detection limit over all layers, so we believe the Fermi level pinning, if any, is not caused by background dopants at the regrowth interface.

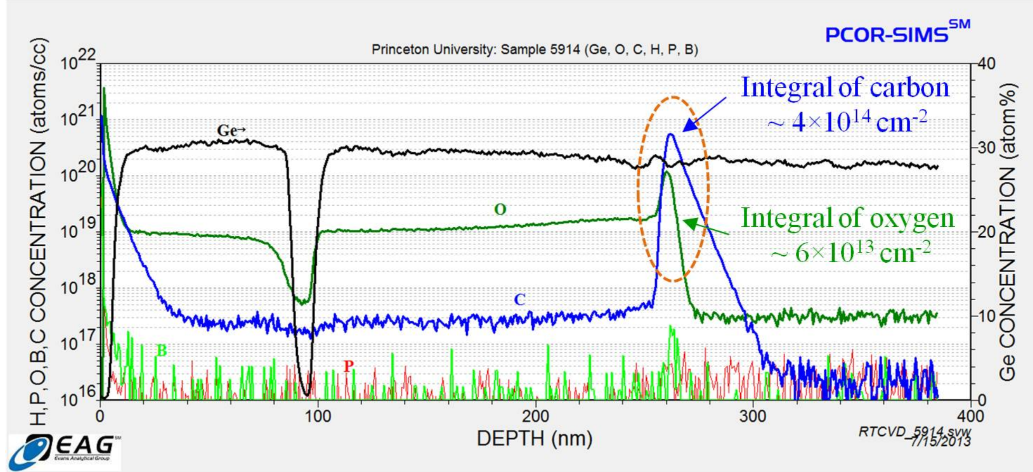


Figure 7.1: A typical SIMS of an undoped 2DEG shows very high densities of oxygen and carbon at the regrowth interface. The integral 2D densities of oxygen and carbon are 6×10^{13} cm^{-2} and 4×10^{14} cm^{-2}, respectively. A typical baking power for SiGe relaxed buffers is 20% for 5 minutes, which is roughly equal to 850 °C.

7.2.2 Fermi Level Pinning

To figure out the most likely pinning position in our samples, we calculated the theoretical maximum n_{2D} in equilibrium (The constant value indicated by the red solid line at high gate voltages in Fig. 6.3) by the Schodinger-Poisson sef-consistency (SPSC) simulator based on different pinning conditions [96]. The experimental maximum n_{2D} in the buried QW in equilibrium of our undoped 2DEG samples (for example, the constant value ~2×10^{11} cm^{-2} in stage III at high gate voltages in Fig. 6.14) are also collected for comparison.

The band diagrams of an undoped 2DEG at a bias 0.2 V with four different Fermi level pinning positions (0.045 eV below conduction band minimum (E_C), 0.25 eV below E_C, midgap and 0.045 eV above valence band maximum (E_V)) are shown in Fig. 7.2. The pinning positions are intentionally selected to cover all possible pinning situations. This example 2DEG layer structure consists of a 4-nm Si cap, a 60-nm SiGe cap, a 11-nm Si channel and a 180-nm SiGe buffer. The gate bias 0.2 V is used to show the situation where the ground state (E_0) of surface QW is still above

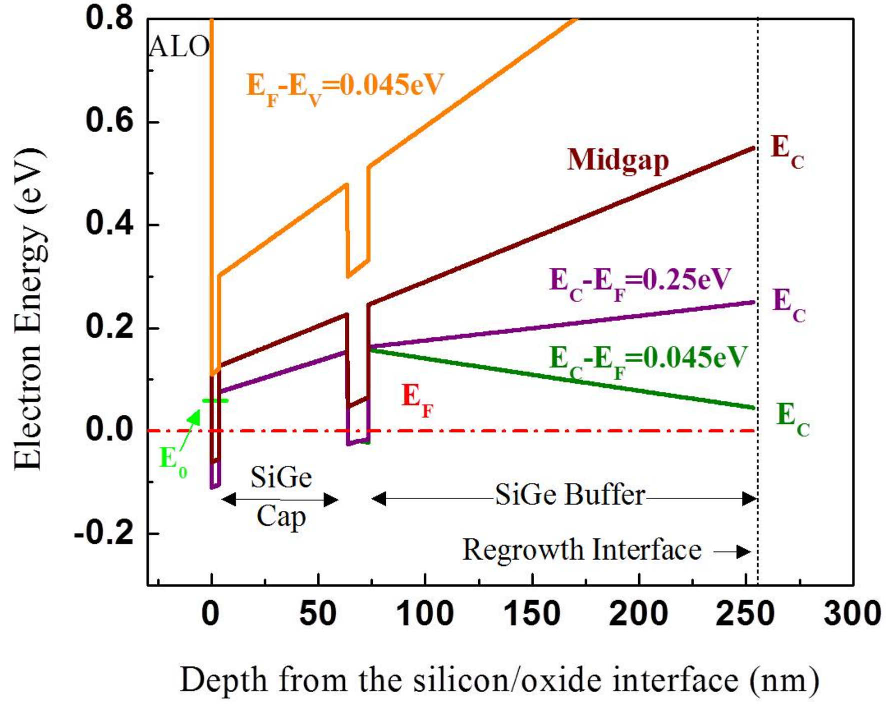


Figure 7.2: Band diagrams of an undoped 2DEG under a 0.2 V bias with the Fermi level pinned at four different positions: 0.045 eV below E_C (green), 0.25 eV below E_C (purple), mid-gap (brown) and 0.045 eV above E_V (orange).

the Fermi level for all pinning conditions. Other boundary conditions include the workfunction of the gate = 5.1 eV (Au) and the electron affinity of aluminum oxide (ALO) = 1 eV [97]. Under this bias, the buried QW with the Fermi level pinned at 0.045 eV and 0.25 eV below E_C touches the Fermi level already, with the ground state (E_0) of the surface QW still above the Fermi level, so electrons only accumulate in the buried QW. The electron density in the buried QW (n_{buried}) keeps increasing until the E_0 of the surface QW is lowered below the Fermi level. The further increase in the gate voltage increases the electron density in the surface QW ($n_{surface}$), with the n_{buried} fixed at a constant value, which is denoted as the theoretical maximum n_{2D} in equilibrium.

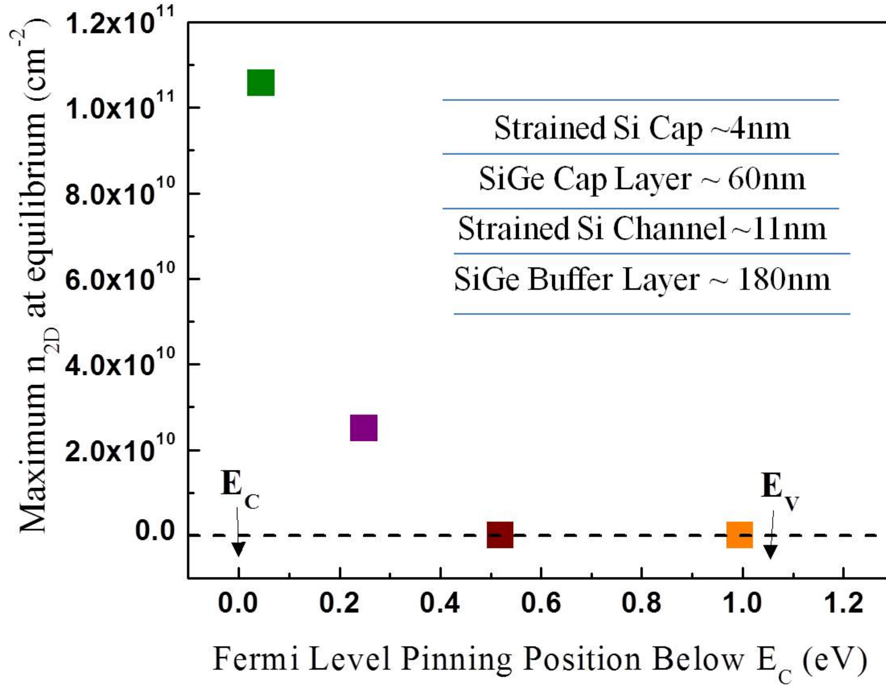


Figure 7.3: The theoretical maximum n_{2D} in equilibrium (with different biases) by the simulation with different pinning conditions. The inset shows the layer structure used in the simulation. (The band gap of $Si_{0.72}Ge_{0.28}$ is set as 1.04 eV [20])

We calculated the theoretical maximum n_{2D} in equilibrium with different pinning conditions based on the layer structure described above (Fig. 7.3). The maximum n_{2D} decreases when the pinning position of the Fermi level gets further below E_C, because it gets earlier for the E_0 of the surface QW to become lower than the Fermi level. For the case with the Fermi level pinned at mid gap or below, the E_0 of the surface QW is always lowered below the Fermi level first (earlier than that of the buried QW), and thus no electrons accumulate in the buried QW.

7.2.3 Comparison of Simulations and Experimental Data

Now the experimental maximum n_{2D} in stage III from our samples are added for comparison. Since the thicknesses of the SiGe cap layer and the SiGe buffer layer

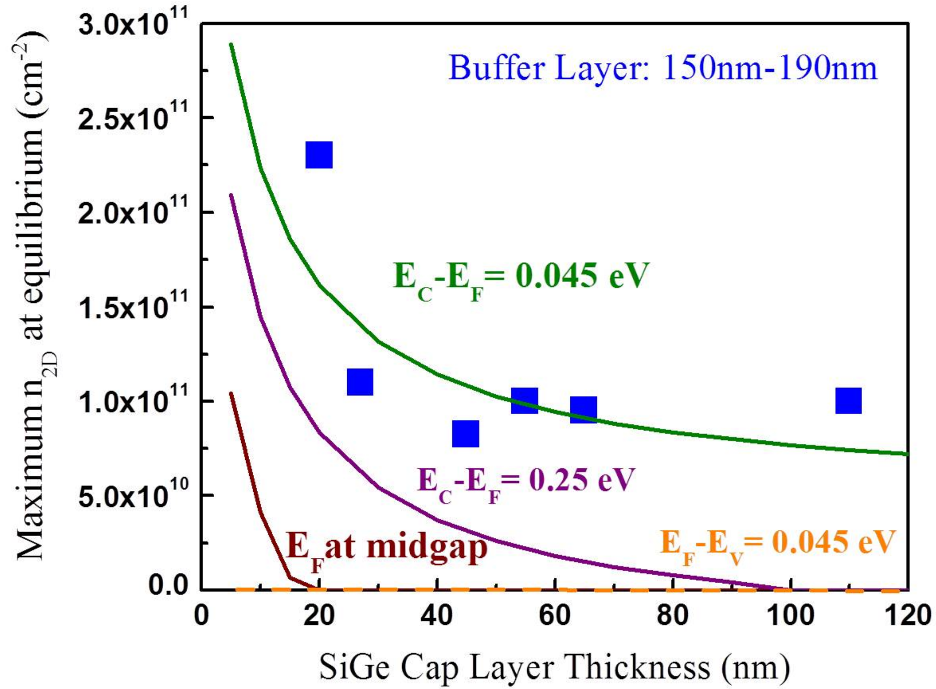


Figure 7.4: The experimental maximum n_{2D} at stage III, from samples whose buffer layers are between 150 nm and 190 nm, versus corresponding SiGe cap thickness. Simulations with a fixed buffer thickness (190 nm) and various E_F pining conditions are shown in green (E_C-E_F =0.045 eV), purple (E_C-E_F=0.25 eV) and brown (E_F at midgap) solid lines and an orange dash line (E_F-E_V =0.045 eV).

both affect theoretical maximum n_{2D}, we vary one parameter each time with another one fixed. For the simulations in Fig 7.4, we vary the thickness of SiGe cap layer in the simulation with the SiGe buffer layer fixed at 190 nm for four different Fermi level pinning positions. The experimental data are shown in blue solid symbols, and their SiGe buffer layers are in the range of 150 nm to 190 nm. It is clear that, when the Fermi level is pinned at 0.045 eV below E_C, the simulation curve fits our experimental data best. With the Fermi level pinning position moving away from E_C, the simulated maximum n_{2D} becomes lower, and eventually no electrons are accumulated in the buried QW because electrons are populated in the surface QW earlier.

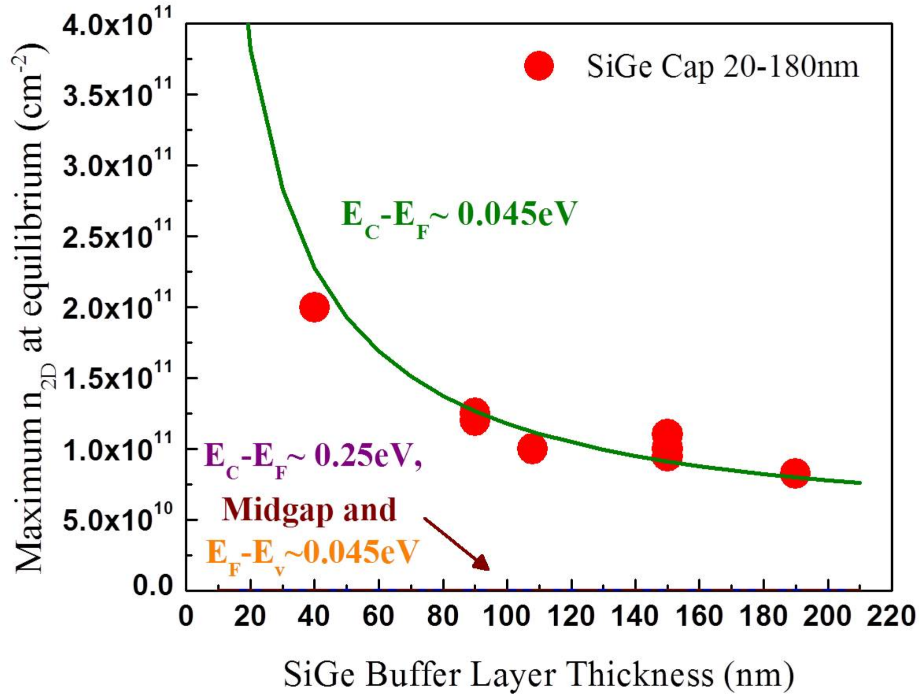


Figure 7.5: The experimental maximum of n_{2D} at stage III from samples whose SiGe cap layers are between 20 nm and 180 nm versus corresponding SiGe buffer layer thickness. The simulations were done with a fixed buffer thickness (190 nm). The simulation curve with the pinning position (E_C-E_F =0.045 eV) in green fits the data best.

Here we note that since the front boundary condition (E_C - E_F = metal workfunction - electron affinity of the insulator) and the bottom boundary condition (Four different Fermi level pinning conditions as shown above) are both fixed, a thicker SiGe cap increases the distance between two boundaries, and reduces the built-in electrical field under the zero bias. Therefore, less increase in gate voltage is needed, after electrons start accumulating in the buried QW, to get E_0 of the surface QW below the Fermi level. Thus a lower n_{buried} is obtained in samples with thicker SiGe cap layers.

Fig 7.5 shows the experimental maximum n_{2D} (red solid symbols with SiGe cap thicknesses in the range of 20 nm to 180 nm) with the simulation curves in which we

vary the SiGe buffer thickness with a fixed SiGe cap thickness at 90 nm. Again, the simulation curve with the Fermi level pinned at 0.045 eV below E_C fits our experimental data best. All other pinning conditions do not allow electrons to accumulate in the buried QW over the wide range of SiGe buffer layer thicknesses, because E_0 of the surface QW is always lowered below the Fermi level earlier than that of the buried QW.

Many other factors also affect the simulation results of the theoretical maximum n_{2D} in equilibrium. For example, the theoretical maximum density strongly depends on background doping concentration in an undoped 2DEG. Higher background doping density may provide unexpected electron accumulation at both silicon QWs. However, based on our SIMS results, we have ensured that the concentration of background impurities in our undoped 2DEG is below 1×10^{14} cm^{-3} (Fig. 5.15). Such low doping levels have been verified to cause no effect on the simulation results.

7.3 Effects of Regrowth Interface on 2DEG Properties: Thickness of SiGe Buffer

Various mobility-limiting mechanisms have been discussed in Ch. 5, and remote scattering was viewed as the most dominant scattering mechanism that limits mobility in our system. However, we also pointed out in Sec. 5.6 that there seems to be an upper limit that stops the mobility curves from moving upwards and limits the highest mobility to 400,000 cm^2/Vs, irrespective of the increasing thickness of SiGe cap above the 2DEG over 40 nm (Fig. 5.16). Interface roughness scattering and the effect of threading dislocations were examined, but none of them were identified as the real mobility-limiting factor.

We note that most samples in earlier experiments have similar thickness of SiGe buffer layer (~165 nm), which is also the distance from the channel to their bottom

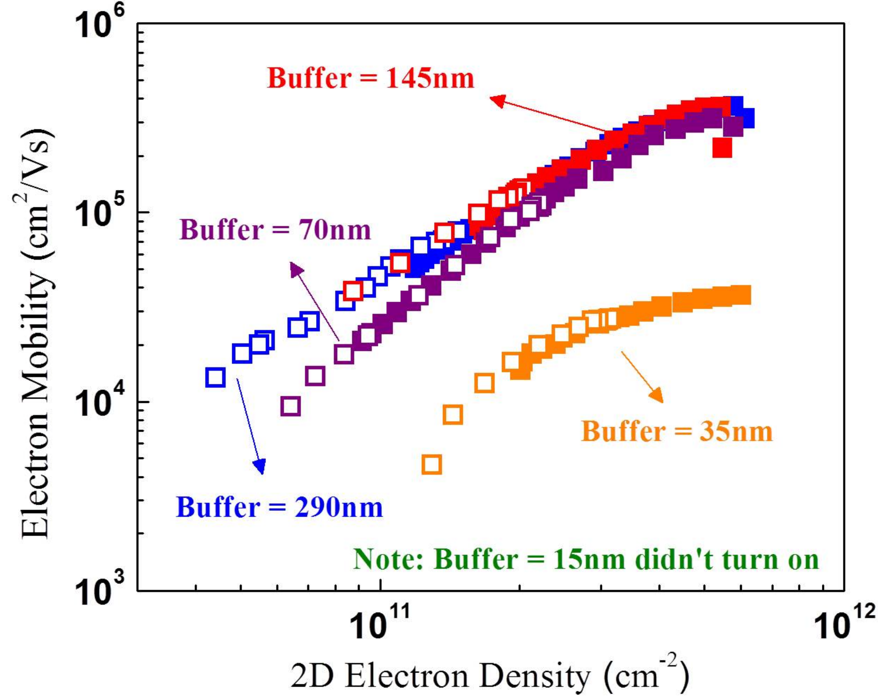


Figure 7.6: Transport properties of samples with various SiGe buffer layer thicknesses. Solid and open symbols represent data measured in stage II (scan up) and stage III (scan down), respectively.

interfaces (regrowth interfaces). In Sec. 7.2.1, high concentrations of contamination (Fig. 7.1) were observed at the regrowth interface, which also cause remote scattering. In other words, there may be two sheets of remote charged impurities existing in our 2DEGs. To verify this argument, we grew a set of samples with various thicknesses of the SiGe buffer layer from 15 nm to 290 nm, with the distance between the surface and the channel fixed (i.e., a fixed SiGe cap layer ~75 nm). Fig. 7.6 shows transport properties of these samples.

A clear degradation in mobility is indeed seen in the samples with a buffer below 145 nm down to 35 nm. Further, the channel couldn't even be turned on in the sample with a 15-nm buffer layer. However, mobility curves of samples with a buffer layer

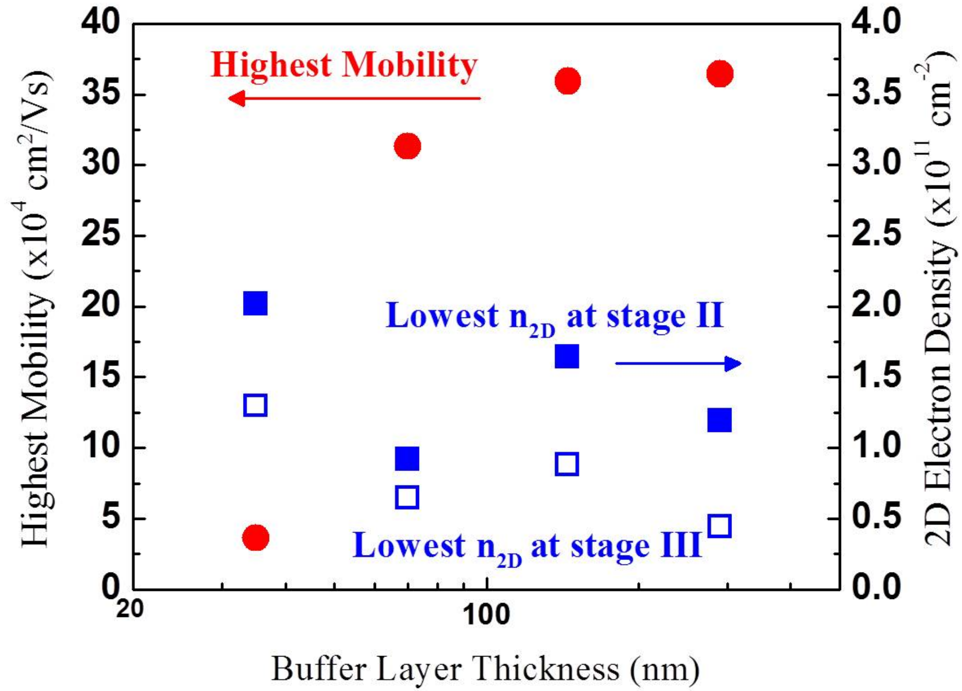


Figure 7.7: Highest mobility and critical densities (the lowest n_{2D}) at both stage II (scan up) and stage III (scan down, as shown in Fig. 6.14) extracted from samples with various thicknesses of SiGe buffer layers. The blue solid and blue open symbols are the lowest n_{2D} at stage II and stage III, respectively.

of 145 nm or greater are still limited at the same level with the highest mobility at about 400,000 cm^2/Vs

In addition, a thicker buffer layer also helps with the reduction of critical densities, both at stage II and stage III. For example, the critical densities (the lowest n_{2D}) at stage II (scan up) and stage III (scan down) of the sample with a 290-nm buffer are about 1.2×10^{11} cm^{-2} and 4.5×10^{10} cm^{-2}, which are two times lower than those of the sample with a 35-nm buffer (~2.1×10^{11} cm^{-2} and 1.3×10^{11} cm^{-2}) (Fig. 7.7).

7.4 Effects of Baking Power at the Regrowth Interface

To improve the quality of the regrowth interface, we varied the baking power of the regrowth interfaces before growing any epi-layers. Except for the baking temperature, all other parameters were intentionally kept the same, including a ~75-nm SiGe cap layer and a 145-nm SiGe buffer layer. As we mentioned in Sec. 2.1.2 , the percentage of full lamp power (baking power) will be used instead of temperature in the following discussion because all the baking temperatures are higher than 750 °C, which is the upper limit of the temperature measurement system in our RTCVD.

A series of transport properties from samples with various baking powers from 18% to 22% (with the new SCR power control unit) are shown in Fig. 7.8. Baking with 20% power for 5 minutes is our standard cleanning recipe for samples shown in Sec. 6.4. Again, all the highest mobilities and critical densities at stage II (scan up) and stage III (scan down) of these samples are extracted for comparison (Fig. 7.9). Mobility curves in Fig. 7.8 do not move upwards, with the highest mobilities still below 400,000 cm^2/Vs, regardless of the baking temperatures. The highest mobilities remain at the same level except for a small drop in mobility of the sample with 21% baking power for unknown reasons.

However, we do see an improvement in critical density at both stage II (scan up) and stage III (scan down) with a decreasing baking power. The critical density at stage III measured from the sample with 18% baking is as low as 3.2×10^{10} cm^{-2}, five times lower than that measured from the sample with 22% baking (1.6×10^{11} cm^{-2}). To the best of our knowledge, this extremely low 2D electron density of 3.2×10^{10} cm^{-2} in an undoped silicon 2DEG with a 75-nm SiGe cap is the lowest value among all the published data with a similar SiGe thickness.

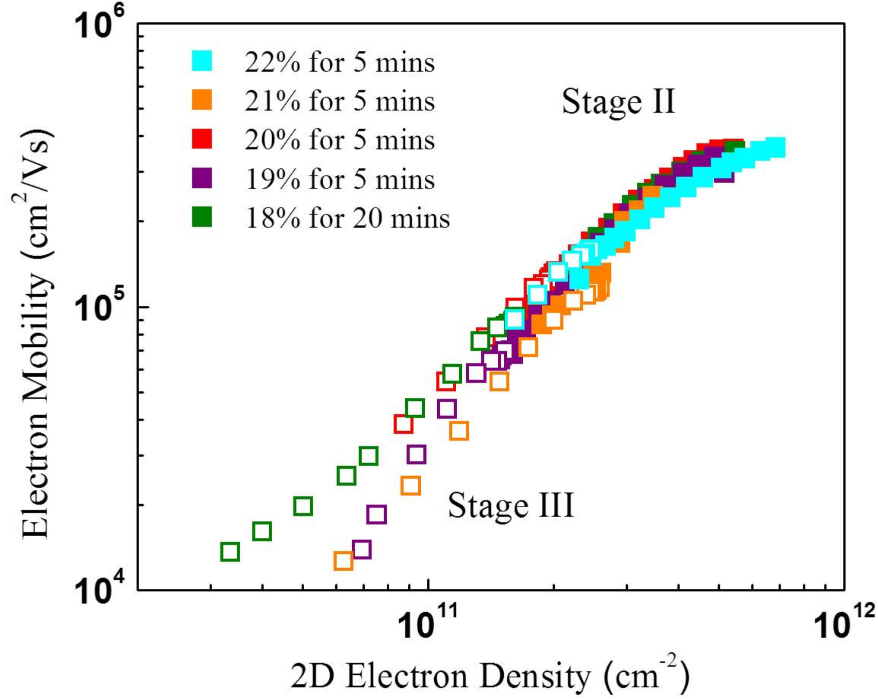


Figure 7.8: Mobility curves from samples with various baking powers. Solid and open symbols represent data measured in stage II (scan up) and stage III (scan down), respectively.

It is still unclear why a lower baking power leads to a lower critical density. It could stem from distinct E_F pinning positions at the regrowth interface after different temperature baking. Further reducing baking power below 18% leads to a difficulty in cleaning the regrowth interface. In fact, it has been very difficult to clean the regrowth interface at even 18% baking power for 5 minutes. The surface of an as-grown sample with an 18% baking was completely hazy after the epitaxy for a 2DEG structure, so we think a low baking temperature may not be effective to remove native oxides or remnant water molecules on a relaxed SiGe substrate. Thus, we lengthened the baking time from the regular 5 minutes to 20 minutes to enhance the cleaning process at 18% baking power. The extended baking time did help regrowth interface cleaning and provided us with a small clean area on an as-grown 2DEG to make a

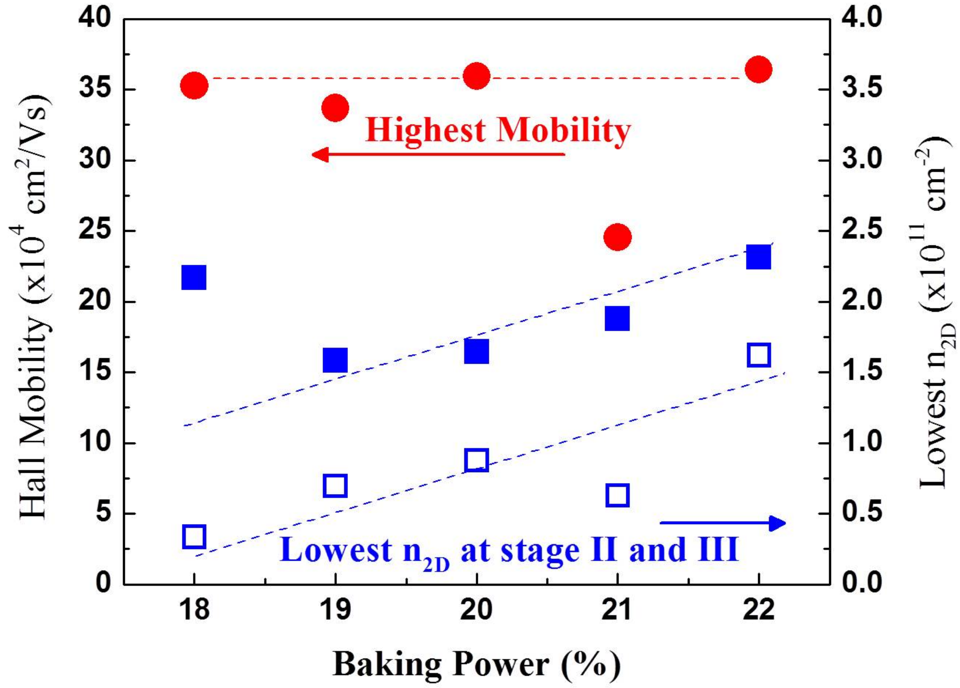


Figure 7.9: Highest mobility and critical densities at both stage II (scan up) and stage III (scan down) extracted from samples with various baking powers. The lowest n_{2D} at stage II and stage III are blue solid and blue open symbols, respectively.

Hall bar device out of it, but roughly 75% of the sample surface was still hazy, making a low baking process impractical.

7.5 Summary

The Fermi level pinning position at the regrowth interface in our 2DEGs has been identified to be very likely near the conduction band minimum, because with Fermi level pinned near E_C, the theoretical maximum 2D electron densities predicted by the simulation showed a good match with experimental data. The remote scattering from bottom interface (regrowth interface) was then examined by means of comparison in mobility curve and critical densities at both stage II (scan up) and stage III (scan

down). A thicker SiGe buffer layer leads to higher electron mobility and lower critical density. Therefore, a buffer layer thicker than 150 nm is recommended for an undoped 2DEG growth to obtain better transport properties. In addition, a lower baking power at the regrowth interface reduces the minimum n_{2D}. A density of 3.2×10^{10} cm^{-2} was obtained for a sample with a 75-nm SiGe cap thickness, which is the lowest value among the published data with a similar SiGe cap thickness. However, the upper limit of the highest electron mobility (400,000 cm^2/Vs) under all conditions still strongly suggests the existence of some other mobility-limiting mechanisms.

Chapter 8

Conclusions

8.1 Conclusions

The realization of a spin-based quantum bit in the form of a single-electron quantum dot device motivated the work in this thesis. The benefits of silicon, such as its inherently long spin coherence time and high compatibility with facilities in industry, make silicon-based material favorable to fabricate single-electron quantum dot devices for spin manipulation. We take advantage of the conduction band offset resulting from the tensile strain in a silicon layer grown pseudomorphically between relaxed SiGe layers to confine a 2DEG in such a quantum well. Both modulation-doped 2DEGs and enhancement-mode undoped 2DEGs were explored and the feasibility as a platform to isolate a single electron in a quantum dot was also evaluated in this thesis. Introductions to both types of 2DEGs and their practical quantum dot devices were given in Ch. 2, combined with an elaboration of our epitaxial growth system and growth details for Si/SiGe heterostructures used in this study.

In Ch. 3, successful suppression of the detrimental phosphorus surface segregation observed in modulation-doped strained silicon 2DEGs were demonstrated. By means of lowering the growth temperature for the SiGe cap layer from 575 °C down to

525 °C after a doping layer growth, a high hydrogen surface coverage was preserved, which blocked the segregation paths for phosphorus atoms in the sub-surface layer. Experimentally, this 50 degree temperature difference enabled a two order of magnitude reduction in surface phosphorus concentration (10^{18} cm^{-3} to 10^{16} cm^{-3}) in doped 2DEGs with a SiGe cap layer thinner than 40 nm. As a result, the lower surface electrical field greatly reduced the gate leakage current in a Schottky gated 2DEG. The resulting tremendous improvement in the breakdown voltage of those Schottky gates (-2 V to -7 V) enabled us to fabricate quantum point contacts (QPCs) without any significant leakage.

A demonstration of the lateral electrical isolation of doped 2DEGs at 4.2 K by ion implantation of silicon and argon was shown in Ch. 4. As an alternative for electrical isolation of quantum devices fabricated on modulation-doped 2DEGs, implant isolation in contrast to conventional mesa etching, preserves surface planarization and thus prevents corner-induced gate leakages. The sheet resistance at 4.2 K in an as-implanted 2DEG was as high as 1×10^{13} $\Omega/\Box$. The stability of damage induced by ion implantation was stable up to 550 °C, high enough for common processes for quantum devices in Si/SiGe heterostructures, such as the aluminum oxide deposition by ALD at 300 °C and the implant contact annealing at 550 °C. Finally, the 2DEG quality in terms of electron mobility was experimentally proven to remain intact after implantation, which convinces us of the reliability of implant isolation for 2DEG-based quantum devices.

The major scattering mechanisms that may limit electron mobility and critical electron density of an enhancement-mode undoped silicon 2DEG grown by RTCVD were first identified, theoretically and experimentally, in Ch. 5. Efforts to alleviate various mobility-limiting factors, such as the influence from charged impurities, successfully allowed for mobility at 4.2 K as high as 400,000 cm^2/Vs and the critical density as low as 4×10^{10} cm^{-2} in undoped 2DEGs with a SiGe cap as thin as 60 nm.

In addition, various experiments such as the variation of silicon growth temperature in the range of 575 °C to 700 °C have been conducted as well. The different growth temperatures as expected resulted in desirable variations in both Si/SiGe interface roughness and threading dislocation density in a series of undoped 2DEGs, which revealed the rarely known influence from the interface roughness scattering and the scattering from threading dislocations. These experiments showed that low silicon growth temperatures (625 °C or lower) for silicon QWs in an undoped 2DEG are preferred for better transport properties.

In Ch. 6, we described the discovery of a strong tunable screening effect, which is resulted from an induced surface electron layer in enhancement-mode undoped 2DEGs with thin SiGe caps (<40 nm). It has two major benefits: much enhanced mobility and reduced critical density. The argument that the formation of this surface electron layer switched a 2DEG system from non-equilibrium back to thermal equilibrium was in good agreement with the simulation results. The dominant scattering sources at the oxide/silicon interface were effectively screened by those shielding surface electrons. The resultant weaker Coulomb forces and potential fluctuations explained the impressive improvement in transport properties of undoped 2DEGs with thin SiGe caps, in which the capability for sharp electron patterning was preserved. An improved critical density was also observed after we reversed the scanning direction of the bias at high gate voltages, because the shielding electron layer is trapped at the oxide/silicon interface. A 2× lower critical density (~8×10^{10} cm^{-2}) in stage III (scan down) than that (~1.6×10^{11} cm^{-2}) in stage II (scan up) was observed in an example sample, but the mobility remained the same. This again concludes electron mobility and critical density may have different limiting mechanisms.

Extensive investigations into the bottom interface (regrowth interface) have been done in Ch. 7 by means of experiments and theoretical simulations. The Fermi level in an undoped 2DEG was found to be very likely pinned near the conduction

band minimum. The effect of remote scattering from the regrowth interface was also discussed. With a thick SiGe buffer layer (290 nm), a low critical density around 4×10^{10} cm^{-2} was observed with electron mobility as high as 400,000 cm^2/Vs. However, mobility gets decreasing with a thinner SiGe buffer layer (75 nm or less) because the remote scattering from the regrowth interface becomes stronger. In addition, with a low baking power for the regrowth interface (18% for 20 minutes), a density of 3×10^{10} cm^{-2} was observed in the sample with a 75-nm SiGe cap in stage III when a gate voltage ramped down, which is the lowest value among the published data with a similar SiGe cap thickness.

8.2 Future Work

8.2.1 Unknown Mobility-Limiting Factors

Much effort regarding quantum computing has built a solid foundation in the past few decades. We may have seen the dawn of the quantum computing era, even though there is still a long way to go for the debut of a quantum computer. We have measured electron mobility at 4.2 K as high as 400,000 cm^2/Vs in our undoped 2DEGs that may provide a promising platform to realize a spin-based quantum bit. However, we are still not able to establish the real mobility-limiting factors hidden in our samples at the low density regime . Various scattering mechanisms such as remote scattering, background scattering, interface roughness scattering and scattering from threading dislocations have been evaluated, but eventually ruled out as our mobility ceiling. Nevertheless, dislocation defects other than threading dislocations in relaxed SiGe layers, which can′t easily be revealed by wet etching, could still play a role in our 2DEGs. Huang et al. [78] reported that higher electron mobility could be achieved by growing Si/SiGe heterostructures with a lower Ge fraction. They claimed that the lower density of threading dislocations in a 2DEG with a lower Ge fraction enabled

the high electron mobility, though we have verified that scattering from threading dislocations in our samples is insignificant. However, some other invisible dislocation defects may still exist in SiGe layers due to the imperfection of crystalline structure and mismatched lattice constant. It is worth trying to grow Si/SiGe heterostructures on a SiGe virtual substrate with lower Ge fractions, hopefully with lower defect densities. We may see the effect, either significant or insignificant, from Ge fraction on electron mobility easily.

Silane became our main silicon precursor five years ago when we introduced the new gas supply system. We avoided using dichlorosilane (DCS) to avoid corrosive issues. However, without the additional in-situ cleaning by chlorine atoms in DCS, oxygen and carbon levels are at least two times higher in both Si and SiGe epi-layers, compared to the growth using DCS, after this precursor replacement. It is still unclear if these incorporated contamination atoms are scattering sources. More experiments are necessary to identify their charge types combined with the investigation of their potential influence on electron mobility.

8.2.2 Isotopically-Enriched Undoped 2DEGs for a Longer Spin Coherence Time

As we mentioned above repeatedly, silicon-based materials are favorable for spin-based qubits because of their naturally weaker hyperfine interaction and resultant longer spin coherence time. Enhanced mobility of an undoped 2DEG represents a great reduction in the density of charged impurities both in the epi-layers and at the oxide/silicon interface. This is may lead to a longer spin coherence time because of fewer scattering sources that may interfere with spin stability. Recently, spintronics experts noticed the importance of silicon and germane isotopes and how they affect the spin coherence time. For example, silicon consists of three stable isotopes with their natural abundances as 92.2% ^{28}Si, 4.7% ^{29}Si and 3.1% ^{30}Si [98]. Among them,

only ^{29}Si has non-zero nuclear spin, which scatters electron spin and thus reduces spin coherence time. Li et. al. [99] grew a strained silicon channel in undoped 2DEGs with isotopically enriched silane. The concentration of isotope ^{28}Si with zero nuclear spin was successfully increased up to 99.72%, while isotope ^{29}Si was lowered down to 0.08%, which translates to a spin dephasing time around 2 μs [100], six times higher than that measured in a silicon QD device grown by the natural silane. Although electrons used for spin manipulation are located in strained silicon channel, the nearby SiGe layers are also considered to be another source responsible for spin dephasing because ^{73}Ge (7.8%) (1 out of five stable Ge isotopes) possesses non-zero nuclear spin, similar to ^{29}Si. A undoped silicon 2DEG in the Si/SiGe heterostructures grown by both isotopically enriched silane and germane is thus promising to achieve unprecedentedly long spin coherence time, that may greatly advance the feasibility of a spin-based qubit.

Appendix A

Publications and Presentations

A.1 Journal Articles and Conference Papers

1. **C.-T. Huang**, J.-Y. Li, and J. C. Sturm, "Screening of remote charge scattering sites at the oxide/silicon interface of undoped enhancement-mode Si/SiGe two-dimensional electron gases," *Appl. Phys. Lett.*, vol. 104, p. 243510 (2014)

2. J.-Y. Li, **C.-T. Huang**, L. P. Rokhinson, and J. C. Sturm, "Extremely high electron mobility in isotopically enriched ^{28}Si quantum wells grown by chemical vapor deposition," *Appl. Phys. Lett.*, vol. 103, p. 162105 (2013)

3. **C.-T. Huang**, J.-Y. Li, and J. C. Sturm, "Very low electron density in undoped enhancement-mode Si/SiGe two-dimensional electron gases with thin SiGe cap layers," *ECS Transactions*, vol. 53, p. 45-50 (2013)

4. **C.-T. Huang**, J.-Y. Li, and J. C. Sturm, "Implant isolation of silicon two-dimensional electron gases at 4.2 K," *Electron Device Lett.*, vol. 34, p. 21-23 (2013)

5. J.-Y. Li, **C.-T. Huang**, L. P. Rokhinson, and J. C. Sturm, "Extremely low electron density in a modulation-doped Si/SiGe two-dimensional electron gas by effective Schottky gating," *ECS Transactions*, vol. 50, p. 145-149 (2012)

6. J.-Y. Li, **C.-T. Huang**, J. C. Sturm, "The effect of hydrogen on the surface segregation of phosphorus in epitaxially grown relaxed $Si_{0.7}Ge_{0.3}$ films by rapid thermal chemical vapor deposition," *Appl. Phys. Lett.*, vol. 101, p. 142112 (2012)

A.2 Conference Presentations

1. **C.-T. Huang**, J.-Y. Li, and J. C. Sturm, "Very low electron density in undoped enhancement-mode Si/SiGe two-dimensional electron gases with thin SiGe cap layers," *223rd Meeting of the Electrochemical Society*, Toronto, ON, Canada, May 12-17 (2013)

2. J.-Y Li, **C.-T. Huang**, L. P. Rokhinson, and J. C. Sturm, "Extremely low electron density in a modulation-doped Si/SiGe 2DEG by effective Schottky gating," *222nd Meeting of the Electrochemical Society*, Honolulu, HI, Octobor 7-12 (2012)

3. J.-Y. Li, **C.-T. Huang**, and J. C. Sturm, "Extremely sharp phosphorus turn-off slope and effect of hydrogen on phosphorus surface segregation in epitaxially-grown relaxed $Si_{0.7}Ge_{0.3}$ by RTCVD," *International SiGe Technology and Device Meeting*, Berkeley, CA, June 4-6 (2012)

4. **C.-T. Huang**, J.-Y. Li, and J. C. Sturm, "High breakdown voltage Schottky gating of doped Si/SiGe 2DEG system enabled by suppression of phosphorus

surface segregation," *International SiGe Technology and Device Meeting*, Berkeley, CA, June 4-6 (2012)

5. J.-Y. Li, **C.-T. Huang**, L. Rokhinson, J. A. Ohlhausen, M. S. Carroll, and J.C. Sturm, "High quality two-dimensional electron gases (2DEGs) in isotopically-enriched strained Si," *2012 APS March Meeting Session*, Boston, MA, Feburary 27-March 2 (2012)

6. J.-Y. Li, K. S. Chou, **C.-T. Huang**, J. C. Sturm, and L. P. Rokhinson, "High quality two-dimensional electron gases (2DEGs) in modulation-doped and enhancement-mode Si/SiGe heterostructures," *2011 PCCM Symposium: Quantum Control of Solid State Systems*, Princeton, NJ, November 3-5 (2011)

7. J.-Y. Li, **C.-T. Huang**, J. C. Sturm, and L. P. Rokhinson, "High quality two-dimensional electron system (2DES) in n-Type Si/SiGe modulation-doped heterostructures grown by RTCVD," *2011 International Workshop on Silicon Quantum Electronics*, Denver, CO, August 14-15 (2011)

8. K. Chou, J.-Y. Li, **C.-T. Huang**, J. C. Sturm, and C. W. Liu, "Stable high quality accumulation-mode Si 2DEG with a shallow top SiGe barrier of 25 nm," *2011 International Workshop on Silicon Quantum Electronics*, Denver, CO, August 14-15 (2011)

Appendix B

Fabrication of Undoped Silicon 2DEGs

B.1 Growth of Undoped Silicon 2DEGs

B.1.1 Baking Before Growth on Si and SiGe Substrates

To reduce possible water vapors or oil vapors back-streamed from the main pump, high temperature baking is necessary before growing any epi-layers. We mentioned in Sec. 2.1.2 that the temperature control system of RTCVD can only precisely control temperatures up to 750 °C. Temperatures higher than that can only be controlled by a fixed lamp power, whose corresponding temperature can be calculated based on the extrapolations shown in Fig. 2.3. After the replacement of the SCR unit, the standard baking power is 23%. A typical baking run consists of (1) 23% baking at 250 torr for 20 minutes with 4 slpm H_2 flow and (2) 23% baking at 6 torr for 1 minute with 3 slpm H_2 flow. We flow 0.5 slpm H_2 after a baking cycle is done for 7 minutes to allow the reactor to cool down. After cooling down, we can start another baking cycle if more baking cycles are necessary.

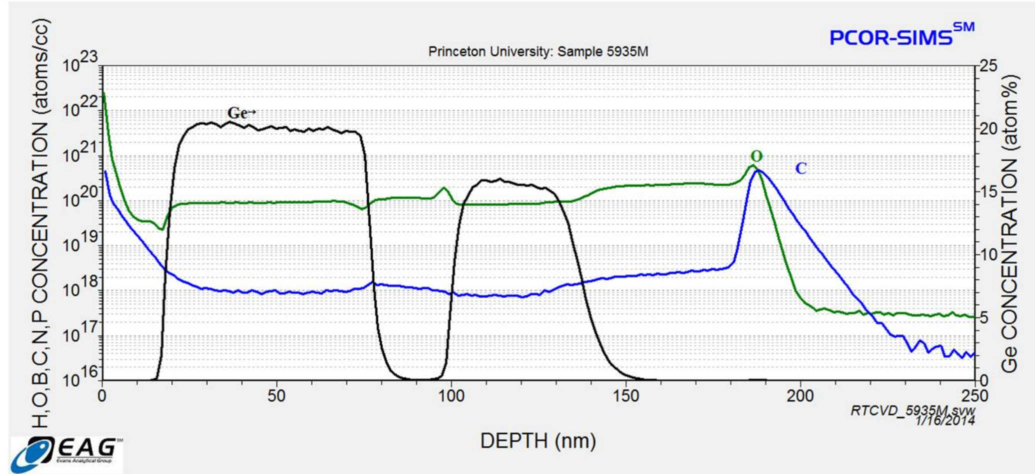


Figure B.1: A typical SIMS measured on dirty epi-layers grown on a silicon substrate.

For a newly-installed, brand new quartz reactor tube, 100× or more baking cycles are recommended. If we grow layers in a dirty reactor, the epi-layers grown on silicon substrates would be still visually clean, but contamination levels in the films would be extremely high (for example, 10^{20}cm^{-3} and 10^{18}cm^{-3} for oxygen and carbon, respectively in Fig. B.1). However, if we try to grow layers on SiGe substrates with high contamination levels in the reactor, no epi-layers would be grown on it and the resultant sample surface must become very hazy. Therefore, it is important to grow a test run to make sure all layers grown on SiGe substrates are clean before growing real samples.

B.1.2 Wet Cleaning for Growth Substrates

Before growth, a 100-mm silicon carrier wafer, silicon temperature control pieces and SiGe buffer pieces are all cleaned by the standard pirahna solution (H_2SO_4:H_2O_2= 1:2) for 20 minutes followed by a 2-minute diluted HF dip (DI water: 49% HF=100:1). Blow the silicon temperature control piece and the SiGe buffer pieces dry carefully, and load them onto the 100-mm silicon carrier wafer. Then we can load the 100-mm

carrier wafer onto the 100-mm quartz wafer stand in the load-locked chamber for growth.

B.1.3 Baking and Carrier Wafer Coating

Even if the reactor is used frequently, we always start with a single baking cycle as we described above without any wafers in it. After a baking, we may also choose to bake the carrier wafer alone (20% baking at 6 torr with 3 slpm H_2 for 10 minutes) and coat a thin silicon layer on it (13% lamp power at 6 torr with 50 sccm SiH_4 and 3 slpm H_2 for 10 minutes) without loading any small pieces of SiGe buffers. This way you can also bake out any remnant water vapors on the carrier wafer to avoid contamination on real samples. In addition, if the carrier wafer is new, this baking and coating procedure must be done before any growth. Here we also note that we do not bake or clean the carrier wafer between growth runs in the same growth day. We unload small Si temperature control piece and SiGe pieces and load a new set of samples onto the carrier for the next growth run in the load-locked chamber without taking it out.

B.1.4 100-mm Carrier Wafer for SiGe Buffer Pieces

The SiGe buffers used in our experiments are 200-mm wafers provided by AmberWave Systems Inc.. Since our reactor is designed for 100-mm wafers, we have to dice them into 1.05-cm^2 pieces by the dicing saw in the cleanroom (ADT proVectus 7100) so that we can load them on a 100-mm carrier wafer into the reactor. The design of a 100-mm carrier wafer is shown in Fig. B.2. Because SiGe buffer pieces are thicker (700 μm) than a regular 100-mm silicon wafer (525 μm), whose thickness is standard thickness for temperature calibrations based on the transmission of infrared lasers in our RTCVD (Sec. 2.1.2), we dice a regular 100-mm silicon wafer into small pieces with the same size as SiGe buffer pieces and load it in the center of the carrier wafer

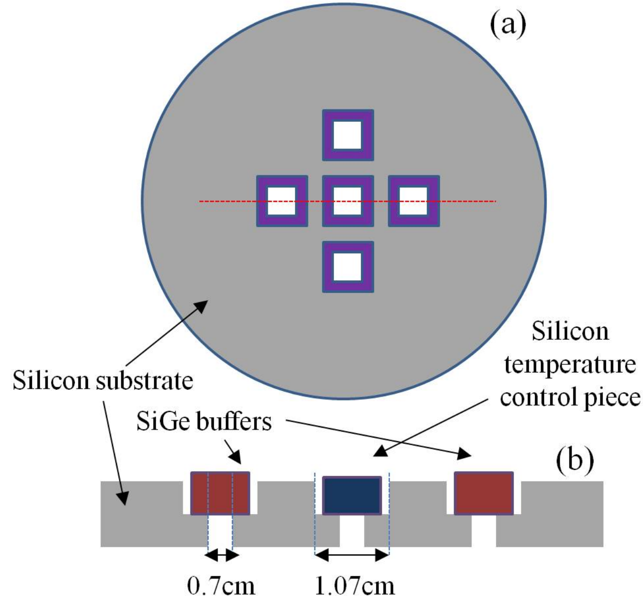


Figure B.2: (a) The top view and (b) the cross section along the red line of a standard 100-mm carrier wafer.

for the temperature control. Here we note that a thick and lightly-doped wafer (1 mm thick FZ wafer) is preferred to make a carrier wafer. It can provide deeper recesses, which can hold small pieces tightly to avoid samples from falling during the loading process. The light doping of the carrier wafer prevents any contamination caused by the autodoping during the high temperature baking. See more details in Ph.D thesis of Kun Yao [101].

B.1.5 Standard Layer Structure of an Undoped 2DEG and Its Growth Recipe

A typical layer structure of an undoped strained silicon 2DEG consists of a 150-nm $Si_{0.72}Ge_{0.28}$ buffer, a 10-nm strained silicon channel, a 60-nm $Si_{0.72}Ge_{0.28}$ cap layer and a 3-4 nm strained silicon cap. The standard growth recipe for this structure is as follows: (1) 20% baking for 5 minutes (2) Grow the SiGe buffer layer with 62 sccm GeH_4 and 50 sccm SiH_4 at 575 °C for 25 minutes (3) Grow the strained silicon channel

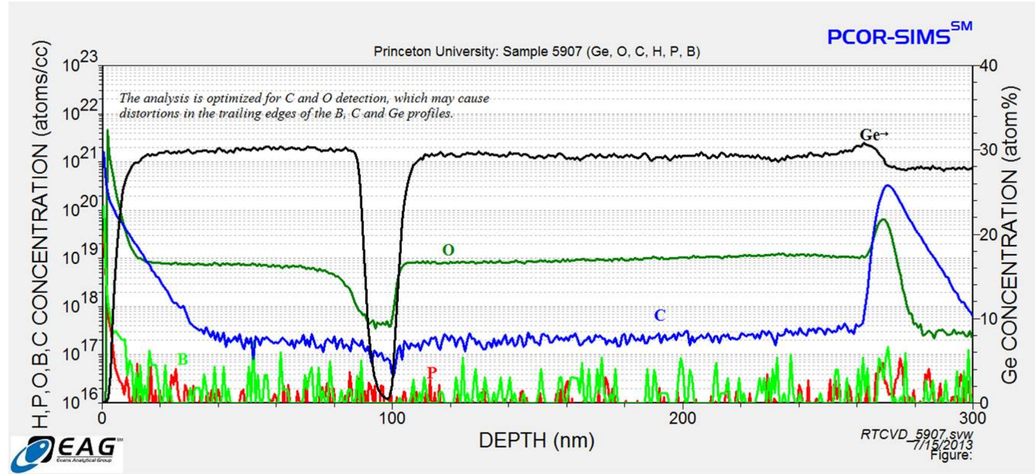


Figure B.3: A typical SIMS of an undoped 2DEG with group record high mobility.

with 200 sccm SiH_4 at 625 °C for 4 minutes (4) Grow the SiGe cap layer with 62 sccm GeH_4 and 50 sccm SiH_4 at 575 °C for 10 minutes (5) Grow the strained silicon cap with 200 sccm SiH_4 at 625 °C for 1.5 minutes. The growth pressure for all steps is 6 torr, with a constant 3 slpm H_2 flow. The typical growth rates for $Si_{0.72}Ge_{0.28}$ and silicon under the growth conditions mentioned above are 6 nm/minute and 2.5 nm/minute, respectively.

B.1.6 A Typical SIMS for a High-Mobility Undoped 2DEG

A typical SIMS for an undoped 2DEG with group record mobility (400,000 cm^2/Vs) is shown in Fig. B.3. The oxygen levels in SiGe and strained silicon channel are 1×10^{19} cm^{-3} and 4×10^{17} cm^{-3}, respectively, while the carbon levels in SiGe and strained silicon channel are 2×10^{17} cm^{-3} and 1×10^{17} cm^{-3}, respectively. The background phosphorus and boron concentrations are below the detection limit for all layers. The detection limit for P and B in a regular SIMS analysis is 4×10^{15} cm^{-3} and 1×10^{16} cm^{-3}, respectively.

B.2 Processes for Enhancement-Mode Undoped 2DEGs

B.2.1 Full Processes

The full process to fabricate a typical undoped 2DEG after growth consists of four photolithography steps (Fig. B.4). Four devices can be made on a single 1 cm×1 cm sample. The details of the full process are described as follows: (1) The first lithography followed by a dry etching by Samco RIE800iPB defines a set of alignment marks for following processes. The etching recipe is recipe 4 with 25 etching loop counts to create about 200-nm deep marks (Fig. B.4a). (2) After stripping photoresist, we deposit a 200-nm silicon dioxide layer as an implant mask by PECVD 790. The deposition recipe is standard cleanroom public recipe ($0SiO_2$) for 10 minutes. (3) The second lithography step followed by a wet etching of oxide by BOE 10:1 defines the patterns for n^+ contact ion implantations (Fig. B.4b). (4) Attach all samples on a 100-mm silicon wafer and send it to Leonard Kroko Inc. for phosphorus ion implantation. The implant recipe we use is a 3-step implantation consisting of 5×10^{15} cm^{-2} at 30 keV, 5×10^{15} cm^{-2} at 60 keV and 5×10^{15} cm^{-2} at 100 keV. The tilt angle is standard 7 degree without any substrate heating.

(5) After implantation, 1-hour annealing at 600 °C in N_2 by Thermco Brute IV, tube 3 is conducted to activate implanted phosphorus. (6) A 90-nm aluminum oxide is then deposited by atomic layer deposition (Cambridge NanoTech, Savannah 100). The detailed recipe for aluminum oxide deposition by ALD along with chamber cleaning procedure will be addressed later. (7) The third lithography followed by a wet etching of the aluminum oxide by BOE 10:1 exposes the contact regions (Fig. B.4c). (8) The fourth lithography defines the Hall-bar-shaped metal gates and the contact regions. After lithography, a 3-nm Cr and a 200-nm Au are evaporated onto samples for both metal gates and contacts (Fig. B.4d). The evaporation is done

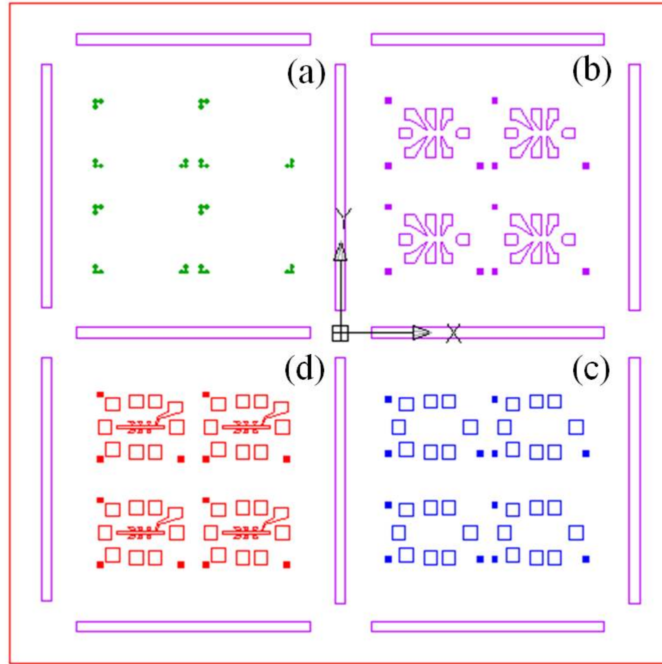


Figure B.4: A mask image that describes the four photolithography steps for enhancement-mode undoped 2DEG fabrication.

by Edwards thermal evaporator in C428. Here we note that the E-beam evaporator for Au deposition has to be avoided because the radiation from the electron beam may damage the aluminum oxide underneath, causing an issue to measure such 2DEGs. (9) Four devices are diced by the dicing saw for the following low-temperature Hall measurements.

B.2.2 ALD Chamber Cleaning and Deposition Recipes

The atomic layer deposition (Cambridge NanoTech, Savannah 100) is used to deposit the aluminum oxide layer in our undoped 2DEGs. After many depositions, flakes may appear and attach on both the lid and the chamber. If you notice some flakes on your samples after the deposition, it is the time to clean the chamber. To clean ALD, you have to contact Joe Palmer first to put the equipment offline for about 3 days. The cleaning processes are as follows: (1) Turn off all the heaters and wait

until all heaters are at room temperature. (2) Use Scotch-Brite to scrub the chamber and the lid until all the flakes are gone. (3) Use Textwipes with methanol to wipe the chamber several times. (4) You can also replace the O-ring, refill DI water bottle and replace empty TMA bottle at this time, but Joe Palmer should be there. (5) Blow the chamber dry with a nitrogen gun. (6) Increase the temperatures for all heaters. 300 °C for center heater, 250 °C for edge heater, 80 °C for precursor heater and 150 °C for the rest of heaters. Flow 100 sccm N_2 carrier gas and let it bake for a half day. (7) Coat the chamber with a regular deposition recipe without loading any samples in for over 1000 cycles (8) Run a test deposition on a silicon wafer. Measure the thickness and refractive index by the ellipsometer (Gaertner L3W16). The normal deposition rate is 0.9 $\AA$ per cycle while the normal refractive index is 1.64.

The recipe of aluminum oxide deposition by this ALD has four parameters: Precursor (0 is water and 1 is TMA), pulse time, exposure time and pump time (the unit is second for all time parameters). Three steps of the recipe are (1) [0, 0.01, 0, 5] and [0, 0.01, 0, 5] for 10 cycles. In this step we repeat water exposure to ensure the sample surface is covered by hydroxyl bonds (-OH) (2) [0, 0.1, 1, 7] and [1, 0.1, 1, 7] for 10 cyles. Here we lengthen the pulse time, exposure time and pump time to make sure the precursors have enough time to complete the reaction for the first few monolayers. (3) [0, 0.01, 0, 5] and [1, 0,01, 0, 5] for 890 cycles. The number of cycles can be adjusted to meet any thickness requirement. Total 900 cycles can give us an 80-nm aluminum oxide with a purple to dark blue color.

Appendix C

Non-Standard Wafer Growth

In addition to the absorption coefficient, the transmissions of two infrared lasers we use to calibrate our growth temperature strongly depend on the wafer thickness. This is the reason why we need to use a 100-mm carrier wafer to carry small pieces of SiGe buffers with a standard silicon piece in the middle. However, the main drawback of using a carrier wafer is that the available 2DEG sample areas are very limited for each growth. If we want to grow epi-layers on a full SiGe buffer wafer with any non-standard thickness, the issue of temperature calibration and control has to be overcome.

C.1 Growth on a Thin SiGe Buffer (400 μm)

One of our outside collaborator has 75-mm SiGe buffer with a 400-μm thickness. To take both loading process and temperature calibration into account, we have several options available to grow epi-layers on theses non-standard substrates.

Figure C.1: The picture of a 125-mm carrier held by a 125-mm quartz wafer stand with a 75-mm wafer on it.

C.1.1 Option 1: 125-mm Carrier Wafer

If we stick to the small silicon temperature control piece for temperature control, we have to make a carrier wafer that can hold the 75-mm wafer along with 1 cm×1 cm silicon piece. The 100-mm wafer is way too small for this option, so we turn to 125-mm wafer (1 mm thick). The design is shown in Fig. C.1. This 125-mm carrier wafer consists of two recesses. The first recess with a hole in the middle is similar to that in a regular 100-mm carrier wafer and designed to hold a small silicon piece for temperature control. The large 10-side polygons are etched (about 500 μm deep) by Samco 800 to hold a 75-mm SiGe buffer.

Here came some difficulties if we choose option 1. First, etching a 125-mm wafer by Samco 800 needs to vent the etcher and modify the setting inside the chamber. We have to contact Pat Watson for this modification, and the etcher has to be set offline for 3 days. Second, a new design for a quartz wafer stand for 125-mm wafer is required because our regular wafer stand is designed for 100-mm wafers (See Fig. C.1). (Technical Glass Products (TGP) helps us to fabricate quartz wafer stands and quartz reactor tubes.) The third issue is the most fatal one: loading difficulty. Although

Figure C.2: The picture of 75-mm SiGe buffer carried by a 125-mm carrier wafer after a test growth. The color rings labeled by yellow lines represent the thickness nonuniformity.

the smallest diameter of the loading path in our RTCVD is 150-mm, it is still very difficult to safely load a 125-mm wafer into the reactor because there are too many blind spots where the carrier can hit the inner walls of the chambers. Fourth, since the temperature control piece is at the front position, the landing position in the reactor for the wafer stand is different from the standard one. A new calibration for the wafer landing position has to be done to make sure lasers going through the silicon piece.

A test growth was done on a 75-mm silicon substrate carried by a 125-mm carrier wafer. The picture of the 75-mm silicon substrate after growth showed several clear color rings (Fig. C.2). The color rings represent the non-uniformity of the thickness of the epi-layers. We sent out four pieces of samples for SIMS analysis, and space between each piece is 1 inch (Fig. C.3). The thickness information extracted from SIMS are listed in Fig. C.4. Referring to the temperature control piece (where is the center of the temperature distribution in the reactor), the thickness of each layer gets thinner when the location of the piece gets further away from the center because

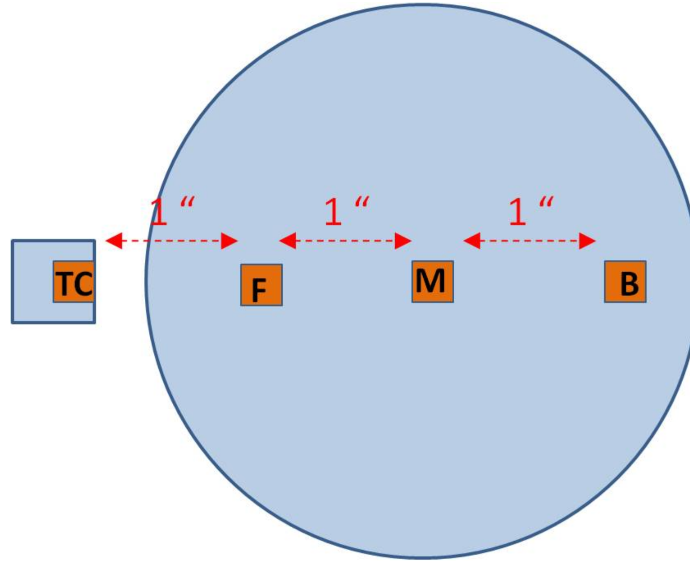


Figure C.3: The schematic of a 75-mm SiGe buffer and a silicon temperature control piece held by a 125-mm carrier wafer. The pieces sent out for SIMSs are highlighted.

	625°C (Si)	575°C (sSiGe) Ge: 19-20%	700°C (Si)	600°C (sSiGe) Ge: 14-15%	750°C (Si)
TC (nm)	**27** (100%)	**55** (100%)	**41** (100%)	**39** (100%)	**78** (100%)
F (nm)	**24** (89%)	**70** (127%)	**30** (73%)	**44** (113%)	**58** (74%)
M(nm)	**19** (70%)	**58** (105%)	**24** (59%)	**35** (90%)	**50** (64%)
B (nm)	**8** (30%)	**23** (42%)	**11** (27%)	**15** (38%)	**28** (36%)
Expected Thickness (nm)	30	40	35	40	70

Figure C.4: The thickness comparison between pieces cut from different locations on the 75-mm SiGe buffer held by a 125-mm carrier wafer.

the growth temperature there is lower. This terrible thickness uniformity makes this option impossible to grow useful epi-layers on 75-mm SiGe buffers for experiments.

C.1.2 Option 2: 100-mm Carrier Wafer

We can also use 100-mm wafer as a carrier to hold 75-mm SiGe buffers, but we have to overcome the temperature calibration issue. The design of this 100-mm carrier

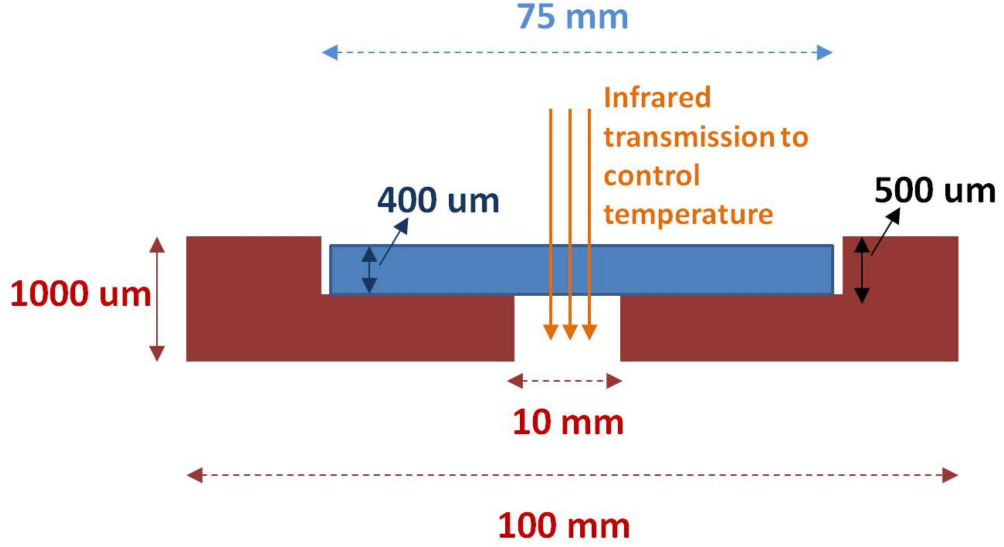


Figure C.5: The schematic of a 75-mm wafer on a 100-mm carrier wafer. The 75-mm is used to calibrate growth temperatures.

wafer is similar to the previous 125-mm carrier wafer. A 10-sides polygon recess is etched in the middle of a 100-mm wafer to hold a 75-mm SiGe buffer as shown in Fig. C.5.

Now we have to deal with the temperature calibration. Based on the following equation, we can calculate the normalized transmission of two lasers for different wafer thicknesses [17]:

$$(NT_{ta}) = (NT_{tb})^{\frac{tb}{ta}} \tag{C.1}$$

where ta and tb are the thickness of the wafer a and wafer b for temperature calibration. NT_{ta} and NT_{tb} are the normalized transmission for wafers with thickness ta and tb, respectively.

The calculated normalized transmissions for a 400-μm, 525-μm (standard) and 680-μm thick silicon wafer for several common growth temperatures are compared in Fig. C.6. For a 75-mm SiGe buffer, we still stick to the standard growth temperatures

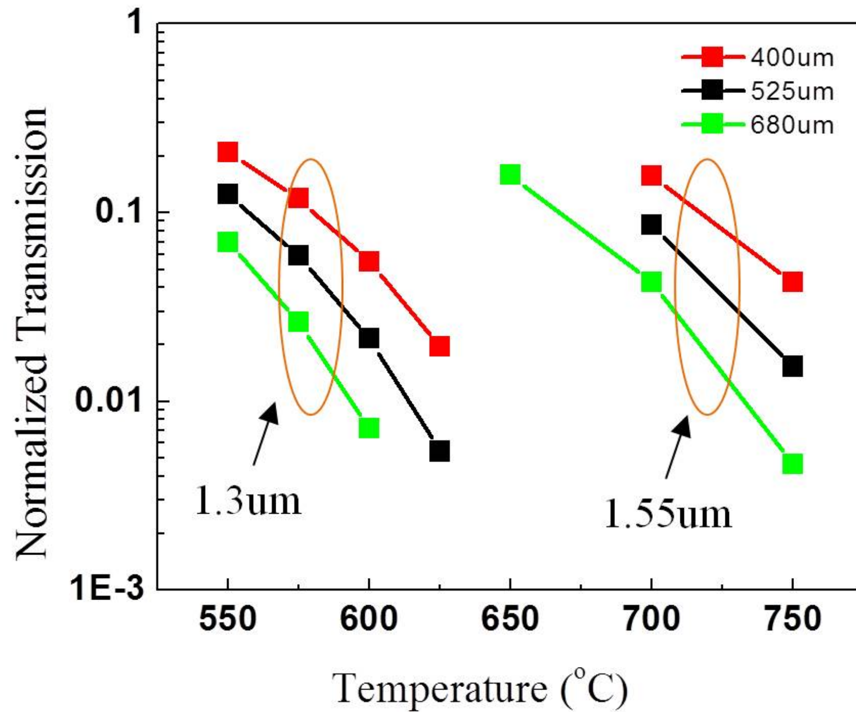


Figure C.6: The normalized transmission of two infrared lasers calculated based on Eq. C.1 for different wafer thicknesses.

for undoped silicon 2DEG growth (575 °C and 625 °C for $Si_{0.72}Ge_{0.28}$ and Si growth, respectively.)

First we worried that the 3-μm thick SiGe buffer has a smaller bandgap, a high intrinsic carrier density and many defects, all of which may additionally absorb infrared signals and affect the accuracy of the temperature calibration. To solve that, we etched about 4-5 μm away in the middle of the 75-mm buffer layer (1 cm$\times$1 cm). This non-planar wafer surface raises a concern about the photoresist uniformity for the following processes after growth, so a simple test was done by spinning a layer of photoresist (5214) on an etched 75-mm wafer and measuring the thickness of the photoresist by NanoSpec. We could see four streaks radiating from four corners of the etched square. The thickness of resist right at the corner (the thickest part) is 1.442 μm measured by Nanospec. Along the streaks, we measured the point roughly

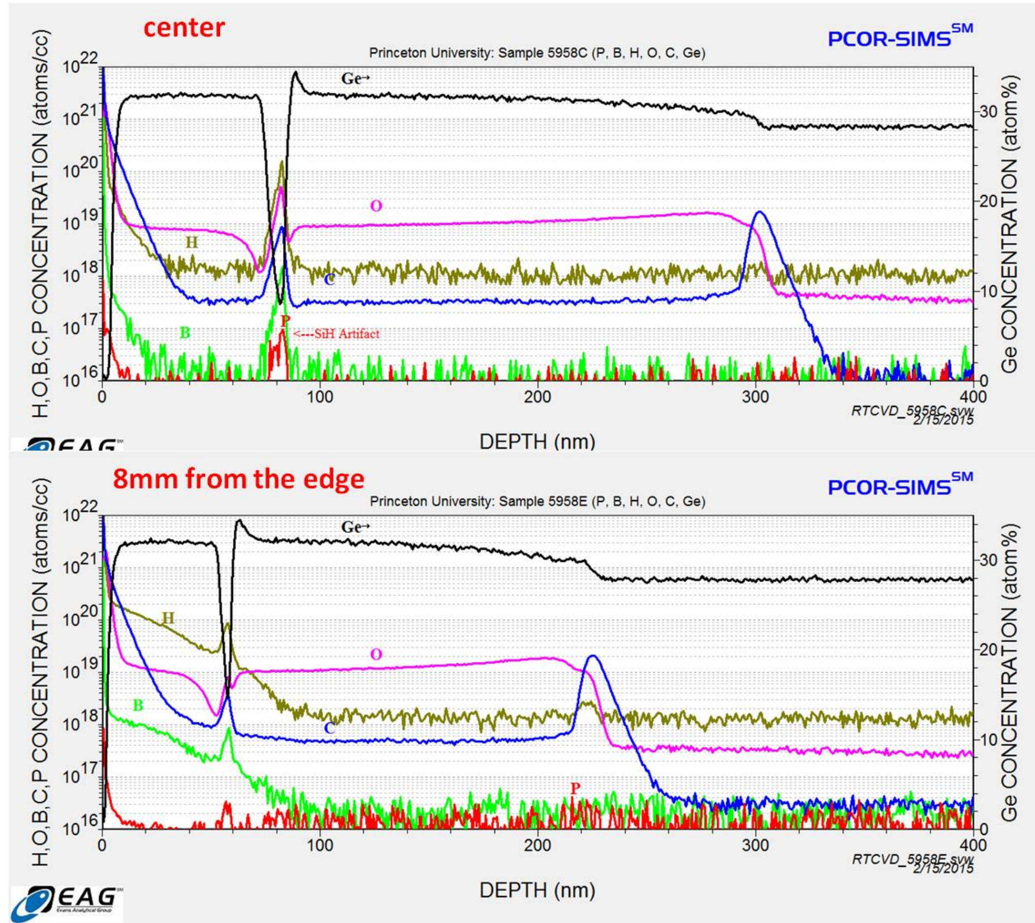


Figure C.7: The SIMS analyses for two separate pieces cut from a 75-mm SiGe buffer carried by a 100-mm carrier wafer. The peaks in the silicon channel could be artifacts.

15 mm away from the corner, the thickness is 1.418 μm. We also measured a point at uniform area, the thickness is 1.417 μm. Therefore, the thickest point (1.442 μm,) is about 1.8% thicker than uniform area, which does not affect too much the following photolithograpy and patterning. Here we note that for the ebeamresist, the color of the resist became uniform after 170 °C soft baking, so the uniformity of the ebeam-resist should be fine.

Even though the uniformity of the resist is OK, we still try to avoid the etching process because it consumes a considerable area which can not be used after growth. Also, we can avoid the patterns (the square in this case) on a substrate to be grown.

Layer	Expected Center Thickness	8mm from the Edge	Center	Growth Rate for Center (Growth Time)	Thickness Percentage (Edge/Center)
625°C Si	4nm	2.5nm	4nm	2.4nm/min (100 seconds)	62.5%
575°C $Si_{0.72}Ge_{0.28}$	70nm	52nm	71nm	7nm/min (10 minutes)	74%
625°C ^{28}Si	12nm	5nm	9nm	3nm/min (3 minutes)	56%
575°C $Si_{0.72}Ge_{0.28}$	210nm	166nm	217nm	7nm/min (30 minutes)	76%

Figure C.8: The thickness non-uniformity of epitaxial layers grown on a 75-mm SiGe buffer carried by a 100-mm carrier wafer.

The patterns on the substrate always cause contamination for the growth, so hazy areas along the patterns are always inevitable. A quick calculation done by Kun Yao [101] showed that the thin layer of SiGe buffer does not affect the normalized transmission too much compared to the silicon substrate with couple of hundreds microns. The only effect is the intensities of lasers at room temperature are slightly lower.

After a typical undoped 2DEG growth (with enriched silicon in the silicon channel) on a 75-mm SiGe buffer carried by a 100-mm carrier wafer without etching a hole, we sent out two pieces (one center piece and one piece 8 mm from the edge) for SIMS, and the results are shown in Fig. C.7. We can still see the thickness non-uniformity, but it is much better than the results of the option 1. The thickness information is extracted and compared in Fig. C.8. The center thickness is very close to the expected thickness. The edge thickness is thinner than the center, but it is still a reasonable undoped silicon 2DEG structure which can be used for the future measurements.

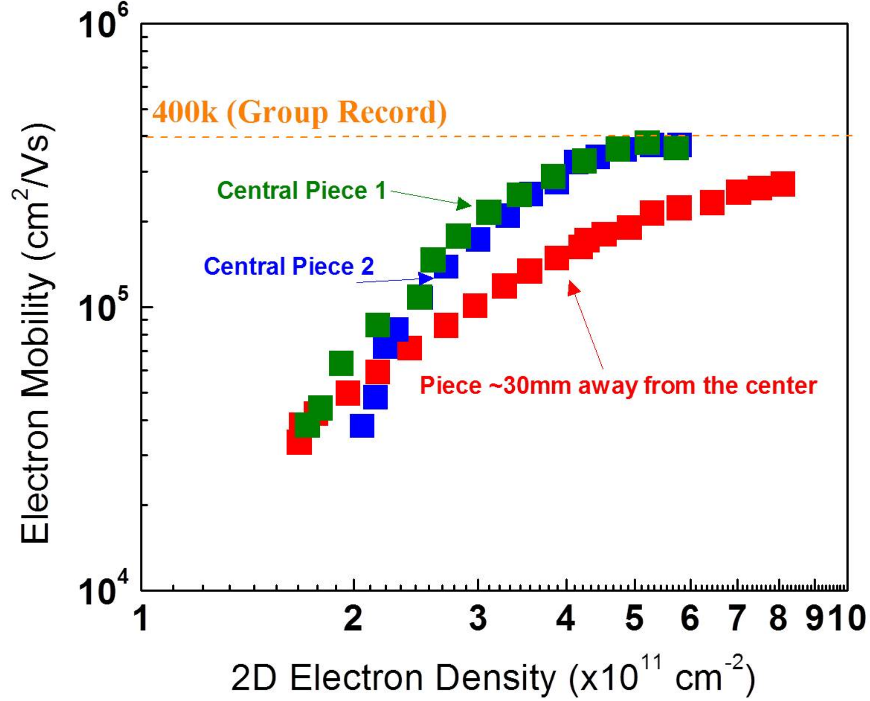


Figure C.9: The mobility data measured at 4.2 K from center pieces and pieces near the edge. The center piece shows a group record high mobility.

Enhancement-mode Hall bar devices were fabricated on both edge and center pieces to check the 2DEG quality. The Hall measurement data at 4.2 K is shown in Fig. C.9. The highest mobility for two center pieces is 400,000 cm^2/Vs, which is our group record. The highest mobility for the edge piece is 200,000 cm^2/Vs, lower than that of the center pieces, but it is still fairly high. The reason for reduction in mobility for the edge piece could be the thinner SiGe cap or buffer layers, or the lower baking temperature before the epitaxial growth. Here we note that the peaks of all elements in the silicon channel in the SIMS could be artifacts (Fig. C.7) because no interruption occurred during the growth, and high electron mobility was still observed in both samples.

One additional figure that shows the thickness uniformity for a 75-mm silicon substrate (400 μm thick) on a 100-mm silicon carrier wafer is shown here for reference

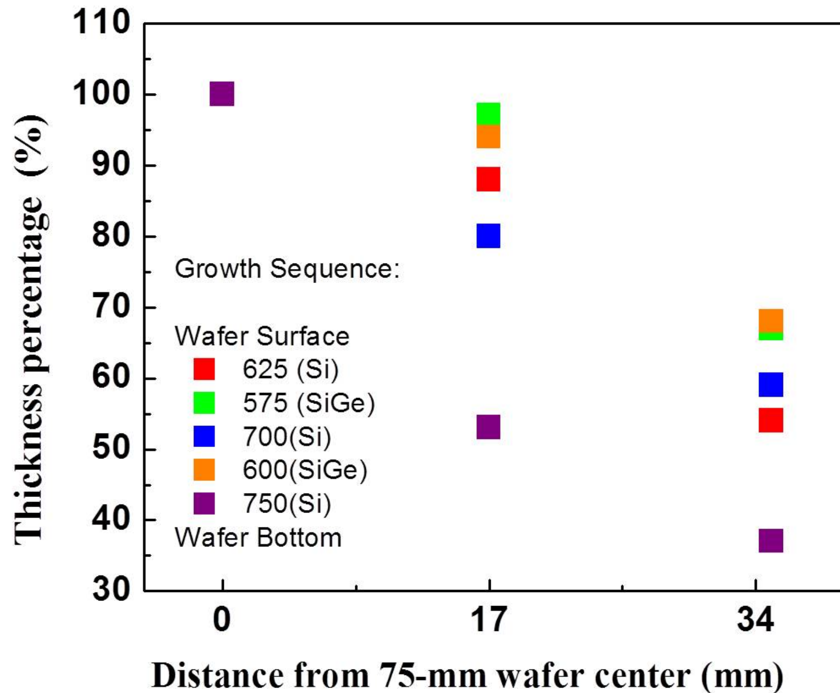


Figure C.10: The thickness percentages of epi-layers grown on a 75-mm silicon substrate carried by a 100-mm carrier wafer.

(Fig. C.10). For SiGe growth, the film thicknesses 17 mm away from the center are still above 90% of film thickness in the wafer center, while they fall to around 70% at the location 34 mm away from the center. In addition, the thickness uniformity of silicon films are worse than SiGe films over the whole 75-mm wafer. Higher silicon growth temperature leads to the worse thickness uniformity.

C.1.3 Option 3: 75-mm Quartz Wafer Stand

Another even simpler option is to fabricate a special quartz wafer stand for 75-mm wafer only. This way, the 100-mm carrier wafer is no longer needed, and the loading process would become easier and safer as well.

C.2 Growth on a Thick SiGe Buffer (680 μm)

C.2.1 Dicing an 150-mm SiGe Buffer into a 100-mm Wafer

One of our collaborators also required us to grow epi-layers on thick SiGe buffers (680 μm). Such thick SiGe buffers are 150-mm wafers, so before we load it into our reactor, we have to dice them down to 100 mm. Bert Harrop helped me to dice the 150-mm wafers by using ADT dicing saw into to a 20-side polygons, whose peak-to-peak distance is 100 mm, and flat-to-flat distance is 99 mm. The size tolerance of this diced wafer is very small because of following two reasons. First, since the diced wafer is held by a quartz wafer holder when we load it into the reactor, the diameter of this diced wafer can not be smaller than 95 mm. Second, we have to load this wafer into the etcher Samco 800 to etch the central SiGe buffer layer out (will talk about this later), so the wafer size has to fit in the stage inside the Samco 800 chamber. A quartz ring used to cover the top of the wafer to be etched by Samco 800 has a groove with 101-mm diameter. A quick test can be done by putting the diced wafer into the groove to see if the diced wafer can fit in it. We have to do a loading test into Samco 800 as well to see if it can sit in the slot inside the chamber and cover all the helium cooling holes. A successful etching test on a diced wafer is shown in Fig. C.11.

C.2.2 Growth Temperature Calibration for a Thick SiGe Buffer

We can choose to etch the center of this thick SiGe buffer layer down to 525 μm, which is our standard thickness for temperature calibration. However, the deep etching could leave the dirty sidewalls very close to our epitaxial areas, leading to hazy regions which reduce the usable sample surfaces. Thus, we decide to remain its thickness for temperature control. Based on the calculation shown in Fig. C.6, we can also calibrate the temperature by a 680-μm thick SiGe buffer. However, since the wafer is thicker

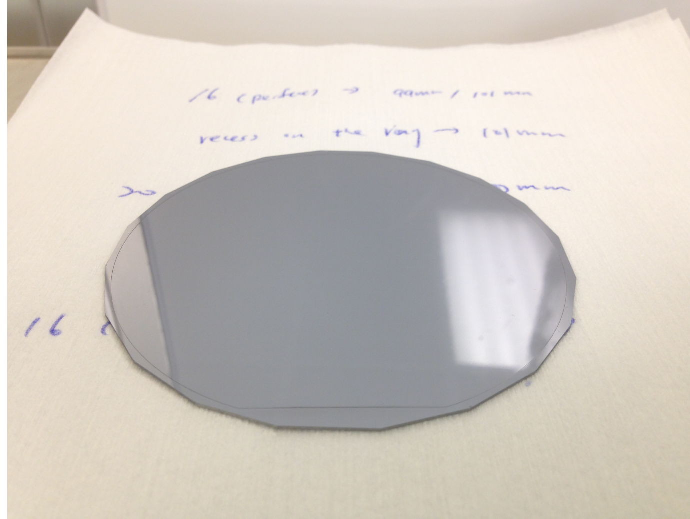


Figure C.11: The picture of a diced 100-mm SiGe buffer from a 150-mm SiGe wafer. The ring along the edge of the diced wafer is the etched pattern from the quartz ring of Samco 800 etcher, showing the quartz ring perfectly covered the edge of the diced wafer during the etching.

than the standard one, the signals of the infrared lasers measured by lock-in amplifiers are smaller. With the SiGe buffer on it, the signals are even smaller. In addition, for a thick wafer, the normalized transmission values for common growth temperatures are smaller too. Therefore, in order to get high enough signals to calibrate temperatures, we still prefer to etch away the SiGe buffer layer for about couple of microns. Here we note that there is always a gap between the normalized transmission of 1.3-μm and 1.55-μm lasers where the temperature can not be precisely controlled (Fig. C.6). The gaps for 525-μm and 400-μm thick wafers are both higher than our regular silicon growth temperature, 625 °C, but that for a 680-μm thick wafer is between 600 °C and 650 °C. Therefore, we lower the silicon growth temperature for thick SiGe buffer down to 600 °C for a better temperature control. (The growth temperature for $Si_{0.72}Ge_{0.28}$ is still kept at 575 °C)

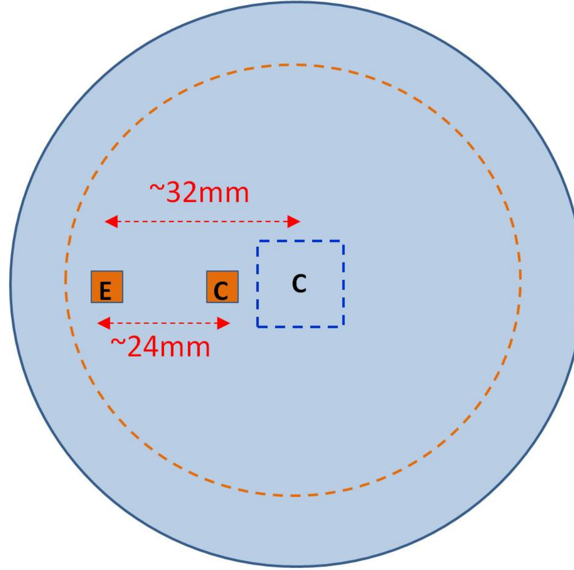


Figure C.12: The pieces cut for SIMS analyses from a diced 100-mm SiGe buffer after a standard undoped 2DEG growth.

C.2.3 Growth Uniformity and Mobility Results

After a regular undoped 2DEG growth, two pieces cut from the diced thick SiGe buffer were sent out for the SIMS analyses (Fig. C.12). The SIMS show again non-uniform thicknesses (Fig. C.13), but the layer structure of the edge piece still gives us a reasonable 2DEG structure. The carbon level in the edge piece is higher than the one closer to the center, which is common in our growth, but the cause is still unknown.

The thickness information is again extracted and compared in Fig. C.14. The SiGe cap thickness percentage of edge piece to the piece closer to the center is less than 50%, which is much worse than that in the undoped 2DEG grown on a 75-mm SiGe buffer (75%) in Fig. C.8. As for the electron mobility, the highest mobility for both edge or center piece are still as high as 200,000 cm^2/Vs (Fig. C.15). Even if this value is only half of our group record, it is still high enough for the following physics experiments.

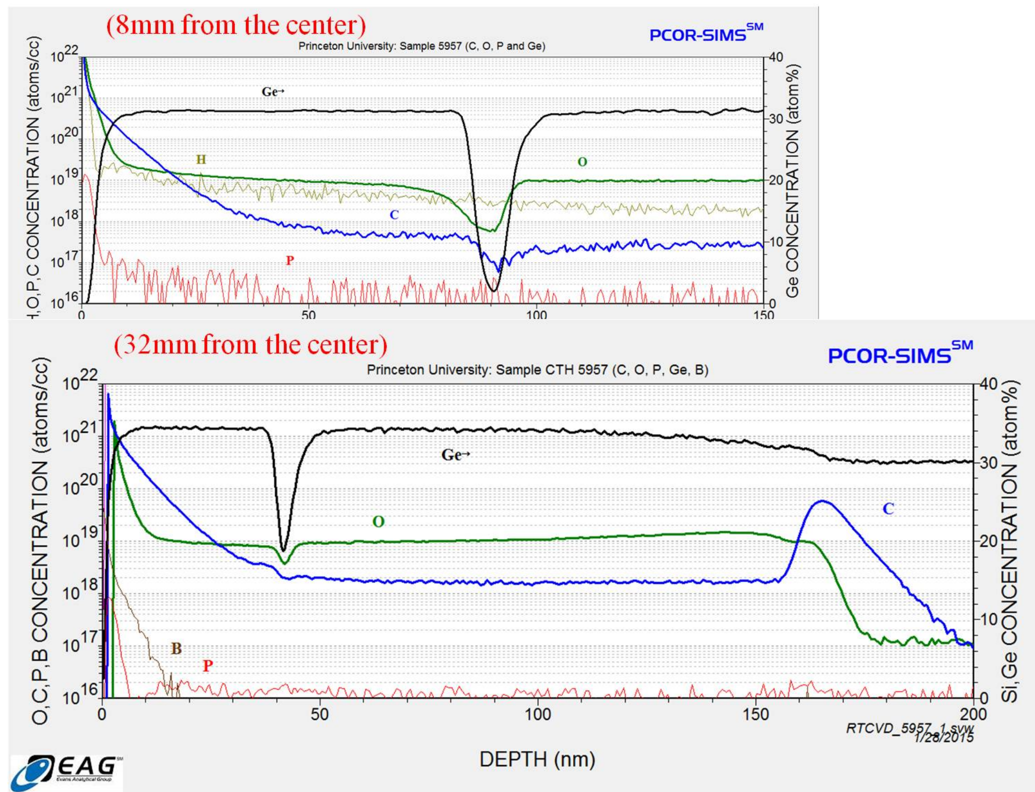


Figure C.13: The SIMS analyses for the pieces with different distances from the wafer center of a diced 100-mm SiGe buffer.

Layer	Expected Center Thickness	32mm from the Center	8mm from the Center	Thickness Percentage (Refer to the Piece 8mm from the Center)
600°C Si	4nm	<2nm	3nm	~55.5%
575°C $Si_{0.7}Ge_{0.3}$	70nm	35nm	83nm	42%
600°C ^{28}Si	10nm	5nm	9nm	55%
575°C $Si_{0.7}Ge_{0.3}$	190nm	120nm	NA	NA

Figure C.14: The thickness non-uniformity of epi-layers grown on a diced 100-mm SiGe buffer.

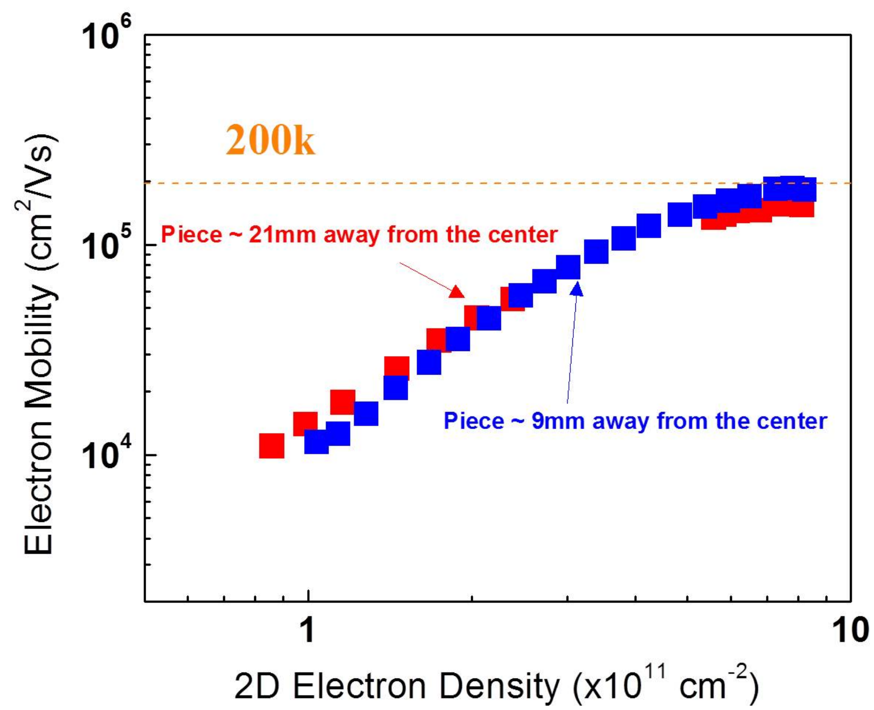


Figure C.15: The mobility measured from pieces with different distances from the wafer center of a diced 100-mm SiGe buffer. The highest mobility at 4.2 K is 200,000 cm^2/Vs.

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