Properties and Applications of Crystalline $Si_{1-x-y}Ge_xC_y$ alloys

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A DISSERTATION

PRESENTED TO THE FACULTY

OF PRINCETON UNIVERSITY

IN CANDIDACY FOR THE DEGREE

OF DOCTOR OF PHILOSOPHY

RECOMMENDATED FOR ACCEPTANCE

BY THE DEPARTMENT OF

ELECTRICAL ENGINEERING

NOVEMBER 1998

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Abstract

We have used both electrical and optical characterization methods to study the effect of carbon on the valence band offset of compressively strained $Si_{1-x-y}Ge_xC_y$ / Si (100) heterojunctions grown by Rapid Thermal Chemical Vapor Deposition (RTCVD) with substitutional C levels from 0% to 2.5%. Our work indicates that the change in the bandgap of $Si_{1-x-y}Ge_xC_y$ as carbon is added is entirely accommodated in the valence band. We also propose a simple model to predict the change of band structure with the incorporation of C.

We have also investigated the transport properties of holes in $Si_{1-x-y}Ge_xC_y$ channels by fabricating a compressively strained $Si_{1-x-y}Ge_xC_y$/Si (100) modulation-doped structures. We found that hole mobility decreased as more C was added. The decrease in hole mobility was determined to be caused by C-related defects, not by change in the effective mass of holes as C was added.

Finally, we demonstrated an application of crystalline $Si_{1-x-y}Ge_xC_y$ by growing polycrystalline $Si_{1-x-y}Ge_xC_y$ and used it as part of a polycrystalline gate structure for PMOS devices. The results showed that the use of carbon in polycrystalline $Si_{1-x-y}Ge_xC_y$ suppressed boron penetration across the gate oxide. No effects of gate depletion with the use of poly-$Si_{1-x-y}Ge_xC_y$ were observed. Our work suggests that the addition of carbon reduced the chemical potential of boron in $Si_{1-x-y}Ge_xC_y$, which deterred boron from diffusing across the underlying gate oxide.

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Chapter 1

Introduction

1.1 Motivation

The last decade has witnessed a tremendous progress in the field of strained $Si_{1-x}Ge_x$/Si (100) heterostructures, from fundamental studies on growth and band structure engineering to a rapidly maturing technology. Various applications have been developed, such as $Si_{1-x}Ge_x$–based heterojunction bipolar transistors as well as infrared detectors for optical communication. The accelerated development of the strained $Si_{1-x}Ge_x$/Si (100) arises from its fortuitous material properties. For example, it is relatively easy to grow $Si_{1-x}Ge_x$ films since Si and Ge are completely miscible over the entire alloy range. Doping in the $Si_{1-x}Ge_x$ film is also no more difficult than that in Si. Due to a 4% larger atomic size of Ge than Si, a $Si_{1-x}Ge_x$ film is compressively strained when it is grown pseudomorphically (without misfit dislocations) on a Si substrate. The incorporation of Ge reduces the bandgap of $Si_{1-x}Ge_x$, with most of the bandgap reduction exhibited as the valence band offset of the strained $Si_{1-x}Ge_x$/Si system.

The strain due to the incorporated Ge in the pseudomorphic $Si_{1-x}Ge_x$ limits the thickness of the film that can be grown without the generation of misfit dislocations, which are detrimental to device performance. Consequently, this poses a severe design constraint and limits its potential device applications. Over the past five years, researchers have been trying to add carbon into pseudomorphic $Si_{1-x}Ge_x$ on Si to relieve the strain. Carbon is a good candidate since it has a much smaller atomic size and it is

iso-electronic to both Si and Ge. Indeed, thicker films have been grown pseudomorphically with the addition of carbon.

Given the ability of C compensating the strain caused by Ge, the next question is to see how C incorporation changes the properties of the resulting $Si_{1-x-y}Ge_xC_y$ materials.

In this thesis, we first discuss efforts to grow high-quality $Si_{1-x-y}Ge_xC_y$ films with a few percentage of substitutional C. We then address the change in fundamental electronic properties due to the inclusion of C, primarily in the band alignment of the still compressively strained $Si_{1-x-y}Ge_xC_y$/Si (100). After obtaining the experimental data of the effect of C on the band alignment of $Si_{1-x-y}Ge_xC_y$/Si, we propose a simple model to predict how C incorporation changes the band alignment of the Si-based epitaxial materials with the underlying Si substrate.

To use $Si_{1-x-y}Ge_xC_y$ for device applications, one of the key parameters is the carrier mobility in the $Si_{1-x-y}Ge_xC_y$ materials. As a result, we study how C incorporation change the hole mobility by fabricating compressively strained $Si_{1-x-y}Ge_xC_y$/Si modulation-doped structures. After observing that C reduces hole mobility, we study whether the change in hole mobility is due to change in hole effective mass or change in scattering mechanism due to C incorporation.

Finally, we go beyond the band structure engineering with C and demonstrate a potential application of using $Si_{1-x-y}Ge_xC_y$ alloys in suppressing undesirable enhanced dopant diffusion, a fundamental problem in current Si and $Si_{1-x}Ge_x$/Si VLSI processing.

1.2 Thesis Outline

Chapter 2 serves as an introduction to the strained $Si_{1-x-y}Ge_xC_y$/Si (100). The growth of $Si_{1-x-y}Ge_xC_y$ and strain compensation by the addition of C is reviewed. The effect of C on the electronic and optical properties of $Si_{1-x-y}Ge_xC_y$ is also presented.

Chapter 3 presents our study on the effect of C on the band alignment of the strained $Si_{1-x-y}Ge_xC_y$ /Si (100). Both electrical and optical characterization methods have been used and their results and reliability are evaluated. A simple model is

With the effect of C on the band alignment understood, we fabricate a strained $Si_{1-x-y}Ge_xC_y$ /Si modulation doped structure in chapter 4 to study the carrier transport properties in the $Si_{1-x-y}Ge_xC_y$ layer. We also study the effect of C on the hole effective mass.

Chapter 5 demonstrates one application of $Si_{1-x-y}Ge_xC_{y.}$ By growing a polycrystalline $Si_{1-x-y}Ge_xC_{y,}$ we are able to suppress boron penetration through the gate oxide in p-channel metal-oxide-semiconductor devices.

Chapter 6 summarizes the contribution of this thesis and suggests directions along which future work may be pursued.

Appendix A lists typical growth sequences of samples used in thesis.

Appendix B lists publications and presentations resulting from this thesis.

Chapter 2

Strained $Si_{1-x-y}Ge_xC_y$ alloys

2.1 Introduction

The concept of strained layer epitaxy was demonstrated theoretically 50 years ago[1]. If a lattice mismatched thin film is grown on a thick substrate, the layer may be pseudomorphic provided that the mismatch is small. In the 1980's, the concept led to the fabrication of a strained $Si_{1-x}Ge_x$ layer on silicon (100) substrate and has since spurred many fundamental studies and device applications based on the advantage of a heterostructure. Si and Ge are isoelectronic; have the same crystal structure, and are completely miscible in the entire range of composition, which makes the growth of $Si_{1-x}Ge_x$ relatively easier compared to other mixtures of elements. Strained $Si_{1-x}Ge_x$ has a smaller band gap than that of Si, and most of the bandgap difference appears at the valence band offset of the strained $Si_{1-x}Ge_x$/Si (100) heterojunction. The advantage of the strained $Si_{1-x}Ge_x$ /Si (100) is the tunable bandgap of $Si_{1-x}Ge_x$ by Ge incorporation. As a result, many device applications have been realized by varying Ge incorporation to achieve bandgap engineering.

Unfortunately, the very benefit of bandgap engineering is limited by the strain involved in the $Si_{1-x}Ge_x$ layer. The lattice parameter of Si is 0.5431 nm and the lattice parameter for Ge is 0.5675nm, which makes the lattice parameter of $Si_{1-x}Ge_x$ alloys between 0.5431 nm and 0.5675 nm. In order to deposit a $Si_{1-x}Ge_x$ film onto a Si substrate pseudomorphically, the film has to be strained. The strain in the film limits the film to a

critical thickness beyond which thermodynamics favors plastic flow, resulting in the generation and propagation of misfit dislocations. Even though modern epitaxial techniques can extend the critical thickness by growing metastable thin films, high temperatures involved in the device processing still cause relaxation of $Si_{1-x}Ge_x$ films above the thermodynamic critical thickness. Thus, it is necessary to find a way to extend the critical thickness while continuing the bandgap engineering.

Since carbon is isoelectronic to both Si and Ge and has a smaller lattice constant (0.3546 nm for diamond structure), researchers have tried to grow $Si_{1-x-y}Ge_xC_y$ alloys since 1990's to overcome the limit of critical thickness. In this chapter, we discuss the growth of $Si_{1-x-y}Ge_xC_y$, strain compensation by the carbon incorporation and the effect of carbon on the electronic structures of $Si_{1-x-y}Ge_xC_y$ alloys.

2.2 Growth of Pseudomorphic $Si_{1-x-y}Ge_xC_y$ alloys

2.2.1 Increased C solubility by epitaxial growth techniques

Even though Si and Ge are completely miscible, silicon carbide (SiC) is the only stable compound according to the Si-C binary phase diagram. In fact, the solubility of substitutional carbon in Si is only $3x10^{17}/cm^3$ at the melting temperature[2], and it is believed to be even smaller in Ge[3]. It seems therefore not possible to grow thermodynamically stable $Si_{1-x-y}Ge_xC_y$ alloys with a meaningful amount of carbon incorporation. However, kinetically-dominated epitaxial growth techniques, typically operated at low temperatures (450-650°C) have been able to incorporate more carbon into Si or $Si_{1-x}Ge_x$. High quality $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ films have been fabricated with ~

2% substitutional carbon[4,5,6] by molecular beam epitaxy (MBE) and chemical vapor deposition (CVD).

During the epitaxial growth process, 'surface solubility' is more important than the bulk solubility in explaining carbon incorporation. The increased surface solubility can be explained by two factors[7]. First, the crystal surface breaks the bulk symmetry and provide sites for adatoms (adsorbed atoms) during the growth process. These surface sites are energetically more favorable compared to the bulk sites. Secondly, surface reconstruction may provide stable sites for carbon incorporation. For example, in a (2x1) reconstructed Si surface, there are two different sites. One site is located beneath the surface dimers (in the sub-surface) and the other is between the dimers[8]. Simulations by Kelires and Tersoff found that the site beneath the surface dimers is under compressive stress, a more favorable site for carbon to reside in[7,8]. Once carbon is incorporated into the sites below surface dimers, it is quickly buried and frozen as the growth continues. An enhancement of 10^4 in the substitutional carbon incorporation over equilibrium bulk solubility has been predicted[7].

2.2.2 Substitutional vs. Interstitial C incorporation

The challenge for the growth of $Si_{1-x-y}Ge_xC_y$ is not just carbon incorporation but the substitutional incorporation of carbon. Only substitutional carbon can compensate the compressive strain caused by Ge and affect the band structure. Interstitital carbon or Si-C complexes may create deep levels which degrade device performance by lowering carrier mobility, reducing carrier lifetime and causing junction leakage. For optimal device performance, it is necessary to incorporate carbon solely on substitutional sites.

Two key parameters, namely, growth temperature and growth rate, greatly affect substitutional carbon incorporation. Osten et al[9] studied $Si_{1-y}C_y$ films grown by molecular beam epitaxy (MBE) and showed that, with identical carbon flux and Si growth rate, the ratio of substitutional to interstitial carbon concentration decreased with an increased growth temperature while the total carbon level in the film is unchanged. They also showed that at the same growth temperature, a higher growth rate led to more efficient substitutional carbon incorporation, accounting for the change in Si/C flux ratio.

Mitchell et al studied the growth of Si_yC_y by chemical vapor deposition (CVD) by varying the growth temperature and silane (Si precusor) partial pressure[10]. They found that lower growth temperatures and higher silane partial pressures led to a higher substitutional C incorporation, as shown in figure 2.1. Since a higher silane partial pressure leads to a higher growth rate, it indirectly supports the above-mentioned observation, although we can not rule out any synergistic interaction between silane and C. They also studied the growth of $Si_{1-x-y}Ge_xC_y$ at 600°C with dichlorosilane, germane, and methylsilane as the precusors for Si, Ge, and C, respectively. They found 100% substitutional C incorporation in the $Si_{1-x-y}Ge_xC_y$ film with 20% [Ge] and up to 1.3% [C]. Above 1.3 at %, there appears to be less substitutional C measured by x-ray diffraction (XRD) than total C determined by secondary ion mass spectroscopy (SIMS)[11].

It is not surprising that lower growth temperatures and higher growth rates lead to more efficient substitutional carbon incorporation. High temperatures provide enough energy for the epitaxial film to go to more thermodynamically stable states, such as SiC or carbon clusters, as have been observed experimentally. Consequently, lower temperatures are needed to form metastable $Si_{1-x-y}Ge_xC_y$ alloys. In addition, a

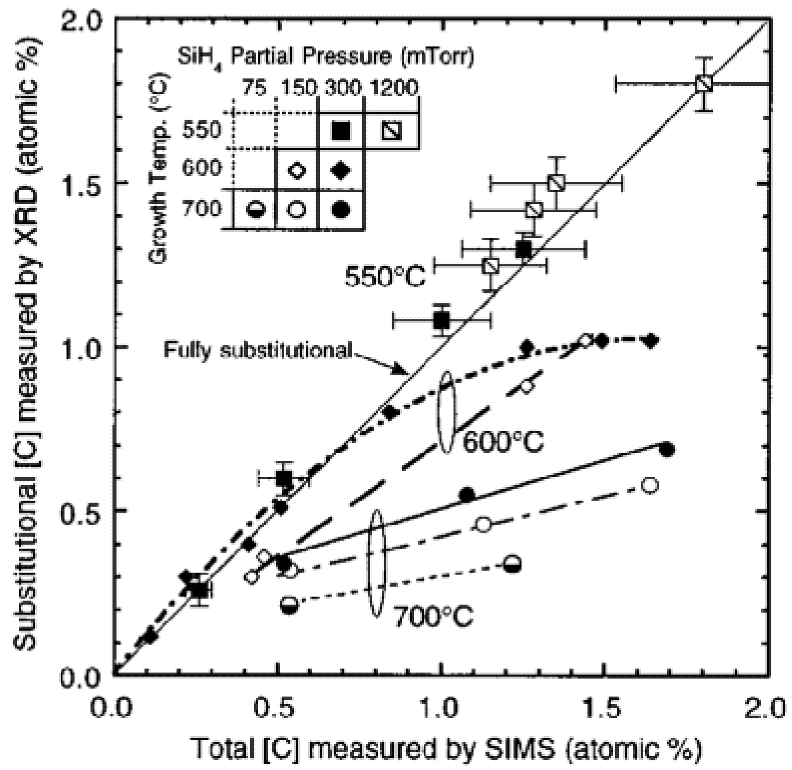

Figure 2.1: Substitutional C incorporation as a function of growth temperature and silane partial pressure. From ref(10).

higher growth rate reduces the accessible time for the frozen carbon to move around the growing surface or for Si to form Si-C and related defect complexes. Unfortunately, lowering growth temperature inevitably lowers the growth rate by CVD and sometimes leads to poor film quality.

We have also studied the growth of $Si_{1-x-y}Ge_xC_y$ alloys by rapid thermal chemical vapor deposition (RTCVD). We found that, by fixing the growth rate (through the change in germane flow) and varying the growth temperature (625°C and 575°C), a lower growth temperature resulted in a higher substitutional C incorporation for the same methylsilane flow. (see Fig. 3.3) By fixing the growth temperature and methylsilane gas flow, and varying the growth rate (again through the germane flow), a superior film quality based on photoluminescence (PL) measurement was obtained with higher growth rate, as shown in figure 2.2. We suspected that superior film quality was due to higher substitutional C to interstitial C ratio. Since the growth rate was controlled by varying the germane gas flow (Ge concentration), it is not clear whether the higher substitutional carbon incorporation is due to the higher growth rate itself or due to the higher germane (and thus strain) level. Nonetheless it seems to indirectly support the above-mentioned argument. This better success at achieving higher substitutional C levels with high germanium is why most of our data for C levels in excess of 2% are for films with relatively high Ge levels of ~0.4. Since disilane gas is known to lead to a higher Si deposition rate, we speculate that a higher substitutional C concentration may be achieved by replacing silane and DCS with disilane.

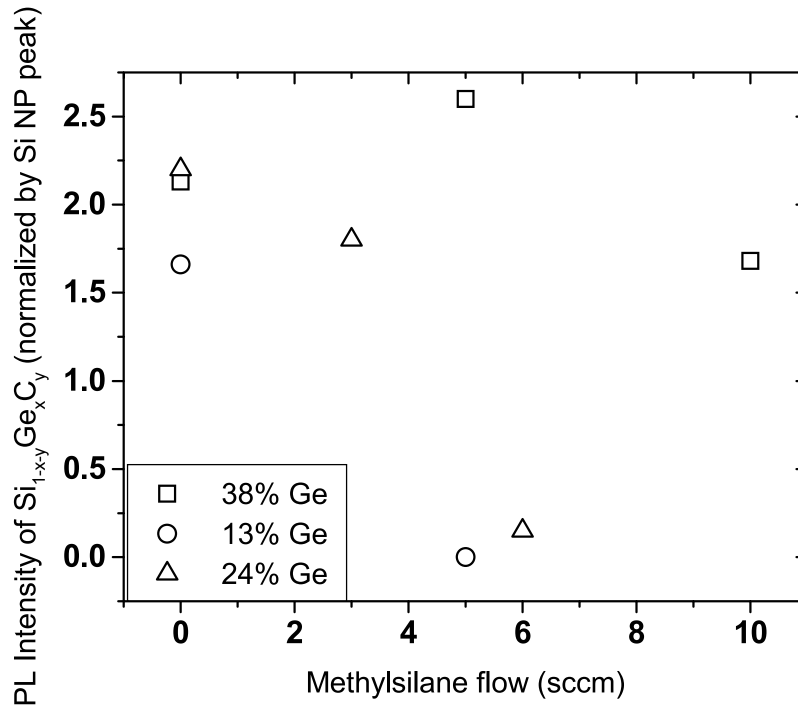

Figure 2.2: PL intensity of no-phonon $Si_{1-x-y}Ge_xC_y$ peak as a function of methylsilane. For the same methylsilane flow, the PL intensity decreases when the Ge concentration (growth rate) is decreased. Note also that for the sample with 13%Ge and 5sccm methylsilane flow, no $Si_{1-x-y}Ge_xC_y$ PL was observed. Instead, there was a broad peak attributed to defects centered at 800 meV. Similar peaks were observed for samples with higher methylsilane flow (~20 sccm). All samples were grown at 575ºC. Typical $Si_{1-x-y}Ge_xC_y$ thickness is ~20nm. All samples had ~15nm Si cap layers grown at 675-700 ºC. PL measurement was performed at 77K.

2.3 Strain Manipulation by Substitutional Carbon Incorporation

2.3.1 Strain Compensation in $Si_{1-x-y}Ge_xC_y$ by Substitutional Carbon

The most common way to investigate the change of strain in the strained $Si_{1-x}Ge_x$ film due to incorporation of substitutional carbon is to study the change in the vertical (the growth direction) lattice constant of the epitaxial film. When a pseudomorphic $Si_{1-x}Ge_x$ film is deposited on a Si (100) substrate, it is under a compressive strain in order to match the in-plane lattice constant with that of the underlying Si substrate. As a result, the vertical lattice constant (the lattice constant along the growth direction) is increased, and the resulting crystal structure of the film is tetragonal. As substitutional carbon is added to the film, the vertical lattice constant is reduced and the strain is reduced. XRD measurement has been widely used to capture the change of lattice constant by substitutional carbon incorporation, based on the Bragg's law,

$$2\, d_{004} \sin\theta = \lambda \qquad (2.1)$$

where d_{004} is the distance between (004) planes of $Si_{1-x-y}Ge_xC_y$; θ is the Bragg angle (angle between the incident beam and the sample), and λ is the wavelength of the x-ray used. Figure 2.3(b) shows (004) x-ray diffraction peak of the lattice constant of Si, $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ with various substitutional carbon levels. One sees that, as substitutional carbon is added to reduce the strain, the vertical lattice constant moves toward that of the underlying Si substrate.

Based on the Bragg's law, one can calculate the vertical lattice constant of the strained $Si_{1-x-y}Ge_xC_y$ ($a^{\perp}_{SiGeC}$). We first observe from the elastic theory[22] that

$$a^{r}_{SiGeC} - a_{Si} = \frac{1-\nu}{1+\nu}\left(a^{\perp}_{SiGeC} - a_{Si}\right) \qquad (2.2)$$

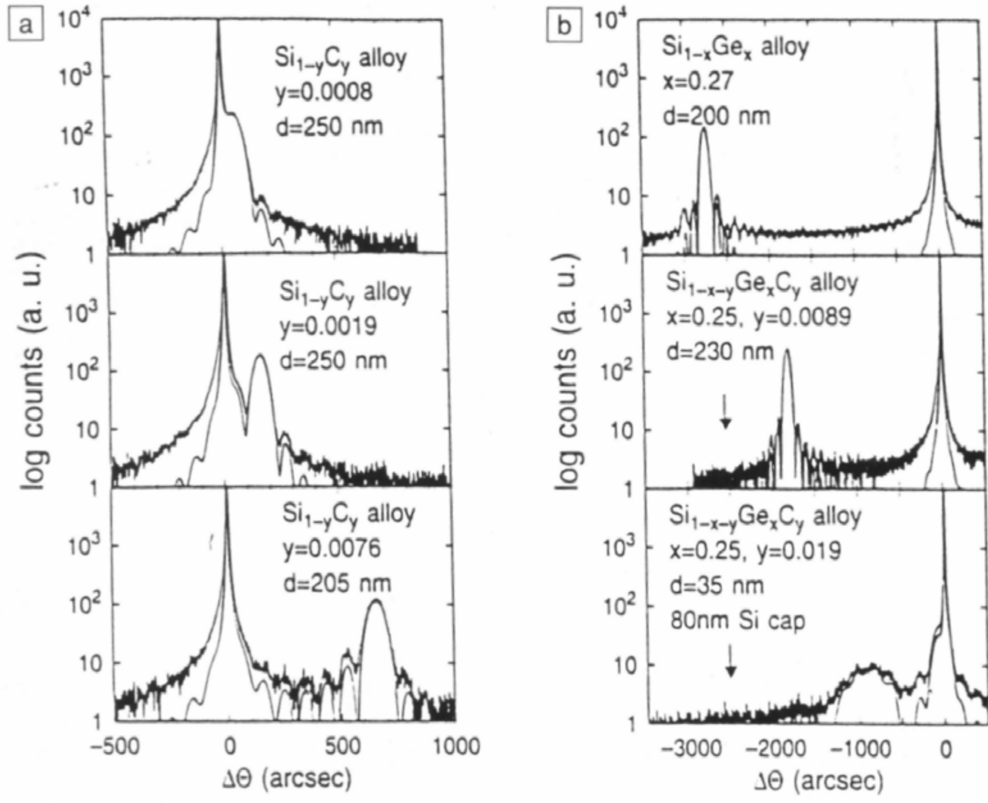

Figure 2.3: X-ray rocking curves of pseudomorphic (a) $Si_{1-y}C_y$ and (b) $Si_{1-x-y}Ge_xC_y$ grown on (100) Si substrate[12].

where a^{r}_{SiGeC} is the lattice constant of the relaxed $Si_{1-x-y}Ge_xC_y$; a_{Si} is the lattice constant of Si and ν is the Poisson's ratio which can be represented by $\nu = \frac{c_{12}}{c_{11}+c_{12}}$ (c_{11}, c_{12} are the elastic constants of $Si_{1-x-y}Ge_xC_y$). After a manipulation, we have

$$a^{r}_{SiGeC} = \frac{c_{11}}{c_{11}+2c_{12}}(a^{\perp}_{SiGeC} - a_{Si}) + a_{Si} \quad (2.3)$$

To obtain the substitutional carbon concentration from shifts in X-ray peaks, one has to make two assumptions. First, one assumes that the elastic constants of $Si_{1-x-y}Ge_xC_y$ can be linearly interpolated between Si, Ge, and diamond[13]. Second, one assumes that Vegard's law applies so that the relaxed lattice constant of $Si_{1-x-y}Ge_xC_y$ can be obtained based on the linear interpolation of the lattice constants of Si (0.5431nm), Ge (0.5678nm) and diamond (0.3546nm)[14]. It follows that,

$$(1-x-y)a_{Si} + x a_{Ge} + y a_C = \frac{c_{11}}{c_{11}+2c_{12}}(a^{\perp}_{SiGeC} - a_{Si}) + a_{Si} \quad (2.4)$$

where $a^{\perp}_{SiGeC}$ can be obtained from equation (2.1). To get *y* (substitutional C concentration), one needs to first obtain *x* (Ge concentration). Ge concentration can be determined separately from XRD on the strained $Si_{1-x}Ge_x$ film[15] or from other methods on the strained $Si_{1-x-y}Ge_xC_y$ film, such as SIMS and Rutherford backscattering (RBS). Once the Ge concentration is independently known, then the substitutional carbon concentration can be obtained based on (2.4). Based on the interpolation between Si, Ge, and diamond[22], the Ge/C strain compensation is 8.3, where the Ge/C strain compensation ratio is defined as the ratio of Ge to C in the unstrained $Si_{1-x-y}Ge_xC_y$ alloys on a (001) Si

substarte. This is the value used for the rest of this work. The compensation ratio becomes 9.5 when the interpolation based on Si, Ge and β-SiC is used[22].

We note that how to apply Vegard's law to calculate the relaxed lattice constant of $Si_{1-x-y}Ge_xC_y$ is still under debate. Some people suggest[16] splitting $Si_{1-x-y}Ge_xC_y$ into a $Si_{1-x}Ge_x$–part and a SiC-part in order to capture the negative deviation from Vegard's law for $Si_{1-x}Ge_x$, according to Dismukes's model[17]. The Ge/C ratio obtained by this method is higher than that obtained directly from linear interpolation of Si, Ge, and SiC. The Ge/C ratio depends on the Ge level since the deviation varies with Ge concentration. Hoyt et al estimated[16] that, for 20 % Ge, the Ge/C strain compensation ratio is 11.4.

Recent theoretical predictions by P.C. Kelires[18] proposed a strong deviation of the lattice parameter of $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ from Vegard's law. A deviation from the Vegard's law would introduce an error in the calculation of the relaxed lattice constant of $Si_{1-x-y}Ge_xC_y$, thereby incurring inaccuracy in calculating the substitutional C level. A physical explanation of the deviation from Vegard's law was given by Martins et al[19], which was based on a charge transfer from Ge to Si or from Si to C, due to their different electronegativities. The charge transfer creates an additional attractive force between atoms and leads to a smaller lattice constant. Stangal et al[20,21]reported that, by measuring the substitutional C concentration independently from the resonant backscattering (rBS)[20] technique, in which the C resonance is observed at the 5.72 MeV He^+ beam energy. A negative deviation from the Vegard's law was observed, in agreement with Kelires's model. As a result, the Ge/C strain compensation ratio was determined to be ~11.

Even though XRD measures the mean value of the strain in the film, it does not provide any information regarding the local lattice structure of $Si_{1-x-y}Ge_xC_y$ since the

interaction between X-rays and the lattice is weak. On the other hand, Raman spectroscopy is a useful tool for studying the microstructure of strained and unstrained alloys[22]. Dietrich[23] grew a perfectly strain-compensated $Si_{1-x-y}Ge_xC_y$ and found that Si-C bonds were stretched by 7% with respect to that in cubic SiC structures. Different Si-Si bond lengths were also observed which were attributed to those Si-Si bonds with substitutional C in the neighborhood. It is expected that these local structure irregularities may reduce carrier mobility, but further studies are needed to investigate the effect on the band structure of $Si_{1-x-y}Ge_xC_y$.

2.3.2 Tensile-strained $Si_{1-y}C_y$ by Substitutional Carbon incorporation

Due to a smaller size of C atoms, a pseudomorphic $Si_{1-y}C_y$ film is under tensile strain when grown on a Si substrate. Figure 2.3(a) shows the pseudomorphic $Si_{1-y}C_y$ film grown on a (100) Si substrate. Although our focus is on compressively strained $Si_{1-x-y}Ge_xC_y$, we note that a tensile-strained $Si_{1-y}C_y$/Si heterostructure possesses a conduction band offset, which is very useful in providing electron-based device applications, such as electron-based field effect transistors. To determine the substitutional C level in a $Si_{1-y}C_y$ film, we follow similar steps and assumptions as in section 2.3.1. Based on equation (2.3), we have

$$a_{SiC}^{\perp} = (1 + 2\frac{c_{12}}{c_{11}})(a_{SiC}^{r} - a_{Si}) + a_{Si} \quad (2.5)$$

where $a_{SiC}^{\perp}$ is the vertical lattice constant of the pseudomorphic $Si_{1-y}C_y$ and a_{SiC}^{r} is the relaxed (cubic) lattice constant of $Si_{1-y}C_y$. Figure 2.4 shows the vertical lattice constant of a pseudomorphic $Si_{1-y}C_y$ with the relaxed lattice constant of cubic $Si_{1-y}C_y$ and elastic

constants calculated based on Vegard's law. The dashed line corresponds to the linear interpolation between Si and diamond. The dotted line represents the linear interpolation between Si and β-SiC and the solid line is plotted according to Kelires's calculations[24]. Once the vertical lattice constant is determined from XRD, the substitutional C fraction can be obtained based on figure 2.4.

2.4 Electrical and Optical Properties of Strained $Si_{1-x-y}Ge_xC_y$

Photoluminescence studies on strained $Si_{1-x-y}Ge_xC_y$ have shown that the addition of C increases the bandgap of the still compressively strained $Si_{1-x-y}Ge_xC_y$ by 21-25meV/%C[25,26]. The bandgap increase by the addition of C has also been confirmed from $Si/Si_{1-x-y}Ge_xC_y/Si$ heterojunction bipolar transistors[27]. The similarity of the two results indicates that the bandgap increase is not a localized effect but is uniform through out the material. Since C increases the bandgap at only half the rate than is expected given the strain it compensates, it is suspected C has an intrinsic effect on the bandgap and the effect is to lower the bandgap by 24-28 meV[28]. Indeed, it was recently reported that 1% C actually decreased the unstrained $Si_{1-x-y}Ge_xC_y$ by 20 meV/%C[29]. It seems surprising since both diamond and β-SiC have a larger bandgap than that of Si and Ge. However, this bowing effect of the curve of bandgap vs. lattice constant has also been observed in III-V materials[30].

Diodes based on $Si_{1-x-y}Ge_xC_y$ were fabricated and results showed that the initial addition of C did not increase the reverse-biased leakage current for levels of C less than 1%. However, the diodes exhibited premature breakdown and higher leakage current when the C concentration is ≥ 1%. Photoresponse spectroscopy on these diodes showed

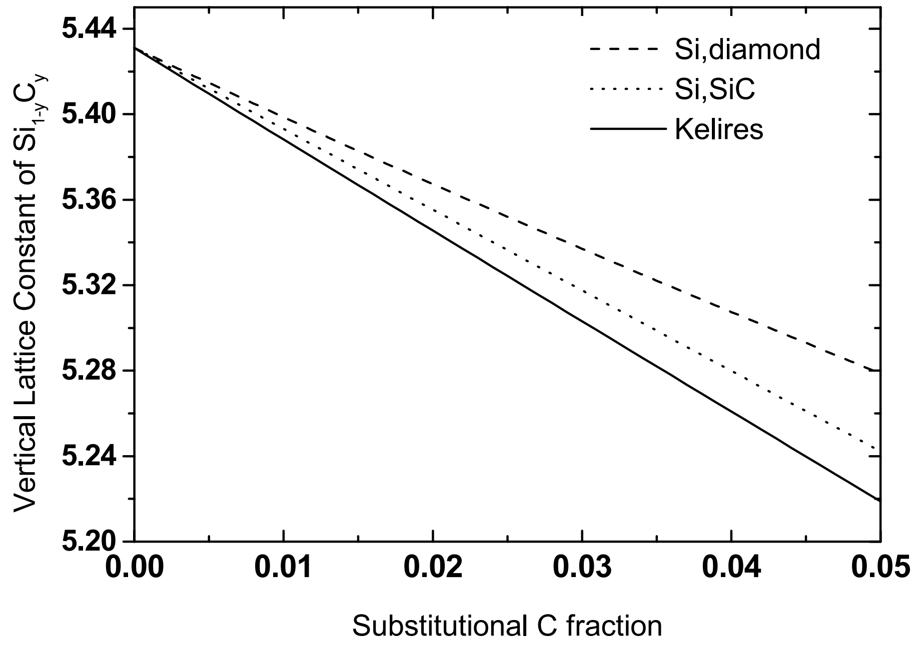

Figure 2.4: Dependence of the vertical lattice constant of pesudomorphic $Si_{1-y}C_y$ on Si (100).

excess defect-related sub–bandgap absorption[31]. We have also fabricated pn diodes (#2114) with below-critical-thickness $Si_{1-x-y}Ge_xC_y$ layers in the depletion region. A much higher leakage current was also observed compared to that in the sample with only $Si_{1-x}Ge_x$. TEM and electron beam induced current studies showed no visible defects. We suspect that C-related point defects are responsible for the high leakage current. Further studies are needed to minimize the C-related defects to optimize $Si_{1-x-y}Ge_xC_y$-based device performance.

2.5 Previous Studies on the Valence Band Offset of Compressively Strained $Si_{1-x-y}Ge_xC_y$ /Si (100)

Knowing the effect of C on the bandgap of the still compressively strained $Si_{1-x-y}Ge_xC_y$ /Si (100), one needs to see how this bandgap change is reflected in the band alignment of the strained $Si_{1-x-y}Ge_xC_y$ /Si (100). Besides the work to be presented in the next chapter, there has been a few other studies on the band offsets of strained $Si_{1-x-y}Ge_xC_y$/Si (100). Rim et al reported that from C-V analysis of $Si_{1-x-y}Ge_xC_y$-based metal-oxide-semiconductor structures, C decreased the valence band offset (ΔE_v) by 20-30 meV/%C [32] (i.e., C shifted down the valence band edge of $Si_{1-x-y}Ge_xC_y$), a magnitude similar to the band gap increase by C. X-ray photoelectron spectroscopy study by Kim et al showed a negligible effect of C on the valence band offset[33], within an accuracy of ±30 meV.

Conflicting reports were also reported. Eberl et al[34] conducted PL measurements on the ΔE_V of $Si_{1-x-y}Ge_xC_y/Si_{1-y}C_y$ double-quantum wells and found that the addition of C increased the ΔE_V by ~10 meV/%C. However, the authors also suggested that more detailed measurements are needed to study factors such as confinement effect and

modified excitonic binding energy. Admittance spectroscopy $Si_{1-x-y}Ge_xC_y$/Si suggested that C reduced the conduction band offset by ~100 meV/%C, and valence band offsets by ~ 80 meV/%C[35]. One concern with this report, however, is a lack of $Si_{1-x}Ge_x$ control samples for comparison.

In the next chapter, we study the valence band offset of the compressively strained $Si_{1-x-y}Ge_xC_y$ /Si (100) by various electrical and optical measurements. We will compare their results and reliability.

2.6 Summary

In this chapter, we have reviewed the strained $Si_{1-x-y}Ge_xC_y$ /Si (100) materials. We first described that both low growth temperature and high growth rate are essential to a high substitutional C incorporation. The strain compensation ratio of Ge/C was then reviewed. We also reviewed electrical and optical properties and reported that the addition of C increased the band gap of $Si_{1-x-y}Ge_xC_y$ by 21-16 meV/%C. Finally, we reviewed previous work on the measurement of the valence band offset of the compressively strained $Si_{1-x-y}Ge_xC_y$ /Si (100) materials.

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Chapter 3

Band Alignment of Strained $Si_{1-x-y}Ge_xC_y$ / Si (100) Heterojunctions

3.1 Introduction

In the previous chapter we reviewed that the addition of 1% substitutional carbon increased the bandgap of $Si_{1-x}Ge_x$ by 21-25 meV. The bandgap increase implies a change of valence and/or conduction band offset of the $Si_{1-x}Ge_x$/Si (100) with the addition of carbon. Our goal is this chapter is to determine how the bandgap change is allocated in the band alignment at the compressively strained $Si_{1-x-y}Ge_xC_y$/Si (100) interface. Understanding the band alignment is crucial since many device applications such as field-effect transistors (FET)[1,2] and various kinds of infrared detectors[3,4] are based on the band offset. In addition, the band alignment determines the type of carrier (electron or hole) to be used. We will use different measurement techniques to determine the valence band offset of compressively strained $Si_{1-x-y}Ge_xC_y$ /Si (100) and discuss their reliability. Once the valence band offset is known, we can infer the conduction band offset based on the total bandgap change due to carbon.

Two types of structures are used to measure the offset. One is a compressively strained p^+ $Si_{1-x-y}Ge_xC_y$ /p^- Si (100) heterojunction diode. If we treat the heavily doped $Si_{1-x-y}Ge_xC_y$ to be metal-like, this heterojunction is very much like a metal-semiconductor Schottky diode. Therefore, we can measure the valence band offset as if measuring the Schottky barrier height. In 3.3, we use current-voltage measurement to study the valence band offset. In 3.4, we use capacitance-voltage measurement to study the same structure

and in 3.5, optical characterization is reported. The other structure we used in this study is a $Si/Si_{1-x-y}Ge_xC_y/Si$ quantum well structure and in 3.6 we discuss the valence band offset measurement on this structure by admittance spectroscopy. We then compare our studies with the reported number in the literature in 3.7.

3.2 Sample Growth and Structure Characterization

The p^+ $Si_{1-x-y}Ge_xC_y/p^-$ Si unipolar diodes were grown by RTCVD at a chamber pressure of 6 torr. Dichlorosilane ($Si_2H_2Cl_2$), germane (GeH_4) and methylsilane ($SiCH_6$) were used as the precursors of Si, Ge, and C, respectively. The flow rates were 26 sccm for dichlorosilane, 1-4.5 sccm for germane, and 0-0.35 sccm for methylsilane, all in a H_2 carrier, resulting in [Ge] = 20% - 39.5%, and [C] = 0% - 2.5%. All $Si_{1-x-y}Ge_xC_y$ layers were in-situ doped with diborane. In each sample, a p^+ Si layer with boron doping ranging from $3x10^{19}$ to $6x10^{19}/cm^3$ was first grown at 1000 °C on a p^- Si substrate for use as a bottom contact, followed by the deposition of a p^- Si layer ($\sim10^{16}/cm^3$) with thickness around 250 ± 50nm. The p^- Si layer was not intentionally doped by a diborane flow, but was doped by the boron outdiffuson from the bottom contact layer during high temperature growth as well as background doping caused by residual boron inside the chamber after the growth of the bottom contact layer. $Si_{1-x-y}Ge_xC_y$ layers were then deposited at growth temperatures between 575 °C and 625 °C. A 2nm thick undoped $Si_{1-x-y}Ge_xC_y$ layer was first deposited as a precaution for preventing heavily doped boron from diffusing to the underlying p^- Si layers followed by the p^+ $Si_{1-x-y}Ge_xC_y$ (~18nm) with dopings ranging from 6 x $10^{18}/cm^3$ to 4 x $10^{19}/cm^3$.

Finally, a 20nm heavily doped (~ $10^{20}/cm^3$) Si layer was grown for a top contact. Diodes were made by a two-step mask process. A mesa creation (320x180 μm^2) by plasma etching was followed by Ti/Al (or Al) metallization. A typical device structure is shown in figure 3.1.

Figure 3.2 shows the (004) X-ray diffraction (XRD) performed on the strained $Si_{1-x-y}Ge_xC_y$ layers with 39.5% Ge and various C concentrations. The concentration of Ge was obtained by measuring the no-carbon XRD peak relative to that of Si substrate. This value is consistent with the Ge concentration obtained by PL measurements. As C is added, the peak starts shifting toward the Si peak, indicating a decrease in lattice constant, i.e., reduced strain. Assuming that the Ge content was unchanged by the addition of methylsilane at constant germane flow (analysis by SIMS indicated that the Ge content was unchanged, within an accuracy of 1-2%Ge), the substitutional C content was quantified by the method discussed in Chapter 2, assuming a Ge:C strain compensation ratio of 8.3. A substitutional C level of up to 2.5% was measured for samples in this study. Figure 3.3 displays the substitutional C level as a function of methylsilane flow. High resolution transmission electron microscopy (HRTEM) performed on the $Si_{0.593}Ge_{0.395}C_{0.012}$ sample at Princeton Materials Institute shows good interface quality and no evidence of dislocations or SiC precipitates[5].

3.3 Valence Band Offset of Strained $Si_{1-x-y}Ge_xC_y$ /Si (100) by Current-Voltage Measurement

Shown in figure 3.4 is the schematic band diagram of the zero-biased and reverse-biased p^+ $Si_{1-x-y}Ge_xC_y$/ p^- Si diode. $E_{F(SiGeC)}$ is the position of Fermi level relative to the valence band of $Si_{1-x-y}Ge_xC_y$; V_{bi} is the built-in voltage of the junction; $E_{F(Si)}$ is the

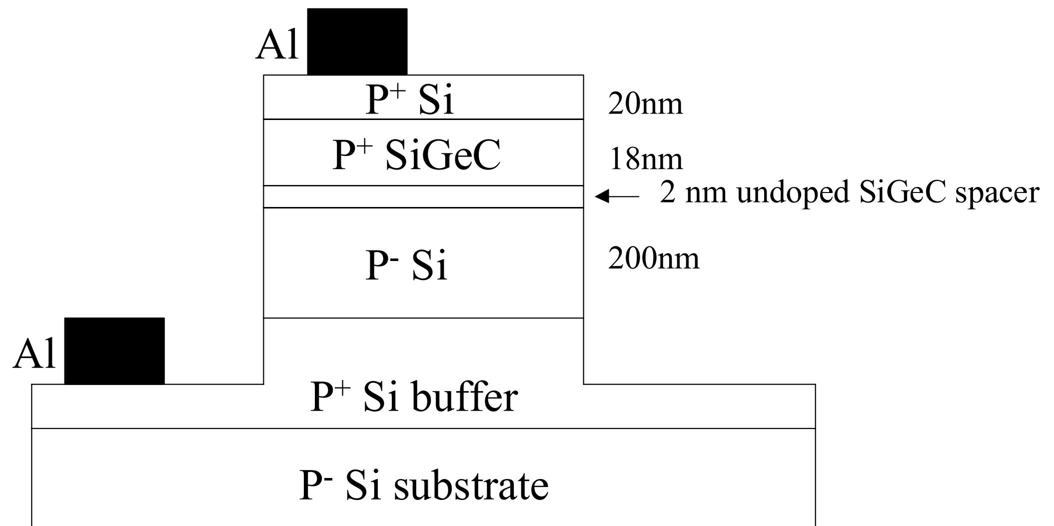


Figure 3.1: A typical device structure of the p^+ $Si_{1-x-y}Ge_xC_y$ / p^- Si diode.

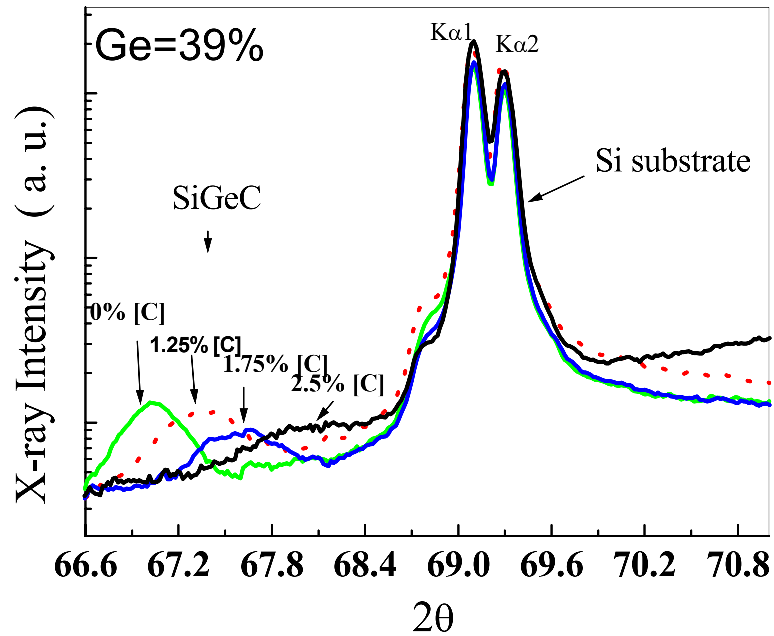


Figure 3.2: (004) X-ray diffraction spectra of $Si_{1-x-y}Ge_xC_y$ thin films on Si (001). Two Si substrate peaks are due to Cu $K\alpha_1$ and $K\alpha_2$ x-ray lines. Broad $Si_{1-x-y}Ge_xC_y$ peaks at high C levels may be due to Scherer broadening in thin films or degraded material quality. XRD characterization was performed in the Chemical Engineering Department at Princeton University with the assistance of C.J. Lay.

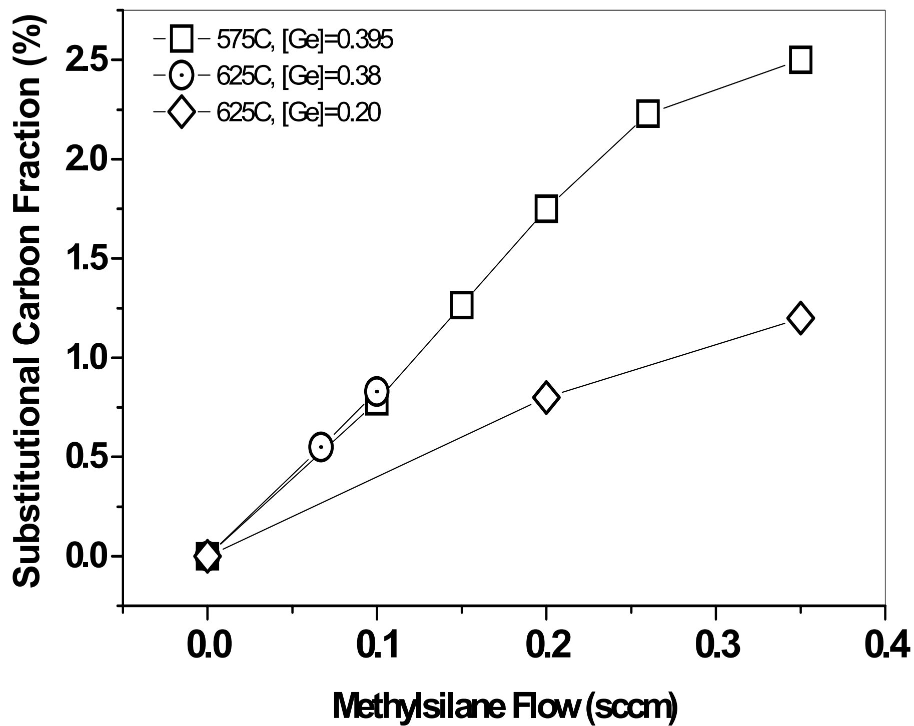
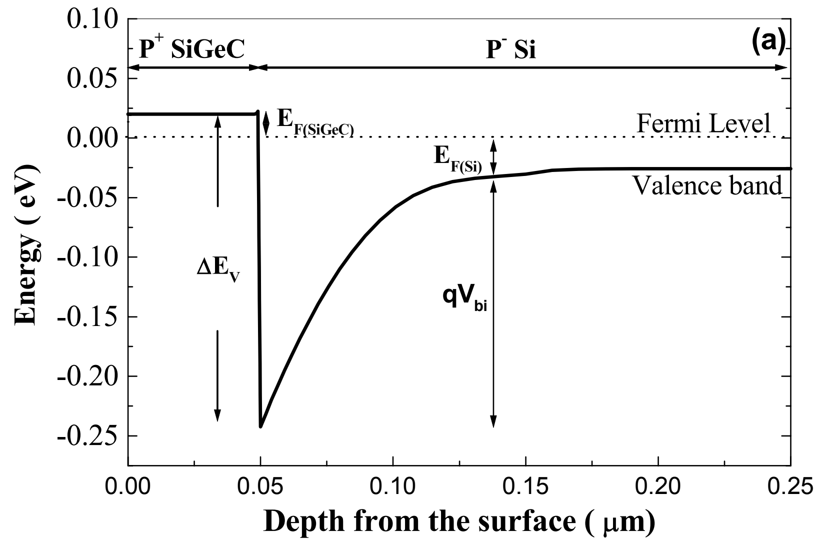


Figure 3.3: Substitutional C level is plotted as a function of the methylsilane flow. Substitutional C level was determined by XRD using Ge/C=8.3. The flow rates were 100sccm, 400 sccm, and 300 sccm for layers with 20%, 38%, and 39.5% Ge, respectively.



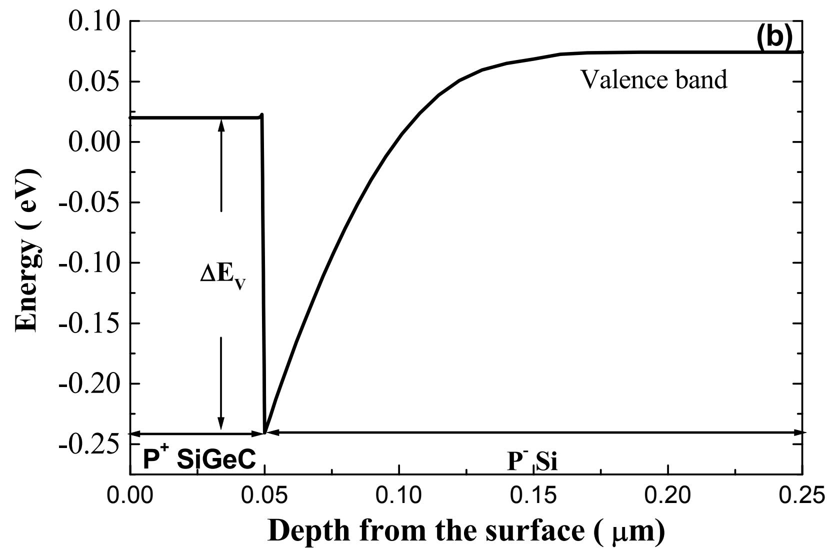


Fig. 3.4: (a)Zero-bias valence band diagram of p+ $Si_{1-x-y}Ge_xC_y$ / p⁻ Si diode. (b) Reverse-biased (-0.1V) valence band diagram of p+ $Si_{1-x-y}Ge_xC_y$ / p⁻ Si diode. The valence band diagram was generated by using the Medici simulator.

distance of the valence band of Si relative to the Fermi level. Under forward bias, the magnitude of hole current from the p^- Si depends on the applied voltage which shifts the valence band structure of the p^- Si relative to that of $Si_{1-x-y}Ge_xC_y$. Under reverse bias ($V_{SiGeC} > V_{si}$), the valence band offset (ΔE_V) between $Si_{1-x-y}Ge_xC_y$ and Si blocks hole current from p^+ $Si_{1-x-y}Ge_xC_y$, so that the device rectifies at low temperatures. Within a certain temperature range, the thermionic emission of holes across the valence band offset determines the ideal reverse current and the hole current is exponentially dependent on temperature. Figure 3.5 is the current-voltage characteristics of the diode containing 20% Ge and 0.84 % of C. The diode rectifies at low temperatures, and the reverse current strongly increases with temperature. The valence band offset of $Si_{1-x-y}Ge_xC_y$/Si was obtained by determining the activation energy of the thermionic current.

The expression for the thermionic current for heterojunction semiconductors is somewhat different from that for a metal-semiconductor contact. Here we use the expression obtained by L.L.Chang[6], in which

$$J = A^* \frac{1}{\sqrt{T}}\left(1 - \frac{qV}{\Delta E_v}\right)\left(e^{\frac{qV}{kT}} - 1\right)e^{\frac{-q\Delta Ev}{kT}} \qquad (3.1)$$

where V is the applied voltage; ΔE_V is the valence band offset, and A^* is defined as the effective Richardson constant which depends on the doping level in p^- Si and ΔE_V. It can be seen that the temperature dependence is different from that for a metal-semiconductor contact. Also the thermionic current increases with the magnitude of the reverse voltage. Figure 3.7 shows the plot of $I \times T^{1/2}$ vs. 1000/T with various reverse bias voltages for the same device shown in figure 3.5. In order to determine the valence band offset, the slope

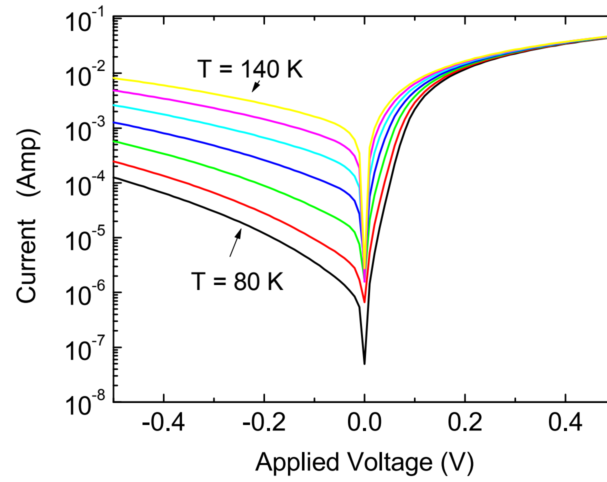


Figure 3.5: Current-voltage characteristics of the p^+ $Si_{1-x-y}Ge_xC_y/p^-$ Si unipolar diode as a function of temperature. The current was plotted at an increment of 10K from 80K.

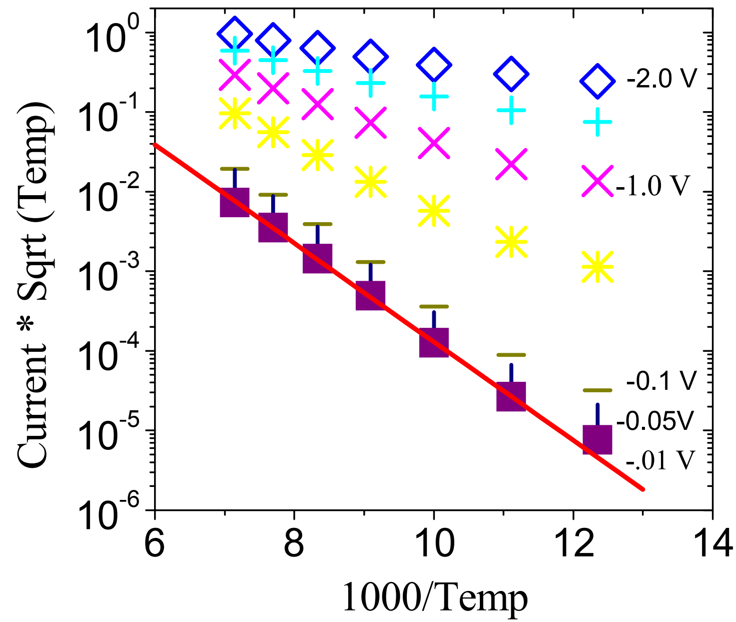


Figure 3.6: Plots of current vs. temperature with various reverse-biased voltages. Plots are based on the same sample with current-voltage characteristics shown in figure 3.5. Note that the slope was little changed for voltage ≤ -0.1 volt. The valence band offset was obtained by linearly fitting the data at V=-0.01 volt.

at very low bias voltage (-0.01) was used due to the fact that the current does not depend on the coupling of voltage and temperature at low voltages, as seen from equation (3.1). Note that at –0.01V, the error caused by $(e^{\frac{qV}{kT}} - 1)$ term in the temperature range studied is less than a factor of two, which is negligible compared to the orders of magnitude change of current due to $e^{\frac{-q\Delta Ev}{kT}}$.

Based on the above-mentioned procedure, the valence band offsets of the $Si_{1-x-y}Ge_xC_y/Si$ heterostructures with 20% [Ge] and different carbon concentrations were determined and plotted in figure 3.7. Although a downward trend of the valence band offsets with increased carbon concentration is observed, there is a wide scatter of data among devices. The wide scatter of data is not surprising since the leakage current of a randomly chosen device can be easily dominated by non-ideal sources such as local defects, edge effects, or carbon-related defects, etc. Measurements on larger devices demonstrated even more smaller band offset, an indication that there is more no-ideal leakage current.

Therefore, in the next section, we use a capacitance-voltage technique to determine the valence band offset. Capacitance-voltage is a measurement over the entire device area and therefore is less sensitive to the local defects.

3.4 Valence Band Offset of Strained $Si_{1-x-y}Ge_xC_y$ /Silicon (100) by Capacitance–Voltage Measurement

In this section, we use capacitance-voltage technique to repeat the valence band offset measurements of the samples used in section 3.3. The capacitance of the diodes was measured as a function of reverse-biased voltage at 100 K. The ac frequency used in

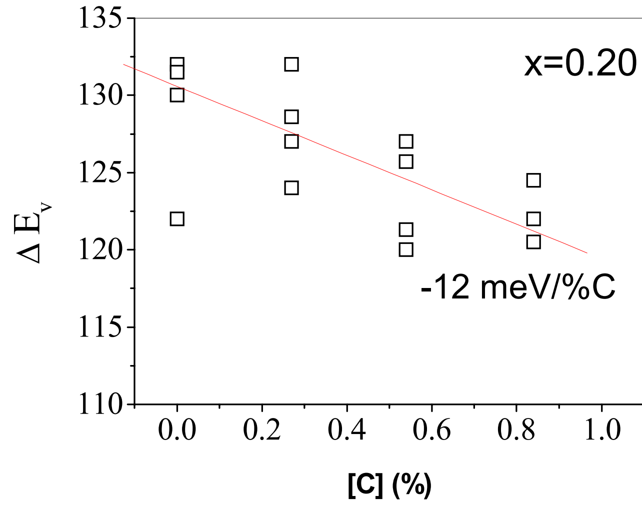


Figure 3.7: Valence band offset of $Si_{1-x-y}Ge_xC_y$ /Si as a function of C concentration with 20% Ge in the $Si_{1-x-y}Ge_xC_y$layer. Scatter of data points may be indicative non-ideal sources of current, such as due to carbon-related defects.

this measurement ranged from 10 KHz to 4 MHz, and the amplitude was set at 25-50 mV.

From the band diagram in figure 3.4(a), we observe that the valence band offset can be expressed by,

$$\Delta E_V = E_{F(SiGeC)} + qV_{bi} + E_{F(Si)} \qquad (3.2)$$

Much like a Schottky barrier or a one-sided pn junction, the capacitance per unit area C is given by,

$$\frac{1}{C^2} = \frac{2(V_{bi} - V)}{q\varepsilon N_A} \qquad (3.3)$$

where V is the DC bias and N_A is the doping concentration on the Si side of the heterojunction. By plotting $1/C^2$ vs. applied DC voltage, V_{bi} and N_A ($E_{F(Si)}$) can be obtained. Figure 3.8 shows the capacitance-voltage characteristics of the samples containing 39.5% Ge and various C fractions. The $1/C^2$-V data points are linear over the range of applied voltages, and the extracted Si doping concentrations are in the range of $10^{17}/cm^3$. The variation of the doping level among samples was due to the variation in the doping level of bottom contact layers and background doping. A spreading resistance measurement was performed on one of the samples and the measured doping concentration is consistent with that obtained by $1/C^2$-V data. The slope and intercept were not affected by ac amplitude used in this study (25-50 mV), and the data shown in figure 3.8 were measured with ac amplitude of 30 mV. The extrapolated built-in voltages decrease as more C is added. Based on the doping level, we calculated $E_{F(Si)}$ at 100K. $E_{F(SiGeC)}$ was obtained by a straightforward calculation from the doping concentrations

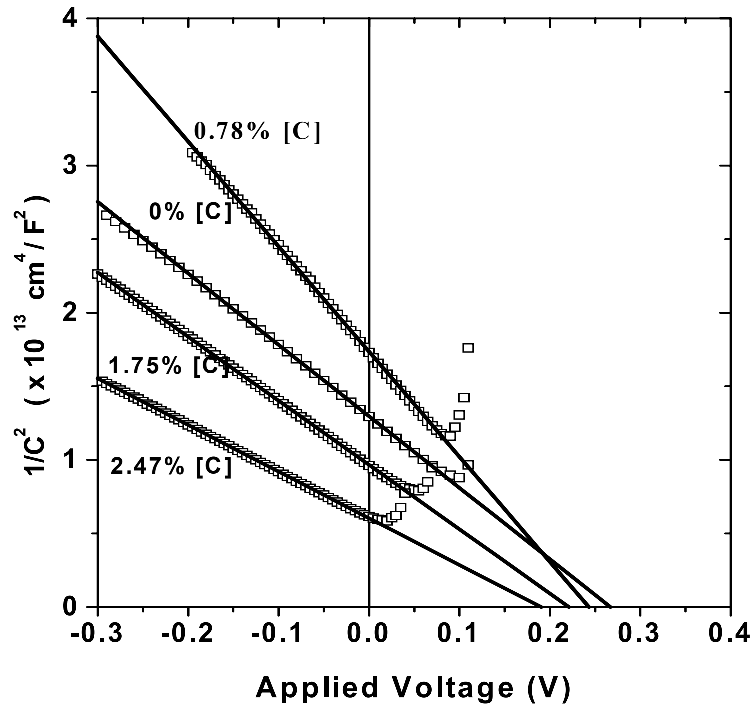


Figure 3.8: $1/C^2$ is plotted against voltage for p^+ $Si_{1-x-y}Ge_xC_y$ / p^- Si with x=0.395 and different C concentrations.

in the $Si_{1-x-y}Ge_xC_y$ obtained by SIMS on similarly grown layers, assuming the density of states is independent of C level[7]. We note that SIMS measurements show the boron incorporation in $Si_{1-x-y}Ge_xC_y$ independent of the C level for a given diborane flow. ΔE_v was calculated by combining qV_{bi}, $E_{F(SiGeC)}$ and $E_{F(Si)}$, as illustrated in equation (3.2). There is a consistent decrease in the valence band offset of $Si_{1-x-y}Ge_xC_y$/Si as C is added, as shown in figure 3.19. It seems that growth temperature, dopings and Ge level have no significant effect on the effect of C on ΔE_V, although more detailed studies are needed. The observed dependence for the three samples plotted are –(25±1) meV/%C, -(20±3) meV/%C, and –(29±3) meV/%C. We also found that the *absolute* ΔE_V measured by the capacitance-voltage technique varied slightly with different AC frequencies (within 15 meV from 10 KHz to 1 MHz). However, the *change* of ΔE_V with C at a given frequency was negligibly influenced by the measurement frequency (< 4 meV/%C), as shown in figure 3.10.

By comparing the total bandgap change of +(21-25 meV)/%C (as reviewed in chapter 2) with the change in valence band offset by carbon, we conclude that all of the change in bandgap as C is added to strained $Si_{1-x-y}Ge_xC_y$ is accommodated in the valence band within experimental errors. The resulting band structure with large ΔE_V and negligible ΔE_c is similar to that of pseudomorphic $Si_{1-x}Ge_x$ on (100) Si.

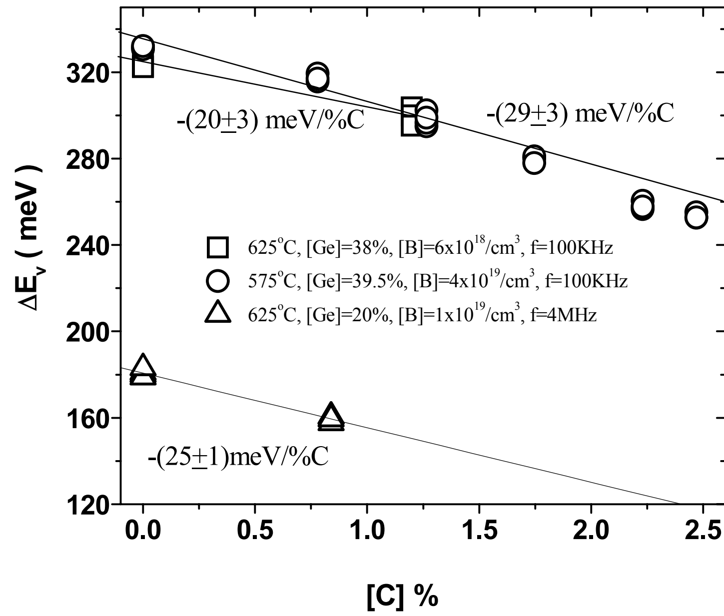


Figure 3.9: $Si_{1-x-y}Ge_xC_y$ valence band offset to Si as a function of substitutional C content for different dopings, Ge concentration, and growth temperature. The lines are the best linear fits over the range of 0-1.3% C, and 0% - 2.5% C.

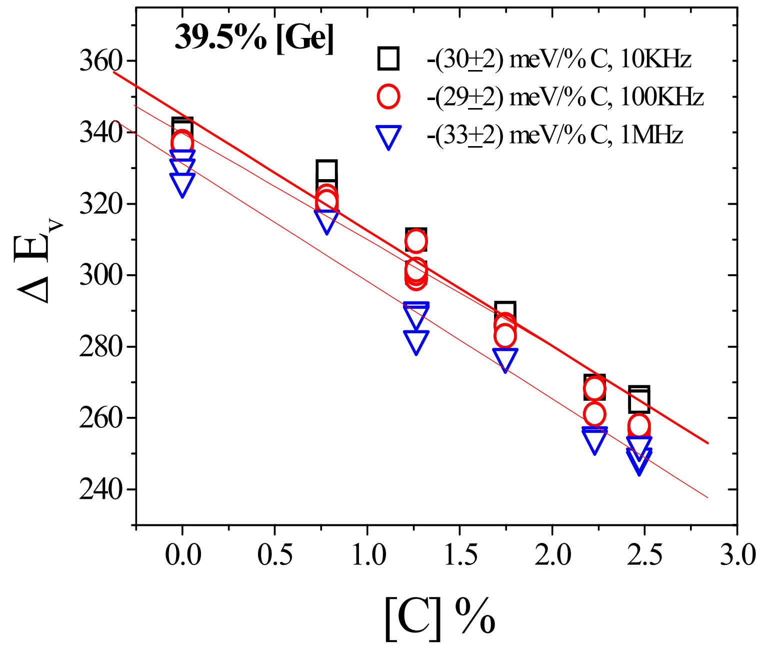


Figure 3.10: Measured valence band offset as a function of C level by three different measurement frequencies.

3.5 Valence Band Offset of Strained $Si_{1-x-y}Ge_xC_y$ /Silicon (100) by Heterojunction Internal Photoemission

In this section, we report the valence band offset measurement by heterojunction internal photoemission (HIP) on the p^+ $Si_{1-x-y}Ge_xC_y/p^-$ Si structures to determine ΔE_V. Devices were fabricated using the same samples studied in 3.3 and 3.4 with the same process but with larger mesa size and contact area for an easy gold wire contact. Good rectifying characteristics were observed at low temperatures (~ 77K), indicating a significant valence band offset between p^+ $Si_{1-x-y}Ge_xC_y$ $/p^-$ Si, consistent with the previous electrical measurements. Samples were further cooled down to ~ 4K to minimize thermionic leakage current for infrared photocurrent measurement. At 4K, good rectifying I-V characteristics were still observed, implying that there was a good ohmic contact, which is expected since both top and bottom contact layers were heavily doped. Optical absorption measurements were performed at 4K using a glowbar IR source, a monochromator and a phase sensitive detection.

From the band diagram in figure 3.4(a), hole current is mostly blocked by the valence band offset under reverse bias and the ideal leakage current comes from thermionically emitted holes from the p^+ $Si_{1-x-y}Ge_xC_y$ layer. When an infrared light is incident on the p^+ $Si_{1-x-y}Ge_xC_y$ layer, holes are excited to higher energy states, and if the photon energy is large enough for hole to overcome the barrier posed by the valence band offset, a photocurrent will result. Since the $Si_{1-x-y}Ge_xC_y$ is heavily doped, the threshold energy for the onset of photocurrent is E_V - $E_{F(Si_{1-x-y}Ge_xC_y)}$. Since $E_{F(SiGeC)}$ is independent of C concentration, we assume the onset photocurrent will track accurately with ΔE_V.

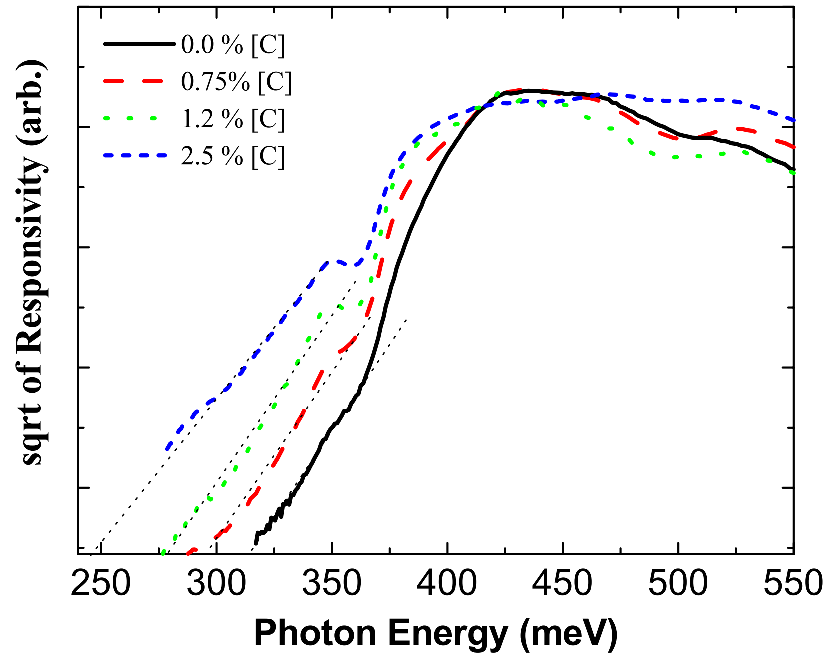


Figure 3.11: Fowler plot of photoresponse curves of p^+ $Si_{1-x-y}Ge_xC_y$ /p^- Si as well as p^+ $Si_{1-x}Ge_x$/ p^- Si. Samples were measured at 4K. The onset of photocurrent decreases as more C is added. The responsivity is defined as photocurrent per absorbed photon.

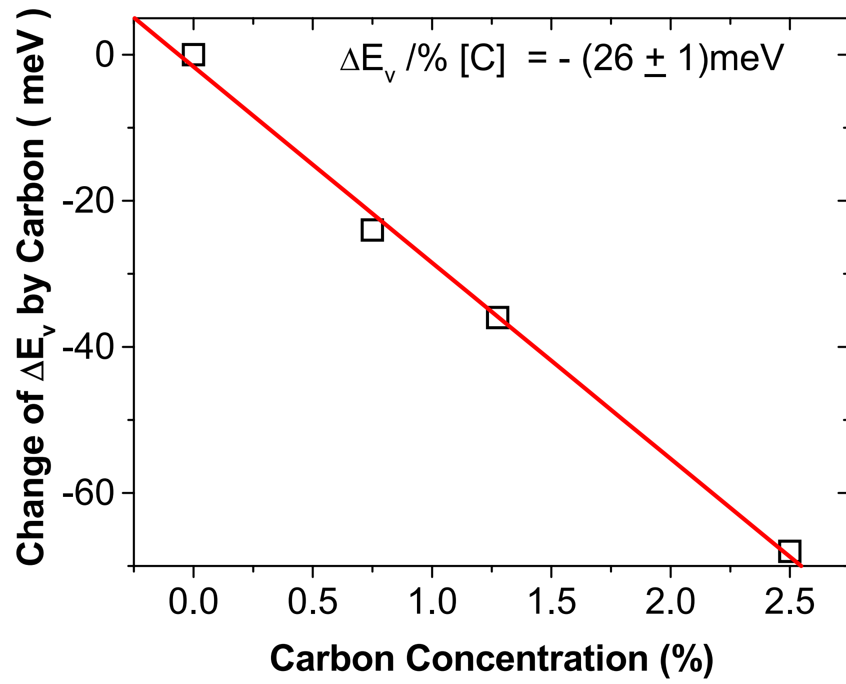


Figure 3.12: Change of ΔE_v of $Si_{1-x-y}Ge_xC_y$ /Si as a function of C concentration obtained by HIP.

Figure 3.11 shows plots of photoresponse curves as a function of photon energy of $Si_{1-x-y}Ge_xC_y/Si$ with different C concentrations. One observes that the onset of photocurrent decreases as C level increases, indicating a decreasing ΔE_V with C. Based on a linear fit as shown in figure 3.11, we obtain the onset energy (from the intercept) for $Si_{0.61}Ge_{0.39}/Si$ of 315 meV. It is observed that C decreases the ΔE_V of $Si_{1-x-y}Ge_xC_y$ / Si by 26±1 meV/%C, as shown in figure 3.12. This is consistent with the values measured by capacitance-voltage in section 3.4, and similar to the increase in bandgap with C. The direct optical measurement concludes again that the increase in bandgap is reflected in the valence band of $Si_{1-x-y}Ge_xC_y$, with very little or no change in the conduction band. Thus little ΔE_c in $Si_{1-x-y}Ge_xC_y$ /Si is expected as in $Si_{1-x}Ge_x/Si$.

3.6 Valence Band Offset of Strained $Si_{1-x-y}Ge_xC_y/Si$ (100) by Admittance Spectroscopy

In this section, we study the valence band offset of $Si_{1-x-y}Ge_xC_y$ /Si by admittance spectroscopy since this technique has previously been applied on $Si/Si_{1-x}Ge_x/Si$ structures to measure the valence band offset of the strained $Si_{1-x}Ge_x/Si$ (100)[8]. This technique has also been applied to band alignment studies on the heterostructures of III-V materials[9]. Our structures were similar to the $Si/Si_{1-x}Ge_x/Si$ quantum well structure in Ref (7), except that Al/Ti Schottky diodes were used instead of pn junctions to provide surface depletion.

Figure 3.13(a) is the band diagram of a typical structure in this study, together with the equivalent circuit in figure 3.13(b). The capacitance C_d corresponds to the depletion region of the metal/Si Schottky junction. G_u and C_u are the conductance and

capacitance of the two $Si/Si_{1-x-y}Ge_xC_y/Si$ junctions in series which are outside of the Schottky barrier depletion region. If we assume the conductance of the heterostructure is ideal, then (G_u) corresponds to the thermionic emission of holes from the $Si_{1-x}Ge_x$ ($Si_{1-x-y}Ge_xC_y$) quantum well and therefore is proportional to $\exp(-\Delta E_V/kT)$.

$$G_u = \alpha T \exp\left(\frac{-\Delta E_V}{kT}\right) \tag{3.4}$$

where α is a constant.[7]

The equivalent circuit can be converted into a capacitance (C_m) in parallel with a conductance (G_m)[10] and C_m and G_m are the experimentally measured values and can be expressed as [11]

$$C_m = \frac{\omega^2 C_u C_d (C_u + C_d) + C_d G_u^2}{G_u^2 + \omega^2 (C_u + C_d)^2} \tag{3.5}$$

$$G_m = \frac{\omega^2 G_u C_u^2}{G_u^2 + \omega^2 (C_u + C_d)^2} \tag{3.6}$$

where ω is the measuring frequency and defined as $\omega = 2\pi f$.

Assuming that C_u and C_d are independent of temperature and knowing G_u is a function of temperature, we know that C_m and G_m are functions of temperature. By plotting C_m and G_m as functions of temperature (T), we expect a step rise in the C_m vs. T curve and a peak in the G_m vs. T curve. At a given measurement frequency, the peak of G_m can be obtained by setting $dG_m/dG_u = 0$. One finds that this occurs at $G_u = \omega(C_u+C_d)$. At a given measurement frequency, this maximum of G_m can be found by varying the temperature to

change G_u, with temperature referred to as T_m at which maximum G_m is found. By combining $G_u = \omega(C_u+C_d)$ at T_m with equation 3.4, we have

$$f = \frac{\alpha T_m \exp(\frac{-\Delta E_V}{kT_m})}{2\pi(C_u + C_d)} \tag{3.7}$$

Thus by plotting the f/T_m as a function of T_m, we can obtain ΔE_V without actual knowledge of C_u and G_u.

Figures 3.14 and 3.15 show the step in the measured capacitance (C_m) and the peak of the measured conductance (G_m) for the $Si/Si_{1-x}Ge_x/Si$ and $Si/Si_{1-x-y}Ge_xC_y/Si$ heterostructures as a function of temperature. Since the emission rate is proportional to $\exp(-\Delta E_V/kT)$, we expect the peak of conductance to occur at higher temperatures for larger excitation frequencies. Given the same excitation frequency, the conductance peak will occur at a lower temperature for a smaller valence band offset. This is indeed the case by comparing Fig. 3.16 and Fig. 3.17. By studying the temperature dependence of capacitance and conductance at different frequencies, the activation energy can be obtained based on equation 3.7, as shown in Fig. 3.16.

Measurements showed a 39 meV reduction in valence band offset for 1.6% C, corresponding to 25 meV/%C, in good agreement with results obtained by capacitance-voltage and HIP techniques. We point out, however, that this method fundamentally assumes that the zero-bias small signal conductance of $Si_{1-x}Ge_x/Si$ (or $Si_{1-xy}Ge_xC_y/Si$) heterojunction scales ideally as $\exp(-\Delta E_V/kT)$. The small signal conductance, like leakage current, can also be dominated by non-ideal local defects. For example, note that the valence band offset of the $Si_{1-x}Ge_x/Si$ with 33% [Ge] obtained by admittance

(a)

(b)

(c)

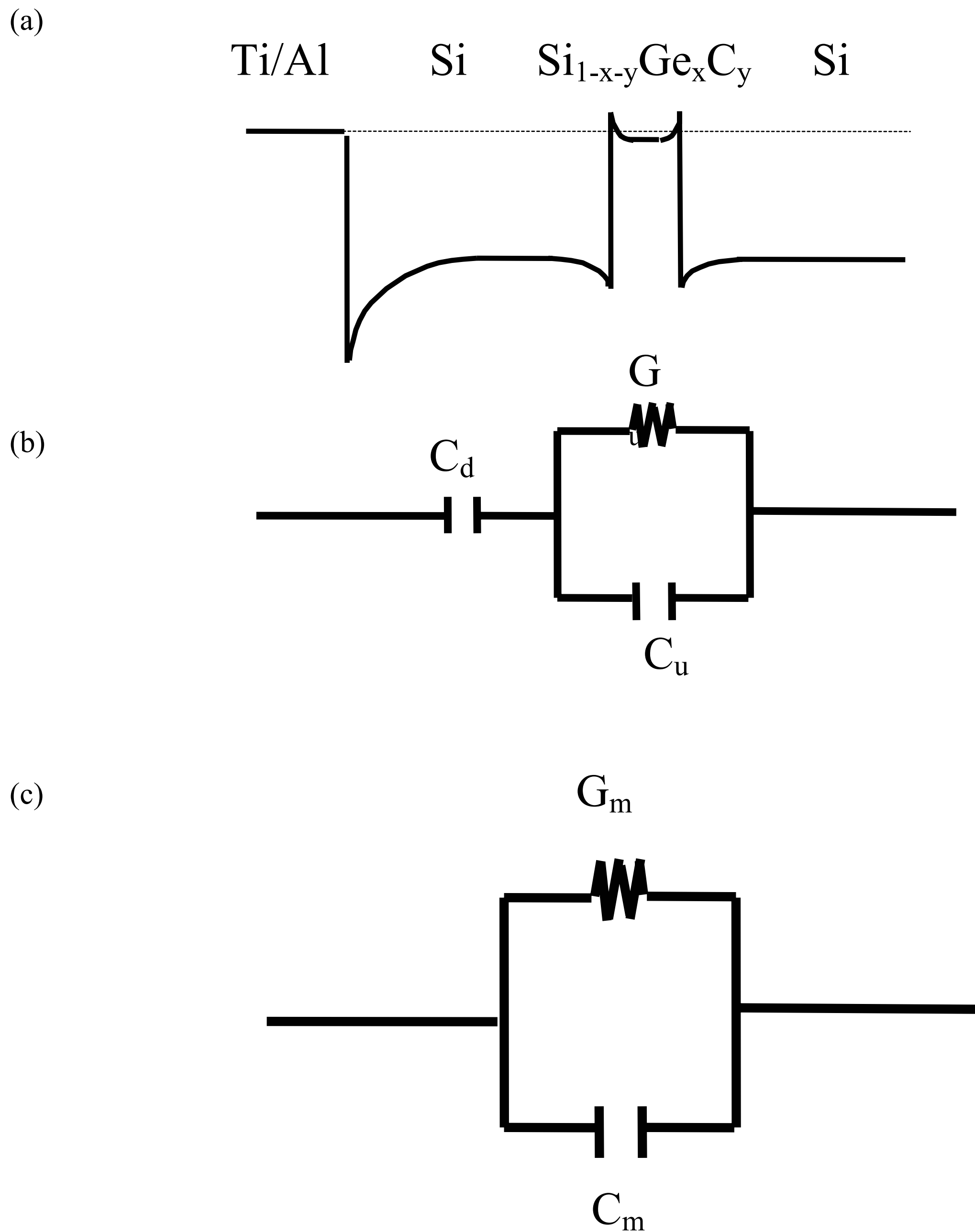


Fig. 3.13: (a) Valence Band Diagram of p-type $Si/Si_{1-x-y}Ge_xC_y/Si$ admittance structure. (b) The equivalent circuit of the admittance structure. (c) The equivalent circuit in which G_m and C_m are experimentally measured.

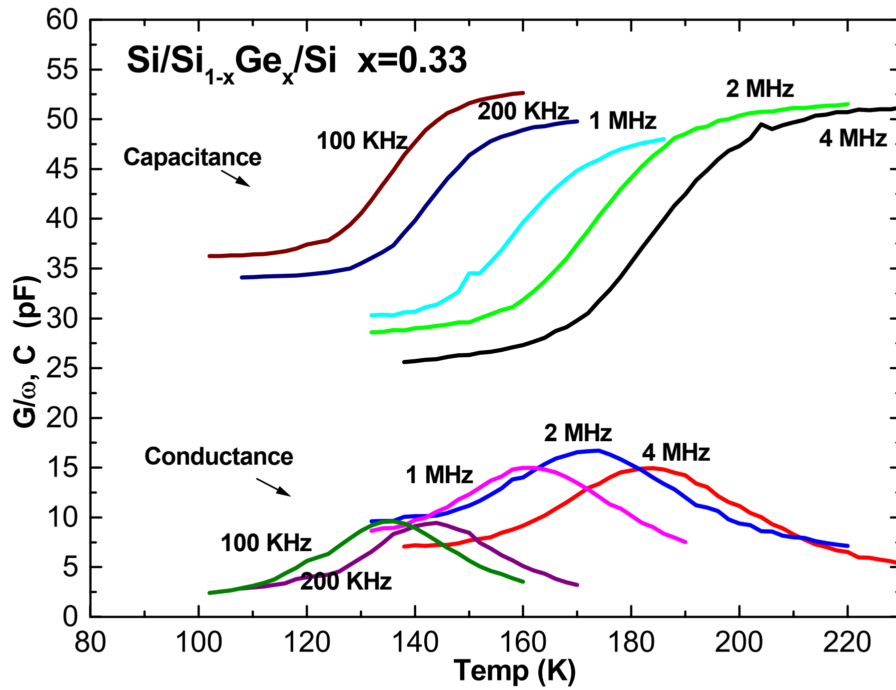


Fig. 3.14: Capacitance (C_m) and conductance (G_m) of the $Si/Si_{1-x}Ge_x/Si$ heterostructure as a function of temperature for various frequencies measured under zero bias condition, with 33% Ge concentration.

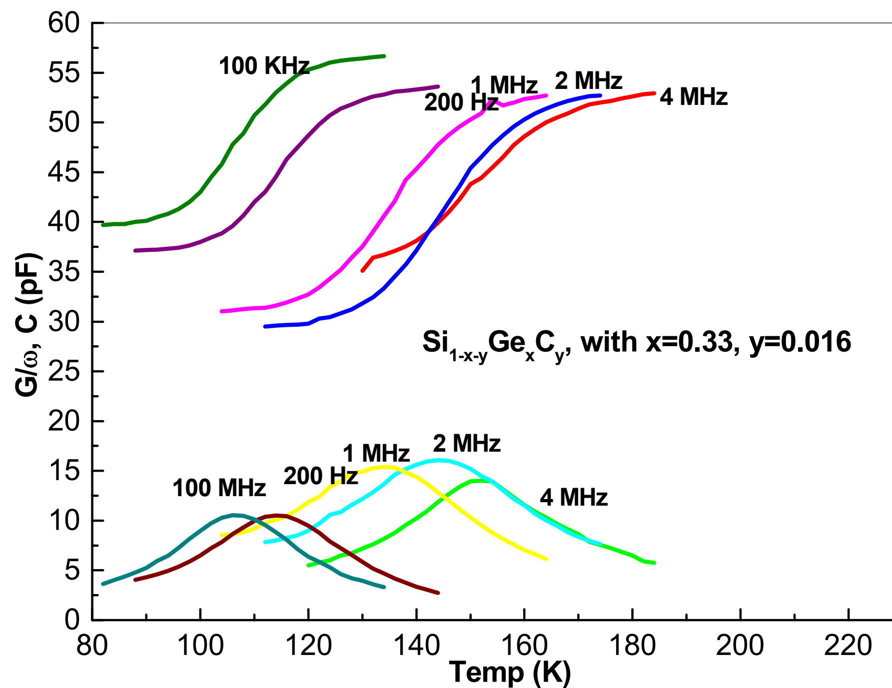


Fig. 3.15: Capacitance (C_m) and conductance (G_m) of the $Si/Si_{1-x-y}Ge_xC_y$ /Si heterostructure as a function of temperature for various frequencies measured under zero bias condition. C content is 1.6% and Ge concentration is 33%.

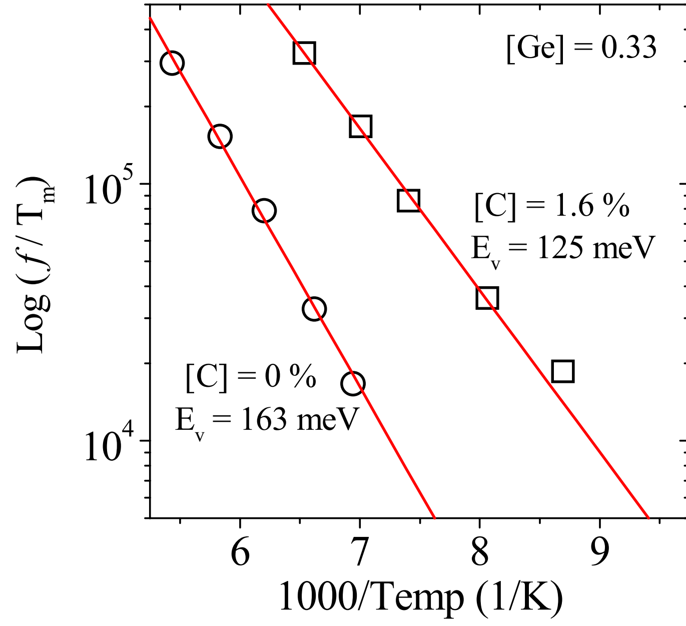


Fig. 3.16: Arrhenius plot of the inverse temperature of the conductance peaks versus measurement frequency.

spectroscopy is only 163 meV, smaller than the widely accepted value for the ΔE_V of the strained $Si_{1-x}Ge_x$ /Si with 33% [Ge] (~250meV). Therefore we feel that the capacitance-voltage and Heterojunction Internal Photoemission techniques are inherently more reliable for band offset measurements.

We mentioned in chapter 2 previous reports on the valence band offset of the strained $Si_{1-x-y}Ge_xC_y$ /Si (100) by different experimental methods. Rim et al, reported that from C-V analysis of $Si_{1-x-y}Ge_xC_y$ based metal-oxide-semiconductor structures[12], C decreased ΔE_v by ~20 meV/%C, in good agreement with our number. X-ray photoelectron spectroscopy showed a negligible effect of C on the valence band offset[13], within an accuracy of ±30 meV. The result confirmed a small effect by C.

On the other hand, recently reported measurements on the ΔE_V of $Si_{1-x-y}Ge_xC_y$ / Si by admittance spectroscopy suggested that C reduced the conduction band offset by ~100 meV/%C, and valence band offsets by ~ 80 meV/%C[14]. One concern with this report is a lack of $Si_{1-x}Ge_x$ control samples for comparison. We have also seen that measurements by admittance spectroscopy can be dominated by non-ideal defects, making this technique less reliable.

In next chapter, we study a p-type modulation doped $Si_{1-x-y}Ge_xC_y$ /Si with a two-dimensional hole gas in the $Si_{1-x-y}Ge_xC_y$ channel. Based on observing a complete carrier transfer from the Si supply layer to a $Si_{0.79}Ge_{0.2}C_{0.01}$, we again confirm that the effect of C on the valence band offset of $Si_{1-x-y}Ge_xC_y$ /Si is small.

3.7 Calculations of Band Alignment of $Si_{1-x}Ge_x$/Si, $Si_{1-x-y}Ge_xC_y$/Si, and $Si_{1-y}C_y$/Si

In the first half of this chapter, we used various methods to measure the valence band offset of compressively strained $Si_{1-x-y}Ge_xC_y$ /Si (100). We found that the net effect of C is to reduce the valence band offset of $Si_{1-x-y}Ge_xC_y$ by 20-29 meV/%C. In this section, we attempt to present a unified picture in which the effect of Ge, C, and strain will be incorporated.

We first note that when Ge or C is added to Si, the change in bandgap (or band offset) of the resulting pesudomorphic layer on the Si (100) can be attributed to two factors. First there is an intrinsic effect (chemical effect) due to the addition of Ge or C. The second effect comes from the introduced strain. For example, strain-free $Si_{1-x}Ge_x$ has a smaller bandgap than that of Si due to the intrinsic effect of Ge. The bandgap is even smaller when the same $Si_{1-x}Ge_x$ is under biaxial compressive strain due to the effect of strain. Our goal is therefore to quantitatively determine how strain and intrinsic effects affect the band alignment due to the addition of C and Ge.

The structure of this section is organized as follows. We first make definitions, assumptions and notations used in this section. We then review the band alignment of strained $Si_{1-x}Ge_x$/Si, considering both the intrinsic and strain effect due to the addition of Ge. The band alignment of strained $Si_{1-x-y}Ge_xC_y$/Si is then investigated. Finally, we will combine both the stain and intrinsic effects of Ge and C to predict the band alignments of tensile-strained $Si_{1-y}C_y$/Si and $Si_{1-x-y}Ge_xC_y$/Si and strain-free $Si_{1-x-y}Ge_xC_y$/Si.

3.7.1 Assumptions and Definitions

(1) We assume that all materials ($Si_{1-x}Ge_x$, $Si_{1-y}C_y$, $Si_{1-x-y}Ge_xC_y$) have Si-like band structures. There are six minima in the conduction band along [001], [010], [100] directions and there are heavy hole (HH), light hole (LH) and spin-orbit (SO) bands in the valence bands.

(2) We assume that the effect on the band alignment can be independently broken into a strain effect, a Ge intrinsic effect, and a C intrinsic effect.

(3) We assume shifts of energies are linear in composition.

(4) We use the deformation potential and elastic constants of Si (as discussed below) to calculate the strain effect due to C incorporation in $Si_{1-y}C_y$. We expect no significant error since the amount of C addition is small. In theory we could use the linearly interpolated deformation potential and elastic constants between Si and Ge in calculating strain effect on compressive-strained $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$. But since calculations are kept only the first order in x, this leads to effectively only assuming Si deformation potentials.

(5) We define ΔE_C as the effect on the lower edge of conduction band from that of unstrained Si.

$\Delta E_C = \Delta E_C$ (strain) $+ \Delta E_C$ (intrinsic C) $+ \Delta E_C$ (intrinsic Ge).

ΔE_C (strain) is the strain effect on the conduction band offset; ΔE_C (intrinsic C) is the intrinsic effect of C on the conduction band offset, and ΔE_C (intrinsic Ge) is the intrinsic effect of Ge on the conduction band offset.

(6) We define ΔE_V as effect on the upper edge of valence band from that of unstrained Si.

$\Delta E_V = \Delta E_V$ (strain) $+ \Delta E_V$ (intrinsic C) $+ \Delta E_V$ (intrinsic Ge).

Where ΔE_V (strain) is the strain effect on the valence band offset; ΔE_V (intrinsic C) is the intrinsic effect of C on the valence band offset, and ΔE_V (intrinsic Ge) is the intrinsic effect of Ge on the valence band offset.

(7) We define $\Delta E_C < 0$ and $\Delta E_V > 0$ for type I offset to unstrained Si. In other word, ΔE_C is negative when the conduction band is shifted down with respect to that of Si. ΔE_V is positive when the valence band is shifted up with respect to that of Si.

(7) We define ΔE_g as the bandgap change from unstrained Si.

$\Delta E_g = \Delta E_C - \Delta E_V$. Note that ΔE_g is negative when the alloy has a gap less than that of bulk silicon.

(8) We define notations used in this section.

(8*a*) $E_{V,av}$: the (weighted) average of the valence bands.

(8*b*) $E_{C,av}$: the (weighted) average of the conduction bands.

(8*c*) $E_{V,hh}$: the heavy hole band.

(8*d*) $E_{V,lh}$: the light hole band.

(8*e*) $E_{C,\Delta 2}$: The two degenerate valleys of the conduction bands.

(8*f*) $E_{C,\Delta 4}$: The four degenerate valleys of the conduction bands.

(8*g*) Δ_o: shift of valence bands due to spin-orbital coupling.

(8*h*) A_V: hydrostatic deformation potential, used in calculating shifts in the weighted average of valence bands due to hydrostatic strain (change in volume).

(8*i*) A_C: hydrostatic deformation potential, used in calculating shifts in the weighted average of conduction bands due to hydrostatic strain (change in volume).

(8*j*) D_V: uniaxial deformation potential, used in calculating the valence band shifts with respect to the weighted average of the valence bands caused by uniaxial strain (change in shape), with strain in (100)-like directions.

(8*k*) D_C: uniaxial deformation potential, used in calculating the conduction band shifts with respect to the weighted average of the conduction bands caused by uniaxial stress (change in shape).

(8*l*) $\Delta E_{V,hh}(*/Si) = E_{V,hh}(*/Si) - E_{V,hh}(Si)$, where * is the epitaxial material on an unstrained Si substrate. Note that $E_{V,hh}(Si)$ is topmost valence band of Si and Si is always unstrained in our case.

(8*m*) $\Delta E_{V,lh}(*/Si) = E_{V,lh}(*/Si) - E_{V,hh}(Si)$, where * is the epitaxial material. Note that light-hole and heavy-hole bands are degenerate in unstrained Si.

(8*n*) $\Delta E_{C,\Delta 2}(*/Si) = E_{C,\Delta 2}(*/Si) - E_{C,av}(Si)$, where * is the epitaxial material. Note that there is no conduction band splitting in unstrained Si.

(8*o*) $\Delta E_{C,\Delta 4}(*/Si) = E_{C,\Delta 4}(*/Si) - E_{C,av}(Si)$, where * is the epitaxial material.

(9) We define the in-plane and out-of-plane lattice strain of the epitaxial film as:

$$\varepsilon_{//} = \frac{a_{Si} - a_*^{relaxed}}{a_*^{relaxed}} \sim \frac{a_{Si} - a_*^{relaxed}}{a_{Si}} \sim -0.042(x - 8.3y),$$

where $a_*^{relaxed}$ is the relaxed lattice constant of the epitaxial materials ($Si_{1-x}Ge_x$, $Si_{1-x-y}Ge_xC_y$, or $Si_{1-y}C_y$) . This simply assumes 8.3 C atoms compensate the strain of one Ge atom, and strain vs. atomic concentration is linear.

$$\varepsilon_{\perp} = -2\frac{C_{12}}{C_{11}}\varepsilon_{//} \sim 0.032(x - 8.3y),$$

where C_{11}, C_{12} are the elastic constants of Si. Table 3.1 lists the values of parameters used in calculating the band alignment.

3.7.2 Band Alignment of compressive strained $Si_{1-x}Ge_x$/Si

In this section, we review the theoretical and experimental work in determining the band alignment of compressively strained $Si_{1-x}Ge_x$/Si.

3.7.2(A): Intrinsic effect of Ge on the band alignment of $Si_{1-x}Ge_x$/Si

We review the intrinsic of Ge on the band alignment of $Si_{1-x}Ge_x$/Si based on the Van de Walle's 'model solid theory'[17]. According to the theory, we have

$E_{V,av}$ (unstrained Ge) = -6.35 eV, (3.8)

$E_{V,av}$ (unstrained Si) = -7.03 eV, (3.9)

As a result, we have

$E_{V,av}$ (unstrained $Si_{1-x}Ge_x$) = -7.03(1-x) – 6.35x (eV). (3.10)

Since the heavy-hole band and light-hole band of unstrained Si and $Si_{1-x}Ge_x$ are shifted up by 1/3 Δ_o from the average bands due to spin-orbital spltting, we have

$$E_{V,HH}\text{ (unstrained }Si_{1-x}Ge_x) = E_{V,av}(\text{unstrained }Si_{1-x}Ge_x) + 1/3\Delta_o(\text{unstrained }Si_{1-x}Ge_x)$$

$$= -7.02 + 0.77x \text{ (eV)} \quad (3.11)$$

$$E_{V,HH}\text{ (unstrained Si)} = E_{V,av}\text{ (Si)} + 1/3\ \Delta_o = -7.02 \text{ (eV)}. \quad (3.12)$$

Therefore, we determine the intrinsic effect of Ge on the valence band offset of $Si_{1-x}Ge_x$/Si as

$$\Delta E_V\text{ (intrinsic Ge)} = E_{V,HH}\text{ (unstrained }Si_{1-x}Ge_x) - E_{V,HH}\text{ (Si)} = 0.77x \text{ (eV)}. \quad (3.13)$$

To calculate the intrinsic effect of Ge on the conduction band offset of $Si_{1-x}Ge_x$/Si, we first note that, since there is no spin-orbital effect on the conduction band, we have

$$E_{C,av}\text{ (Si)} = E_{C,\Delta 2}\text{ (Si)} = E_{C,\Delta 4}\text{ (Si)}. \quad (3.14)$$

$$E_{C,av}\text{ (unstrained }Si_{1-x}Ge_x) = E_{C,\Delta 2}(\text{unstrained }Si_{1-x}Ge_x) = E_{C,\Delta 4}\text{ (unstrained }Si_{1-x}Ge_x). \quad (3.15)$$

The intrinsic effect of Ge on the conduction band offset of $Si_{1-x}Ge_x$/Si is indirectly derived by first observing that

$$\Delta E_C\text{ (intrinsic Ge)} = \Delta E_g\text{ (intrinsic Ge)} + \Delta E_V\text{ (intrinsic Ge)}$$

$$= \Delta E_g\text{ (intrinsic Ge)} + 0.77x \text{ (eV)}. \quad (3.16)$$

ΔE_g (intrinsic Ge) was obtained experimentally from the measured bandgap of unstrained $Si_{1-x}Ge_x$ as a function of Ge content. Although the change in bandgap of unstrained $Si_{1-x}Ge_x$ is not a linear function of Ge, it is close to linear for up to 40%Ge. Based on a fit[15] to the experimental data obtained by Braunstein et al[16] on relaxed $Si_{1-x}Ge_x$, we observed that Ge decreases the bandgap of relaxed $Si_{1-x}Ge_x$ by ~ 4.0 meV/%Ge for up to 40%Ge. Thus we have

$$\Delta E_g\text{ (intrinsic Ge)} = -0.40x \text{ (eV)}. \quad (3.17)$$

Properties	**Si**	**Ge**
Elastic constants	C_{11} = 165 GPa C_{12}= 64 GPa	C_{11} = 128 GPa C_{12}= 48 GPa
Δ_o	0.04 eV	0.3 eV
A_V	2.46 eV	1.24 eV
A_C	4.18 eV	2.55 eV
D_V	-2.35 eV	-2.55 eV
D_C	9.16 eV	9.42 eV

Table 3.1: Values of parameters used in the band structures calculation. Elastic constants are based on reference (22) in chapter 2. The rest of numbers are based on reference (19).

As a result, we have

$$\Delta E_C \text{(intrinsic Ge)} = 0.37x \text{ (eV)}. \qquad (3.18)$$

3.7.2(B): Strain effect due Ge incorporation on the band alignment of compressively strained $Si_{1-x}Ge_x$/Si

Strain-induced conduction and valence band shifts are described based on the deformation potential[17], which is the straightforward derivative of the energies with respect to strain. The concept of the deformation potential was introduced in 1950 by Bardeen and Shockley[18]and has since been used to calculate strain-induced shifts in the conduction and valence bands.

If a pseudopomorphic Si film is grown on a Si (100) substrate with the addition of Ge, the film is under a biaxial stress perpendicular to the growth direction. As a result, the six-fold degeneracy of the conduction band is lifted. The bands along [100] and [010] (Δ_4) split off from the one along [001] (Δ_2). Similarly, the two-fold degeneracy (HH and LH band) of the valence band is lifted.

In addition, the biaxial stress introduces a volume change of the material. As a result, there is a shift in the average position of the valence band ($\Delta E_{V,av}$) and conduction band ($\Delta E_{C,av}$).

By combining both the shift of bands due to change in volume and splitting of bands due to change in shape, we have

$$\Delta E_{C,\Delta 4} \text{(strain due to Ge)}$$

$$= E_{C,\Delta 4} \text{(strained } Si_{1-x}Ge_x) - E_{C,\Delta 4}\text{(unstrained } Si_{1-x}Ge_x)$$

$$= E_{C,\Delta 4} \text{(strained } Si_{1-x}Ge_x) - E_{C,av}\text{(unstrained } Si_{1-x}Ge_x) \qquad \text{(from 3.15)}$$

$= [E_{C,\Delta 4}$ (strained $Si_{1-x}Ge_x$) – $E_{C,av}$(strained $Si_{1-x}Ge_x$)] + [$E_{C,av}$(strained $Si_{1-x}Ge_x$) – $E_{C,av}$(unstrained $Si_{1-x}Ge_x$)],

where the first term is due to change in shape, and the second term is due to change in volume,

$$= \frac{-1}{3} D_C(\varepsilon_\perp - \varepsilon_{//}) + A_C(\varepsilon_\perp + 2\varepsilon_{//})$$

$$= -0.44x. \quad (3.19)$$

Similarly, we have

$\Delta E_{C,\Delta 2}$ (strain due to Ge)

$$= \frac{2}{3} D_C(\varepsilon_\perp - \varepsilon_{//}) + A_C(\varepsilon_\perp + 2\varepsilon_{//})$$

$$= 0.25x. \quad (3.20)$$

As for the strain-induced change in the valence band offsets of strained $Si_{1-x}Ge_x$/Si, we have

$\Delta E_{V,HH}$ (strain of Ge)

$= E_{V,HH}$ (strained $Si_{1-x}Ge_x$) – $E_{V,HH}$(unstrained $Si_{1-x}Ge_x$)

$= E_{V,HH}$ (strained $Si_{1-x}Ge_x$) – [$E_{V,av}$(unstrained $Si_{1-x}Ge_x$) + $\frac{1}{3}\Delta_o$ ($Si_{1-x}Ge_x$)]

$= [E_{V,HH}$ (strained $Si_{1-x}Ge_x$) – $E_{V,av}$(strained $Si_{1-x}Ge_x$)] + [$E_{V,av}$(strained $Si_{1-x}Ge_x$) – $E_{V,av}$(unstrained $Si_{1-x}Ge_x$)] - $\frac{1}{3}\Delta_o$ ($Si_{1-x}Ge_x$)

$$= [\frac{1}{3}\Delta_o - D_V(\varepsilon_\perp - \varepsilon_{//})] + A_V(\varepsilon_\perp + 2\varepsilon_{//}) - \frac{1}{3}\Delta_o \ (Si_{1-x}Ge_x)$$

$$= 0.04x, \quad (3.21)$$

and

$\Delta E_{V,LH}$ (strain of Ge)

$$= [\frac{-1}{6}\Delta_o + \frac{1}{4}\Xi + \frac{1}{2}(\frac{9}{4}\Xi^2 + \Delta_o^2 + \Xi\Lambda)^{1/2}] + A_V(\varepsilon_\perp + 2\varepsilon_{//}) - \frac{1}{3}\Delta_o(Si_{1-x}Ge_x)$$

$$= -0.02 - 0.34x + .5(.0016 + 0.007x + 0.25x^2)^{1/2} \quad (3.22)$$

,where D_C, D_V, A_C, A_V are the deformation potentials used in calculating energy shifts due to band split and hydrostatic strain (volume change), $\varepsilon_\perp$ and $\varepsilon_{//}$ are the out-of-plane strain and in-plane strain, respectively. $\Xi = 2D_V(\varepsilon_\perp - \varepsilon_{//})$. Δ_o is the energy associated with spin-orbit splitting. All numbers of the parameters in the equation above are from table 3.1[19].

Table 3.2 summarizes the strain and intrinsic effect Ge on the band alignment of compressively strained $Si_{1-x}Ge_x$/Si.

3.7.3 Band Alignment of compressive strained $Si_{1-x-y}Ge_xC_y$/Si

In this section, we aim to investigate the effect of C incorporation on the band alignment of compressively strained $Si_{1-x-y}Ge_xC_y$/Si.

We first calculate the strain effect, using the same method in 3.7.2. Based on the reported experimental data of the total C effect on the bandgap of compressively strained $Si_{1-x-y}Ge_xC_y$, we then extract the intrinsic effect of C on the bandgap by substracting the strain effect of C (from calculation) from the total effect of C (from experimental data).

Once the intrinsic effect of C on the bandgap of compressively strained $Si_{1-x-y}Ge_xC_y$ is obtained, we then investigate the intrinsic effect of C on both the conduction band offset and valence band offset of compressively strained $Si_{1-x-y}Ge_xC_y$/Si.

The intrinsic effect of C on the valence band offset of compressively strained $Si_{1-x-y}Ge_xC_y$/Si is obtained by substracting the strain effect of C (from calculation) from the

	Strain effect (Ge)	Intrinsic effect (Ge)	Total effect (Ge)
$\Delta E_{C,\Delta 4}$	-0.44x	0.37x	-0.07x
$\Delta E_{C,\Delta 2}$	0.25x	0.37x	0.62x
ΔE_C (lower edge)	-0.44x	0.37x	-0.07x
$\Delta E_{V,HH}$	0.04x	0.77x	0.81x
$\Delta E_{V,LH}$	( )	0.77x	( ) + 0.77x
ΔE_V (higher edge)	0.04x	0.77x	0.81x
ΔE_G	-0.48x	-0.40x	-0.88x

Unit: eV
( ) = $-0.02 - 0.34x + .5(.0016+0.007x+0.25x^2)^{1/2}$
Commonly used terms:
$(\varepsilon_\perp - \varepsilon_{//})$ = 0.074x,
$(\varepsilon_\perp + 2\varepsilon_{//})$ = -0.052x,
$\Xi = 2D_V(\varepsilon_\perp - \varepsilon_{//}) \sim -0.34x$
$A_C(\varepsilon_\perp + 2\varepsilon_{//}) \sim -0.21x$
$A_V(\varepsilon_\perp + 2\varepsilon_{//}) \sim -0.13x$
Δ_o ($Si_{1-x}Ge_x$) = 0.04 + 0.26x			

Table 3.2: Effect of Ge incorporation on the band structure of compressive-strained $Si_{1-x}Ge_x$/Si and band alignment of $Si_{1-x}Ge_x$/Si. Note that during the calculation, all terms involving x^2 were neglected.

experimental results of the total effect of C on the valence band offset of compressively strained $Si_{1-x-y}Ge_xC_y/Si$. By combining both the intrinsic effect of C on the bandgap of compressively strained $Si_{1-x-y}Ge_xC_y$ and the intrinsic effect of C on the valence band offset of the compressively strained $Si_{1-x-y}Ge_xC_y/Si$, we deduct the intrinsic effect of C on the conduction band offset of the compressivley strained $Si_{1-x-y}Ge_xC_y/Si$

3.7.3(A): Strain effect due Ge and C incorporation on the band alignment of compressively strained $Si_{1-x-y}Ge_xC_y/Si$

The strain effect due Ge and C incorporation on the band alignment of compressively strained $Si_{1-x-y}Ge_xC_y/Si$ can be calculated based on the same method used in 3.7.2 to calculate strain effect in $Si_{1-x}Ge_x$ by simply substituting (x-8.3y) for x. The results are summarized as follows.

$$\Delta E_{C,\Delta 2}\text{(strain due to Ge, C)} = \frac{2}{3} D_C(\varepsilon_\perp - \varepsilon_{//}) + A_C(\varepsilon_\perp + 2\varepsilon_{//}) = 0.25\ (x-8.3y) \qquad (3.23)$$

$$\Delta E_{C,\Delta 4}\text{(strain due to Ge, C)} = \frac{-1}{3} D_C(\varepsilon_\perp - \varepsilon_{//}) + A_C(\varepsilon_\perp + 2\varepsilon_{//}) = -0.44\ (x-8.3y) \qquad (3.24)$$

$$\Delta E_{V,HH}\text{(strain due to Ge, C)} = [\frac{1}{3}\Delta_o - D_V(\varepsilon_\perp - \varepsilon_{//})] + A_V(\varepsilon_\perp + 2\varepsilon_{//}) - \frac{1}{3}\Delta_o\ (Si_{1-x-y}Ge_xC_y)$$

$$= 0.04\ (x-8.3y) \qquad (3.25)$$

$$\Delta E_{V,LH}\text{(strain due to Ge, C)} = [\frac{-1}{6}\Delta_o + \frac{1}{4}\Xi + \frac{1}{2}(\frac{9}{4}\Xi^2 + \Delta_o^2 + \Xi\Lambda)^{1/2}] + A_V(\varepsilon_\perp + 2\varepsilon_{//})$$

$$- 1/3\ \Delta_o\ (Si_{1-x-y}Ge_xC_y)$$

$$= -0.02 - 0.34(x-8.3y) + .5[.0016+0.007(x-8.3y)+0.25(x-8.3y)^2]^{1/2} - 1/3\ \Delta_o\ (Si_{1-x-y}Ge_xC_y) \qquad (3.26)$$

The results are tabulated in the first column of table 3.3.

3.7.3(B): Intrinsic effect C on the band alignment of compressively strained $Si_{1-x-y}Ge_xC_y/Si$

To further complete table 3.3, we need data on the intrinsic effect of C on bandgap of $Si_{1-x-y}Ge_xC_y$ and band offsets of $Si_{1-x-y}Ge_xC_y/Si$, which has to date not been available. Thus we will use experimental data to extract these values so that table 3.3 can be completed.

We observe from the first column in table 3.3 that

$$\Delta E_{C,\Delta 4}\text{ (strain due to Ge, C)} = -0.44\,(x-8.3y), \tag{3.27}$$

$$\Delta E_{V,HH}\text{ (strain due to Ge, C)} = 0.04\,(x-8.3y), \tag{3.28}$$

$$\Delta E_g\text{ (strain due to Ge, C)} = -0.48\,(x-8.3y). \tag{3.29}$$

Therefore the strain effect due to C only is

$$\Delta E_{C,\Delta 4}\text{ (strain due to C)} = -0.44\,(-8.3y) \sim 3.7y, \tag{3.30}$$

$$\Delta E_{V,HH}\text{ (strain due to C)} = 0.04\,(x-8.3y) \sim -0.3y, \tag{3.31}$$

$$\Delta E_g\text{ (strain due to C)} = -0.48\,(x-8.3y) \sim 4.8y. \tag{3.32}$$

We observe that the strain effect of adding 1% C increases the conduction band offset by ~37 meV and decreases the valence band offset by ~3 meV. As a result, the strain effect of adding 1% C increases the bandgap of compressively strained $Si_{1-x-y}Ge_xC_y$ by ~40 meV.

We mentioned in chapter 2 that, based on the result of PL on the compressively strained $Si_{1-x-y}Ge_xC_y$, 1% C increased the band gap by ~21 meV/%C. Since

$$\Delta E_g\text{ (total effect of C)} = \Delta E_g\text{ (strain effect due to C)} + \Delta E_g\text{ (intrinsic effect of C)},$$

we have

$$\Delta E_g \text{ (intrinsic effect of C)} = \Delta E_g \text{ (total effect of C)} - \Delta E_g \text{ (strain effect due to C)}$$

$$= 21\text{meV/\%C (data)} - 40 \text{ meV/\%C (calculation)}$$

$$= -19 \text{ meV/\%C}$$

As a result, we deduct that the intrinsic effect of C is to decrease the bandgap by ~ -19 meV/%C, consistent with recent reports on the intrinsic effect of C on the bandgap (see reference 26, 29 in chapter 2).

The intrinsic effect of C on the band alignment of compressively strained $Si_{1-x-y}Ge_xC_y/Si$ can also be determined. Following a similar approach, we have

$$\Delta E_{V,HH} \text{ (total effect of C)} = \Delta E_{V,HH} \text{ (intrinsic C)} + \Delta E_{V,HH} \text{ (strain due to C)}.$$

The total effect of C on the valence band offset of the compressively strained $Si_{1-x-y}Ge_xC_y/Si$ was found experimentally in the first half of this chapter. There we found that 1% C decreased the valence band offset of compressively strained $Si_{1-x-y}Ge_xC_y/Si$ by ~26 meV (based on the optical measurement), i.e.

$$\Delta E_{V,HH} \text{ (experimental obtained total effect of C)} = -26 \text{ meV/\%C}.$$

Since the calculated strain effect of adding 1% C is to decrease the valence band offset by ~3 meV(from equation 3.31), we have

$$\Delta E_{V,HH} \text{ (intrinsic C)} = \Delta E_{V,HH} \text{ (total effect of C)} - \Delta E_g \text{ (strain due to C)}$$

$$= -26 \text{ meV/\%C} - (-3 \text{ meV/\%C})$$

$$= 23 \text{ meV/\%C}. \qquad (3.33)$$

Thus the intrinsic effect of 1% C is to decrease the valence band offset (lower the HH band of strained $Si_{1-x-y}Ge_xC_y$) by ~23 meV.

Combining both the intrinsic effect of C on the bandgap and valence band offset, we deduct that the intrinsic effect of C is to increase the conduction band offset (lower the Δ_4 band of $Si_{1-x-y}Ge_xC_y$) by ~ 42 meV, i.e.

$$\begin{aligned}\Delta E_{C,\Delta 4}\text{(intrinsic C)} &= \Delta E_g\text{(intrinsic C)} + \Delta E_{V,HH}\text{(intrinsic C)}\\ &= 19\text{meV/\%C} + 23\text{ meV/\%C}\\ &= 42\text{ meV/\%C.}\end{aligned} \tag{3.34}$$

It is then straightforward to work out the rest of table 3.3. Table 3.3 summarizes both the strain and intrinsic of Ge and C on the band structure of compressively strained $Si_{1-x-y}Ge_xC_y$. Figure 3.19 shows the conduction and valence band energy of the compressively strained $Si_{1-x}Ge_x$ (solid lines) and $Si_{1-0.4-y}Ge_{0.4}C_y$ (dashed lines). One sees that, for compressively strained $Si_{1-x-y}Ge_xC_y$/Si and $Si_{1-x}Ge_x$/Si, most of the bandgap difference is valence band offset.

3.7.4 Band Alignment of tensile-strained $Si_{1-y}C_y$/Si and $Si_{1-x-y}Ge_xC_y$/Si

We have learned both the strain and intrinsic effect of adding C and Ge on the band alignment of $Si_{1-x-y}Ge_xC_y$/Si. In this section, we will apply the numbers to predict the band alignment of $Si_{1-y}C_y$/Si and compare it with reported experimental results. We will also predict the band alignment of tensile-strained $Si_{1-x-y}Ge_xC_y$/Si.

The calculation of the band alignment of tensile-strained $Si_{1-x-y}Ge_xC_y$/Si and $Si_{1-y}C_y$/Si is similar to that in section 3.7.3. However, since $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ are tensile-strained in this case, the lower edge of the conduction band is Δ_2 band and the higher edge of the valence band is LH band.

	Strain effect (Ge, C)	Intrinsic effect (Ge, C)	Total effect (Ge, C)
$\Delta E_{C,\Delta 4}$	-0.44 (x-8.3y)	0.37x - 4.2y	-0.07x – 0.5y
$\Delta E_{C,\Delta 2}$	0.25 (x-8.3y)	0.37x – 4.2y	0.62x – 6.3y
ΔE_C (lower edge)	-0.44 (x-8.3y)	0.37x – 4.2y	-0.07x –0.5y
$\Delta E_{V,HH}$	0.04 (x-8.3y)	0.77x - 2.3y	0.81x – 2.6y
$\Delta E_{V,LH}$	( )	0.77x - 2.3y	( ) + 0.77x –2.3y
ΔE_V(higher edge)	0.04 (x-8.3y)	0.77x - 2.3y	0.81x – 2.6y
ΔE_G	-0.48 (x-8.3y)	-0.4x – 1.9y	-0.88x + 2.1y

Unit: eV.
For compressive $Si_{1-x-y}Ge_xC_y$, x > 8.3y
( ) = -0.02 - 0.34(x-8.3y) + .5[.0016+0.007(x-8.3y)+0.25(x-8.3y)^2]$^{1/2}$
Commonly used terms:
$(\varepsilon_\perp - \varepsilon_{//})$ = 0.074(x-8.3y),
$(\varepsilon_\perp + 2\varepsilon_{//})$ = -0.052(x-8.3y),
$\Xi = 2D_V(\varepsilon_\perp - \varepsilon_{//}) \sim$ -0.34(x-8.3y)
$A_C(\varepsilon_\perp + 2\varepsilon_{//}) \sim$ -0.21(x-8.3y)
$A_V(\varepsilon_\perp + 2\varepsilon_{//}) \sim$ -0.13(x-8.3y)
Δ_o = 0.04 + 0.26x

Table 3.3: Effect of Ge and C incorporation on the band structure compressive-strained $Si_{1-x-y}Ge_xC_y$ and band alignment of $Si_{1-x-y}Ge_xC_y$/Si. Note that the total effects of C on the bandgap and valence band offset are experimentally obtained. The strain effect due to C is from calculation based on "model solid theory". By combining the experimental data and calculation, we obtain the intrinsic effect of C on the bandgap and band offsets.

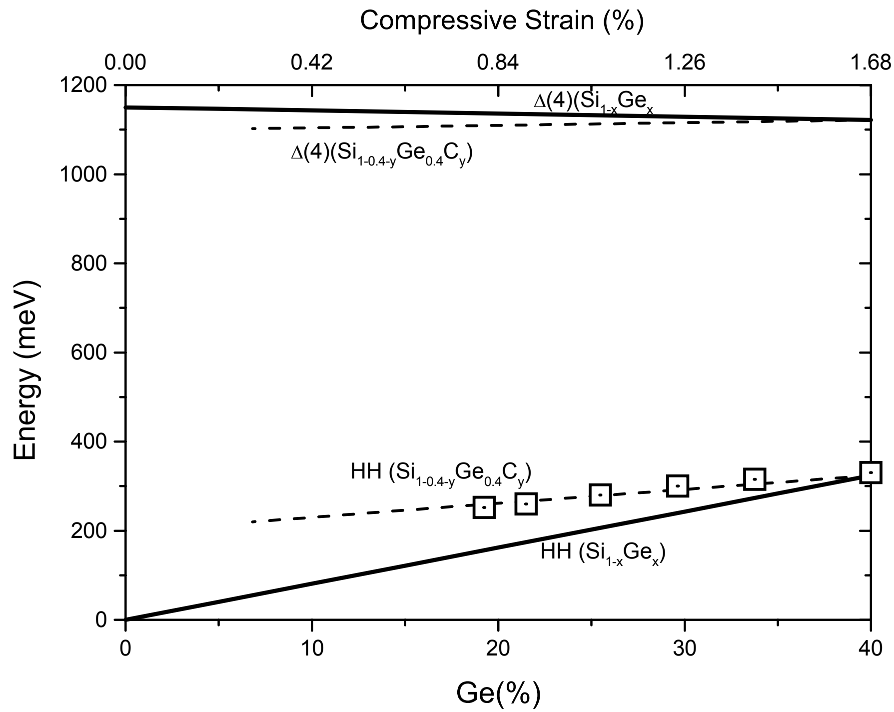


Figure 3.17: The conduction and valence band energy of the compressively strained $Si_{1-x}Ge_x$ (solid lines) and $Si_{1-0.4-y}Ge_{0.4}C_y$ (dashed lines). The lower axis is Ge content and the upper axis is the corresponding strain. All energies are referred to the valence band energy of Si. Dot-centered symbols are data points obtained by C-V measurement for $Si_{1-x-y}Ge_xC_y$ with 39.5% Ge and up to 2.5% C in section 3.4. In this case, only the upper axis is relevant.

Table 3.4 summarizes both the strain and intrinsic of Ge and C on the band structures of tensile-strained $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$. First using parameters derived in the previous section for compressively strained $Si_{1-x-y}Ge_xC_y$, we predict that the total effect of adding 1% C into $Si_{1-y}C_y$ is to increase the conduction band offset of $Si_{1-y}C_y$/Si by 63 meV/%C. It was recently reported, based on a least-square fit to the MOS data, that C lowered the conduction band offset of tensile-strained $Si_{1-y}C_y$/Si by ~57 meV/%C[20], consistent with our prediction. It is also consistent with the estimate, based on the measurement of modulation doped Si/$Si_{1-y}C_y$/Si, that C increased the conduction band offset of $Si_{1-y}C_y$/Si by ~75 meV/%C[21].

Recent studies showed that the addition of C reduced the bandgap of tensile-strained $Si_{1-y}C_y$ by ~66 meV/%C[22]. Our calculation shows that, even though the change in LH band is not a linear function of C concentration, the strain effect of C increases the band offset by ~34 meV/%C. Combining both the strain and intrinsic effect of C, we predict that the valence band offset of $Si_{1-y}C_y$ /Si is ~ 11 meV/%C. As a result, the bandgap change of $Si_{1-y}C_y$ with C is expected to be ~74 meV/%C, consistent with the reported experimental result.

Figure 3.20 plots the conduction and valence band energy of the tensile-strained $Si_{1-y}C_y$ (solid lines) and $Si_{1-x-.05}Ge_xC_{.05}$ (dashed lines). For $Si_{1-y}C_y$/Si, most of the band offset is in the conduction band. When Ge is added into $Si_{1-x-.05}Ge_xC_{.05}$, the conduction band offset is reduced due to (1) offsetting intrinsic effect of Ge and C, and (2) reduced strained effect. The valence band offset of $Si_{1-x-.05}Ge_xC_{.05}$/Si begins to increase when Ge is added, which is largely attributed to the intrinsic effect of Ge.

	Strain effect (Ge, C)	Intrinsic effect (Ge, C)	Net effect (Ge, C)
$\Delta E_{C,\Delta 4}$	-0.44 (x-8.3y)	0.37x - 4.2y	-0.07x – 0.5y
$\Delta E_{C,\Delta 2}$	0.25 (x-8.3y)	0.37x – 4.2y	0.62x – 6.3y
ΔE_C (lower edge)	0.25 (x-8.3y)	0.37x – 4.2y	0.62x – 6.3y
$\Delta E_{V,HH}$	0.04 (x-8.3y)	0.77x - 2.3y	0.81x – 2.6y
$\Delta E_{V,LH}$	( )	0.77x - 2.3y	( ) + 0.77x –2.3y
ΔE_V(higher edge)	( )	0.77x - 2.3y	( ) + 0.77x –2.3y
ΔE_G	0.25 (x-8.3y)-( )	-0.4x – 1.9y	-0.15x-4.0y-( )

Unit: eV.
For tensile-strained $Si_{1-x-y}Ge_xC_y$, x < 8.3y
( ) = -0.02 - 0.34(x-8.3y) + .5[.0016+0.007(x-8.3y)+0.25(x-8.3y)^2]$^{1/2}$
Commonly used terms:
$(\varepsilon_\perp - \varepsilon_{//})$ = 0.074(x-8.3y),
$(\varepsilon_\perp + 2\varepsilon_{//})$ = -0.052(x-8.3y),
$\Xi = 2D_V(\varepsilon_\perp - \varepsilon_{//}) \sim$ -0.34(x-8.3y)
$A_C(\varepsilon_\perp + 2\varepsilon_{//}) \sim$ -0.21(x-8.3y)
$A_V(\varepsilon_\perp + 2\varepsilon_{//}) \sim$ -0.13(x-8.3y)
Δ_o = 0.04 + 0.26x

Table 3.4: Effect of Ge and C incorporation on the band tensile-strained $Si_{1-x-y}Ge_xC_y$/Si and $Si_{1-y}C_y$/Si. Note that during the calculation, all terms involved x^2 are neglected.

3.7.5 Band Alignment of unstrained $Si_{1-x-y}Ge_xC_y/Si$

For the unstrained $Si_{1-x-y}Ge_xC_y/Si$, the effect on band offsets arises from the intrinsic effect of both Ge and C. Table 3.5 summarizes the results of our calculation. We observe that about 80% of the bandgap difference is located in the valence band of unstrained $Si_{1-x-y}Ge_xC_y/Si$ and the bandgap of unstrained $Si_{1-x-y}Ge_xC_y$ is significantly less than that of Si.

From table 3.5, we predict that the bandgap of unstrained $Si_{1-x-y}Ge_xC_y$ is smaller than that of Si by ~ -5.2y (eV). It was reported recently[23], based on PL study, that the no-phonon energy of unstrained $Si_{1-x-y}Ge_xC_y$ decreased linearly with increasing C content by ~-6.8y (eV). Since the authors conducted PL study was on a 87Å thick $Si_{1-x-y}Ge_xC_y$ quantum well, they estimated the confinement to blueshift the heavy hole by ~10 meV and electron by ~ 3 meV. If we subtract out the confinement effect, the bandgap decreases by ~ 55 meV/%C, consistent with our prediction.

3.8 Summary

We began this chapter by discussing various electrical and optical characterization methods to measure the total C effect on the valence band offset of compressively strained $Si_{1-x-y}Ge_xC_y/Si$.

After obtaining this information along with reported total effect of C on the bandgap of compressively strained $Si_{1-x-y}Ge_xC_y$, we proposed a simple model to predict the band alignment of strained $Si_{1-x-y}Ge_xC_y/Si$, $Si_{1-y}C_y/Si$ and unstrained $Si_{1-x-y}Ge_xC_y/Si$.

We proposed a simple model by assuming the effect of Ge and C incorporation can be independently broken into a strain effect due to Ge and C, an intrinsic effect of Ge, and an intrinsic effect of C. The strain effect is derived based on a "model solid

theory". In addition, the theory allows us to derive the intrinsic Ge effect on the valence band. By taking the experimental data of the intrinsic effect of Ge on the bandgap of unstrained $Si_{1-x}Ge_x$, we were able to obtain the intrinsic effect of Ge on the conduction band. Similarly, by combining the experimental data of the total effect of C on the bandgap and valence band of compressively strained $Si_{1-x-y}Ge_xC_y$ with the calculated strain effect due to C, we were able to derive the intrinsic effect of C on the bandgap, conduction band and valence band.

After the strain and intrinsic effects due to Ge and C addition are known, we were able to predict the band alignment of strained $Si_{1-x-y}Ge_xC_y$/Si, tensile-strained $Si_{1-y}C_y$ /Si and strain-free $Si_{1-x-y}Ge_xC_y$/Si. We found that recently reported numbers were consistent with our prediction.

	Ge	C	Strain-free $Si_{1-x-y}Ge_xC_y$
$\Delta E_C = \Delta E_{C,\Delta 2} = \Delta E_{C,\Delta 4}$	0.37x	-4.2y	0.37x – 4.2y (~ -1.16y)
$\Delta E_V = \Delta E_{V,HH} = \Delta E_{V,LH}$	0.77x	-2.3y	0.77x - 2.3y (~ 4.07y)
ΔE_g	-0.4x	-1.9y	-0.4x-1.9y (~ -5.23y)
In strain-free $Si_{1-x-y}Ge_xC_y$ x=8.3y			

Table 3.5: Intrinsic effect of Ge and C incorporation on the band structures.

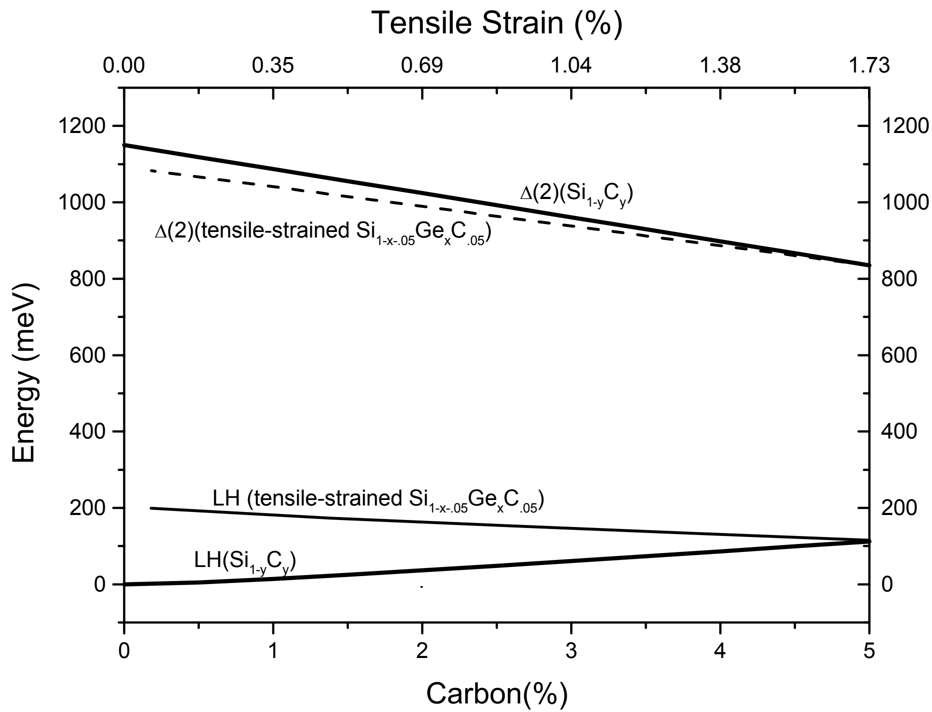


Figure 3.18: Solid lines show the conduction and valence band of the tensile-strained $Si_{1-y}C_y$ on a Si (100) substrate. The lower axis is C content and the upper axis is the corresponding strain. All energies are referred to the valence band energy of Si. Dashed lines show calculated conduction and valence band of the tensile-strained $Si_{1-x-.05}Ge_xC_{.05}$. In this case, only the top axis (strain) is relevant.

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Chapter 4

Two-Dimensional Hole Gas in Compressively Strained $Si_{1-x-y}Ge_xC_y$/ Si (100) Modulation Doped Structures

4.1 Introduction

One of the key parameters to study in applying $Si_{1-x-y}Ge_xC_y$ for potential device applications is the carrier mobility. To date, however, there are very few reports on the transport properties of holes in $Si_{1-x-y}Ge_xC_y$, and reports of transport properties are limited to the temperature range of 77K to 300K[1]. In this chapter, we report a transport study of two-dimensional hole gas in strained $Si_{1-x-y}Ge_xC_y$/ (100) Si modulation doped structures from room temperature down to 0.3K. We also investigate the effective mass of holes in strained $Si_{1-x-y}Ge_xC_y$ channels. By studying the effect of C on the effective mass, we can determine if the change in hole mobility by C incorporation is due to the change in effective mass or other C-related scattering.

4.2 Transport Study of Holes in Compressively Strained $Si_{1-x-y}Ge_xC_y$ Channels

In chapter 3, we discovered that the effect of C on the valence band offset of compressively strained $Si_{1-x-y}Ge_xC_y$ /Si (100) is small. As a result, the band structures of compressively strained $Si_{1-x-y}Ge_xC_y$ /Si (100) and $Si_{1-x}Ge_x$ /Si(100) with the same band gap are similar, with most of the band offset located in the valence band and with a negligible conduction band offset. To study the transport of holes as a function of carbon concentration, we fabricated a single heterojunction modulation doped structure. The

samples used in this study were grown by Rapid Thermal Chemical Vapor Deposition (RTCVD). The epitaxial layers were grown on lightly doped n type (100) Si wafers ($5x10^{15}/cm^3$). A 1 μm-thick undoped Si buffer layer was first deposited at 1000°C on the Si substrate, followed by the growth of 180Å undoped $Si_{1-x-y}Ge_xC_y$ at 575°C. A 50Å undoped Si spacer was then grown at 700°C, with the subsequent growth of 50Å boron-doped p type Si layer (doping $\sim 2x10^{18}/cm^3$) to supply holes to the $Si_{1-x-y}Ge_xC_y$ channels. After continuing the growth with 600Å undoped Si, a 150Å p-type Si (doping $\sim 1x10^{18}/cm^3$) was deposited as a cap layer. The doped Si cap layer was used to prevent depletion caused by surface states. Meanwhile, the doping concentration in both the cap and supply layer was carefully chosen to avoid the formation of degenerately doped layers which occurs at doping level above $\sim 3x10^{18}/cm^3$, which would result in parallel hole conducting channels even at low temperatures. The germanium content in the $Si_{1-x-y}Ge_xC_y$ alloys was fixed at 24% and the C level ranged from 0% to 1%. Figure 4.1 shows a typical sample structure and figure 4.2 shows the schematic energy band diagram for the structure with a two-dimensional hole transport in the compressively strained $Si_{1-x-y}Ge_xC_y$ channel.

A Hall bar structure was used in this study. A 1000Å thick blanket Al was first thermally evaporated on the wafer. The Hall geometry was then patterned and dry-etched in CF_4/O_2 ambient. Finally, the metal contact was formed by Al wet etching to remove Al from the no-contact areas. The contact to the hole gas in the $Si_{1-x-y}Ge_xC_y$ channel was obtained by annealing the sample at 300°C for 1-2 minutes, which results in Al diffusion to the $Si_{1-x-y}Ge_xC_y$ channel and thus a contact to the hole gas. The annealing temperature

used for Al contact was lower then the typical number reported in the literature (~ 500°C.)

Si cap ~150 Å (~ $1x10^{18}/cm^3$) (shielding layer)
undoped Si cap ~ 600Å
p+ Si ~ 50 Å (~ $2x10^{18}/cm^3$) (supply layer)
undoped Si spacer~ 50Å 5050Å
+ + + + + 2DHG + + + +   SiGeC ~ 180 Å (strained)
undoped Si buffer ~ 1μm
(100) n- Si substrate

Figure 4.1: The sample structure of the compressively strained $Si_{1-x-y}Ge_xC_y$ /Si (100) modulation doped structure. The doping levels are $2x10^{18}/cm^3$ for the supply layer and $1x10^{18}/cm^3$ for the cap layer. The spacer layer is 50 Å. The position of the two-dimensional hole gas is schematically indicated.

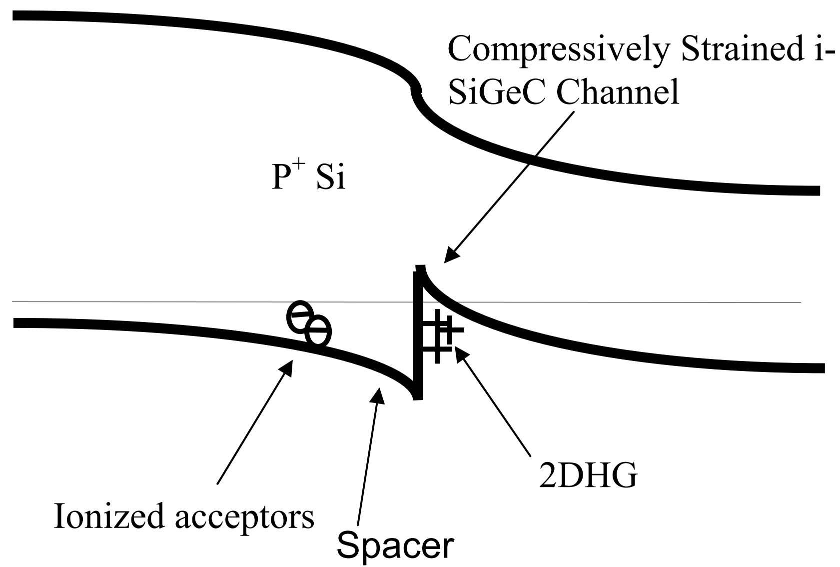


Figure 4.2: Schematic energy band diagram of a compressively strained $Si_{1-x-y}Ge_xC_y$ /Si (100) modulation doped structure. The holes are confined in the compressively strained $Si_{1-x-y}Ge_xC_y$ layer.

We found that by working at lower temperatures, we avoided the excess Al spiking to the p-n junction or even further to the n-type Si substrate, which could result in a parallel conducting path.

Figure 4.3 shows the mobility and carrier density of the two-dimensional (2-D) hole gas in the $Si_{1-xy}Ge_xC_y$ channel from room temperature to 10K. The initial decrease and eventual saturation of the hole density indicate the freeze-out of parallel conduction paths. The hole mobility increases with decreasing temperature. This is the first evidence of the formation of a 2-D hole gas in the $Si_{1-x-y}Ge_xC_y$ channels. The carrier density saturates at $10^{12}/cm^2$ at low temperatures, suggesting a complete hole transfer, as designed for, from the Si dopant layer to the $Si_{1-xy}Ge_xC_y$ channel. The variations in the density from sample to sample may be due to imperfect doping control during growth, and are not thought to be caused by changes in the valence band offset.

The hole mobility at low temperatures decreases as C is incorporated. It is not clear that if the decrease in hole mobility is due to enhanced alloy scattering with the addition of C, or other factors, such as increased interface roughness or C-related defects. In the next section, we will find that the hole effective mass is unchanged in the $Si_{1-x-y}Ge_xC_y$ channel as C is added (up to 0.6%) compared to that in the $Si_{1-x}Ge_x$ channel. We conclude that the reduction in hole mobility is due to increased scattering. The increased scattering could be due to alloy scattering, C-related defects, or interstitial C. If the reduction is dominated by the increased alloy scattering, we can estimate the alloy scattering potential due to C ($V_{\mathrm{alloy,C}}$). We have

$$\frac{1}{\mu_{SiGeC}} = \frac{1}{\mu_{SiGe}} + \frac{1}{\mu_{alloy,C}} \tag{4.1}$$

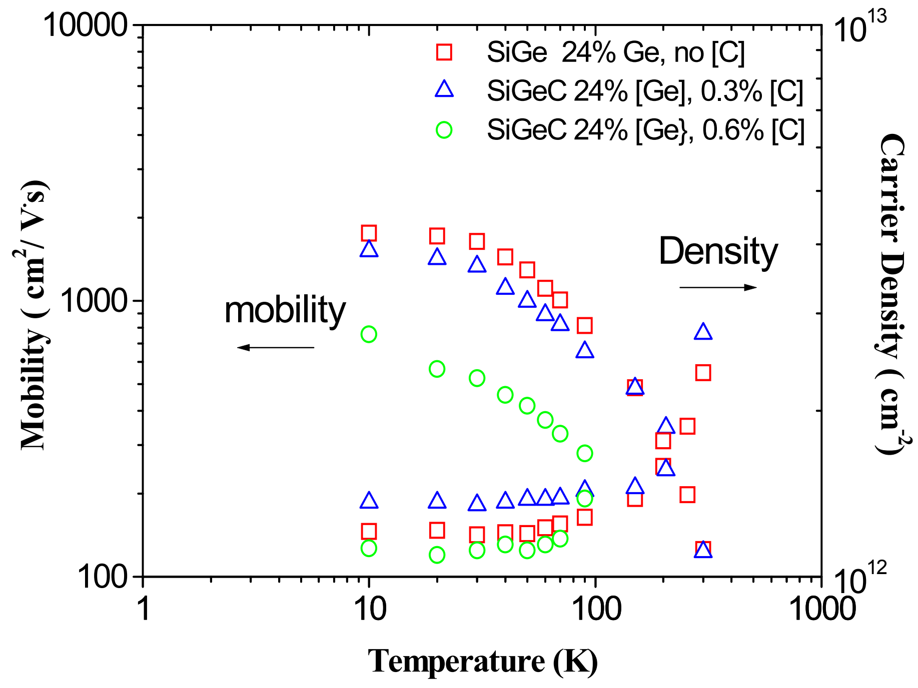


Fig 4.3: Carrier density and mobility as a function of temperature of the compressively strained $Si/Si_{1-x-y}Ge_xC_y$ modulation-doped heterostructure.

Where $\mu_{alloy,C}$ is alloy scattering caused by C and μ_{SiGe} is mobility of $Si_{1-x}Ge_x$. From our data, we have $\mu_{alloy,C}$ =11337 cm^2/Vs for the sample with 0.3%C and $\mu_{alloy,C}$ =1331 cm^2/Vs for the sample with 0.6%C. Based on the alloy scattering model[2], we have

$$\frac{1}{\mu_{alloy}} = \frac{K}{V^2_{alloy,C}\, y(1-y)\, n^{\frac{1}{3}}} \tag{4.2}$$

Where K is a material dependent parameter; y is the C level and n is the carrier concentration. Figure 4.4 plots $\frac{\mu_{alloy,C} K^{1/2}}{n^{\frac{1}{3}}}$ vs. $[y(1-y)]^{1/2}$. According to equation 4.2, the plot should ideally be a straight line with slope of $V_{alloy,C.}$ The y=0 and y=0.3% points can be fit with a slope of $V_{alloy,C}$= 0.42eV. This compared to V_{alloy} of 0.6eV, for alloy scattering plots of Ge for holes in $Si_{1-x}Ge_x$ under similar condition[3]. For the layer with y=0.06%, the increase in scattering is much stronger than that predicted by the alloy scattering model of Eqn 4.2. This suggests that C-related defects (such as C interstitials), which appear mostly at high C level, dominate the scattering.

4.3 Effective Mass Measurement of Holes in Strained $Si_{1-x-y}Ge_xC_y$ Channels

To measure the hole effective mass, samples were first placed in the ^{3}He system for the observation of Shubnikov-deHaas (SdH) oscillations in the Hall and magnetotransport measurements. Figure 4.5 shows the SdH oscillations of $Si_{1-x-y}Ge_xC_y$ with 0.6% C with

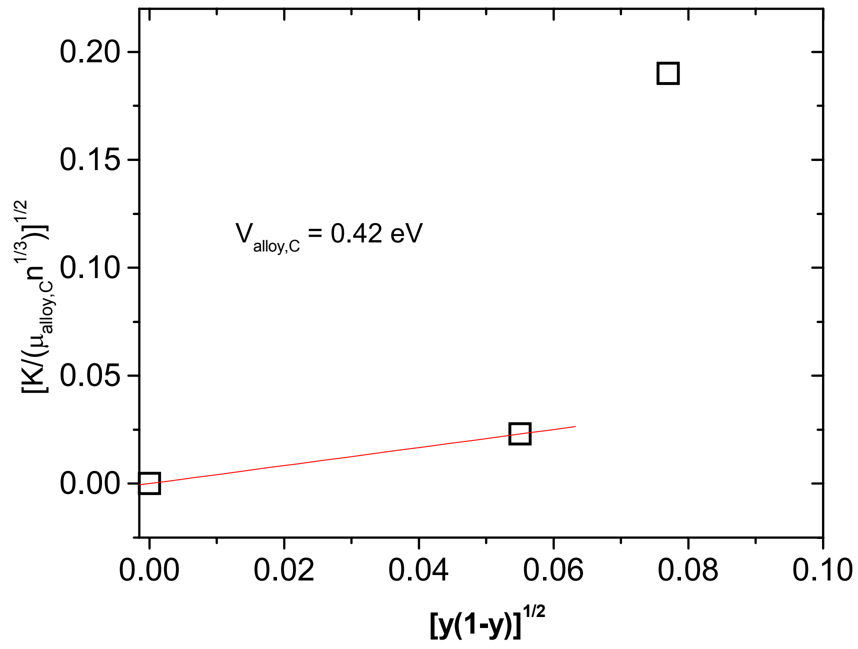


Figure 4.4: Alloying scattering model calculations. The y=0 and y=0.003 plots are fitted with $V_{\text{alloy,C}} = 0.42$ eV.

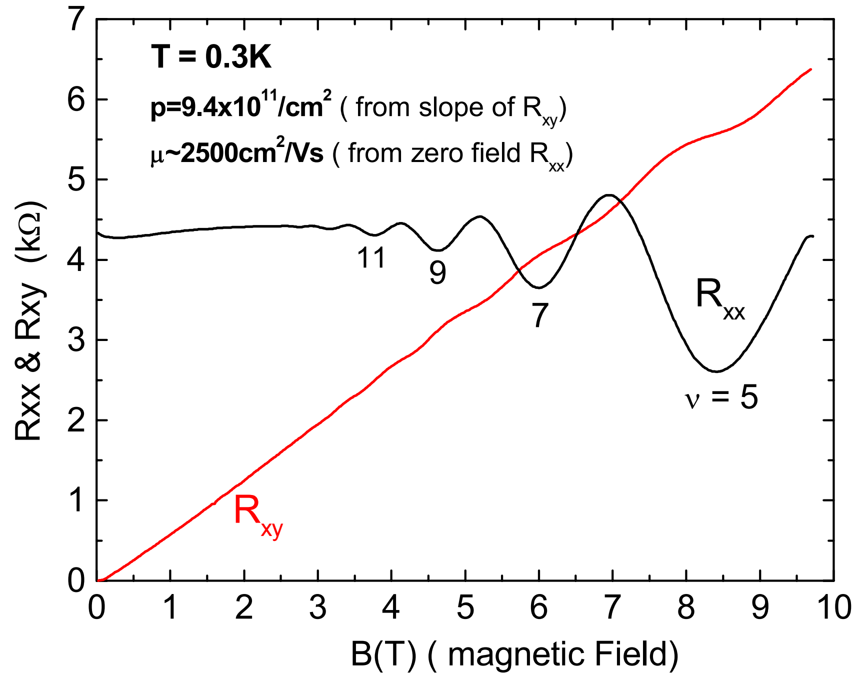
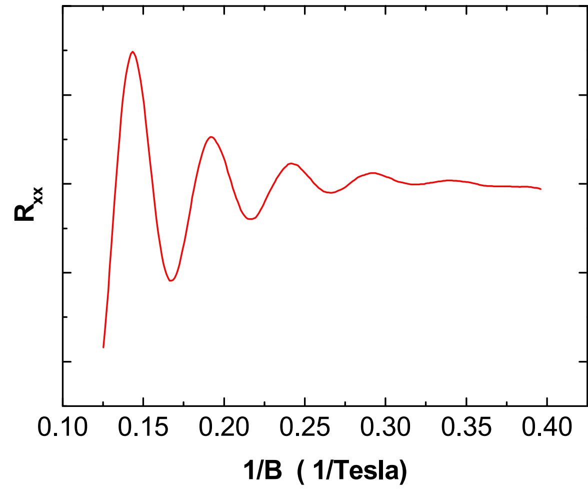


Figure 4.5: The longitudinal and transverse resistances of the 2D hole gas in the compressively strained $Si_{0.754}Ge_{0.24}C_{0.006}$ channel at 0.3K. SdH oscillations are revealed and ν is the filling factor.

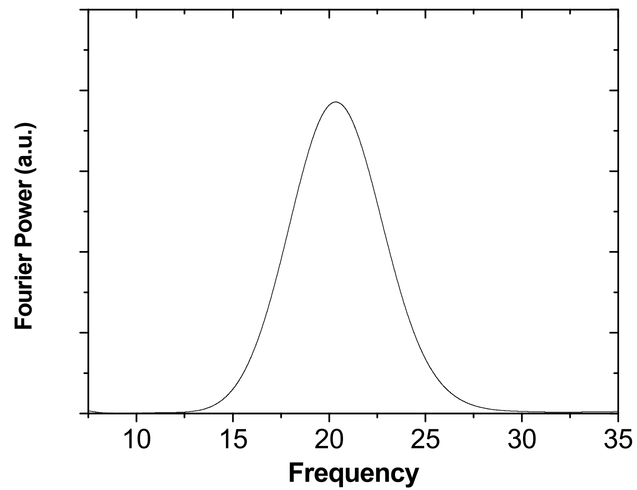
magnetic sweep from 0 Tesla to 10 Tesla at 0.3K. The oscillation begins at around 3 Tesla and the swing becomes larger at higher magnetic fields, suggesting that the oscillation is moving toward quantum Hall regime. At the same time, transverse resistance (R_{xy}) weakly reveals a few quantum Hall plateaus. It is noted that only odd filling factors are resolved, which could be due to rather large g-factor, causing the Zeeman splitting to match the Landau level splitting[4]. Since the SdH oscillation is periodic in the reciprocal magnetic field, as shown in figure 4.6, one can determine the carrier density from the periodicity. The obtained number from this method is $9.8 \times 10^{11}/cm^2$. From the slope of R_{xy} at low magnetic fields in figure 4.5, one finds carrier density of $9.4 \times 10^{11}/cm^2$, which agrees with the value obtained form the oscillation periodicity, within 5%. By combining R_{xx} and R_{xy}, one finds the low-field hole mobility to be 2500 $cm^2/V \cdot sec$ at 0.3K for $Si_{1-x-y}Ge_xC_y$ with 0.6% carbon.

The hole effective mass in the $Si_{1-x-y}Ge_xC_y$ channels is determined by measuring the change of SdH oscillation amplitudes as a function of temperature[5,6,7]. The amplitude decreases with increasing temperature (see figure 4.7) as the Fermi distribution broadens at higher temperatures and leads to partial occupation of holes at higher Landau levels for holes in the higher energy tail of the Fermi function. The dependence of the oscillation amplitudes on the effective mass arises from its dependence on the energy spacing of the Landau levels, which scales inversely to the effective mass change. The temperature dependence of the oscillation amplitude (A) at a given magnetic field (B) can be expressed by

$$A \sim \frac{\xi}{\sinh(\xi)} \exp\left(-\frac{\pi}{\tau \omega_C}\right) \qquad (4.2)$$



(a)



(b)

Figure 4.6: (a) The periodic SdH oscillations are shown in the reciprocal magnetic field. The hole density is determined to be $9.8x10^{11}/cm^2$ for the periodicity. (b) The Fourier transform of the periodic SdH oscillations in reciprocal magnetic field. The hole density can also be determined from the position of the peak.

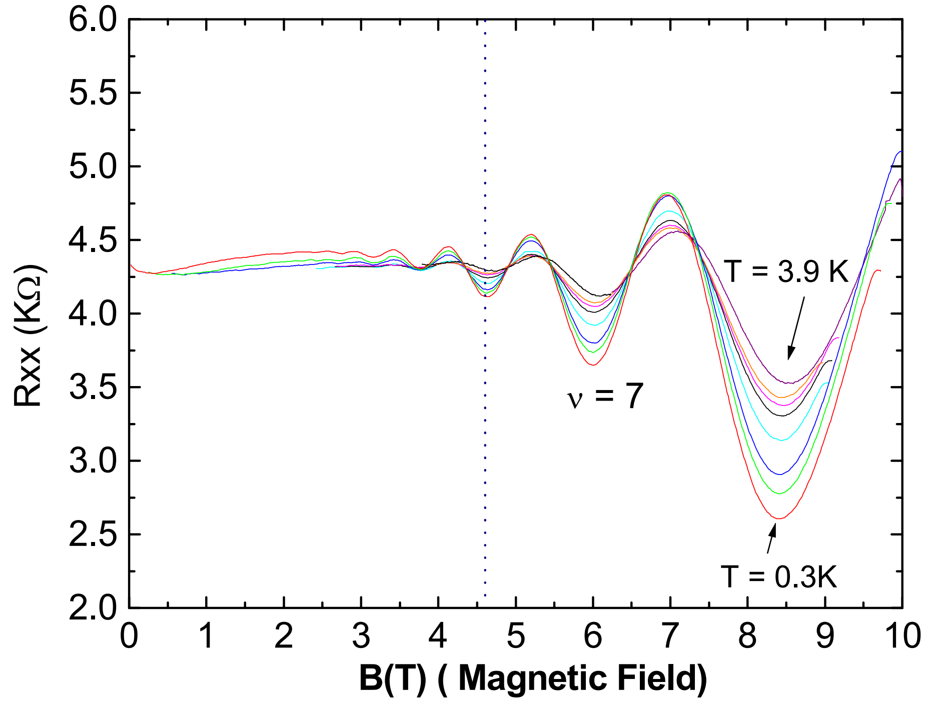


Figure 4.7: SDH oscillations of 2D hole gas in the $Si_{0.754}Ge_{0.24}C_{0.006}$ channel at various temperatures. The amplitude of the oscillation decreases as temperature is increased.

where $\xi = \frac{2\pi^2 \kappa T}{\hbar\omega_c}$, $\omega_c = \frac{eB}{m^*}$, κ is the Boltzmann constant, m^* is the hole effective mass and τ is the lifetime. It is observed from the above equation that the oscillation amplitude depends on temperature and the spacing of Landau levels, which is determined by the magnetic field and effective mass. Therefore, if the change of the oscillation amplitude is plotted as a function of temperature at a given magnetic field, one can determine the effective mass by using it as an adjustable parameter to fit the experimental data. This can be repeated at each magnetic field at which there is a peak or valley of the SdH oscillation, generating effective mass as a function of the magnetic field.

Figure 4.8 is the result of such an analysis for the sample with a carbon level of 0.6%. In this sample, the hole effective mass ranges from 0.31~ 0.32 m_o. The fitting error in this procedure of extracting m* from the original data of R_{xx} versus B is estimated at 0.01 m_o, as illustrated in figure 4.9. The lifetime we obtained in these samples is in the order of 10^{-13} s, which is close to the transport lifetime obtained at a zero magnetic field. It implies that large angle scattering dominates in these samples, attributable to a significant amount of C-related defecs in the channel. Figure 4.10 shows the comparison of hole effective mass in the $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ channels. There is no significant change in the effective mass as C is added substitutionally up to 0.6%. It shows for the first time that the valence band structure of the compressively strained $Si_{1-x-y}Ge_xC_y$ is similar to that of $Si_{1-x}Ge_x$. It is also noted that the effective mass obtained in our samples is close to the number reported by People et al. for the MBE-grown modulation-doped heterostructure with similar Ge concentration (20%) and no carbon[7].

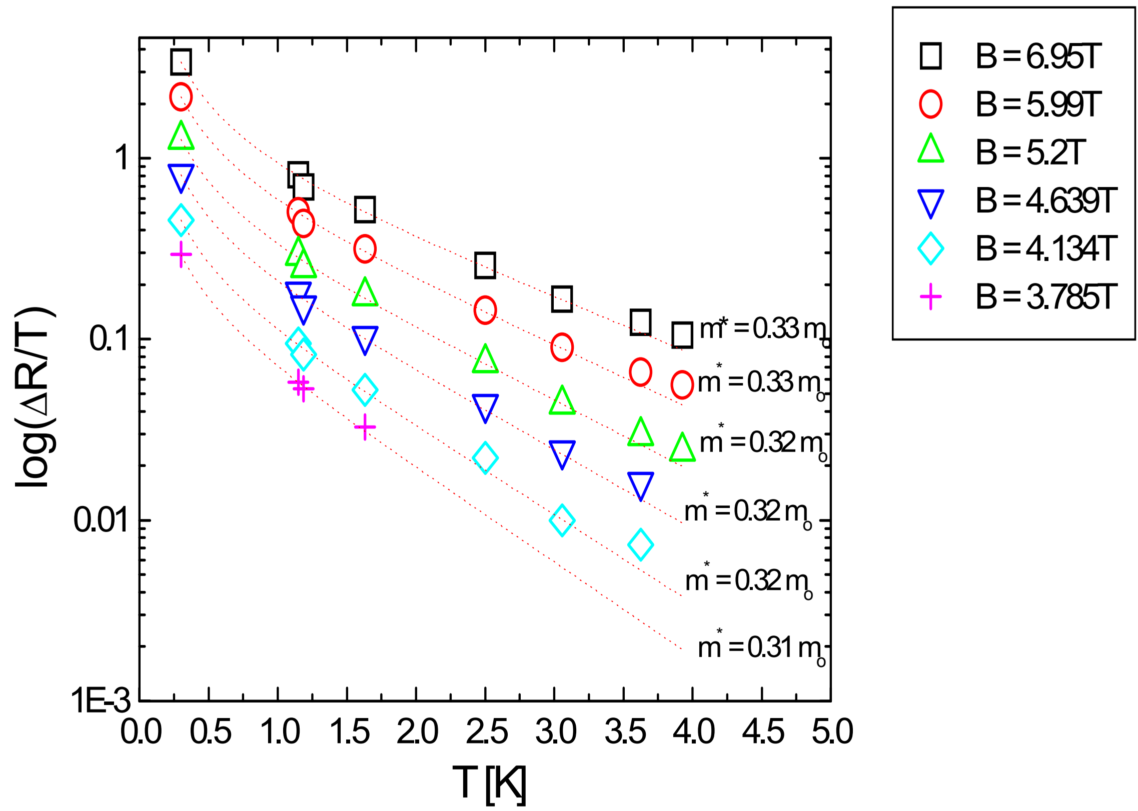


Figure 4.8: Hole effective mass in the $Si_{0.754}Ge_{0.24}C_{0.006}$ channel measured at various magnetic fields. The change in R_{xx} vs. temperature is modeled with m* as adjustable parameter at various magnetic fields.

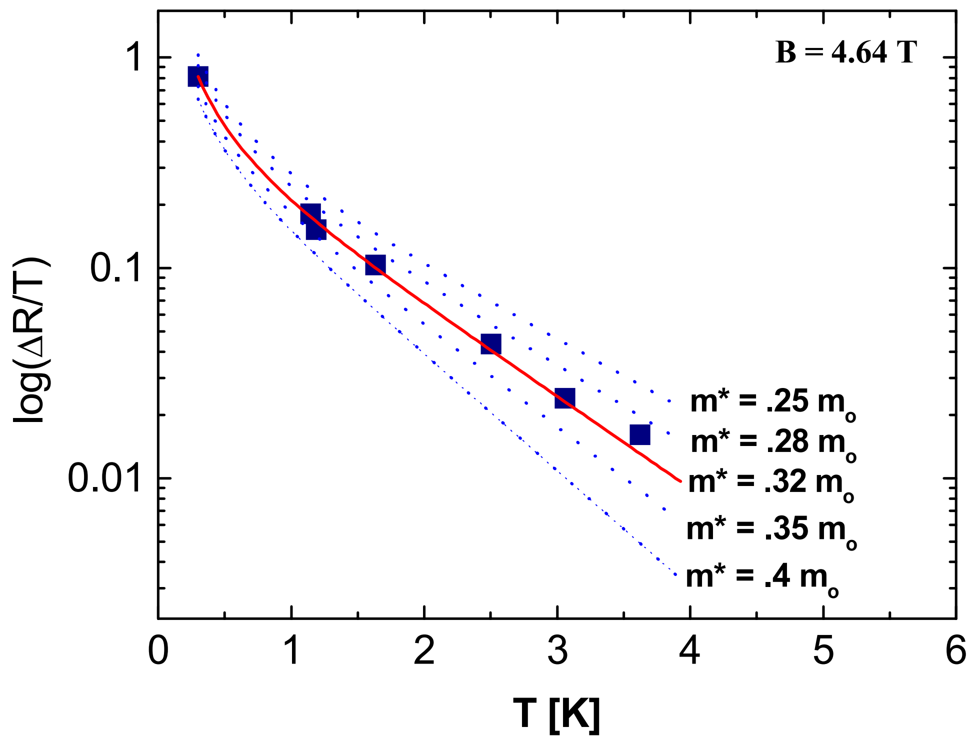


Figure 4.9: The change in R_{xx} vs. temperature at B=4.64 T of the sample with 0.6%C is modeled with various number of m* to find the best fit.

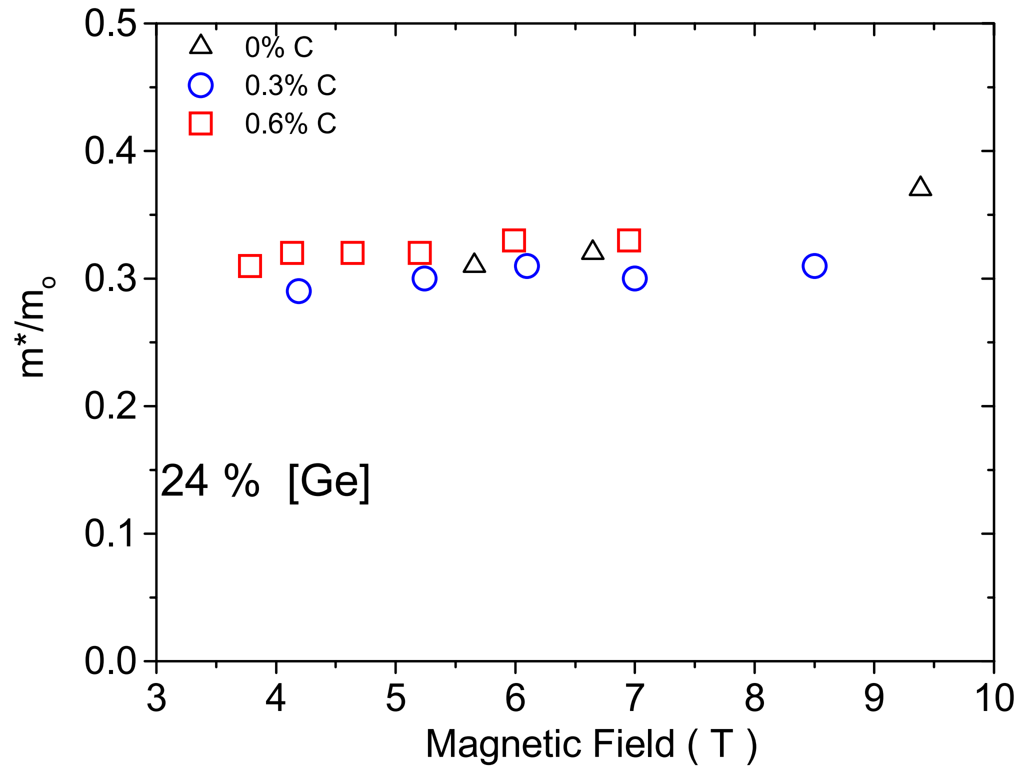


Fig 4.10: Hole effective mass in $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ channels measured by various magnetic fields. There is no significant change in the effective mass as C is added

A calculation of the valence band structure of $Si_{1-x}Ge_x$ with 24% Ge shows that energy splitting between heavy hole band (HH) and light hole band (LH) at k= 0 (wave vector) is 47 meV[8]. In the sample with 0.6% carbon, if one considers the strain reduction due to the incorporation of substitutional carbon and assumes the deformation potential in $Si_{1-x-y}Ge_xC_y$ to be the same as that in $Si_{1-x}Ge_x$, the HH-LH splitting in the sample is 39 meV. It will be even larger in the sample without C (larger strain). For the two-dimensional hole concentration in this study (~$1x10^{12}/cm^2$), the Fermi level is 7 meV away from the top of the heavy hole band, (assuming effective mass of $0.3m_o$). This indicates that holes occupy only the very top of the heavy hole band. The effective mass obtained in this study is therefore the heavy hole effective mass and is not affected by any nonparabolicity due to interactions of HH and LH bands.

4.4 Summary

In this chapter, we demonstrated a two-dimensional hole gas in modulation doped $Si_{1-xy}Ge_xC_y$ channels. We found that the hole mobility decreases as more carbon is added to the $Si_{1-x}Ge_x$ alloys. To investigate if the decrease in hole mobility is due to a fundamental change in effective mass by carbon incorporation or due to increased scattering by carbon or its related defects, we measured the hole effective mass based on the analysis of SdH oscillations as a function of temperature. It revealed that the heavy hole effective mass of $Si_{1-x-y}Ge_xC_y$ is 0.32 m_o and the effective mass remains unchanged for carbon level up to 0.6%. Thus we conclude that the reduction in mobility as C is added is due to increased scattering by the addition of carbon. Also, the valence band structure of compressively strained $Si_{1-xy}Ge_xC_y$ is similar to that of $Si_{1-x}Ge_x$.

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Chapter 5

Polycrystalline $Si_{1-x-y}Ge_xC_y$ to Suppress Boron Penetration in Polycrystalline-Gated Metal-Oxide-Semiconductor Structures

5.1 Introduction

In a traditional complementary metal-oxide-semiconductor (CMOS) technology, heavily doped n-type (n^+) polycrystalline silicon gates are used for both n- channel (NMOS) and p- channel (PMOS) devices. In order to achieve a high drive current and an optimal logic-gate performance, it is desirable that both n- and p- channel devices have small and opposite threshold voltages (V_T) with comparable magnitudes. The n^+ polycrystalline silicon gate yields a reasonable threshold voltage for n-channel devices, but the threshold voltage of the p-channel devices has a much higher magnitude. As a result, boron is implanted into the device channel to adjust threshold voltage, forming a buried-channel PMOS device.

Even though buried-channel devices generally exhibit a higher carrier mobility than typical surface-channel devices by moving carriers away from the SiO_2/Si interface, the advantage is outweighed by other deleterious short-channel effects, such as threshold voltage lowering, higher subthreshold currents and higher susceptibility to punchthrough[1]. Furthermore, buried channels are not suitable for low temperature operation due to a dopant freeze-out problem[2]. As a result, as devices are scaled down in size to below 0.35 μm in gate length, "dual-gate" devices are desirable to create both PMOS and NMOS surface-channel devices with better short-channel characteristics.

In dual-gate CMOS devices, n^+ polycrystalline silicon is used as the gate for NMOS devices and p^+ polycrystalline silicon is used for PMOS devices. A single undoped polycrystalline silicon layer is deposited, which is then doped n^+ or p^+ by the source/drain implantation process of the n-channel and p-channel devices, respectively. For a p^+ polycrystalline-silicon-gated device, the gate is implanted with boron or boron difluoride (BF_2^+) at the same time as are source and drain. Unfortunately, boron has been observed to penetrate through the thin gate oxide into the channel region of the substrate during post-implant anneal, resulting in a undesirable shift in threshold voltage[3]. Moreover, even though gate oxides with the presence of fluorine have been shown to increase the resistance to hot-carrier effects, enhanced boron penetration has been reported due to the presence of fluorine in gate oxide[4]. Fluorine increases the boron diffusion constant in oxide[5] and it has been shown that the boron diffusivity increases approximately as the square root of the fluorine dose.

Efforts have been made to alleviate the problem of boron penetration. P^+ polycrystalline silicon gates co-implanted with arsenic (or phosphorus) were reported to exhibit less of a boron penetration problem due to the formation of a physical barrier by the segregation of arsenic (or phosphorus) at the gate electrode/gate oxide interface[6]. One concern with this co-implantation is that arsenic or phosphorus may compensate boron at the top oxide interface, resulting in gate depletion under reverse bias, which reduces drive currents.

Nitrided oxide which is of interest for its immunity to hot carrier damage[7], has also been proposed as a solution to suppress boron penetration as well as hot-carrier effects. Nitrided oxides are produced by growing oxides in NO or N_2O ambients, or by thermal nitridation of silicon dioxides in NH_3, NO, or N_2O ambients, all resulting in

oxynitrides. In an oxynitride, nitrogen atoms pile up at the oxynitride/ Si substrate interface and act as a physical barrier to prevent boron from penetrating into the Si substrate. There are problems associated with oxynitrides, however. First, oxynitrides produced by NH_3-based ambients result in higher amounts of fixed charge, even though a more effective barrier can be formed due to a higher level of nitrogen incorporation (up to 10%). Second, oxynitrides obtained from NO or N_2O ambients require a higher thermal budget due to a smaller growth rate of oxynitrides. Furthermore, oxynitrides grown by this method have only up to 2% nitrogen incorporation, diminishing the ability to be a physical barrier.

In this chapter, we discuss how we can improve the problem of boron penetration by using polycrystalline $Si_{1-x-y}Ge_xC_y$ as part of a polycrystalline gate. It has recently been reported that substitutional carbon in single crystalline $Si_{1-x-y}Ge_xC_y$ can dramatically suppress boron diffusion due to thermal annealing in nitrogen[8], oxidation- enhanced diffusion[9], or transient-enhanced diffusion[10]. Since Si interstitials are responsible for enhanced boron diffusion, it suggests that C atoms can act as a trap for Si interstitials, therefore, suppress enhanced diffusion. In this chapter we find that by growing polycrystalline $Si_{1-x-y}Ge_xC_y$ as part of a gate electrode in a PMOS device, we can suppress boron penetration through the thin gate oxide.

Polycrystalline $Si_{1-x}Ge_x$-based gates have previously been studied because it is possible to adjust the work function of the gate electrode by a few tenths of a volt by varying the amount of germanium fraction[11]. Furthermore, the sheet resistance of polycrystalline $Si_{1-x}Ge_x$ is lower than that of the polycrystalline silicon due to the larger grain size which reduces carrier scattering[12]. However, the effects of $Si_{1-x}Ge_x$ or $Si_{1-x-y}Ge_xC_y$ in the gate on boron penetration have not yet been studied or reported.

5.2 Polycrystalline $Si_{1-x-y}Ge_xC_y$ to Suppress Boron Penetration in PMOS Devices

Samples were fabricated by first thermally oxidizing n-type silicon wafers in dry oxygen at 900ºC. The RCA-cleaned Si wafers were first loaded into an oxidation furnace (furnace #3) in a N_2 ambient. The loading process was rather slow (~3 minutes) to avoid any temperature fluctuation. We waited for ~3 minutes after loading for the temperature of the wafers to be stable before the dry O_2 gas was switched on. The oxidation process lasted for ~ 15 minutes, resulting in 80-90 Å oxides. After that, the N_2 gas was switched back on and the oxidized wafers were annealed at 900ºC for ~25 minutes before unloading. The oxidized Si wafer was then loaded into the RTCVD chamber for the polycrystalline gate deposition without further solvent or acid cleaning. Before the deposition, the wafer was cleaned at 18% lamp power (~700ºC) under 3 lpm H_2 flow at a chamber pressure of 6 torr. Note that the cleaning was performed at a much lower temperature and pressure than that under our regular pre-epitaxial condition (250 torr, 1000ºC) to avoid any H_2 reaction with the thin gate oxide.

It was reported that the incubation time for the deposition of polycrystalline $Si_{1-x-y}Ge_xC_y$ on oxide is less than that of polycrystalline Si[13]. Therefore, a 100 sccm 10% SiH_4 in Ar mixture was first flowed at 700ºC for 10 seconds to deposit a thin polycrystalline Si layer on the oxide surface in every sample grown in this study. It is estimated that the "wetting layer" is less than 1nm. Polycrystalline silicon was deposited at 700ºC using silane, and polycrystalline $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ layers were deposited at 625ºC with silane, germane and methylsilane flow, all with H_2 as a carrier gas at 6 torr. The flow

rate was 100sccm for both SiH_4/Ar mixture and the GeH_4 mixture(1% GeH_4 in H_2). The methylsilane flow ranged from 0 to 8 sccm, resulting in an estimated 0-0.8%C in the $Si_{1-x-y}Ge_xC_y$ layers. Diborane was used for p-type doping if samples were in-situ doped and the flow rate was 500 sccm. A typical growth sequence is listed in appendix A.3. Appendix A.4 summarizes the growth details of all samples studied in this Chapter.

Ion-implantation was performed with $5x10^{15}/cm^2$ BF_2^+ doses at 60 keV, resulting in ~ 100nm deep implantation damage. BF_2^+ was used because it has been widely used in industry for gates as well as source/drain shallow implants of MOSFET devices. Fluorine-enhanced boron diffusion will also make the effect of boron penetration significant in this study even with the relatively thick oxide (~10nm). Samples were annealed in nitrogen after implantation. To study boron penetration across the gate oxide, metal-oxide-semiconductor (MOS) capacitors were fabricated. The sample was first patterned by photolithography and wet etching. The wet etching was used instead of dry etching due to concern about damage to the gate oxide. Al was then evaporated on the back of the wafer for a bottom contact after the gates and the gate oxides were removed from the back of the wafer. No difference was observed for the initial test samples with and without Al used for top contacts on top of the polycrystalline gates, and no effect of forming gas anneal was seen on the high-frequency C-V curves. Therefore for simplicity of processing, no Al top contact was used and no forming gas anneal was performed for all data reported in this chapter. We checked two samples (A(1) and A(3) annealed at 900ºC for 60 minutes after BF_2^+ implantation) with Al used for top contact and with forming gas anneal at 300ºC for 5 minutes. No difference was found compared to the same samples with no Al top contact and forming gas treatment.

There are five different sets of samples studied in this chapter. Diagram 5.1 shows a typical sample structure of each set and Table 5.1 summarizes all sample structures of each set.

5.2.1 Undoped Polycrystalline $Si_{1-x-y}Ge_xC_y$ as an Intermediate Layer

The first set (A series) contains four samples with different gate structures. Sample A(1) (#2250) is a traditional MOS structure, with a ~ 400nm polycrystalline silicon on a 90Å gate oxide. In sample A(2) (#2251), we grew a 25nm intermediate polycrystalline $Si_{1-x-y}Ge_xC_y$ layer with 20% germanium and 0.6% substitutional carbon on top of the gate oxide, followed by 375nm of polycrystalline silicon to keep the entire gate thickness unchanged. Sample A(3) (#2252) is similar to A(2) except polycrystalline $Si_{1-x}Ge_x$ was used instead of polycrystalline $Si_{1-x-y}Ge_xC_y$. The last sample, A(4) (#2253), is similar to A(1) except for the fact that methylsilane (carbon precursor) was flowed in the first 25nm of polycrystalline Si layer. Figure 2.1 shows that, for single crystalline $Si_{1-y}C_y$ grown by silane and methylsilane flow at 700ºC, most C occupies interstitial and not substitutional sites. We therefore suspect that most carbon in sample A(4) also occupies interstitial sites. All layers were initially undoped and subsequently doped by BF_2^+ implants.

Figure 5.1 shows high-frequency (1 MHz) capacitance-voltage (C-V) curves samples annealed at 900ºC for 40 and 80 minutes. There is no significant shift in the threshold voltage after 40 minutes anneal. After 80 minutes anneal, however, we observed that the threshold voltage shifted positively by ~7 volts in sample A(1), an indication of boron penetration through the gate oxide into the substrate. A lesser shift

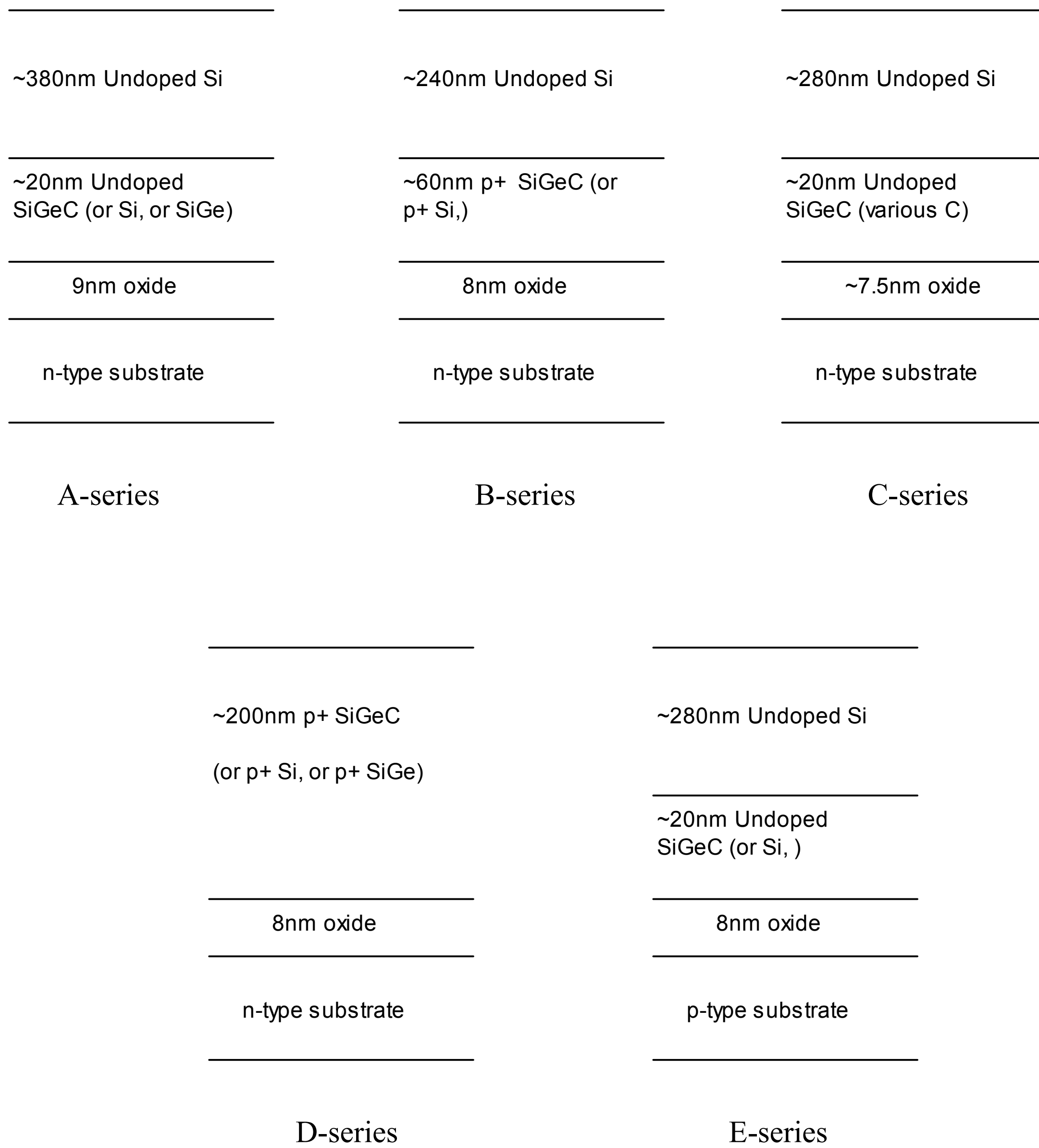
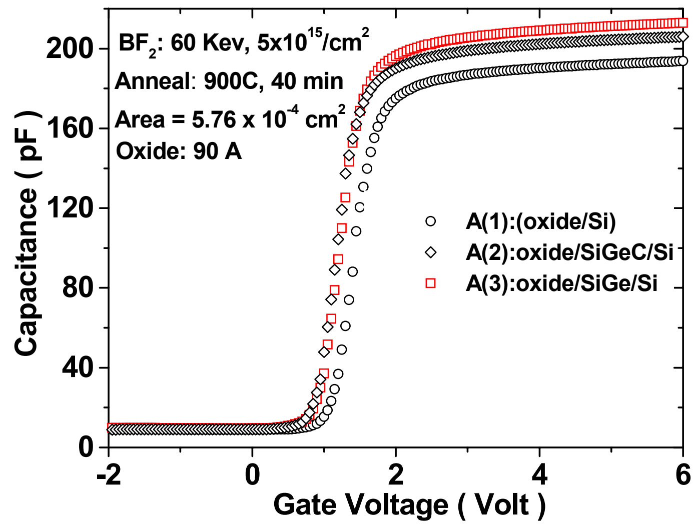


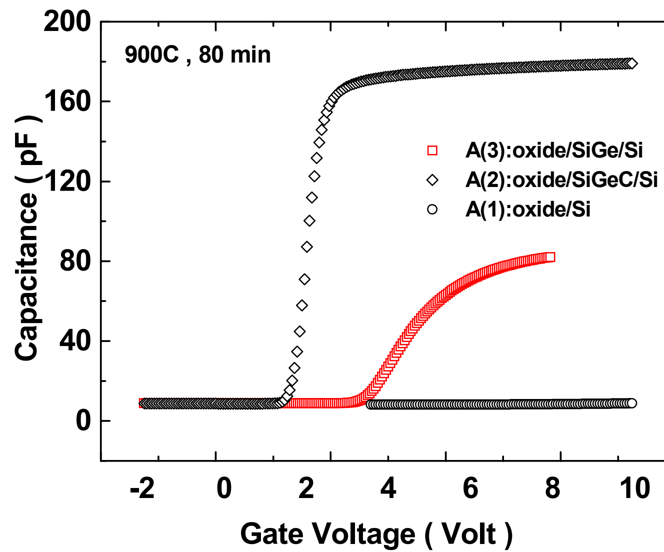
Diagram 5.1: Typical sample structures of A,B, C, D, E series.

A series: A(1)(#2250) n-type Si/9nm oxide/~400nm Si/ A(2)(#2251) n-type Si/9nm oxide/~25nm undoped $Si_{.794}Ge_{.2}C_{.006}$ / ~375nm undoped Si/ A(3)(#2252) n-type Si/9nm oxide/~25nm undoped $Si_{.8}Ge_{.2}$/~375 nm undoped Si A(4)(#2253) n-type Si/9nm oxide/~25nm undoped Si:C/375 nm undoped Si
B Series B(1)(#2262) n-type Si/8nm oxide/~300nm undoped Si/ B(2)(#2261) n-type Si/8nm oxide/~60nm p^+ $Si_{.794}Ge_{.2}C_{.006}$ / ~240nm undoped Si/ B(3)(#2259) n-type Si/8nm oxide/~60nm p^+ Si / ~240nm undoped Si/
C series: C(1)(#2290) n-type Si/7.5nm oxide/~300nm Si/ C(2)(#2292) n-type Si/7.5nm oxide/~20nm undoped $Si_{.792}Ge_{.2}C_{.008}$ / ~280nm undoped Si/ C(3)(#2291) n-type Si/7.5nm oxide/6nm undoped Si/~20nm undoped $Si_{.792}Ge_{.2}C_{.008}$/~280nm undoped Si C(4)(#2293) n-type Si/7.5nm oxide/~20nm undoped $Si_{.796}Ge_{.2}C_{.004}$ / ~280nm undoped Si/
D series: D(1)(#2335,#2398) n-type Si/8nm oxide/~200nm p^+ Si/ D(2)(#2336) n-type Si/8nm oxide/~200nm p^+ $Si_{.8}Ge_{.2}$/ D(3)(#2334) n-type Si/8nm oxide/~200nm p^+ $Si_{.798}Ge_{.2}C_{.002}$ / D(4)(#2400) n-type Si/8nm oxide/~200nm p^+ $Si_{.794}Ge_{.2}C_{.006}$ /
E series: E(1)(#2450) p-type Si/8nm oxide/~300nm Si/ E(2)(#2452) p-type Si/8nm oxide/~25nm undoped $Si_{.794}Ge_{.2}C_{.006}$ / ~375nm undoped Si/

Table 5.1: A summary of sample structures used in this study.



(a)



(b)

Figure 5.1: (a) High-frequency C-V curves of implanted samples annealed at 900ºC for 40 minutes. (b) C-V curves after 80 minutes of annealing.

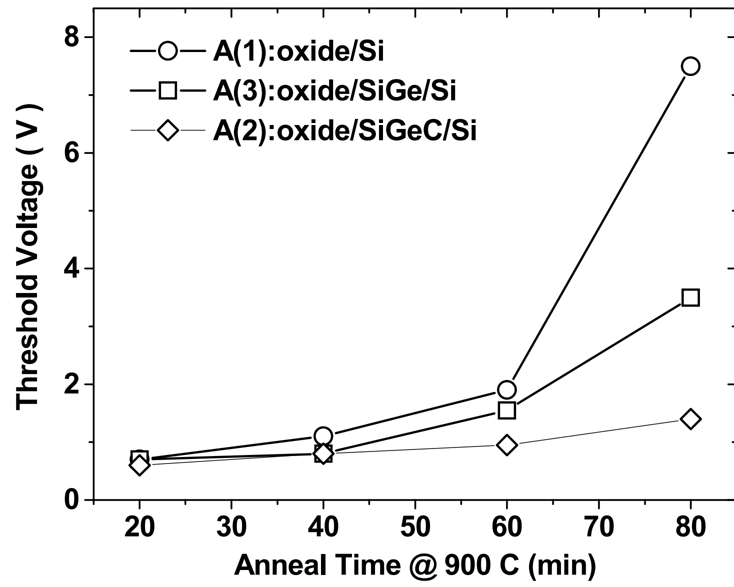
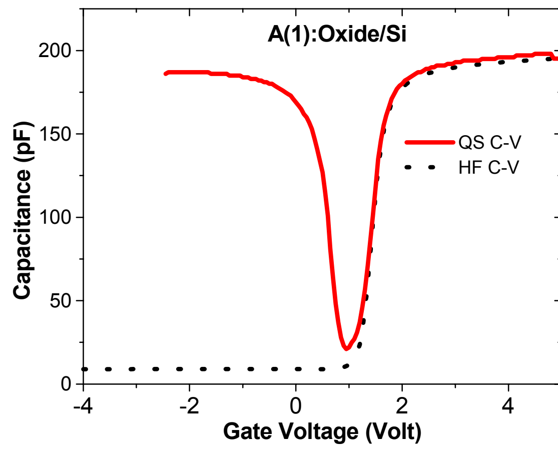


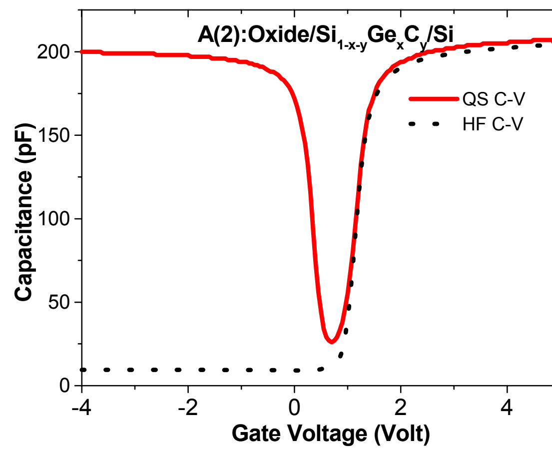
Figure 5.2: Threshold voltage as a function of annealing time.

(~2 volts) was observed in sample A(3), suggesting that $Si_{1-x}Ge_x$ is effective in suppressing boron penetration. It also clearly revealed that $Si_{1-x-y}Ge_xC_y$ is most effective in suppressing boron penetration, as there was no significant threshold shift in sample A(2). Figure 5.2 shows the threshold voltage as a function of annealing time. It is concluded that the $Si_{1-x-y}Ge_xC_y$ layer greatly suppresses boron penetration and even the $Si_{1-x}Ge_x$ layer has a significant effect. We also observed the largest threshold voltage shift in sample A(4). It is not clear if it is due to the suspected interstitial C in the sample.

Although the $Si_{1-x-y}Ge_xC_y$ layer suppressed boron penetration, it is crucial that boron still diffuse through the $Si_{1-x-y}Ge_xC_y$ so that the entire polycrystalline gate is heavily doped. This is necessary to avoid gate depletion effects for negative gate bias (inversion), which would reduce the charge in the inversion layer (and the transistor drive current). Figure 5.3 displays the quasi-static C-V curve of sample A(2) annealed for 40 minutes, which shows the same capacitance in inversion and accumulation. If depletion occurred in the gate when a negative bias was applied to the gate, the quasi-static capacitance for negative gate bias would be less than that for positive gate bias (accumulation condition on the p-type gate surface). Thus we conclude that no gate depletion effect occurs with the $Si_{1-x-y}Ge_xC_y$ layer. A smaller lower-frequency capacitance is observed in sample A(1) for negative gate voltage, which could be the result of boron penetration[14] and not gate depletion effects.

Figure 5.4 shows the boron concentration profiles analyzed by Secondary Ion Mass Spectrometry (SIMS) for sample A(1) and A(2) annealed at 900ºC, 80 minutes. Boron reached down to the top oxide interface in both sample A(1) and A(2), an





(a)

(b)

Figure 5.3: Quasi-Static Capacitance-Voltages curves of sample A(1) and A(2) annealed at 900ºC, 40 minutes.

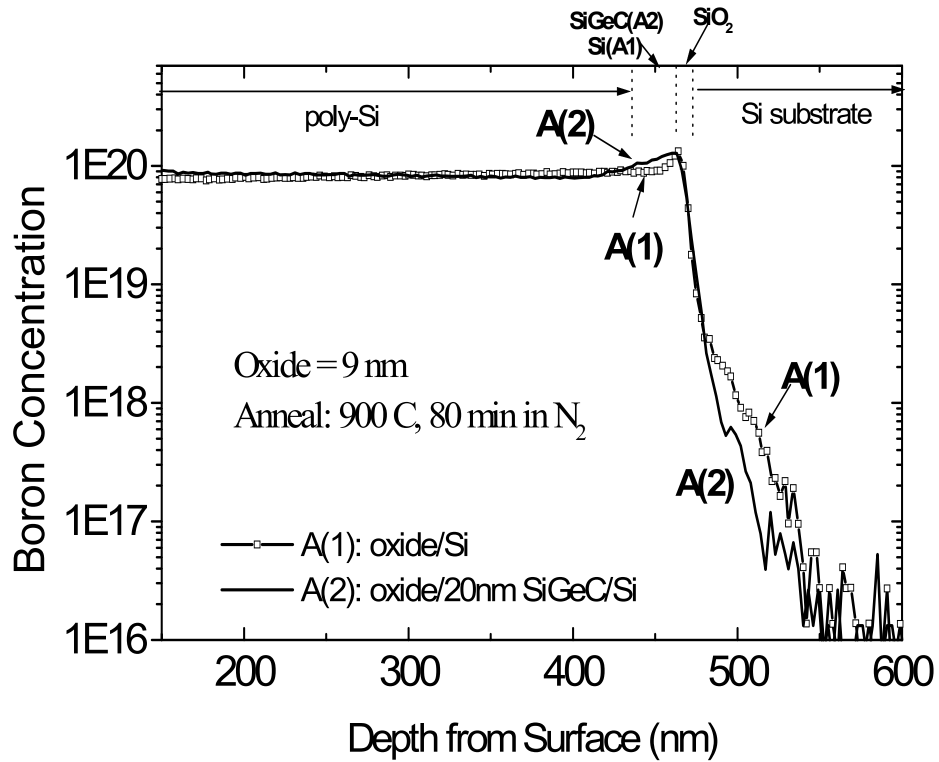


Figure 5.4: Boron profiles in sample A(1), A(2) by SIMS. Samples were BF_2^+ implanted and annealed at 900ºC for 80 minutes.

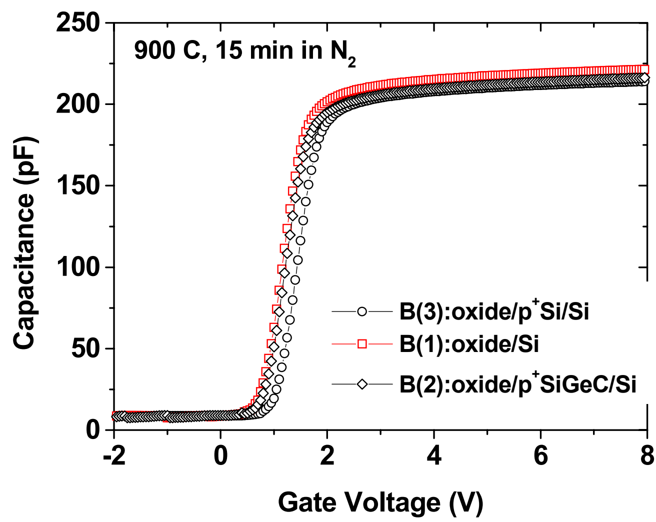
indication that boron indeed diffused through the $Si_{1-x-y}Ge_xC_y$ layer. SIMS also revealed boron penetration to the Si substrate in sample A(1) but not with the sample with the $Si_{1-x-y}Ge_xC_y$ (A(2)) intermediate layer. This is most surprising, since although $Si_{1-x-y}Ge_xC_y$ does not block boron diffusion into it, as evidenced by the SIMS result and lack of gate depletion effects, boron diffusion into the gate oxide is greatly suppressed. We also observed that fluorine piled up in gate oxides for both sample A(1) and A(2) and there is no evidence of fluorine accumulation in $Si_{1-x-y}Ge_xC_y$. Therefore, we concluded that the effect of carbon on suppressing boron penetration is not due to trapping of fluorine to reduce the boron diffusion constant in oxide. We feel that the reduction in boron penetration is due to a lower chemical potential of boron in $Si_{1-x-y}Ge_xC_y$ than in Si, which suppresses boron from diffusing into the underlying oxide. This argument is supported by the observation of a preferential boron segregation in $Si_{1-x-y}Ge_xC_y$ compared to Si, as in figure 5.4. This higher boron concentration will further reduce gate depletion effect, which shows another advantage of using polycrystalline $Si_{1-x-y}Ge_xC_y$ as part of a gate structure. Note that the apparent ability of boron to diffuse through poly-$Si_{1-x-y}Ge_xC_y$ as opposed to single crystalline $Si_{1-x-y}Ge_xC_y$ may be due to grain boundary diffusion in the polycrystalline film.

5.2.2 In-Situ Doped Polycrystalline $Si_{1-x-y}Ge_xC_y$ as an Intermediate Layer

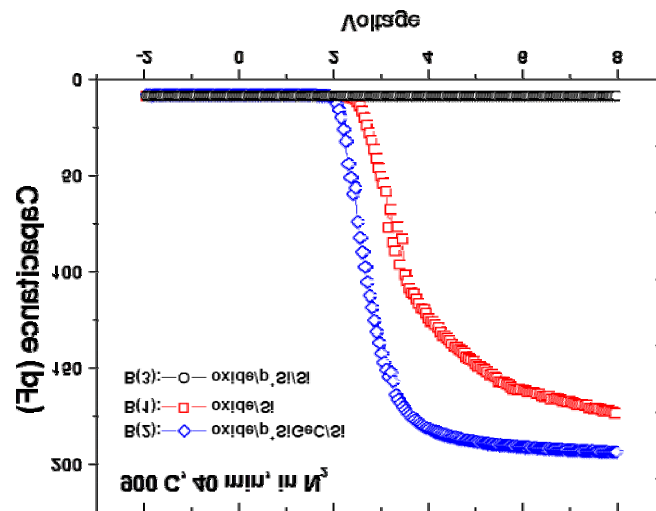
To further eliminate the possibility that poly-$Si_{1-x-y}Ge_xC_y$ suppressed boron penetration through the underlying gate oxide by blocking the incoming boron flux, we designed another set of samples (B series) in which $Si_{1-x-y}Ge_xC_y$ is in-situ doped with boron. Sample B(1) is a typical PMOS structure with ~300nm undoped polycrystalline silicon on a ~ 8nm oxide, used as a control sample. In B(2), we grew a 50nm p^+ poly-Si_{1-}

$_{x-y}Ge_xC_y$ layer between the undoped polycrystalline silicon and the gate oxide while keeping the total gate thickness unchanged. For comparison, we grew sample B(3) similar to sample B(2) except for the fact that p^+ poly-$Si_{1-x-y}Ge_xC_y$ was replaced by p^+ polycrystalline silicon. After growth, all samples were subjected to ion-implantation with $5x10^{15}/cm^2$ BF_2^+ doses at 60 keV. SIMS indicated that the boron concentration in the in-situ doped $Si_{1-x-y}Ge_xC_y$ and Si is ~$10^{21}/cm^3$, while the boron concentration is $10^{20}/cm^3$ in the initially undoped polysilicon after doping by implantation of BF_2^+ and annealing.

Figure 5.5 shows C-V curves of samples annealed at 900ºC for two different annealing times and figure 5.6 shows threshold voltage shifts as a function of various annealing conditions. It is interesting that even with $10^{21}/cm^3$ boron at the p^+ $Si_{1-x-y}Ge_xC_y$ /oxide interface, sample B(2) has a smaller threshold voltage shift than sample B(1), which has only $10^{20}/cm^3$ boron in the polycrystalline silicon after implantation and annealing. Also, for boron to penetrate across the gate oxide in sample B(1), it has to first travel through the polysilicon gate (via grain boundaries) and reach the top oxide interface. Both lower doping and a longer distance would seem to warrant less boron penetration in sample B(1), which is opposite from what was observed. This is further evidence that $Si_{1-x-y}Ge_xC_y$ suppresses boron penetration by lowering the chemical potential of boron in the gate. Figure 5.7 shows the boron concentration profiles analyzed by SIMS for sample B(2) and B(3) annealed at 900ºC, 80 minutes. A greater boron penetration is observed in sample B(3). A slightly lower boron concentration in the in-situ doped p^+ $Si_{1-x-y}Ge_xC_y$ region in B(2) than that in the in-situ doped p^+ Si region



(a)



(b)

Figure 5.5: (a) High-frequency C-V curves of implanted samples annealed at 900ºC for 15 minutes. (b) C-V curves of 40 minutes anneal.

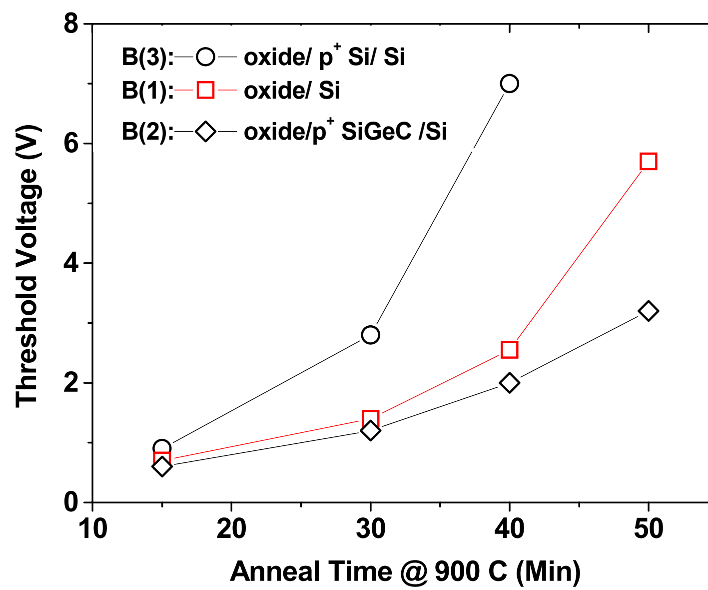


Figure 5.6: Threshold voltage as a function of annealing time.

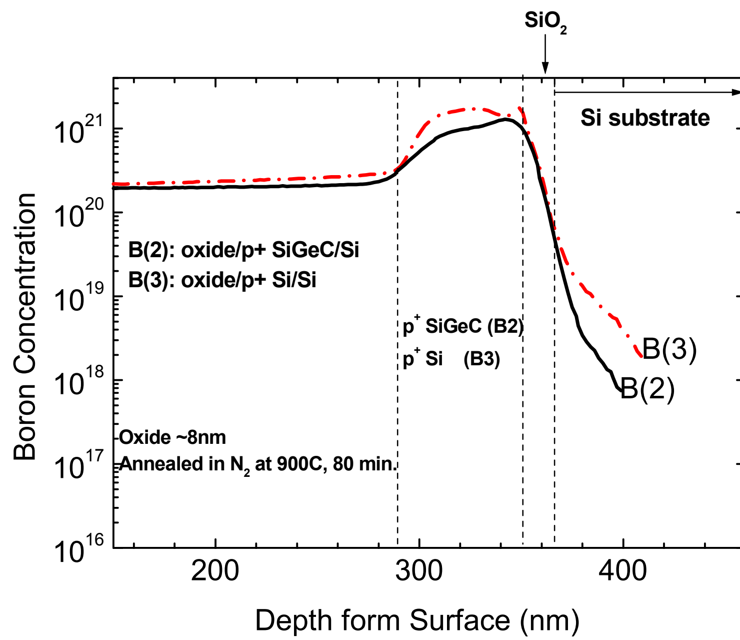


Figure 5.7: Boron profiles in sample B(2), B(3) by SIMS. Samples were BF_2^+ implanted and annealed at 900ºC for 80 minutes.

in B(3) is believed to be due to variations in doping control during the growth of the films.

5.2.3 $Si_{1-x-y}Ge_xC_y$ Intermediate layer with different Carbon Concentrations

Knowing that polycrystalline $Si_{1-x-y}Ge_xC_y$ has the largest effect in suppressing boron penetration, we study in this section how different C concentrations in $Si_{1-x-y}Ge_xC_y$ affect the suppression of boron penetration. We designed a set of samples (C series) similar to series A. The oxide thickness of samples in C series is estimated to be ~1.5nm thinner than that in series A (based on oxidation time and also consistent with the difference measured by C-V). Sample C(1) (#2290) is designed to be identical to sample A(1). Sample C(2) (#2292) has a 18nm intermediate polycrystalline $Si_{1-x-y}Ge_xC_y$ layer with 20%Ge and 0.8%C on top of the gate oxide, followed by a ~280nm polycrystalline silicon. Sample C(3) (#2291) is similar to sample C(2) except for a ~6nm polycrystalline silicon between the intermediate $Si_{1-x-y}Ge_xC_y$ and the gate oxide. Sample C(4) is similar to C(2) except for the fact that 0.4% C is incorporated in the $Si_{1-x-y}Ge_xC_y$ layer. All layers were initially undoped and subsequently doped by BF_2^+ implants under the same condition as that in series A.

Figure 5.8 shows the threshold voltage of implanted samples annealed at 900°C for different times. Even though the earlier study showed that $Si_{1-x-y}Ge_xC_y$ with y=0.6% has the strongest effect on suppressing boron penetration, the optimal effect seems to be bounded by a certain C fraction. Sample C(4) has smaller threshold voltage shifts than C(2) and C(3) in spite of a smaller C fraction. It is not clear whether there is any interstitial C in C(2) and C(3) or if the interstitial C is the cause of a less pronounced

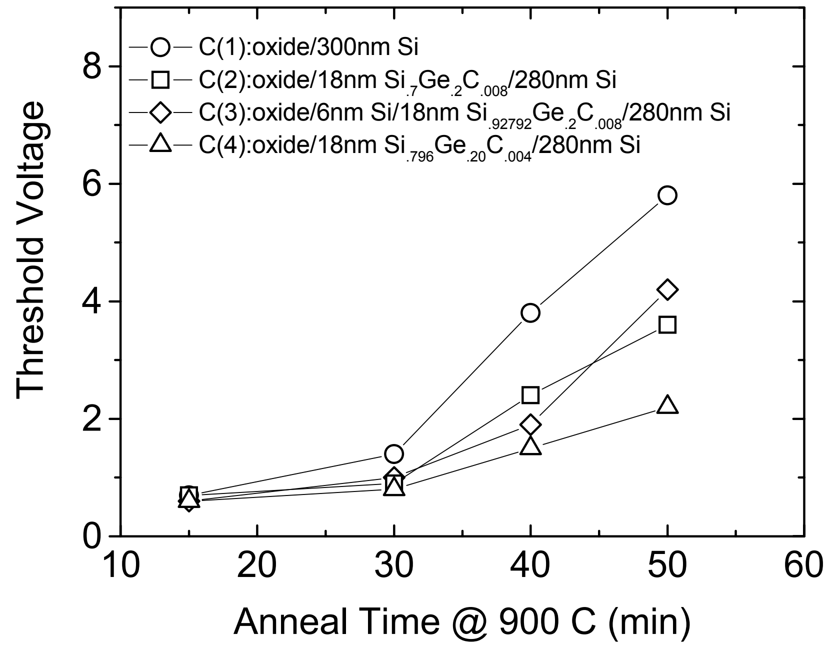


Figure 5.8: Threshold voltage as a function of annealing time.

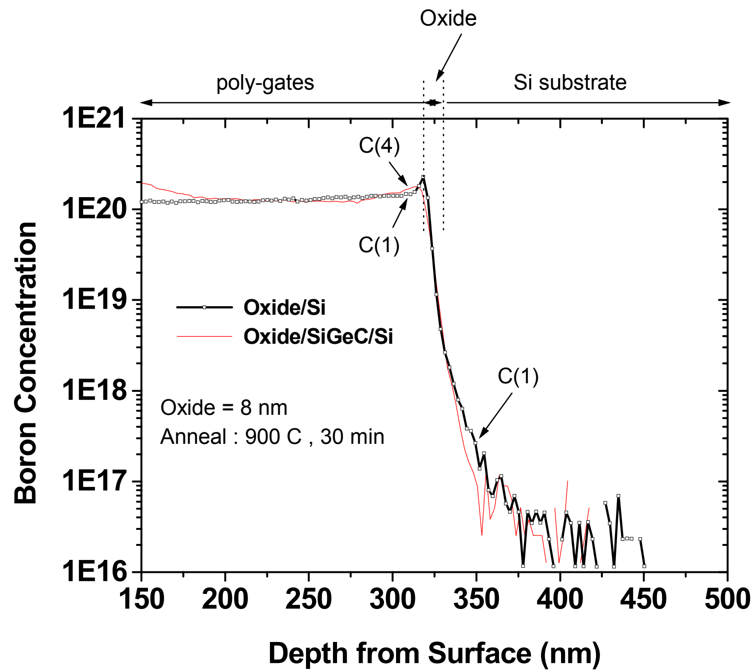


Figure 5.9: Boron profiles in sample C(1), C(4) by SIMS. Samples were BF_2^+ implanted and annealed at 900ºC for 30 minutes.

effect. The effect of 6nm-thick interfacial Si layer in C(2) is also not clear as there is no consistent trend revealed by comparing threshold voltage shifts in C(2) and C(3). We also observed higher threshold voltage shifts compared to those in A-series samples under identical annealing conditions, which may be due to thinner oxide thickness. Figure 5.9 shows the boron concentration by SIMS of sample C(1) and C(4) annealed at 900°C for 30 minutes after BF_2^+ implantation. One observed a slight boron penetration in sample C(1), consistent with a small shift in threshold voltage. We observed again slight boron segregation in the $Si_{1-x-y}Ge_xC_y$ layer.

5.2.4 In-Situ Doped Polycrystalline $Si_{1-x-y}Ge_xC_y$ as a Gate Electrode

The final set of p-type polycrystalline gates (D series) consists of five samples with four structures (two samples with the same structure)[15] with in-situ doped boron throughout the entire gates. Sample D(1) is a polycrystalline silicon gate (#2335, #2398). Sample D(2) is a polycrystalline $Si_{1-x}Ge_x$ gate (#2336). Sample D(3) (#2334) and D(4) (#2400) are polycrystalline $Si_{1-x-y}Ge_xC_y$ gates with 0.2 and 0.6% of substitutional carbon, respectively. The thickness is estimated to be ~200nm and the boron doping to be $\sim 10^{21}/cm^3$.

Figure 5.10 shows the sheet resistance of as-grown samples as well as of the annealed samples after B and BF_2^+ implantation of as-grown samples. The $Si_{1-x}Ge_x$ gate has a smaller sheet resistance than that of Si, possibly due to a larger grain size, as has been reported in the literature and the addition of C does not noticeably change the sheet

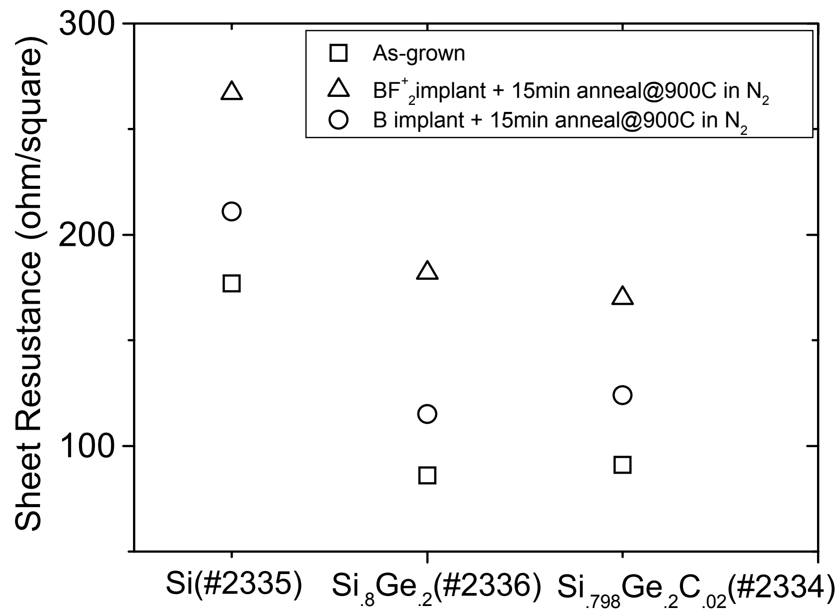


Figure 5.10: Sheet resistance of samples under various process conditions. The implant dose is $5x10^{15}$/cm2 for both B and BF_2^+, while the implant energy is 20KeV and 50KeV for B and BF_2^+, respectively.

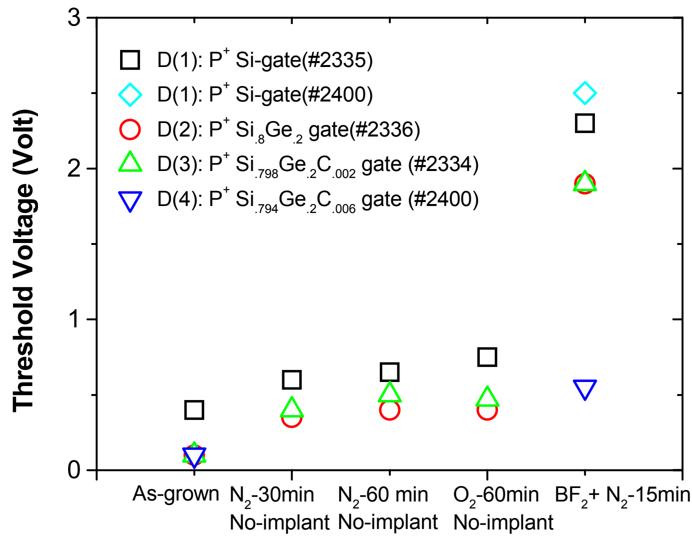


Figure 5.11: (a) Threshold voltage of in-situ doped polycrystalline gates is plotted as a function of different processing conditions. The BF_2^+ implant dose is $5 \times 10^{15}/cm^2$ and the implant energy is 50KeV.

resistance. By implanting B and BF_2^+ ($5x10^{15}/cm^2$) into the in-situ doped samples and annealing the implanted samples, the sheet resistance increased. Since the in-situ doped samples have already $\sim10^{21}/cm^3$, we suspect that the increase in sheet resistance is probably due to scattering caused by interstitial boron or boron clusters.

Thermal annealing of in-situ doped samples (no ion-implantation) in N_2 at 900ºC for up to 1 hr showed no evidence of boron penetration (see figure 5.11), which is expected due to a lower boron diffusivity in oxide without the presence of fluorine (~20 times lower at 900ºC)[16]. There was also no evidence of boron penetration when samples were subject to heat treatment in O_2 at 900ºC for 1 hr (also see figure 5.11(a)), which suggests that the boron penetration is not significantly affected by the injected Si interstitials from the oxidizing surface.

To observe the boron penetration effect, these in-situ samples were subjected to BF_2^+ implantation and post-implantation anneal. Threshold voltage shifts were observed for samples after BF_2^+ implantation and post-implantation anneal, as shown in figure 5.11. We also observed a much more pronounced effect when C was increased from 0.2% to 0.6%. Based on data from this study and previous study in this chapter, it appears that the strongest effect by C is for concentrations between 0.4%-0.6%C.

In order to observe boron penetration without the aid of BF_2^+ implantation, we annealed D(1) (#2398) and D(4) at 900 ºC for 20 hrs in N_2, with their high-frequency C-V curves shown in figure 5.12. The threshold voltage shifted by ~1V in D(1) while no normal C-V curve was obtained for D(4). It is not clear based on the C-V curves if there is any boron penetration in D(4). However, a large capacitance at negative bias suggested the presence of defects. The formation of C cluster or SiC compound has been reported when $Si_{1-x-y}Ge_xC_y$ or $Si_{1-y}C_y$ were annealed at 900º for a few hours. The C-

related defects may be the cause of the abnormal C-V curve. Figure 5.13 shows the boron concentration by SIMS of sample D(1) (#2398) and D(4) annealed at 900°C for 22 hrs in N_2. Due to thickness variations in the polycrystalline layer thickness, the oxide/poly interface has been aligned in the presentation of SIMS data.. It is not clear if there is more boron penetration in D(4) since the boron tails of D(1) and D(4) have different slopes which make comparison difficult.

5.2.5 Hydrogen Annealing Effects of In-Situ Doped Polycrystalline $Si_{1-x-y}Ge_xC_y$

It was reported that the reaction of oxide with hydrogen reduced the density of trapping states for boron through removing unsaturated silicon or oxygen bonds[17]. As a result, boron becomes more mobile in oxide due to the passivation of dangling bonds. We therefore experimented with thermal anneal of D(1) (#2398) and D(4) (without ion-implantation) in forming gas at 900ºC for shorter time for evidence of boron penetration. Figure 5.14 shows high-frequency C-V curves of both D(1) and D(4). Hydrogen-enhanced boron penetration was evident for both D(1) and D(4) as we observed higher threshold voltage shifts compared to those in an N_2 anneal for the same annealing time and temperature. Moreover, unlike the previous results in this chapter, we observed more threshold voltage shift in $Si_{1-x-y}Ge_xC_y$ gate than that in Si gate. We note that SIMS analysis is needed for direct evidence of boron penetration. It is not clear why hydrogen induced more boron penetration in the $Si_{1-x-y}Ge_xC_y$ gate than that in Si. Further investigation is required to study possible interaction of hydrogen and carbon, such as possible hydrogen-induced out-diffusion of C from lattice sites.

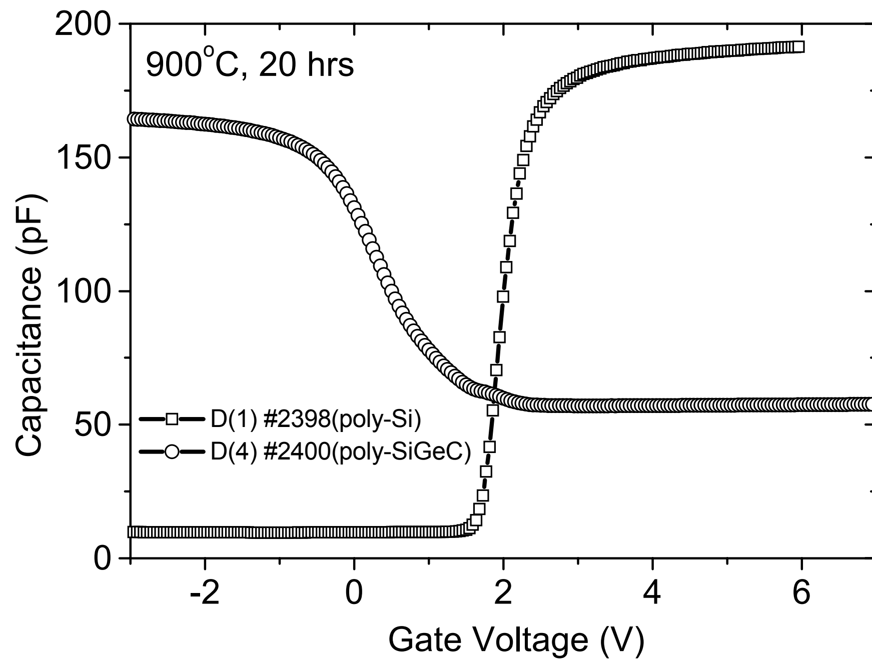


Figure 5.12: High-frequency C-V curves of samples D(1) and D(4). Samples were annealed at 900ºC for 20 hrs in N_2.

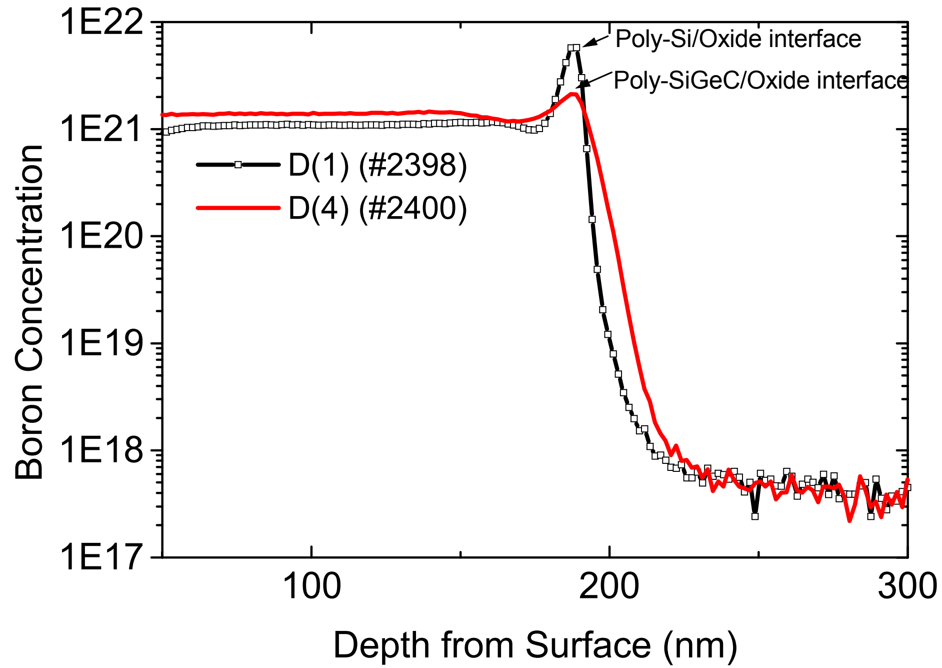
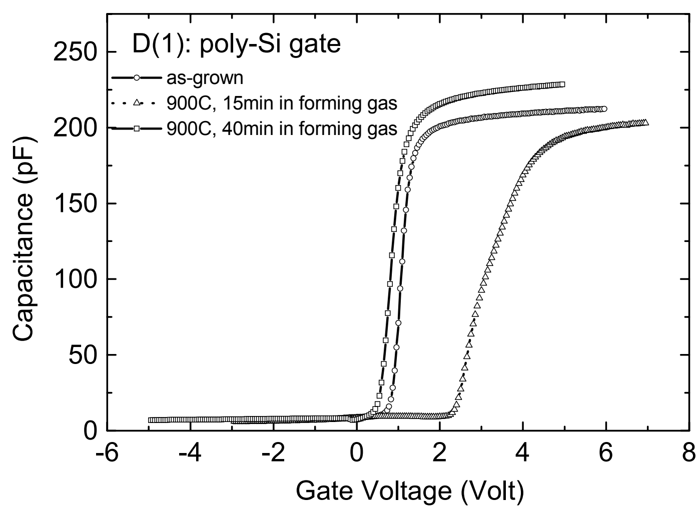
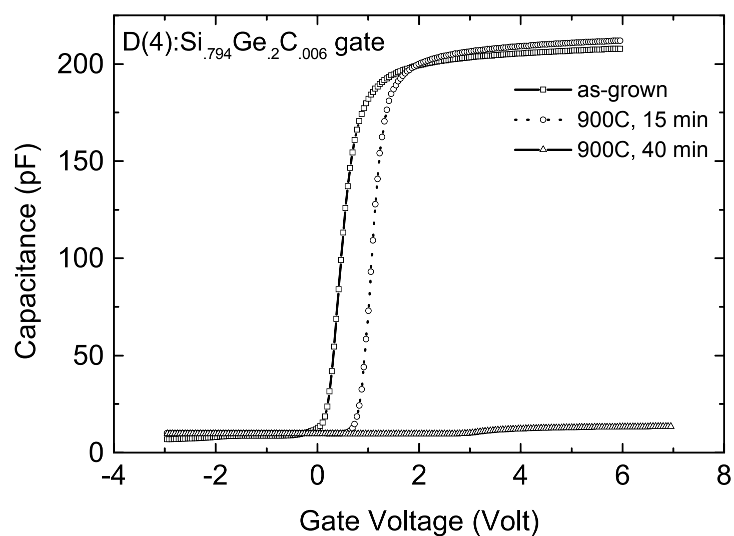


Figure 5.13: Boron profiles in sample D(1) and D(4) by SIMS. Samples were annealed at 900ºC for 22 hrs. Note different slopes of the tails of boron profiles, which make comparison difficult.



(a)

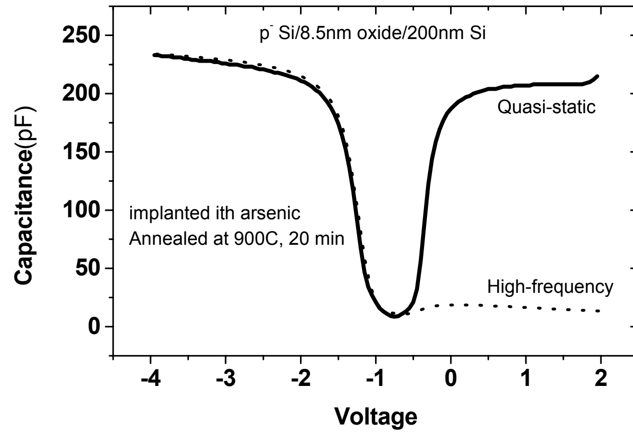


(b)

Figure 5.14: High-frequency C-V curves of (a) sample D(1), (b) sample D(4) annealed in forming gas at 900ºC.

5.3 Polycrystalline $Si_{1-x-y}Ge_xC_y$ in NMOS Devices: Toward "Dual-Gate" Processing

To apply polycrystalline $Si_{1-x-y}Ge_xC_y$ into a dual-gate CMOS process, a simple polycrystalline layer is used for both p-channel and n-channel devices. In the previous section we have focused on the effect of $Si_{1-x-y}Ge_xC_y$ on suppressing boron penetration that would occur in PMOS devices. In this section, we briefly examine n^+ implanted structures to make sure no deleterious effect of $Si_{1-x-y}Ge_xC_y$ on n-channel devices. Specifically, we need to ensure that the n-type dopant can penetrate the $Si_{1-x-y}Ge_xC_y$ layer so that no gate depletion effects on the NMOS devices occur. Therefore, we have fabricated NMOS capacitors on a thermally oxidized p^- silicon substrate with gate structures (E(1) and E(2)) similar to A(1) and A(2). NMOS gates were doped by arsenic implantation and post-implantation anneal. The quasi-static C-V curve in figure 5.15 displays no gate depletion when $Si_{1-x-y}Ge_xC_y$ was part of the gate structure (E(2)). Evidence of gate depletion for the n-type gates would be a low quasi-static capacitance for positive gate bias. In contrast, a slighly less capacitance under positive gate bias was observed in the traditional NMOS with all polysilicon (E(1)) after 900°C anneal for 20 minutes. It may suggest that there is a slight gate depletion in E(1), although more studies are needed. Unfortunately, we were unable to obtain quasi-static C-V curves of those samples with longer annealing times, although the reasons are uncertain.



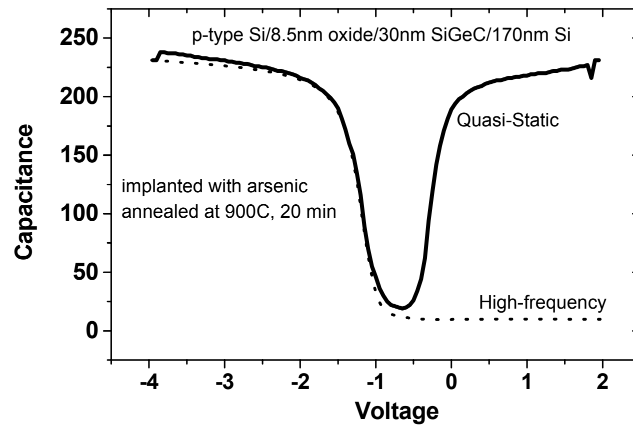


Figure 5.15: Quasi-Static Capacitance-Voltages curves of NMOS capacitors. No gate depletion was observed when $Si_{1-x-y}Ge_xC_y$ was used.

We conclude that arsenic can at least diffuse across through the $Si_{1-x-y}Ge_xC_y$ layer without extra difficulty. Therefore, in principle polycrystalline $Si_{1-x-y}Ge_xC_y$ can be incorporated into today's "dual-gate" CMOS processing.

5.4 Discussion

As discussed earlier, we think the mechanism by which polycrystalline $Si_{1-x-y}Ge_xC_y$ suppresses boron penetration is a lowering of the chemical potential of boron compared to that of boron in polycrystalline silicon or polycrystalline $Si_{1-x}Ge_x$. This argument is supported by the observation of the boron segregation in $Si_{1-x-y}Ge_xC_y$. Hu *et al* laid a theoretical framework for describing dopant segregation in strained $Si_{1-x}Ge_x$/Si(100) heterostructures through the concept of chemical potential of dopant[18]. The chemical potential of dopant was derived from mainly two contributions, i.e., the configurational entropy and the electronic energy. In addition, the strain energy of compressively strained $Si_{1-x}Ge_x$ also needs to be taken into account. By adding boron into strained $Si_{1-x}Ge_x$, there is added configurational entropy due to the mixture of Si, Ge and B. Therefore, boron prefers to stay in $Si_{1-x}Ge_x$ than in Si. The electronic energy of boron in $Si_{1-x}Ge_x$ is also reduced compared to that in Si due to higher valence band edge (hence lower hole energy) of hole accompanying each B in the $Si_{1-x}Ge_x$. Therefore, electronic energy also predicted preferred boron segregation in $Si_{1-x}Ge_x$ than that in Si. Finally, the strain energy of compressively strained $Si_{1-x}Ge_x$ is reduced with a smaller boron atom occupying the Si lattice site, another driving force for boron segregation in $Si_{1-x}Ge_x$.

In the polycrystalline $Si_{1-x}Ge_x$ gate, a similar argument can be made to predict the boron segregation in polycrystalline $Si_{1-x}Ge_x$ (except the strain energy argument if the polycrystalline is unstrained). This prediction was confirmed by observing that with the addition of polycrystalline $Si_{1-x}Ge_x$ gate, the problem of boron penetration is improved, as shown in figure 5.2.

It is not clear how this argument can be applied to that in polycrystalline $Si_{1-x-y}Ge_xC_y$ gate. Even though the addition of C increased the configurational entropy, the effect should be evident with the initial addition of a small amount of C. However, no significant effect was observed, as seen in figure 5.11 with 0.02% C in the $Si_{1-x-y}Ge_xC_y$ gate. In addition, the net effect of C on the band structure of $Si_{1-x}Ge_x$ is small, as described in chapter 2. Moreover, we observed in figure 5.8 that adding more C does not necessarily enhance the effect on suppressing boron penetration. The argument of strain energy reduction does not apply to polycrystalline $Si_{1-x-y}Ge_xC_y$ either. Even assuming that a $Si_{1-x-y}Ge_xC_y$ grain is partially strained, the strain condition does not provide more driving force compared to that of $Si_{1-x}Ge_x$ for boron to segregate.

We are unable to explain why polycrystalline $Si_{1-x-y}Ge_xC_y$ lowers the chemical potential of boron at this point. However, we like to note a very recent study by Carroll in our lab, which shows preferred boron segregation to polycrystalline $Si_{1-x-y}Ge_xC_y$ in polycrystalline $Si_{1-x-y}Ge_xC_y/Si_{1-x}Ge_x$ supperlattices. The segregation is enhanced when more C is added up to 0.5% C, consistent with our results shown in this chapter.

Finally, we do not know why the annealing in hydrogen gas destroyed the beneficial effect of $Si_{1-x-y}Ge_xC_y$ on suppressing boron penetration. More study is needed, such as annealing samples of A series in forming gas and performing SIMS analysis, to verify the effect of hydrogen. Furthermore, we need to examine the role of interstitial C

and investigate if the existence of interstitial C has any detrimental effect, such as what we observed in A(4) (or possibly C(2) and C(3)).

5.5 Summary

We have used polycrystalline $Si_{1-x-y}Ge_xC_y$ as part of a polycrystalline gate structure to study the effect on boron penetration across gate oxide. Although boron readily penetrated through the $Si_{1-x-y}Ge_xC_y$ and accumulated in it, boron penetration across the gate oxide into the substrate was greatly suppressed compared to that in structures without $Si_{1-x-y}Ge_xC_y$ layer. Our work suggests that the addition of carbon reduced the chemical potential of boron in polycrystalline $Si_{1-x-y}Ge_xC_y$, compared to that in polycrystalline silicon or polycrystalline $Si_{1-x}Ge_x$. We have also observed no gate depletion effects with the use of poly-$Si_{1-x-y}Ge_xC_y$ in both PMOS and NMOS gates. It indicates that polycrystalline $Si_{1-x-y}Ge_xC_y$ is attractive for "dual-gate" CMOS processing.

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[15] Initially, we designed #2334, #2335, and #2336 with the same gate oxide thickness and expected that #2334 with only 0.02%C to have a significant effect. However, results showed that #2334 had only a small effect. We therefore fabricated #2400 (0.6%C) in anticipation of a stronger effect. Concerned about variations of gate oxide thickness, we oxidized #2398 and #2400 at the same time and grew the same poly-gate in #2398 as that in #2335. As a result, we have two samples for D(1) structure.

[16] Based on figures in ref(5).

[17] See ref (5) and ref (6). Also references therein.

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Chapter 6

Conclusion

6.1 Summary

We began this thesis by investigating the effect of C on the compressively strained $Si_{1-x-y}Ge_xC_y$/Si (100) heterostructures. We found that the effect of C on the still compressively strained $Si_{1-x-y}Ge_xC_y$ /Si (100) is small, with the valence band offset reduced by ~25 meV/%C. The reduction in the valence band offset is consistent with the increase in the bandgap of strained $Si_{1-x-y}Ge_xC_y$. The resulting band structure of compressively strained $Si_{1-x-y}Ge_xC_y$ /Si (100) is similar to that of strained $Si_{1-x}Ge_x$/ Si (100), with most of the band gap difference accommodated in the valence band and a negligible conduction band offset. By combining this experiment result with others, we proposed a simple model to predict the band alignment of strain $Si_{1-x-y}Ge_xC_y$/Si, $Si_{1-y}C_y$/Si as well as unstrained $Si_{1-x-y}Ge_xC_y$/Si and compared out predictions with experimental numbers.

With the understanding of band alignment, we fabricated a modulation doped $Si_{1-x-y}Ge_xC_y$/Si (100) and observed a two-dimensional hole gas in the strained $Si_{1-x-y}Ge_xC_y$ channel. Even though the hole effective mass is not changed with the C incorporation, the hole mobility decreased with the addition of C. It suggests that the decrease in hole mobility may be due to non-substitutional C related defects besides an increased alloy scattering.

In the second part of this thesis, we extend the use $Si_{1-x-y}Ge_xC_y$ towards potential application in current CMOS processing. By growing polycrystalline $Si_{1-x-y}Ge_xC_y$ and incorporated it as part of a polycrystalline gate electrode, we were able to suppress boron

penetration across the thin gate oxide in the PMOS devices. We think that polcrystalline $Si_{1-x-y}Ge_xC_y$ lowers the chemical potential of boron, which prevents it from diffusing through the underlying gate oxide.

6.2 Directions for future work

The fundamental research on $Si_{1-x-y}Ge_xC_y$ has evolved from growing compressively strained $Si_{1-x-y}Ge_xC_y$ with C compensating strain caused by Ge to studying band structures of tensile-strained $Si_{1-y}C_y$, $Si_{1-x-y}Ge_xC_y$ as well as strain-free $Si_{1-x-y}Ge_xC_y$. We have proposed a model to predict the band alignments of these materials with underlying Si substrate and compared our predictions with recently reported numbers.

By tuning the band structures of the Si-based epitaxial materials through strain manipulation and employing the intrinsic (chemical) effect of C and Ge, Si-based band structure engineering can produce materials for potential device applications. For example, based on the conduction and valence band offset of the epitaxial materials to Si, modulation doped field effect transistors can be realized. Moreover, based on our prediction, band structure engineering is also possible on the strain-free $Si_{1-x-y}Ge_xC_y$/Si system. It is important since a strain-free $Si_{1-x-y}Ge_xC_y$/Si with a tunable band structure can avoid the problem of stain relaxation (and generation of dislocations) during heat cycles in device processing

The key issue to realizing these potential applications is the ability to grow these materials with high material quality. This is no easy task since thermodynamics favors SiC formation instead of alloys. Thus more efforts are needed to study the growth of these materials.

In the area of C suppressing boron penetration in PMOS devices, how C lowers the chemical potential of boron is still not understood? Moreover, how would the chemical potential of C change with the presence of hydrogen.

Finally, more studies are needed to study the thermal stability of C in the Si and $Si_{1-x}Ge_x$ matrix. In order to apply these potential applications into practical use, we have to understand the process window of these materials. Moreover, how would the properties of these materials change after thermal processing requires more studies on this subject.

A.1 p^+ $Si_{1-x-y}Ge_xC_y$ / p^- Si #1946

Sequencer Table #0

Step #	Action	Comment
0	CONTROL ON&	Turn on Control
1	SCAN ON(0.3)&	and Scan simultaneously
2	SET(SP7,0)&	Override power to zero
3	SET(SP4,0)&	Turn off PID control
4		
5	SET(DO0,1)&	N2 off
6	SET(DO1,0)&	H2 off
7	SET(DO2,1)&	GeH4 select on
8	SET(DO3,0)&	SiH4 off
9	SET(DO4,1)&	B2H6 select on
10	SET(DO5,0)&	PH3 off
11	SET(DO6,1)&	X on
12	SET(DO7,1)&	DCS on
13	SET(DO8,0)&	SiCH6 off
14	SET(DO9,0)&	GeH4 inject off
15	SET(DO10,0)&	SiH4 off
16	SET(DO11,0)&	B2H6 off
17	SET(DO12,0)&	PH3 off
18	SET(DO13,0)&	Source off
19	SET(AO0,0.617)&	H2 flow = 3 slpm
20	SET(DO15,1)	Vacuum on
21	SET(DO1,1)&	H2 on
22	SET(AO1,0.212)&	GeH4 flow = 100 sccm
23	SET(AO2,0.01)&	SiH4
24	SET(AO3,0.9)&	B2H6 flow = 450 sccm
25	SET(AO4,0.01)&	PH3 high
26	SET(AO5,0.01)&	PH3 low
27	SET(AO6,0.537)&	DCS flow = 26 sccm
28	SET(AO7,0.165)	SiCH6 flow = 15 sccm
29	SET(AO8,0.0)	Pressure = 0
30	SEQUENCER ON(0.3,1,0)	Start Sequencer #1
31		

Sequencer Table #1

Step #	Action	Comment
0		
1	SET(SP2,0.0)&	Reset loop control
2	SEQUENCER ON(0.3,6,0)	Call cleaning sequence
3	WAITUNTIL(SP2>0.5)	Cleaning sequence
4	SET(SP2,0.0)&	Reset loop control
5		
6	SEQUENCER ON(0.3,5,0)	Call buffer sequence
7	WAITUNTIL(SP2>0.5)	Buffer sequence
8	SET(SP2,0.0)	Reset loop control
9	SET(SP5,3.5)	T=700C
10	SET(SP4,1.0)	Feedback on
11	WAIT(60)	
12	SEQUENCER ON(0.3,4,0)	Call $Si_{1-x-y}Ge_xC_y$/Si sequence
13	WAITUNTIL(SP2>0.5)	$Si_{1-x-y}Ge_xC_y$ /Si sequence
14	SET(SP2,0.0)&	Reset loop control
15		
16	SET(SP4,0.0)&	Feedback off
17		
18		
19	RAMP(SP7,-0.4,0.0)&	Lamps down to zero
20		
21		
22		
23		
24		
25		
26	SEQUENCER ON(0.3,7,0)&	Call reload sequence
27		
28		
29		
30		
31		

Sequencer Table #4

Step #	Action	Comment
0	SET(SP5,1.92)	Set T = 575C
1	WAIT(60)	Stabilize temperature
2	SET(DO13,0)	DCS inject off
3		SiCH6 already selected
4		
5	WAIT(10)	Open manual SiCH6 inject
6		
7	SET(DO13,1)&	Inject DCS and SiCH6
8	SET(DO9,1)	Inject GeH4
9	WAIT(30)	Undoped $Si_{1-x-y}Ge_xC_y$
10	SET(DO11,1)	Inject B2H6
11	WAIT(195)	P^+ $Si_{1-x-y}Ge_xC_y$ layer
12	SET(DO9,0)	GeH4 inject off
13		Close SiCH6 manual valve
14	SET(AO3,0.8)	B2H6 400 sccm
15	WAIT(20)	
16	SET(DO2,0)	GeH4 select off
17		
18		
19		
20		
21		
22	SET(SP5,3.31)	T = 675C
23	WAIT(1200)	Si cap
24	SET(DO13,0)	DCS inject off
25	SET(DO7,0)	DCS select off
26	SET(DO11,0)	B2H6 inject off
27	SET(DO4,0)	B2H6 select off
28	SET(SP2,1.0)	Set loop control
29	END	
30		
31		

Sequencer Table #5

Step #	Action	Comment
0	WAITUNTIL(AI29<10)	Pumping out
1	WAITUNTIL(AI24>0.5)	GO for buffer
2	SET(AO11,1.0)&	Low pressure select
3	WAITUNTIL(AI28<5.5)	Pressure stabilizing
4	SET(AO8,0.60)&	Set P=6torr
5	WAITUNTIL(AI28>5.5)	Pressure stabilizing
6		
7		
8		
9	SET(DO13,1)&	Inject DCS
10	SET(DO11,1)	Inject B2H6
11	WAIT(450)	Buffer I
12	SET(DO13,0)&	DCS inject off
13	SET(DO11,0)	B2H6 inject off
14		
15	RAMP(SP7,-0.4,0.0)	Lamps off
16		
17		
18	WAITUNTIL(AI24>0.5)	GO for cold values
19	SET(SP3,1)	Get cold values
20	WAIT(1)	
21	SET(SP3,0)	Latch cold values
22		
23	RAMP(SP7,0.4,0.2)	Reheat wafer
24	WAIT(60)	Clean
25		
26		
27	SET(DO13,1)	Inject DCS
28	WAIT(60)	Buffer II
29	RAMP(SP7,-0.4,0.17)	Lamps down to 17%
30	WAIT(30)	Si at 17%
31	SET(SP2,1.0)	Set loop control

Sequencer Table #6

Step #	Action	Comment
0	WAITUNTIL(AI24>0.5)	GO for clean
1	SET(AO11,0)&	High pressure select
2	SET(AO8,0.250)&	P=250torr
3	SET(AO0,0.817)&	H2 flow=4slpm
4	WAITUNTIL(AI29>$250)	Pressure stabilizing
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
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22		
23		
24		
25		
26		
27	RAMP(SP7,0.4.0.274)	Lamps to 1000C
28	WAIT(120)	Clean
29	SET(AO8,0.0)	Pump out
30	SET(AO0,0.617)&	H2 flow=3slpm
31	SET(SP2,1.0)&	Set loop control

Sequencer Table #7

Step #	Action	Comment
0	SET(SP7,0)	Lamps off
1	SET(DO13,0)&	DCS inject off
2	SET(DO12,0)&	PH3 off
3	SET(DO11,0)&	B2H6 off
4	SET(DO10,0)&	SiH4 off
5	SET(DO9,0)&	GeH4 off
6	SET(DO7,0)&	DCS select off
7	SET(DO5,0)&	PH3 off
8	SET(DO4,0)&	B2H6 off
9	SET(DO3,0)&	SiH4 off
10	SET(DO2,0)&	GeH4 off
11	SET(DO1,0)&	H2 off
12	SET(AO8,0.0)&	Pump out
13	SET(AO7,0.0)&	B2H6 low
14	SET(AO6,0.0)&	DCS
15	SET(AO5,0.0)&	PH3 low
16	SET(AO4,0.0)&	PH3 high
17	SET(AO3,0.0)&	B2H6 high
18	SET(AO2,0.0)&	SiH4
19	SET(AO1,0.0)&	GeH4
20	SET(AO0,0.00)	H2
21	WAITUNTIL(AI28<0.5)	Pump out
22	SET(DO15,0)&	Vacuum off
23		
24	SEQUNCER OFF(0)	Sequencer 0 off
25	SEQUNCER OFF(1)	Sequencer 1 off
26	SEQUNCER OFF(2)	Sequencer 2 off
27	SEQUNCER OFF(3)	Sequencer 3 off
28	SEQUNCER OFF(4)	Sequencer 4 off
29	SEQUNCER OFF(5)	Sequencer 5 off
30	SEQUNCER OFF(6)	Sequencer 6 off
31	SEQUNCER OFF(7)	Sequencer 7 off

A.2 $Si_{1-x-y}Ge_xC_y$ /Si Modulation-Doped Structure #2110

Sequencer Table #0

Step #	Action	Comment
0	CONTROL ON&	Turn on Control
1	SCAN ON(0.3)&	and Scan simultaneously
2	SET(SP7,0)&	Override power to zero
3	SET(SP4,0)&	Turn off PID control
4		
5	SET(DO0,1)&	N2 off
6	SET(DO1,0)&	H2 off
7	SET(DO2,1)&	GeH4 select on
8	SET(DO3,0)&	SiH4 off
9	SET(DO4,1)&	B2H6 select on
10	SET(DO5,0)&	PH3 off
11	SET(DO6,1)&	X on
12	SET(DO7,1)&	DCS on
13	SET(DO8,0)&	SiCH6 off
14	SET(DO9,0)&	GeH4 inject off
15	SET(DO10,0)&	SiH4 off
16	SET(DO11,0)&	B2H6 off
17	SET(DO12,0)&	PH3 off
18	SET(DO13,0)&	Source off
19	SET(AO0,0.617)&	H2 flow = 3 slpm
20	SET(DO15,1)	Vacuum on
21	SET(DO1,1)&	H2 on
22	SET(AO1,0.212)&	GeH4 flow = 100 sccm
23	SET(AO2,0.01)&	SiH4
24	SET(AO3,0.04)&	B2H6 flow = 20 sccm
25	SET(AO4,0.01)&	PH3 high
26	SET(AO5,0.01)&	PH3 low
27	SET(AO6,0.537)&	DCS flow = 26 sccm
28	SET(AO7,0.08)	SiCH6 flow = 6.7 sccm
29	SET(AO8,0.0)	Pressure = 0
30	SEQUENCER ON(0.3,1,0)	Start Sequencer #1
31		

Sequencer Table #1

Step #	Action	Comment
0		
1	SET(SP2,0.0)&	Reset loop control
2	SEQUENCER ON(0.3,6,0)	Call cleaning sequence
3	WAITUNTIL(SP2>0.5)	Cleaning sequence
4	SET(SP2,0.0)&	Reset loop control
5		
6	SEQUENCER ON(0.3,5,0)	Call buffer sequence
7	WAITUNTIL(SP2>0.5)	Buffer sequence
8	SET(SP2,0.0)	Reset loop control
9	SET(SP5,3.5)	T=700C
10	SET(SP4,1.0)	Feedback on
11	WAIT(60)	
12	SEQUENCER ON(0.3,4,0)	Call $Si_{1-x-y}Ge_xC_y/Si$ sequence
13	WAITUNTIL(SP2>0.5)	$Si_{1-x-y}Ge_xC_y/Si$ sequence
14	SET(SP2,0.0)&	Reset loop control
15		
16	SET(SP4,0.0)&	Feedback off
17		
18		
19	RAMP(SP7,-0.4,0.0)&	Lamps down to zero
20		
21		
22		
23		
24		
25		
26	SEQUENCER ON(0.3,7,0)&	Call reload sequence
27		
28		
29		
30		
31		

Sequencer Table #4

Step #	Action	Comment
0	SET(SP5,1.92)	Set T = 575C
1	WAIT(30)	Stabilize temperature
2	SET(DO13,0)	DCS inject off
3		SiCH6 already selected
4		
5	WAIT(10)	Open manual SiCH6 inject
6		
7	SET(DO13,1)&	Inject DCS and SiCH6
8	SET(DO9,1)	Inject GeH4
9	WAIT(900)	Undoped $Si_{1-x-y}Ge_xC_y$
10		
11		
12	SET(DO9,0)	GeH4 inject off
13		Close SiCH6 manual valve
14		
15	WAIT(30)	
16	SET(DO2,0)	GeH4 select off
17	SET(SP5,3.51)	T=700C
18	WAIT(100)	Undoped Si spacer
19	SET(DO11,1)	Inject B2H6
20	WAIT(100)	Dopant supply layer
21	SET(DO11,0)	
22	WAIT(1200)	Si
23	SET(AO3,0.02)	10sccm B2H6
24	SET(DO11,1)	Inject B2H6
25	WAIT(200)	Shielding layer
26	SET(DO11,0)&	B2H6 inject off
27	SET(DO13,0)	DCS inject off
28	SET(SP2,1.0)	Set loop control
29	END	
30		
31		

Sequencer Table #5

Step #	Action	Comment
0	WAITUNTIL(AI29<10)	Pumping out
1	WAITUNTIL(AI24>0.5)	GO for buffer
2	SET(AO11,1.0)&	Low pressure select
3	WAITUNTIL(AI28<5.5)	Pressure stabilizing
4	SET(AO8,0.60)&	Set P=6torr
5	WAITUNTIL(AI28>5.5)	Pressure stabilizing
6		
7		
8		
9	SET(DO13,1)&	Inject DCS
10	SET(DO11,1)	Inject B2H6
11	WAIT(300)	Buffer I
12	SET(DO13,0)&	DCS inject off
13	SET(DO11,0)	B2H6 inject off
14		
15	RAMP(SP7,-0.4,0.0)	Lamps off
16		
17		
18	WAITUNTIL(AI24>0.5)	GO for cold values
19	SET(SP3,1)	Get cold values
20	WAIT(1)	
21	SET(SP3,0)	Latch cold values
22		
23	RAMP(SP7,0.4,0.2)	Reheat wafer
24	WAIT(30)	Clean
25		
26		
27	SET(DO13,1)	Inject DCS
28	WAIT(30)	Buffer II
29	RAMP(SP7,-0.4,0.16)	Lamps down to 16%
30	WAIT(60)	Si at 16%
31	SET(SP2,1.0)	Set loop control

Sequencer Table #6

Step #	Action	Comment
0	WAITUNTIL(AI24>0.5)	GO for clean
1	SET(AO11,0)&	High pressure select
2	SET(AO8,0.250)&	P=250torr
3	SET(AO0,0.817)&	H2 flow=4slpm
4	WAITUNTIL(AI29>$250)	Pressure stabilizing
5		
6		
7		
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24		
25		
26		
27	RAMP(SP7,0.4.0.274)	Lamps to 1000C
28	WAIT(120)	Clean
29	SET(AO8,0.0)	Pump out
30	SET(AO0,0.617)&	H2 flow=3slpm
31	SET(SP2,1.0)&	Set loop control

Sequencer Table #7

Step #	Action	Comment
0	SET(SP7,0)	Lamps off
1	SET(DO13,0)&	DCS inject off
2	SET(DO12,0)&	PH3 off
3	SET(DO11,0)&	B2H6 off
4	SET(DO10,0)&	SiH4 off
5	SET(DO9,0)&	GeH4 off
6	SET(DO7,0)&	DCS select off
7	SET(DO5,0)&	PH3 off
8	SET(DO4,0)&	B2H6 off
9	SET(DO3,0)&	SiH4 off
10	SET(DO2,0)&	GeH4 off
11	SET(DO1,0)&	H2 off
12	SET(AO8,0.0)&	Pump out
13	SET(AO7,0.0)&	B2H6 low
14	SET(AO6,0.0)&	DCS
15	SET(AO5,0.0)&	PH3 low
16	SET(AO4,0.0)&	PH3 high
17	SET(AO3,0.0)&	B2H6 high
18	SET(AO2,0.0)&	SiH4
19	SET(AO1,0.0)&	GeH4
20	SET(AO0,0.00)	H2
21	WAITUNTIL(AI28<0.5)	Pump out
22	SET(DO15,0)&	Vacuum off
23		
24	SEQUNCER OFF(0)	Sequencer 0 off
25	SEQUNCER OFF(1)	Sequencer 1 off
26	SEQUNCER OFF(2)	Sequencer 2 off
27	SEQUNCER OFF(3)	Sequencer 3 off
28	SEQUNCER OFF(4)	Sequencer 4 off
29	SEQUNCER OFF(5)	Sequencer 5 off
30	SEQUNCER OFF(6)	Sequencer 6 off
31	SEQUNCER OFF(7)	Sequencer 7 off

A.3 #2251

Sequencer Table #0

Step #	Action	Comment
0	CONTROL ON&	Turn on Control
1	SCAN ON(0.3)&	and Scan simultaneously
2	SET(SP7,0)&	Override power to zero
3	SET(SP4,0)&	Turn off PID control
4		
5	SET(DO0,1)&	N2 off
6	SET(DO1,0)&	H2 off
7	SET(DO2,1)&	GeH4 select on
8	SET(DO3,1)&	SiH4 select on
9	SET(DO4,0)&	B2H6 off
10	SET(DO5,0)&	PH3 off
11	SET(DO6,1)&	X on
12	SET(DO7,0)&	DCS off
13	SET(DO8,0)&	SiCH6 off
14	SET(DO9,0)&	GeH4 inject off
15	SET(DO10,0)&	SiH4 off
16	SET(DO11,0)&	B2H6 off
17	SET(DO12,0)&	PH3 off
18	SET(DO13,0)&	Source off
19	SET(AO0,0.617)&	H2 flow = 3 slpm
20	SET(DO15,1)	Vacuum on
21	SET(DO1,1)&	H2 on
22	SET(AO1,0.212)&	GeH4 flow = 100 sccm
23	SET(AO2,0.165)&	SiH4 flow = 100 sccm
24	SET(AO3,0.01)&	B2H6 high
25	SET(AO4,0.01)&	PH3 high
26	SET(AO5,0.01)&	PH3 low
27	SET(AO6,0.0)&	DCS
28	SET(AO7,0.063)	SiCH6 flow = 6 sccm
29	SET(AO8,0.0)	Pressure = 0
30	SEQUENCER ON(0.3,1,0)	Start Sequencer #1
31		

Sequencer Table #1

Step #	Action	Comment
0		
1	SET(SP2,0.0)&	Reset loop control
2		
3		
4		
5		
6	SEQUENCER ON(0.3,5,0)	Cleaning Sequence
7	WAITUNTIL(SP2>0.5)	
8	SET(SP2,0.0)&	Reset loop control
9		
10		
11		
12	SEQUENCER ON(0.3,4,0)	Call $Si_{1-x-y}Ge_xC_y$/Si sequence
13	WAITUNTIL(SP2>0.5)	$Si_{1-x-y}Ge_xC_y$ /Sisequence
14	SET(SP2,0.0)&	Reset loop control
15		
16	SET(SP4,0.0)&	Feedback off
17		
18		
19	RAMP(SP7,-0.4,0.0)&	Lamps down to zero
20		
21		
22		
23		
24		
25		
26	SEQUENCER ON(0.3,7,0)&	Call reload sequence
27		
28		
29		
30		
31		

Sequencer Table #4

Step #	Action	Comment
0	SET(SP5,3.51)	Set T = 700C
1	SET(SP4,1.0)	Closed-loop
2	WAIT(60)	
3	SET(DO10,1)	Silane inject on
4	WAIT(10)	
5	SET(DO13,0)	Silane inject off
6	SET(SP5,2.9)	Set T = 625C
7	WAIT(30)	
8	SET(DO10,1)	Inject SiH4 and SiCH6
9	SET(DO9,1)	Inject GeH4
10	WAIT(240)	$Si_{1-x-y}Ge_xC_y$ layer
11	SET(DO9,0)	GeH4 inject off
12		Close SiCH6 manual valve
13	WAIT(30)	
14	SET(DO2,0)	GeH4 select off
15		
16		
17		
18		
19	SET(SP5,3.51)	T = 700C
20	WAIT(2700)	Si
21	SET(DO10,0)	SiH4 inject off
22	SET(DO3,0)	SiH4 select off
23	SET(SP2,1.0)	Set loop control
24	END	
25		
26		
27		
28		
29		
30		
31		

Sequencer Table #5

Step #	Action	Comment
1	WAITUNTIL(AI24>0.5)	GO for cold values
2	SET(SP3,1)	Get cold values
3	WAIT(1)	
4	SET(SP3,0)	Latch cold values
5	SET(AO8,0.6)	Pressure = 6 torr
6	RAMP(SP7,0.4,0.18)	Clean at 18% lamp power
7	WAIT(120)	Clean
8		
9		
10		
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25		
26		
27		
28		
29		
30		
31	SET(SP2,1.0)	Set loop control

Sequencer Table #7

Step #	Action	Comment
0	SET(SP7,0)	Lamps off
1	SET(DO13,0)&	DCS inject off
2	SET(DO12,0)&	PH3 off
3	SET(DO11,0)&	B2H6 off
4	SET(DO10,0)&	SiH4 off
5	SET(DO9,0)&	GeH4 off
6	SET(DO7,0)&	DCS select off
7	SET(DO5,0)&	PH3 off
8	SET(DO4,0)&	B2H6 off
9	SET(DO3,0)&	SiH4 off
10	SET(DO2,0)&	GeH4 off
11	SET(DO1,0)&	H2 off
12	SET(AO8,0.0)&	Pump out
13	SET(AO7,0.0)&	B2H6 low
14	SET(AO6,0.0)&	DCS
15	SET(AO5,0.0)&	PH3 low
16	SET(AO4,0.0)&	PH3 high
17	SET(AO3,0.0)&	B2H6 high
18	SET(AO2,0.0)&	SiH4
19	SET(AO1,0.0)&	GeH4
20	SET(AO0,0.00)	H2
21	WAITUNTIL(AI28<0.5)	Pump out
22	SET(DO15,0)&	Vacuum off
23		
24	SEQUNCER OFF(0)	Sequencer 0 off
25	SEQUNCER OFF(1)	Sequencer 1 off
26	SEQUNCER OFF(2)	Sequencer 2 off
27	SEQUNCER OFF(3)	Sequencer 3 off
28	SEQUNCER OFF(4)	Sequencer 4 off
29	SEQUNCER OFF(5)	Sequencer 5 off
30	SEQUNCER OFF(6)	Sequencer 6 off
31	SEQUNCER OFF(7)	Sequencer 7 off

A4

A series: (n-type substrate)

Sample: A(1) (#2250)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
3000	700	100				300*	undoped poly-Si

* Expected thickness:~300nm, actual thickness by SIMS:~400nm.

Sample: A(2) (#2251)*

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
240	625	100	100	6.3		~24	undoped $Si_{1-x-y}Ge_xC_y$
2700	700	100				~270	undoped poly-Si

actual total thickness by SIMS: ~400nm

Sample: A(3) (#2252)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
240	625	100	100			~ 24	undoped $Si_{1-x-y}Ge_xC_y$
2700	700	100				~270	undoped poly-Si

Sample: A(4) (#2253)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
240	700	100		6.3		~ 24	undoped $Si_{1-y}C_y$
2760	700	100				~276	undoped poly-Si

B series: (n-type substrate)

Sample: B(1) (#2259)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
600	700	100			500	~ 60	p^+ poly-Si
2400	700	100				~240	undoped poly-Si

Sample: B(2) (#2261)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
600	625	100	100	6	500	~ 60	p^+ $Si_{1-x-y}Ge_xC_y$
2400	700	100				~240	undoped poly-Si

Sample: B(3) (#2262)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
3000	700	100				~300	undoped poly-Si

C series: (n-type substrate)

Sample: C(1) (#2290)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
3000	700	100				~300	undoped poly-Si

Sample: C(2) (#2292)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
180	625	100	100	8		~ 18	undoped $Si_{1-x-y}Ge_xC_y$
2400	700	100				~240	undoped poly-Si

Sample: C(3) (#2291)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
60	700	100				~6	2nd interfacial poly-Si
180	625	100	100	8		~ 18	undoped $Si_{1-x-y}Ge_xC_y$
2820	700	100				~282	undoped poly-Si

Sample: C(4) (#2293)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
180	625	100	100	4		~ 18	undoped $Si_{1-x-y}Ge_xC_y$
2820	700	100				~282	undoped poly-Si

D series: (n-type substrate)

Sample: D(1) (#2235, #2398)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
2000	700	100			500	~200	p^+ poly-Si

Sample: D(2) (#2234)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
2000	625	100	100	2	500	~200	p^+ poly-$Si_{1-x-y}Ge_xC_y$

Sample: D(3) (#2236)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
2000	700	100	100		500	~200	p^+ poly-$Si_{1-x}Ge_x$

Sample: D(4) (#2400)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
2000	625	100	100	6	500	~200	p^+ poly-$Si_{1-x-y}Ge_xC_y$

E Series (p-type substrate)

Sample: E(1) (#2450)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
2000	700	100				200	undoped poly-Si

Sample: E(2) (#2452)

time sec	temp ºC	SiH4 sccm	GeH4 sccm	SiCH6 sccm	B2H6 sccm	thickness nm	description
10	700	100				~1	interfacial poly-Si
240	625	100	100	6		~24	undoped $Si_{1-x-y}Ge_xC_y$
2700	700	100				~176	undoped poly-Si

Appendix B

Publications and Presentations Resulting from this Thesis

Publications

1. C.L. Chang, J.C. Sturm, "Suppression of Boron Penetration by Polycrystalline $Si_{1-x-y}Ge_xC_y$ in Metal-Oxide-Semiconductor Structures," submitted to *Applied Physics Letters*.

2. C.L. Chang, L. Rokhinson, and J.C. Sturm, "Direct Optical Measurement of the Valence Band Offset of p^+ $Si_{1-x-y}Ge_xC_y$ / p^- Si (100) by Heterojunction Internal Photoemission," submitted *Applied Physics Letters.*

3. C.W. Liu, C.L. Chang, J.C. Sturm, "Thermal stability of $Si/Si_{1-x-y}Ge_xC_y$ /Si quantum wells grown by rapid thermal chemical vapor deposition," submitted to *Applied Physics Letters.*

4. C.L. Chang, J.C. Sturm, "Polycrystalline $Si_{1-x-y}Ge_xC_y$ for Suppression of Boron Penetration in PMOS Structures," to be published, *Materials Research Society Symposium Proceeding,* **525,** (1998).

5. C.L. Chang, L. Rokhinson, and J.C. Sturm, "Direct Optical Measurement of the Valence Band Offset of p^+ $Si_{1-x-y}Ge_xC_y$ / p^- Si (100) by Heterojunction Internal Photoemission," to be published, *Materials Research Society Symposium Proceeding,* **523,** (1998).

6. C.L. Chang, S. P. Shukla, W. Pan[a], V. Venkataraman[b], J.C. Sturm,, and M. Shayegan, "Effective mass measurement in two-dimensional hole gas in strained $Si_{1-x-y}Ge_xC_y$ / (100) Si modulation doped heterostructures," to be published in *Thin Solid Films*, (1998).

7. C.L. Chang, A. St. Amour, and J.C. Sturm, "The effect of carbon on the valence band offset of compressively strained $Si_{1-x-y}Ge_xC_y$ / (100) Si," *Applied Physics Letters*, **70**, 1557 (1997).

8. A. St. Amour, L.D. Lanzerotti, C.L. Chang, and J.C. Sturm, "Optical and Electrical-Properties of $Si_{1-x-y}Ge_xC_y$ thin films and devices," *Thin Solid Films*, **294**, 112, (1997).

9. C.L. Chang, A. St. Amour, and J.C. Sturm, "Effect of carbon on the valence band offset of $Si_{1-x-y}Ge_xC_y$ / Si heterojunctions," *International Electronic Devices Meeting Technical Digest* (1996).

10. C.L. Chang, A. St. Amour, L. Lanzerotti, And J.C. Sturm, "Growth and electrical performance of heterojunction p+ $Si_{1-x-y}Ge_xC_y$ / p- Si diodes" *Materials Research Society Symposium Proceeding,* **402**, 437 (1995).

Conference Presentations

1. M.S. Carroll, C.L. Chang, J.C. Sturm, T. Buyuklimanli, "Complete suppression of oxidation enhancement of boron diffusion using substitutional carbon incorporation," *Electronic Materials Conference,* (1998).

2. C.L. Chang, J.C. Sturm, "Polycrystalline $Si_{1-x-y}Ge_xC_y$ for suppression of boron penetration in the p^+ poly-silicon gated MOS structures," *Materials Research Society Spring Meeting*, San Francisco, (1998).

3. C.L. Chang, L. Rokhinson, and J.C. Sturm, "Direct Optical Measurement of the Valence Band Offset of p^+ $Si_{1-x-y}Ge_xC_y$ / p^- Si (100) by Heterojunction Internal Photoemission," *Materials Research Society Spring Meeting*, San Francisco, (1998).

4. C.L. Chang, S. P. Shukla, W. Pan[a], V. Venkataraman, J.C. Sturm,, and M. Shayegan, "Effective Mass Measurement in Two-Dimensional Hole Gas in Strained $Si_{1-x-y}Ge_xC_y$ / (100) Si Modulation Doped Heterostructures," *The Seventh International Symposium on Silicon Molecular Beam Epitaxy*, Banff, Canada, (1997).

5. M. Carroll, L.L. Lanzerotti, C.L. Chang, and J.C. Sturm, "Silicon epitaxial regrowth in RTCVD for passivation of reactive ion etched Si/$Si_{1-x}Ge_x$ /Si microstructures," *Electronic Materials Conference*, Fort Collins, Colorado, (1997).

6. C.L. Chang, A. St. Amour, S. Samavedam, J.C. Sturm, E.A. Fitzgerald, T. Persall, and M. Sarikaya, " Correlation of structural and minority carrier electrical properties of $Si_{1-x-y}Ge_xC_y$ / Si epitaxial structures grown by RTCVD," *Materials Research Society Spring Meeting*, San Francisco, (1997).

7. C.L. Chang, S. P. Shukla, V. Venkataraman, J.C. Sturm,, and M. Shayegan, "Two-Dimensional Hole Gas of $Si_{1-x-y}Ge_xC_y$ / (100) Si grown by Rapid Thermal Chemical Vapor Deposition" *Materials Research Society Spring Meeting*, San Francisco, (1997).

8. C.L. Chang, A. St. Amour, and J.C. Sturm, "Effect of carbon on the valence band offset of $Si_{1-x-y}Ge_xC_y$ / Si heterojunctions," *IEEE International Electron Devices Meeting*, San Francisco, CA, (1996).

9. (invited) A. St. Amour, L.D. Lanzerotti, C.L. Chang, J.C. Sturm, Y. Lacroix, and M.L.W. Thewalt, "Optical and Electrical Properties of $Si_{1-x-y}Ge_xC_y$ Thin Films Devices," *European Materials Research Society Spring Meeting*, Strasbourg, France (1996).

10. (invited) J.C. Sturm, A. St. Amour, L.D. Lanzerotti, C.L. Chang, Y. Lacroix, and M.L.W. Thewalt, "Optical and Electrical Properties of $Si_{1-x-y}Ge_xC_y$ structures grown by RTCVD," *Materials Research Society Spring Meeting*, San Francisco, CA (1996).

11. C.L. Chang, A. St. Amour, L. Lanzerotti, And J.C. Sturm, "Growth and Electrical Performance of Heterojunction p^+ $Si_{1-x-y}Ge_xC_y$ / p^- Si Diodes" *Materials Research Society Fall Meeting*, Boston, MA (1995).