Reliability of Highly Stable Amorphous-Silicon Thin-Film Transistors Under Low Gate-Field Stress—Part II: Optimization of Fabrication Conditions and Gate Voltage Dependence

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***Abstract*—Part I of this paper introduced a two-stage model for reliability characterization and lifetime prediction of amorphous-silicon thin-film transistors (a-Si TFTs) under low gate-field stress that includes both charge trapping in the silicon nitride (SiN_x) gate dielectric and defect generation in the a-Si channel. In part II, the model is used to experimentally reduce the drain current instability under room temperature operation of a-Si TFTs under a prolonged gate bias of 5 V. Deposition conditions for the SiN_x gate insulator and the a-Si channel layer were varied, and TFTs were fabricated with all reactive-ion-etch steps, or with all wet-etch steps. The stability of the a-Si channel also depends on the deposition conditions for the underlying SiN_x gate insulator, and TFTs made with wet etching are more stable than TFTs made with reactive ion etching. Combining the various improvements raised the extrapolated 50% lifetime of the drain current of back-channel-passivated dry-etched TFTs under continuous operation in saturation at 20 °C with $V_{GS} = 5$ V from 3×10^4 s (9.2 h) to 4×10^7 s (1.4 years). We also extend the model, so that parameters from the degradation at one gate voltage can be used to estimate the degradation at other low gate voltages.**

***Index Terms*—Stability, a-Si TFTs, two-stage model, charge-trapping, defect-generation.**

I. Introduction

HYDROGENATED amorphous silicon thin-film transistors (a-Si:H TFTs) have been widely used as digital switches for the low-duty-cycle active-matrix addressing of liquid crystal displays, optical scanners and sensors [1], [2] since their first demonstration in 1976 [3]. Extending to their use in continuous operation, such as for pixel current sources in active matrix organic light emitting diode displays (AMOLEDs) where brightness is proportional to the TFT current, makes stability a critical issue. Stable current is also important in X-ray image sensors. Thus a stable threshold is critical [4]. Low power dissipation while operating in saturation also requires a low gate voltage ($\leqslant$5 V). At low gate bias a different physical mechanism (a-Si defect generation) is the dominant cause of threshold voltage shift (part I of this paper and [2], [5], [6]) instead of charge trapping in the gate dielectric, which is thought to dominate at much higher gate voltages such as those used in Active matrix liquid-crystal display (AMLCD) circuits.

In Part II of the paper, a systematic experimental study to optimize a-Si stability for low-voltage (5 V $V_{\rm GS}$) operation at room temperature is presented. We varied both deposition conditions and etching methods, and linked their effects with the physical mechanisms that change the threshold voltage of a-Si TFTs under low gate bias. The a-Si TFT stability depends on their fabrication processes, in particular a-Si and SiN_x deposition conditions and etching methods. Among the deposition conditions, hydrogen dilution [7], [8] and ammonia to silane flow ratio for SiN_x gate insulator growth [8], [9], SiN_x deposition temperature [7]–[9], a-Si deposition temperature [10], [11] and hydrogen dilution [5], [6], [10] for a-Si growth have been shown to affect the stability of a-Si TFTs. Wet-etched a-Si TFTs [12] have been reported to be more stable than dry-etched TFTs.

In Part I of this paper, we presented a two-stage model for characterizing stability and predicting the saturation mode lifetime of highly stable a-Si TFTs under low gate-field stress ($\sim 1.5 \times 10^5$ V/cm, 5 V $V_{\rm GS}$ for 300-nm-thick SiN_x). The drain current degradation can be modeled as an effective total threshold voltage shift $\Delta V_{T,\mathrm{eff},\mathrm{total}}(t)$, where all the change in drain current was attributed to the threshold voltage change

$$I_D(t) = \mu_n C_{\rm ins} \frac{W}{2L} \left[V_{\rm GS} - (V_{T0} + \Delta V_{T,\mathrm{eff},\mathrm{total}}(t))\right]^2. \quad (1)$$

The "effective" threshold voltage terminology is used because the devices are in saturation (Part I, Sect. C.2).

Our experiments showed that even with accelerated tests up to 160 °C, with the current decreasing to as low 14% of its original value [13], the mobility changed by less than 10%, justifying modeling the current degradation as an effective threshold voltage increase. The effective threshold voltage shift $\Delta V_{T,\mathrm{eff},\mathrm{total}}(t)$ of a-Si TFTs develops in two stages: the fast initial threshold voltage shift $\Delta V_{T,\mathrm{eff},I}(t)$ (Stage I), and the dominant long-term threshold voltage shift $\Delta V_{T,\mathrm{eff},II}(t)$ (Stage II)

$$\Delta V_{T,\mathrm{eff},\mathrm{total}}(t) = \Delta V_{T,\mathrm{eff},I}(t) + \Delta V_{T,\mathrm{eff},II}(t). \quad (2)$$

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The threshold voltage shift in Stage I is most likely caused by charge trapping in SiN_x. It can be modeled with a stretched exponential model

$$\Delta V_{T,\mathrm{eff},I}(t) = \Delta V_{T,\mathrm{eff},\max,I}\left\{1-\exp\left[-\left(\frac{1}{t_{0,\mathrm{eff},I}}\right)^{\beta_I}\right]\right\}. \tag{3}$$

The threshold voltage shift in Stage II, $\Delta V_{T,\mathrm{eff},II}(t)$, is caused by defect creation in a-Si also fits a stretched exponential expression

$$\Delta V_{T,\mathrm{eff},II}(t) = (V_{\mathrm{GS}} - V_{T0} - \Delta V_{T,\mathrm{eff},\max,I}) \times\left\{1-\exp\left[-\left(\frac{t}{t_{0,\mathrm{eff},II}}\right)^{\beta_{II}}\right]\right\} \tag{4}$$

where

$$\beta_{II} = \frac{T}{T_0} \tag{5}$$

$$t_{0,\mathrm{eff},II} = v^{-1}\exp\left(\frac{E_{\mathrm{act,eff}}}{kT}\right) \tag{6}$$

or, in terms of fundamental parameters

$$t_{0,\mathrm{eff},II} = v^{-1}\left(\frac{n_{\mathrm{ch},o}}{C_0 k T_0}\right)^{\frac{T_0}{T}} \tag{7}$$

where v is an attempt frequency, T_0 is the characteristic temperature reflecting the weak bond distribution in energy, $E_{\mathrm{act,eff},II}$ is an effective activation energy of the defect creation, C_0 is the pre-exponential constant in the distribution of weak bonds versus bond strength, and $n_{\mathrm{ch},o}$ is a constant inversely reflecting the sensitivity of the bond breaking rate of electron density. We now go on to use the model to optimize process conditions for long-term reliability near room temperature.

II. Fabrication of a-Si TFTs

The a-Si TFTs in our experiments were fabricated with a standard bottom-gate non-self-aligned process in the back-channel passivated (BCP) structure on 3 in × 3 in glass substrates (Fig. 1). SiN_x and a-Si layers were deposited in a plasma-enhanced chemical vapor deposition (PECVD) system at 13.56 MHz. 300-nm gate SiN_x, 200-nm intrinsic hydrogenated a-Si and 300-nm passivation SiN_x were deposited sequentially without breaking vacuum. The passivation SiN_x was deposited at a substrate temperature of 220 °C. The n^+ a-Si was deposited at a substrate temperature of 150 °C. The deposition conditions of the gate SiN_x and the channel a-Si layers will be varied to study the effect on the stability of a-Si TFTs in Section III.

For dry-etched a-Si TFTs, reactive-ion etching (RIE) was used for patterning the silicon nitride and a-Si. For wet-etched a-Si TFTs, the four plasma etching steps were replaced by wet-etching methods as described in Table I. For both the dry-etch process and wet-etch process, we use the same PECVD steps for the TFT stack growth, unlike an earlier wet-etch a-Si TFT process which requires an additional SiN_x layer [12], [14]. At the end of TFT fabrication, both dry and wet-etched TFTs were annealed at 180 °C for one hour in vacuum.

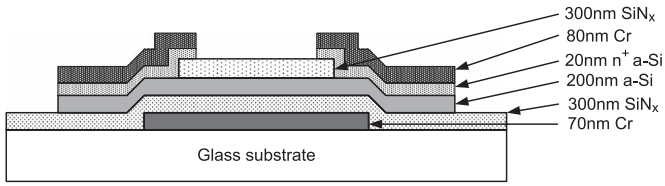


Fig. 1. Schematic cross-section of the back-channel passivated TFT structure.

III. Effects of SiN_x and a-Si PECVD Conditions

All TFTs have the gate nitride dielectric layers grown at 320 °C and use the dry-etching process. In the gate SiN_x growth, we varied the hydrogen dilution and ammonia (NH_3) to silane (SiH_4) ratio. In the channel a-Si growth, we varied a-Si substrate temperature and hydrogen dilution. We also varied the deposition power for SiN_x and a-Si near the SiN_x/a-Si interface. The TFTs were biased in saturation with a constant gate-source voltage of 5 V (a gate field of $\sim 1.5 \times 10^5$ V/cm) and a constant drain-source voltage of 7.5 V. The drain current was measured at temperatures from 20 °C to 140 °C in steps of 20 °C, with a new device for each temperature. The deposition conditions and the corresponding stability parameters extracted from the two-stage model at 20 °C are listed in Table II.

The stability in Stage I was fit to the model by adjusting two parameters: the maximum threshold voltage shift $\Delta V_{T\max,I}$ and the characteristic time $t_{0,I}$ (preferably long), mostly from 20 °C data. At higher temperatures, Stage I effects saturated before they could be measured. The stability in Stage II was characterized by parameters $t_{0,\mathrm{eff},II}$ and β_{II} (both preferably large) obtained from the stretched exponential fit in (4) from accelerated tests at high temperatures. $t_{0,\mathrm{eff},II}$ and β_{II} are related to the attempt-to-escape frequency v, the activation energy E_{act} and the characteristic temperature T_0, which reflect the a-Si properties. The fitting procedure is described in Part I of this paper. The difference between the total degradation measured at 20 °C and the Stage II degradation (extrapolated from the high temperature data) allowed the Stage I degradation at room temperature to be isolated.

The two-stage 50% lifetime $\tau_{50\%}$ is defined as the time when the drain current has dropped to 50% of its initial value, predicted with the two-stage model combining effects of Stage I and Stage II. Because the TFTs were biased continuously, without any off-time for recovery effects, the lifetimes should be considered "worst case" lifetimes. The initial threshold voltage, before gate bias stress applied to a-Si TFTs, is $V_{T0} = 0.83 \pm 0.45$ V. It is not obviously correlated with the TFT stability.

A. SiNx Gate Insulator Deposition Conditions

Except for the SiN_x gate insulator deposition conditions, processes #1, #2, #3, #5, #7, and #8 have the same fabrication conditions. We plotted the two-stage 50% lifetimes $\tau_{50\%}$ of TFTs fabricated with these six processes in Fig. 2.

TABLE I
COMPARISON OF DRY-ETCHING AND WET-ETCHING STEPS

	Plasma etching Step in dry-etching	Dry-etching		Wet-etching	
		Mask	Etchant	Mask	Etchant
1	Passivation SiN_x etch	Photoresist	Plasma	Photoresist	HF
2	Channel a-Si etch	Photoresist	Plasma	Passivation SiNx	KOH
3	n+ a-Si etch	Photoresist	Plasma	S/D Cr	KOH
4	Gate SiN_x via etch	Photoresist	Plasma	Shadow mask	n.a.

TABLE II
DEPOSITION CONDITIONS AND CORRESPONDING STABILITY PARAMETERS AT 293 K. PROCESS #5/6 AND #8/9 ARE COMPARISONS OF DRY VERSUS WET ETCHING. TFT'S FROM PROCESS #16 (IN BOLD) ARE THE MOST STABLE

	Etch	Gate SiN_x		a-Si			Stage I		Stage II					Two-stage
No.	Wet / Dry	Hydrogen dilution?	$[NH_3]$ / $[SiH_4]$	Temp. (°C)	$[H_2]$ / $[SiH_4]$	Power density (mW/cm^2)	$\Delta V_{T,max,I}$ (V)	$t_{0,eff,I}$ (s)	ν (kHz)	T_0 (K)	$E_{Act,II}$ (eV)	$t_{0,eff,II}$ (in 10^6 s)	β_{II}	$\tau_{50\%}$ (in 10^4 s)
1	Dry	No	10	220	10	17	0.3	<<1	5	1160	0.60	4.5	0.25	3.2
2	Dry	No	15	220	10	17	0.1	<<1	50	1035	0.69	13.3	0.28	25.0
3	Dry	No	25	220	10	17	0.1	<<1	100	967	0.69	8.3	0.30	20.7
4	Dry	Yes	10	200	10	17	0.1	1.0	500	830	0.78	53.9	0.35	219
5	Dry	Yes	10	220	10	17	0.08	8.7	500	730	0.79	77.9	0.40	455
6	Wet	Yes	10	220	10	17	0.31	69.5	500	565	0.79	67.8	0.52	543
7	Dry	Yes	15	220	10	17	0.15	42.7	500	797	0.78	49.1	0.37	201
8	Dry	Yes	20	220	10	17	0.14	10.1	500	964	0.78	49.1	0.30	111
9	Wet	Yes	20	220	10	17	0.23	29.8	500	793	0.78	55.0	0.37	192
10	Dry	Yes	10	220	2	8.6	0.16	22.4	1000	781	0.82	124	0.38	518
11	Dry	Yes	10	220	5	8.6	0.12	55.0	1000	772	0.82	118	0.38	562
12	Dry	Yes	10	220	10	8.6	0.23	1224	1000	766	0.82	120	0.38	449
13	Dry	Yes	10	300	10	8.6	0.08	206	5000	685	0.88	215	0.43	1800
14	Dry	Yes	10	320	10	17	0.06	1.2	5000	709	0.88	312	0.41	2100
15	Dry	Yes	10	320	2	8.6	0.19	0.3	5000	698	0.90	522	0.42	3040
16	**Dry**	**Yes**	**10**	**320**	**5**	**8.6**	**0.08**	**0.2**	**5000**	**643**	**0.90**	**524**	**0.46**	**4490**
17	Dry	Yes	10	320	7.5	8.6	0.15	0.5	5000	831	0.90	667	0.35	2250
18	Dry	Yes	10	330	2	8.6	0.2	0.3	5000	744	0.89	215	0.40	1320

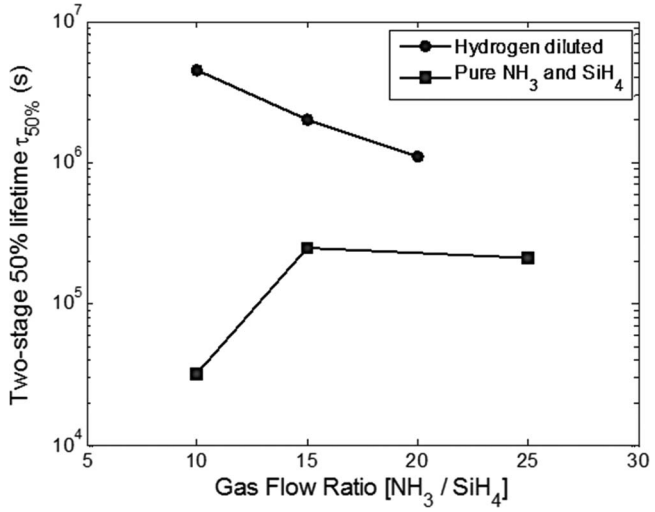


Fig. 2. Dependence of 50% lifetime from the two-stage model fit on the gate SiN_x deposition conditions. The squares represent processes #1, #2, and #3 without hydrogen dilution and the dots represent processes #5, #7, and #8 with hydrogen dilution.

1) Effect of Hydrogen Dilution: In the gate SiN_x depositions for processes #5, #7, and #8, the H_2 to SiH_4 ratio is about 50. Fig. 2 shows that the two-stage 50% lifetime $\tau_{50\%}$ can be raised 10 to 100 times by this hydrogen dilution during nitride growth compared to no dilution. Hydrogen dilution makes the SiN_x film more compact, and drives the film to be compressive [15]. The longer Stage I characteristic time $t_{0,I}$ for processes #5, #7, and #8 than for processes #1, #2, and #3 (Table II) shows that hydrogen dilution during the gate SiN_x growth raises the stage I stability by improving SiN_x film itself by making it less susceptible to charge trapping. More important is improvement in the a-Si channel (through Stage II lifetime) deposited directly on top of the SiN_x caused by the hydrogen dilution during SiN_x. The hydrogen dilution improves the Stage II lifetime by roughly an order of magnitude (Table II, Fig. 2). This effect may come from the increased effective activation energy for defect formation in the a-Si.

2) Effect of Ammonia to Silane Ratio: Comparing processes #1, #2, #3, #5, #7, and #8, we find the NH_3 to SiH_4 gas flow ratio $[NH_3/SiH_4]$ also affects the TFT stability. Fig. 2 shows that in the absence of the hydrogen dilution, the best $[NH_3/SiH_4] = 15$. For the hydrogen-diluted processes, the best $[NH_3/SiH_4] = 10$. A high but proper $[NH_3/SiH_4]$ flow ratio produces nitrogen-rich SiN_x, which has a low content of Si-H bonds and good electrical properties, including high resistivity, high breakdown voltage and low charge trapping rate [16]. Both with and without hydrogen dilution, the processes with best $[NH_3/SiH_4]$ have both the best stage I stability (smallest $\Delta V_{T\max,1}$) and the best stage II stability (longest $t_{0,II}$), again showing a relation between the gate SiN_x and a-Si quality.

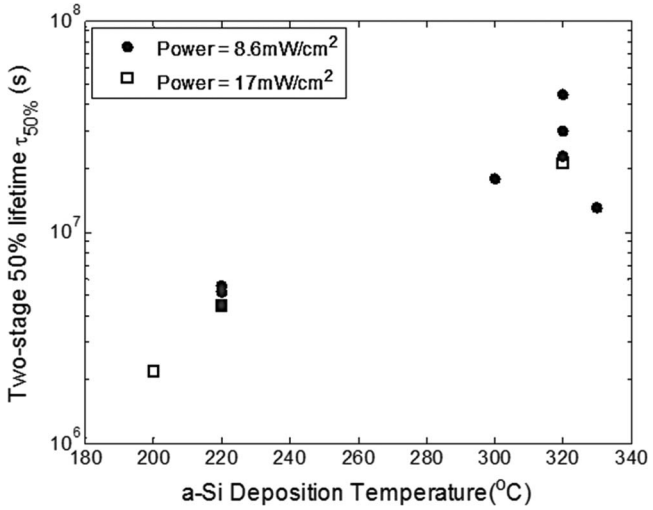


Fig. 3. Dependence of two-stage 50% lifetime on the a-Si deposition temperature and power. The open squares represent processes #4, #5, and #14 with a-Si deposition power at 17 mW/cm^2, and the solid dots represent processes #10–#13 and #15–#18 with a-Si deposition power at 8.6 mW/cm^2.

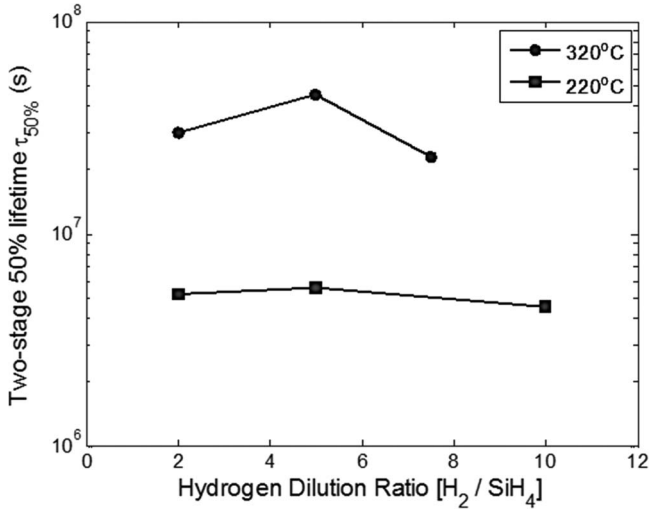


Fig. 4. Dependence of 50% lifetime on the hydrogen dilution during a-Si deposition using two-stage model. The squares represent processes #10, #11, and #12 with the a-Si deposition temperature of 220 °C and the dots represent processes #15, #16, and #17 with the a-Si deposition temperature of 320 °C.

B. a-Si Channel Layer Deposition Conditions

As shown above, when a-Si deposition conditions are fixed, the best gate SiN_x is deposited using hydrogen dilution and $[NH_3/SiH_4] = 10$. Given this SiN_x deposition condition, we varied the a-Si deposition conditions. The resulting two-stage 50% lifetimes $\tau_{50\%}$ are shown in Fig. 3. The open squares represent processes #4, #5, and #14 with a-Si deposition power at 17 mW/cm^2, and the solid dots represent processes #10–#13 and #15–#18 with a-Si deposition power at 8.6 mW/cm^2.

1) Effect of a-Si Deposition Temperature: Fig. 3 shows that by increasing the substrate temperature from 200 °C (process #4) to 320 °C (process #14) during a-Si deposition, with all other deposition conditions staying the same, the two-stage 50% lifetime $\tau_{50\%}$ can be raised 10 times for the TFTs deposited at 17 mW/cm^2. For the TFTs deposited at 8.6 mW/cm^2, the two-stage 50% lifetime $\tau_{50\%}$ can be raised about 8 times by increasing the a-Si deposition temperature from 220 °C (processes #10–#12) to 320 °C (processes # 15–#17). However, if the deposition temperature for the a-Si exceeds that for the gate SiN_x (process #18), the stability deteriorates. Thus, we find that the best a-Si deposition temperature is the same as the gate SiN_x deposition temperature. Most of this effect is from changes in the defect formation in a-Si (Stage II). Higher temperature enables *in-situ* annealing during deposition and a reduction of the number of weak bonds in the a-Si.

2) Effect of Hydrogen Dilution: The a-Si layers in processes #10, #11, and #12 are deposited at 220 °C with three different H_2 to SiH_4 gas flow ratios [H_2/SiH_4]. The a-Si layers in processes #15, #16, and #17 are deposited at 320 °C, also with three different [H_2/SiH_4] ratios. The squares in Fig. 4 show that for a-Si deposited at 220 °C, the effect of hydrogen dilution has no effect on the two-stage 50% lifetime $\tau_{50\%}$. At the a-Si deposition temperature of 320 °C (solid dots in Fig. 4), the most stable a-Si TFTs are made with $[H_2/SiH_4] = 5$ (process #16).

3) Effect of Deposition Power at Both Sides of the SiN_x/a-Si Interface: The deposition power for the a-Si and the gate SiN_x near the SiN_x/a-Si interface also affects the stability of the TFTs. In processes #4, #5, and #14, the gate SiN_x is deposited at 21.5 mW/cm^2 and the a-Si is deposited at 17 mW/cm^2. In processes #10–#13 and #15–#18, the a-Si and the gate SiN_x near the SiN_x/a-Si interface are deposited at 8.6 mW/cm^2. Because the growth of SiN_x at 8.6 mW/cm^2 is slow, the SiN_x more than 50 nm away from the interface is still deposited at 21.5 mW/cm^2. Fig. 3 and Table II suggest that the stability may be slightly improved through decreasing deposition power near the SiN_x/a-Si interface (processes #10–#12 versus process #5 at 220 °C, and processes #15–#17 versus process #14 at 320 °C). The stability improvement is reflected in the rise of $E_{\mathrm{act,eff}}$. A lower plasma power may lead to a reduced number of weak bonds in the a-Si because the plasma may damage the a-Si.

C. Discussion

We observed that deposition conditions of the gate SiN_x and a-Si affect the stability of a-Si TFTs in a regime where a-Si defect formation dominates the degradation. Since the a-Si channel is deposited immediately after the gate SiN_x for the bottom gate TFT structure, that the results depend on the SiN_x suggest the quality and microstructure of the a-Si at or near the SiN_x interface (where the channel electrons are and where we thus expect the defect formation to occur [4], [17], [18]) can, not surprisingly, be subtly affected by that of the underlying SiN_x. Hydrogen dilution and a proper [NH_3/SiH_4] flow ratio for SiN_x growth can slow down both instability mechanisms in two stages—charge trapping in SiN_x and defect creation in a-Si. The a-Si layer of the most stable a-Si TFTs in our work (process #16) was deposited at the same temperature 320 °C as that of the gate SiN_x, at low deposition power near the interface and with hydrogen dilution during deposition.

It is interesting to note that the Stage II (bond breaking) attempt frequency parameter v varies from 5 to 5000 kHz over our range of fabrication conditions. Such a wide range has been observed previously (factor of 2000), depending on changes in the microstructure [19]. A low attempt frequency was explained

as having resulted from regions having weak bonds (likely to break) having a small number of electrons, which accelerate the defect-formation process. This implies the electron density may not be uniform on a microscopic level in samples with low ν.

There was no single parameter which was key to high Stage II stability, but rather their combination is important. High T_0 implies that the number of bonds does not rapidly increase as bond strength is increased—a low number of weak bonds and thus high T_0 is desirable. Also, important is a low pre-exponential constant C_0 in the distribution of bonds versus bond strength and a large $n_{\mathrm{ch},o}$, which inversely reflects the sensitivity of bond breaking to electron density (see (7) for $t_{0,\mathrm{eff},II}$ above, and (6) and (8) in Part I). In modeling, these dependences are reflected through the activation energy of the characteristic time $t_{0,\mathrm{eff},II}$ parameter in Stage II, $E_{\mathrm{act,eff},II}$

$$E_{\mathrm{act,eff},II} = kT\ln(vt_{0,\mathrm{eff},II}) = kT_0\ln\left(\frac{n_{\mathrm{ch},o}}{C_0kT_0}\right). \quad (8)$$

Thus, a high $E_{\mathrm{act,eff}}$ is desirable. Also, note that outside its dependence on $E_{\mathrm{act,eff},II}$, there is no dependence of $t_{0,\mathrm{eff},II}$ on T_0 or any other physical parameter other than the escape frequency.

Repeating (34) in Part I of this paper, the time $\tau_{x\%,II}$ for the drain current to decrease to x percent of its original value in stage II is

$$\tau_{x\%,II} = \left(\frac{-\ln(x\%)}{2}\right)^{\frac{T_0}{T}} t_{0,\mathrm{eff},II} = \left(\frac{1}{v}\right)\left(\frac{-\ln(x\%)}{2}\right)^{\frac{T_0}{T}} e^{\frac{E_{\mathrm{Act,eff},II}}{kT}}. \quad (9)$$

(9) summarizes that for a high lifetime, a high $E_{\mathrm{Act,eff},II}$ is crucial. Outside of the exponential dependence on $E_{\mathrm{Act,eff},II}$, the dependence of lifetime on T_0 is only modest. This is reflected experimentally in the fact that in Table II our most stable process (#16) has a relatively low T_0 but the highest $E_{\mathrm{Act,eff},II}$.

IV. Stability of Wet Versus Dry-Etched TFTs

We also investigated the effects of dry versus wet etching on the TFT stability under low gate-field stress. The DC transfer characteristics of dry-etched and wet-etched TFTs are similar and uniform across the 75-mm × 75-mm substrates (Fig. 5). The dry-etched a-Si TFTs had initial threshold voltages $V_{T0} = 0.71 \pm 0.28$ V and field-effect mobilities $\mu_n = 1.14 \pm 0.04$ cm^2/V · s. The wet-etched a-Si TFTs had $V_{T0} = 0.80 \pm 0.15$ V and $\mu_n = 1.08 \pm 0.03$ cm^2/V · s.

We randomly picked three dry-etched and three wet-etched a-Si TFTs from processes #8 and #9 in Table II. At 20 °C, we stressed them in saturation with a constant gate-source voltage of 5 V and a constant drain-source voltage of 7.5 V for about 24 hours. $\Delta V_{T,\mathrm{total}}(t)$ was extracted from measured drain current data versus time. These are the squares in Fig. 6(a) for dry etching and (b) for wet etching. To separate Stage I and Stage II effects, high-temperature measurements, as described earlier,

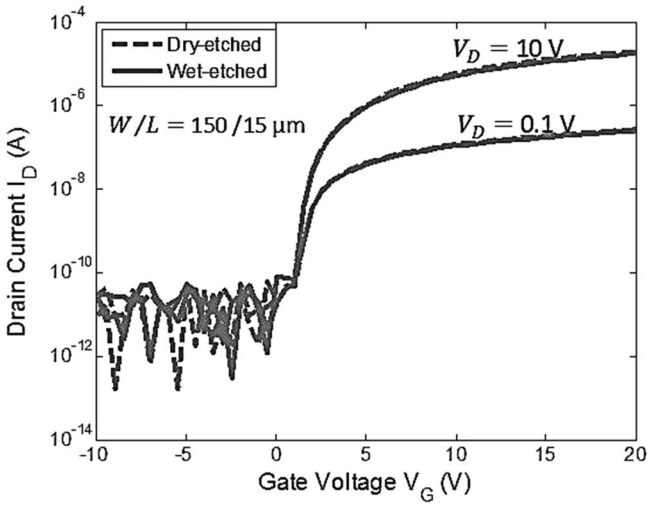
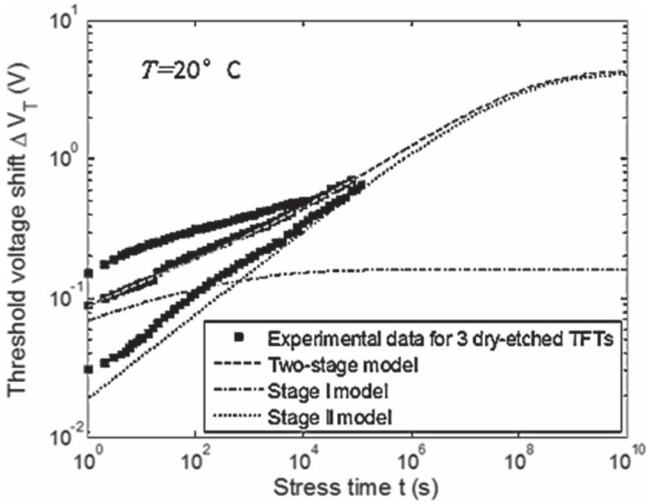
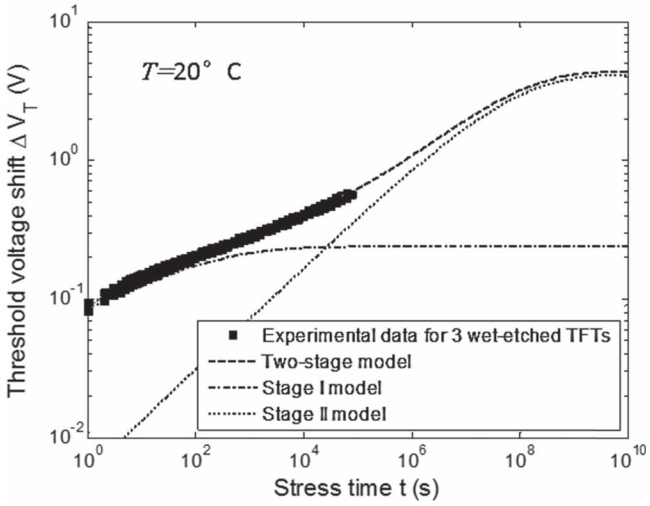


Fig. 5. Transfer characteristics of dry- and wet-etched a-Si TFTs (processes #8 and #9 in Table II).



(a)



(b)

Fig. 6. (a) Threshold voltage shift of three randomly picked dry-etched a-Si TFTs at 20 °C and two-stage model fitting to the threshold voltage shift of one TFT. (b) Threshold voltage shift of three randomly picked wet-etched a-Si TFTs at 20 °C (indistinguishable) and two-stage model fitting to the threshold voltage shift of one TFT.

TABLE III
STAGE I FITTING PARAMETERS FOR DRY- AND WET-ETCHED A-SI TFTS

	Dry-etched a-Si TFTs			Wet-etched a-Si TFTs		
TFTs	$\Delta V_{Tmax,I}$ (V)	$t_{0,eff,I}$ (s)	β_I	$\Delta V_{Tmax,I}$ (V)	$t_{0,eff,I}$ (s)	β_I
1	0	0	NA	0.24	35	0.24
2	0.16	28.8	0.18	0.23	15	0.25
3	0.25	1.4	0.36	0.23	39	0.24
Average	0.14±93%	10.1±160%	0.27±48%	0.23±2.5%	30±43%	0.24±2.3%

were performed to get Stage II parameters. Comparing the measured room-temperature degradation and the modeled Stage II degradation, we obtained the stage I degradation [dot-dash line in Fig. 6(a) and (b)], with parameters listed in Table III. Wet-etched a-Si TFTs are clearly more uniform in Stage I than dry-etched TFTs. We attribute this variation in Stage I in the dry-etched TFT's to spatially non-uniform surface charge buildup during plasma etching, which can induce surface states at the SiN_x/a-Si interface and eventually trap charge in SiN_x [20]. Regarding the effects of the plasma processing, we note that during the back-channel passivation dry etch, the a-Si channel is still not yet patterned. Thus we think this step is the least likely dry etch step for causing a spatially non-uniform charge build-up in the gate dielectric and variable Stage I damage.

Accurate extraction of the Stage I parameters requires assuming Stage II on that device is similar to that in the devices used for the Stage II parameter extraction at different temperatures. This assumption is justified by visual inspection of the effective threshold shift versus time at room temperature for the three devices of Fig. 6(a). For long times (when Stage II is most important), the experimental curves all begin to converge and have a much smaller divergence than they do for the Stage I degradation at short times. This shows that the primary variation in the devices is in Stage I, so that a single set of Stage II parameters can be used for all three devices.

The Stage II 50% lifetime was about twice as large for TFTs fabricated with the wet-etched processes (Series A in Fig. 7, with parameters in Table II, processes #8 and #9). This is because wet etching produces a lower T_0 than dry-etching, while the parameters v and $E_{\rm act}$ are similar. A lower T_0 means that the energy distribution of weak Si-Si bonds in wet-etched a-Si TFTs is steeper than that in dry-etched TFTs. Another series of dry and wet-etched a-Si TFTs (Series B in Fig. 7) fabricated under different deposition conditions (processes #5 and #6 in Table II) gave similar results. Reactive ion etching (RIE) can cause damage by ion bombardment and plasma radiation [21]. Because our a-Si TFTs have the back-channel passivated structure, surface damage from ion bombardment should not affect the channel region. Thus the RIE-induced degradation observed in Stage II may be the result of the high photon energy plasma radiation, which could cause the Staebler-Wronski type defects in the a-Si layer that are not fully reversible by thermal annealing [21], [22]. We do not know which plasma step is most likely to cause such damage. Comparing the stability between dry and wet-etched a-Si TFTs suggests that some damage caused by RIE still remains after a one-hour long annealing at 180 °C [12]. Overall, the wet-etched TFT's had about twice the two-stage 50% lifetimes at 20 °C compared to the dry-etched TFTs (Fig. 7).

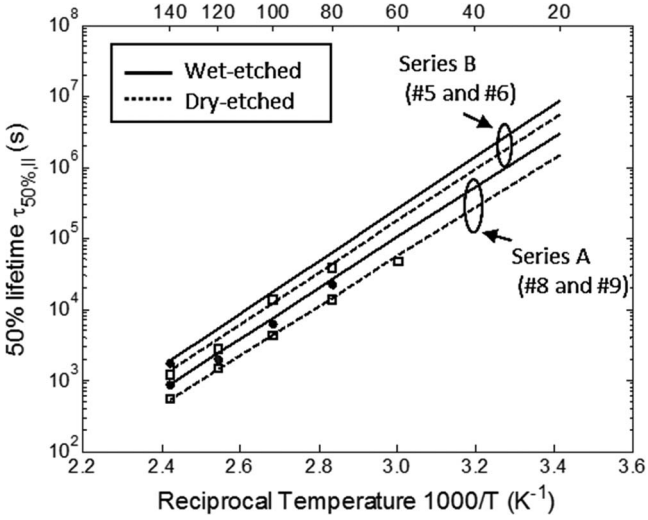


Fig. 7. 50% lifetime at different temperatures for two series of dry and wet-etched a-Si TFTs (solid squares: experimental data; straight lines: stage II model).

V. EFFECT OF GATE VOLTAGE

Up to this point, all data presented in this paper has been for a gate-source voltage of 5 V. We now briefly examine the degradation at different gate voltages. Fig. 8 presents normalized drain current versus time for TFT's fabricated similar to those analyzed in process #5 in Table II, but two years earlier than those devices. Thus the devices might not behave exactly the same as those in process #5. The degradation in saturation at gate-source voltages of 5.0 V, 7.5 V, 10.0 V, and 12.5 V are presented, all at 60 °C. These voltages are still fairly "low" for operation of a-Si TFTs. The drain voltage was 2.5 V larger than the gate voltage. The gate voltage has only a small effect (on a logarithmic time scale), with the 50% degradation time for current decreasing from 2.5×10^5 s to 0.9×10^5 s as the gate voltage is increased from 5 V to 12.5 V. Stage I effects (which had a ∼5% effect on the current) were saturated already by 1s after the bias voltage was applied. Thus to focus on Stage II, the current at 1 second was used as the initial time for normalization.

The curves were fit with the models of (1) and (3). For parameters, v was set to 5×10^5 Hz as in Table II process #5, and T_0 of 830 K was used, close to the 730 K of line 5. If all of the fundamental parameters of the model developed in this paper were ideally independent of gate voltage, meaning the model presented was exact in all physical attributes, the normalized current versus time would be independent of gate voltage, as gate voltage does not appear in the normalized current which results from the stretched exponential model

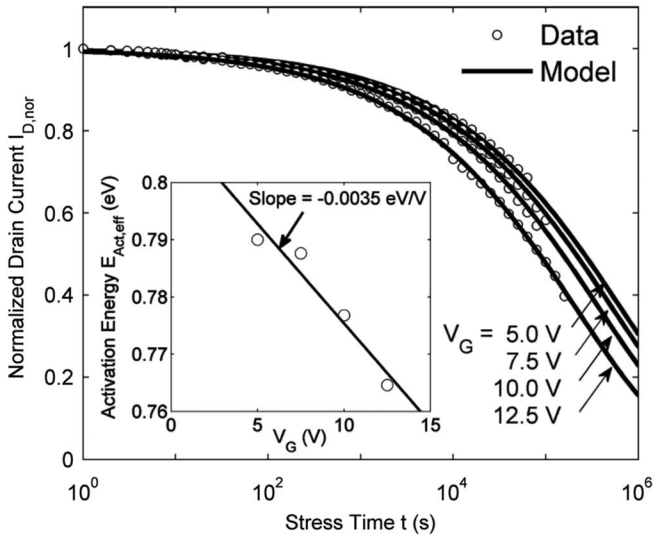


Fig. 8. Normalized current in saturation at gate voltages of 5.0, 7.5, 10.0, and 12.5 V at 60 °C for TFT's fabricated similarly to those of Table II, process #5. Stage II fits are also presented using $\beta = 0.4$, $v = 5 \times 10^5$, and effective activation energy $E_{\mathrm{act,eff}}$ of 790, 788, 777, and 765 meV for the four gate voltages, respectively. The inset shows the dependence of $E_{\mathrm{act,eff}}$ on gate voltage.

[(29) from Part I of this paper]:

$$I_{D,\mathrm{nor}}(t) = \exp\left[-2\left(\frac{t}{t_{0,\mathrm{eff},II}}\right)^{\beta}\right]. \qquad (10)$$

At high gate voltages, a higher threshold shift is required to reduce drain current by a fractional amount compared to a low-gate-voltage condition, but at high gate voltages the higher channel electron density leads to a faster threshold shift, a fundamental assumption of our model.

Such ideality rarely occurs in practice; to use the models of this paper to span different gate voltages, we empirically adjusted one parameter, the effective activation energy $E_{\mathrm{act,eff},II}$ (8) as a function of gate voltage. Physically, this could result from the higher Fermi level at high carrier densities—a higher fraction of the electrons could then be able to physically access the weak bond sites to enable bond-breaking (reducing $n_{\mathrm{ch},o}$ and thus $E_{\mathrm{act,eff},II}$). The dependence of $E_{\mathrm{act,eff},II}$ on gate voltage is shown as an inset in Fig. 8, with a slope of -3.5 meV/V. This slope was fairly insensitive to the fit; changing T_0 to 730 K changed the slope by only $\sim$10%. With knowledge of the slope of $E_{\mathrm{act,eff},II}$ versus gate voltage, one can use data for Stage II extracted at one gate voltage to predict degradation at other gate voltages. Further work is necessary to determine if this dependence of $E_{\mathrm{act,eff},II}$ on gate voltage is sensitive to process conditions.

VI. Summary

Using results from low gate-field stress over a range of temperatures and their fit to a two-stage model for threshold voltage shift, we evaluated the effect of a-Si TFT fabrication processes on the stability of the drain current in saturation with $V_{\mathrm{GS}} =$ 5 V. The two-stage model is necessary because the initial degradation at room temperature is dominated by charge trapping in the gate SiN_x, but the dominant long term mechanism is defect creation in the a-Si. Achieving high stability requires a high ($\sim$320 °C) deposition temperature for the gate SiN_x and the a-Si, hydrogen dilution for the SiN_x deposition, and low a-Si deposition power near the SiN_x interface. By combining these deposition techniques, we raised the extrapolated 50% lifetime of the drain current under continuous operation at room temperature in saturation with $V_{\mathrm{GS}} = 5$ V from 3.3×10^4 s (9.2 hours) to 4.4×10^7 s (1.4 years) for a dry-etch process. We also showed how degradation at one gate voltage is related to that at other gate voltages. Further improvement in stability may be possible by minimizing damage from plasma-etch steps during processing.

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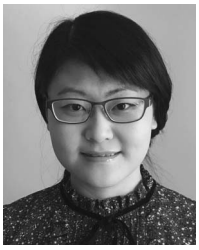

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