A 12% Efficient Silicon/PEDOT:PSS Heterojunction Solar Cell Fabricated at < 100 °C

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***Abstract*—Solar cells based on a heterojunction between crystalline silicon and the organic polymer PEDOT:PSS were fabricated at temperatures <100 °C by spin coating. The Si/PEDOT interface blocks electrons in n-type silicon from moving to the anode and functions as a low-temperature alternative to diffused p-n junctions. The device takes advantage of the light absorption and transport properties of silicon and combines it with the simplicity of fabrication afforded by organics. Reverse recovery measurements were used to analyze the electron-blocking effectiveness of the heterojunction. The data show that current in the device is primarily due to holes injected from the anode into the silicon. At AM1.5, Si/PEDOT heterojunction solar cells achieve power conversion efficiency of 11.7%, which is among the highest reported values for this class of devices.**

***Index Terms*—Heterojunction, hybrid photovoltaics, PEDOT:PSS, silicon organic.**

I. Introduction

HYBRID photovoltaic devices incorporating inorganic and organic materials are receiving great interest as an approach to next generation photovoltaics. These technologies are aimed at combining the advantages of different material systems to provide better efficiency, more cost efficient manufacturing, or both. Silicon/organic heterojunctions (SOH) are attractive because they can be fabricated at temperatures <100 °C, using simple methods such as spin coating [1], [2]. In comparison, conventional crystalline silicon solar cells require p-n junctions that are fabricated at temperatures higher than 800 °C [3]. SOH-based solar cells also do not require a plasma-enhanced chemical vapor deposition process to deposit amorphous silicon, as in the heterojunction with intrinsic thin-layer (HIT) technology. However, like HIT cells, SOH-based solar cells make use of crystalline silicon as the absorbing material, and therefore may reach the high efficiency (>24%) reported by the best crystalline silicon solar cells [4], [5]. Due to the simplicity of fabrication and the potential for high efficiency, SOH solar cells may substantially reduce the cost of silicon photovoltaics. Previously, a Si/P3HT heterojunction solar cell with 10% power conversion efficiency was demonstrated [1]. In this paper, we report an investigation of the origin of dark current in SOH devices, and demonstrate a SOH solar cell with an AM1.5 power conversion efficiency of 11.7%.

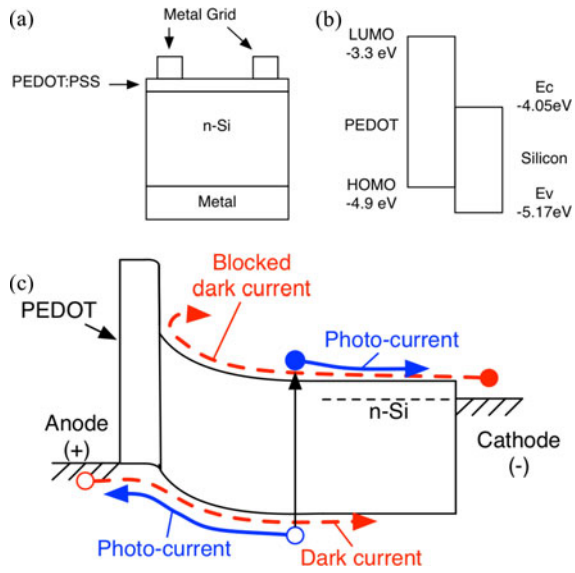

Fig. 1. (a) Physical structure and (b) electronic band alignment of SOH device. (c) Band diagram of device under illumination with positive bias. Dashed red lines represent dark current, solid blue lines represent photocurrent.

Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) is an organic polymer that is commonly used as a transparent conductor. The PEDOT polymer and PSS together form a macromolecular salt, in which the PSS is reduced, forming the anion and the PEDOT is oxidized, forming the cation. PEDOT:PSS is readily dispersed in the aqueous solution [6]. The dispersion is readily spin cast and the resulting films are highly conductive and transparent. Several methods have been demonstrated to increase the conductivity further via solvent modification [7]–[9]. PEDOT thin films act as heavily doped p-type semiconductor with a large bandgap of ~1.6 eV [10]–[12].

The structure of Si/PEDOT heterojunction solar cell is shown in Fig. 1(a), and the electronic band structure is shown in Fig. 1(b). The diagram reflects the highest occupied molecular orbital/lowest unoccupied molecular orbital (HOMO/LUMO) levels in low-conductivity (<10 S/cm) PEDOT:PSS [11]. Our work uses high-conductivity (~1000 S/cm) PEDOT:PSS, which

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has the same doping characteristics to first order. The conductivity enhancements result primarily through morphology changes of the insulating PSS surrounding conductive PEDOT grains [13]. Therefore, we model the high-conductivity PEDOT:PSS in our work with a HOMO/LUMO of 3.3 and 4.9 eV as measured in low-conductivity PEDOT:PSS. Light enters from the top of the cell, where the PEDOT:PSS is coated. The PEDOT:PSS layer is more than 90% transparent at such film thicknesses (<100 nm); therefore, under illumination, most of the light is absorbed in silicon. As shown in Fig. 1(b), the LUMO level of PEDOT is much higher than the conduction band of silicon; therefore, the electrons in silicon should be blocked from flowing into PEDOT. On the other hand, the HOMO level of PEDOT is closely aligned with the valence band of silicon, allowing holes in silicon to flow into PEDOT unimpeded. This is illustrated in the band diagram of the SOH device in Fig. 1(c). Due to the high work-function of the conductive, heavily-doped PEDOT layer (∼4.9 eV), there exists a depletion region in n-type silicon at the Si/PEDOT interface (expected ∼1 um for $N_D = 10^{15}$ cm^{-3}). The depletion region separates the photogenerated carriers in silicon, causing a photocurrent. The negligible hole barrier at the Si/PEDOT interface allows the efficient collection of holes at the anode [solid blue line in valence band of Fig. 1(c)] and the large electron barrier at the Si/PEDOT interface reduces the electron dark current to the anode [dotted red lines in the conduction band of Fig. 1(c)] leading to low J_0 and high $V_{\rm OC}$.

II. Experimental Details

PEDOT:PSS was purchased as 1.4% dispersion by weight in water (Clevios PH1000) and 10% w/w dimethyl sulfoxide was added to enhance the conductivity of the film [12], [13]. The silicon wafers were cleaned using the standard RCA cleaning procedure [14]. Si/PEDOT devices were fabricated by spin coating a 70-nm thick layer of PEDOT on 2–4 Ω·cm (∼1.5 × 10^{15} cm^{-3}) phosphorus-doped n-type silicon wafers. To make electrical contacts, thermally evaporated silver and aluminum were deposited on the front and backside of the wafer to form anode and cathode, respectively. The anode (front side contact) was patterned by a shadow mask to allow light to be absorbed in silicon [Fig. 1(a)]. The top metal grid covers ∼10% of the surface. The device size was 4 mm × 4 mm. Lowering the PEDOT conductivity or increasing the metal grid spacing increases the parasitic lateral resistance. The maximum process temperature was 100 °C. The Si/ PEDOT solar cell does not require the fabrication of the p-n junction. The devices also did not have any back surface fields.

Electrical measurement of the devices was performed with an Agilent/Hewlett-Packard 4155 parameter analyzer. For characterization at AM1.5 illumination, a xenon lamp solar simulator was used. The illumination was calibrated to 1000 W/m^2 using a silicon reference cell. A 4 mm × 4 mm aperture was used to illuminate a fixed active area of a single device and prevent overestimation of photocurrent due to laterally diffusing carriers.

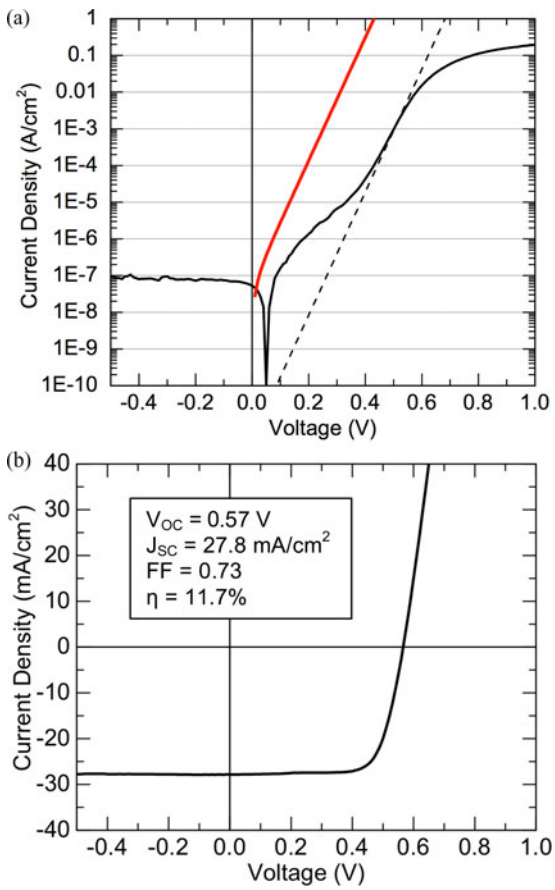

Fig. 2. (a) J–V characteristic of the SOH solar cell in the dark and calculated from a Schottky barrier (1). (b) J–V characteristic and parameters of SOH solar cell under AM1.5 illumination.

III. Results and Analysis

A. Current–Voltage Measurements

Fig. 2(a) presents the J–V characteristics for a Si/PEDOT heterojunction cell under dark conditions (continuous black line). The diode shows some nonideality ($n = 2$) at lower current levels (∼10^{-6}–10^{-7} A/cm^2), which may be due to surface defect states at the Si/PEDOT interface. The diode regains an ideality factor of close to 1 at higher values of forward-bias (>0.4 V). At 1.3-mA/cm^2 forward current, and using an ideality factor of 1, we can extract a saturation current (J_0) to be 3.8 × 10^{-12} A/cm^2 [dashed line in Fig. 2(a)].

If the Si/PEDOT:PSS interface does not function as an electron-blocking barrier then one would expect the Si/PEDOT junction to behave just like a regular Schottky diode. The saturation current for such a Schottky diode is dominated by electrons, the majority carrier, and is given as

$$J_{0,\text{electrons}} = A^* T^2 e^{-\frac{\phi_B}{kT}} \quad (1)$$

where A^* is the Richardson constant, T is temperature, ϕ_B is the Schottky barrier height, and k is the Boltzmann constant. Given the work function of PEDOT:PSS (∼4.9 eV), the n-Si PEDOT Schottky junction would have a barrier height of $\phi_B = 0.8$ eV. Fig. 2(a) presents the current expected for such a

metal/Si Schottky barrier (red line). Fig. 2(a) clearly shows the dark current in the SOH device is lowered by over four orders of magnitude than that expected from a simple Schottky device. This suggests that the PEDOT:PSS heterojunction does indeed act as a barrier to the electron current.

Fig. 2(b) shows that under AM1.5 illumination, an open-circuit voltage of 0.57 V was achieved along with a short-circuit current of 27.8 mA/cm^2 and fill factor of 73%. The overall power conversion efficiency of this device was 11.7%, which is among the best reported for this class of the photovoltaic device.

B. Reverse Recovery

The open-circuit voltage of a solar cell is limited by the amount of dark current in the device. To further increase the $V_{\rm OC}$ of the Si/PEDOT devices, the dark current should be reduced. The $V_{\rm OC}$ ideally depends on the saturation current (J_0), as

$$V_{\rm OC} \equiv \frac{kT}{q}\ln\left(1+\frac{J_{\rm SC}}{J_0}\right) \tag{2}$$

where q is the elementary charge and $J_{\rm SC}$ is the short-circuit current. The first step toward reducing the J_0 is to determine which carrier contributes most to the dark current—electron or hole? It has been previously shown that in Si/P3HT devices, the electron-blocking is so good that the dark current is mostly caused by holes [minority carriers; the dashed red curve in the valence band Fig. 1(c)], not electrons (majority carriers) [1]. Si/PEDOT devices operate under the same principle in that the organic heterojunction blocks the electron current. To investigate this, we tested the device for stored minority carriers using the diode reverse recovery method [15]–[17].

In forward-bias, minority carriers will be injected from the anode into the quasi-neutral region of the diode, as shown in Fig. 1(c) (dashed red line in the valence band). In the steady state, a stored charge of holes will be built up in the n-type silicon. Another possible current mechanism is electrons overcoming the barrier presented by the heterojunction (thermionic emission). However, in this case, no stored charge would be observed because of the short electron lifetime in PEDOT:PSS [13]. The current may also be due to recombination at the heterojunction interface (silicon surface defects); however, this would not contribute to stored charge either. Therefore, the stored charges can be used to estimate the current due to minority carriers.

The extracted minority carrier charge can be measured by switching the diode from forward to reverse bias. Under reverse-bias the stored carriers (holes) get swept back out of the device to the PEDOT:PSS, momentarily causing a large reverse current (I_R). The circuit used to measure the transient along with the voltage and current waveforms is shown in Fig. 3(a) and (b). The area under the curve until the beginning of the decay point in reverse bias is defined as the charge extracted from the diode $(Q_{\rm extracted})$. For a given forward-bias current (I_F), $Q_{\rm extracted}$ depends on the transient current in reverse bias (I_R) by the following equation [15]:

$$Q_{\rm extracted} = I_R\tau_{\rm bulk}\left[\text{erfc}^{-1}\left(\frac{1}{1+\frac{I_R}{\alpha I_F}}\right)\right]^2 \tag{3}$$

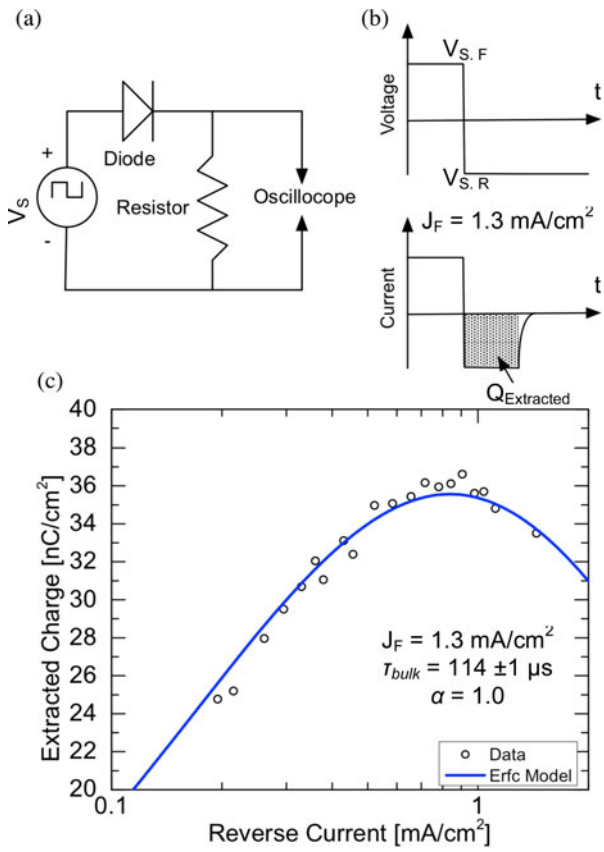

Fig. 3. (a) Circuit used for the reverse recovery experiment to measure effective injected hole lifetime $\tau_{\rm bulk}$ and hole injection ratio α. (b) Typical waveforms for a device which has substantial minority carrier current, showing the $Q_{\rm extracted}$. (c) $Q_{\rm extracted}$ as a function of I_R. Black circles represent measured data and blue line shows best fit to the data for $\tau_{\rm bulk} = 114$ μs and $\alpha = 1.0$.

where $\tau_{\rm bulk}$ is the bulk recombination lifetime and α is the ratio of the minority-carrier current to the total current. If the dark current is composed only of holes injected into silicon, $\alpha = 1$.

Fig. 3(c) shows the measured value of $Q_{\rm extracted}$ as a function of J_R, for an $J_F = 1.3$ mA/cm^2. At low J_R, the holes are not extracted fast enough; therefore, most of them recombine in silicon, leading to low value of $Q_{\rm extracted}$. At higher J_R, the holes are removed quickly, before they can recombine, and hence, the $Q_{\rm extracted}$ is large. The blue line in Fig. 3(c) is the best fit of the data to (3). From the best fit, the extracted value of α and $\tau_{\rm bulk}$ are 1.0 and 114 μs, respectively.

The value of $\alpha = 1.0$ proves that most of the dark current is indeed caused by minority carriers and subsequently shows that the barrier is effective at blocking electrons. The $\tau_{\rm bulk}$ can be further used to estimate the value of minority carrier current $(J_{0,\rm hole})$, using the following equation:

$$J_{0,\rm hole} = q\frac{n_i^2}{N_D}\sqrt{\frac{D_{\rm hole}}{\tau_{\rm bulk}}} \tag{4}$$

where N_D is the silicon doping level, $D_{\rm hole}$ is the hole diffusion coefficient, and n_i is the intrinsic carrier concentration of silicon. From the extracted value of $\tau_{\rm bulk} = 114$ μs, we estimate the $J_{0,\rm hole}$ to be 6.64 $\times$ 10^{-12}A/cm^2.

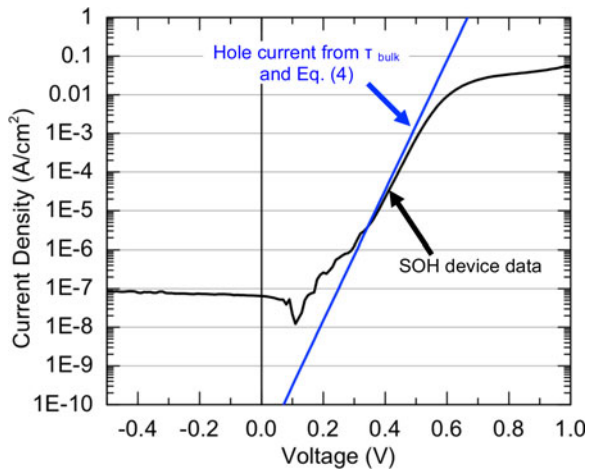

Fig. 4. $J-V$ characteristic of SOH device measured with reverse recovery and hole current calculated from the measured $\tau_{\rm bulk}$ and (4).

Fig. 4 plots the $J-V$ characteristics of the SOH device measured with the reverse recovery experiment (black curve). In addition, shown is the hole current expected in the device, as calculated from (4) (blue line). Comparing the curves, we see excellent agreement in the ideal diode region of the device. This shows that in the $n\sim1$ region, the dark current is entirely accounted for by the hole current and that the contribution of electron current is negligible. Clearly, the PEDOT layer is an effective electron-blocker. The forward bias current used for the reverse recovery measurement was intentionally chosen to lie in this region, as this is the relevant operating region for the solar cell. This gives us confidence that our approach accurately extracts the minority carrier lifetime, and that $\alpha = 1$ for our devices.

Furthermore, by using measured values of $J_{\rm SC}$ ($\sim$25 mA/cm^2) and the calculated $J_{0,\rm hole}$ from (4), one can calculate an *expected* value of $V_{\rm OC}$ using (1): i.e., the $V_{\rm OC}$ one expects if the dark current is composed of only holes as measured via the reverse recovery experiment. The expected $V_{\rm OC}$ is 0.57 V, which agrees with the experimentally measured value of 0.57 V. These results suggest that in Si/PEDOT devices, dark current is predominantly composed of hole (minority) carriers and not electrons (majority) carriers.

IV. Conclusion

We have demonstrated an electron-blocking Si/PEDOT heterojunction that is fabricated by a room temperature spin coating process. Reverse recovery experiments provide a measurement of the stored charge provided by injection of minority carriers in forward bias. This provides a measurement of the current in the Si/PEDOT device that is carried by minority carrier hole injection from the anode. The data show that the Si/PEDOT interface is very effective at blocking electrons, to the extent that dark current in heterojunction devices on n-Si is not limited by electrons, but by the minority-carrier hole injection from anode into silicon. The best Si/PEDOT solar cells yield a high open-circuit voltage of 0.57 V and an efficiency of 11.7%, which is among the highest reported for this class of devices.

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