Reliability of Highly Stable Amorphous-Silicon Thin-Film Transistors Under Low Gate-Field Stress—Part I: Two-Stage Model for Lifetime Prediction

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***Abstract*—To predict reliability, an analytical model for drain current degradation in amorphous-silicon (a-Si) thin-film transistors (TFTs) is developed for the low-gate-field region, where defect creation dominates the threshold voltage shift. Starting with fundamental models where the local threshold shift depends on the local channel electron density, a stretched exponential expression for current degradation in linear and saturation modes is derived and related to an effective threshold voltage. The model was used to predict room temperature stability from accelerated stress up to 140 °C in highly stable TFTs with hydrogenated a-Si channels and silicon nitride (SiN_x) gate insulators. For high temperatures and long times at all temperatures, defect creation dominated the decay. A "unified" stretched exponential fit, in which a single fitting parameter is used to convert time into "thermalization energy," unifies drain current decay at different temperatures into a single curve. At short times near room temperature, a second mechanism ascribed to charge trapping also contributes to the initial degradation. This contribution is attributed to charge trapping in the SiN_x gate insulator and can also be fitted with a stretched exponential expression. A two-stage model that combines both mechanisms is used for best predictions of room temperature stability. Part II of this paper will show that this two-stage model facilitates the optimization of the fabrication of a-Si TFTs with very high stability.**

***Index Terms*—Two-stage model, a-Si TFTs, unified stretched exponential, stability, defect creation and charge trapping.**

NOMENCLATURE

$C_{\rm ins}$	Capacitance of the gate insulator.
C_0	Weak bond distrib'n. pre-exponential const.
$E_{\rm act}$	Arrhenius activation energy of characteristic time t_0.
$E_{\rm act,eff}$	Effective activation energy in saturation.
$E_{\rm act,eff,II}$	Stage II effect. saturation activ'n. energy.
$E_{{\rm act},\tau x,{\rm II}}$	Arrhenius activation energy for time for normalized current to degrade to $x\%$.
E_b	Barrier-breaking energy.
$E_{\rm th}$	Thermalization energy, $E_{\rm th} \equiv kT\ln(\upsilon t)$.
k	Boltzmann constant.
I_D	Drain current.
$I_{D,{\rm Sat}}$	Drain saturation current.
$I_{D,{\rm nor}}$	Normalized drain current, $I_{D,{\rm nor}}(t) \equiv I_D(t)/I_D(t=0)$.
L	TFT channel length.
n_A	Number of weak bonds per unit energy per unit volume.
N_A	Number of weak bonds per unit volume.
N_B	Number of broken bonds per unit volume.
$N_{\rm tot}$	Total density of traps in channel.
N_T	Density of traps in insulator.
$n_{\rm ch}$	Number of channel electrons per unit volume.
$n_{{\rm ch},o}$	Channel density normalization constant.
q	Electron charge.
r_d	Constant in the logarithmic time dependence of charge trapping.
t	Time.
t_0	Characteristic time $t_0 = \upsilon^{-1}\exp(E_{\rm act}/kT)$.
$t_{0,{\rm eff}}$	Effective characteristic time in saturation.
$t_{0,{\rm eff,I}}$	Effective characteristic time in saturation in Stage I.
$t_{0,{\rm eff,II}}$	Effective characteristic time in saturation in Stage II.
T	Temperature.
T_0	Characteristic temperature.
$V_{{\rm Ch},S}$	Channel-source voltage.
$V_{\rm GS}$	Gate-source bias voltage.
$V_{\rm DS}$	Drain-source bias voltage.
$V_{D,{\rm Sat}}$	Drain saturation voltage.
V_T	Threshold voltage.
V_{T0}	Initial threshold voltage.
x	Depth in channel layer.
y	Lateral distance from source to drain.
β	Exponent in the stretched exponential expression, $\beta = T/T_0$.
$\beta_{\rm I}$	Exponent in the stretched exponential expression for Stage I.
$\beta_{\rm II}$	Exponent in the stretched exponential expression for Stage II.
ε	Dielectric permittivity of gate insulator.

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λ	Tunneling constant in insulator.
μ_n	Electron field-effect mobility.
$\tau_{x\%}$	Time for normalized current to decay to $x\%$.
$\tau(E_b)$	Characteristic time to overcome the barrier E_b, $\tau(E_b) = v^{-1}\exp(E_b/kT)$.
v	Attempt-to-escape frequency.
$\langle d \rangle$	Centroid of trapped charge measured from the gate metal.
ΔV_T	Threshold voltage shift.
$\Delta V_{T,\mathrm{eff}}$	Effective threshold voltage shift in saturation.
$\Delta V_{T,\mathrm{eff,I}}$	Threshold effective voltage shift in Stage I degradation.
$\Delta V_{T,\mathrm{eff,II}}$	Threshold effective voltage shift in Stage II degradation.
$\Delta V_{T,\max}$	Maximum threshold voltage shift.
$\Delta V_{T,\mathrm{eff},\max}$	Maximum effective threshold voltage shift in saturation.
$\Delta V_{T,\mathrm{eff},\max,\mathrm{I}}$	Maximum effective threshold voltage in Stage I degradation.
$\Delta V_{T,\mathrm{eff},\max,\mathrm{II}}$	Maximum effective threshold voltage in Stage II degradation.
$\Delta V_{T,\mathrm{eff,total}}$	Total effective threshold voltage shift in saturation.

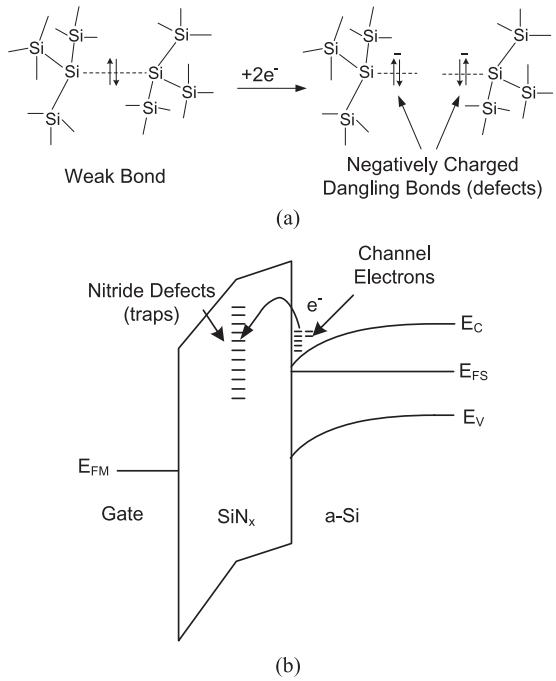

Fig. 1. Instability mechanisms in a-Si TFTs: (a) defect creation in a-Si; and (b) charge trapping near the SiN_x/a-Si interface.

I. Introduction

AMORPHOUS-Si (a-Si) TFTs are traditionally used in low-duty-cycle operation as digital pixel access switches in Active Matrix Liquid Crystal Displays (AMLCDs). At the gate voltages used in these applications (typically well over 10 V), the drain current degrades quickly. For use as pixel current drivers in active matrix organic light-emitting diode (AMOLED) displays, high stability under DC operation is required, because the pixel brightness depends on the current. Operation in saturation with under 5 V gate voltage is required for low pixel power consumption.

For such low-gate-voltage operation, defect formation in the a-Si and the resulting threshold increase can dominate the current degradation [1]–[3], in contrast to trapping in the gate dielectric which dominates at much higher gate voltages [4]–[6]. Recently, highly stable a-Si TFTs have been reported with extremely long operating lifetimes under DC gate bias with $\sim$7.5 V [3], [7], [8]. The time for the DC saturation current to drop to 50% of its initial value has been estimated to be over 100 years. However, the lifetimes were extrapolated with a stretched-exponential expression based on only month-long tests at room temperature, leading to uncertainty in the validity of the extrapolation.

In this work, Part I develops a physically-based analytical model for modeling threshold shift in a-Si TFTs in saturation, which incorporates both defect formation and charge trapping mechanisms, and uses these models to develop a rigorous approach to accelerated testing at elevated temperatures for modeling long-term room temperature. Part II then uses these models to experimentally optimize the fabrication of TFTs for room temperature stability in saturation with 5 V V_{GS}.

We begin Part I by reviewing two instability mechanisms in a-Si TFTs—defect creation in a-Si and charge trapping in the silicon nitride (SiN_x) gate insulator. Because of the distributed barrier energy and/or trapping parameters, both mechanisms can be modeled with a stretched exponential expression. The *effective* threshold voltage shift for circuit modeling in saturation is derived based on fundamental material parameters. When all sets of drain current vs. time data at different temperatures are plotted against the "thermalization energy" $E_{\mathrm{th}} = kT\ln(vt)$ [9], which requires only a single fitting parameter, they can be represented by a single curve. This leads us to propose a "unified stretched exponential fit" to the drain current degradation caused by defect creation in a-Si. The unified stretched exponential fit agrees well with the experimental results obtained in the temperature range from 80 °C to 140 °C. At short times (days) and lower temperatures, charge trapping must also be considered for fast initial shifts.

II. Instability Mechanisms in a-Si TFTs

In n-channel a-Si TFTs, the threshold voltage increases under positive gate bias, and the drain current drops. It is well established that two mechanisms may cause the threshold voltage to rise (Fig. 1): (a) defect creation in the channel a-Si layer and subsequent electron trapping [1], [2], [10], and (b) electron trapping in the SiN_x gate insulator [4]–[6], [11], [12]. Under negative gate voltage, defect creation and hole trapping contribute to an opposite threshold shift [2], [13]. This paper focuses on DC positive gate bias. In mechanism (a) [10], [14], electrons accumulated in the channel reduce their energy by breaking the weak Si-Si bonds, which form negatively charged dangling bonds [Fig. 1(a)]. In mechanism (b) [12], channel electrons leak into the SiN_x dielectric and are captured by traps in the SiN_x [Fig. 1(b)]. We now review why both threshold shifts vs. time caused by these two mechanisms can be represented by a "stretched exponential" [10], [12].

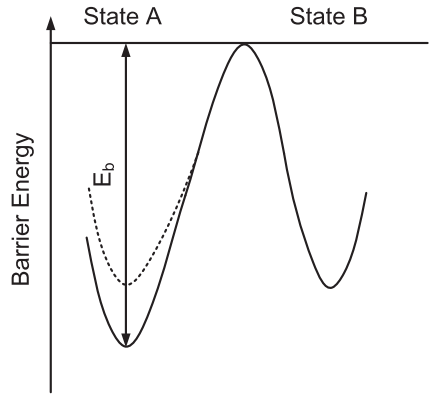

Fig. 2. Two-level configuration coordinate diagram for metastability in a-Si. State A represents the weak bond state, and state B represents the dangling bond state. E_b is the barrier-breaking energy.

A. Modeling Defect Creation in a-Si

Electrons in the channel induce weak Si-Si bonds (which give rise to states in the band tails) to break into dangling bonds. This process is reversible unless the dangling bonds relax into stable configurations. Two alternative models explain this defect relaxation kinetics—hydrogen-diffusion-controlled defect-relaxation (HCR) and defect-controlled defect-relaxation (DCR). In the HCR model, a hydrogen atom diffuses to the site, attaches itself to one of the dangling bonds, and thereby separates the two dangling bonds [15]–[17]. In the DCR model, the two dangling bonds relax locally without the aid of a diffusing atom [18].

In the DCR model, defect creation in a-Si is modeled as a transition in energy from an initial weak bond state to stabilized but metastable dangling bond states [18]. In the two-level configuration coordinate diagram (Fig. 2), state A is the weak bond state and state B is the dangling bond state. Because of variations of bond lengths and bond angles in a-Si, the number of weak bonds per unit energy per unit volume n_A with breaking-barrier energy E_b has an exponential distribution in fresh a-Si TFTs before stress (Fig. 3) [18], [19]

$$n_A(E_b) = C_0 e^{\frac{E_b}{kT_0}}. \tag{1}$$

This distribution means that few very weak bonds are easily broken (dotted curve in Fig. 2) and an increasing number of stronger bonds are harder to break. The characteristic temperature T_0 reflects the degree of disorder. A low value of T_0 implies a steep tail in the energy distribution of weak bonds [20]. The transition from the weak bond state to the dangling bond state is thermally activated (Fig. 2), with a characteristic time $\tau(E_b)$

$$\tau(E_b) = v^{-1} \exp\left(\frac{E_b}{kT}\right). \tag{2}$$

v is the attempt-to-escape frequency. Transitions over low energy barriers are frequent, while those over high energy barriers are rare. To a first-order approximation, at time t, weak bonds with a characteristic time $\tau(E_b)$ less than the time t will all have been broken, and those with a characteristic time $\tau(E_b)$ larger than t will not yet have been broken. This statement can also be

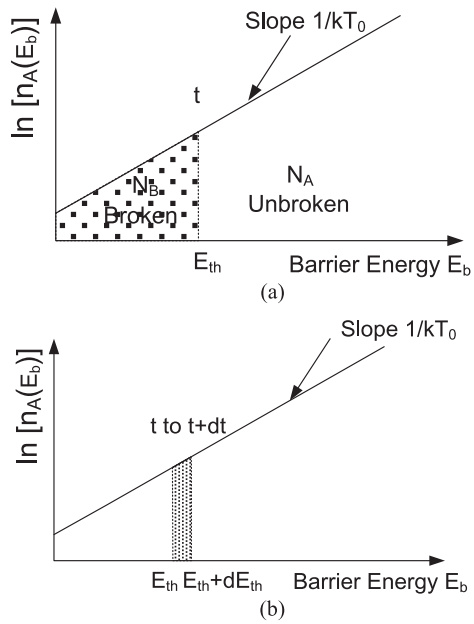

Fig. 3. Logarithm of the number of weak bonds per unit energy per unit volume n_A vs. bond strength (energy barrier for bond breaking): (a) Schematic distribution of the volume density of weak bonds N_A in a-Si (mostly in the valence band tail) and broken bonds N_B; and (b) illustration of the progress of bond breaking with increasing duration t of gate-bias stress, expressed as $E_{\rm th} = kT\ln(vt)$.

expressed in terms of a "thermalization energy" $E_{\rm th}$ [9], which is defined as

$$E_{\rm th} \equiv kT\ln(vt). \tag{3}$$

At time t, we can approximate that weak bonds with a barrier energy E_b less than $E_{\rm th}$ will have been broken and the stronger bonds above $E_{\rm th}$ will be intact [Fig. 3(a)]. It follows that between time t and $t + dt$, bonds with barrier energies between $E_{\rm th}$ and $E_{\rm th} + dE_{\rm th}$ will break [the shaded region in Fig. 3(b)]. Defining $N_B(t)$ as the number of broken bonds per unit volume, the defect creation rate is then

$$\frac{dN_B(t)}{dt} = \frac{dN_B}{dE_{\rm th}}\frac{dE_{\rm th}}{dt}. \tag{4}$$

The area of the shaded region in Fig. 3(b) is

$$dN_A(E_{\rm th}) = n_A(E_{\rm th})dE_{\rm th}. \tag{5}$$

Because one weak bond breaks into two dangling bonds, we have $dN_B(E_{\rm th}) = 2dN_A(E_{\rm th})$. Here we relate the weak bond states to the created dangling bond states with a ratio of 1:2. Thus the defect creation rate with thermalization energy is

$$\frac{dN_B}{dE_{\rm th}} = 2n_A(E_{\rm th}) = 2C_0 e^{\frac{E_{\rm th}}{kT_0}}. \tag{6}$$

Combined with (3), the defect creation rate is

$$\frac{dN_B(t)}{dt} = \frac{dN_B}{dE_{\rm th}}\frac{dE_{\rm th}}{dt} = 2C_0 kT\, v(vt)^{T/T_0-1}. \tag{7}$$

Experiments show that the defect creation rate increases with the applied gate voltage $V_{\rm GS}$ [21], [22]. Often the defect

creation rate is assumed to be proportional to the number of channel electrons per unit volume $n_{\rm ch}$ [18], [22], because electrons induce the weak bonds to break [9], [18], [22], [23]. After factoring the electron volume density n_{ch} into (7), the defect creation rate as a function of time becomes

$$\frac{dN_B(t)}{dt} = \frac{2C_0 n_{\rm ch}(t) kT\, v(vt)^{T/T_0-1}}{n_{{\rm ch},o}} \tag{8}$$

where $n_{{\rm ch},o}$ is a new constant inversely reflecting the sensitivity of the rate on electron density. Because channel electrons are captured by the dangling bonds and raise the threshold voltage, the threshold voltage is related to the number of dangling bonds per unit volume by

$$\frac{dV_T(t)}{dt} = q\int \frac{dN_B(t)}{dt} dx / C_{\rm ins} \tag{9}$$

where $C_{\rm ins}$ is the capacitance of the gate SiN_x and the integration is across the channel thickness x. Here we assume that the defects in the a-Si are created very close to the SiN_x/a-Si interface. With gate-source bias $V_{\rm GS}$

$$\int n_{\rm ch}(y,t)dx = \frac{C_{\rm ins}\left[V_{\rm GS} - V_{{\rm Ch},S}(y,t) - V_T(y,t)\right]}{q}. \tag{10}$$

Parameter y is the position along the channel, 0 at the source and L at the drain, since the electron density varies along the channel depending on channel voltage $V_{{\rm Ch},S}$ for any non-zero $V_{\rm GS}$. Thus the local threshold voltage varies along the channel as well due to different rates of defect creation. Substituting (9) and (10) into (8) leads to a differential form of the stretched exponential expression for the threshold voltage shift vs. time.

Threshold voltage shift can be modeled with a differential equation

$$\frac{\partial V_T(y,t)}{\partial t} = \left(\frac{2C_0}{n_{{\rm ch},o}}\right)\left[V_{\rm GS} - V_T(y,t) - V_{{\rm Ch},S}(y,t)\right] kTv(vt)^{T/T_0-1}. \tag{11}$$

If we define "characteristic time" t_0

$$t_0 \equiv v^{-1}\left(\frac{2C_0 kT_0}{n_{{\rm ch},o}}\right)^{-1/\beta} \tag{12}$$

and define

$$\beta \equiv \frac{T}{T_0} \tag{13}$$

Eq'n. (14) becomes

$$\frac{\partial V_T(y,t)}{\partial t} = \left[V_{\rm GS} - V_T(y,t) - V_{{\rm Ch},S}(y,t)\right]\frac{\beta}{t_0}\left(\frac{t}{t_0}\right)^{\beta-1}. \tag{14}$$

β is the ratio of kT to the characteristic energy of the distribution of the weak bonds and β decreases as the distribution broadens. The term "activation energy" $E_{\rm act}$ is often used in the literature on stretched exponential processes and is by definition the Arrhenius activation energy of t_0, assuming v is independent of temperature.

$$E_{\rm act} = kT\ln(vt_0) = -kT_0\ln\left(\frac{2C_0 kT_0}{n_{{\rm ch},o}}\right). \tag{15}$$

This does not imply a single energy barrier as in a conventional activation energy in an Arrhenius relation for degradation experiments. Rather, $E_{\rm act}$ is closely related to the maximum energy barrier surmountable on the time scale of the experiment and will depend on time t [2]. (See Sect. IV D and (35)).

In Section II-C we will derive drain current vs. time based on (14). Here, if we assume for simplicity that $V_{\rm DS} = 0$, so that $V_{{\rm Ch},S}(y,t) = 0$ everywhere for all time, for constant $V_{\rm GS}$, we can integrate (14) to give the well-known "stretched exponential" expression for threshold voltage shift vs. time [9].

$$\begin{aligned}\Delta V_T(t) &\equiv V_T(t) - V_{T0} \\ &= (V_{\rm GS} - V_{T0})\left\{1 - \exp\left[-\left(\frac{t}{t_0}\right)^{\frac{T}{T_0}}\right]\right\}\end{aligned} \tag{16}$$

where V_{T0} is the initial threshold voltage before the application of gate bias.

The threshold voltage shift will saturate when $n_{\rm ch}$ is zero and there is no more defect formation. Defining the maximum possible threshold shift as $\Delta V_{T,\max}$

$$\Delta V_{T,\max} \equiv V_{\rm GS} - V_{T0.} \tag{17}$$

The stretched exponential expression (16) becomes

$$\Delta V_T(t) = \Delta V_{T,\max}\left\{1 - \exp\left[-\left(\frac{t}{t_0}\right)\right]^{\beta}\right\}. \tag{18}$$

Initially, the threshold voltage shift ΔV_T is zero and then it rises because the exponential term in (18) becomes smaller. For $t \gg t_0$, the exponential term is so insignificant that ΔV_T saturates. When $t = t_0$, $\Delta V_T(t_0) = \Delta V_{T,\max}(1 - e^{-1}) \approx 0.63\ \Delta V_{T,\max}$ and $E_{\rm th} = E_{\rm act}$. We note that hydrogen-diffusion-controlled defect-relaxation (HCR) models [15]–[17] also lead to (18), if we assume the diffusion of hydrogen is a thermally-activated process with a barrier energy E_b and the density of hydrogen atoms with diffusion energy barrier E_b has an exponential function $n_A(E_b) = C_0 e^{E_b/kT_0}$. Thus, for the purpose of fitting experimental results, the defect-controlled defect-relaxation (DCR) model and the hydrogen-diffusion-controlled defect-relaxation (HCR) model are equivalent. For the rest of this paper, we will use the terminology associated with the DCR model.

B. Modeling Charge Trapping in the Gate SiN_x

When channel electrons enter the gate insulator and then are captured by traps there, the threshold voltage shifts. If one assumes that all electrons that enter the insulator are trapped, the threshold voltage shift depends strictly on the process of electron tunneling into the gate insulator and has a logarithmic time dependence [5].

$$\Delta V_T(t) = r_d \log(1 + t/t_0) \tag{19}$$

TABLE I
STRETCHED EXPONENTIAL EXPRESSION FOR INSTABILITY MECHANISMS IN a-Si TFTs

$$\Delta V_T(t) = \Delta V_{T,max}\left\{1 - \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right]\right\}$$

Parameter	Defect creation in a-Si (Stage II)	Charge trapping in gate insulator (Stage I)
$\Delta V_{T,max}$	$V_G - V_{T0}$	$qN_{tot} < d > /\varepsilon \cdot area$
β	A measure of the distribution of defects vs. barrier energy E_b with $\beta = T/T_0$	A measure of width of the distribution of the capture cross section $0 \le \beta \le 1$
t_0	Time scale to reach $\Delta V_{T,max}$. Depends on the attempt-to-escape frequency ν, activation energy E_{act}, and temperature T, with $t_0 = \nu^{-1}\exp(E_{act}/kT)$.	Time scale to reach $\Delta V_{T,max}$. Depends on the gate leakage current and characteristic capture cross section.

The constant r_d contains the density of traps N_T [cm^{-3}] and a tunneling constant λ [cm] [5]. This tunneling mechanism typically dominates at high gate-field stress ($> 10^6$ V/cm) [7], [8] and produces a weak temperature dependence [5].

On the other hand, if most electrons that enter the gate insulator are not trapped and continue to the gate electrode, the threshold voltage shift can be shown to follow the stretched exponential expression as (18) [5], [6], [12], [24]. This expression can be derived by assuming a continuous distribution in the capture cross section of the trapping sites [12]. The parameters $\Delta V_{T,\max}$, β and t_0 in (18), which characterize charge trapping in the gate SiN_x, have physical origins that are different from those to characterize defect creation in a-Si. When all traps in the SiN_x are filled, the threshold voltage shift saturates and reaches $\Delta V_{T,\max}$. Thus, the parameter $\Delta V_{T,\max} = qN_{\rm tot}\langle d\rangle/\varepsilon \cdot$ area, where $N_{\rm tot}$ is the total density of traps, $\langle d\rangle$ is the centroid of trapped charge measured from the gate metal, and ε is the permittivity of the gate SiN_x. β is a measure of the distribution width of capture cross section, with a value between 0 and 1. β decreases as the distribution broadens, and $\beta = 1$ implies a single trap cross section. In principle, the characteristic time t_0 can be determined from the gate leakage current and characteristic capture cross section for the ensemble of traps [12]. In practice, t_0 is determined from (18) as the time when $\Delta V_T = 0.63\ \Delta V_{T,\max}$. Because gate leakage current and capture cross section may depend on temperature [12], the threshold voltage shift also may depend on temperature.

The above charge-trapping model, based on continuous distribution in trapping capture cross section, was first derived to explain the threshold voltage shift in single crystalline Si field-effect transistors with high permittivity dielectric gate insulator, such as Al_2O_3 and HfO_2. When applied to a-Si TFTs with a SiN_x gate insulator, the stretched exponential form of (18) also corresponds well to experimental data, although without connecting to an explicit physical model.

The stretched exponential expression for threshold voltage (18) can be used to model the shifts caused by either defect creation (Section II-A) in a-Si or by charge trapping in the gate SiN_x (this section). The model in either case requires three parameters, $\Delta V_{T,\max}$, β and t_0, the physical origins of which are listed in Table I. It is difficult to determine which instability mechanism is operating in a-Si TFTs from simply observing the threshold voltage shift [24]. However as noted in Section II-A, for defect creation in a-Si, we expect $\Delta V_{T,\max} = V_{\rm GS} - V_{T0}$, while for charge trapping in SiN_x, $\Delta V_{T,\max}$ could be less than $V_{\rm GS} - V_{T0}$ if the number of traps in the gate insulator is small. Such an observation, in practice, would allow one to differentiate between the two instability mechanisms. Furthermore, defect spectroscopy techniques [14] would allow one to observe the newly created defect states in a-Si.

C. Drain Current Degradation Models

1) Effect of Non-Zero Drain-Source Voltage: As noted in Section II-A, the stretched exponential model for drain current degradation, implicitly assuming uniform electron density along the channel (i.e., $V_{\rm DS} = 0$) has been previously developed [25]. However, in devices with drain voltage applied, the electron density and thus local threshold voltage varies along the channel. A first-principles model for drain current degradation with the threshold voltage varying along the channel has not previously been presented. We now rigorously derive the drain current degradation vs. time in this general case when $V_{\rm DS}$ and thus the channel potential $V_{{\rm Ch},S}(y)$ are not zero. With a uniform initial threshold voltage V_{T0} assumed, from (16) the threshold voltage can be expressed as

$$V_T(y,t) = (V_{\rm GS} - V_{{\rm Ch},S}(y,t) - V_{T0})\left\{1 - \exp\left[-\left(\frac{t}{t_0}\right)\right]^{\beta}\right\}. \tag{20}$$

To derive drain current vs. time, we start with the assumption, which we will soon justify, that for constant $V_{\rm GS}$ and $V_{\rm DS}$ that the voltage at any point in the channel $V_{{\rm Ch},S}(y,t)$ remains unchanged with time, i.e., $V_{{\rm Ch},S}(y,t) = V_{{\rm Ch},S}(y)$.

The classical gradual channel approximation in linear mode ($V_{\rm DS} \le V_{\rm GS} - V_{T0}$) gives

$$\int_0^L I_{D,\rm lin}(t)dy = \mu_n W C_{\rm ins}\int_0^{V_{\rm DS}} [V_{\rm GS} - V_T(y,t) - V_{{\rm Ch},S}(y)]dV. \tag{21}$$

Since the changes of mobility were far less significant to the drain current degradation than the changes of threshold voltage in our experiments (e.g., less than 10% mobility degradation when current was reduced to under 15% of its original value (degradation was $> 85\%$) [20]), we neglect mobility changes in our analysis.

Then substitute for $V_T(y,t)$ from (20)

$$I_{D,\mathrm{lin}}(t)L = \mu_n W C_{\mathrm{ins}} \int_0^{V_{\mathrm{DS}}} [V_{\mathrm{GS}} - V_{T0} - V_{\mathrm{Ch},S}(y)] \times \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right] dV = \mu_n C_{\mathrm{ins}} W \left[\left(V_{\mathrm{GS}} - V_{T0} - \frac{1}{2}V_{\mathrm{DS}}\right) V_{\mathrm{DS}}\right] \times \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right]. \quad (22)$$

The saturation current can be found from (22) by substituting $V_{D,\mathrm{Sat}} = V_{\mathrm{GS}} - V_{T0}$ for V_{DS}. In principle, $V_{D,\mathrm{Sat}}$ could be reduced over time if there were defect formation and a rise in the local threshold at the drain end of the channel. However, since $n_{\mathrm{ch}} = 0$ at the drain end of the device ($y = L$), there is no threshold shift at that end of the device and $V_{D,\mathrm{Sat}}$ is unchanged with time. Thus the current degradation in saturation is

$$I_{D,\mathrm{sat}}(t) = \mu_n C_{\mathrm{ins}} \frac{W}{2L} \left[(V_{\mathrm{GS}} - V_{T0})^2\right] \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right]. \quad (23)$$

Defining a normalized current $I_{D,\mathrm{nor}}(t)$ as the current normalized by its value at $t = 0$, we have

$$I_{D,\mathrm{nor}}(t) = \frac{I_D(t)}{I_D(t=0)} = \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right]. \quad (24)$$

In both saturation and low V_{DS} regimes, the current decays according to a stretched exponential model vs. time, with parameters β and t_0 depending on material properties.

Up to this point we have derived an analytical solution for drain current degradation vs. time without changing the channel voltage profile $V_{\mathrm{Ch},S}(y,t)$ as a function of time. By having shown a formal solution which is consistent with this, the assumption of $V_{\mathrm{Ch},S}(y,t) = V_{\mathrm{Ch},S}(y)$, i.e., independent of time, is thus valid.

To further reinforce this surprising and non-intuitive result, we also numerically modeled the threshold voltage increase at each location in the channel as a function of time. At each time point we re-evaluated the potential distribution and carrier density along the channel depending on the previous local carrier density (and thus local resistance) and the local threshold along the channel. The numerical model confirmed that the channel potential vs distance along the channel does not change in saturation [26].

2) Threshold Voltage Fitting Approach in Saturation: We have proved that I_D decays as a stretched exponential for fixed V_{DS} and V_{GS} both for small V_{DS} and in saturation. In practice, the decay is often reported as an effective threshold voltage shift $\Delta V_{T,\mathrm{eff}}(t)$. We stress the word "effective," since if V_{DS} is nonzero, the local threshold voltage varies along the channel. The decay in drain current vs. time is often reported simply as a $\Delta V_{T,\mathrm{eff}}(t)$, where this is the effective shift in a single threshold required to model the drain current at any time using the simple device classical device laws, instead of introducing defects as a function of time and location in the channel [3], [27]–[30].

The a-Si TFT is usually biased in saturation to operate as a current source to drive OLEDs in flat panel display. In saturation, with $V_{D,\mathrm{sat}} = V_{\mathrm{GS}} - V_T$, $\Delta V_{T,\mathrm{eff}}(t)$ can be defined by the square law equation for drain current,

$$I_D(t) = \mu_n C_{\mathrm{ins}} \frac{W}{2L} \left[V_{\mathrm{GS}} - (V_{T0} + \Delta V_{T,\mathrm{eff}}(t))\right]^2. \quad (25)$$

Using the definition of normalized current (24) and $\Delta V_{T,\max} = V_{\mathrm{GS}} - V_{T0}$, $\Delta V_{T,\mathrm{eff}}(t)$ can be solved to be

$$\Delta V_{T,\mathrm{eff}}(t) = \Delta V_{T,\max} \left\{1 - \exp\left[-\frac{1}{2}\left(\frac{t}{t_0}\right)^{\beta}\right]\right\}. \quad (26)$$

By defining an effective characteristic time for saturation, $t_{0,\mathrm{eff}}$

$$t_{0,\mathrm{eff}} \equiv 2^{\frac{1}{\beta}} t_0. \quad (27)$$

The effective threshold voltage shift can be simplified to a stretched exponential expression,

$$\Delta V_{T,\mathrm{eff}}(t) = \Delta V_{T,\max} \left\{1 - \exp\left[-\left(\frac{t}{t_{0,\mathrm{eff}}}\right)^{\beta}\right]\right\}. \quad (28)$$

This is similar to the threshold voltage shift (18) under zero V_{DS}, except for the redefinition of $t_{0,\mathrm{eff}}$, which is due to the variation of n_{ch} and thus shift in ΔV_T along the channel. The effective threshold voltage expression is useful because of its compatibility with circuit simulators.

From (25), the normalized drain current degradation in saturation can be expressed as

$$I_{D,\mathrm{nor}}(t) = \exp\left[-2\left(\frac{t}{t_{0,\mathrm{eff}}}\right)^{\beta}\right] \quad (29)$$

or, in terms of the fundamental parameters,

$$I_{D,\mathrm{nor}}(t) = \exp\left[-\left(\frac{2C_0 k T_0}{n_{\mathrm{ch},o}}\right)(vt)^{\frac{T}{T_0}}\right]. \quad (30)$$

In analogy to (15), we can also define an effective activation energy $E_{\mathrm{act,eff}}$ with

$$E_{\mathrm{act,eff}} \equiv kT\ln(vt_{0,\mathrm{eff}}) = E_{\mathrm{act}} + kT_0\ln(2). \quad (31)$$

III. Sample Preparation and Bias-Temperature-Stress Measurement

Highly stable a-Si TFTs were fabricated with a standard bottom-gate non-self-aligned process in the back-channel passivated (BCP) structure. The silicon nitride and amorphous silicon were deposited in a plasma-enhanced chemical vapor deposition (PECVD) system. 300-nm gate nitride, 200-nm intrinsic hydrogenated a-Si and 300-nm passivation nitride were deposited sequentially at 320 °C, 320 °C, and 220 °C, respectively. The SiN_x and a-Si were patterned with dry-etching. All the samples were annealed at 180 °C for an hour to remove the plasma-induced damage from the dry-etching process [20].

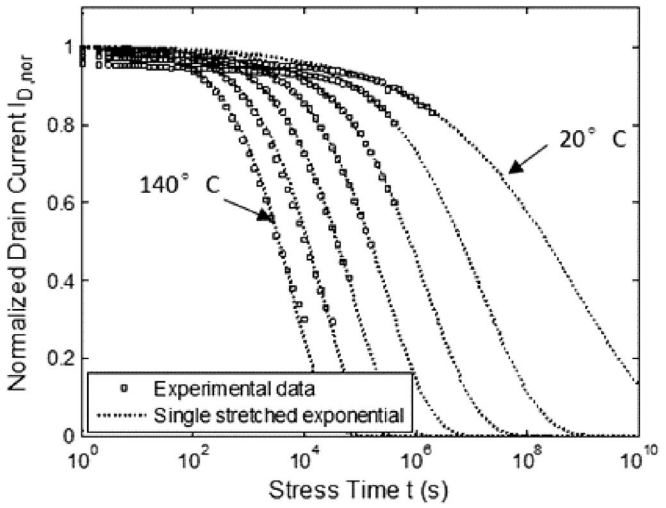

Fig. 4. Single stretched exponential fits to normalized drain current data at temperatures from 20 °C to 140 °C in steps of 20 °C. $V_{\rm GS} = 5$ V, $V_{\rm DS} = 7.5$ V. A fresh TFT was used at each temperature.

After annealing, the initial threshold voltage V_{T0} was 1.0 V and the electron mobility μ_n was 0.9 cm^2/V · s.

The TFTs were biased in saturation with a constant gate-source voltage $V_{\rm GS}$ of 5 V (a gate field of $\sim 1.5 \times 10^5$ V/cm) and a constant drain-source voltage $V_{\rm DS}$ of 7.5 V. Saturation, in contrast to the linear mode, was used because this mode of operation is used for driving OLEDs, an application which demands very high stability [7]. We raised the substrate temperature from 20 °C to 140 °C in steps of 20 °C. At each temperature we biased a fresh TFT on the same substrate without any prior stress and measured the drain current as a function of time. At the end of this period of bias stress, the gate-bias voltage was swept at fixed drain voltage to measure the $I_D - V_{\rm GS}$ characteristics of the TFTs [20]. This measurement provides the electron mobility of the TFT at the end of the stress period. The experimental data points of normalized drain current $I_{D,\rm nor}(t) \equiv I_D(t = 0)$ in function of time at temperatures from 20 °C to 140 °C are shown in Fig. 4.

IV. Experimental Results and Two-Stage Model

A. Single Stretched-Exponential Fit of Current Degradation at Different Temperatures

Fig. 4 shows that at 5 V gate bias, the drain current approaches zero at long times and depends strongly on temperature. We fit the stretched exponential expression of (29) for defect creation in a-Si to the experimental data for each temperature (dotted curves in Fig. 4). Each temperature requires separate fitting parameters $T_0 \equiv T/\beta$ and $t_{0,\rm eff}$, which are plotted in Fig. 5(a) and (b), respectively. Fig. 5(a) shows that the characteristic temperature T_0 of the defect energy distribution changes from 1032 K at 20 °C to 616 K at 140 °C, and that it decreases rapidly in low temperature range. Similar results were reported in [6] and [25]. From the slope of the Arrhenius plot of $\log t_{0,\rm eff}$ [straight line in Fig. 6(b)], the effective activation energy $E_{\rm act,eff} = 0.89$ eV and the attempt-to-escape frequency $v = 4 \times 10^6$ Hz are extracted from (31)

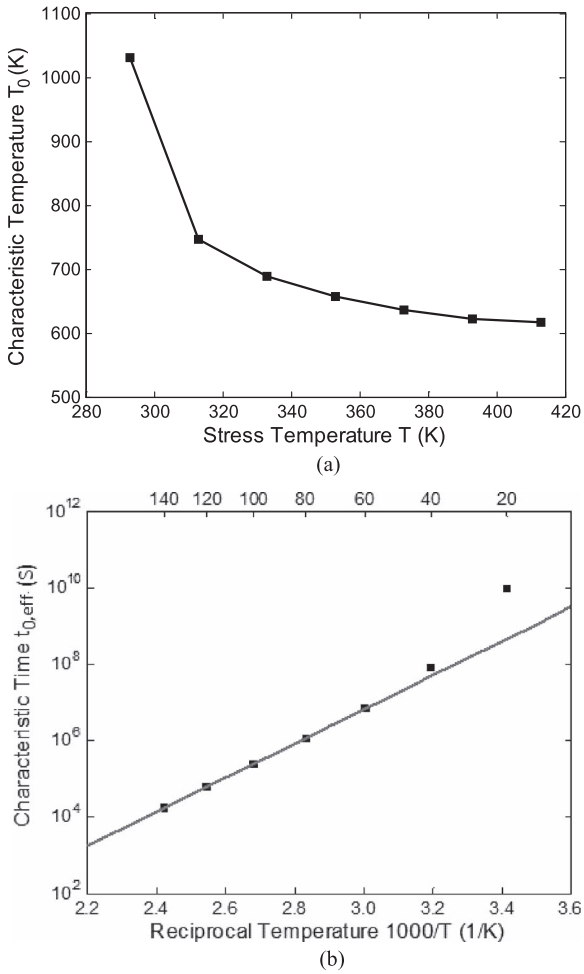

Fig. 5. Fitting parameters for the single stretched exponential fits of Fig. 4: (a) characteristic temperature T_0 as a function of bias stress temperature, and (b) characteristic time $t_{0,\rm eff}$ as a function of reciprocal stress temperature in an Arrhenius plot. Line is a fit with $E_{\rm act,eff} = 0.89$ eV and $v = 4 \times 10^6$ Hz.

$t_{0,\rm eff} \equiv v^{-1} \exp(E_{\rm act,eff}/kT)$. However, the experimental $t_{0,\rm eff}$ does not fall on the straight line at low temperatures.

From the discussion of instability in a-Si of Section II-A and Section II-C, the anomalously large T_0 and $t_{0,\rm eff}$ near room temperature result from either changes in material properties with temperature, or a single stretched exponential fit not being appropriate for the entire temperature range. In Section IV-D, we will show that material properties do not change, and that a second instability mechanism relevant near room temperature (charge trapping in the gate dielectric) for a short time makes the single stretched exponential fit inadequate. Further, much of this effect occurs between 0.1 s after applying gate bias (the time to our first measured point, which we call $t = 0$) and 1.0 s after that point (which is the first plotted time point). This explains why the normalized current curves seem to start at under 1.00 in Fig. 4 near room temperature. At high temperatures, this effect is already over at 0.1 s (the first measurement point).

B. Unification of Time and Temperature

If the instability is caused by defect creation in a-Si and the material properties do not change with temperature, the

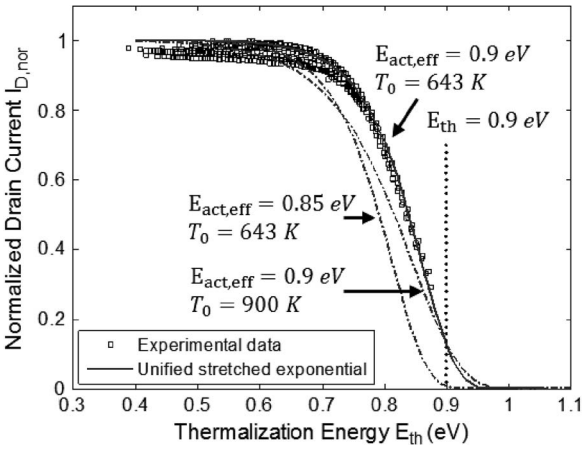

Fig. 6. Data of normalized drain current $I_{D,\mathrm{nor}}$ vs time of Fig. 4 for 7 temperatures (20–140 °C), "unified" by replacing the x-axis of temperature with-thermalization energy $E_{\mathrm{th}} = kT\ln(vt)$, with $v = 5 \times 10^6$ Hz, and one single stretched exponential fit to the unified curves with parameters $E_{\mathrm{act,eff}} =$ 0.90 eV and $T_0 = 643$ K (solid curve). To show the sensitivity to the fitting parameters, dash-dotted curves are single stretched exponential models at $E_{\mathrm{act,eff}} = 0.85$ eV (with $T_0 = 643$ K), or $T_0 = 900$ K (with $E_{\mathrm{act,eff}} =$ 0.90 eV).

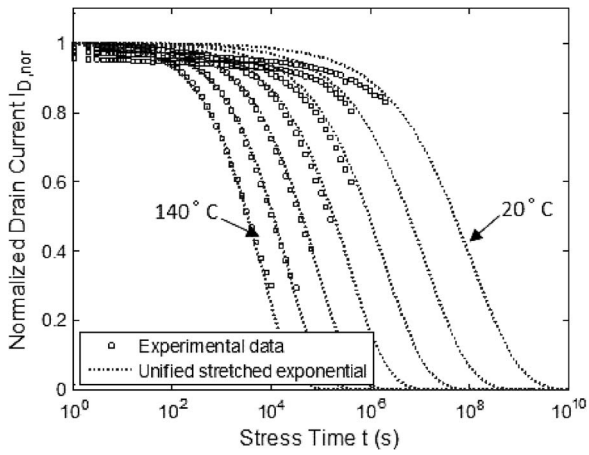

Fig. 7. Unified stretched exponential fits (Stage II) vs. stress times to experimental data from 20 °C to 140 °C in steps of 20 °C, with fitting parameters $v = 5 \times 10^6$ Hz, $E_{\mathrm{act,eff}} = 0.9$ eV and $T_0 = 643$ K.

instability can be captured with a formulation that unifies time and temperature dependence. The definition of the thermalization energy E_{th} of (3) implies that the time scale can be converted to the E_{th} scale. Doing that enables reducing all sets of current vs. time data for different temperatures to a single curve [9]. As discussed in Section II-A, for a given thermalization energy, a given number of bonds has been broken. This leads to a specified change in threshold voltage and drain current. As time t advances and weak bonds with higher barrier energy E_b are broken, the thermalization energy E_{th} increases. Schematically, this is represented by an increase to the area of the shaded region in Fig. 3(a). Temperature affects only how long it takes to reach a given thermalization energy.

Given a set of experimental data of normalized current vs. time at different temperatures as in Fig. 4, we choose parameter v to unite all of the curves when the time axis is replaced with E_{th} [via (3)] This is illustrated in Fig. 6. When v is set to be 5×10^6 Hz, all experimental data on drain current degradation from 20 °C to 140 °C cluster as shown into a single curve shown by the open squares. The fitting parameter v is close to that obtained from Fig. 5(b) of 4×10^6 Hz. This agreement suggests that the material properties remain essentially unchanged between 20 °C and 140 °C in our experiment. This observation gives us confidence for applying the unified stretched exponential fit to drain current degradation that follows. Further, because E_{th} depends logarithmically on v, this small difference in v determined by different approaches is of little practical consequence.

C. Unified Stretched Exponential Fit to Drain Current Degradation (Stage II Model)

By substituting (3) $E_{\mathrm{th}} = kT\ln(vt)$, (31) $t_{0,\mathrm{eff}} \equiv v^{-1}\exp(E_{\mathrm{act,eff}}/kT)$, and (13) $\beta = T/T_0$ into (24), we obtain the unified stretched exponential expression for $I_{D,\mathrm{nor}}$ as a function of thermalization energy E_{th}

$$I_{D,\mathrm{nor}}(E_{\mathrm{th}}) = \exp\left\{-2\exp\left[\frac{E_{\mathrm{th}} - E_{\mathrm{act,eff}}}{kT_0}\right]\right\}. \quad (32)$$

The effective activation energy $E_{\mathrm{act,eff}}$ is related to the barrier energy E_{act} for defect creation when the normalized drain current has dropped to $e^{-2} \approx 0.135$. Note that this unified stretched exponential expression is independent of temperature. The solid curve in Fig. 6 shows that (32) provides an excellent fit to the clustered data. The fitting parameters are $E_{\mathrm{act,eff}} =$ 0.90 eV and $T_0 = 643$ K, which are typical values for a-Si [23]. The dash-dotted curves in Fig. 6 are plotted for $E_{\mathrm{act,eff}}$ of 0.85 eV with T_0 643 K, and for T_0 of 900 K with $E_{\mathrm{act,eff}}$ of 0.90 eV to show the effect of varying $E_{\mathrm{act,eff}}$ and T_0 on the curve fit. Reducing the effective activation energy $E_{\mathrm{act,eff}}$ is seen to shift the current degradation to smaller E_{th} and thus shorter time, while varying the characteristic temperature T_0 affects the slope.

The relation of $E_{\mathrm{th}} = kT\ln(vt)$ between thermalization energy and time enables plotting stretched exponential fits in a direct function of time as shown by dotted curves in Fig. 7. The experimental data fit well at high temperatures from 80 °C to 140 °C. At low temperatures, the experimental drain current degradation lies below the unified stretched exponential fit at short times, but trends toward the unified stretched exponential fit at long times. These observations suggest that an additional instability mechanism causes the drain current to drop at the beginning of the tests. This initial instability mechanism, which is manifest at low temperatures and short times, requires an additional physical model.

D. Two-Stage Model and Discussion

In order to model this initial additional instability at low temperatures, we define the threshold voltage shift caused by the initial instability mechanism as $\Delta V_{T,\mathrm{eff,I}}$ (Stage I), and add it to the long-term threshold voltage shift characterized by the unified stretched exponential model $\Delta V_{T,\mathrm{eff,II}}$ (Stage II), to

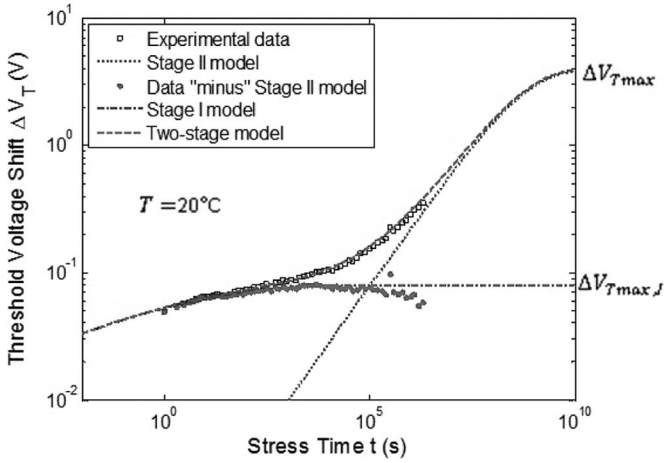

Fig. 8. Two-stage model fits to threshold voltage shift vs. time at 20 °C (dashed curve, overlaps with Stage I curve at lower left and overlaps with Stage II curve at upper right). The dots for Stage I "data" result from subtracting the Stage II model (determined by high temperature experiments) from the experimental data. The fitting parameters for Stage I are $\Delta V_{T,\mathrm{eff,max,I}} = 0.08$ V, $t_{0,\mathrm{I}} = 0.7$ s and $\beta_I = 0.15$; and for Stage II are $t_{0,\mathrm{II}} = 5.2 \times 10^8$ s and $\beta_{\mathrm{II}} = 0.46$.

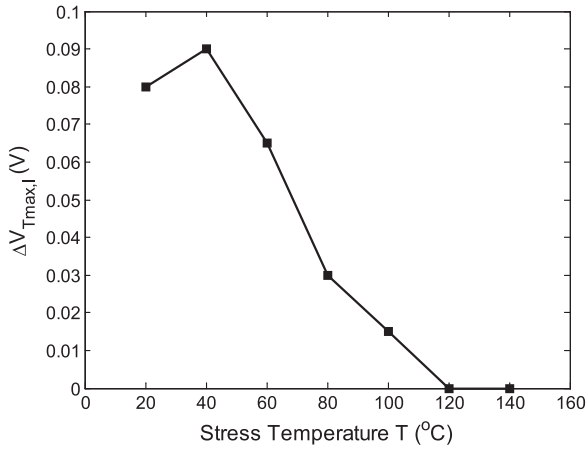

Fig. 9. Maximum threshold voltage shift in Stage I, $\Delta V_{T,eff,\max,\mathrm{I}}$, at temperatures from 20 °C to 140 °C.

obtain the total threshold voltage shift $\Delta V_{T,\mathrm{eff,total}}(t)$

$$\Delta V_{T,\mathrm{eff,total}}(t) = \Delta V_{T,\mathrm{eff},I}(t) + \Delta V_{T,\mathrm{eff,II}}(t). \tag{33}$$

(The terminology of "effective" thresholds is used because the experimental devices are in saturation, with possible non-uniform defect densities from source to drain.)

We first analyze the threshold voltage shift at 20 °C, where the initial instability is most pronounced and which is most relevant for consumer device application. Fig. 8 shows the experimental data points of effective threshold shift vs. time and model fits. Open squares are the experimental data for $\Delta V_{T,\mathrm{eff,total}}(t)$ extracted from the measured drain current data using Eq'n. (25). The dotted curve is the Stage II model (t) from the unified stretched exponential fit in Section IV-C. At long times, the Stage II model approaches the experimental data. However, at short times ($< 10^3$ seconds), a fast initial "Stage I" mechanism makes the threshold voltage shift rise above the unified stretched exponential fit. Stage I degradation saturates at $\Delta V_{T,\mathrm{eff,max,I}} = 0.08$ V, which is marked in Fig. 8. $\Delta V_{T,\mathrm{eff,II}}(t)$ for Stage II is obtained from (18) with $\Delta V_{T,\mathrm{eff,max,II}} = V_{\mathrm{GS}} - V_{T0} - \Delta V_{T,\mathrm{eff,max,I}}$. By subtracting $\Delta V_{T,\mathrm{eff,II}}(t)$ from the total threshold voltage shift vs. time data, $\Delta V_{T,\mathrm{eff,I}}(t)$ is obtained. While the mechanism of Stage I is not strictly known, in any case we can also fit the $\Delta V_{T,\mathrm{eff,I}}(t)$ data with a stretched exponential expression (18) (see Section II-B and Table I).

From Section IV-C, the Stage II (defect creation) parameters are $v = 5 \times 10^6$ Hz, $E_{\mathrm{act,eff,II}} = 0.9$ eV and $T_0 = 643$ K, corresponding to $t_{0,\mathrm{eff,II}} = 5.2 \times 10^8$ s and $\beta_{\mathrm{II}} = 0.46$ at 20 °C. The Stage I parameters are $\Delta V_{T\,\max,\mathrm{I}} = 0.08$ V, $t_{0,\mathrm{eff,I}} = 0.7$ s and $\beta_I = 0.15$, and give the dash-dotted curve in Fig. 8. The two-stage fit of the dashed curve then is obtained by adding Stage I fit and Stage II fit of effective threshold voltage. The result agrees well with the experimental data taken at 20 °C during the entire measurement time.

We also applied the two-stage model to the experimental data taken at temperatures from 40 °C to 140 °C. The maximum threshold voltage shift in Stage I, $\Delta V_{T,\mathrm{eff,max,I}}$, varies with temperature as illustrated in Fig. 9. As mentioned earlier, at high temperature, the Stage I effect saturates before our first measured current point, so thus Stage I is not captured in our measurements. Therefore, at elevated temperatures, the total threshold shift vs. time can be modeled reliably with only the Stage II unified stretched exponential, because the effect of Stage I can be neglected. (We attribute the smaller $\Delta V_{T,\mathrm{eff,max,I}}$ at 20 °C than at 40 °C due to the device to device variation of the Stage I effect, shown in more detail in Part II of this paper.)

Because Stage I saturates at $\Delta V_{T,\mathrm{eff,max,I}}$ at only 0.08 V, far below $V_{\mathrm{GS}} - V_{T0}$ of ~3 V, we attribute the instability mechanism of Stage I to charge trapping in the gate SiN_x, where the trap density is grown-in and independent of the density of electrons in the channel. The threshold voltage shift in Stage II is attributed to defect creation in a-Si, which is induced by the density of electrons in the channel and therefore rises with rising gate bias.

After converting the threshold voltage back to drain current via (25), the two-stage fits to the normalized drain current degradation from 20 °C to 140 °C in steps of 20 °C are shown as dashed curves in Fig. 10. The fits agree well with the experimental data at all temperatures and times, and are much better than the Stage-II-only model (Fig. 7), especially for the early stages of degradation at lower temperature. For 20 °C, relevant for prediction of lifetimes under typical consumer product conditions, a single stretched exponential fit is also given in as a dotted line. Because there are two different underlying mechanisms occurring, as shown in Fig. 8 the single exponential cannot accurately model the predicted device behavior vs. time, and severely underestimates the rate of drain current degradation vs. time compared to the two-stage model. For 50% degradation of current, the single stretched exponential can easily overestimate the device lifetime by a factor of 10. Thus a main conclusion of our work is that gate-bias stress tests conducted only at 20 °C for times shorter than 10^6 seconds [3], [7], [8], may not accurately predict the long term (Stage II) performance.

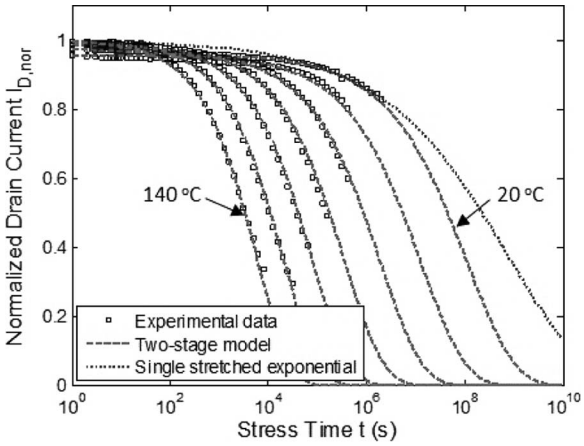

Fig. 10. Two-stage model fit to experimental data from 20 °C to 140 °C in steps of 20 °C (dashed curves), and the single stretched exponential fit at 20 °C (dotted curve at right).

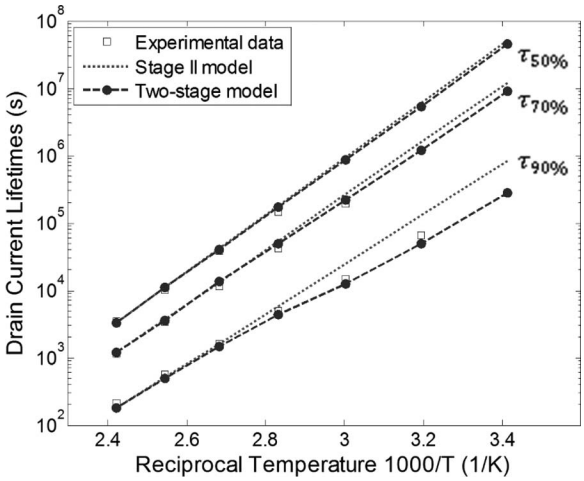

Fig. 11. Time at which the drain current drops to 50%, 70% and 90% of its initial value, as function of temperature. Open squares: experimental data; dotted lines: Stage II model with unified stretched exponential fit; solid dots and dashed lines: two-stage model.

Let's define the time for the TFT drain current under constant gate voltage bias to drop to $x\%$ of its initial value as the $x\%$ drain current lifetime $(\tau_{x\%})$. Fig. 11 demonstrates the 90%, 70%, and 50% lifetimes $(\tau_{90\%}, \tau_{70\%}, \tau_{50\%})$ measured in our experiment (open squares), and the lifetimes extrapolated from only the Stage II model (unified stretched exponential fits, dotted lines) and the full two-stage model (solid dots and dashed lines). Since the threshold voltage shift in Stage I of our highly stable a-Si TFTs saturates at no more than 0.1 V, at long times the threshold voltage shift will be dominated by Stage II. The Stage I fitting parameters are the same as those described above except for $t_{o,\mathrm{I,eff}} = 0.7$ s and $\beta_1 = 0.15$. Note the effect of Stage I is most pronounced for early stages of degradation (e.g. $\tau_{90\%}$) at low temperatures.

In Fig. 11, the slopes of the Stage II model for the 90%, 70% and 50% lifetimes, classical Arrhenius energies for each $\tau_{x\%}$ by definition, are 730, 800, and 840 meV, respectively. They are larger for higher degradation levels. Physically, at the end of the process for higher amounts of degradation, stronger bonds are being broken and the thermalization energy E_{th} is higher. Analytically, from (29)–(31), the time $\tau_{x\%,\mathrm{II}}$ for the current to decrease to x percent of its original value in stage II is

$$\begin{aligned}\tau_{x\%,\mathrm{II}} &= \left(\frac{-\ln(x\%)}{2}\right)^{\frac{T_0}{T}} t_{0,\mathrm{eff,II}} \\ &= \left(\frac{-\ln(x\%)}{2}\right)^{\frac{T_0}{T}} \left(\frac{1}{v}\right) \left(\frac{n_{\mathrm{ch},o}}{C_0 k T_0}\right)^{\frac{T_0}{T}} \\ &= \left(\frac{1}{v}\right) \left(\frac{-\ln(x\%)}{2}\right)^{\frac{T_0}{T}} e^{\frac{E_{\mathrm{act,eff}}}{kT}} = \left(\frac{1}{v}\right) e^{\frac{E_{\mathrm{act},\tau\mathrm{x,II}}}{kT}}\end{aligned} \tag{34}$$

The last line implicitly defines the classical Arrhenius energy for $\tau_{x\%,\mathrm{II}}$, which is

$$E_{\mathrm{act,eff},\tau x,\mathrm{II}} = E_{\mathrm{act,eff}} + kT_0 \ln\left(\frac{-\ln(x\%)}{2}\right). \tag{35}$$

Using (35), and model parameters of $\beta = 0.46$ and $E_{\mathrm{act,eff}} = 900$ meV, one predicts $E_{\mathrm{act,eff},\tau x,\mathrm{II}}$ of 737, 805, and 842 for the 90%, 70%, and 50% lifetimes, closely matching the observed slopes in Fig. 11.

V. Conclusion

Defect creation in a-Si TFTs under low gate fields with drain voltage bias (where the electron density and thus local threshold shift vary along the channel) has been formally shown to result in a stretched exponential degradation of the drain current with time, and related to an effective shift in the threshold voltage, both in linear and saturation modes. This model combined with a similar one for charge trapping were used to model the drain current degradation and threshold voltage shift of a-Si TFTs under low gate-field stress between 20 °C and 140 °C. Over most of the time-temperature range, the unified stretched exponential model that reflects defect creation in the a-Si channel is most important, and all current vs. time curves can be unified with a single fitting parameter. Near room temperature, a separate mechanism contributes to initial TFT degradation. While this mechanism makes only a minor contribution to the overall threshold voltage shift and drain current degradation, it can considerably impact TFT lifetimes extrapolated from tests done at room temperature, showing the necessity of temperature-dependent measurements to reliably find device lifetimes.

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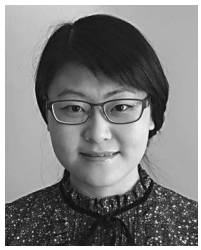

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