

Role of Majority and Minority Carrier Barriers Silicon/Organic Hybrid Heterojunction Solar Cells

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Solar cells based on crystalline silicon offer high efficiency but they are expensive not only due to the cost of the silicon wafers but also due to the high temperatures required to fabricate p–n junctions.^[1,2] The alternative approach using organic solar cells is potentially cheaper due to low-temperature processing, but the organic devices are not very efficient.^[3] Here we demonstrate a hybrid approach to solar cells in which an organic semiconductor deposited on top of silicon at low temperatures is used to replace the silicon p–n junction. It must also be noted that in the hybrid solar cell light is still predominately absorbed in silicon, so the efficiency can theoretically be very high, but the junction formation is done at room temperature so manufacturing costs are low. Thus, a hybrid device exploits the advantageous properties of both organic and silicon to enable potentially low-cost and efficient solar cells.

Previous work on hybrid silicon-organic heterojunction photovoltaic devices has demonstrated a low power conversion efficiency of 2 to 5%,^[4–7] and the crucial role of band offsets on open-circuit voltage and photocurrent was not clarified.

In this work, we identify and experimentally demonstrate how the design of band offsets at the silicon/organic interface relates to both electrons and hole currents. We show that using careful band-engineering, both the photocurrent and open-circuit voltage can be independently tuned in these devices. We then use these insights to demonstrate an unoptimized silicon/organic heterojunction cell with 10.1% AM1.5 efficiency.

While light is easily absorbed in crystalline silicon, extraction of the photogenerated electrons and holes typically requires the fabrication of a p–n junction.^[1,2] On the surface of a n-type wafer, the p-type layer (Figure 1a) serves two functions: 1) it creates a built-in electric field to separate the photogenerated electrons and holes to yield a photocurrent (solid lines in Figure 1a) and b) it presents a barrier to electrons, reducing their recombination at the anode (dotted line in the conduction band in Figure 1a). Lower electron recombination leads to a lower saturation current density of the device (J_0 : also called the

pre-exponential constant), which in turn leads to a larger open circuit voltage (V_{OC}) according to the well known relation:^[8]

$$V_{OC} = \frac{nkT}{q} \ln \left(\frac{J_{sc}}{J_0} \right) \quad (1)$$

where, J_{SC} is the short-circuit current density and is generally equal to the photocurrent, q is the charge of an electron, n is the ideality factor, k is the Boltzmann constant, and T is the temperature. To attain high open-circuit voltages, the saturation current density needs to be very low. The saturation current density of well engineered p–n junctions can be as low as 10^{-13} A cm⁻², which allows these cells to achieve very high power conversion efficiencies (>20%).^[2] However the performance comes at a price; the high temperatures and ultraclean materials required to fabricate the p–n junction make these solar cells very expensive.

The Schottky barrier, fabricated by depositing a metal with high work function on n-type silicon, could be a lower-cost alternative to p–n junctions. As is the case for p–n junctions, it has a built-in electric field that can separate electrons and holes, generating a high photocurrent (Figure 1b). However, the barrier that impedes the recombination of electrons at anode is relatively small, resulting in a saturation current density that is typically much larger than that of p–n junction diodes (> 10^{-7} A cm⁻²).^[9] This is also the reason why the open-circuit voltages of Schottky barrier solar cells are only 0.3 V,^[10] instead of 0.6 to 0.7 V typical for p–n junction silicon solar cells.^[2]

The work described in this paper improves the photovoltaic performance of the Schottky barrier device by reducing the electron recombination at the anode. This is achieved by inserting an organic semiconductor, with a wider energy gap than 1.1 eV, between the silicon and the metal (Figure 1c), such that the lowest unoccupied molecular orbital (LUMO) of the organic is much higher than the conduction band minimum (E_C) of Si. This E_C -LUMO offset presents a large barrier, confining the electrons in silicon, which otherwise would have recombined at the anode. This should lead to a lower saturation current density and hence a larger open-circuit voltage. However to maintain the short-circuit current, the organic layer must not block the photogenerated holes traveling from silicon to anode (Figure 1d, illustrates the counter example). The hole barrier, given by the E_V -HOMO offset, should be very small, i.e., the HOMO of the organic should also be very close to valence band maximum (E_V) of the silicon. Finally, to minimize resistive losses, the hole mobility of the organic layer should also be reasonably high.

Formation of such straddling gap (type I) heterojunctions on silicon using inorganic semiconductors is a difficult problem.^[11,12] However, organic semiconductors can be easily layered on top of silicon using low-cost solution processing.

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DOI: 10.1002/adma.201102712

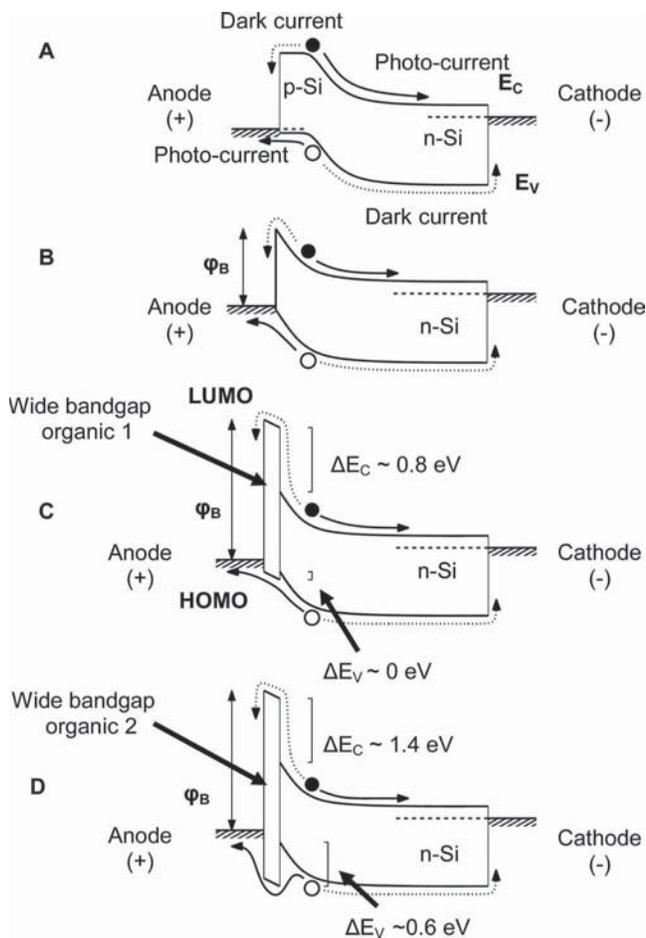


Figure 1. Band diagrams of photovoltaic devices under small forward bias. The filled and hollow dots represent electrons and holes, respectively. The dashed lines represent the dark current, or equivalently, the current due to recombination. The bold lines show the photogenerated current. A) A p–n junction solar cell. B) A silicon/metal Schottky barrier solar cell. C) An silicon/organic heterojunction solar cell with a large LUMO– E_C offset to block electron recombination at the metal anode. D) An silicon/organic heterojunction solar cell with a large HOMO– E_V offset, so the photogenerated hole current is impeded.

Organic semiconductors also offer a large design space to tailor the physical and electrical properties of thin films by manipulating the chemical structure.^[13] All these advantages make the task of designing and fabricating silicon/organic heterojunctions (SOH) considerably simpler.

In this report we have used a well-known conducting polymer poly(3-hexylthiophene) (P3HT). The highest occupied molecular orbital (HOMO) and LUMO edges of P3HT are at 5.1 eV and 3.2 eV, respectively,^[14] compared to 5.17 eV and 4.05 eV for E_V and E_C of silicon, respectively. Thus we expect a large E_C –LUMO barrier of ≈ 0.8 eV, and a negligible E_V –HOMO barrier at the silicon/P3HT interface. Among organics thin films, P3HT also boasts of a high bulk mobility of $\approx 10^{-4}$ V cm⁻¹ s⁻¹.^[15]

To experimentally verify that the Si/P3HT interface satisfies the two key band-alignment criteria, diodes with the structure shown in **Figure 2a** were fabricated, and their current–voltage

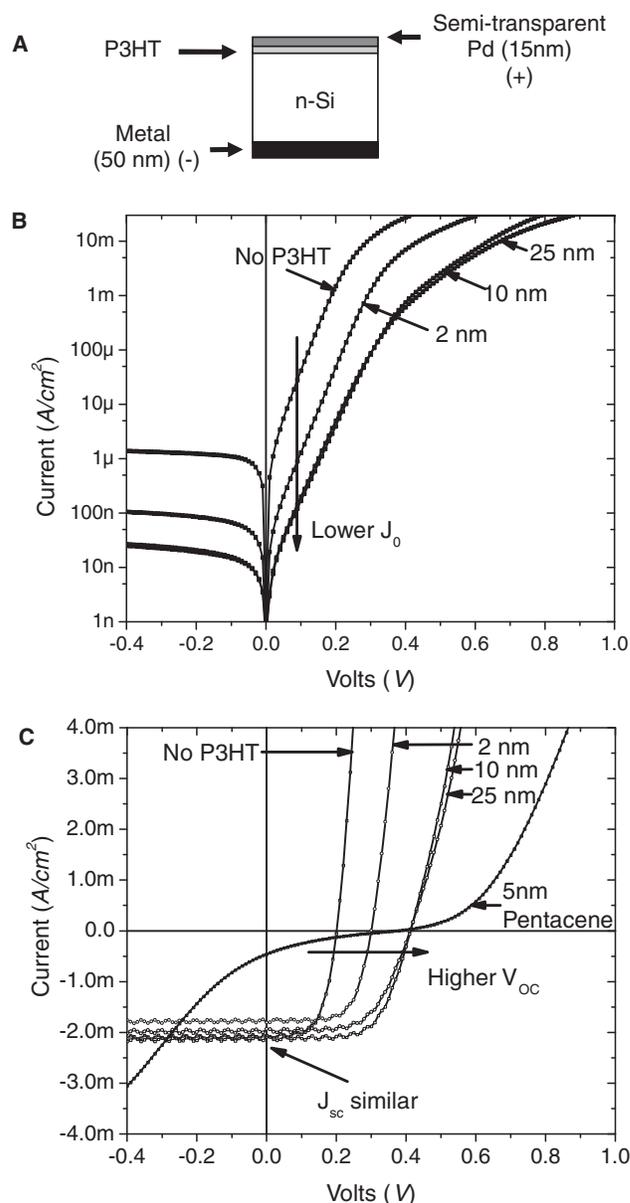


Figure 2. Effect of P3HT layer on current–voltage characteristics. A) Structure of the device. The device area is 3.14×10^{-2} cm². B) Current–voltage characteristics in the dark of SOH diodes with different P3HT layer thicknesses. C) Current–voltage characteristics of the same devices under illumination. To illustrate the detrimental effect of large HOMO– E_V offset (Figure 1d), the characteristic of a silicon/PQ/pentacene heterojunction is also shown.

characteristics were measured with and without light. The active area of the device, as defined by the top electrode, was 3.1×10^{-2} cm². To allow light absorption in Si, the top metal (Pd) electrode in these devices was made semi-transparent by keeping it very thin (15 nm).

The current–voltage characteristics measured in the dark for the different thicknesses of P3HT layer (2, 10, and 25 nm) and a control device without P3HT are shown in **Figure 2b**. Clearly the currents in forward and reverse bias are lower for

devices with thicker P3HT films. The diode saturation current density, extracted from the intercept on the vertical axis from the log(current)–voltage graph, falls from a high of 10^{-6} A cm $^{-2}$ for diodes with no P3HT to 3.7×10^{-9} A cm $^{-2}$ for diodes with P3HT. It is well known that the dark current in a Schottky diode is dominated by majority carrier injection (electron injection in n-type Si) into the metal anode,^[16] so this reduction in current is clear evidence for reduced electron current. P3HT is an ambipolar conductor that conducts electrons^[15] but the currents in these devices do not scale exactly with P3HT thickness. This allows us to further conclude that the shift in curves is not just due to a resistive drop across the P3HT layer but is due to the electron barrier at the Si/P3HT interface.

To test the transport of holes, current–voltage characteristics were measured under illumination from a microscope lamp (Figure 2c). The intensity of the lamp caused a short-circuit current of ≈ 4 mA cm $^{-2}$ in a commercial silicon diode with an antireflection coating and no blocking metal, roughly corresponding to one-tenth the intensity of sunlight. At zero bias, holes that are photogenerated in silicon must cross the Si/P3HT interface before being collected at the anode. Any impediment in this transport due to a barrier between the valence band and the HOMO of P3HT would lead to a reduced short-circuit current. In devices both with and without P3HT, the values of short-circuit current were similar (≈ 2 mA cm $^{-2}$). This suggests a lack of any hole barrier, hence the HOMO of the P3HT must be closely aligned to the valence band edge of silicon.

As mentioned before, the J_0 of the best heterojunction device is lower than J_0 of the Schottky device, 3.7×10^{-9} A cm $^{-2}$ instead of 1.0×10^{-6} A cm $^{-2}$ (Figure 2). Furthermore, the ideality factor (n) of the Si/metal Schottky device is equal to 1, while for SOH devices n is equal to 1.2. Substituting both these parameters in Equation 1 at a photocurrent of ≈ 2 A cm $^{-2}$, we can calculate the theoretical open-circuit voltage, which for the heterojunction cells is expected to be 0.20 V higher than for Schottky devices. This is confirmed in experiments, where the measured V_{OC} shows an increase from 0.20 V to 0.41 V. Overall the results are consistent with the proposed mechanism, where the larger electron barrier results in a lower saturation current density.

To illustrate the detrimental effect of a hole barrier, we fabricated organic heterojunction diodes with a known non-zero of E_V –HOMO offset (band structure in Figure 1d). The interface between n-type Si and 9,10-phenanthrenequinone (PQ) is a system with a known E_V –HOMO offset (0.6 eV).^[17] Pentacene is a well-known hole conductor with HOMO and LUMO energy levels of 5.0 eV and 2.8 eV respectively,^[18] which gives the Si/pentacene interface a large E_C –LUMO offset (1.4 eV). If both organics, PQ and pentacene, are deposited on silicon to form Si/PQ/pentacene heterojunction, the resulting diodes will have large offsets at both the conduction and valence bands. Thus a Si/PQ/pentacene diode would block not only electrons but holes as well. Figure 2c shows the current–voltage characteristic under illumination of one such diode. The electron barrier reduces J_0 , allowing a high open-circuit voltage of 0.4 V. Unfortunately, the hole barrier blocks the photocurrent as well and the fill factors are very poor. The performance of the cell is degraded to such an extent by the E_V –HOMO offset that despite the increase in V_{OC} , the power conversion efficiencies of Si/PQ/pentacene diodes is lower than that of Si/metal devices.

In summary, hole barriers due to non-zero E_V –HOMO offset severely degrade device performance.

For even further improvements in saturation current density of the Si/P3HT device, an understanding of the dominant component of the dark current is required. For a n-Si/metal device in forward bias, the electron current dominates saturation current density (the dotted line in the conduction band of Figure 1b). However, the minority carrier (hole) current, from the metal to the n-type silicon (the dotted curve in the valence band of Figure 1b), also contributes a small part to the saturation current density.^[19] We have already established that E_C –LUMO barrier at the P3HT/Si interface blocks the electrons (majority carriers) but has little effect on the holes (minority carriers). Therefore, in the devices with P3HT, it is possible that the electron current is reduced to a point where the hole current starts to dominate the saturation current density. Further increases in open-circuit voltage would then require a reduction in the hole injection rather than reduction in electron injection.

It is well known that the minority carrier injection current into n-type silicon at a given voltage can be reduced by increasing the n-type doping level (N_D) and/or increasing the minority carrier lifetime in the silicon (τ_R), as give by the relation^[20]

$$J_{\text{minority}} \propto \frac{1}{N_D} \frac{1}{\sqrt{\tau_R}} \quad (2)$$

To test the hypothesis that holes might be the dominant source of dark current, we switched from wafers grown by a Czochralski (CZ) process, used in the experiments of Figure 2, to wafers grown by the float zone (FZ) process. FZ wafers have higher τ_R of ≈ 10 ms^[21] compared to < 1 ms for CZ wafers.^[22] The doping of these wafers was also 6×10^{15} cm $^{-3}$, which is higher than doping of the CZ substrates used in earlier experiments ($\approx 4 \times 10^{14}$ cm $^{-3}$). These higher doped FZ substrates resulted in an even higher V_{OC} of 0.45 V (Figure 3), suggesting that the dark currents in P3HT/Si devices of Figure 2 were indeed dominated by hole injection from the anode into silicon, and not electron injection from silicon into the anode.

To decrease light absorption in the semitransparent anode, the blanket Pd layer was replaced by a spin-coated 80 nm thick layer of the conductive organic poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS). This PEDOT:PSS layer is far more transparent than the Pd layer, but not as conductive in the lateral direction. To improve the lateral resistance, a metal grid shadowing $\approx 10\%$ of the surface area was also integrated on top of the PEDOT:PSS electrode (Figure 4a). The metal grid itself consisted of a 15 nm layer of Pd and a 250 nm thick layer of Ag. This dual metal layer is important because it allowed the electrode to have a high work function (due to Pd) as well as low resistivity (due to Ag). The active area of the solar cell is 4 mm \times 4 mm.

In dark, the current–voltage characteristics of SOH device clearly shows a diode-like behavior (Figure 4b). For comparison a Si/metal Schottky barrier device without the organic layer and only the metal grid was also measured (Figure 4b). The SOH device has a much lower J_0 ($\approx 9 \times 10^{-9}$ A cm $^{-2}$) than the Si/metal device ($\approx 4 \times 10^{-7}$ A cm $^{-2}$). The ideality factor of the heterojunction device is 1.37, while that of the Si/metal device is 1.

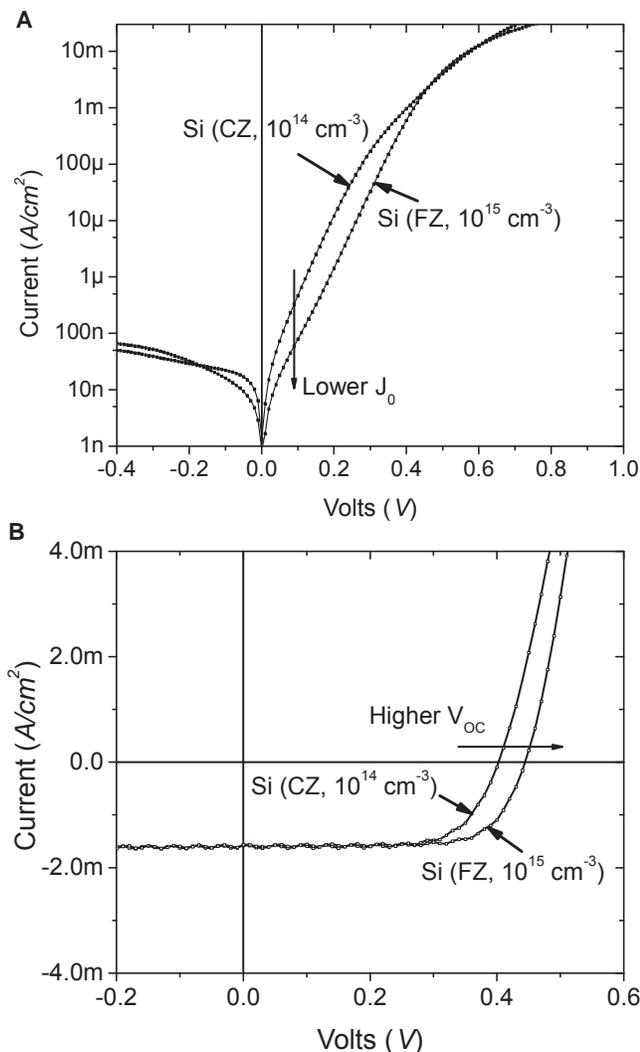


Figure 3. Effect of silicon substrate type. A) Current–voltage characteristics in dark for P3HT/silicon devices with different substrates. B) Current–voltage characteristics under illumination of the same set of devices.

Under AM 1.5 illumination, the reduced J_0 , leads to an increased open-circuit voltage (Figure 4c). The hybrid heterojunction device has an open-circuit voltage of 0.59 V. At this early stage of demonstration, this compares very well with highly engineered silicon solar cells with diffused p–n junctions, which typically exhibit open-circuit voltage of 0.6–0.7 V.

The measured short-circuit current density is 29 mA cm^{-2} , which is only about 30% lower than the theoretical maximum of 42 mA cm^{-2} .^[2] Using a calibrated silicon diode, we have performed transmission experiments to measure the absorption losses in the layers on top of silicon. The PEDOT:PSS/P3HT stack accounts for a 9% reduction in short-circuit current, while the top metal grid accounts for a further 10% reduction in short-circuit current. The rest of the loss in short-circuit current ($\approx 10\%$) can be accounted for by the reflections off the silicon and organic surface, which at present has no light trapping or antireflection structures. The overall power efficiency of

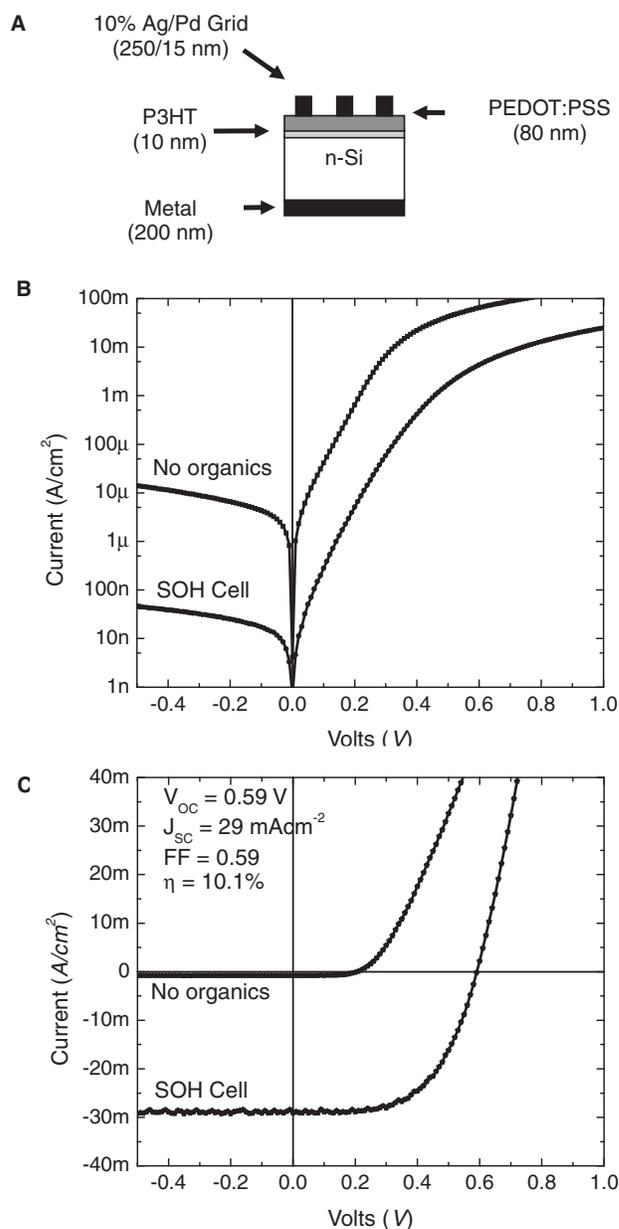


Figure 4. Solar cell. A) Structure of the Si/P3HT heterojunction solar cell. B) The current–voltage characteristics in the dark of a SOH solar cell and a device without a PEDOT/P3HT stack. C) The current–voltage characteristics of the same devices under AM1.5 illumination.

the device is 10.1%, which could be improved by lowering the series resistance, for example by using a finer metal grid.

In summary, we have demonstrated a hybrid silicon/organic heterojunction for photovoltaic applications that is a viable low-temperature alternative to the traditional p–n junctions for silicon-based solar cells. We have outlined the crucial design parameters for efficient photovoltaic operation on n-type silicon wafers: 1) a low offset between silicon valence-band and the HOMO for a high photocurrent and 2) a large offset between the silicon conduction band and organic LUMO for a high

open-circuit voltage. The silicon/P3HT interface satisfies these requirements and using it we have demonstrated a 10.1% efficient silicon/organic heterojunction solar cell. Silicon/organic hybrid heterojunctions are a new approach towards photovoltaic devices that harness the advantageous properties of both organic and inorganic materials.

Experimental Section

Unless otherwise stated, all devices were fabricated on crystalline phosphorous-doped silicon wafers. Regioregular (>95%) P3HT with an average molecular weight of $\approx 46\,000\text{ g mol}^{-1}$ was bought from Merck KGaA and high-conductivity grade PEDOT:PSS (2.2–2.6% in H_2O) was bought from Sigma Aldich.

Device fabrication began by first cleaning the silicon surface by the RCA recipe^[23] followed by a HF dip to etch away the native-oxide layer. On top of this H-passivated surface the organic layer (P3HT) was spin-coated from a solution in chlorobenzene. To vary the P3HT layer thickness, the concentration of P3HT in the casting solution was changed. If needed, the PEDOT:PSS layer was also deposited by spin-coating. The top and bottom metal electrodes were deposited by thermal evaporation in a vacuum chamber with base pressure of 10^{-6} mbar.

All layer thicknesses were measured by a KLA-Tencor surface profilometer. Electrical measurements were acquired with an Agilent/Hewlett-Packard 4155 parameter analyzer. For AM 1.5 measurements, a xenon lamp solar simulator (Opti-Beam 1000 manufactured by Optical Radiation Corporation) was used and provided illumination nominally at AM 1.5G (1000 W m^{-2}) over a 6-in. diameter circle. The power density in the center $\approx 4.5\text{ cm}^2$ of the simulator output was measured using a bolometer to be 103 mW cm^{-2} (vs. the expected 100 mW cm^{-2} for AM1.5), implying that the photon flux of the simulator was within 3% of a true AM 1.5 illumination. All measurements were taken at the center of the light beam so spatial non-uniformity is not expected to be an issue. As measured by a silicon photodiode (manufactured by United Detector), day-to-day variations in the light intensity were typically less than 3% and were corrected for before a photovoltaic device was tested. While the absolute power level of the simulator was calibrated, the distribution of power across the optical spectrum was not checked. The uncorrected spectrum could cause an error in the reported AM1.5 efficiencies, so to be cautious the error in our power calibrations was estimated to be less than 10%.

Acknowledgements

The work was supported by the National Science Foundation under the Princeton MRSEC grant (DMR-0819860).

Received: July 14, 2011

Revised: September 1, 2011

Published online: November 23, 2011

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