# Self-Aligned Amorphous Silicon Thin-Film Transistors Fabricated on Clear Plastic at 300 °C

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***Abstract*—We fabricated back-channel-cut and back-channel-passivated hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) on clear-plastic (CP) foil substrates using a silicon nitride ($SiN_x$) deposition temperature of 300 °C. The TFTs were fabricated on CP and are as stable under high gate bias as TFTs made on glass substrates. A self-alignment technique was developed to align the channel passivation, the a-Si:H island, and the source/drain (S/D) terminals to the gate. Self-alignment allowed us to fabricate discrete TFTs across $7 \times 7$ cm$^2$ of a free-standing sheet of CP foil to reduce the TFT channel length $L$ to 3 $\mu$m and reduce the S/D overlap with the gate $L_{SD}$ to ∼1 $\mu$m. To test the self-alignment techniques, we fabricated ring oscillators on the CP substrates. These results show that it is possible to fabricate state-of-the-art self-aligned a-Si:H TFTs and TFT circuits on plastic substrates.**

***Index Terms*—Amorphous silicon (a-Si:H) thin-film transistors (TFTs), flexible electronics, self-alignment.**

## I. Introduction

Display backplanes based on amorphous silicon (a-Si:H) thin-film transistors (TFTs) are routinely fabricated on rigid-glass substrates. Backplanes fabricated on flexible substrates are expected to find new applications and could be more rugged, lightweight, and cheaper if fabricated using a roll-to-roll process [1]. Desirable flexible-substrate properties include the ability to withstand high processing temperatures (i.e., that have a high glass transition temperature or $T_g$), a low coefficient of thermal expansion (CTE), and a smooth surface. Both plastic [2]–[4] and steel foil [5], [6] have been used as substrates for successful a-Si:H TFT fabrication processes. Commonly used commercial clear plastics (CPs) generally have low CTE values but suffer from low glass transition temperatures—for example, polyethylene naphthalate has a $T_g$ of 120 °C and a CTE of 13 ppm/°C, and polyethylene terephthalate has a $T_g$ of 70 °C–110 °C and a CTE of 15 ppm/°C. In comparison, steel foil is attractive for flexible-display applications due to its high melting point ($T_g = 1400$ °C) and low CTE of ∼18 ppm/°C [7]. However, untreated steel foil has a high surface roughness of $> 1000$ nm as rolled and needs to be coated with a thick passivation layer to achieve a smooth surface [6]. A key advantage to using CP substrates instead of steel foil is that certain flexible displays (for example, transmissive displays [8] and bottom-emitting organic light-emitting displays [9]) require substrates to be optically transparent. Our collaborators have developed CP substrates with a CTE of $< 10$ ppm/°C, $T_g > 300$ °C, and a surface roughness of around 14 nm [3]–[5]. These material properties make our clear substrates competitive with steel foil, and they are highly promising as substrates to fabricate high-performance a-Si:H TFT circuits.

To fabricate flexible displays on CP substrates while still achieving a display performance equivalent to that of devices fabricated on commercially available rigid glass substrates, it is necessary to fabricate functional display pixels, including state-of-the art a-Si:H TFTs [10]. However, the fabrication of functional a-Si:H TFTs on plastic substrates, particularly over large surface areas, is more challenging than on glass substrates. Fabricating a-Si:H TFTs on CP substrates that achieve a "glasslike" electrical stability [11] is even more challenging. In this paper, we address the challenges in fabricating flexible displays on CP substrates and demonstrate our process by fabricating functional TFT circuits across the entire $7 \times 7$ cm$^2$ working area of our flexible plastic substrate by using self-alignment between the device layers.

Stable a-Si:H TFTs are fabricated commercially using plasma-enhanced chemical vapor deposition (PE-CVD). The a-Si:H and n$^+$ doped a-Si:H (which are replaced by n$^+$ nc-Si:H in our devices) device layers are deposited at an optimal deposition temperature $T_{\text{deposition}} = 250$ °C [12] and the $SiN_x$ gate dielectric layer at $T_{\text{deposition}} = 300$ °C–350 °C [13]. However, to accommodate the low process temperatures of commercial clear polymers [14], the trend has been to reduce $T_{\text{deposition}}$ to as low as 75 °C [15]. While the stability of TFTs fabricated using a-Si:H and $SiN_x$ layers deposited at 150 °C has been improved [16], the work carried out by our group indicates that a deposition temperature above 250 °C [17] as well as high RF deposition power during PE-CVD deposition of the $SiN_x$ layer [18] are required to achieve glasslike TFT stability under high gate bias. The high-field stability is determined by electron injection into the gate nitride, which is reduced when the $SiN_x$ is deposited at high temperature and RF power. The TFT stability at low gate field is determined by defect creation in the a-Si:H channel, which is kept low by depositing the a-Si:H layer at 250 °C and with hydrogen dilution growth [3].

Depositing device layers at such high temperatures introduces large and varying mechanical strains into the substrate/device-layer composite structure [19], [20]. Therefore, when using standard photolithography to align the device

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layers, it becomes impossible to fabricate functional TFTs over the entire plastic substrate. To obtain functional devices over the entire surface area, one needs to implement one of the following methods: 1) control the strain by adjusting the stress in certain device layers [19]—however, stress design for the entire backplane has not yet been developed; 2) temporarily bond the substrate to a rigid carrier [21]; 3) design photolithography masks with very large tolerances; or 4) implement self-alignment methods between critical device layers [22]–[29]. The alignment of layers patterned by self-alignment is not affected by the strain developed during layer deposition. To prepare for future roll-to-roll processing, we investigate self-alignment as a tool for fabricating functional TFTs over the entire surface area of our CP substrate.

Self-alignment is a broad term covering various methods used to align device layers *in lieu* of standard photolithography. The distinguishing feature of self-alignment methods is that they resort to a previously patterned layer as a mask to pattern a subsequent device layer. This is in contrast to a standard photolithographic process, where patterns are transferred from a succession of glass masks to the top device layer. Usually, the device layers that act as "masks" in self-alignment processes are opaque metal layers, such as the patterned gate electrodes. Self-alignment processes that have been attracting attention include ion implantation followed by laser annealing to form the source/drain (S/D) contacts [24], chromium silicide formation [25], and exposure of the photoresist from the backside to pattern TFTs on glass [26]–[28] and CP [29].

The method described in [29] aligns the channel passivation to the gate electrode of a-Si:H TFTs; however, this is only one of the overlaps that is critical for fabricating functional back-channel-passivated TFTs over the entire substrate surface. Equally critical is the overlap between the S/D electrodes and the gate electrode. Therefore, we adapted the self-alignment method of [29] to also align the S/D electrodes to the gate electrode. Finally, in an effort to self-align as many device layers as possible to the gate electrode, we also self-aligned the a-Si:H island to the gate electrode.

In the following sections, we describe the fabrication methods that were developed to fabricate standard a-Si:H TFTs (without self-alignment), self-aligned TFTs, and ring oscillators. Results are evaluated as follows: Individual TFTs are evaluated by measuring their current–voltage characteristics and extracting the electron field-effect mobility and high-field electrical stability. The alignment that can be achieved between various device layers using standard (nonself-aligned) and self-aligned TFT fabrication methods is evaluated by comparing the TFT yield over the substrate surface for each respective method. Finally, we evaluate ring oscillators fabricated using standard and self-aligned TFTs and evaluate them by measuring propagation delay and power consumption per oscillator stage.

## II. Device Fabrication

### A. Substrate Choice

The choice of flexible substrate is important for developing a successful high-temperature self-aligned a-Si:H TFT fabrication process. The most important substrate property required to develop a high-temperature process is an ability to withstand the maximum processing temperature, which, in our work, is 300 °C during $SiN_x$ deposition. This means that the temperature at which the substrate softens, known as the glass transition temperature $T_g$, needs to be higher than 300 °C. The higher the $T_{\text{deposition}}$ is, the more important it becomes to have a substrate with a low CTE to minimize the thermal strain that develops in the inorganic device layers deposited on the plastic substrate [19], [20]. Finally, an essential requirement for implementing backside self-alignment is the ability to expose the photoresist through the substrate [29]—therefore, we require an optically CP. In our work we used a 7.5 cm $\times$ 7.5 cm optically CP substrate designed to have a CTE of $< 10$ ppm/°C and $T_g > 300$ °C. The mask area was 7.0 cm $\times$ 7.0 cm. All substrates were processed as free-standing foils held loosely in a frame [30]. During photolithography, the substrates were temporarily bonded to a glass backing slide using a thin film of deionized (DI) water.

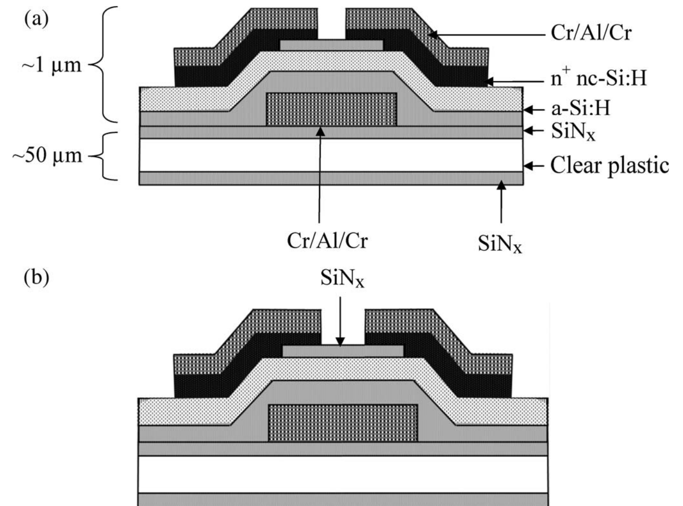


Fig. 1. a-Si:H TFT configurations: (a) Back-channel cut. (b) Back-channel passivated.

### B. Standard TFT Fabrication Process

We fabricated a-Si:H TFTs in both the back-channel-cut—Fig. 1(a)—and the back-channel-passivated—Fig. 1(b)—geometries, using both standard photolithography and self-alignment between various device layers. In this paper, we classify the fabrication processes by the maximum temperature that the substrate is exposed to. Therefore, referring to a 300 °C fabrication process implies a $SiN_x$ deposition temperature $T_{\text{deposition}}$ of 300 °C. While a 350 °C fabrication process was explored for making TFTs [31], a maximum deposition temperature of 300 °C was used in all fabrication processes reported in this paper. The details of our standard TFT fabrication process on CP, including substrate preparation and special loading techniques, are described in [32]. In both back-channel-cut and back-channel-passivated TFT fabrication, the gate electrode and S/D electrodes consist of trilayers of Cr/Al/Cr that are 15-/50-/15-nm thick.

The TFT stack of back-channel-etched TFTs consists of a 300-nm-thick $SiN_x$ layer, a 200-nm-thick a-Si:H active layer, and a 30-nm-thick $n^+$ doped nc-Si:H layer deposited using PE-CVD. For TFTs with a back-channel-passivated TFT geometry, an additional 150-nm-thick $SiN_x$ passivation layer was deposited immediately following the a-Si:H active-layer deposition.

### *C. Self-Aligned TFT Fabrication Process*

We developed three separate self-alignment steps: SA1) self-alignment between the gate electrode and the channel passivation; SA2) self-alignment between the gate electrode and the S/D electrodes; and SA3) self-alignment between the gate electrode and the a-Si:H island. To develop the self-alignment process, we measured the transmission of UV light through the CP substrate and the TFT layers. We selected the 405-nm mercury line in our mask aligner for photolithographic exposure because the transmittance of our CP substrates is ~15% at 405 nm [29]. While the optical absorption of $SiN_x$ at 405 nm is relatively small, a-Si:H strongly absorbs in this region. The measured transmittance of 405-nm UV light through our CP substrate coated with a 20-nm-thick a-Si:H layer is 0.02% and drops to ~0.005% for a 40-nm-thick a-Si:H layer. To keep the exposure time for the self-alignment step reasonably short, we chose an a-Si:H channel layer thickness of 25 nm for all of our self-aligned TFT processes. Fig. 2 shows the schematics of the self-aligned back-channel-passivated TFT at various stages during fabrication. The details of the process are described in the following paragraphs.

We first deposit $SiN_x$ barrier layers on both sides of a CP substrate (step 1). Then, a metal trilayer of 15-/50-/15-nm Cr/Al/Cr is deposited using thermal evaporation (step 2) and patterned with mask 1 to form the gate electrodes (step 3). Next, the TFT stack is deposited (step 4). At this point, the first self-alignment step SA1, described in [23], aligns the $SiN_x$ channel-passivation layer to the gate electrode (steps 5–6). During SA1 self-alignment, the sample is spin coated with a layer of hexamethyldisilazane (HMDS) and AZ5214E photoresist. Then, we load the substrate into the mask aligner facing downwards and expose the photoresist through the back of the substrate using a mask-aligner power density of 3.5 mW/cm$^2$ for approximately 10 min. In this step, the bottom-gate metal layer acts as a mask to block UV light from reaching the photoresist directly above the gate, and this acts to self-align the photoresist that will subsequently be used to pattern the top $SiN_x$ layer (i.e., the channel passivation) to the gate. After photoresist exposure and standard development, the top $SiN_x$ layer is now wet etched in buffered oxide etch (BOE = $HF:NH_4F:H_2O$) for 50 s. By slightly overetching the top $SiN_x$ layer, the required gap between the edge of the gate and the edge of the channel passivation is achieved. Following this step, the sample surface is cleaned using piranha etch (3:1 $H_2SO_4 : H_2O_2$) and a short dip in BOE diluted 1:100 with DI water. This ensures a clean interface between the exposed a-Si:H channel layer and the $n^+$ nc-Si:H layer that is subsequently deposited using PE-CVD (step 7). Fig. 2(a) shows a cross section of the workpiece at this point during fabrication.

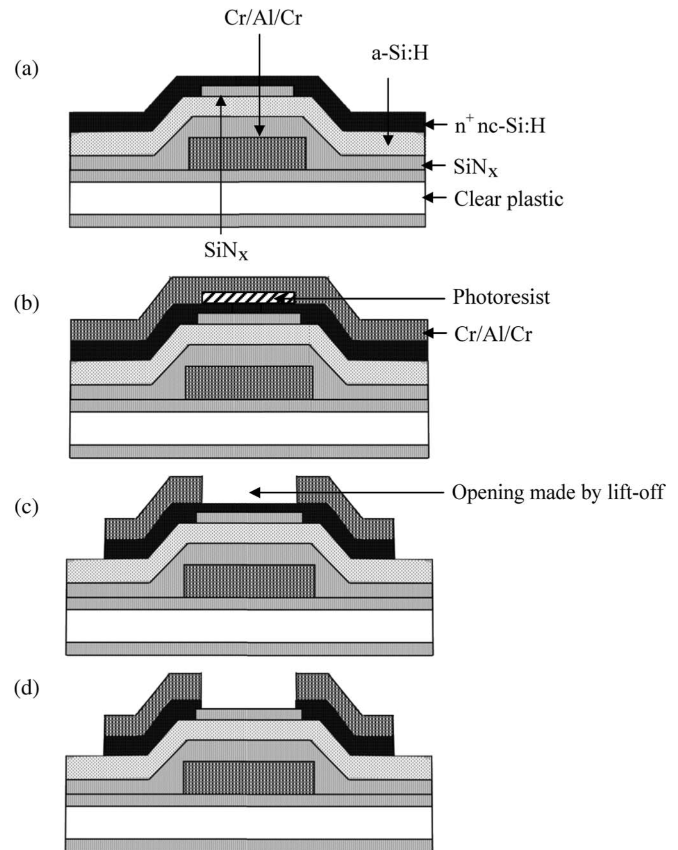


Fig. 2. Schematic of self-aligned back-channel-passivated a-Si:H TFT at various stages during the fabrication process: (a) After SA-1 self-alignment and deposition of the $n^+$ nc-Si layer. (b) After patterning the photoresist stripe above the gate electrode (see text) and deposition of the S/D electrode metal. (c) After lift-off to complete the SA-2 self- alignment. (d) Finished self-aligned TFT.

Next, the sample is unloaded from the PE-CVD system for the second self-alignment step SA2. A stripe of photoresist is patterned above the TFT gate electrode in the channel region using a combination of standard photolithography and self-alignment as described next. Then, a blanket S/D metal layer is deposited, and the photoresist is removed from the channel region by lift-off. This removes the S/D metal in the TFT channel region, effectively self-aligning the edges of the S/D electrodes in the TFT channel to the gate. To achieve an S/D metal overlap with the gate electrode $L_{SD}$, we pattern the photoresist stripe so that the edge of the photoresist stripe lies within the edge of the gate metal, as shown in Fig. 3. Following lift-off to remove the necessary S/D metal in the channel region, standard photolithography is used to pattern the remaining metal to form the S/D electrodes. In this step, we use a mask in which the pattern defining the S/D metal electrodes is connected across the channel (i.e., the S/D contacts are short circuited in the mask layout).

The detailed procedure for patterning the photoresist stripe over the TFT gate is as follows: We mount the substrate on a glass slide with a film of DI water and coat it with HMDS adhesion promoter and AZ5214 photoresist. Then, we prebake the substrate on a hotplate at 110 °C for 90 s. Next, we use mask 2 (containing the pattern of the TFT a-Si:H islands for the standard TFT fabrication process) to expose the photoresist

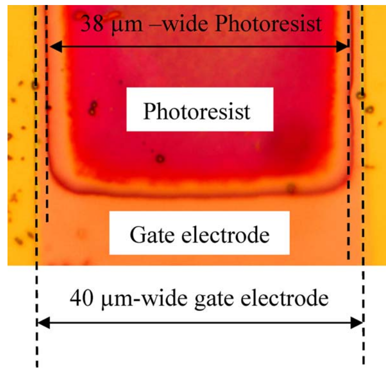


Fig. 3. Close-up of the TFT channel region after step 8 of the self-alignment process (see text) showing the photoresist stripe patterned over the gate. The gate electrode is 38 $\mu$m long, while the photoresist stripe is 40 $\mu$m long. The $L_{SD}$ of 1 $\mu$m ensures sufficient overlap of the S/D layers with the gate electrode.

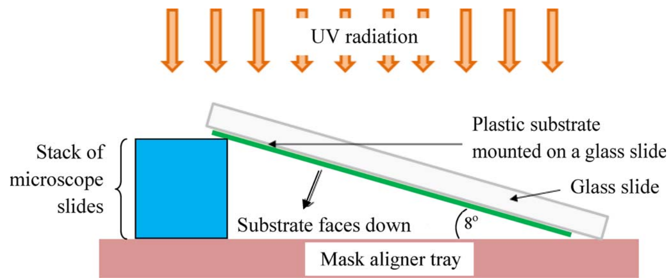


Fig. 4. Schematic for positioning the substrate for step 8 of the self-alignment process (see text).

everywhere except for large squares covering the TFT channel region. After unloading the mask, the substrate (still attached to the glass backing slide) is then loaded facing downwards into the mask aligner at an 8° angle. The angle is set by placing a stack of microscope slides underneath one edge of the glass backing slide as shown in Fig. 4. The loaded substrate is now exposed to 405-nm UV radiation for 12 min using a power density of 3.5 mW/cm$^2$. Then, the substrate is rotated by 90° (still facing downwards) and is again exposed for 12 min. The substrate exposure and rotation are carried out four times in total, giving a total exposure time of 48 min. Had we not loaded the substrate at an angle, the backside exposure would only have resulted in exposure of all photoresist areas not protected by the bottom-gate metal. However, when the substrate is loaded at an angle, we also expose a thin stripe of photoresist lying directly inside the outer edge of the gate metal. This is essential for creating sufficient S/D electrode overlap with the gate electrode. By adjusting the loading angle, we adjust the S/D overlap $L_{SD}$. A larger angle results in a larger $L_{SD}$. For the conditions stated previously, we routinely achieve $L_{SD} \approx 1$ $\mu$m.

After the backside exposure, the substrate is unloaded, removed from the glass backing slide, and developed in AZ300 for 40 to 60 s to define a photoresist stripe over the channel region (step 8). Next, the substrate is dipped in BOE mixed with DI water (1:100) for 2 to 4 s, followed by the deposition of 10-/50-/10-nm Cr/Al/Cr by thermal evaporation (step 9). Fig. 2(b) shows the schematic of the workpiece at this point during fabrication.

We next remove the photoresist from the channel region via lift-off by sonicating the substrate in isopropanol for 20 min (step 10). Any photoresist remnants in the channel are then removed by soaking the substrate in AZ400 developer for about 10 s while rubbing the surface gently with cotton q-tips, followed by oxygen-plasma descumming. Next, standard photolithography with mask 2 and wet etching of the remaining S/D metal are used to define the outline of the S/D terminals (step 11). This completes the second self-alignment step SA2.

For SA3 self-alignment, we make use of the fact that the a-Si:H material in the channel region is covered with photoresist after developing the mask 3 pattern during step 11. Therefore, prior to stripping this photoresist pattern, we use reactive ion etching (RIE) to remove the exposed $n^+$ a-Si:H material (step 12), which effectively self-aligns the a-Si:H active layer to the gate electrode. Fig. 2(c) shows the schematic of the workpiece at this point during fabrication.

We then strip the photoresist and continue with standard photolithography using mask 4 and RIE to open the gate via holes over the gate pads (step 13). This completes the TFT fabrication process with self-alignment. Fig. 2(d) shows the schematic of the finished back-channel-passivated TFTs. We used self-alignment to pattern the channel passivation, the S/D electrodes, and the a-Si:H islands. In each case, the layers being patterned are self-aligned with respect to the gate electrode.

To study the TFT properties in circuits, we fabricated inverters and ring oscillators using both the standard and the self-aligned fabrication processes. In the active load inverter made of two n-channel a-Si:H TFTs, the gate and drain of the top (load or pull up) TFT is connected to the power supply voltage $V_{DD}$, and the bottom TFT is the driver TFT. We fabricated five- and seven-stage ring oscillators with $\beta = 10$, where $\beta$ is defined in terms of the channel width ($W$) and the channel length ($L$) as $\beta = (W_{DRIVER}/L_{DRIVER})/(W_{LOAD}/L_{LOAD})$ [33]. We fabricated the following runs of five and seven-stage ring oscillators: 1) back-channel-cut nonself-aligned TFTs on glass and CP ($L = 20$ $\mu$m, $L_{SD} = 10$ $\mu$m); 2) back-channel-passivated TFTs, self-aligning the channel passivation to the gate, on CP ($L = 20$ $\mu$m, $L_{SD} = 10$ $\mu$m); 3) back-channel-cut nonself-aligned TFTs on glass and CP ($L = 10$ $\mu$m, $L_{SD} = 15$ $\mu$m); and 4) back-channel-passivated TFTs with the S/D terminals, the channel passivation, and the a-Si:H layer self-aligned to the gate on CP ($L = 38$ $\mu$m, $L_{SD} = 1$ $\mu$m).

In ring oscillators, the common node of the TFTs of one inverter (i.e., the connected S/D electrodes) is connected to the gate of the driver TFT of the following inverter. Connecting the gate electrode of one TFT to the S/D electrodes of another TFT requires interconnections between the bottom (gate) and top (S/D) metal layers. To achieve this, we modified our TFT fabrication process steps by etching via holes through the $SiN_x$ gate dielectric (to expose the gate metal) prior to depositing the second metal layer during SA2 self-alignment (step 9). The interconnects are included in mask 2 and are patterned during step 11. To ensure sufficient via coverage and therefore, an electrical connection between the top and bottom metal layers, we increased the thickness of the Al layer in the usual Cr/Al/Cr trilayer used for S/D electrode fabrication from 50 nm to 250 nm.

## III. Evaluation Techniques and Instrumentation

We evaluated our fabrication processes by measuring the degree of misalignment between device layers and TFT yield over the working area. Misalignment between two different TFT layers is defined as $\Delta \equiv 10^6 \times d/\lambda$ (ppm). Here, $d$ is the local misalignment between the two layers measured at a specific reference point, and $\lambda$ is the distance from the center of the substrate to the reference point. The TFT yield $Y_{\mathrm{TFT}}$ is defined as the ratio of functional TFTs $T_{\mathrm{WORK}}$ to the total number of TFTs fabricated across the working area $T_{\mathrm{TOTAL}}$. It is defined as follows: $Y_{\mathrm{TFT}} = T_{\mathrm{WORK}}/T_{\mathrm{TOTAL}} \times 100(\%)$.

We evaluated the electrical performance of our TFTs by measuring their transfer characteristics ($I_{\mathrm{DS}}$ versus $V_{\mathrm{DS}}$) with an HP4155A parameter analyzer and extracting the TFT parameters. Transfer characteristics were measured by sweeping $V_{\mathrm{GS}}$ after setting $V_{\mathrm{DS}}$ first at 0.1 V and then at 10 V. The measured current between the drain and source electrodes ($I_{\mathrm{DS}}$) and the current between the gate and source electrode ($I_{\mathrm{GS}}$) for both sweeps are plotted on a semilog plot (using the same set of axes). We extracted the following TFT performance parameters from the transfer characteristic by using standard equations to model the TFT current [34]: the threshold voltage ($V_{\mathrm{TH}}$), $\mu_{\mathrm{eff},e}$ in the linear regime of operation ($\mu_{\mathrm{LIN}}$), $\mu_{\mathrm{eff},e}$ in the saturation regime of operation ($\mu_{\mathrm{SAT}}$), the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ current ratio, and the subthreshold slope ($S$).

Finally, we measured the performance of our ring oscillators using the HP4155A parameter analyzer to supply power to the oscillator. The output of the ring oscillator (after a buffer inverter stage) was connected to a Tektronix TDS303 oscilloscope.

## IV. Results and Discussion

### A. TFT Electrical Performance

Previously, we showed that there is no significant difference between the measured transfer curves for a-Si:H TFTs fabricated on glass and plastic or for TFTs fabricated using back-channel cut and back-channel etched geometries [35], [36]. Furthermore, we also showed that the electrical stability of TFTs fabricated on plastic at 300 °C is equivalent to that of devices fabricated on glass. Therefore, our 300 °C fabrication process enables us to fabricate a-Si:H TFTs on plastic substrates that have an equivalent electrical performance to devices fabricated on glass. The transfer characteristic of a self-aligned back-channel-cut TFT with a $W/L$ of 80 $\mu$m/40 $\mu$m fabricated on CP at 300 °C, using self-alignment between the channel passivation, the S/D terminals, the a-Si:H island, and the gate, is shown in Fig. 5. TFTs with smaller channel lengths that were fabricated using this self-alignment method had a high $I_{\mathrm{DS}}$ current in the OFF state. This can be seen in the transfer characteristic for a back-channel-passivated TFT with a $W/L$ ratio of 360 $\mu$m/5 $\mu$m that is plotted and shown in Fig. 6. TFTs with a $W/L$ ratio of 360 $\mu$m/3 $\mu$m fabricated on CP hardly even turned off. The performance parameters extracted from transfer characteristics of back-channel-cut and back-channel-passivated standard TFTs and the transfer characteristics of self-aligned TFTs plotted in Figs. 5 and 6 are listed in Table I.

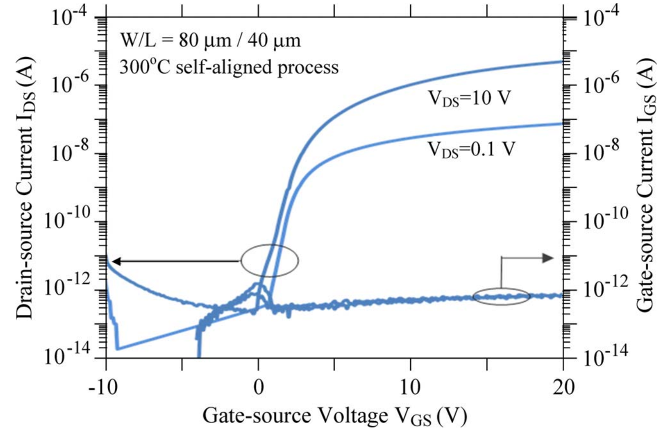


Fig. 5. Transfer characteristics of an a-Si:H TFT fabricated at 300 °C on CP using a back-channel-cut geometry and self-alignment.

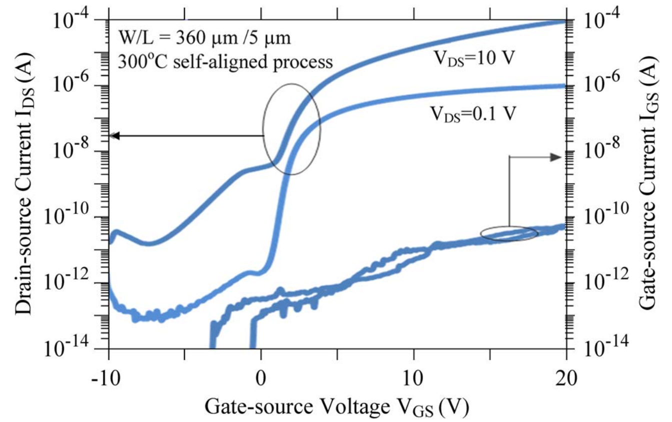


Fig. 6. Transfer characteristic of a self-aligned a-Si:H TFT fabricated on CP. See text for detail.

TABLE I
Performance Parameters of a-Si:H TFT Fabricated on CP at 300 °C

| TFT configuration | Back-channel cut | Back-channel passivated | Back-channel cut | Back-channel passivated |
|---|---|---|---|---|
| Alignment | standard | standard | self-aligned | self-aligned |
| W (µm) / L (µm) | 80/40 | 80/40 | 80/40 | 360/5 |
| Linear mobility $\mu_{\mathrm{LIN}}$ (cm$^2$/Vs) | 1.08 | 1.09 | 1.1 | 0.36 |
| Saturation mobility $\mu_{\mathrm{SAT}}$ (cm$^2$/Vs) | 0.86 | 0.91 | 0.92 | 0.40 |
| Threshold voltage $V_{\mathrm{TH}}$ (V) | 1.21 | 2.25 | ~ 2 | ~ 2 |
| Subthreshold slope S (mV/decade) | 670 | 510 | 500 | 380* |
| $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ | > $10^7$ | > $10^7$ | > $10^7$ | 0.36 |

To explain the high OFF currents of self-aligned TFTs with small channel lengths, one can consider similar high OFF currents which have been reported in papers for short-channel a-Si:H TFTs fabricated with thin a-Si:H layers [37]–[42]. These

high OFF currents are believed to be the result of Fermi-level pinning at the front channel of the 25-nm-thick a-Si:H layer. The high OFF currents we experience for self-aligned a-Si:H TFTs are likely a combination of Fermi-level pinning due to the thin 25-nm-thick a-Si:H channel layer and short-channel effects resulting in drain-voltage induced barrier lowering at the drain electrode. Fermi-level pinning at the back channel (the interface between the top $SiN_x$ channel-passivation layer and the a-Si:H layer) depends on the back-channel defect density. Higher defect densities result in a Fermi level pinned closer to the conduction band and higher OFF currents [43], [44]. The theoretical model derived in [44] suggests that the OFF current for TFTs with a Fermi level pinned 0.6 eV below the conduction-band edge causes high OFF current similar to the effect we see in our short-channel TFTs. For TFTs with channel lengths of less than 6 $\mu$m, the drain electric field penetrates sufficiently deep into the a-Si:H channel region to lower the potential barrier at the source electrode, which results in higher OFF currents that increase with increasing $V_{DS}$ [45]. To resolve this issue, we need to reduce defects in the back channel of our self-aligned short-channel TFTs during fabrication, possibly by introducing a fine structure to the channel as proposed in [38].

## B. Misalignment

The minimum misalignment that we achieved using conventional photolithography to pattern device layers was obtained by reducing the total stress in the workpiece. This method enabled us to reduce the misalignment between the gate and the S/D layers to $d = 15$ $\mu$m for $\lambda = 5$ cm ($\Delta = 300$ ppm) [36]. On the 7.0 cm $\times$ 7.0 cm size mask area, the TFT yield $Y_{TFT} = 47.6\%$ for TFTs designed with $L = 40$ $\mu$m and $L_{SD} = 5$ $\mu$m, and $Y_{TFT} = 95.2\%$ for TFTs designed with $L = 40$ $\mu$m and $L_{SD} = 10$ $\mu$m. In order to achieve functional TFTs over the entire substrate surface area using standard photolithography and 300 °C deposition temperature, we were forced to design TFTs with minimum channel lengths of $L = 40$ $\mu$m and $L_{SD} \approx 15$ $\mu$m.

In contrast—when implementing self-alignment between the S/D electrodes, the channel passivation, the a-Si:H active layer, and the gate electrode—we were able to reduce the minimum TFT channel length $L$ from 40 to 3 $\mu$m and reduce $L_{SD}$ to 1 $\mu$m while still achieving functional TFTs over the entire surface area ($Y_{TFT} = 100\%$). Fig. 7 shows close-up optical micrographs of TFT channel regions where the TFT channel lengths are 5 $\mu$m [Fig. 7(a)] and 3 $\mu$m [Fig. 7(b)]. These back-channel-passivated TFTs were fabricated on CP using a $SiN_x$ deposition temperature of 300 °C and the SA1, SA2, and SA3 self-alignment processes that we developed. All self-aligned TFTs had an a-Si:H layer thickness of 25 nm. Fig. 8 shows a small section of the finished workpiece, at a distance of ~5 cm away from the center. The TFT on the right-hand side of the figure is patterned using self-alignment between the gate, the channel passivation, the S/D terminals, and the a-Si:H island layers. It is a back-channel-passivated a-Si:H TFT with $L = 5$ $\mu$m and $L_{SD} = 1$ $\mu$m. In contrast, the alignment mark on the left-hand side of Fig. 10 is patterned without self-alignment. The photoresist stripes patterned during SA2 self-alignment are only formed over the TFT channel regions; the

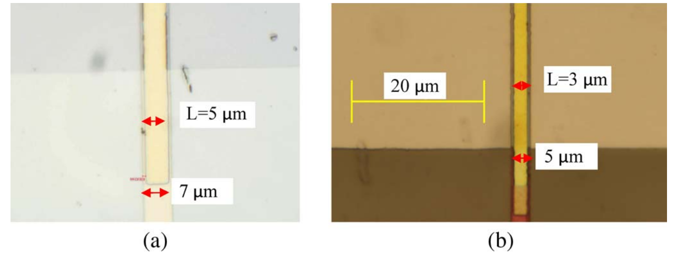


Fig. 7. Optical micrograph of the channel region of back-channel-passivated TFTs on CP fabricated using self-alignment with channel lengths of (a) $L = 5$ $\mu$m and (b) $L = 3$ $\mu$m. The maximum process temperature was 300 °C, and $L_{SD} = 1$ $\mu$m.

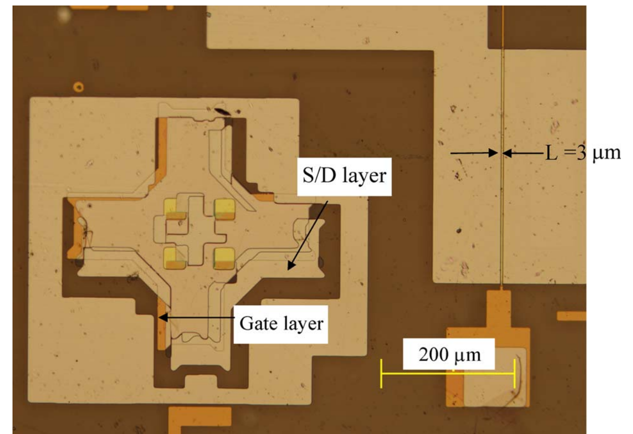


Fig. 8. Right-hand side of the optical micrograph shows a back-channel-passivated TFT fabricated at 300 °C on CP and has a $W/L$ ratio of 360 $\mu$m/3 $\mu$m. Self-alignment was used to align the S/D electrodes, the channel passivation, and the a-Si:H island to the gate electrode (see text). This TFT lies in the corner of the mask set, ~5 cm from the center of the substrate. The left-hand side of the optical micrograph shows an alignment mark patterned without self-alignment between the bottom-gate electrode layer and the top S/D electrode layer.

alignment mark formed in the S/D mask layer is patterned using mask 3 and standard photolithography during step 11. The gate layer of the alignment mark (patterned with mask 1) and the S/D layer (patterned with mask 3) of the alignment mark are displaced by $\approx 15$ $\mu$m. This gives an alignment error of $\Delta \equiv 10^6 \times 15/50000 = 300$ ppm. We would never have been able to fabricate a-Si:H TFTs with channel lengths as short as 3 $\mu$m free-standing as a plastic substrate at 300 °C had we only relied on standard photolithography.

## C. Ring Oscillators

We evaluated the performance of ring oscillators from four fabrication runs (refer to the Device Fabrication Section for details). The measured gate delay and power dissipation per inverter stage are plotted and shown in Fig. 9 for oscillators from runs #1, #2, and #3. The measured gate delay and power consumption per inverter stage for oscillators from run #4 is plotted and shown in Fig. 10. The results in Fig. 9 show that the ring-oscillator performance is not affected when using either TFTs in which all layers are patterned by standard photolithography (run #1) or TFTs in which the channel passivation is aligned to the gate by self-alignment (run #2). It has been shown that the propagation delay time through an oscillator inverter stage decreases (i.e., the oscillation frequency increases) when

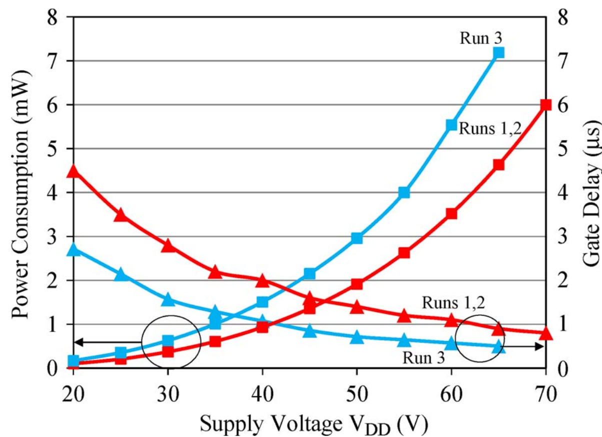


Fig. 9. Power consumption and gate delay per stage for ring-oscillator runs #1–#3 fabricated on CP.

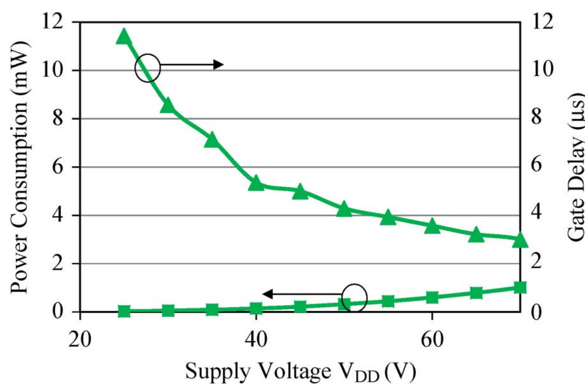


Fig. 10. Power consumption and gate delay per stage for ring-oscillator run #4 fabricated on CP.

the channel length of the driver TFT $W_{\mathrm{DRIVER}}$ decreases [33]. The channel length of TFTs in run #3 is half that of TFTs in runs #1 and #2, and the oscillation frequency increases by 50% (delay per stage decreases by 50%) as expected. The ring oscillators for run #4 were made using self-alignment between the TFT channel passivation, the S/D electrodes, the a-Si:H channel, and the gate electrode. The channel length of TFTs from run #4 is ∼2 times that of TFTs from runs #1 and #2, and the oscillation frequency is correspondingly 50% slower than the oscillation measured for circuits from runs #1 and #2. These results show that functional circuits can be fabricated over the whole surface area of free-standing CP foils when multiple self-alignment steps are employed between the TFT device layers.

## V. Conclusion

Our most important result is the feasibility of fabricating flexible a-Si:H TFTs and circuits over the whole working area of free-standing CP foil substrates while achieving a TFT performance comparable with that obtained on display glass. To overcome the substrate distortion induced by thermal stress, we have introduced self-alignment between the S/D electrodes, the channel passivation, the a-Si:H island, and the gate electrode of our TFTs. Back-channel-passivated TFTs on CP were fabricated at a maximum deposition temperature of 300 °C, with channel lengths as small as 3 $\mu$m and 1-$\mu$m S/D overlaps with the gate. All self-aligned TFTs over the entire 7.0 cm × 7.0 cm mask area were functional. The a-Si:H TFTs were tested in circuits by building ring oscillators. We believe that our technique and results amount to a significant step toward the fabrication of a-Si:H TFT circuits with a glasslike stability on free-standing CP substrates.

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