Self-Aligned Top-Gate Coplanar a-Si:H Thin-Film Transistors With a SiO_2–Silicone Hybrid Gate Dielectric

Lin Han, Yifei Huang, James C. Sturm, *Fellow, IEEE*, and Sigurd Wagner, *Fellow, IEEE*

***Abstract*—We have made self-aligned top-gate coplanar hydrogenated amorphous-silicon (a-Si:H) thin-film transistors using a SiO_2–silicone hybrid material as the gate dielectric. The hybrid dielectric layer is 150 nm thick and separates a chromium gate electrode from nickel silicide source and drain. The nickel silicide is formed by rapid thermal reaction of a deposited nickel film with the underlying a-Si:H. The electron field-effect mobility is $\sim$1.0 $cm^2/V \cdot s$, the subthreshold slope is $\sim$380 mV/decade, and the ON/OFF current ratio is $\sim 10^5$. The gate leakage current of $\sim$10 pA across the 150-nm-thick hybrid dielectric is $\sim$1/10 of that observed across the typical 300-nm-thick SiN_x dielectric. The whole process needs only two masks.**

***Index Terms*—Amorphous silicon (a-Si:H), coplanar top-gate thin-film transistor (TFT), plasma-enhanced chemical vapor deposition (PE-CVD), SiO_2–silicone hybrid.**

I. Introduction

THIN-FILM transistors (TFTs) made with hydrogenated amorphous silicon (a-Si:H) are used on a very large scale for active-matrix backplanes. Therefore it is of great practical interest to improve their performance and simplify their manufacture. One path to improvement and process step reduction is to make a-Si:H TFTs with the gate self-aligned to source and drain. This reduces parasitic capacitance and thereby the gate delay of TFT and the parasitic voltage shift across the load (liquid crystal or TFT gate) that the TFT switches. Polycrystalline Si TFTs are self-aligned by using the top gate as the mask for doping by ion implantation or ion shower [1], [2], which can be combined with silicidation for preparing metallic contacts [2]. This process has the additional advantage of a low mask count. Self-alignment by postdeposition doping is not possible with a-Si:H. The classical approach to self-aligning standard bottom-gate a-Si:H TFTs has been to employ the gate electrode as the mask for exposure of photoresist through the substrate [3]–[5]. This can be done with only two masks [3] but requires optically transparent structures and long exposure times. While top-gate staggered a-Si:H TFTs have been fabricated to reduce the mask count, they have not been self-aligned [6], [7]. Top-gate a-Si:H TFTs can be self-aligned by a nickel silicide process that forms low-resistance source/drain (S/D) [8]. In this process, nickel diffuses into silicon at 250 °C [9] to form a layer with a low sheet resistance; because this layer is inert against nickel etchant, it remains when the unreacted nickel is etched away from the sidewall of the gate dielectric [8]. Here, we introduce our new insulator, which is a SiO_2–silicone hybrid material [10], [11], as the dielectric for top-gate self-aligned a-Si:H TFTs, in which the hybrid replaces the standard SiN_x gate insulator. Its deposition conditions are described in [10] and a large number of properties in [11]. The source and drains are formed as described in [8], by reacting nickel with the a-Si:H channel material to form a layer that functions as both S/D and metallic S/D contact. Our motivation was the observation of very low leakage currents measured in capacitors with the new dielectric [11]. This suggested that sidewall leakage might be low even across a thin gate dielectric layer. Our results show that this is indeed the case.

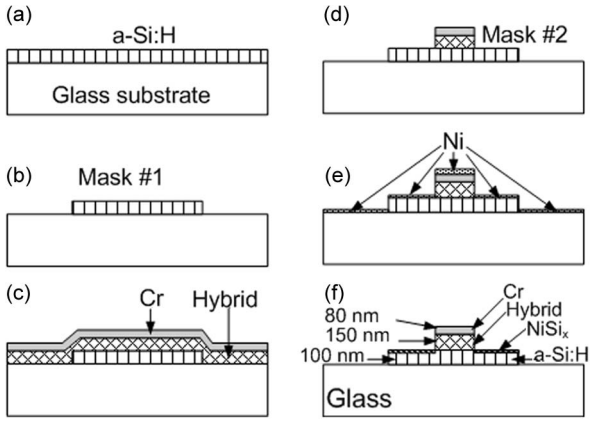

Fig. 1. Schematic of top-gate TFT fabrication process. (a) Deposition of a-Si:H channel layer. (b) a-Si:H island definition. (c) Deposition of hybrid gate dielectric and gate metal Cr. (d) Patterning of gate. (e) Sputtering of Ni. (f) Annealing to form S/D silicide.

II. Transistor Fabrication and Evaluation

The top-gate self-aligned a-Si:H TFT is fabricated in a two-mask process on Corning 1737 glass substrates, as shown in Fig. 1. We deposit the a-Si:H and the hybrid insulator in two different reactors. The 100-nm-thick channel layer is deposited in a four-chamber reactor by plasma-enhanced chemical vapor deposition (PE-CVD) from SiH_4 and H_2, directly on the

Manuscript received August 9, 2010; revised September 25, 2010; accepted September 28, 2010. Date of publication November 11, 2010; date of current version December 27, 2010. This work was supported by Universal Display Corporation. The work of L. Han was supported by the U.S. Department of Energy under Contract DE-AC02-76-CHO-3073 through a Princeton Program in Plasma Science and Technology Fellowship. The review of this letter was arranged by Editor A. Nathan.

The authors are with the Department of Electrical Engineering and the Princeton Institute for the Science and Technology of Materials, Princeton University, Princeton, NJ 08544 USA (e-mail: linhan@princeton.edu).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2010.2084558

glass substrate, at 250 °C substrate temperature, a pressure of 900 mtorr, and a plasma power density of 17 mW/cm^2. Before insulator deposition, we pattern the a-Si:H to islands by reactive-ion etching (RIE) with SF_6 and CCl_2F_2 and then dip the sample for 30 s into 100 H_2O:1 buffered HF/NH_4F (BOE). The 150-nm-thick gate insulator is deposited in the hybrid PE-CVD reactor at nominal room temperature under the conditions described in [10]. An 80-nm-thick Cr layer is thermally evaporated and patterned using Cr-7 etchant (perchloric acid and ceric ammonium nitrate). The patterned gate electrode serves as the mask for RIE of the underlying hybrid insulator with CF_4 and O_2, to expose the a-Si:H channel layer. The sample is dipped again for 30 s into 100:1 diluted BOE, before sputter depositing a 30-nm-thick Ni layer. Finally, the sample is rapid thermally annealed for 2 min at 250 °C, and the unreacted Ni is etched away with $HNO_3 : HCl : H_2O = 1 : 5 : 3$. To ensure that the Ni is removed completely, the sample is overetched for 40 s.

The TFTs are evaluated for I_{DS}–V_{DS} output characteristics, I_{DS}–V_{GS} transfer characteristics, and high-field gate-bias-stress stability with an HP4155A parameter analyzer. For output characteristics, the S/D voltage V_{DS} is swept from 0 to +15 V, and the gate voltage V_{GS} is swept from +4 to +22 V in steps of 2 V. For transfer characteristics, V_{GS} is swept from +20 to −10 V or −10 to +20 V at $V_{DS} = 0.1$ and 10 V. The sum of the S/D contact resistances is derived from the output characteristics in the linear regime of TFTs with channel lengths L ranging from 40 to 160 μm, following the approach introduced in [12]. For each data point of gate-bias stressing [13], the source and drain of a fresh unstressed transistor are grounded, and a positive V_{GS} is applied for 600 s. Following that, the transfer characteristics are measured by sweeping the V_{GS} from +20 to −10 V at a fixed V_{DS} of 10 V. The threshold voltage shift ΔV_T is evaluated for gate-bias voltages between 5 and 22.5 V, which produce electric fields in the hybrid dielectric that range from 0.33 to 1.5 MV/cm. ΔV_T (not V_T itself) is determined on the subthreshold slope of the transfer curve at $I_{DS} = 1 \times 10^{-10}$ A.

III. Transistor Characteristics

Fig. 2(a) shows the I_{DS}–V_{DS} characteristics of a TFT with channel width $W = 160$ μm and length $L = 80$ μm. The dc transfer characteristics are shown as $(\log_{10} I_{DS}) - V_{GS}$ in Fig. 2(b). The on/off current ratio is $\sim 10^5$, the subthreshold slope $S = \partial V_{GS}/\partial(\log_{10} I_{DS}) = 380$ mV/decade, and the off and gate leakage currents are ∼10 pA each. We observe a hysteresis between the two directions of V_{GS} sweep of 0.4 V. The least squares fits of I_{DS} and $\sqrt{I_{DS}}$ to V_{GS} swept from −10 to +20 V (Fig. 3) to the linear ($V_{DS} = 0.1$ V) and saturated ($V_{DS} = 10$ V) regimes yield values for the electron field-effect mobility μ of 0.9 and 1.0 cm^2/V · s, and for the threshold voltage V_T of 2.7 and 1.9 V, respectively. The sum of the S/D contact resistances decreases as a function of V_{GS}, and it is less than 0.6 MΩ when V_{GS} is larger than 10 V. Fig. 4 shows the bias-stress data in the form of a log–log plot of ΔV_T versus gate-bias field applied for 600 s. The TFT has the hybrid dielectric deposited near room temperature, while the representative ΔV_T data for standard-process bottom-gate TFTs shown for

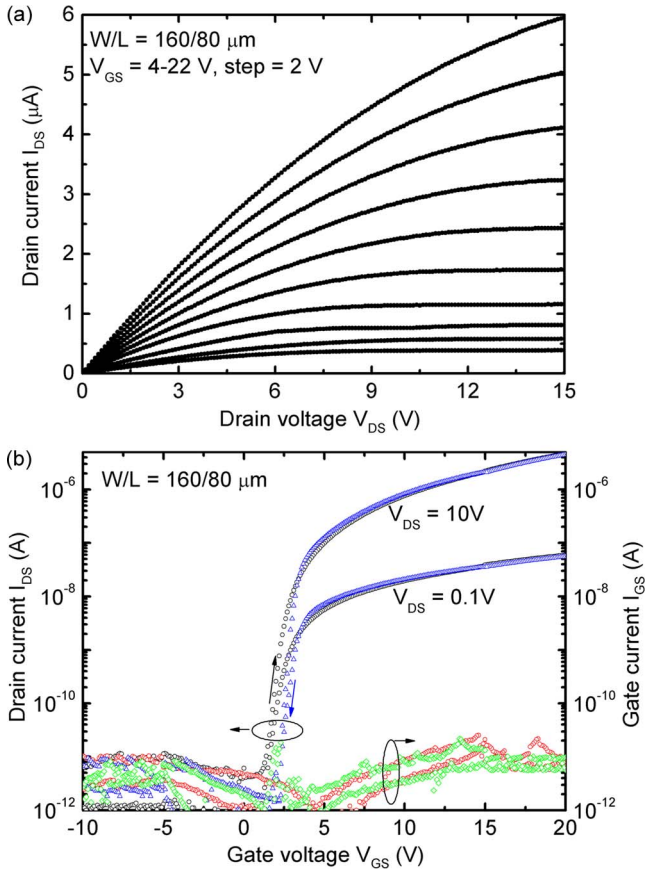

Fig. 2. (a) Output characteristics of the top-gate a-Si:H TFT with hybrid dielectric and nickel silicide S/D. (b) Transfer characteristics and gate leakage current.

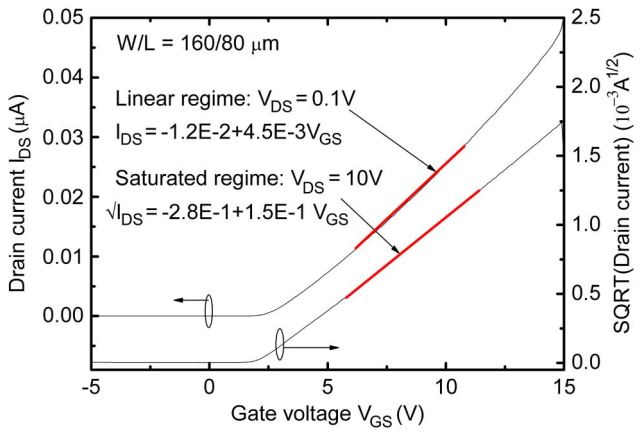

Fig. 3. Least squares fits to the linear regime ($V_{DS} = 0.1$ V) and saturated regime ($V_{DS} = 10$ V) for the determination of mobility μ and threshold voltage V_T.

comparison had their SiN_x gate dielectric deposited without breaking vacuum at 150 °C and 250 °C [14], 300 °C [15], and 350 °C [16]. The field-effect mobility, subthreshold slope, and off current do not change in this experiment. V_T returns to its original value during storage for ten days at room temperature.

IV. Discussion

The TFT with the hybrid dielectric has an electron mobility as high as the highest value reported to date for a top-gate

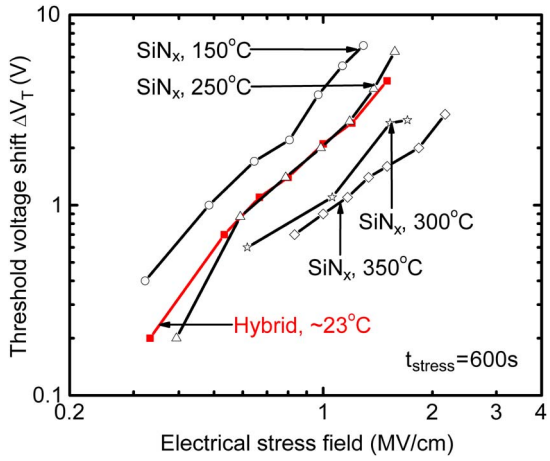

Fig. 4. Threshold-voltage shift ΔV_T versus gate-bias field for top-gate a-Si:H TFTs with the hybrid gate dielectric (each point from a fresh TFT) and for bottom-gate TFTs with the conventional SiN_x gate dielectric fabricated at 150 °C, 250 °C [14], 300 °C [15], and 350 °C [16]. Gate-bias stress was applied for 600 s to all TFTs.

device [9], while its gate leakage current of ∼10 pA is approximately an order of magnitude lower. This difference suggests that the hybrid dielectric with its thickness of only 150 nm is better suited to the top-gate configuration than the SiN_x dielectric, which must be made 300 nm thick. However, the gate leakage current of TFTs in the bottom-gate configuration (with either SiN_x or hybrid dielectric) is lower still, as it lies in the femtoampere range. Increasing the thickness of the hybrid dielectric to reduce leakage would reduce the specific gate capacitance of hybrid TFTs to values less than that of SiN_x TFTs [17]. Answering this question merits further study of edge currents in capacitors made with the hybrid dielectric, preferably in an environment with controlled low humidity. Fig. 4 again points to the high stability of the hybrid dielectric against electron injection, as observed earlier in inverted staggered TFTs with the hybrid dielectric [10]. That ΔV_T is higher than that in the staggered configuration may be the result of exposing the a-Si:H channel layer to the atmosphere prior to deposition of the dielectric, instead of exposing the dielectric prior to a-Si:H deposition. The noticeable hysteresis in the $(\log_{10} I_{\mathrm{DS}}) - V_{\mathrm{GS}}$ characteristics in Fig. 2(b) may have the same origin.

The sheet resistance of the S/D pads is ∼10 Ω/sq. The existence of a highly conducting layer that is not nickel metal is supported by the literature on the diffusion coefficient of Ni in a-Si at 250 °C of $D = 1.0 \times 1.0^{-15}$ cm^2/s [9]. An annealing time of $t = 120$ s results in a diffusion length $\sqrt{\mathrm{Dt}}$ of 3.5 nm. While this value is for diffusion into a-Si, not for a diffusion reaction, it is reasonable to assume that the depth of a reacted layer will have a comparable value and that the reaction product is a nickel silicide with the resistivity of a metal. When the unreacted nickel is not removed by a thorough etch, the gate–source path becomes so conducting that the TFT will "burn" during its electrical evaluation. Therefore we always overetch. The gate leakage current across a 150-nm-thick hybrid is lower than that across a 300-nm-thick SiN_x, which suggests that the edge current is lower across the hybrid than across the SiN_x. We have sought but not been able to devise a chemical analysis of the sidewall of the top-gate dielectric, in either the hybrid or the SiN_x structures in [8].

V. Conclusion

We have demonstrated self-aligned coplanar top-gate a-Si:H TFTs with a new hybrid gate dielectric. The TFTs have high electron mobility and sharp subthreshold slope and are comparatively stable at high gate fields. The simple and low-temperature process, combined with mechanical flexibility [18], makes the self-aligned coplanar top-gate a-Si:H TFT a promising candidate for high-speed and low-power a-Si:H TFT circuitry on flexible substrates.

References

[1] J. R. Pfiester, R. D. Sivan, H. M. Liaw, C. A. Seelbach, and C. D. Gunderson, "A self-aligned elevated source/drain MOSFET," *IEEE Electron Device Lett.*, vol. 11, no. 9, pp. 365–367, Sep. 1990.
[2] J. I. Ryu, H. C. Kim, S. K. Kim, and A. J. Jang, "A novel self-aligned polycrystalline silicon thin-film transistor using silicide layers," *IEEE Electron Device Lett.*, vol. 18, no. 6, pp. 272–274, Jun. 1997.
[3] Y. Kuo, "A new process using two photo-masks to prepare trilayer thin film transistors," *J. Electrochem. Soc.*, vol. 138, no. 2, pp. 637–638, 1991.
[4] D. B. Thomasson and T. N. Jackson, "Fully self-aligned tri-layer a-Si:H thin-film transistors with deposited doped contact layer," *IEEE Electron Device Lett.*, vol. 19, no. 4, pp. 124–126, Apr. 1998.
[5] M. J. Powell, C. Glasse, J. E. Curran, J. R. Hughes, I. D. French, and B. F. Martin, "A fully self-aligned amorphous silicon TFT technology for large area image sensors and active-matrix displays," in *Proc. Mater. Res. Soc. Symp.*, Apr. 1998, vol. 507, pp. 91–96.
[6] M. Le Contellec, F. Maurice, J. Richard, B. Vinouze, and F. Richou, "Very simple a-Si:H TFT fabrication process for LCD-TV application," *J. Non-Cryst. Solids*, vol. 97/98, pp. 297–300, Dec. 1987.
[7] Y. Miyata, T. Kawamura, H. Tsutsu, and T. Chikamura, "Two mask step-inverted staggered a-Si TFT addressed LCDs," *SID Proc.*, vol. 31, no. 1, pp. 3–6, 1990.
[8] Y. Huang, B. Hekmatshoar, S. Wagner, and J. C. Sturm, "Top-gate amorphous silicon TFT with self-aligned silicide source/drain and high mobility," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 737–739, Jul. 2008.
[9] A. Y. Kuznetsov and B. G. Svensson, "Nickel atomic diffusion in amorphous silicon," *Appl. Phys. Lett.*, vol. 66, no. 17, pp. 2229–2231, Apr. 1995.
[10] L. Han, P. Mandlik, and S. Wagner, "A new gate dielectric for highly stable amorphous-silicon thin-film transistors with ∼1.5 $\mathrm{cm}^2/\mathrm{Vs}$ electron field-effect mobility," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 502–504, May 2009.
[11] L. Han, P. Mandlik, J. Gartside, S. Wagner, J. Silvernail, R. Ma, M. Hack, and J. J. Brown, "Properties of a new permeation barrier material deposited from hexamethyl disiloxane and oxygen," *J. Electrochem. Soc.*, vol. 156, no. 2, pp. H106–H114, Jan. 2009.
[12] S. Luan and G. W. Neudeck, "An experimental study of the source/drain parasitic resistance effects in amorphous silicon thin film transistors," *J. Appl. Phys.*, vol. 72, no. 2, pp. 766–772, Jul. 1992.
[13] M. J. Powell, C. Van Berkel, and J. R. Hughes, "Time and temperature dependence of instability mechanisms in amorphous silicon thin-film transistors," *Appl. Phys. Lett.*, vol. 54, no. 14, pp. 1323–1325, Apr. 1989.
[14] K. Long, A. Z. Kattamis, I.-C. Cheng, H. Gleskova, S. Wagner, and J. C. Sturm, "Stability of amorphous-silicon TFTs deposited on clear plastic substrates at 250 °C to 280 °C," *IEEE Electron Device Lett.*, vol. 27, no. 2, pp. 111–113, Feb. 2006.
[15] K. H. Cherenack, A. Z. Kattamis, B. Hekmatshoar, J. C. Sturm, and S. Wagner, "Amorphous-silicon thin-film transistors fabricated at 300 °C on a free-standing foil substrate of clear plastic," *IEEE Electron Device Lett.*, vol. 28, no. 11, pp. 1004–1006, Nov. 2007.
[16] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," *Appl. Phys. Lett.*, vol. 62, no. 11, pp. 1286–1288, Mar. 1993.
[17] L. Han, P. Mandlik, K. H. Cherenack, and S. Wagner, "Amorphous silicon thin-film transistors with field-effect mobilities of 2 $\mathrm{cm}^2/\mathrm{Vs}$ for electrons and 0.1 $\mathrm{cm}^2/\mathrm{Vs}$ for holes," *Appl. Phys. Lett.*, vol. 94, no. 16, pp. 162 105-1–162 105-3, Apr. 2009.
[18] L. Han, K. Song, P. Mandlik, and S. Wagner, "Ultraflexible amorphous silicon transistors made with a resilient insulator," *Appl. Phys. Lett.*, vol. 96, no. 4, pp. 042 111-1–042 111-3, Jan. 2010.