Top-Gate Amorphous Silicon TFT With Self-Aligned Silicide Source/Drain and High Mobility

Yifei Huang, Bahman Hekmatshoar, Sigurd Wagner, and James C. Sturm

***Abstract*—We report a process for top-gate amorphous silicon thin-film transistors (α-Si TFTs) that employs a self-aligned metal silicide for source and drain (S/D). All process steps, including deposition of active layers and formation of metal silicide, are accomplished at temperatures that are less than or equal to 280 °C. The thermal budget is compatible with flexible polymer substrates. The fabricated devices exhibit threshold voltages of ~2.7 V, saturation electron field-effect mobility of 1.0 $cm^2/V \cdot s$, subthreshold slope of 600 mV/dec, and on/off ratio of $\sim 2 \times 10^6$. These top-gate α-Si TFTs with self-aligned silicide S/D have dc performance that is comparable to that of conventional bottom-gate α-Si TFTs. Our results suggest that the top-gate α-Si TFT geometry merits reevaluation for industrial use.**

***Index Terms*—Amorphous silicon (α-Si), self-aligned silicide, thin-film transistor (TFT), top gate.**

I. Introduction

STANDARD bottom-gate amorphous silicon thin-film transistors (α-Si TFTs), as widely used in display backplanes, have a large overlap between the gate and the source and drain (S/D) terminals, leading to high parasitic capacitances. A self-aligned S/D reduces the capacitive coupling and the parasitic series resistance, which are crucial for circuits that require high speed and/or low power consumption [1]. The standard technique for self-alignment of S/D in bottom-gate α-Si TFTs is the exposure of the photoresist from the back through the substrate and channel layer, using the bottom metal gate as the photomask [2], [3]. This technique is limited to transparent substrates, which precludes metals and many plastics, and it requires thin α-Si channel layers for sufficient transparency to the exposing light. Moreover, unconventional equipment is required for projecting UV light through the backside of the wafer. Polycrystalline silicon TFTs typically have self-aligned S/D made by ion implantation or ion shower of an S/D dopant using the gate as mask [4], [5]. The temperature required for the subsequent annealing makes this process unrealistic for TFTs on plastic substrates, except when laser annealing is used, which brings its own challenges of nonuniformity and high production cost [6], [7].

We present top-gate α-Si TFTs with silicide S/D that are self-aligned to the edges of the gate. The S/D are formed directly on the intrinsic α-Si at low temperatures, and the TFT structure contains no n^+ doped regions at all. In the operation of this device, electrons are directly injected from the silicide source into the channel. The self-alignment eliminates the parasitic gate to S/D overlap capacitance at a temperature viable for flexible substrates. The process does not require lithography through the back of the substrate.

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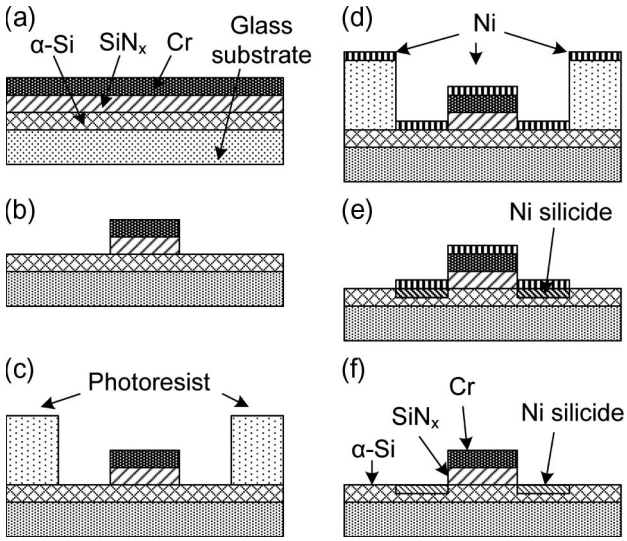

Fig. 1. Illustration of fabrication process: (a) Deposition of TFT stack (α-Si, gate dielectric, and gate metal); (b) definition of gate electrode; (c) definition of the channel width and electrical isolation of devices; (d) blanket deposition of Ni; (e) liftoff and silicidation; and (f) selective removal of unreacted Ni.

II. Fabrication Process

The fabrication process is shown in Fig. 1. The process starts with the deposition of the TFT stack on 1.1-mm-thick Corning 1737 glass slides using plasma-enhanced chemical vapor deposition (PECVD) with an excitation RF frequency of 13.56 MHz. The PECVD pressures and temperatures are 500 mT and 280 °C unless otherwise noted. First, a 250-nm layer of α-Si is deposited from a SiH_4 plasma with power density of 18 mW/cm^2. This is followed, without breaking vacuum, by the deposition of a 300-nm SiN_x gate dielectric layer using a plasma with a gas flow ratio of $SiH_4 : NH_3 = 14$ sccm : 130 sccm and power density of 22 mW/cm^2. An 80-nm layer of Cr is then thermally evaporated over the nitride as the gate metal. The gate is patterned by photolithography and wet etching. Gate lengths range from 5 to 80 μm and width from 10 to 160 μm. The self-alignment begins with the reactive-ion etching of the gate insulator SiN_x in a fluorinated plasma, where the gate metal is used as the etch mask. The etch recipe $(CF_4 : H_2)$ is optimized for a high etch rate and a vertical

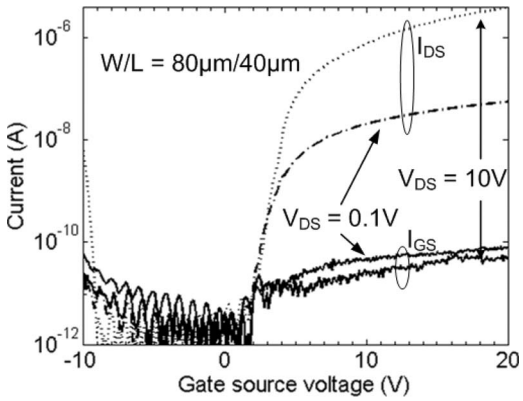

Fig. 2. Room temperature transfer characteristics (drain–current versus gate–source voltage for S/D biases of 0.5 and 10 V) for a top-gate α-Si TFT with self-aligned nickel silicide S/D. $W/L = 80\ \mu$m/40 μm.

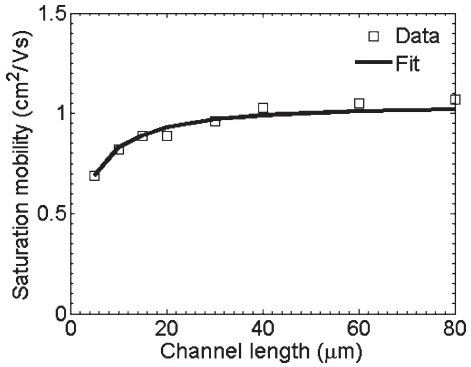

Fig. 3. Channel length dependence of saturation field-effect mobility. The fitting model uses parameters of long-channel mobility of 1.0 cm^2/V $\cdot$ s and S/D series resistance per contact of 130 kΩ at $W = 80\ \mu$m.

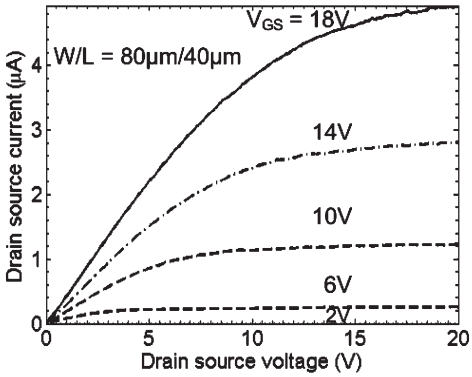

Fig. 4. Room temperature output characteristics (drain–current versus S/D voltage for gate–source bias from 2 to 18 V) of a top-gate α-Si TFT with self-aligned silicide S/D. $W/L = 80\ \mu$m/40 μm.

sidewall. This anisotropy is extremely important for reasons to be discussed below. To form the self-aligned silicide S/D, photoresist is first patterned with openings that expose the regions that will become S/D, as well as the intervening gate electrode (for example, one rectangle for each device). This step defines the width of the device and also electrically isolates one device from another. A blanket 30-nm nickel layer is deposited and then removed outside the device region by liftoff. The devices are then annealed at 280 °C in N_2 ambient for 1 h to convert the nickel to nickel silicide by reaction with the underlying α-Si. The unreacted nickel is removed in a selective wet etch consisting of $HNO_3 : HCl : H_2O$ (1 : 5 : 3). Nickel was chosen because of its low temperature requirement for silicidation reaction is compatible with several plastic substrates [8]–[10].

The final structure then has nickel silicide on top of the α-Si, which is directly adjacent to the gated channel region, and there is no overlap between the gate electrode and the silicide S/D electrode. Since no silicide formed on the sidewall or on top of the metal gate, unreacted nickel can be selectively removed to ensure that there are no conducting paths between the gate contact and the S/D. It is very important that there is a vertical sidewall in the dielectric layer below the metal gate, because any undercut will result in a nonconducting region between the S/D and the gated channel.

III. Results and Discussion

The sheet resistance of the nickel silicide was measured by using the Van der Pauw structures integrated into the photomasks and fabricated along with the devices. The value is approximately 10 Ω/sq. for samples annealed for 1 h at 280 °C. The observed value is in reasonable agreement with those reported in literature [11]. The phase of the silicide is unclear at the present, but it is likely a mixture of amorphous Ni_2Si and amorphous NiSi, based on prior work on crystalline and polycrystalline silicon of similar anneal conditions [12].

The dc transfer characteristics of a typical α-Si top-gate TFT with nickel silicide S/D ($W/L = 80\ \mu$m/40 μm) fabricated on glass at 280 °C are shown in Fig. 2. The performance metrics are extracted from the saturation curve ($V_D = 10$ V) using conventional MOS theory. The long-channel devices ($L > 40\ \mu$m) exhibit a threshold voltage of 2.7 V, saturation field-effect mobility of 1.0 cm^2/V $\cdot$ s (averaged over gate–source voltages of 3–12 V), subthreshold slope of 600 mV/dec, and an on/off ratio of $\sim 2 \times 10^6$. The performance parameters of these TFTs are comparable with those of state-of-the-art conventional bottom gate TFTs. The dependence of the saturation field-effect mobility on channel length (in the range of 5–80 μm) is consistent with previous studies (Fig. 3) [13]. As the channel resistance drops with decreasing channel length, the contact resistance at the S/D-to-channel junction becomes increasingly significant, resulting in a decrease in apparent mobility at shorter channel lengths. For devices with a 5-μm channel, the apparent (uncorrected for contact resistance) saturation field-effect mobility is still 0.7 cm^2/V $\cdot$ s, which suggests that the contact resistance between the S/D and channel is low. Simple modeling with two fitting parameters (long-channel mobility and S/D resistance) of the data in Fig. 3 shows a low effective S/D series resistance of 130 kΩ (for $W = 80\ \mu$m). This low series resistance is also supported by the TFT output characteristics shown in Fig. 4, which shows a linear relationship between S/D current and S/D voltage at low S/D biases. A poor contact to S/D typically leads to rectifying behavior and concave output curves at low S/D biases.

Previously published top-gate a-Si TFTs have mobilities in the range of 0.3–0.9 cm^2/V $\cdot$ s and subthreshold slopes from 0.75 to 1.7 V/dec [14]–[17]. The exception is an experiment

using a process temperature as high as 625 °C that resulted in mobility of 1.2 $cm^2/V \cdot s$ [18]. Therefore, the mobilities and subthreshold slopes we obtained are among the best ever measured in top-gate TFTs.

In conventional bottom gate devices, electrons move directly into the conduction band of the channel from the conduction band of the n^+ α-Si. In our Schottky-contact devices, there is a tunneling barrier from the metal-like source into the conduction band of the channel. The tunneling barrier is decreased as the gate voltage increases and creates a channel [19]. As such, device turn-on depends simultaneously on the tunneling threshold of the source Schottky contact and the inversion of the channel. Furthermore, the subthreshold behavior and leakage current may also be affected by the tunnel injection mechanism. At the present, it is unclear if the channel or the contact dominates the device behavior. A direct comparison of threshold voltage, subthreshold, or leakage current between our devices and conventional bottom devices is not possible because of the different electron mechanism and the inherently different nature of the $\alpha - \mathrm{Si/SiN}_x$ interface in the top-gate versus bottom-gate configuration (e.g., potentially different interface charges). Gated four-terminal devices are being fabricated to help understand the nature of the contact and of the interface.

IV. Summary and Conclusion

We have demonstrated a top-gate α-Si TFT process with silicide S/D self-aligned to the gate edge. The FET performance is excellent with sharp subthreshold slopes and high saturation mobilities at relatively short channel length. The low process temperature makes it viable for flexible plastic substrates. These observations suggest that the top-gate self-aligned silicide structure is an attractive path for high-speed and low-power α-Si TFT circuitry on flexible substrates.

References

[1] J. P. Lu, P. Mei, J. Rahn, J. Ho, Y. Wang, J. B. Boyce, and R. A. Street, "The impact of self-aligned amorphous Si thin film transistors on imager array applications," *J. Non-Crystalline Solids*, vol. 266–269, pt. 2, pp. 1294–1298, May 2000.

[2] D. B. Thomasson and T. N. Jackson, "Fully self-aligned tri-layer a-Si:H thin-film transistors with deposited doped contact layer," *IEEE Electron Device Lett.*, vol. 19, no. 4, pp. 124–126, Apr. 1998.

[3] M. J. Powell *et al.*, "A fully self-aligned amorphous silicon TFT technology for large area image sensors and active-matrix displays," in *Proc. MRS Symp.*, 1998, vol. 507, pp. 91–98.

[4] J. R. Pfiester, R. D. Sivan, H. M. Liaw, C. A. Seelbach, and C. D. Gunderson, "A self-aligned elevated source/drain MOSFET," *IEEE Electron Device Lett.*, vol. 11, no. 9, pp. 365–367, Sep. 1990.

[5] J. I. Ryu, K. H. Churl, K. S. Ki, and A. J. Jang, "A novel self-aligned polycrystalline silicon thin-film transistor using silicide layers," *IEEE Electron Device Lett.*, vol. 18, no. 6, pp. 272–274, Jun. 1997.

[6] S. Takeuchi *et al.*, "An excimer laser assisted process for top gate a-Si TFTs," in *Proc. IEEE AMLCD Int. Workshop*, 1994, pp. 108–111.

[7] C. C. Tsai, Y.-J. Lee, K.-Y. Chiang, J.-L. Wang, I. C. Lee, H.-H. Chen, K.-F. Wei, T.-K. Chang, B.-T. Chen, and H.-C. Cheng, "Polycrystalline silicon thin-film transistors with location-controlled crystal grains fabricated by excimer laser crystallization," *Appl. Phys. Lett*, vol. 91, no. 20, p. 201 903-3, Nov. 2007.

[8] W. A. MacDonald, "Engineered films for display technologies," *J. Mater. Chem.*, vol. 14, no. 1, pp. 4–10, 2004.

[9] K. Long, A. Z. Kattamis, I. C. Cheng, H. Gleskova, S. Wagner, and J. C. Sturm, "Stability of amorphous-silicon TFTs deposited on clear plastic substrates at 250 °C to 280 °C," *IEEE Electron Device Lett.*, vol. 27, no. 2, pp. 111–113, Feb. 2006.

[10] K. H. Cherenack, A. Z. Kattamis, B. Hekmatshoar, J. C. Sturm, and S. Wagner, "Amorphous-silicon thin-film transistors fabricated at 300 °C on a free-standing foil substrate of clear plastic," *IEEE Electron Device Lett.*, vol. 28, no. 11, pp. 1004–1006, Nov. 2007.

[11] Y. Hu and S. P. Tay, "Spectroscopic ellipsometry investigation of nickel silicide formation by rapid thermal process," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 16, no. 3, pp. 1820–1824, May/Jun. 1998.

[12] B. Froment *et al.*, "Nickel vs. Cobalt silicide integration for sub-50 nm CMOS," in *Proc. 33rd Conf. Eur. Solid-State Device Res.*, Sep. 2003, pp. 215–218.

[13] S. Luan and G. W. Neudeck, "An experimental study of source/drain parasitic resistance effects in amorphous silicon TFTs," *J. Appl. Phys.*, vol. 72, no. 2, pp. 766–772, Jul. 1992.

[14] C. S. Chiang, J. Kanicki, and F. R. Libsch, "Electrical performance of top-gate amorphous silicon thin-film transistor," in *Proc. IEEE AMLCD Int. Workshop*, Sep. 1995, pp. 33–36.

[15] A. R. Rolland, J. Richard, J. P. Kleider, and D. Mencaraglia, "Electrical properties of amorphous silicon transistors and MIS-devices: Comparative study of top nitride and bottom nitride configurations," *J. Electrochem. Soc.*, vol. 140, no. 2, pp. 3679–3683, Dec. 1993.

[16] S. Martin, C. S. Chiang, J. Y. Nahm, T. Li, J. Kanicki, and Y. Ugai, "Influence of the amorphous silicon thickness on top gate thin-film transistor electrical performances," *Jpn. J. Appl. Phys.*, vol. 40, no. 2A, pp. 530–537, Feb. 2001.

[17] M. J. Powell, C. Glasse, P. W. Green, I. D. French, and I. J. Stemp, "An amorphous silicon thin-film transistor with fully self-aligned top-gate structure," *IEEE Electron Device Lett.*, vol. 21, no. 3, pp. 104–106, Mar. 2000.

[18] K. Pangal, J. C. Sturm, and S. Wagner, "Integration of amorphous and polycrystalline silicon thin-film transistors through selective crystallization of amorphous silicon," *Appl. Phys. Lett.*, vol. 75, no. 14, pp. 2091–2093, Oct. 1999.

[19] M. Jang, K. Kang, S. Lee, and K. Park, "Simulation of Schottky barrier tunnel transistor using simple boundary condition," *Appl. Phys. Lett.*, vol. 82, no. 16, pp. 2718–2720, Apr. 2003.