Amorphous-Silicon Thin-Film Transistors Fabricated at 300 °C on a Free-Standing Foil Substrate of Clear Plastic

Kunigunde H. Cherenack, Alex Z. Kattamis, Bahman Hekmatshoar, James C. Sturm, and Sigurd Wagner

***Abstract*—We have made hydrogenated amorphous-silicon thin-film transistors (TFTs) at a process temperature of 300 °C on free-standing clear-plastic foil substrates. The key to the achievement of flat and smooth samples was to design the mechanical stresses in the substrate passivation and transistor layers, allowing us to obtain functional transistors over the entire active surface. Back-channel-passivated TFTs made at 300 °C on glass substrates and plastic substrates have identical electrical characteristics and gate-bias-stress stability. These results suggest that free-standing clear-plastic foil can replace display glass as a substrate from the points of process temperature, substrate and device integrity, and TFT performance and stability.**

***Index Terms*—Amorphous silicon (a-Si), gate-bias stress, mechanical stress, plastic substrate, stability, thin-film transistor (TFT).**

I. Introduction

THIN-FILM transistor (TFT) backplanes made on optically clear-plastic foil substrate could find universal use in flexible displays because they may be employed with any kind of display frontplane—be it transmissive, emissive, or reflective. Transistors [1] and displays [2]–[4] on clear-plastic substrates have been demonstrated in the past. However, to accommodate the low process temperatures of commercial clear polymers [5], the deposition of the hydrogenated amorphous-silicon TFT (a-Si:H TFT) stack has been reduced from ∼300 °C on glass [6], [7] to as low as 75 °C [8]. While the initial electrical performance of a-Si:H TFTs fabricated at such ultralow temperatures is satisfactory, recent experiments have shown poor stability under gate-bias stress [9]–[12]. In response, we have been raising the a-Si:H-TFT process temperature on clear plastic [13], [14] to conduct a "glasslike" process at 300 °C in order to achieve "glasslike" TFT stability on plastic.

Our long-term goal is to enable roll-to-roll fabrication; therefore, we are working with free-standing substrates. To obtain functional transistors on free-standing plastic foil substrates, the mechanical stress needs to be carefully designed [15], [16]. In this letter, we focus on the mechanical stresses built into the device layers and on comparing the performance and stability of the TFTs made on clear-plastic foil to those made on glass.

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II. Substrate Preparation

The 7.5×7.5 cm^2 and 75-μm-thick optically clear-plastic foil substrates that we use have a working temperature of ≥ 300 °C. Their in-plane coefficient of thermal expansion $\alpha_{\mathrm{substrate}}$ is ≤ 10 ppm/°C, which is sufficiently low to obtain intact device layers in a 300-°C process [17]. A rule of thumb for crack prevention is $(\alpha_{\mathrm{substrate}} - \alpha_{\mathrm{TFT}}) \times (\mathrm{T}_{\mathrm{process}} - \mathrm{T}_{\mathrm{room}}) \leq 0.3\%$. During plasma-enhanced chemical-vapor deposition (PE-CVD), the substrate is placed in a frame facing downward and is backed first with a Kapton E polyimide foil, then with a glass slide, and finally with a graphite plate, as shown in Fig. 1(a). The carbon serves as a black-body absorber for radiative heating in the nominally isothermal PE-CVD preheat and deposition zones. This mount lets the substrate expand and contract to some extent during PE-CVD. Following an outgassing anneal at 200 °C in the load lock, the substrate is transferred to the SiN_x deposition chamber for deposition at 280 °C of a 300-nm-thick SiN_x passivation layer on the future device side (front) of the substrate, at an RF (13.56 MHz) power density of 20 mW/cm^{-2}, which puts the SiN_x under tensile stress. The substrate is transferred back to the load lock and is flipped to expose its back side. It is then returned to the SiN_x chamber, and a 300-nm-thick SiN_x passivation layer is deposited at 280 °C on the back side of the substrate at a high plasma power density (90 mW/cm^{-2}), which produces compressive stress in the SiN_x.

III. Control of Mechanical Stress

In the order of increasing difficulty, the goals of stress control are the following: 1) prevention of circuit fracture during fabrication; 2) keeping the substrate flat; and 3) accurate overlay alignment between device layers. While the overall principles of stress control are known [15], [18], working at 300 °C and close to the glass-transition temperature of the substrate takes considerable experimentation. Although we had expected to need compressive stresses in both SiN_x passivation layers, we found that the first SiN_x layer must be grown with tensile stress and the second with a compressive stress. Together with the mechanical stresses built into the TFT films [15], this passivation procedure results in the smooth and flat surface of the final product shown in the photograph of Fig. 1(b). The principal tool for setting film stress is the RF power used in PE-CVD, which is aided, in some instances, by the deposition temperature. While

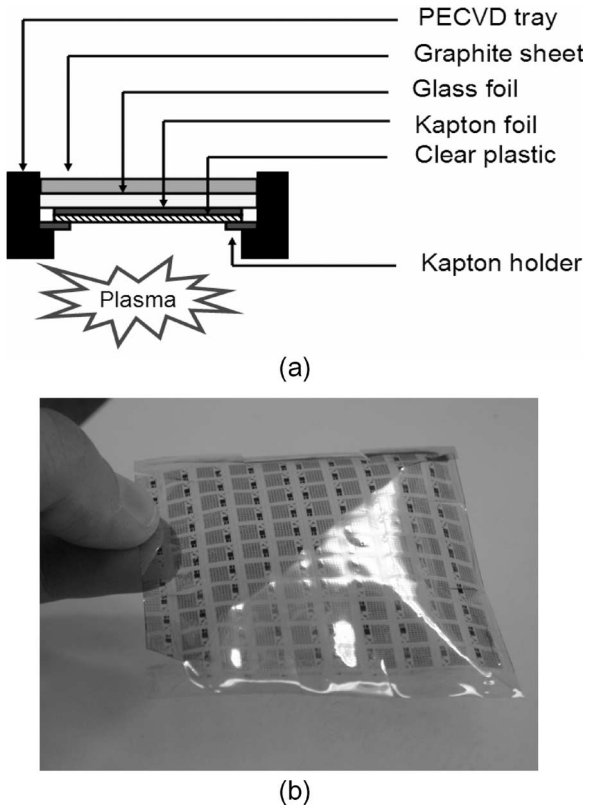

Fig. 1. (a) Cross-sectional view of face-down substrate mount for PE-CVD. (b) Photograph of a fully processed sample, which is bent under its own weight.

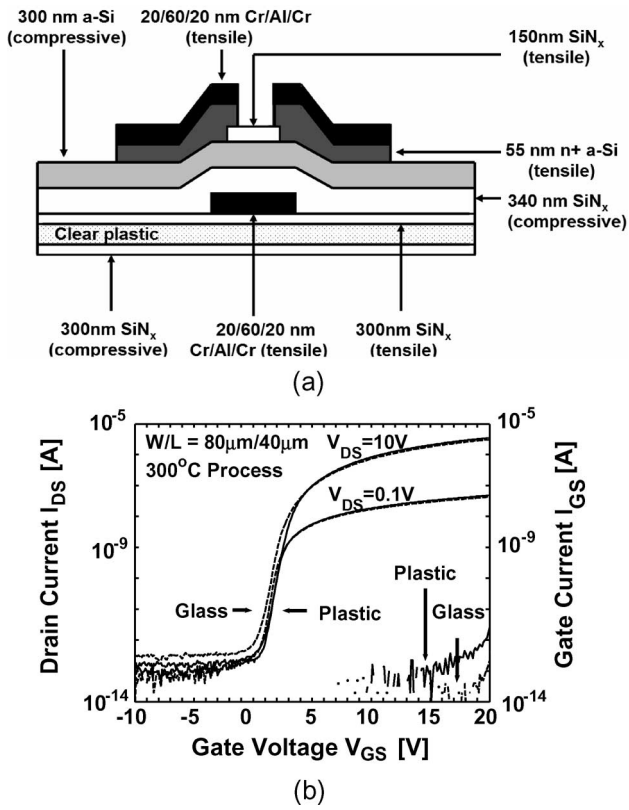

Fig. 2. (a) Schematic cross-sectional view of the back-channel-passivated TFT with layer materials, thicknesses, and stresses. (b) Transfer characteristics of a-Si:H TFTs made on clear plastic and glass at 300 °C.

the relation between stress and RF power has been determined for a polyimide foil substrate at 150 °C [15], we have not yet quantified the relation for the clear-plastic substrates at 300 °C. A number of experimental observations suggest that additional parameters affect the stress in films deposited near the glass-transition point of a free-standing polymer substrate. The stress in each device film is listed in the following section and in Fig. 2(a).

IV. Transistor Fabrication and Evaluation

A schematic cross section of the back-channel-passivated TFT is shown in Fig. 2(a). For comparison with earlier results, we make the channel length $L = 40$ μm and width $W = 80$ μm. The source–drain/gate overlap is set to 10 μm to provide tolerance against change in substrate dimensions between patterning of the gate metal and the source/drain contacts, which are made of thermally evaporated trilayers of 20-nm Cr, 80-nm Al, and 20-nm Cr. While the power for the gate nitride must be kept high to ensure electrical stability [19], the deposition conditions for the other SiN_x layers may be varied. The 340-nm-thick SiN_x gate dielectric is deposited at 300 °C and at a power density of 90 mW/cm^{-2} (compressive stress). The 300-nm a-Si:H channel layer is deposited at 17 mW/cm^{-2} (compressive), the 55-nm n^+ a-Si:H layer at 20 mW/cm^{-2} (tensile), and the 150-nm-thick SiN_x layer for back-channel passivation at 20 mW/cm^{-2} (tensile), all at 280 °C. After fabrication, the samples are annealed at 180 °C for 30 min in air.

The TFTs are evaluated and gate-bias-stressed using an HP4155A parameter analyzer. For transfer characteristics, the gate voltage is swept from 20 to -10 V at 10-V drain–source voltage. During gate-bias stressing, the source and drain are grounded, and a positive voltage is applied to the gate for 600 s. Then, the transfer characteristic is measured again by sweeping the gate voltage from 20 to -10 V. This was done for gate-bias voltages of 30 to 60 V, corresponding to electric fields of $(0.9 \text{ to } 1.8) \times 10^8$ V/m. The shift in the threshold voltage was determined on the subthreshold slope of the transfer curves at the drain–current value of 1×10^{-10} A.

V. Results and Discussion

Typical transfer characteristics for back-channel-passivated a-Si:H TFTs are shown in Fig. 2(b). On clear plastic, the linear mobility is 0.95 cm^2/V $\cdot$ s, the saturation mobility is 0.96 cm^2/V $\cdot$ s, the threshold voltage is $\sim$3.5 V, the on/off current ratio is $> 1 \times 10^7$, and the subthreshold slope is 500 mV/decade. To confirm that the TFT characteristics are independent of the substrate on which they are fabricated, we also fabricated identical a-Si:H TFTs on a glass substrate at 300 °C. The transfer characteristics for TFTs fabricated on glass, which are also shown in Fig. 2(b), are almost identical to those measured for TFTs fabricated on the clear plastic, although it should be noted that the gate-leakage current I_{gs} is slightly lower on glass.

The threshold-voltage shifts after gate-bias stressing for TFTs fabricated at 300 °C on glass and plastic substrates are

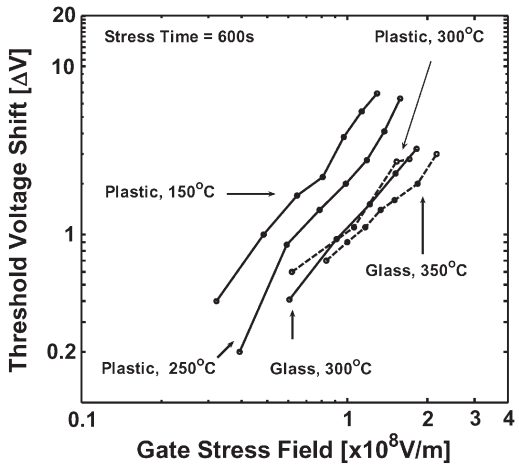

Fig. 3. Threshold-voltage shift versus gate-bias field for the a-Si:H TFTs of this letter and TFTs fabricated at 150 °C, 250 °C [12], and 350 °C [20]. Solid lines for clear-plastic foil; dashed lines for glass substrates.

shown in Fig. 3, together with the results that we obtained earlier for back-channel-etched TFTs fabricated on plastic (150 °C, 200 °C, and 250 °C) [12] and the literature data obtained at 350 °C on glass [20]. These results clearly demonstrate that the a-Si:H-TFT stability improves as the TFT process temperature is raised. At the stress field of 1×10^8 V/s, the voltage shift for 150 °C TFTs is 4 V and decreases to 2 V for 250 °C and to 1.1 V for 300 °C. Clearly, increasing process temperature is important for fabricating highly stable devices.

VI. Conclusion

Fabricating a-Si:H TFTs on clear plastic at 300 °C produces initial electrical characteristics and gate-bias-stress stability comparable to TFTs made on glass. Proper combination of mechanical stresses in the substrate passivation and TFT layers produces intact and aligned devices on a flat substrate.

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References

[1] J. Y. Kwon, D. Y. Kim, H. S. Cho, K. B. Park, J. S. Jung, J. M. Kim, Y. S. Park, and T. Noguchi, "Low temperature Poly-Si thin film transistor on plastic substrates," *IEICE Trans. Electron.*, vol. E88-C, no. 4, pp. 667–671, 2005.

[2] D. P. Gosain, T. Noguchi, and S. Usui, "High mobility thin film transistors fabricated on plastic substrates at a processing temperature of 110 °C," *Jpn. J. Appl. Phys. 2, Lett.*, vol. 39, no. 3A/B, pp. L179–L181, Mar. 2000.

[3] K. Long, A. Z. Kattamis, I-C. Cheng, H. Gleskova, S. Wagner, J. C. Sturm, M. Stevenson, G. Yu, and M. O'Regan, "Active-matrix amorphous-silicon TFTs arrays at 180 °C on clear plastic and glass substrates for organic light-emitting displays," *IEEE Trans. Electron Devices*, vol. 53, no. 8, pp. 1789–1796, Aug. 2006.

[4] K. R. Sarma, "A-Si TFT OLED fabricated on low-temperature flexible plastic substrate," in *Mater. Res. Soc. Symp. Proc.*, 2004, vol. 814, pp. I13.1.1–I13.1.12.

[5] W. A. MacDonald, "Engineered films for display technologies," *J. Mater. Chem.*, vol. 14, no. 1, pp. 4–10, 2004.

[6] C. Blaauw, "Preparation and characterization of plasma-deposited silicon nitride," *J. Electrochem. Soc.*, vol. 131, no. 5, pp. 1114–1118, 1984.

[7] S. Wagner, H. Gleskova, J. C. Sturm, and Z. Suo, "Novel processing technology for macroelectronics," in *Technology and Application of Amorphous Silicon*, R. A. Street, Ed. Berlin, Germany: Springer-Verlag, 2000, pp. 222–251.

[8] C. R. McArthur, "Optimization of 75 °C amorphous silicon nitride for TFTs on plastics," M.S. thesis, Univ. Waterloo, Waterloo, ON, Canada, 2003.

[9] R. B. Wehrspohn, S. C. Deane, I. D. French *et al.*, "Relative importance of the Si–Si bond and Si–H bond for the stability of amorphous silicon thin film transistors," *J. Appl. Phys.,* vol. 87, no. 1, pp. 144–154, Jan. 2000.

[10] C.-S. Yang, L. L. Smith, C. B. Arthur, and G. N. Parsons, "Stability of low-temperature amorphous silicon thin film transistors formed on glass and transparent plastic substrates," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 18, no. 2, pp. 683–689, Mar./Apr. 2000.

[11] Y. Kaneko, A. Sasano, and T. Tsukada, "Characterization of instability in amorphous silicon thin-film transistors," *J. Appl. Phys.*, vol. 69, no. 10, pp. 7301–7305, May 1991.

[12] K. Long, A. Z. Kattamis, I-C. Cheng, H. Gleskova, S. Wagner, and J. C. Sturm, "Stability of amorphous-silicon TFTs deposited on clear plastic substrates at 250 °C to 280 °C," *IEEE Electron Device Lett.*, vol. 27, no. 2, pp. 111–113, Feb. 2006.

[13] K. Long, "Towards flexible full-color active matrix organic light-emitting displays: Dry dye printing for OLED integration and 280 °C amorphous-silicon thin-film transistors on clear plastic substrates," Ph.D. dissertation, Princeton Univ., Princeton, NJ, 2006.

[14] A. Z. Kattamis, I-C. Cheng, K. Long, B. Hekmatshoar, K. Cherenack, S. Wagner, J. C. Sturm, S. Venugopal, D. E. Loy, S. M. O'Rourke, and D. R. Allee, "Amorphous silicon thin-film transistor backplanes deposited at 200 °C on clear plastic," *IEEE J. Display Technol.*, vol. 3, no. 3, pp. 304–308, Sep. 2007.

[15] I-C. Cheng, A. Kattamis, K. Long, J. Sturm, and S. Wagner, "Stress control for overlay registration in a-Si:H TFTs on flexible organic-polymer-foil substrates," *J. Soc. Inf. Disp.*, vol. 13, no. 7, pp. 563–568, 2005.

[16] H. Gleskova, I-C. Cheng, S. Wagner, and Z. G. Suo, "Thermomechanical criteria for overlay alignment in flexible thin-film electronic circuits," *Appl. Phys. Lett.*, vol. 88, no. 1, pp. 011905-1–011905-3, Jan. 2006.

[17] S. Wagner, H. Gleskova, I-C. Cheng, J. C. Sturm, and Z. Suo, "Mechanics of TFT technology on flexible substrates," in *Flexible Flat Panel Displays*, G. P. Crawford, Ed. West Sussex, U.K.: Wiley, 2005, pp. 263–283.

[18] H. Gleskova, I-C. Cheng, S. Wagner, and Z. Suo, "Mechanical theory of the film-on-substrate-foil structure: Curvature and overlay alignment in amorphous silicon thin-film devices fabricated on free-standing foil substrates," in *Flexible Electronics: Materials and Applications*, W. S. Wong and A. Salleo, Eds. New York: Springer-Verlag. in press.

[19] A. Z. Kattamis, K. Cherenack, B. Hekmatshoar, I-C. Cheng, H. Gleskova, J. C. Sturm, and S. Wagner, "Effect of SiN_x gate dielectric deposition power and temperature on a-Si:H TFT stability," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 606–608, Jul. 2007.

[20] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," *Appl. Phys. Lett.*, vol. 62, no. 11, pp. 1286–1288, Mar. 1993.