Tradeoff regimes of lifetime in amorphous silicon thin-film transistors and a universal lifetime comparison framework

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We report that the dependence of the lifetime of hydrogenated amorphous silicon (*a*-Si:H) thin-film transistors (TFTs) versus channel sheet resistance (R_{sheet}) exhibits two distinctly different regimes. At low R_{sheet} (high gate electric field) the lifetime is strongly dependent on R_{sheet}, decreasing as R_{sheet} is decreased. At high R_{sheet} (low gate electric field), the lifetime becomes independent of R_{sheet}. These two regimes of lifetime are dominated by different degradation mechanisms. By including hydrogen dilution in the deposition process, the extrapolated time for the 10% and 50% decay of the TFT current under dc operation in the low gate field regime can be raised to over 2 and 1000 yr, respectively. © *2009 American Institute of Physics*. [doi:10.1063/1.3238559]

The electrical stability of hydrogenated amorphous silicon (*a*-Si:H) thin-film transistors (TFTs) is important for new large-area applications such as active-matrix organic light-emitting diode (AM-OLED) displays. The threshold voltage of *a*-Si:H TFTs increases during operation, reducing the TFT drive current.[1,2] It is well-known that AM-OLED displays are far more sensitive to the TFT threshold voltage shift than active-matrix liquid crystal displays.[3,4]

In this letter, we demonstrate two regimes of *a*-Si:H TFT lifetime versus the TFT channel sheet resistance and explain their physical origins. We also show that at a high channel sheet resistance, the extrapolated TFT lifetime can be raised to over 2 and 1000 yr for 10% and 50% current decay under dc operation, respectively. Finally, we compare the lifetime of our *a*-Si:H TFTs with other *a*-Si:H TFTs in the literature as well as other TFT technologies.

TFTs were first fabricated with a back-channel etched process,[3] using "standard" *a*-Si:H (grown from pure silane at 250 °C) and 300-nm-thick standard gate nitride (grown from silane and ammonia at 300 °C), both by plasma-enhanced chemical vapor deposition (PECVD). dc stress measurements were performed in the linear and saturation modes by applying drain-source voltages of 0.1 V (for gate voltages up to 120 V) and 15 V (for gate voltages up to 10 V), respectively, and the TFT current decay was measured over time (Fig. 1). Because the current decays faster (lifetime is lower) at high gate voltages (low channel sheet resistance), from an application point of view, it is useful to examine the lifetime versus channel sheet resistance. The channel sheet resistance (R_{sheet}) is defined as $(V_{DS}/I_{TFT,lin})\cdot(L/W)$, where V_{DS} is the drain-source voltage, $I_{TFT,lin}$ is the TFT current in the linear mode, L is the channel length, and W is the channel width. We choose channel sheet resistance instead of gate voltage since the drain current and circuit delay can be determined directly from the channel sheet resistance without being affected by changes in the gate insulator capacitance, carrier mobility, and initial threshold voltage.

The lifetime for a 10% decay of current ($\tau_{10\%}$) from the data of Fig. 1 shows two different regimes (Fig. 2). At low channel sheet resistance there is a tradeoff between high lifetime and low channel sheet resistance (both desirable device parameters). At high channel sheet resistance, the lifetime becomes independent of channel sheet resistance.

To understand the physical origin of the two regimes, we extracted the TFT threshold voltage rise (ΔV_T) from the decay of current (Fig. 3), assuming negligible shift in mobility and other TFT parameters.[1–4] We assume first-order TFT equations in the linear and saturation regimes

$$I_{TFT,lin}(t) = 2k[V_{GS} - V_{T0} - \Delta V_{T,lin}(t)]V_{DS}, \tag{1a}$$

$$I_{TFT,sat}(t) = k[V_{GS} - V_{T0} - \Delta V_{T,sat}(t)]^2, \tag{1b}$$

where k is defined as $\mu_{FE}C_{ins}(W/2L)$, V_{GS} is the gate-source voltage, V_{T0} is the initial threshold voltage, μ_{FE} the field-effect mobility of carriers (electrons), and C_{ins} the gate dielectric capacitance per unit area, i.e., $\varepsilon_{ins}/t_{ins}$, where ε_{ins} and t_{ins} are the dielectric constant and thickness of the gate dielectric ($\varepsilon_{ins}=7.4\varepsilon_0$ for nitride). The subscripts "lin" and "sat" refer to the linear and saturation modes, respectively. For our standard *a*-Si:H TFTs ($L=5$ μm), $\mu_{FE}=0.64\pm0.05$ cm^2/V s, and $V_{T0}=2.2\pm0.2$ V.

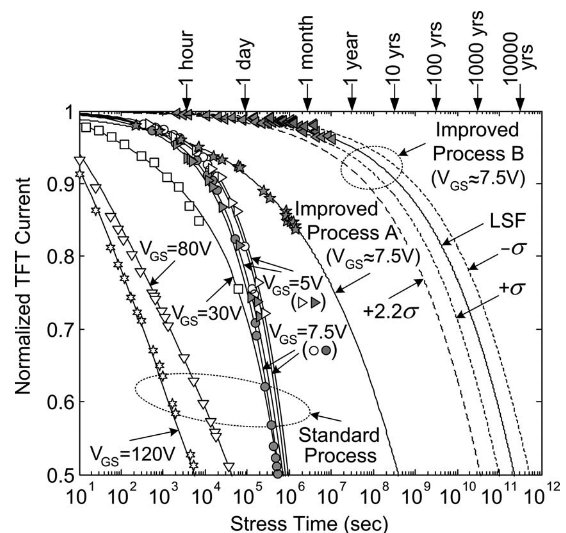

FIG. 1. Degradation of *a*-Si:H TFT current in the linear (open symbols) and saturation mode (solid symbols). The lines are predictions based on Eqs. (3) and (5). The dashed lines show the error bounds of the fitting.

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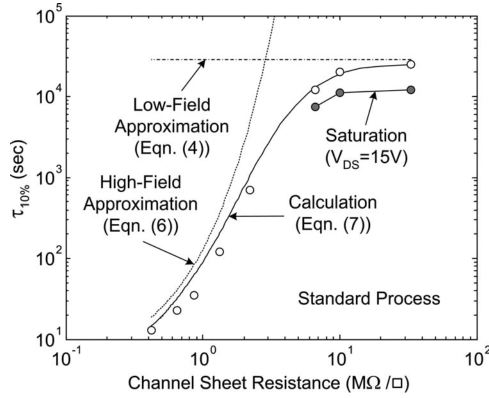

FIG. 2. The 10% current decay lifetime ($\tau_{10\%}$) vs channel sheet resistance ($1/[\mu_{FE}C_{ins}(V_{GS}-V_{T0})]$) for our standard TFTs along with the high and low field approximations and calculation for the linear mode. Open and solid symbols indicate the linear and saturation modes, respectively.

Qualitatively, the two regimes may be understood as follows. The TFT threshold voltage shift is caused by the channel electrons trapped into the gate nitride or the defects created in the a-Si:H channel.[1,2] The channel sheet resistance increases with the drop in the number of mobile channel electrons, n_{chan} (note $n_{chan}=C_{ins}(V_{GS}-V_T)=C_{ins}(V_{GS}-V_{T0})+Q_{trap}/q$, where V_T is the TFT threshold voltage, Q_{trap} is the trapped charge ($Q_{trap}<0$), and q is the electron charge). The fractional change in channel sheet resistance is

$$\frac{\Delta R_{sheet}}{R_{sheet}} \approx \frac{-\Delta n_{chan}}{n_{chan}} \propto \frac{-Q_{trap}/\varepsilon_{ins}}{n_{chan}} \propto \frac{-Q_{trap}/\varepsilon_{ins}}{E_{ins}}, \qquad (2)$$

where E_{ins} is the gate electric field, defined as V_{GS}/t_{ins}. In writing Eq. (2), we assume the gate insulator is thick compared to the a-Si:H/nitride interface region where charge trapping occurs). At low gate electric fields ($V_{GS}<\sim 7.5$ V for our nitride thickness), the threshold voltage shift is dominated by defect creation in a-Si:H and electron trapping in these defects.[3,4] The rate of this process (and thus the trapped charge) and ΔR_{sheet} are proportional to the number of mobile channel electrons.[2,5] Thus $\Delta R_{sheet}/R_{sheet}$ (and thus the TFT lifetime) is independent of R_{sheet} in this regime, explaining the observation in Fig. 2. At high gate fields ($V_{GS}>\sim 30$ V), the threshold voltage shift is dominated by charge trapping in the PECVD gate nitride, where Fowler–Nordheim tunneling is dominant at room temperature,[6] resulting in an approximately quadratic dependence on the gate electric field.[7] Therefore at high gate fields, $\Delta R_{sheet}/R_{sheet} \propto E_{ins}$. The TFT lifetime drops with increasing the gate electric field (lowering R_{sheet}), again consistent with Fig. 2.

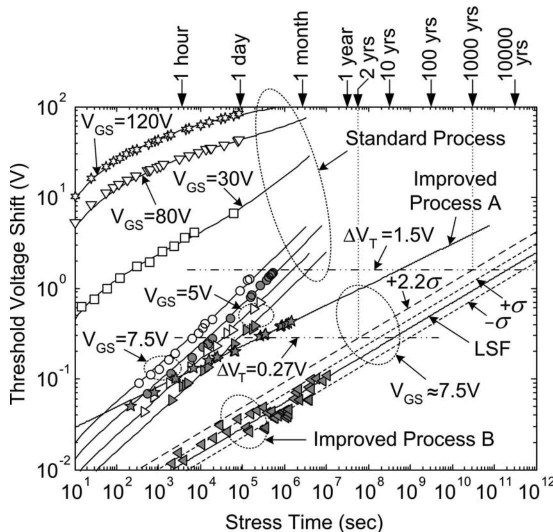

FIG. 3. Threshold voltage shifts of a-Si:H TFTs extracted from Fig. 1. The models (lines) are based on Eqs. (3) and (5). Open and solid symbols refer to the linear and saturation modes, respectively. The 0.27 and 1.5 V shifts correspond to 10% and 50% current drop at $V_{GS}=\sim 7.5$ V in saturation. The dashed lines show the error bounds of the fitting.

The two regimes of lifetime may be quantitatively modeled as follows. In the low-field regime (subscript "low-V_{GS}"), the threshold voltage shift may be approximated by a power law[1,2] (β and τ_0 are constants),

$$\Delta V_{T,\text{lin,low-}V_{GS}} \approx (V_{GS}-V_{T0})\cdot(t/\tau_0)^{\beta}. \qquad (3)$$

The saturation regime is important at low fields because it is the desired operation regime for driving OLEDs. In this regime, $\Delta V_{T,\text{sat,low-}V_{GS}}=(2/3)\Delta V_{T,\text{lin,low-}V_{GS}}$ as n_{chan} is lower by a factor of 2/3 compared to the linear mode.[5] For our standard TFTs, $\beta=0.45$ and $\tau_0=2.8\times10^6$ s. Using Eqs. (3) and (1a), the low-field lifetime in the linear regime is

$$\tau_{10\%,\text{lin,low-}V_{GS}} \approx \tau_0(0.1)^{1/\beta}. \qquad (4)$$

Using Eqs. (1b) and (3) (including the 2/3 factor), the low-field lifetime in saturation is lower than that in the linear regime by a factor of $[(2/3)\cdot(1+\sqrt{0.9})]^{1/\beta}$. This is because of a higher sensitivity of the TFT current to threshold voltage in saturation. In the high-field regime (subscript "high-V_{GS}"), ΔV_T is logarithmic in time[2,7] (B and t_0 are constants).

$$\Delta V_{T,\text{lin,high-}V_{GS}} \approx B\cdot {V_{GS}}^2\cdot\ln(1+t/t_0). \qquad (5)$$

For our standard TFTs, $t_0=4.7$ s and $B=5.8\times10^{-4}$ V^{-1}. The high field lifetime is found from Eqs. (5) and (1a)

$$\tau_{10\%,\text{lin,high-}V_{GS}} \approx t_0\exp(0.1/BV_{GS}). \qquad (6)$$

When both degradation mechanisms are important, $\tau_{10\%}$ may be calculated numerically

$$(V_{GS}-V_{T0})\cdot(\tau_{10\%,\text{lin}}/\tau_0)^{\beta}+B\cdot {V_{GS}}^2\cdot\ln(1+\tau_{10\%,\text{lin}}/t_0) \approx 0.1(V_{GS}-V_{T0}). \qquad (7)$$

This model fits the data quantitatively (Fig. 2).

We now show that the two lifetime regimes are present for other a-Si:H TFT fabrication technologies. The quality of a-Si:H may be improved by "*in situ*" removal of weak Si–Si bonds by hydrogen dilution during the PECVD of a-Si:H and a back-channel passivated TFT structure.[3,4] The improved a-Si:H (improved process A), improves the lifetime at high channel sheet resistance (red triangles in Fig. 4), as a result of a lower defect creation rate in the improved a-Si:H. Improving the quality of the gate nitride as well (improved process B) further improves the lifetime at both high and low channel sheet resistance (red squares in Fig. 4). This was achieved by using a deposition temperature of 350 °C and hydrogen dilution during the PECVD of the gate nitride for the *in situ* removal of weakly bonded Si atoms.[8] The improvement at high fields is due to lower charge trapping in the improved nitride as a result of a lower density of nitride traps. The improvement at low-fields may be due to an improved a-Si:H quality close to the a-Si:H/nitride interface. Since a-Si:H is deposited after the gate nitride, the quality of a-Si:H may be affected by that of the nitride underneath it.[3,4]

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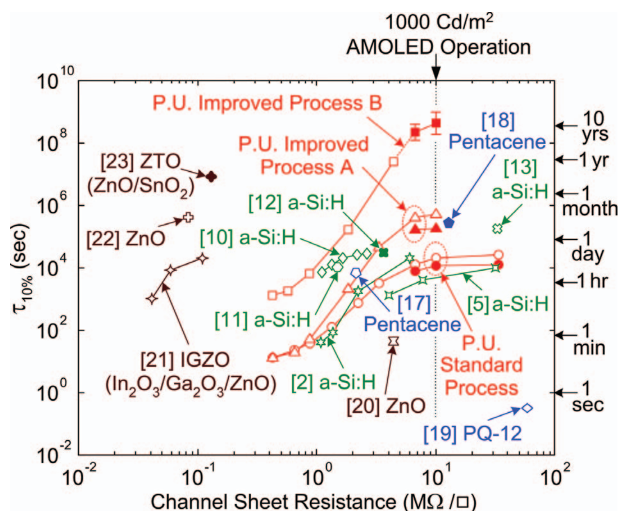

FIG. 4. (Color) The 10% current decay lifetime vs channel sheet resistance for our a-Si:H TFTs (P.U. refers to "Princeton University" and the error bars indicate the standard deviations of fitting errors), along with those of a-Si:H TFTs and other TFT technologies from other groups. Open and solid symbols refer to the linear and saturation modes, respectively.

For both improved processes, the two distinct lifetime regimes are clearly evident.

A low gate voltage of ~7.5 V ($V_{GS}-V_{T0}$=5.3 V and R_{sheet}=10 MΩ/□) is required for driving high quality OLEDs at a luminance of 1000 Cd/m^2 in a typical AMOLED design.[9] The current degradation of the improved a-Si:H TFTs at this drive condition is plotted in Fig. 1 (V_{T0} =2.4±0.2 V and 2.6±0.2 V for the improved processes A and B, respectively). The threshold voltage shifts are extracted from the current degradation and extrapolated based on Eq. (3) (including the 2/3 factor) using linear least squares fits (LSFs) (Fig. 3). These fits are then used to extrapolate the current degradation in Fig. 1 using Eq. (1b). The upper and lower error bounds corresponding to the standard deviation of errors in the LSF ($+\sigma$ and $-\sigma$) are also plotted for the improved process B. An upper error bound of $+2.2\sigma$ corresponds to 2 and 1000 yr of lifetime for 10% and 50% current decay, respectively. Assuming a normal distribution of errors, the $+2.2\sigma$ bound indicates a confidence of ~99% (~1% error) in prediction.

Converting the published plots of threshold voltage shift versus time to current decay for a-Si:H TFTs reported in the literature[2,5,10–13] shows that at low fields (high channel sheet resistances), the lifetimes of our standard a-Si:H TFTs (red circles in Fig. 4) and those reported in the literature (green symbols in Fig. 4) are comparable. Our improved a-Si:H TFTs have significantly higher lifetimes. This improvement is due to low defect creation rates in a-Si:H as indicated from both small values of β (0.22 and 0.26 for the improved processes A and B, respectively, versus 0.45 for the standard process) and large values of τ_0 (1.1×10^8 and 4×10^{10}, versus 2.8×10^6 s) extracted from the fits in Fig. 3. The low β of the improved TFTs physically corresponds to a sharper low energy tail of the distribution of bond energies, i.e., a lower density of weak bonds and thus a more stable material.[14,15] The large τ_0 implies a lower attempt frequency for bond breaking,[15,16] indicating a larger localization length of the electron wave-function and stronger Si–Si bonds.[16]

The presented lifetime comparison framework can be applied to other TFT technologies as well. The lifetimes of various TFTs reported in the literature TFTs are compared in Fig. 4. These lifetimes were determined by inspecting the published plots of TFT current decay versus time or converting the published plots of TFT threshold voltage shift versus time to plots of current decay, using Eq. (1a) or (1b) and extrapolation when necessary. Organic devices (blue symbols)[17–19] generally fall to the right due to their low mobilities and in the best case have a lifetime of ~3 days at 12.8 MΩ/□. Metal-oxide devices (brown symbols)[20–23] with low mobilities (~1 cm^2/V s) have channel sheet resistance values close to that of a-Si:H and those with higher mobilities (10–15 cm^2/V s) fall to the left, with a highest lifetime of ~100 days at 130 KΩ/□.

In summary, at low channel electron density, the lifetime of a-Si:H TFTs is independent of the channel sheet resistance. In contrast, at high channel electron density, the lifetime decays with decreasing the channel sheet resistance. At high channel sheet resistance, the extrapolated TFT lifetime can be raised to over 2 and 1000 yr for 10% and 50% current decay, respectively. This was achieved by including hydrogen dilution during growth to improve the quality of a-Si:H and the gate nitride.

[1]W. B. Jackson and M. D. Moyer, Phys. Rev. B **36**, 6217 (1987).
[2]M. J. Powell, C. van Berkel, and J. R. Hughes, Appl. Phys. Lett. **54**, 1323 (1989).
[3]B. Hekmatshoar, K. Cherenack, A. Kattamis, K. Long, S. Wagner, and J. C. Sturm, Appl. Phys. Lett. **93**, 032103 (2008).
[4]B. Hekmatshoar, K. Cherenack, S. Wagner, and J. C. Sturm, Tech. Dig. - Int. Electron Devices Meet. **2008**, 89.
[5]K. S. Karim, A. Nathan, M. Hack, and W. I. Milne, IEEE Electron Device Lett. **25**, 188 (2004).
[6]S. M. Sze, J. Appl. Phys. **38**, 2951 (1967).
[7]R. H. Walden, J. Appl. Phys. **43**, 1178 (1972).
[8]B. Hekmatshoar, S. Wagner, and J. C. Sturm, Device Research Conference, Conference Digest, 2009, p. 189.
[9]B. Hekmatshoar, A. Z. Kattamis, K. H. Cherenack, K. Long, J.-Z. Chen, S. Wagner, J. C. Sturm, K. Rajan, and M. Hack, IEEE Electron Device Lett. **29**, 63 (2008).
[10]F. R. Libsch and J. Kanicki, Appl. Phys. Lett. **62**, 1286 (1993).
[11]S. M. GadelRab and S. G. Chamberlain, IEEE Trans. Electron Devices **45**, 2179 (1998).
[12]H.-Y. Tseng, K.-Y. Chiang, H.-Y. Lui, C.-P. Kung, and T.-C. Chang, Jpn. J. Appl. Phys., Part 1 **46**, 1318 (2007).
[13]M. Kang, Y. Nam, S. Hong, E. Lee, J. Kim, J. Hur, D. Oh, S. Kim, J. Jang, S. Mano, and Y. Iketsu, SID Int. Symp. Digest Tech. Papers **39**, 93 (2008).
[14]M. J. Powell, C. Berkel, A. R. Franklin, S. C. Deane, and W. I. Milne, Phys. Rev. B **45**, 4160 (1992).
[15]R. S. Crandall, Phys. Rev. B **43**, 4057 (1991).
[16]R. B. Wehrspohn, S. C. Deane, I. D. French, and M. J. Powell, Thin Solid Films **383**, 117 (2001).
[17]S. Cipolloni, L. Mariucci, A. Valletta, D. Simeone, F. De Angelis, and G. Fortunato, Thin Solid Films **515**, 7546 (2007).
[18]T. Sekitani and T. Someya, Jpn. J. Appl. Phys., Part 1 **46**, 4300 (2007).
[19]T. N. Ng, M. L. Chabinyc, R. A. Street, and A. Salleo, IEEE Annual International Reliability Physics Symposium, 2007, p. 243.
[20]R. B. M. Cross, M. M. De Souza, S. C. Deane, and N. D. Young, IEEE Trans. Electron Devices **55**, 1109 (2008).
[21]A. Suresh and F. Muth, Appl. Phys. Lett. **92**, 033502 (2008).
[22]D. H. Levy, D. Freeman, S. F. Nelson, P. J. Cowdery-Corvan, and L. M. Irving, Appl. Phys. Lett. **92**, 192101 (2008).
[23]T. Riedl, P. Görrn, P. Hölzer, and W. Kowalsky, Phys. Status Solidi Rapid Res. Lett. **1**, 175 (2007).

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