Journal of the Korean Physical Society, Vol. 54, No. 1, January 2009, pp. 415∼420

Amorphous Silicon Thin-Film Transistors made on Clear Plastic at 300 °C

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(Received 24 January 2008)

We have made a-Si:H TFTs at a process temperature of 300 °C on free-standing clear plastic foil substrates and have improved the large-area alignment of TFT device layers. The key to achieving flat and crack-free samples is to design the mechanical stresses in the substrate passivation and transistor layers, allowing us to obtain functional transistors over the entire active surface. The TFT gate and the back-channel passivation were self-aligned. Back-channel passivated TFTs made at 300 °C on glass substrates and plastic substrate have identical electrical characteristics and gate bias stress stability. These results suggest that free-standing clear plastic foil can replace display glass as a substrate from the points of process temperature, substrate and device integrity and TFT performance and stability.

PACS numbers: 85
Keywords: a-Si:H Thin Film Transistors, Polymer Substrates, Strain Control, Self-alignment

I. INTRODUCTION

Thin-film transistor backplanes made on optically clear plastic substrate foils could find universal use in flexible displays because they may be employed with any kind of display frontplane, be it transmissive, emissive, or reflective. Transistors [1] and displays [2–4] on clear plastic substrates have been demonstrated in the past. However, in order to accommodate the low process temperatures of commercial clear polymers [5], the deposition of the a-Si:H thin film transistor (TFT) stack has been reduced from ∼300 °C on glass [6,7] to as low as 75 °C [8]. While the initial electrical performance of a-Si:H TFTs fabricated at such ultra-low temperatures is satisfactory, recent experiments have shown poor stability under gate-bias stress [9–12]. In response we have been raising the a-Si:H TFT process temperature on clear plastic [13–16] to conduct a "glass-like" process at 300 °C to achieve "glass-like" TFT stability on plastic.

Our long-term goal is to enable roll-to-roll fabrication - therefore we are working with free-standing substrates. To obtain functional transistors on free-standing plastic foil substrates, the mechanical stress needs to be designed carefully [17, 18]. Even if the device layers are crack-free, the stress in the TFT stack causes the substrate to expand or contract (depending on the nature of the combined strain of the total structure). This results in misalignment between consecutive mask layers. After high process temperatures this misalignment can be very large. It causes the TFTs at the edges of the substrate to malfunction. If it is not possible to reduce the total strain in the substrate by engineering the strain, as mentioned above, it becomes necessary to investigate alternative methods. The misalignment can be reduced by laminating or electrostatically bonding the substrate to a stiff carrier plate [19], by clamping the substrate into a rigid frame [20], or by digitally compensating the masks for substrate distortion [21]. In our work we focus on developing self-alignment methods which would serve to eliminate overlay misalignment completely. One requirement necessary to implement self-alignment is the ability to expose the photoresist through the back of the substrate [22]. Since the amorphous silicon layer in the TFT stack is very absorptive at the UV wavelength, this means that we need to reduce the thickness of our amorphous silicon channel region as much as possible. We chose to use a back-channel passivated TFT geometry that allowed us to reduce the a-Si:H layer thickness from our conventional thickness of ∼300 nm down to ∼25 nm while still maintaining a rugged TFT fabrication process. In this process the self-alignment is achieved between the gate (mask 1) and the channel passivation (mask 2). We discuss how the mechanical stress that is built into the device layers is adjusted to obtain crack-free device layers, the fabrication of self-aligned a-Si:H TFTs at 300 °C on a clear plastic substrate and the alignment issues that we overcame by using a self-aligned process.

II. EXPERIMENTS AND DISCUSSION

In order of increasing difficulty the goals of stress control are (i) prevention of circuit fracture during fabrica-

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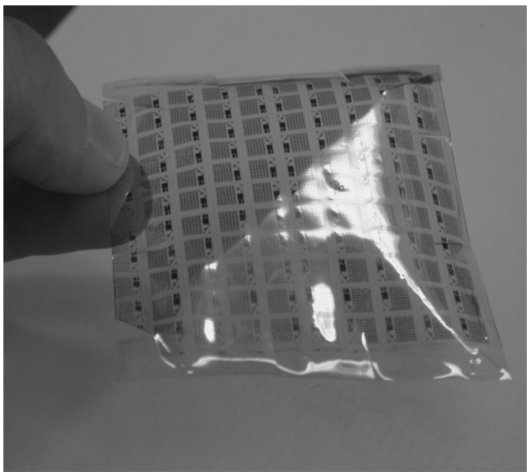

Fig. 1. Photograph of a fully processed sample which is bent under its own weight. The square substrate measures 7.5 cm on each side.

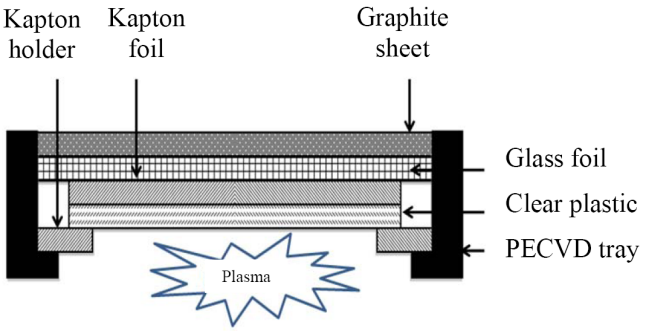

Fig. 2. Cross-sectional view of a face-down substrate mount for plasma-enhanced chemical vapor deposition.

tion (ii) keeping the substrate flat and (iii) accurate overlay alignment between device layers. While the overall principles of stress control are known [17,23], working at 300 °C and close to the glass transition temperature of the substrate takes considerable experimentation. Initially we had expected to need compressive stresses in both SiN_x passivation layers. We found that the first SiN_x layer must be grown with a tensile stress and the second with a compressive stress. Together with the mechanical stresses built into the TFT films [17], this approach to substrate passivation results in the smooth and flat surface of the final product shown in the photograph of Figure 1. The principal tool for setting film stress is the RF power used in plasma-enhanced chemical vapor deposition (PECVD), aided in some instances by the deposition temperature. While the relation between stress and RF power has been determined for a polyimide foil substrate at 150 °C [17], we have not yet quantified the relation for the clear plastic substrates at 300 °C. Several experimental observations suggest that additional parameters affect the stress in films deposited near the glass transition point of a free-standing polymer substrate. The 7.5 × 7.5 cm^2 and 75 μm thick optically clear plastic (CP) foil substrates that we use have a working temperature of ≥300 °C. Their in-plane coefficient of thermal expansion $\alpha_{\rm substrate}$ is ≤10 ppm/°C, which is sufficiently low to obtain intact device layers in a 300 °C process [23]. A rule of thumb for crack prevention is $(\alpha_{\rm substrate} - \alpha_{\rm TFT}) \times (T_{\rm process} - T_{\rm room}) \leq 0.3$ %. For plasma enhanced chemical vapor deposition (PE-CVD) the substrate is placed in a frame facing downward and is backed first with a Kapton E polyimide foil, then with a glass slide and finally with a graphite sheet, as shown in Figure 1. The graphite serves as a black body absorber for radiative heating in the nominally isothermal PE-CVD pre-heat and deposition zones. This mount lets the substrate expand and contract to some extent during PE-CVD. Following an outgassing anneal at 200 °C in the load lock, the substrate is transferred to the SiN_x deposition-chamber for deposition at 280 °C of a 300 nm thick SiN_x passivation layer on the future device side (front) of the substrate at an RF (13.56 MHz) power density of 20 mW/cm^{-2}, which puts the SiN_x under tensile stress. The substrate is transferred back to the load lock and flipped to expose its back side. It is then returned to the SiN_x chamber and a 300 nm thick SiN_x passivation layer is deposited at 280 °C on the back side of the substrate at a high plasma power density (90 mW/cm^{-2}), which produces compressive stress in the SiN_x.

From past experiments we know that the substrate has an optical transmission, T, of ∼88 % in the visible region and an optical absorption edge at $\lambda \sim 400$ nm [24]. Therefore, for photolithographic exposure, we selected the mercury line at 405 nm. The optical absorption at 405 nm by SiN is negligibly small but a-Si:H strongly absorbs in this region. We studied the optical transmission of our clear plastic at $\lambda = 405$ nm, which had been coated with (i) the usual barrier layers and (ii) the usual barrier layers as well as a variety of amorphous silicon layers deposited on top of the front barrier layer. The results are shown in Figure 3. To keep the exposure time for the self-alignment step relatively short, we chose an a-Si:H channel layer thickness of 25 nm for our TFT process.

The transistor fabrication process is shown in Figure 4. Throughout the process the substrate is kept free-standing except that is precisely flattened for photolithography by temporarily bonding it to a glass plate with water. After our usual substrate preparation (step 1), a thermally evaporated tri-layer of 20 nm Cr, 60 nm Al and 20 nm Cr. is deposited (step 2). The sample is loaded into the PE-CVD system and the following depositions are carried out: (i) a 340 nm thick SiN_x gate dielectric at 300 °C (step 3) at a power density of 90 mW/cm^{-2}, (ii) a 25 nm a-Si:H channel layer deposited at 17 mW/cm^{-2} (step 4) and (iii) a 150 nm thick SiN_x layer as the channel passivation (step 5). Now the sample is removed from the PE-CVD system and we spin-coat the sample with the photoresist. We then expose the substrate through the back in our mask aligner

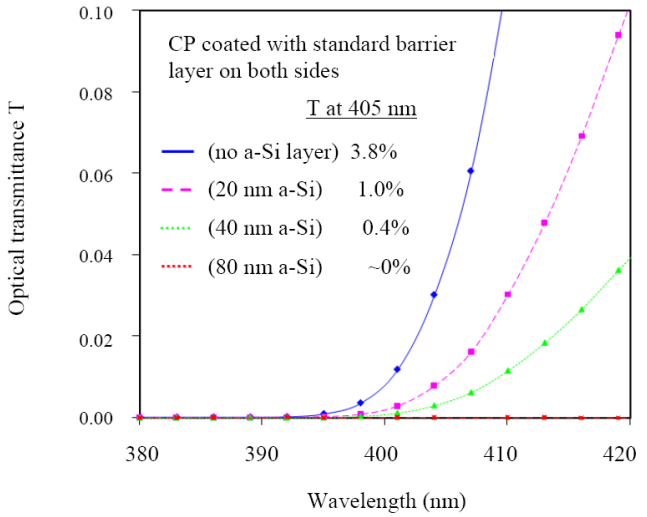

Fig. 3. Optical transmission in the violet and near-UV region of (a) a clear plastic substrate coated with a standard SiN_x barrier layer and of a clear plastic coated only with (b) 20 nm, (c) 40 nm and (d) 80 nm thick i a-Si:H layers.

for 15 minutes at a power density of 3.5 mW/cm^2. In this step the bottom gate electrode acts as the mask to self-align the channel passivation to the gate (step 6). The SiN_x layer is now wet etched in buffered oxide etch ($HF:NH_4F:H_2O$) for 50 seconds. By slightly over-etching the back-channel SiN_x protection layer during the patterning, the required overlap over the gate is created (step 7). A piranha clean (H_2O_2:H_2SO_4), followed by a short buffered oxide etch dip, ensures a clean interface between the exposed a-Si:H channel layer and the subsequently deposited S/D layer. Next, 50-nm n^+ a-Si:H and a 20/60/20-nm trilayer Cr/Al/Cr film are deposited and patterned for source/drain contacts (second mask level, step 8). This is followed by etching the a-Si:H to isolate individual devices (third mask level). Finally, holes are opened to contact the bottom gate (fourth mask level).

The extent of the channel passivation-gate electrode overlap is determined by a combination of (i) overexposure of the photoresist in process step 6, (ii) overdevelopment of the photoresist in step 6; and (iii) overetch of the back-channel SiN_x protection layer in step 7. Among these techniques past experience has shown [22] that overexposure of the photoresist provides best control of the degree of overlap on a large surface area. Over-development of the photoresist during step 6 can lead to ragged edges for the channel passivation while over-etching of the SiN_x layer during step 7 can result in dramatic over-etch or removal of the passivation layer entirely if care is not taken to control the etch. With the back-exposure conditions chosen in this experiment (back exposure for 15 minutes and a 50 second dip in 10 : 1 buffered HF) the over-etch was on the order of $\sim 1 - 2$ μm on either side of the gate-edge.

After fabricating the samples, they are annealed at

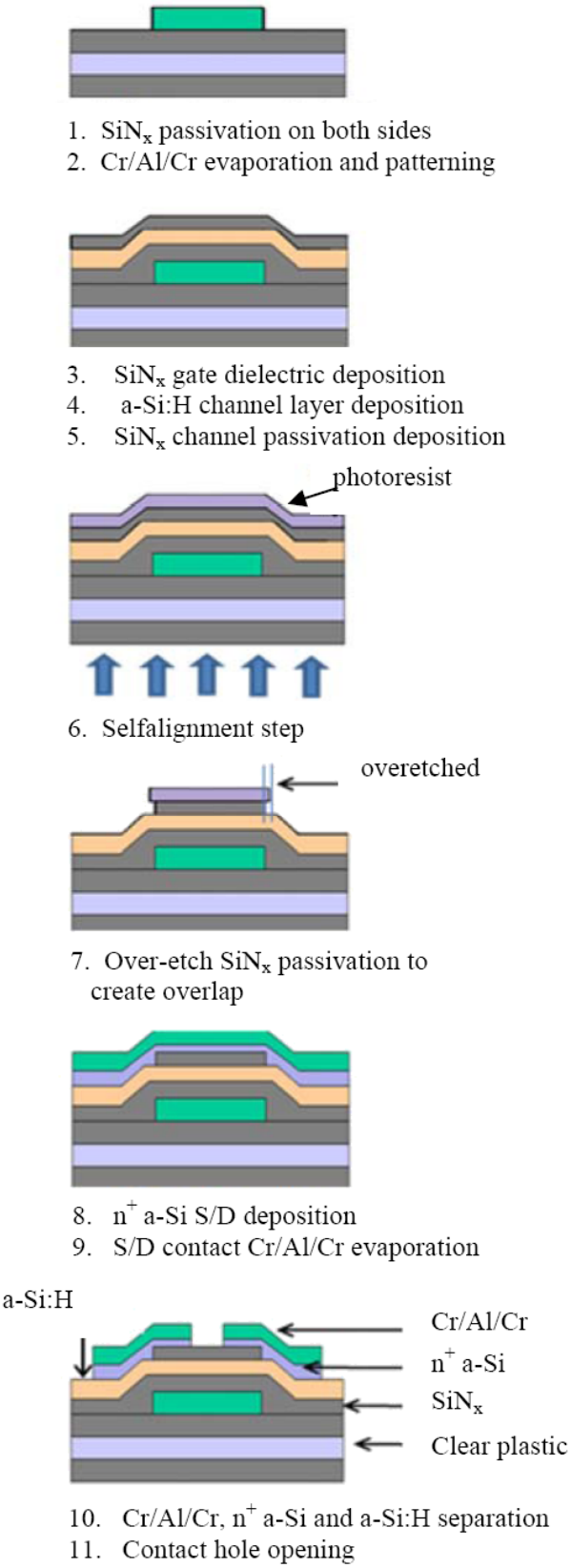

Fig. 4. Process sequence for a bottom-gate, back-channel passivated a-Si:H TFT made at 300 °C on a clear plastic substrate. The channel passivation is self-aligned to the gate by using a backside exposure that is self-aligned to the gate.

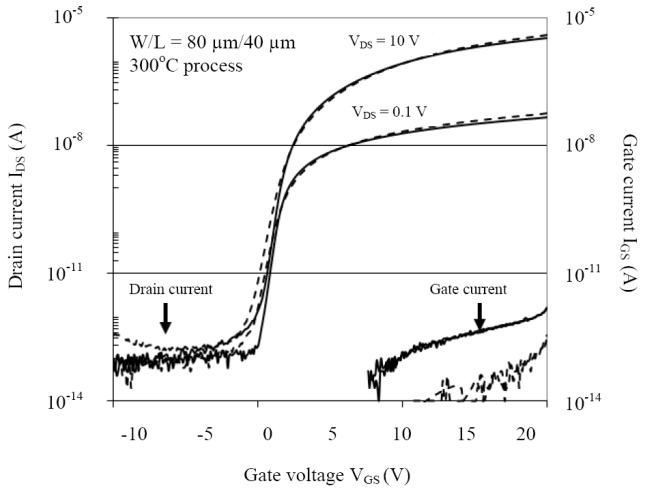

Fig. 5. Transfer characteristic of a-Si:H TFTs made with standard photolithography on clear plastic and on glass at 300 °C.

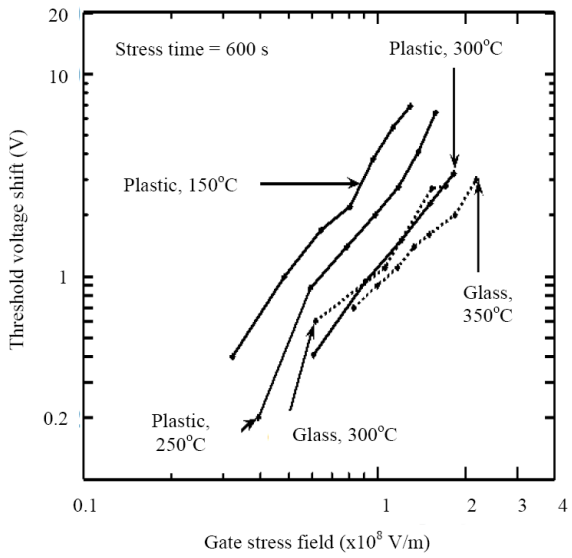

Fig. 6. Threshold voltage shift vs. gate bias field for the present a Si:H TFTs and TFTs fabricated at 150 °C, 250 °C [12] and 350 °C [?]. Solid lines indicate measurements for devices on clear plastic foil and dashed lines indicate those for glass substrates. $W/L = 80\ \mu$m/40 μm.

135 °C for 30 minutes in air. The TFTs are evaluated and gate-bias stressed using an HP4155A parameter analyzer. For the transfer characteristics, the gate voltage is swept from 20 V to −10 V, for a 10 V drain-source voltage. During gate bias stressing, the source and drain are grounded and a positive voltage is applied to the gate for 600 seconds. Then the transfer characteristic is measured again by sweeping the gate voltage from 20 V to −10 V. This is done for gate bias voltages from 30 V to 60 V, corresponding to electric fields of 0.9 to 1.8×10^8 V/m. The shift in the threshold voltage was determined on the subthreshold slope of the transfer curves at a drain

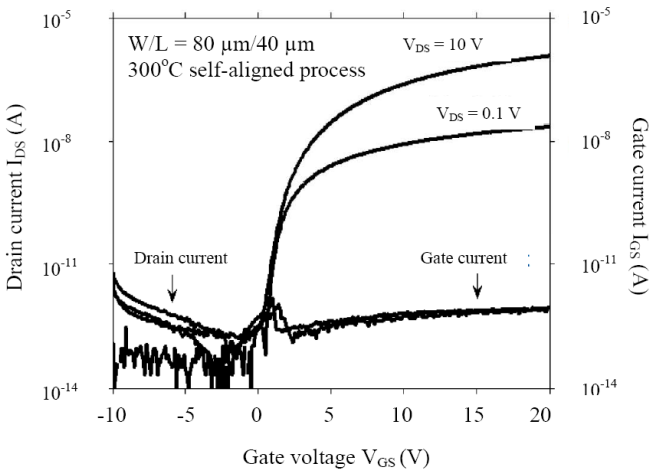

Fig. 7. Transfer characteristics of a self-aligned a-Si:H TFT made on clear plastic at 300 °C.

current value of 1×10^{-10} A. We use TFTs with a W/L ratio of 80 μm/40 μm.

Typical transfer characteristics for back-channel passivated a-Si:H TFTs are shown in Figure 5. These TFTs were fabricated using standard photolithography. On clear plastic the linear mobility is 0.95 cm^2/Vs, the saturation mobility 0.96 cm^2/Vs, the threshold voltage ∼3.5 V, the on/off current ratio $>1 \times 10^7$ and the subthreshold slope 500 mV/decade. To confirm that the TFT characteristics are independent of the substrate on which they are fabricated, we also fabricated identical a-Si:H TFTs on a glass substrate at 300 °C. The transfer characteristics for TFTs fabricated on glass with the same process are also shown in Figure 5. They are almost identical to those measured for TFTs fabricated on the clear plastic, although it should be noted that the gate leakage current, I_{gs}, is slightly lower on glass. In essence, the choice of substrate does not affect TFT performance.

Now we consider the device stability for TFTs fabricated at 300 °C. The threshold voltage shifts after gate bias stressing for TFTs fabricated at 300 °C on glass and plastic substrates are plotted in Figure 6, together with results we obtained earlier for back-channel etched TFTs fabricated on plastic (150 °C, 200 °C, 250 °C) [12] and literature data obtained at 350 °C on glass [24]. These results clearly demonstrate that the a-Si:H TFT stability improves as the TFT process temperature is raised. At the stress field of 1×10^8 V/m, the voltage shift for 150 °C TFTs is 4 V. It decreases to 2 V for 250 °C and to 1.1 V for 300 °C. Clearly, increasing the process temperature is important for fabricating highly stable devices.

Finally, typical transfer characteristics for back-channel passivated a-Si:H TFTs made using the self-aligned process are shown in Figure 7. On clear plastic the linear mobility is 1.13 cm^2/Vs, the saturation mobility 0.82 cm^2/Vs, the threshold voltage 2.3 V, the on/off current ratio $>1 \times 10^7$ and the subthreshold slope 800 mV/decade. Clearly the self-aligned process results in

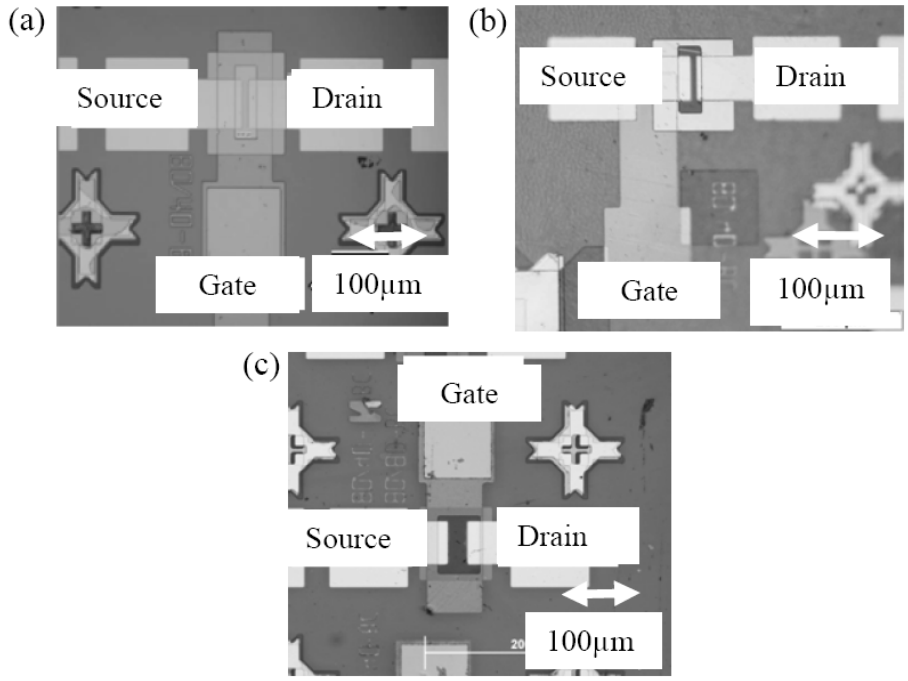

Fig. 8. Optical micrographs showing TFTs fabricated without using self-alignment (a) at the center of the substrate and (b) 5 cm away from the center. (c) Optical micrograph of a TFT 5 cm away from the center of the substrate where improved alignment is achieved by engineering the total strain in the workpiece.

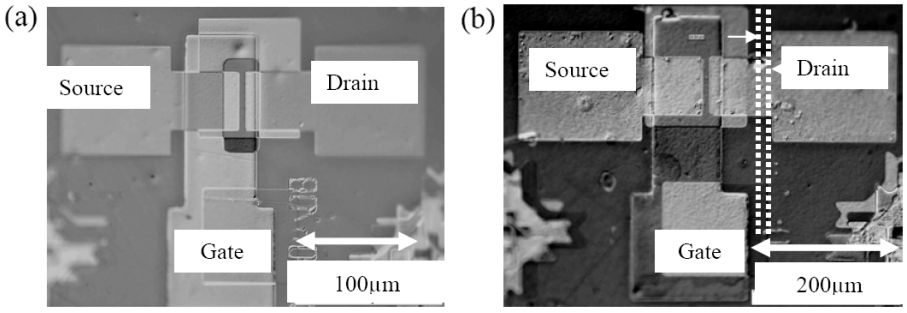

Fig. 9. Optical micrograph showing (a) a TFT patterned using standard photolithography and (b) a self-aligned TFT at a distance of 2.4 cm away from the center of the substrate along the diagonal.

high-quality TFTs with higher mobilities than the standard lithographic process. The measured threshold voltages measured from several processing runs using standard photolithography have ranged from $\sim 1 - 4$ V and we believe that the 4 V threshold voltage measured for the self-aligned process is within normal process variation.

It is not possible to achieve perfect alignment between the gate and subsequent device layers over the entire substrate area since the size of the substrate changes during the TFT stack deposition. When our TFTs are fabricated by using standard photolithography (without self-alignment) the TFT layers are aligned at the center of the substrate. Such a TFT is shown in Figure 8(a). The misalignment between device layers becomes more pronounced the further a TFT position lies from the center. We define misalignment as $\Delta \equiv 10^6 \times d/\lambda$ [ppm], where d is the local misalignment and λ is the distance from the center of the substrate to the center of the TFT. For TFTs made by using standard photolithography the misalignment between the bottom mask layer (the TFT gate) and the second mask layer (the channel passivation) is $\Delta \approx 1500$ ppm at the edge of the substrate. Such a TFT is shown in Figure 8(b) and is no longer functional.

One way to reduce the misalignment is to engineer the stress in the whole structure to minimize the strain the substrate experiences by adjusting the stresses in the individual layers. In this way we reduced the misalignment near the corner of the substrate to 300 ppm, as is shown in Figure 8(c). To completely eliminate the misalignment between the gate and the channel passivation

a self-alignment method was implemented. Figure 9(a) and Figure 9(b) both show a TFT at a distance of 2.4 cm from the center of the substrate. The same mask set and process was used for both fabrication runs, except that self-alignment was used to pattern the channel passivation for the TFT shown in Figure 9(b). Due to the misalignment between the gate and the channel passivation, the TFT shown in Figure 9(a) is not functional while the TFT in Figure 9(b) will still turn on.

III. CONCLUSIONS

Fabricating a-Si:H TFTs on clear plastic at 300 °C produces initial electrical characteristics and gate bias-stress stability comparable to TFTs made on glass. A proper combination of mechanical stresses in the substrate passivation and TFT layers produces intact devices on a flat substrate. Alignment far away from the fiduciary alignment mark at the center of the clear plastic substrate is improved by stress control and misalignment is partially eliminated by using a self-alignment method. However, since flexible displays will ultimately be fabricated using roll-to-roll fabrication on free-standing web substrates, we still require the introduction of new techniques for aligning the gate with the source/drain contact and the interconnects.

ACKNOWLEDGMENTS

We gratefully acknowledge technical collaboration with the DuPont Company and the sponsorship of this research by the United States Display Consortium. K. H. C. thanks the Princeton Plasma Physics Laboratory for a PPST Fellowship.

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