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# Titanium dioxide/silicon hole-blocking selective contact to enable double-heterojunction crystalline silicon-based solar cell

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In this work, we use an electron-selective titanium dioxide ($TiO_2$) heterojunction contact to silicon to block minority carrier holes in the silicon from recombining at the cathode contact of a silicon-based photovoltaic device. We present four pieces of evidence demonstrating the beneficial effect of adding the $TiO_2$ hole-blocking layer: reduced dark current, increased open circuit voltage ($V_{OC}$), increased quantum efficiency at longer wavelengths, and increased stored minority carrier charge under forward bias. The importance of a low rate of recombination of minority carriers at the Si/$TiO_2$ interface for effective blocking of minority carriers is quantitatively described. The anode is made of a poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) heterojunction to silicon which forms a hole selective contact, so that the entire device is made at a maximum temperature of 100 °C, with no doping gradients or junctions in the silicon. A low rate of recombination of minority carriers at the Si/$TiO_2$ interface is crucial for effective blocking of minority carriers. Such a pair of complementary carrier-selective heterojunctions offers a path towards high-efficiency silicon solar cells using relatively simple and near-room temperature fabrication techniques. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4916540]

Crystalline silicon solar cells offer high efficiencies (~25%) but are expensive to fabricate, in part due to the need to form p-n junctions at high-temperature (>800 °C) in high purity furnaces.[1–3] This work demonstrates a solar cell with crystalline silicon as the absorbing material but no conventional p-n junction or any other doping gradient in the silicon. The device instead uses two heterojunctions that form carrier selective contacts, all formed at 100 °C or less.

The energy level alignments for the Si/titanium dioxide ($TiO_2$) interface measured as part of this work (via direct and inverse photoemission spectroscopy) are shown in Figure 1(a). The Si/$TiO_2$ heterojunction has a large offset between the valence band maximums of the two materials ($\Delta E_V \geq 2.3$ eV), which provides a barrier that prevents holes in the silicon valence band from flowing to the metal cathode. However, the conduction band minimum of the $TiO_2$ is closely aligned with that of silicon ($\Delta E_C < 0.3$ eV), which allows electrons from the silicon conduction band to flow through the $TiO_2$, thus making the $TiO_2$ an electron-selective contact to silicon. The device architecture is shown in Figure 1(b). Starting with an n-type ($10^{15}$ cm$^{-3}$) float-zone (100) silicon wafer, the $TiO_2$ electron selective layer is deposited as a blanket layer on the wafer backside after conventional chemical cleaning and a dip in dilute hydrofluoric acid. The deposition process for $TiO_2$ is a low-temperature chemical vapor deposition (CVD) technique.[4] In this method, substrates are cooled via thermoelectric controller to −10 °C in a vacuum chamber and exposed to titanium tert-butoxide vapor. After 10 min to adsorb the precursor onto the substrates, the substrates are heated to 100 °C for 10 min in order to convert the precursor to $TiO_2$. This cycle is repeated 3 times for a typical $TiO_2$ deposition. This deposition is followed by thermal evaporation of 20 nm of aluminum and 200 nm of silver to form the cathode.

The complementary hole-selective contact on the front side is formed by spin-coating poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT) on the silicon after the front surface is treated with dilute hydrofluoric acid. Clevios PH1000 was used, and 10% w/w dimelthyl sulfoxide was added to enhance conductivity,[5] as was 0.25% Zonyl FS-300 to promote adhesion[6] before spin coating at room-temperature at 3700 RPM. Samples were placed into a high vacuum chamber immediately after coating to remove excess water from the PEDOT film and receive metallization. The lowest unoccupied molecular orbital (LUMO) in the PEDOT is at 3.6 eV below the vacuum level, presenting a barrier to electrons from silicon of ~0.45 eV, and the PEDOT highest unoccupied molecular orbital (HOMO) is at 4.9 eV, close to the valence band of silicon as shown in Figure 1(a) (LUMO and HOMO energy levels were also measured via direct and inverse photoemission spectroscopy in this work and agree with values previously presented in literature).[7] The high work function of the degenerately doped p-type PEDOT,[8] near the HOMO, leads to band-bending at the top silicon surface, and a rectifying device.[9–12] Cells based on the PEDOT/n-Si structure have reached up to 13.8% efficiency using organic interlayers for the back contact.[13] When coupled with a conventional, high-temperature diffused back surface field

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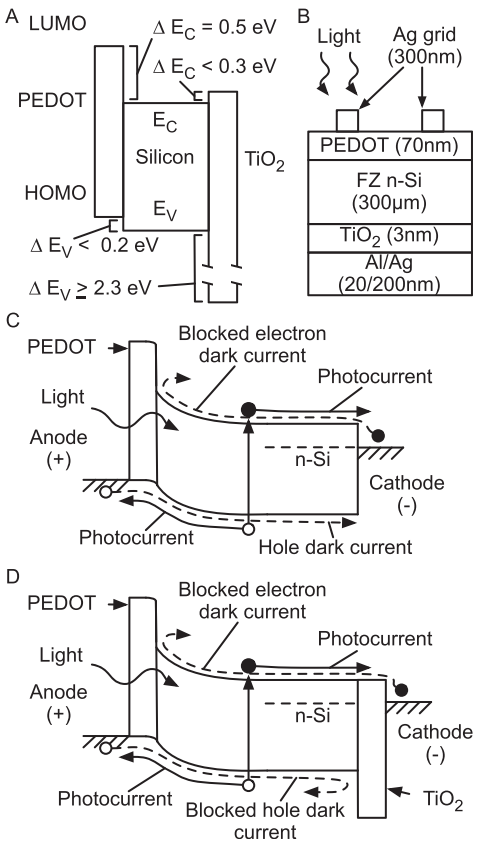



FIG. 1. Band alignments, structure, and band diagrams of heterojunction devices. (a) Band alignment at PEDOT/Si and Si/$TiO_2$ heterojunctions. (b) Cross-section of the double-heterojunction solar cell with layer thicknesses. (c) Band-diagram of single-sided PEDOT/Si device under illumination and forward bias. The filled and hollow circles represent electrons and holes, respectively. The dashed lines represent dark current. The bold lines represent photocurrent. (d) Band diagram of double-sided PEDOT/Si/$TiO_2$ heterojunction device under same conditions.

in a PEDOT/n-Si/$n^+$ structure, the efficiency of these devices has been shown to reach 17.4%.[12] In photovoltaic operation, incident light passes through a silver anode contact grid on top of the PEDOT and through the PEDOT to be absorbed in the silicon, creating excess minority carriers (holes). The electric field at the surface of the silicon collects these photo-generated minority carriers. The degenerate doping also makes the PEDOT a good conductor (300 Ω $sq^{-1}$ for 70 nm thickness), which allows the collected photocurrent to travel laterally to the top silver grid contact.

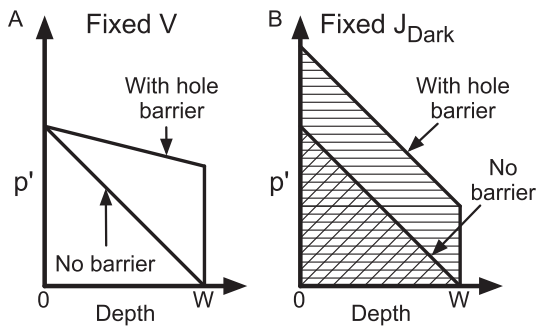


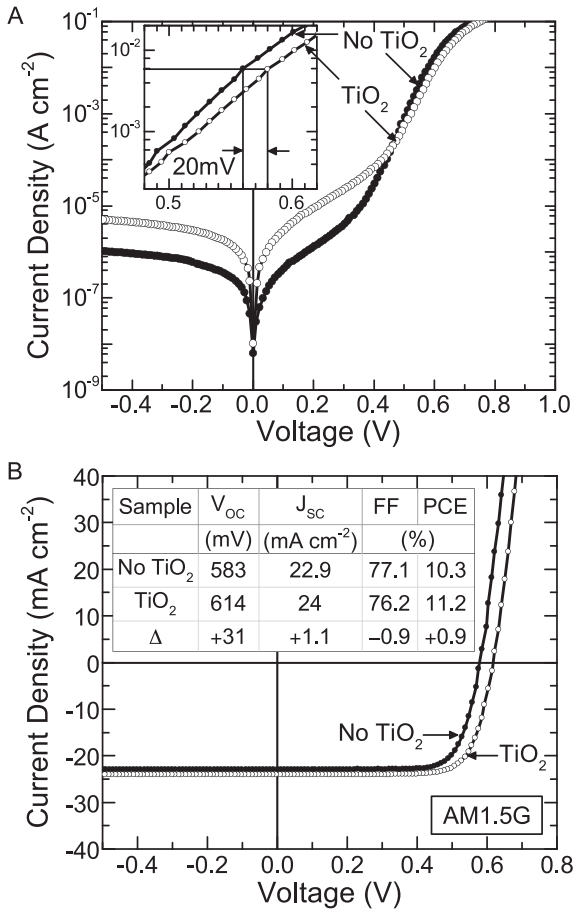

FIG. 2. Excess minority carrier hole concentration ($p'$) profile in silicon substrate under forward bias in the dark. $W$ is the wafer thickness. (a) Profile comparing devices with (Figure 1(d)) and without (Figure 1(c)) hole-barrier at cathode under fixed voltage bias. (b) Profile of same devices under fixed current bias, with crosshatching to indicate the stored charge measured by reverse recovery.

In prior work, we made similar devices, but without the hole-blocking back contact; a thermally evaporated blanket metal backside contact was used. This previous work has shown that under forward bias, the PEDOT/Si[14] (or PEDOT-P3HT/Si[15]) heterojunction blocks electrons in the n-type Si from flowing to the anode, so the majority of the dark current in the device is caused by hole injection from the PEDOT into the silicon substrate. The carrier paths within such a device are shown in the band diagram of Figure 1(c). For wafers with hole diffusion length $L_{D,p}$ in the n-type silicon greater than the thickness of the wafer $W$ (for this work $L_{D,p} > 1$ mm and $W = 0.3$ mm), the PEDOT/n-Si device is in the "narrow-base" or "short-base" condition.[16] In such a device, nearly all holes injected from the PEDOT would reach the backside metal contact and recombine there. As a result, the profile of the concentration excess of minority carriers ($p'$) as a function of depth in the wafer would have a constant slope (Figure 2(a)). The dark current carried by diffusing holes is proportional to the slope of this profile and dominates the dark current in the PEDOT/n-Si device because the PEDOT serves as a barrier to block electron dark current.

A high $V_{OC}$ requires further lowering of the dark current. In conventional $p^+$-n silicon cells, this is accomplished by a backside $n^+$ diffusion to create a "back-surface field" that prevents the holes from recombining at the metal contact. We chose to raise $V_{OC}$ by replacing the conventional backside $n^+$ diffusion process with a hole-blocking heterojunction formed by depositing a ~3 nm $TiO_2$ layer via low-temperature CVD ($TiO_2$ layer thicknesses were measured using spectroscopic ellipsometry). Previously, 8-hydroxyquinolinolato-lithium and cesium carbonate have been used as interlayers to improve the interface between silicon and aluminum cathode.[17,18] Figure 1(d) shows the paths of the blocked dark current and unimpeded photocurrent in the double-heterojunction device. The minority carrier concentration profile in a device without a hole-barrier is compared to a device with a hole-barrier in Figure 2(a), where reduction in dark current is indicated by the decrease in the slope of the hole concentration profile. While an ideal hole-barrier would reduce the dark current due to holes to zero, for reasons that will be addressed later, any physically realistic barrier provides only a finite reduction in the dark current.

This double-heterojunction structure without doping gradients in silicon is analogous to the Heterojunction with Intrinsic Thin layer (HIT) solar cell, in which amorphous silicon (a-Si) layers deposited by plasma-enhanced CVD (PECVD) form the electron and hole barriers.[19] The HIT concept has enabled record efficiencies for c-Si based solar cells (25.6%).[20] Recent work has shown that the initial growth of the a-Si heterojunction can result in epitaxial growth of a thin, heavily doped crystalline silicon layer at the interfaces, which can be difficult to control.[21] Compared to the HIT cell, our work involves no plasma processing, no interfacial silicon epitaxy, and no doping profiles in the silicon.

We now experimentally compare the double-sided heterojunction device (PEDOT/Si/$TiO_2$) to a single-sided heterojunction device (PEDOT/Si) to demonstrate the role of the




| Sample | $V_{OC}$ (mV) | $J_{SC}$ (mA cm$^{-2}$) | FF | PCE (%) |
|---|---|---|---|---|
| No $TiO_2$ | 583 | 22.9 | 77.1 | 10.3 |
| $TiO_2$ | 614 | 24 | 76.2 | 11.2 |
| Δ | +31 | +1.1 | –0.9 | +0.9 |

FIG. 3. Effect of hole-blocking $TiO_2$ on current-voltage characteristics. The areas of the two devices are 0.16 cm$^2$, with approximately 16% metal grid coverage. (a) Current-voltage characteristics in the dark of single-sided PEDOT/Si and double-sided PEDOT/Si/$TiO_2$ devices. Inset: Ideal exponential region ($n \approx 1$). (b) Current-voltage characteristics of same devices under AM1.5 illumination. Inset table summarizes solar cell parameters.

$TiO_2$. No AR coating on top of the PEDOT was used. The current density-voltage (J-V) characteristics (Figure 3(a)), measured using Agilent/Hewlett-Packard 4155c parameter analyzer, show that the dark current in the double-sided device is reduced substantially compared to the single-sided one. The ideal exponential portion ($n \approx 1$) of the J-V characteristics in forward bias is shown in the inset of Figure 3(a). For a fixed bias voltage, the hole-blocking layer causes a 1.8-fold reduction in dark current. Equivalently, to reach the same current, a 20 mV greater bias voltage is required for the double-sided heterojunction device. The J-V characteristics under AM1.5G illumination are shown in Figure 3(b). Inset in Figure 3(b) is a table showing the $V_{OC}$, short circuit current ($J_{SC}$), fill factor (*FF*), and power conversion efficiency (*PCE*) for the devices with $TiO_2$ and without $TiO_2$. Both $J_{SC}$ and *PCE* are calculated using total device area, including the metallized grid. AM1.5G measurements were made using an OAI systems AAA Tri-sol solar simulator equipped with a 4 mm × 4 mm aperture; the solar simulator output was measured using a silicon reference cell (PV Measurements, Inc.) that was calibrated using Newport Corporation's PV Cell Lab. The double-sided device with a $TiO_2$ hole-blocking layer exhibits improvement over the single-sided device of up to 31 mV in $V_{OC}$ and 1.1 mA cm$^{-2}$ in short circuit current

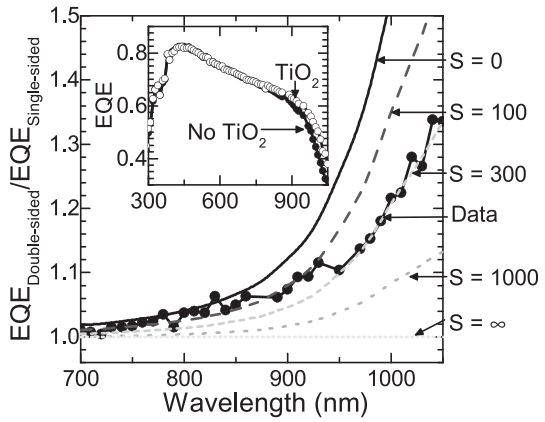



FIG. 4. EQE of a double-sided device normalized to a single-sided device, compared to modeled normalized EQE with different values of S at Si/$TiO_2$ interface. Inset: Full EQE spectra of devices with $TiO_2$ and without $TiO_2$.

($J_{SC}$). The increase in $V_{OC}$ is readily explained by the measured reduction in dark current, and the increase in $J_{SC}$ is explained by quantum efficiency measurements described subsequently. That $V_{OC}$ closely matched that expected from the dark I-V curves, and that the $V_{OC}$ improvement due to the $TiO_2$ was similar to the dark J-V shift confirm the role of the $TiO_2$ layer as a hole blocker and that the $V_{OC}$ of the control device was not artificially suppressed by an electron barrier at the back interface in the control device due to $p^+$ doping from the Al.[22]

The external quantum efficiency (EQE) spectra for a single-sided device and double-sided device also demonstrate the ability of the $TiO_2$ to reduce hole recombination at the back interface. The EQE of the double-sided device is shown normalized to the EQE of the single-sided device in Figure 4 ($EQE_{double\text{-}sided}/EQE_{single\text{-}sided}$), and the full EQE spectra is shown in the inset. EQE measurements were made using an Oriel tunable light source system. At $\lambda > 800$ nm, the EQE of the double-sided device is higher than that of the single-sided device, with the relative increase increasing with wavelength; Figure 4 presents the normalized EQE to highlight this effect. Long wavelength photons are more probable to be absorbed near the back of the wafer than short wavelengths, and the holes generated by these photons are therefore subject to recombination at the Si/cathode interface without a blocking layer. Thus, the increase in EQE for

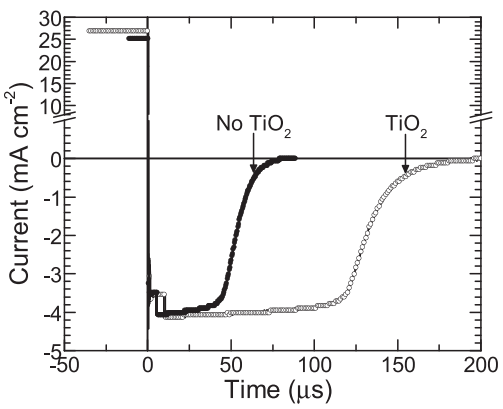



FIG. 5. Current vs. time oscilloscope waveform from reverse recovery measurement, comparing single-sided and double-sided devices.

$\lambda > 800$ nm is expected because the $TiO_2$ hole-blocker prevents photogenerated holes from recombining at the cathode and therefore holes generated deep in the silicon have a greater probability of being collected at the anode and contributing to photocurrent. Multiplying the EQE increase with the AM1.5G spectral irradiance at each wavelength and the electronic charge, dividing by the energy at each wavelength, and integrating over all wavelengths yields an increase in $J_{SC}$ of 1.1 mA, in exact agreement with the observed increase in photocurrent measured in Figure 3(b).

The effectiveness of the $TiO_2$ hole-blocking layer can also be determined by measuring the stored minority hole charge $Q_{Stored}$ in the neutral n-type silicon of the device under forward bias. For the same current in forward bias and thus the same slope of the hole concentration profile, the double-sided device will contain a greater $Q_{Stored}$ as indicated by the crosshatched area in Figure 2(b). We used the reverse recovery method,[23–26] in which a device is switched rapidly from forward bias at a fixed current to reverse bias with another fixed reverse current, $I_{Rev}$, to estimate $Q_{Stored}$. The reverse current is due to the holes leaving the silicon back to the PEDOT and will continue to flow up to a time $t_{Storage}$, at which point the holes are nearly all removed and $I_{Rev}$ begins to fall. $Q_{Stored}$ is approximated by the product of $I_{Rev}$ and $t_{Storage}$. Figure 5 shows $I_{Rev}$ as a function of time for a single-sided and a double-sided device. The double- sided device maintains a flow of $I_{Rev}$ for a three-fold longer $t_{Storage}$ and therefore contains approximately a three-fold greater initial $Q_{Stored}$ compared to the single-sided device without $TiO_2$.

The $TiO_2$ barrier is not perfect; minority carrier holes may recombine at the $Si/TiO_2$ interface through states in the Si bandgap due to dangling Si bonds, for example. This leads to a finite hole current that decreases the efficacy of the barrier; experimentally, this is observed by the dark current decreasing by only a factor of ~2 for fixed forward bias when the $TiO_2$ barrier is introduced. Recombination kinetics at Si interfaces are typically quantified by the parameter $S$, known as the surface recombination velocity. The current density from holes that recombine at the $Si/TiO_2$ interface, $J_{p,Si/TiO2}$, can be determined using Eq. (1), in which $q$ is the elementary charge and $p'(W)$ is the excess hole density at the $Si/TiO_2$ interface

$$J_{p,Si/TiO2} = qSp'(W). \tag{1}$$

The hole current density across the silicon, $J_{p,Si}$, depends on the hole concentration gradient across the wafer as shown in Eq. (2), where $D_p$ is the hole diffusion coefficient, $W$ is the thickness of the wafer, and $p'(0)$ is the excess hole density at the front (PEDOT) side of the silicon, at the edge of the quasi-neutral region

$$J_{p,Si} = \frac{qD_p}{W}\left[p'(0) - p'(W)\right]. \tag{2}$$

Because of current continuity at the $Si/TiO_2$ interface, $J_{p,Si/TiO2}$ and $J_{p,Si}$ must both be equal, and they equivalently describe the total hole dark current, $J_{p,Dark}$. Rearranging Eq. (1) for $p'(W)$ and substituting this into Eq. (2) results in Eq. (3); the term $J_{p,Dark,S.B.}$ on the right side of Eq. (3) is the classic short-base current (with all holes recombining when they reach at the metal cathode) and the term $[1 + D_p/WS]^{-1}$ represents the dark current reduction factor due to the hole-blocking layer.

$$J_{p,Dark} = \frac{qD_p}{W}p'(0)\left[\frac{1}{1+\frac{D_p}{WS}}\right] = J_{p,Dark,S.B.}\left[\frac{1}{1+\frac{D_p}{WS}}\right]. \tag{3}$$

The measured dark current of the double-sided device is reduced by a factor of 1.8 compared to the single-sided heterojunction device with the $TiO_2$ layer; using $D_p = 10\,cm^2\,s^{-1}$ and $W = 300\,\mu m$, we estimate $S$ to be $\sim 400\,cm\cdot s^{-1}$. The increase in the normalized EQE (Figure 4(a)) can also be related to the recombination velocity, $S$, at the $Si/TiO_2$ interface. Using the optical absorption dependence on wavelength of silicon and a simple carrier diffusion model, normalized EQE spectra for various $S$ values are shown in Figure 4(b). An $S$ value of $\sim 300\,cm\cdot s^{-1}$ fits the experimental curve. For comparison, an unpassivated Si surface can have an $S$ of $10^6\,cm\cdot s^{-1}$, and a high quality $Si/SiO_2$ interface formed at 1000 °C can have an $S$ of 10–30 $cm\cdot s^{-1}$.

In summary, we have demonstrated a silicon-based double-sided heterojunction solar cell utilizing non-silicon barrier materials; an organic semiconductor forms the electron barrier and a metal-oxide forms the hole-barrier, both of which are deposited at ≤100 °C. Compared to a device with only a PEDOT electron-barrier, the beneficial effect of adding a $TiO_2$ hole-barrier is shown by four pieces of evidence; a dark current decrease, an increase of $V_{OC}$ under AM1.5 illumination, an increased EQE towards longer wavelengths, and increased $Q_{Stored}$. Such complementary carrier-selective heterojunctions offer an opportunity to prepare high-efficiency silicon solar cells using relatively simple and near room-temperature fabrication techniques.

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