Amorphous-silicon thin-film transistors made at 280°C on clear-plastic substrates by interfacial stress engineering

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Abstract — A process temperature of ~300°C produces amorphous-silicon (a-Si) thin-film transistors (TFTs) with the best performance and long-term stability. Clear organic polymers (plastics) are the most versatile substrate materials for flexible displays. However, clear plastics with a glass-transition temperature (T_g) in excess of 300°C can have coefficients of thermal expansion (CTE) much larger than that of the silicon nitride (SiN_x) and a-Si in TFTs deposited by plasma-enhanced chemical vapor deposition (PECVD). The difference in the CTE that may lead to cracking of the device films can limit the process temperature to well below that of the T_g of the plastic. A model of the mechanical interaction of the TFT stack and the plastic substrate, which provides design guidelines for avoid cracking during TFT fabrication, is presented. The fracture point is determined by a critical interfacial stress. The model was used to successfully fabricate a-Si TFTs on novel clear-plastic substrates with a maximum process temperature of up to 280°C. The TFTs made at high temperatures have higher mobility, lower leakage current, and higher stability than TFTs made on conventional low-T_g clear-plastic substrates.

Keywords — *Thin-film transistors, amorphous silicon, flexible, plastic substrate, thermal stress.*

1 Introduction

Amorphous-silicon (a-Si) thin-film transistors (TFTs) on plastic substrates are attractive for driving flexible displays because they provide thin, light-weight, rugged, rollable, and foldable backplanes. The plastic substrates for the TFT backplane must be optically clear for active-matrix liquid-crystal displays (AMLCDs) and for bottom-emitting active-matrix organic light-emitting diode (AMOLEDs) displays that require the light to pass through the substrates.

In the AMLCD industry, a-Si TFTs are fabricated on glass at a maximum plasma-enhanced chemical vapor deposition (PECVD) process temperature of 300–350°C. This high temperature results in the best a-Si TFT performance; in particular, because ~350°C is required for obtaining a silicon nitride (SiN_x) gate insulator of high quality and good TFT reliability.[1] High-temperature plastics, such as the polyimide Kapton® E, have glass-transition temperatures T_g of ~350°C and have been used for TFT fabrication at process temperatures of 150–250°C.[2–4] However, Kapton is not optically clear. The optical transmission of a 50-µm-thick Kapton 200E substrate cuts off at a wavelength of about 500 nm (Fig. 1), which gives it an orange–brown color.

The properties of the clear-plastic substrates available to date have restricted the a-Si TFT fabrication process to temperatures below 140°C, since most clear plastics have a glass-transition temperature (T_g) of 120°C or less.[5–7] A widely used clear-plastic substrate is poly (ethylene terephthalate) (PET).[8] Its glass-transition temperature (T_g) of 70–110°C is too low for fabricating high-quality a-Si:H TFT's (Table 1). Another popular clear-plastic substrate is poly(ethylene naphthalate) (PEN). It has a T_g of 120°C. We have fabricated a-Si TFTs on it at a maximum process tem-

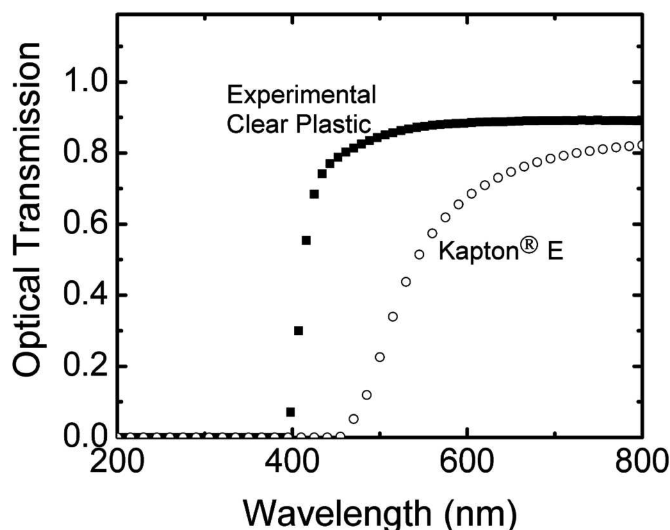

FIGURE 1 — Optical transmission spectra of a 50-µm-thick foil of Kapton® 200E and of a 75-µm-thick clear-plastic foil.

TABLE 1 — Clear-plastic substrates for TFT fabrication. Optical transmission at 700 nm, glass-transition temperature, coefficient of thermal expansion, and maximum a-Si TFT fabrication temperatures are listed. Substrate A and B were used in this work.

Substrate	Optical transmission (λ = 700 nm)/thickness	T_g (°C)	CTE (10^{-6}/°C)	Max. process temperature (°C)
Polyethylene Terephthalate (PET)	88%/125 µm	70–110	15	<120[14]
Poly(ethylene naphthalate) (PEN)	82%/125 µm	120	13	130[15]
Poly-Carbonate	90%/125 µm	130	60–70	120[16]
Experimental clear plastic substrate A	90%/100 µm	326	45	180 (this work)
Experimental clear plastic substrate B	85%/100 µm	315	≤10	Up to 280 (this work)

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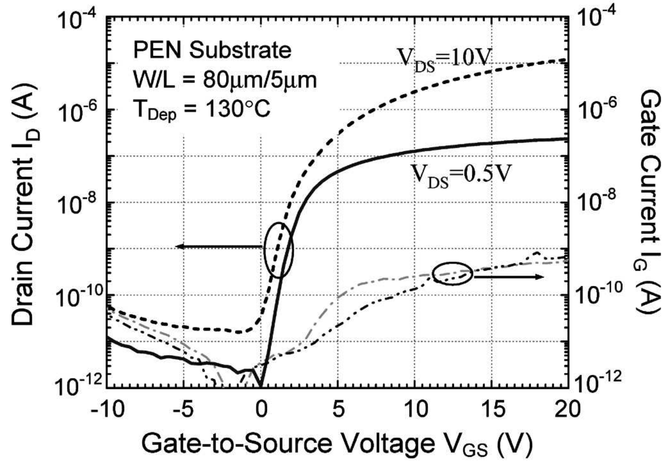


FIGURE 2 — Transfer characteristics of a TFT fabricated at 130°C on PEN.

perature of 130°C (Fig. 2). However, their electron mobility is only 0.3 cm^2/V-sec, in contrast to ~0.8 cm^2/V-sec for the TFTs fabricated at 150°C on Kapton E,[3] which demonstrates the loss in device quality as the process temperature is reduced. In addition, the TFTs on PEN have high source-to-gate leakage current (up to 200 pA/μm). A low mobility may lead to low refresh rate and low brightness of the displays. More critically, a high leakage current would produce flicker over a display frame time. The TFT results are consistent with earlier results that showed that TFTs deposited at temperatures below 140°C have low electron mobility, high leakage current, and show pronounced drift in the transfer characteristics due to charge trapping.[5,7]

Thus clear-plastic substrates with a glass-transition temperature (T_g) in excess of 300°C are desired to allow process temperatures close to those used on glass substrates. However, clear plastics with a high T_g typically have a coefficient of thermal expansion (CTE) far larger than that of the silicon nitride and a-Si layers used in the TFTs. This difference easily cracks the device films and may limit the process temperature to well below the T_g of the plastic. To avoid cracking, we modeled the mechanical interaction of the TFT stack and the plastic substrate to develop mechanical design guidelines. This model was then used to successfully fabricate a-Si TFTs on clear experimental-plastic substrates at process temperatures up to 280°C. The TFTs made at high temperatures exhibit higher mobility, lower leakage current, and higher stability than TFTs made on conventional low-T_g clear-plastic substrates.

Section 2 describes the engineering of the strain which is developed at the interface between a plastic substrate (high CTE and low Young's modulus) and a device layer (low CTE and high Young's modulus). The fracture limit of the structure is experimentally quantified and design guidelines for the fabrication of crack-free TFT are developed. Section 3 then describes the properties of such TFTs fabricated on clear substrates at maximum process temperatures of 180°C (on a plastic substrate with relatively high CTE) and at 250–280°C (on a plastic substrate with a low CTE).

2 Mechanical behavior of device films on plastic substrates

To obtain crack-free device films, the SiN_x-on-plastic structure was studied in order to develop design guidelines to avoid cracking. SiN_x was chosen because in our typical process on plastic, a relatively thick nitride layer (~0.5 μm) is deposited on both sides of the substrate to seal it against chemical attack during processing. As a first-order approximation, we assume the entire TFT stack [SiN_x, a-Si, Cr (Fig. 8)] is SiN_x for mechanical modeling, since at least half of the total thickness (including the buffer) is SiN_x.

2.1 Mechanical behavior of film-on-substrate structures

A film-on-substrate structure has a mismatch strain in the device films after they were deposited at high temperature and then cooled down to room temperature. The total mismatch strain ε_M can be described by the following equation:

$$\varepsilon_M = \varepsilon_0 + \varepsilon_{th} + \varepsilon_{ch}, \qquad (1)$$

where ε_0 is the built-in strain, ε_{th} is the thermal mismatch strain, and ε_{ch} is the moisture mismatch strain.

The built-in strain ε_0 is produced by built-in stress, which arises from atoms deposited in out-of-equilibrium positions. It is a function of the material system and the deposition conditions. The built-in stress tends to be tensile in chromium (Cr) and compressive in a-Si, and can be varied from tensile to compressive in SiN_x by increasing the PECVD deposition power.[9]

The thermal mismatch strain ε_{th} is introduced by the CTE mismatch between the film and the substrate. During a-Si TFT fabrication, the films are typically deposited at elevated temperature. The thermal mismatch strain produced by cooling down to room temperature is given by

$$\varepsilon_{th} = \Delta\text{CTE} \times \Delta T, \qquad (2)$$

where $\Delta\text{CTE} = \text{CTE}_{substrate} - \text{CTE}_{device\ film}$ is the CTE difference between the substrate and the device film, ΔT is the process temperature excursion (defined >0).

The moisture mismatch strain ε_{ch} is observed in films deposited on plastic substrates after vacuum bake and brought into moist air after deposition. It is described by

$$\varepsilon_{ch} = \Delta\text{CHE} \times \%\text{RH}, \qquad (3)$$

where ΔCHE is the difference in coefficient of humidity expansion (CHE) and %RH is the percent of relative humidity.

In our experiments, the plastic substrate was coated on each side with a layer of SiN_x buffer, which acts as a very good moisture barrier. Therefore, we assume that the moisture mismatch strain ε_{ch} in our experiments is zero and con-

sider only the built-in strain ε_0 and thermal mismatch strain ε_{th}:

$$\varepsilon_M = \varepsilon_0 + \varepsilon_{th} = \varepsilon_0 + \Delta\text{CTE} \times \Delta T. \tag{4}$$

When a film is deposited on a compliant substrate, deformation occurs in both the film and the substrate. During deposition, our substrates are free-standing and not rigidly bonded to a glass or wafer carrier. Bonding limits the lateral thermal expansion, but removal of the bonding agent after processing without damaging the optically clear property of the back of the plastic is very challenging. In our work, during PECVD deposition, the substrate is held in a frame, so that the substrate is constrained to be flat, although it can expand and contract laterally. Under this flat condition, the stress in the film after returning to room temperature is given by Ref. 3

$$\sigma_f = \frac{\varepsilon_M Y_f^*}{1 + \left(Y_f^* d_f\right) / \left(Y_f^* d_s\right)}. \tag{5}$$

where $Y_f^* = Y_f/(1 - \nu_f)$ is the biaxial elastic modulus of the film, with Y_f being Young's modulus and ν_f Poisson's ratio. Y_s^* is the biaxial elastic modulus of the substrate, d_f is the film thickness, and d_s is the substrate thickness. The stress in the substrate is given by

$$\sigma_s = -\sigma_f d_f / d_s. \tag{6}$$

In most cases, $d_s > d_f$, so the stress in the substrate is quite small compared to the stress in the film.

After deposition of the film, if the structure is released from the frame, the substrate bends into a roll.[10] Elementary beam theory can be used to model the structure as a bimetallic strip. The radius of curvature is given by Ref. 2

$$R = \frac{\left(Y_s' d_s^2 - Y_f' d_f^2\right)^2 + 4 Y_f' Y_s' d_f d_s \left(d_f + d_s\right)^2}{6 \varepsilon_M Y_f' Y_s' d_f d_s \left(d_f + d_s\right)}. \tag{7}$$

Here, $Y' = Y/(1 - \nu^2)$ is the plane-strain elastic modulus. If the bare substrate is stress free, this radius of curvature can be used to quantify the strain levels in the films.[11]

If the inorganic device films are under tensile strain, the films fail by crack propagation from pre-existing defects. Under compressive strain, device films fail by delamination from the substrate coupled with buckling and fracture. The films may crack during or after deposition. The main strain component during deposition is built-in strain, and both built-in strain and thermal mismatch strain make up the total strain after deposition. Once the substrate and the process temperature have been selected, the thermal mismatch strain is fixed. The total mismatch strain can be reduced by controlling the built-in strain, *i.e.*, by adjusting the deposition conditions of the device films. Typical brittle inorganic films for a-Si TFTs can be strained more in compression than in tension.[12] Good adhesion between the device films and the substrate can suppress the compressive strain failure, since we will show in the next section that interfacial effects appear to control the onset of failure.

2.2 Effect of deposition conditions on built-in strain

Our goal was to fabricate a-Si TFTs at a temperature as high as possible on two new types of clear-plastic substrates, substrate A and substrate B, each with T_g > 315°C (Table 1). They are transparent down to λ = 400 nm. The optical transmission spectrum of substrate A is shown in Fig. 1. Substrate A is more transparent at λ = 700 nm than substrate B (90% *vs.* 85%), but it also has a much higher CTE (45 ppm/°C) than substrate B (<10 ppm/°C) (see Table 1).

SiN_x films of various thicknesses were deposited on clear-plastic substrates A or B under different deposition conditions. The SiN_x was deposited in a multi-chamber rf-powered PECVD system with electrode area of 6 × 6 in. in a triode configuration. The typical deposition pressure is 500 mTorr, and the source gases are SiH_4 for a-Si, NH_3 and SiH_4 for SiN_x, with H_2 dilution for depositions at temperatures below 200°C.

The total strain in the device films can be reduced by choosing the appropriate deposition condition and by employing the built-in strain to compensate for the thermal mismatch strain. Because the CTE of substrate A (45 ppm/°C) is much higher than that of the SiN_x film (2.7 ppm/°C) (Table 2), the thermal strain in the SiN_x film is compressive when the SiN_x is cooled down to room temperature from the elevated deposition temperature. Therefore, we want the built-in strain of the SiN_x film to be tensile to compensate for the thermal mismatch strain.

The built-in strain in the SiN_x can be controlled by adjusting the rf power during the PECVD process. To measure the built-in strain ε_0 of SiN_x films *vs.* rf power, SiN_x films were deposited on one side of 50-μm-thick Kapton 200E substrates. The substrates were held in a frame during the nitride-film deposition to keep it flat. After the deposition, the samples were cooled down to room temperature in the frame. When they were released after the cooling, the samples bent into a roll because of the mismatch strain. Equation (7) allows the calculation of the total mismatch strain ε_M in the nitride film from the radius of curvature.

TABLE 2 — Mechanical properties of the new clear plastic substrates and the device films. The properties of SiN_x, a-Si, and chromium are from Ref. 11.

		Clear Plastic A	Clear Plastic B	SiN_x	i a-Si	n^+ a-Si	Cr
Thickness (μm)	t	60-100	60-100	0.3	0.2	0.05	0.1
Coeff. thermal exp. (10^{-6}/K)	α	45	≤10	2.7	3 (2.2 - 4.5)		3 (1-5)
Young's modulus (GPa)	Y	2.9	2.9	210	170		140
Poisson's ratio	ν	0.34	0.34	0.25	0.22		0.21
Biaxial modulus* (GPa)	Y*	4.4	4.4	280	218		180
Plane strain modulus** (GPa)	Y'	3.3	3.3	224	180		146
Built-in stress in film (GPa)	σ_{BI}	--	--	Power dependent	Compressive –0.16		Tensile 0.54

*Biaxial modulus: $Y^* = Y/(1 - \nu)$.
** Plane strain modulus: $Y' = Y/(1-\nu^2)$.

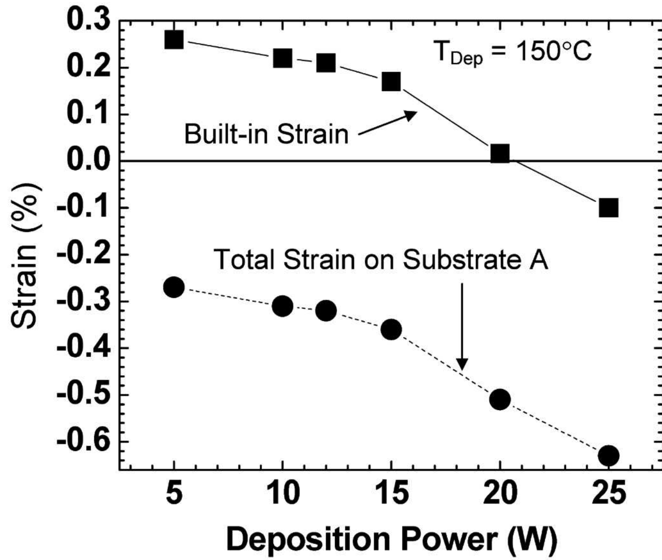


FIGURE 3 — Built-in strain (squares) and total strain (circles) of SiN_x films deposited on substrate A at 150°C by PECVD over a range of rf power.

Then we can calculate the built-in strain ε_0 in the SiN_x film from Eq. (4). For SiN_x films deposited at 150°C, the built-in strain changes from tensile to compressive as the deposition power increases (Fig. 3), from 0.26% at 5-W deposition power to –0.1% at 25-W deposition power. Tensile strain in the film is defined as positive. The crossover point lies at about 21 W (90 mW/cm^2).[11] At a deposition power below 5 W, the SiN_x does not adhere well to the plastic substrate and may detach from the substrate during deposition. Thus, a deposition power of 5 W produces the most tensile built-in strain we can obtain in SiN_x. This power was used for all later device work unless stated otherwise.

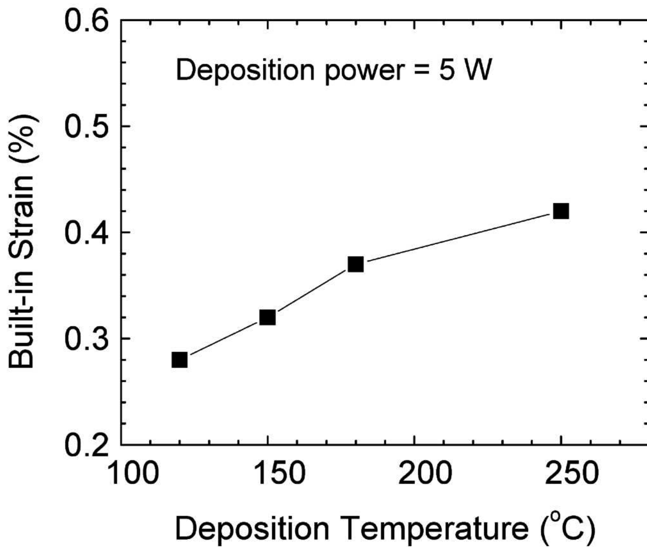


FIGURE 4 — Built-in strain of SiN_x films deposited over a range of temperatures at 5-W RF power.

We then deposited SiN_x on substrate A (75 μm thick) at a temperatures of 120, 150, 180, and 250°C, respectively, with the deposition power fixed at 5 W. Again, the built-in strain in the nitride films was calculated from Eqs. (7) and (4). The built-in strain increases slightly with rising deposition temperature, from 0.28% at 120°C to 0.42% at 250°C (Fig. 4). The built-in strain of SiN_x deposited at 150°C on clear plastic substrate A is calculated to be slightly higher than that on Kapton 200E (0.32% *vs.* 0.26%). This difference may be due to uncertainties in the thickness, elastic modulus, or CTE between the two substrates.

For SiN_x on substrate A, $\Delta CTE = (45–2.7) \times 10^{-6}/°C = 42.3 \times 10^{-6}/°C$. From Eq. (4) and Fig. 3, one finds that even the most tensile built-in strain of SiN_x, deposited at an rf power of 5 W, for any deposition temperatures above 100°C, will leave the SiN_x film in compression after cooling to room temperature. The deposition power of 5 W will result in the lowest total strain, however.

2.3 Film fracture and critical interfacial force

At all PECVD temperatures (120, 150, 180, and 250°C), the SiN_x films still cracked above a certain thickness. Figure 5(a) shows the film thickness *vs.* deposition temperature. The filled symbols represent crack-free films, and the open symbols represent cracked films. The maximum crack-free nitride-film thickness decreases as the temperature increases. When the temperature increased to 250°C, only a 200-nm-thick SiN_x film could be deposited without cracking. Since the strain in the nitride is essentially independent of thickness, these experiments show that the critical factor leading to the film failure and thus limiting the TFT fabrication is not a fixed strain level in the film.

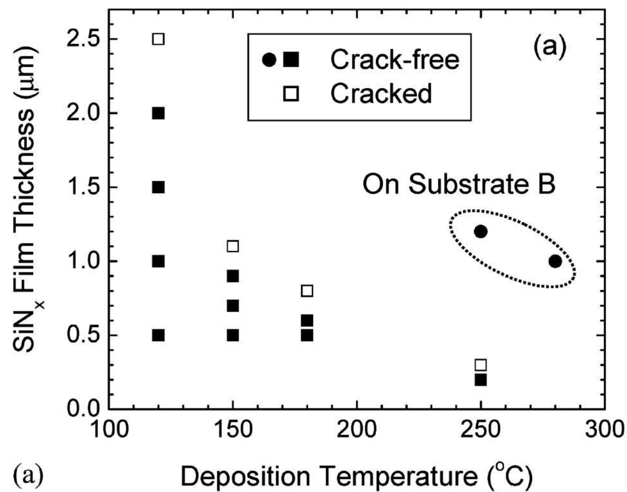
Any stress in the device film must be supported by an interfacial force between the device films and the substrate. From Eq. (5), the interfacial force per unit width is

$$\frac{F}{L} = \sigma_f \cdot d_f = \frac{\varepsilon_M Y_f^* d_f}{1+\left(Y_f^* d_f\right)/\left(Y_s^* d_s\right)}, \tag{8}$$

where $\varepsilon_M = \varepsilon_0 + \varepsilon_{th} = \varepsilon_0 + \Delta CTE \times \Delta T$.

This interfacial force increases as the film thickness increases. We then re-plotted the data of Fig. 5(a) with the interfacial force required to support all the stress in the device film as the ordinate [Fig. 5(b)]. From the data, it is clear that the critical condition for the onset of mechanical failure is a critical interfacial force, which is independent of temperature. This critical interfacial force is ~–300 N/m (the minus sign represents compressive stress). SiN_x films with higher interfacial force cracked, while SiN_x films with lower interfacial force could be deposited without cracking.

Assuming the existence of a critical interfacial force in the SiN_x-on-plastic system, we can now engineer structures to remain below this critical force. Equation (8) indicates that decreasing the substrate thickness can raise the maxi-



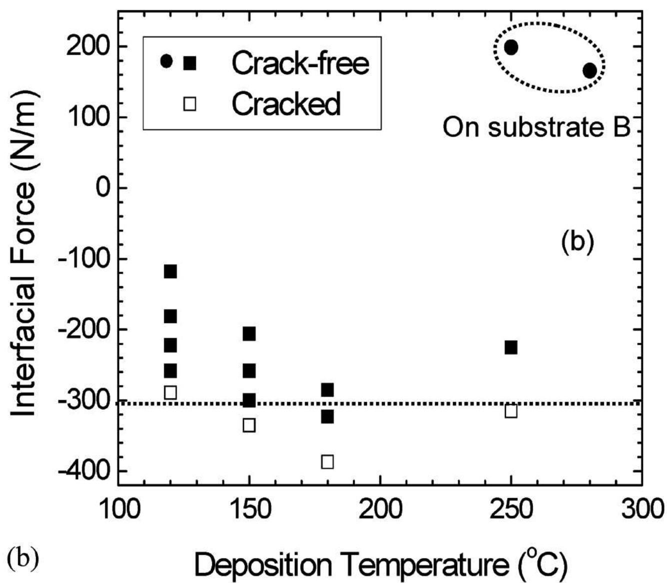
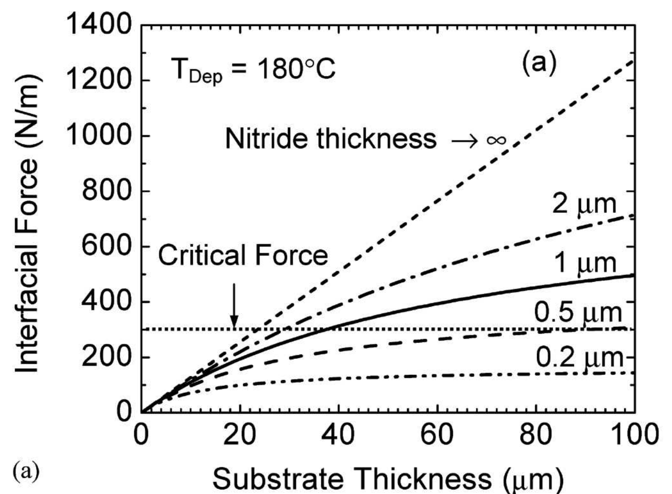


FIGURE 5 — (a) Thickness and (b) interfacial force of cracked (open symbols) and crack-free (close symbols) SiN_x films deposited over a range of temperatures. The two films on substrate B (with low CTE) are labeled separately.



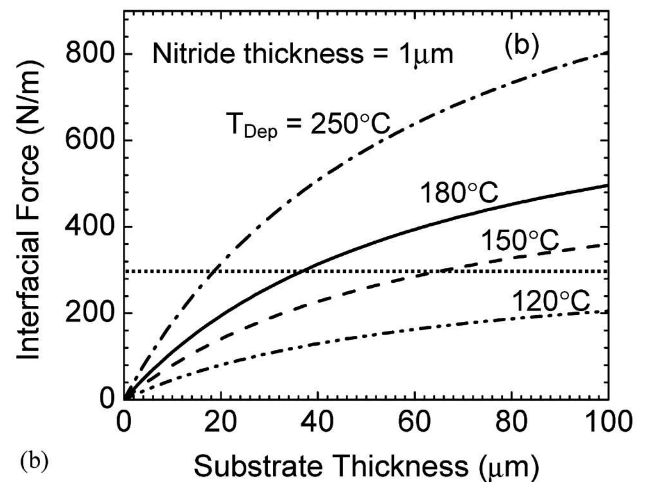


FIGURE 6 — Calculated interfacial force as a function of substrate thickness for SiN_x-on-plastic substrate A (high CTE). (a) SiN_x with a range of thicknesses deposited at 180°C; (b) 1-μm-thick SiN_x deposited over a range of temperatures.

mum film thickness allowed for a fixed critical interfacial force. When the nitride (or TFT stack) is made thicker, it forces the substrate to comply more with the nitride, which in turn lowers the interfacial force. Thin substrates and those with low Young's modulus comply more easily than thick and stiff substrates. For SiN_x of the present series of experiments deposited at 180°C with 5-W rf power on substrate A with CTE = 45 ppm/°C and Young's modulus = 2.9 GPa, the interfacial force is shown as a function of substrate thickness in Fig. 6(a) for a range of nitride thicknesses. For a nitride thickness of 0.2 and 0.5 μm, the predicted interfacial force will not exceed the critical value on any substrate up to a thickness of 100 μm. However, for a 1-μm-thick nitride, the substrate must be thinner than 40 μm to keep the interfacial force below the cracking point.

Because the deposition temperature determines the differential thermal contraction, it also affects the interfacial force. For a nitride layer of 1-μm thickness, Fig. 6(b) shows the interfacial force *vs.* substrate A thickness, with deposition temperatures ranging over 120, 150, 180, and 250°C. With a 120°C process, 1 μm of nitride can be deposited without cracking for a substrate thickness up to 100 μm. The maximum substrate thickness decreases to 70 μm when process temperature is raised to 150°C. For the even higher temperature of 250°C, the substrate thickness must be less than 20 μm, which may be too thin for practical use as a free-standing substrate. Given the results shown in Fig. 6(b), we fabricated TFT's on 75-μm-thick substrate A at 180°C, as will be described in a later section.

With a CTE less than 10 ppm/°C, substrate B is a better candidate to achieve 1-μm crack-free device layers at a deposition temperature of 250°C than substrate A (CTE = 45 ppm/°C). To test this conclusion, we deposited SiN_x films on substrate B at 250 and 280°C, also with an rf power of 5 W. Crack-free 1.2- and 1-μm-thick SiN_x films were deposited on substrate B at 250 and 280°C, respectively [Fig. 5(a)]. The calculated interfacial force in these two films is

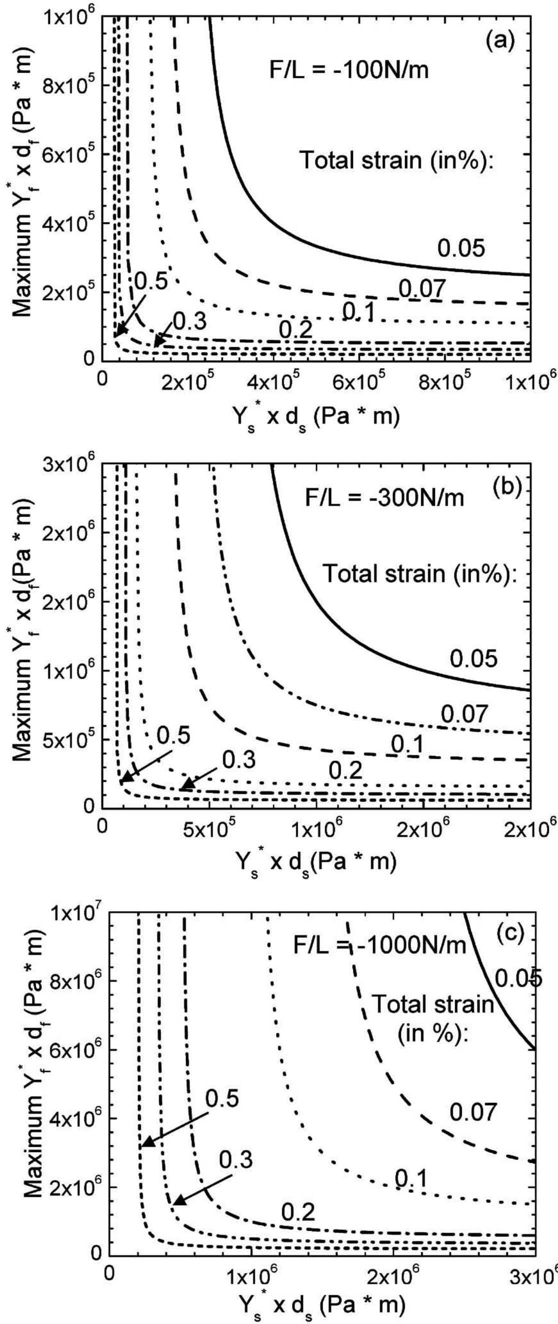


FIGURE 7 — Calculated maximum allowed products of device layer thickness times its Young's modulus ($d_f \cdot Y_f$*) *vs.* the substrate thickness times its Young's modulus ($d_s \cdot Y_s$*), for a range of values of the total strain level in the film. The critical interfacial force is assumed to be (a) –100 N/m; (b) –300 N/m; (c) –1000 N/m.

also plotted in Fig. 5(b). The total stress in these SiN_x films is tensile, with absolute values much smaller than those of SiN_x films deposited on substrate A.

The guideline of Figs. 6(a) and 6(b) apply only to the substrates, device film (nitride), and parameters we used. A more generally useful relationship can be realized by plotting the maximum allowed product of the layer thickness times its biaxial Young's modulus ($d_f \cdot Y_f$*) *vs.* the product of the substrate thickness times its biaxial Young's modulus ($d_s \cdot Y_s$*), for different values of the total mismatch strain between the film and the substrate. From Eq. (8), one finds

$$Y_f^* \cdot d_f = \frac{F/L}{\varepsilon_M - (F/L)\big/\left(Y_s^* d_s\right)}, \tag{9}$$

where the total strain ε_M is calculated from Eq. (4). Such relationships are shown in Figs. 7(a)–7(c) for a critical interfacial force of –100, –300, and –1000 N/m, respectively. In each case, the allowable film thickness decreases as the film becomes stiffer, or as the substrate thickness and/or stiffness increases. Note that for a suitably thin/soft substrate (denoted by a small $Y_s{}^* \cdot d_s$), there is no limit to the device film thickness. This maximum $Y_s{}^* \cdot d_s$ product increases as the allowed interfacial force increases:

$$Y_s{}^* \cdot d_s = (F/L)/\varepsilon_M. \tag{10}$$

3 Fabrication of amorphous-silicon thin-film transistors at high temperatures on clear-plastic substrates

Figure 8 shows the cross-section of the TFT structure made on plastic substrates A and B. A thick silicon-nitride (SiN_x) buffer layer on each side of the substrate planarizes the substrate, passivates it against process chemicals and moisture, and makes the device layers adhere to the organic polymer. The TFT structure is the standard inverted-staggered structure with a bottom gate and top source/drain contacts. The TFT channel is defined by back channel etch. In contrast to previous work with high-temperature plastic substrates that were mounted to rigid carriers for TFT fabrication,[4] we kept our substrates free-standing to keep the back surface optically clean and clear. During PECVD deposition, the substrates were held in a frame which forced them to remain flat and not curl through the deposition and cool-down process. First, a 100-nm-thick chromium layer was deposited by sputtering and was wet-etched as the bottom gate electrode. A silicon nitride (SiN_x) layer, an undoped amorphous-silicon layer, and a thin highly doped n^+ a-Si layer were deposited

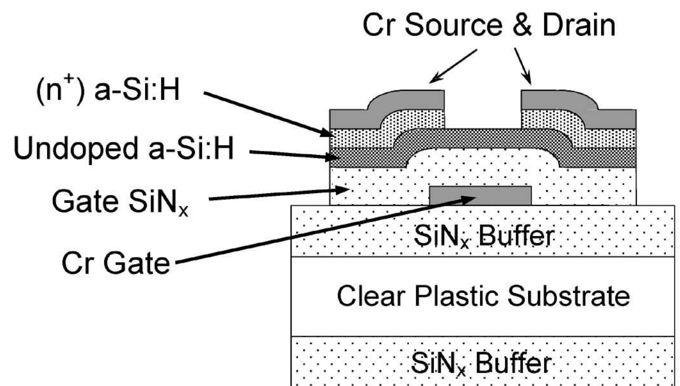


FIGURE 8 — Schematic cross section of the a-Si TFT structure on clear-plastic substrates.

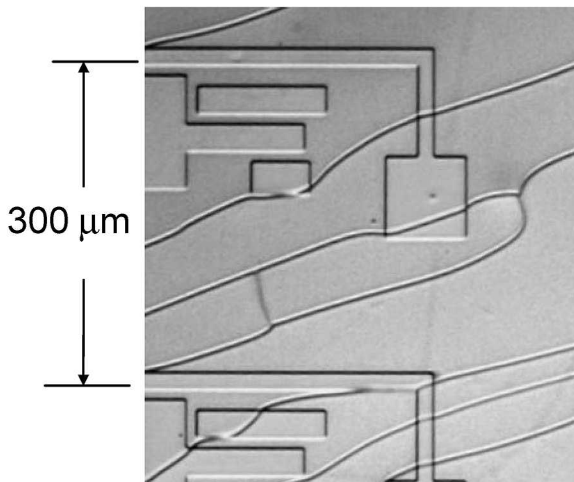


FIGURE 9 — Cracks in device films deposited at 250°C on substrate A. Film thicknesses were: buffer nitride, 500 nm; gate chromium, 100 nm; gate nitride, 350 nm; intrinsic a-Si, 200 nm; n^+ a-Si, 50 nm.

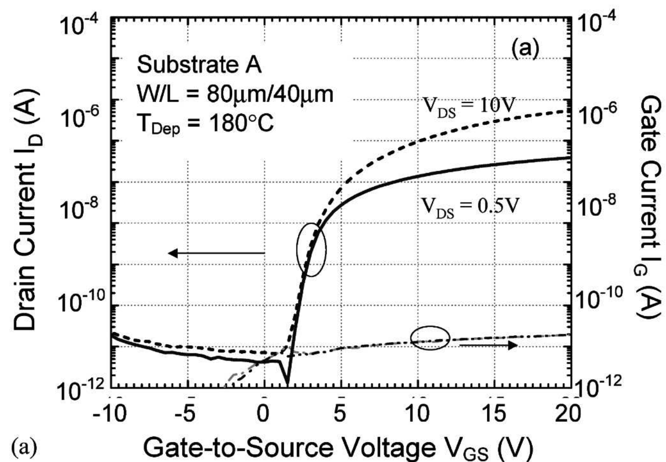
as the gate insulator, the active channel layer, and the source/drain contact layer, respectively. They were deposited in a multi-chamber PECVD system in one run, without breaking the vacuum. Before any patterning, another 80-nm-thick chromium layer was put down using thermal evaporation. This chromium layer was wet-etched to form the source/drain electrodes, and the n^+ a-Si layer was dry-etched with the same pattern. Then the undoped a-Si was dry-etched to define the transistor island. The TFT fabrication was finished by dry-etching windows into the gate nitride to open access to the gate contact pads.

3.1 a-Si TFTs on clear-plastic substrate A with high coefficient of thermal expansion

We first experimented with clear-plastic substrate A which has a high coefficient of thermal expansion (CTE) of 45 ppm/°C. When we attempted a 250°C process on substrate A (75 μm thick), the large CTE mismatch (ΔCTE) produced a large stress in the device layers and cracked them (Fig. 9). Cracking is expected from the data and modeling presented in Section 2.

To prevent cracking in the device films, we followed the guidelines developed in our earlier discussion. We reduced the process temperature to 180°C, used the thinnest substrates available (60 μm thick) and modified the TFT device structure to decrease the total thickness of the device stack. We reduced the thickness of the front nitride buffer layer from the 500 nm of the standard structure on Kapton 200E[3] to 200 nm, while keeping the buffer layer on the back side 500 nm thick. The thickness of the TFT layers was reduced from the standard design as follows: gate chromium from 100 to 80 nm, gate nitride from 350 to 300 nm, intrinsic a-Si from 200 to 150 nm, and n^+ a-Si from 50 to 30 nm.

After these modifications we successfully fabricated TFTs on substrate A at 180°C with very good performance (Fig. 10). For a TFT with a channel width/length of W/L =



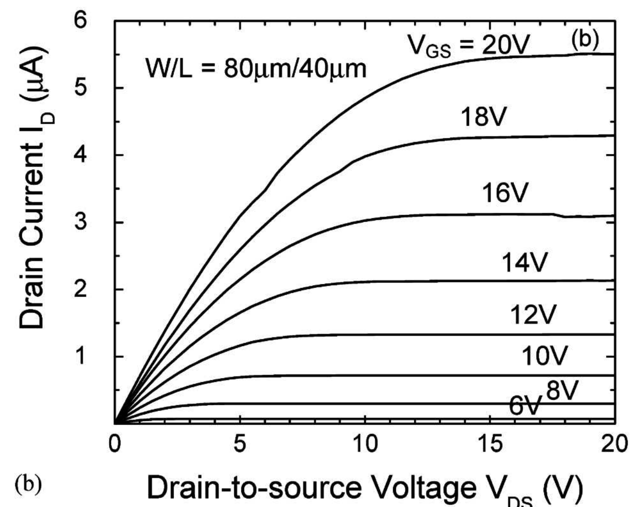


FIGURE 10 — (a) Transfer and (b) output characteristics of TFTs processed at 180°C on clear-plastic substrate A.

80 μm/40 μm, the threshold voltage is 3.2 V, the ON/OFF ratio is ~10^6 with gate voltages varied from –10 to 20 V, the linear mobility is 0.67 cm^2/V-sec, and the saturation mobility is 0.55 cm^2/V-sec. The source-gate leakage current is smaller than 20 pA and is close to the limit of the instrumentation. At a process temperature of 250°C, the device films still seriously cracked with the modified structure. This is not surprising given that Fig. 5 reveals that only 0.2 μm of SiN_x can be deposited without cracking, which is too thin for TFT fabrication. This is an instance where the maximum process temperature is not limited by the T_g of the substrate, but by the CTE mismatch between the substrate and the device layers.

3.2 a-Si TFTs on clear-plastic substrate B fabricated at temperatures up to 280°C

To increase the TFT process temperature, we used the second experimental clear-plastic substrate B. Because substrate B has a coefficient of thermal expansion of ≤10

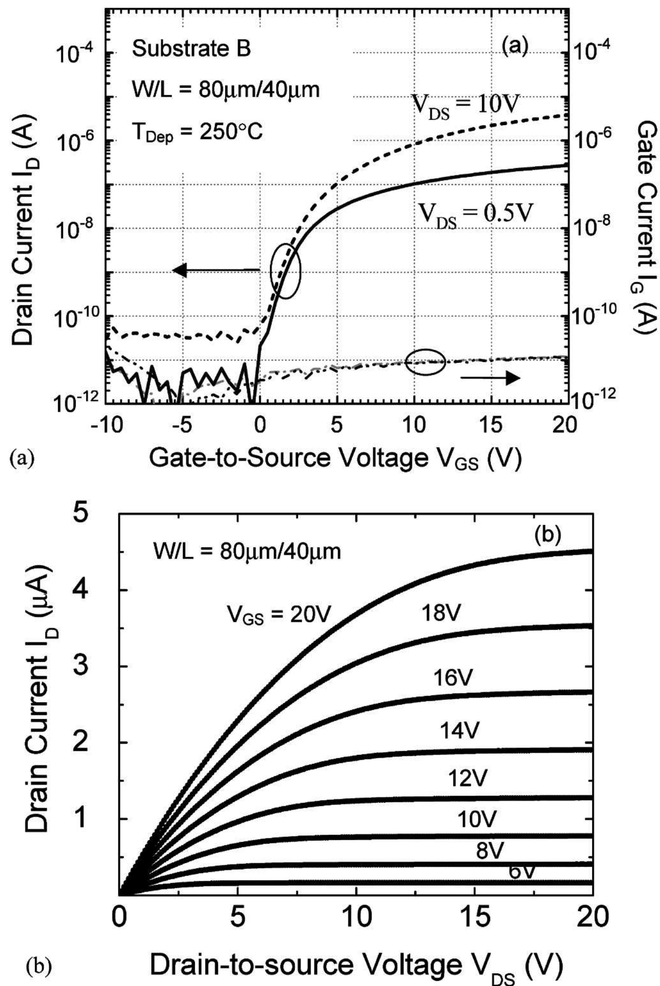


FIGURE 11 — (a) Transfer and (b) output characteristics of TFTs on clear-plastic substrate B, fabricated at a maximum process temperature of 250°C.

ppm/°C, it allowed thick SiN_x films (>1μm) to be deposited without cracking at 250 and 280°C (Fig. 5).

We successfully fabricated TFTs on substrate B at these maximum process temperatures of 250 and 280°C. These deposition temperatures are desirable because they lie close to the standard industrial process temperatures of 300–350°C. A 200-nm SiN_x buffer layer was used on each side of the plastic substrate. The device layer thicknesses were: gate chromium, 80 nm; gate nitride, 250 nm; intrinsic a-Si, 200 nm, n^+ a-Si, 30 nm.

For TFT's made at 250 and 280°C, the threshold voltages range from 2.0 to 3.8 V, the ON/OFF ratios are ~10^6 for a gate voltage swing from –10 to 20 V, the subthreshold slopes are about 500 mV/dec, the source-gate leakage is 4–10 pA at V_{GS} = 20 V (which is set by instrumentation). The electron mobilities in TFTs made at 280°C are slightly higher than those made at 250°C. In TFTs with a gate width/length of W/L = 80 μm/40 μm, the average saturation mobility is 1.1 cm^2/V-sec for 280°C TFTs *vs.* 0.8 cm^2/V-sec for 250°C TFTs. The transfer and output characteristics of a-Si TFTs made on substrate B at 250°C are shown in Fig.

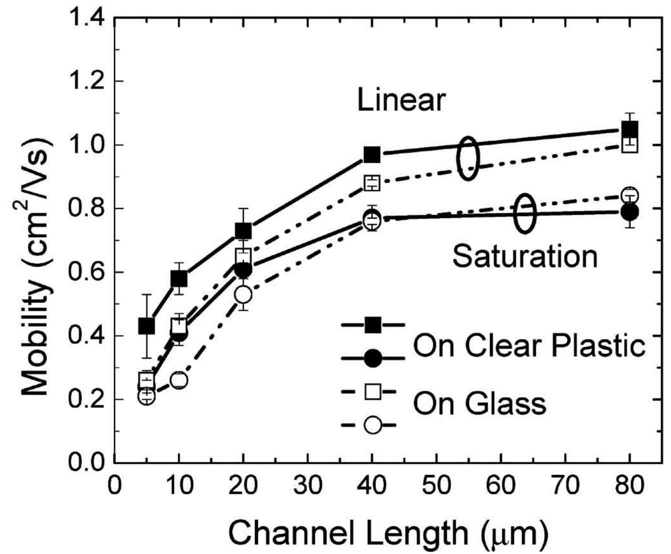


FIGURE 12 — Saturation and linear mobilities, not corrected for contact resistance, *vs.* channel length for a-Si:H TFTs fabricated at 250°C on clear-plastic substrate B and on glass. W = 80 μm.

11. It is evident that the process temperatures of 250 and 280°C on substrate B produce TFTs with higher mobility and lower threshold voltage than the 180°C process on substrate A.

Both the linear and saturation mobilities of TFTs made on clear-plastic substrate B tend to be higher than those made on glass substrates at the same process temperature of 250°C (Fig. 12), which is also the case for TFTs made on substrate A *vs.* glass at 180°C. The reason for this difference is not known. It might be a lower contact resistance in devices on clear substrates than on glass. The mobility extracted from I–V data increases for long channels, presumably because the contact resistance affects the short-channel devices more and manifests itself by lower mobility values (the mobilities of Fig. 12 are not corrected for contact resistance).

Figure 13 compares the mobilities and leakage currents of TFTs fabricated over a range of process temperatures from 130 to 280°C. Raising the process temperature raises the field-effect mobility and reduces the leakage current. Increasing the process temperature from 130°C on PEN to 280°C on the clear-plastic substrate B increased the mobility from 0.3 to 1 cm^2/V-sec, and reduced the leakage current by at least two orders of magnitude. Raising process temperature also greatly increased the device stability which has been reported in Ref. 13. Stability is an important issue for a-Si TFTs for AMOLED applications, especially for TFTs made at low temperature. In Ref. 13, we recently reported in a-Si TFTs on clear plastic with stability approaching those of industry standard a-Si TFTs made on glass. The critical step was to raise the process temperature on plastic substrate to 280°C.

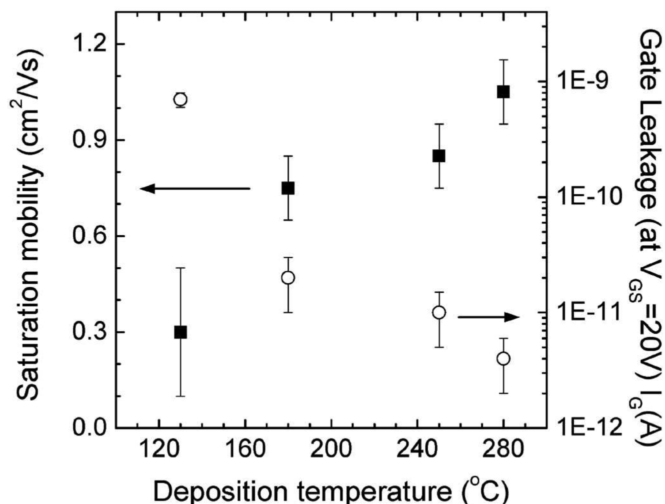


FIGURE 13 — Electron mobilities and gate leakage currents of TFTs made at four different maximum process temperatures.

4 Conclusion

The mechanical interaction of a silicon nitride layer and a plastic substrate is modeled to develop design guidelines for the TFT stack to avoid crack formation during TFT fabrication. Experiments show that the TFT films crack when the film stress per unit length exceeds a critical interfacial force. The film stress developed in the device stack can be reduced by controlling the built-in strain of the PECVD nitride into tension, by reducing the thickness of the device stack and by using a substrate with a low coefficient of thermal expansion. The PECVD deposition power can be used to control the built-in strain in the SiN_x film to compensate for the thermal mismatch strain. This method was then used to successfully fabricate a-Si TFTs on experimental clear-plastic substrates with a maximum process temperature of up to 280°C. The TFTs made at high temperatures have higher mobility and lower leakage current and are more stable than TFTs made at low temperatures on conventional low-T_g clear-plastic substrates.

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