

Active-Matrix Amorphous-Silicon TFT Arrays at 180 °C on Clear Plastic and Glass Substrates for Organic Light-Emitting Displays

K. Long, *Member, IEEE*, A. Z. Kattamis, I.-C. Cheng, H. Gleskova, *Member, IEEE*, S. Wagner, *Fellow, IEEE*, J. C. Sturm, *Fellow, IEEE*, M. Stevenson, G. Yu, and M. O'Regan

Abstract—An amorphous-silicon thin-film transistor (TFT) process with a 180 °C maximum temperature using plasma-enhanced chemical vapor deposition has been developed on both novel clear polymer and glass substrates. The gate leakage current, threshold voltage, mobility, and on/off ratio of the TFTs are comparable with those of standard TFTs on glass with deposition temperature of 300 °C–350 °C. Active-matrix pixel circuits for organic light-emitting displays (LEDs) on both glass and clear plastic substrates were fabricated with these TFTs. Leakage current in the switching TFT is low enough to allow data storage for video graphics array timings. The pixels provide suitable drive current for bright displays at a modest drive voltage. Test active matrices with integrated polymer LEDs on glass showed good pixel uniformity, behaved electrically as expected for the TFT characteristics, and were as bright as 1500 cd/m².

Index Terms—Active matrix, amorphous-silicon, flexible, organic light-emitting display, plastic substrate, thin-film transistor (TFT).

I. INTRODUCTION

ORGANIC light-emitting displays (OLEDs) have many potential advantages over the current dominant liquid crystal displays (LCDs), such as self-emission, video response, wide viewing angle, very thin form factor, and the compatibility with flexible plastic substrates to enable flexible displays. Furthermore, active-matrix OLED displays (AMOLEDs) have wider applications than passive matrices because AMOLEDs can more easily achieve high resolution, large size, and lower power consumption. To date, several groups have demonstrated AMOLEDs on glass substrates driven by amorphous-silicon (a-Si) transistor backplanes with very good performance [1], [2].

AMOLED on flexible plastic substrates are very attractive because of potential thin, light-weight, rugged, rollable, and foldable properties. The plastic substrates for the thin-film transistor (TFT) backplane must be optically clear if conventional OLEDs are used, which emit light through the substrate.

Manuscript received December 20, 2005; revised April 21, 2006. This work was supported by DuPont Company, DARPA, and NJCST. The review of this paper was arranged by Editor H. S. Tae.

K. Long, A. Z. Kattamis, I.-C. Cheng, H. Gleskova, S. Wagner, and J. C. Sturm are with the Department of Electrical Engineering, Princeton University, Princeton, NJ 08544 USA.

M. Stevenson, G. Yu, and M. O'Regan are with DuPont Displays, Santa Barbara, CA 93117 USA.

Digital Object Identifier 10.1109/TED.2006.878028

Because of the inability of most clear plastics to date to tolerate high process temperatures, the standard a-Si TFT processes used for AMLCDs and AMOLED demonstrations on glass cannot be used on clear plastic substrates because they require temperatures of up to 300 °C–350 °C [3]. A lower process temperature (e.g., 130 °C or lower) for the backplane could be a disadvantage for the AMOLED display, since at lower process temperatures, a-Si TFTs have lower mobility and high leakage current [4], [5]. These could degrade the drive current for the OLED and the data storage in the pixel, respectively. In this paper, a-Si:H TFTs with a 180 °C maximum process temperature have been developed on a novel clear plastic substrate not previously available. We present initial pixel performance on glass and on clear plastic substrates and integrated polymer LEDs on glass, which show that 180 °C a-Si TFTs on plastic or glass substrates can provide adequate drive current for bright light emission at low driving voltages and have the necessary low leakage current.

II. a-Si TFTs AT 180 °C ON CLEAR PLASTIC SUBSTRATE

The properties of the clear plastic substrates available to date have generally restricted the a-Si TFT fabrication process to temperatures below ~ 130 °C [4], [6]. A widely used clear plastic substrate is poly(ethylene terephthalate) (PET) [7]. Its glass transition temperature T_g of 70 °C–100 °C is too low for fabricating high-quality a-Si:H TFTs. Another popular clear plastic substrate is poly(ethylene naphthalate) (PEN). It has a T_g of 120 °C, and a-Si TFTs have been fabricated on it with maximum process temperature of 130 °C [5]. However, TFTs deposited at temperatures below 140 °C have low electron mobility and high leakage current and show pronounced drift due to charge trapping [4]. High-temperature plastics, such as the polyimide Kapton E, have a T_g of ~ 350 °C. Kapton E has a low coefficient of thermal expansion (CTE) and allows the fabrication of TFTs with excellent performance at process temperatures of 150 °C–250 °C [8], [9]. However, Kapton is not optically clear. Fig. 3 shows that the optical transmission of a 50- μ m-thick Kapton 200E substrate cuts off at about 500 nm, which gives it an orange-brown color.

Clear plastic substrates with a higher T_g than PET or PEN are therefore desirable to achieve good performance a-Si TFTs. In this paper, we used a new high-temperature clear plastic substrate, which is transparent down to 400 nm, as shown in

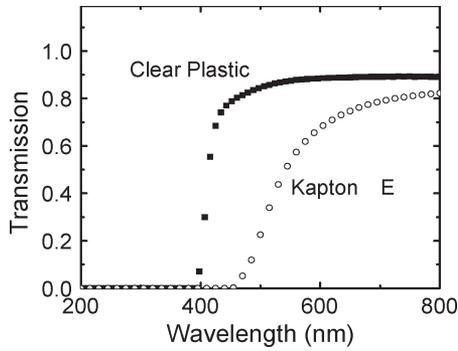


Fig. 1. Optical transmission spectra of 50- μm -thick Kapton 200E and 75- μm -thick clear plastic substrates.

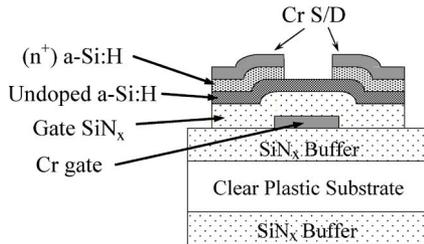


Fig. 2. Schematic cross section of the a-Si TFT structure on clear plastic substrates. (Color version available online at <http://ieeexplore.ieee.org>.)

Fig. 1. The substrate thickness we used is about 75 μm , and its glass transition temperature is 326 $^{\circ}\text{C}$.

Fig. 2 shows the cross section of the TFT structure in this paper on plastic substrates for the 180 $^{\circ}\text{C}$ process. First, a thick SiN_x buffer layer was deposited on each side of the substrate. It planarizes the substrate, passivates it against process chemicals, and helps the device layers adhere to the plastic substrate. In contrast to previous work with high-temperature plastic substrates that were mounted to rigid carriers for TFT fabrication [9], we kept our substrates freestanding to keep the back surface optically clean and clear. The TFT structure is the standard inverted staggered structure, with a bottom gate and top source/drain contacts. The TFT channel is defined by back-channel etch. First, a 100-nm-thick chromium layer was deposited by sputtering and wet etched as the bottom-gate electrode. A 300-nm-thick silicon nitride (SiN_x) layer, a 200-nm-thick undoped a-Si layer, and a thin (30 nm) highly doped n^+ a-Si layer were deposited continuously without breaking the vacuum in a multichamber plasma-enhanced chemical vapor deposition (PECVD) system as the gate insulator, the active channel layer, and the source/drain contact layer, respectively. The deposition temperature was $\sim 180^{\circ}\text{C}$. Before patterning, another 80-nm-thick chromium layer was put down using thermal evaporation. This chromium layer was wet etched as the source/drain electrodes, and the n^+ a-Si layer was dry etched with the same pattern. Then, the undoped a-Si was dry etched to define the transistor island. The TFT fabrication was finished by dry etching of windows into the gate nitride to open access to the gate contact pads.

Fig. 3(a) shows the transfer characteristics of a TFT on clear plastic with a width/length (W/L) of 80 $\mu\text{m}/5 \mu\text{m}$, and Fig. 3(b) is the output characteristics. The threshold voltage is 3.4 V, the linear mobility is 0.73 $\text{cm}^2/\text{V}\cdot\text{s}$, and the saturation

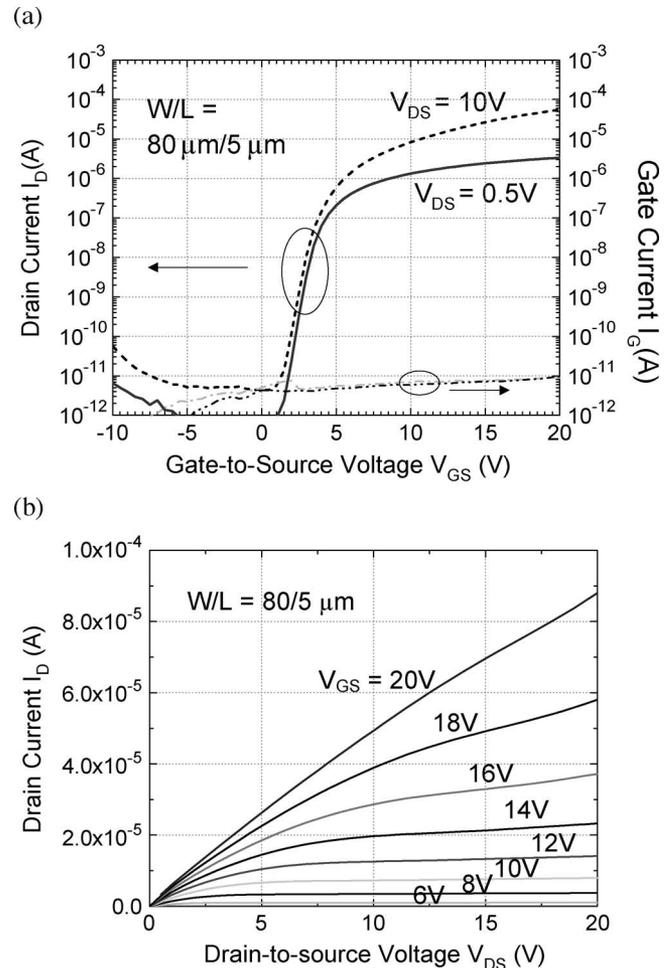


Fig. 3. (a) Transfer and (b) output characterizations of a-Si TFTs made on clear plastic with a maximum process temperature at 180 $^{\circ}\text{C}$.

mobility is 0.68 $\text{cm}^2/\text{V}\cdot\text{s}$. The off current at $V_{\text{GS}} = -10 \text{ V}$ is $\sim 10 \text{ pA}$, and the on/off ratio is $\sim 10^7$ with gate voltages varied from -10 to 20 V, and the subthreshold slope was $\sim 400 \text{ mV/dec}$. The source-gate leakage current at $V_{\text{GS}} = 20 \text{ V}$ is smaller than 10 pA, limited by the measurement system. The mobilities were not corrected for series resistance. The threshold voltages of ten TFTs range from 2.6 to 4.3 V. These values are comparable with those of a-Si TFTs fabricated in our lab at temperature of 300 $^{\circ}\text{C}$ –350 $^{\circ}\text{C}$. The very low off current and low gate leakage indicates that a relatively high-quality gate SiN_x was achieved with a relatively low deposition temperature of 180 $^{\circ}\text{C}$. This is essential for achieving a-Si TFTs with excellent performances on flexible plastic substrates. The mobility increases at longer channel length, presumably due to series resistance adversely affecting the short-channel devices (Fig. 5).

Control samples were also made on glass (Corning 1737) substrates with the same deposition temperature of 180 $^{\circ}\text{C}$. The TFT structure and fabrication process on glass were the same as those on plastic except that there were no buffer layers needed on glass substrate. For an 80 $\mu\text{m}/5 \mu\text{m}$ TFT on glass, the threshold voltage is 2.0 V, the linear mobility is 0.70 $\text{cm}^2/\text{V}\cdot\text{s}$, and the saturation mobility is 0.67 $\text{cm}^2/\text{V}\cdot\text{s}$ (Fig. 4). The threshold voltages of ten TFTs range from 1.5 to 3.3 V. These

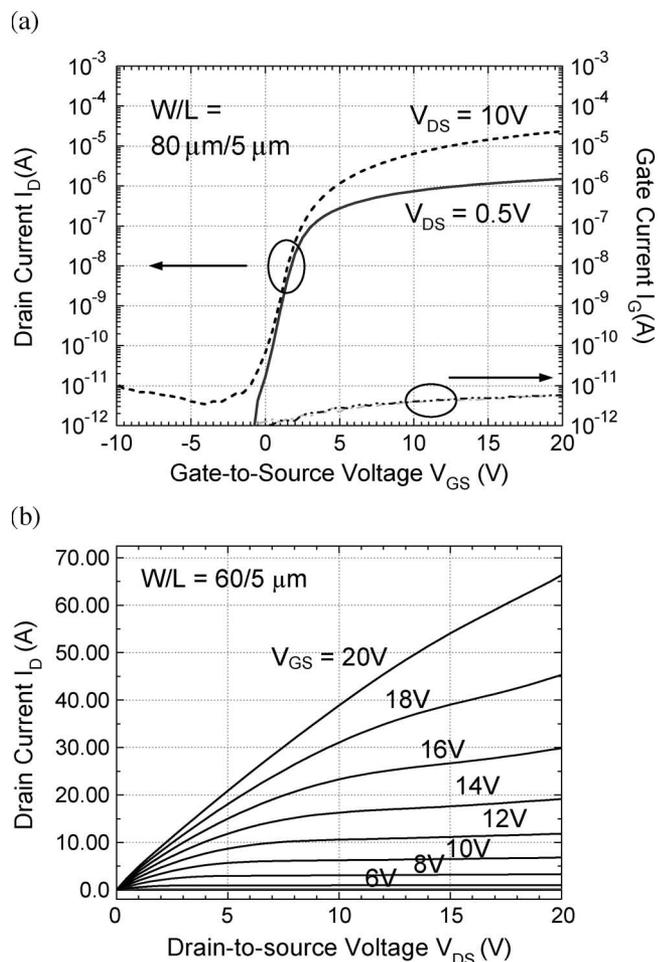


Fig. 4. (a) Transfer and (b) output characterizations of a-Si TFTs made on glass with a maximum process temperature at 180 °C.

are similar to those on the plastic substrates, as were the other device parameters. As was the case for the TFTs on plastic, both the linear and saturation mobilities (uncorrected for series resistance) increase with channel length. Both the linear and saturation mobilities of TFTs made on clear plastic substrate compare favorably with those made on glass substrates at the same process temperature of 180 °C (Fig. 5). The reason for this difference is not known, perhaps indicating a lower series resistance in devices on clear substrates.

The clear plastic substrate used in this paper had a CTE of ~ 50 ppm/°C, which was much higher than that of the a-Si TFT device layers (~ 3 ppm/°C for a-Si and 2.7 ppm/°C for SiN_x). The stress σ in the device films caused by thermal expansion mismatch between the device films and the substrate is proportional to the product of the difference in CTE between the device films and the plastic, ΔCTE , times the process temperature excursion, ΔT , i.e.,

$$\sigma \propto \Delta CTE \cdot \Delta T. \quad (1)$$

$\Delta CTE \cdot \Delta T$ in this paper was ~ 0.008 (0.8%) for the 180 °C process. This limited our ability to further raise the process temperature, as the device layer cracked after deposition.

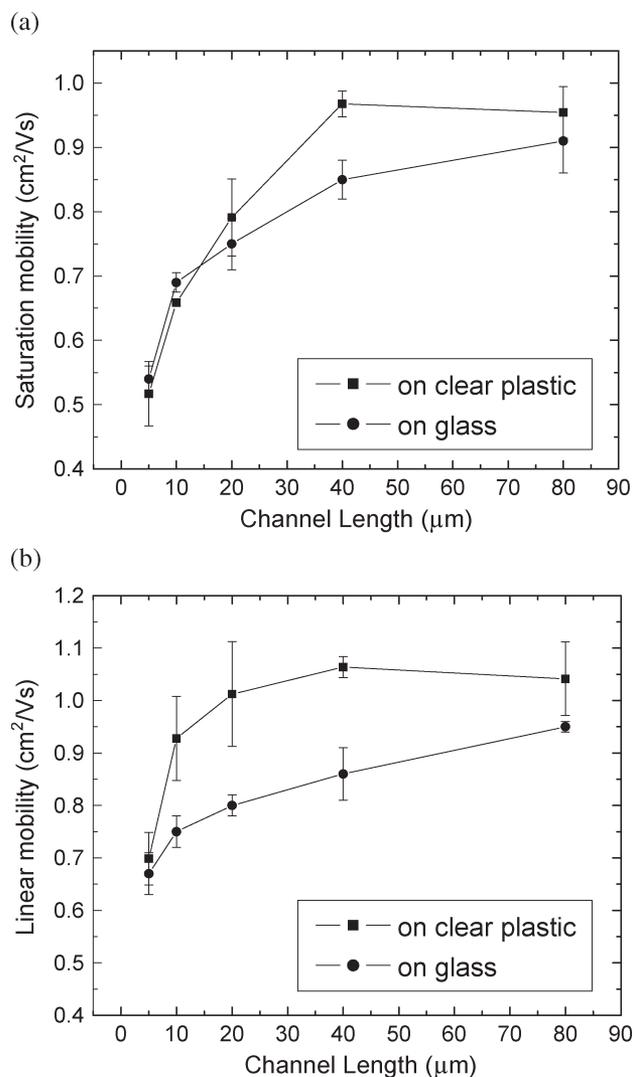


Fig. 5. Mobility versus channel length for a-Si:H TFTs fabricated at 180 °C on clear plastic substrate and on glass, for devices with a width of 80 μm . (a) Saturation region. (b) Linear region.

III. AMOLED BACKPLANE WITH 180 °C a-Si TFT

A. Design and Fabrication of 180 °C a-Si TFT AMOLED Backplane

The AMOLED pixel circuit design (Fig. 6) is the simple 2-TFT scheme. T1 is the switching TFT, whose function is similar to the one in AMLCD pixel, and controls writing and holding of data signal (V_{DATA}) to the storage capacitor (V_{STORE}). T2 is the driving TFT, which provides current to drive OLED to the desired brightness according to the data voltage on its gate. The data voltage (V_{DATA}) is stored on the capacitor (V_{STORE}) to drive T2.

We now estimate the W/L ratio required of the driving transistor for a desired pixel brightness. Note that the source of T2 is connected to the OLED anode (V_{OLED}); thus, the applied data voltage (V_{DATA}) is split between the OLED and T2. This is because the lower OLED terminal is typically the cathode. For a transistor under saturation, the drain-current I_{DS} is

$$I_{\text{DS}} = (W/2L)\mu_{\text{SAT}}(\epsilon_{\text{SiN}_x}\epsilon_0/t)(V_{\text{GS}} - V_{\text{T}})^2 \quad (2)$$

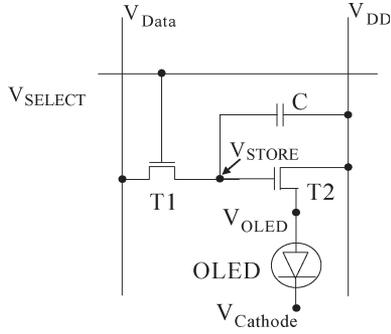


Fig. 6. Schematic circuit of the 2-TFT pixel used in this paper. T1 is the switching transistor, T2 is the drive transistor, and C is the storage capacitor. The OLED anode connected to source of T2.

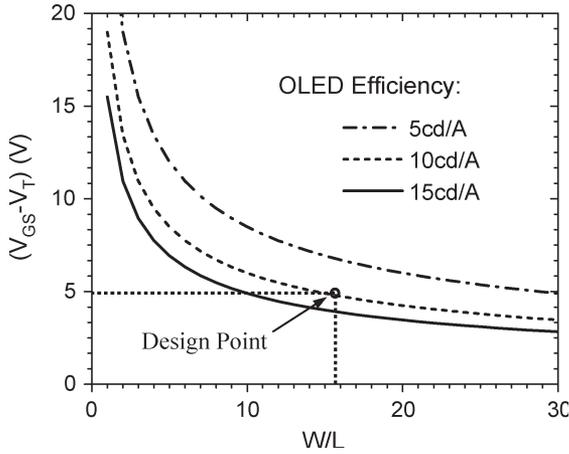


Fig. 7. Required $V_{GS} - V_T$ on drive transistor as a function of W/L , for various OLED efficiencies, assuming a pixel size of $300 \mu\text{m} \times 300 \mu\text{m}$, a polarizer efficiency of 50%, an a-Si TFT mobility of $0.5 \text{ cm}^2/\text{V} \cdot \text{s}$, and a gate SiN_x thickness of 250 nm. Our design point is $W/L = 16$, with OLED efficiency of $\sim 10 \text{ cd/A}$.

where W and L are the channel width and length, respectively, μ_{SAT} is the field effective mobility in saturation, ϵ_{SiN_x} and t are the dielectric constant and thickness of the gate nitride, respectively, V_{GS} is the gate voltage ($V_{\text{STORE}} - V_{\text{OLED}}$), and V_T is the threshold voltage. The relationship between the OLED drive current I and the OLED luminance L is

$$L = \eta_0 I \quad (3)$$

where η_0 is the OLED luminance efficiency.

The required gate voltage for a brightness B for a pixel of area A and polarizer efficiency η_p is then

$$V_{GS} - V_T = (AB / (\eta_0 (W/2L) \mu_{\text{SAT}} (\epsilon_{\text{SiN}_x} \epsilon_0 / t)))^{1/2}. \quad (4)$$

This is shown in Fig. 7, as a function of W/L of T2, for a display brightness B (luminance over area) of 100 cd/m^2 (nits), a pixel size A of $300 \mu\text{m} \times 300 \mu\text{m}$, a polarizer efficiency η_p of 50%, an a-Si TFT mobility μ_{SAT} of $0.5 \text{ cm}^2/\text{V} \cdot \text{s}$, and a gate SiN_x thickness of 250 nm and assuming OLED efficiencies of 5, 10, and 15 cd/A . Our design point assumed the above parameters, an OLED efficiency of 10 cd/A , and a maximum difference of the data voltage from the OLED anode voltage

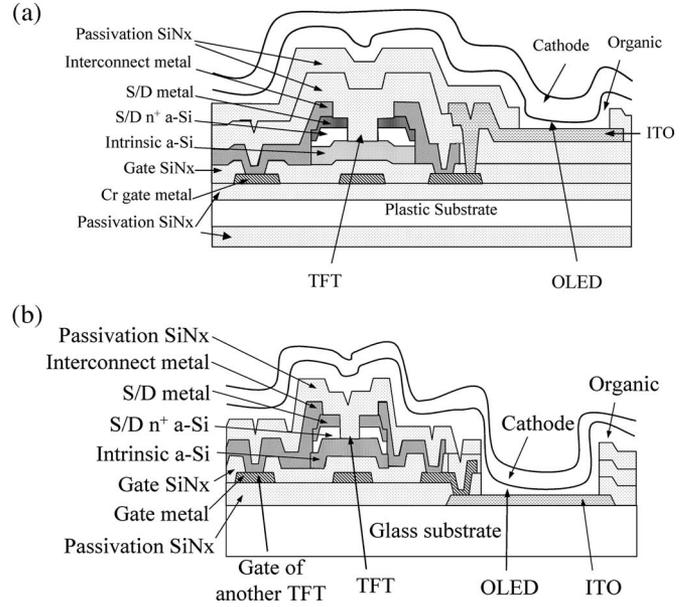


Fig. 8. Schematic cross section of the TFT-OLED integration (a) on clear plastic substrates and (b) on glass.

($V_{\text{DATA}} - V_{\text{OLED}}$) of 5 V, resulting in a required W/L of T2 of 16. At this point, the pixel current would be $2 \mu\text{A}$.

A $3 \text{ in} \times 3 \text{ in}$ test sample with several small AMOLED arrays and test structures in the center $1 \text{ in} \times 1 \text{ in}$ area was fabricated. The outside area was for interconnecting lines, for external connection for driving electronics and environmental sealing. Fig. 8(a) is the schematic cross section of the a-Si TFT AMOLED backplane on plastic. The a-Si TFTs were fabricated using the same structure and process mentioned in Section II. After the TFT fabrication, aluminum was deposited and patterned with liftoff process as the interconnect metal, to connect different TFTs to form AMOLED circuits, forming interconnect lines and contact pads for making contact to external drivers. To avoid an undesirable indium tin oxide (ITO)-aluminum interaction, the ITO and aluminum were connected to each other through connections to the gate metal (chromium). A thick SiN_x (500 nm) layer was deposited as the passivation layer to cover the whole backplane before OLED integration. ITO was then deposited by sputtering at room temperature and was patterned by wet etching. Another SiN_x layer was deposited on top of the patterned ITO to passivate the edge of the ITO. A window was opened on top of the ITO through the SiN_x by dry etching to expose the ITO for the OLED integration. Blanket organic layer deposition and a cathode (limited by a shadow mask to the central area) completed the structure.

On glass substrates, the process was similar except that we started with ITO-coated glass from an external supplier. After the ITO was patterned by wet etching, a 100-nm-thick SiN_x was deposited using PECVD to protect the ITO from the TFT process. After that, the TFT structure and interconnect metal were fabricated and covered by thick SiN_x . Then, ITO was exposed, and OLED was integrated [Fig. 8(b)]. Fig. 9 is a micrograph of a pixel in the array before OLED integration. The size of one pixel is $300 \mu\text{m} \times 300 \mu\text{m}$. T1 was implemented as two TFTs with width/length of $20 \mu\text{m}/5 \mu\text{m}$ in series for

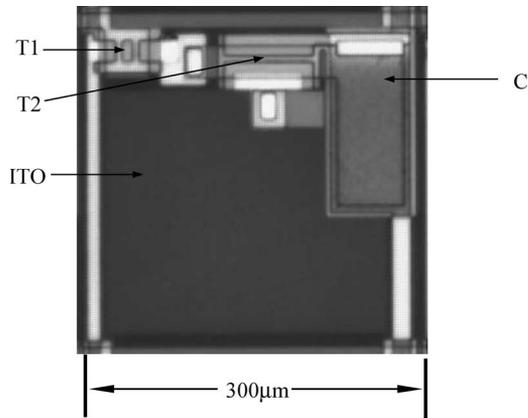


Fig. 9. Micrograph of a pixel in a 2-TFT AMOLED array before OLED integration. T1 is the switching transistor, T2 is the drive transistor, and C is the storage capacitor. The patterned ITO will become the anode of the OLED.

insuring a low leakage current [10]. T2 had width/length of 80 $\mu\text{m}/5 \mu\text{m}$, and its source connected to the anode of the OLED. The storage capacitance was about 2 pF. The fill factor of the pixel is about 46%. It was limited by the minimum linewidth of our design, which is 5 μm .

B. Current Drivability

Before the OLED was deposited, we tested the drive current generated by a pixel by applying dc control voltages to pixels on both plastic and glass substrates. V_{DD} was applied to the drain of the driving transistor T2, which was fixed at 20 V. The source of T2 (future OLED anode) was connected to ground. We scanned the data voltage (V_{DATA}) from 0 to 20 V and stepped the voltage on the gate of T1 (V_{SELECT}) as 5, 10, and 15 V. The current flowing through T2 is measured as the pixel current (Fig. 10(a) for plastic). As $V_{DATA} - V_{OLED}$ is increasing, the pixel current increases as expected, with T2 in saturation. In this region, (2) describes the pixel current. For large $V_{DATA} - V_{OLED}$, the current saturates because T1 limits the charging of the storage capacitor (controlled by V_{SELECT}). The open circles are the circuit simulation results using an a-Si TFT model. In the simulation, threshold voltage $V_T = 4.5 \text{ V}$, mobility $\mu = 0.65 \text{ cm}^2/\text{V} \cdot \text{s}$ for T1 and $V_T = 3.5 \text{ V}$, $\mu = 0.80 \text{ cm}^2/\text{V} \cdot \text{s}$ for T2 were assumed, which are consistent with the measured TFT results in Section II. The simulation results agree well with the measurement data. For the desired pixel current of 2 μA for 100 nits display brightness (assuming an OLED efficiency of 10 cd/A), a $V_{DATA} - V_{OLED}$ of only 9 V is required, corresponding to $V_{GS} - V_T = 5.5 \text{ V}$ on T2. This result is close to the design point of the previous section, showing that the 180 °C a-Si TFT backplanes on clear plastic substrates provide sufficient drive current for AMOLED application.

Similar results were found on glass substrates [Fig. 10(b)]. In this case, modeling parameters of $V_T = 2.0 \text{ V}$, $\mu = 0.7 \text{ cm}^2/\text{V} \cdot \text{s}$ for both T1 and T2 were used to fit the data. On the glass substrate, the $V_{DATA} - V_{OLED}$ needed to get 100 nits brightness ($\sim 2 \mu\text{A}$ of drive current) is only 6 V, which corresponded to $V_{GS} - V_T = 4 \text{ V}$ on T2. This is lower than the design goal of 5 V (Fig. 7) due to the higher experimen-

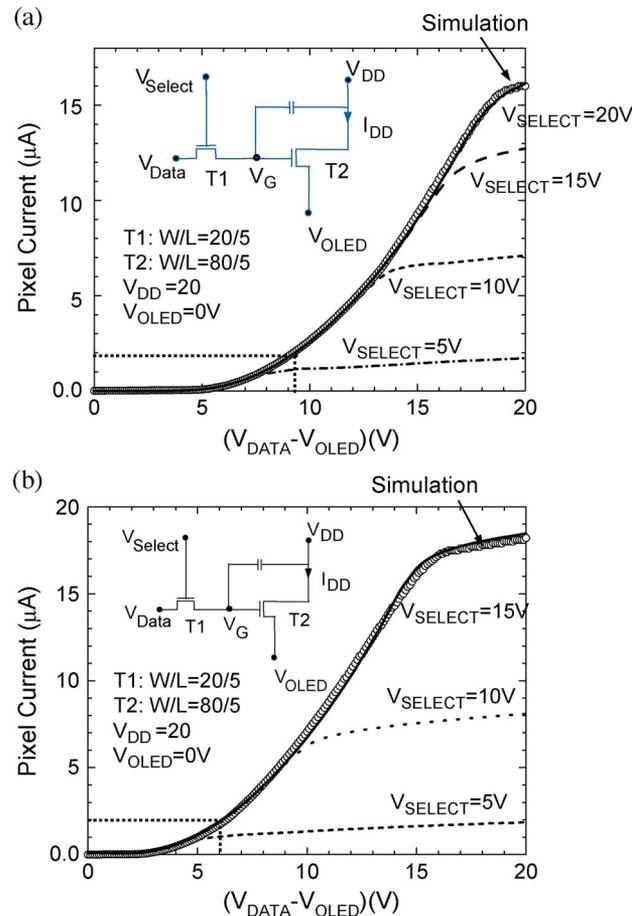


Fig. 10. DC drive current as a function of data voltage tested a 2-TFT pixel before OLED integration on (a) clear plastic and (b) glass substrates for different select voltages. The open circles are simulation results using H-SPICE. The data voltage needed for 100 nits display brightness (2- μA pixel current) is also labeled with dotted line. (Color version available online at <http://ieeexplore.ieee.org>.)

tal mobility of 0.7 $\text{cm}^2/\text{V} \cdot \text{s}$ versus the earlier conservative assumption of 0.5 $\text{cm}^2/\text{V} \cdot \text{s}$.

C. Data Storage and Leakage Current

An important property of an AMOLED pixel is its ability to hold the data signal programmed into it through a frame time. To test this storage ability of the a-Si TFT backplane, before OLED integration, we connected a 1-M Ω resistor in place of the OLED in a test pixel on a glass substrate; thus, we could use its voltage as a measure of the drive current [Fig. 11(a)]. With V_{DD} (drain of T2) of 24 V, pulse signals as V_{DATA} and V_{SELECT} were applied with different frame times to test the data storage of the pixel. In the duration of one frame time, the programmed V_{DATA} should be stored as V_G . If there is a leak in T1, or if there is a leaky gate nitride, the gate voltage will decrease, which can be observed as a drop in the voltage over the resistor due to decreased current in T2. Fig. 11(b) shows the waveform of V_{DATA} and V_{SELECT} applied to the pixel and the measured voltage drop on V_{OLED} on a multichannel oscilloscope. The select signal went from -10 V (off) to 20 V (on), with a pulsewidth of 20 μs . The DATA signal went from 0 (off) to V_{DATA} (on), with a pulsewidth of 40 μs . Fig. 12 shows the

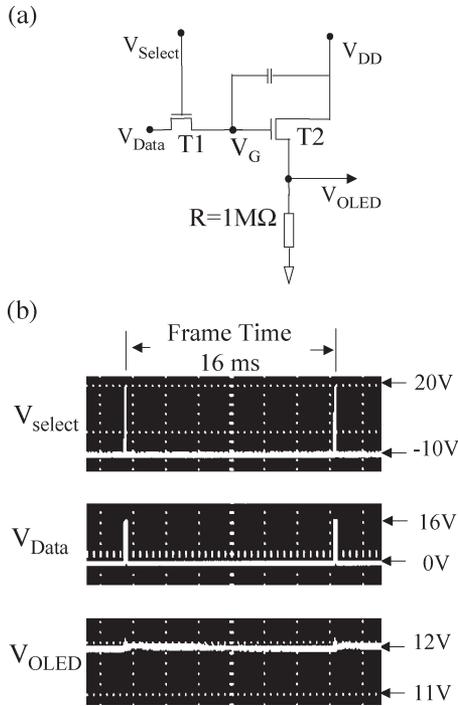


Fig. 11. (a) Schematic circuit for dynamic testing of pixels before OLED integration, with OLED replaced by a 1-M Ω resistor for current monitoring. (b) Applied data signal, applied select signal, and V_{OLED} (proportional to drive current) versus time.

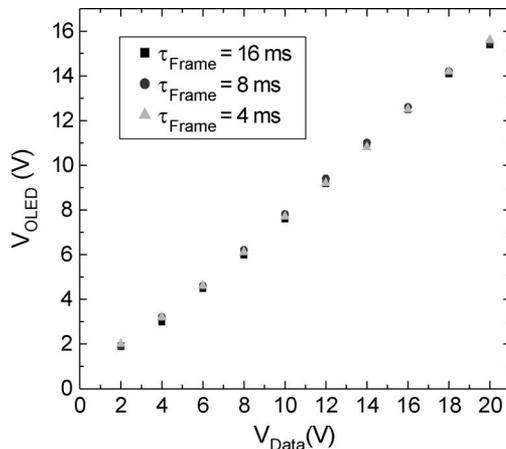


Fig. 12. Stored voltage as a function of input data voltage for different frame times of 4, 8, and 16 ms.

time-averaged V_{OLED} (proportional to drain-current) as a function of V_{DATA} with different frame times. On a scale of volts, no difference of V_{OLED} could be detected with different frame times of 4, 8, and 16 ms, showing that any loss of data voltage during a frame time is very small. (A 16-ms frame time and ~ 60 - μs row time are characteristics of quarter video graphics array (QVGA) display timing.) There is a slight voltage drop on V_{OLED} during a frame time if directly observed on an oscilloscope [Fig. 12(b)]. Voltage drops of V_{OLED} as 80, 120, and 160 mV for frame times of 4, 8, and 16 ms were observed. With the storage capacitor of 2 pF, this places an upper limit on the leakage current through T1 of 2×10^{-11} A. This is in agreement with the TFT leakage current under reverse gate bias

of -10 V, which is $\sim 10^{-11}$ A as shown in Fig. 2(a). While the exact voltage decay allowed in an application depends on the degree of gray scale, the observed decay shows that the 180 $^{\circ}\text{C}$ process provides leakage currents low enough for most applications. This low leakage current is a crucial advantage in those 180 $^{\circ}\text{C}$ TFTs on clear plastic over those shown earlier on other substrates with lower process temperatures [4], [5].

Besides leakage, reliability is an important issue for a-Si TFTs for AMOLED applications, especially for TFTs made at low temperature. In a separate effort, we recently reported a a-Si TFTs on clear plastic with reliability approaching those of industry standard a-Si TFTs made on glass [12]. The critical step was to raise the process temperature beyond the 180 $^{\circ}\text{C}$ reported in this paper (which focuses on integration) to near 300 $^{\circ}\text{C}$.

D. AMOLED Test Array

We integrated the a-Si TFT backplane on glass with polymer OLEDs to make AMOLED test arrays. The OLED integration on the two clear plastic substrates was limited by practical yield problems during the interconnect metal patterning step. After the TFT fabrication, the backplane was covered by a thick SiN_x passivation layer, which prevents the OLED cathode metal from connecting with the TFT circuits [Fig. 8(b)]. The polymer layer and the cathode layer were unpatterned within the active region. After windows were opened in the SiN_x passivation down to the ITO, a poly(3,4-ethylenedioxythiophene) (PEDOT) layer was spun on as the hole injection layer. After the drying of the PEDOT layer, a “super-yellow” emissive polymer (a poly(phenylene vinylene)-type polymer from Merck) was deposited by spin coating and dried. Finally, the cathode was deposited. The organic layer and cathode were limited to the central active region, and the active area is sealed with a glass cap and epoxy for environmental stability. The contact pads at the edges of the display sample were then connected to the external driving electronics using flex cables and tape-automated bonding (TAB).

Fig. 13 shows a 5×5 AMOLED array being driven with a QVGA timing with 16-ms frame time and 50- μs row time, under different data voltages V_{DATA} . V_{DD} , V_{SELECT} , and the cathode voltage were set at 24, 20, and 0 V, respectively. Because of the limitation of our driving electronics, all pixels were driven to the same brightness. One row contact failed; thus, only four rows are visible. The uniformity of the brightness of the pixels is visibly good. The current-voltage (I - V) characteristics of a $250 \mu\text{m} \times 250 \mu\text{m}$ test OLED, close to the area of the OLEDs in the pixels, are in Fig. 14. For the target current density of 2 mA/cm 2 for a pixel brightness of 200 nits before any polarizer, an OLED voltage of 5.5 V is required, which adds to the data voltages in the previous section where the OLED anode contact was grounded.

A large-area photodiode was used to collect the light emitted from the array. The detected photocurrent was then converted to the total luminance of the array, knowing the efficiency of the photo diode and the collection efficiency. Then, the average brightness of the array was calculated using the area of the 20 working pixels. The average pixel current and the

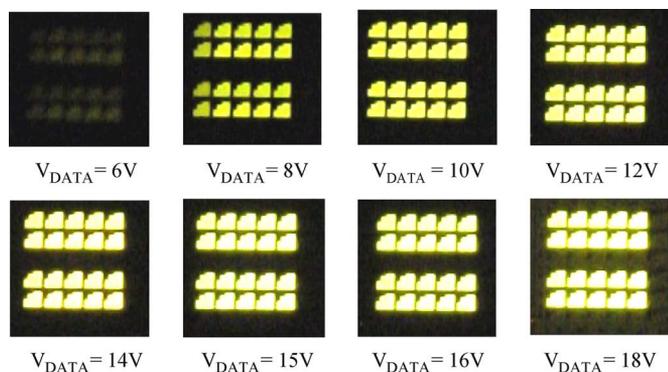


Fig. 13. Images of a 5 × 5 AMOLED array (one row contact is missing) under QVGA driving with different data voltages. (Color version available online at <http://ieeexplore.ieee.org>.)

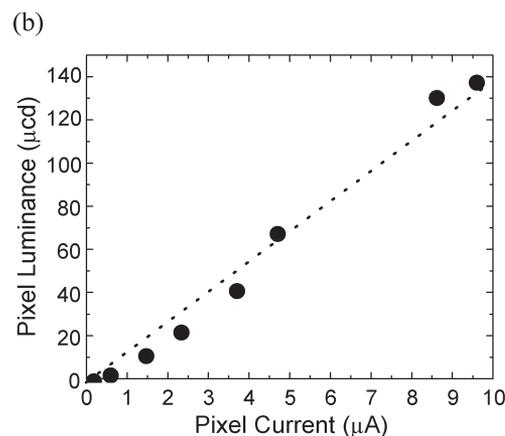
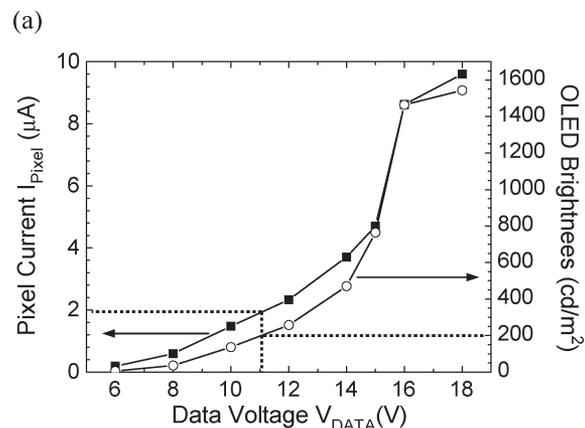


Fig. 15. (a) Measured pixel current and pixel brightness as a function of data voltage. The dotted lines indicate 1-V data voltage is needed for 100 nits display brightness. (b) Pixel brightness as a function of pixel current.

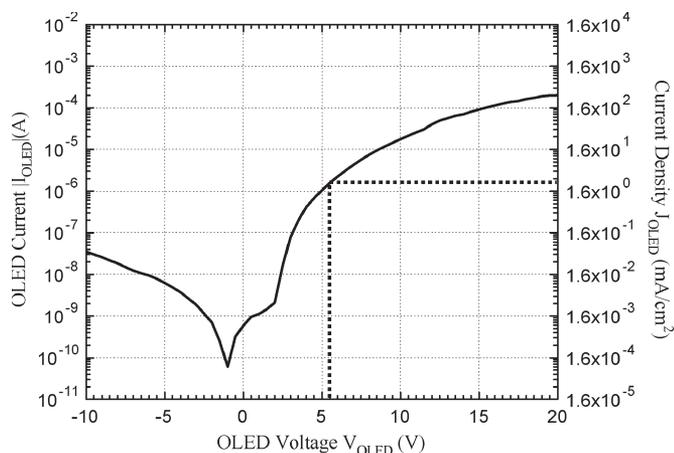


Fig. 14. I - V characteristics of a test OLED with an area of $250 \mu\text{m} \times 250 \mu\text{m}$. Dotted lines show current density needed for 200 nits OLED brightness.

display brightness as a function of the data voltage are shown in Fig. 15(a). Including the ~ 4 -V OLED turn on voltage, the display starts to turn on at $V_{\text{DATA}} = 6 \text{ V}$, implying a TFT threshold voltage of $\sim 2 \text{ V}$. From the slope of pixel luminance versus pixel current [Fig. 15(b)], the luminance efficiency of the OLED is 14 cd/A , which was typical of that expected for polymer LEDs made of the super-yellow polymer [11]. For a display brightness of 100 nits (pixel brightness of 200 nits), V_{DATA} of 11 V is required, corresponding to V_{OLED} of $\sim 5.5 \text{ V}$ and a gate-source voltage ($V_{\text{DATA}} - V_{\text{OLED}}$) on T2 of 5.5 V. This number is slightly lower than the required 6 V estimated by dc electrical testing before the OLED integration. The primary reason for the lower drive requirement is that the actual OLED luminance efficiency of 14 cd/A is higher than that used in the estimation (10 cd/A).

IV. CONCLUSION

a-Si TFTs with excellent performance at process temperature of $180 \text{ }^\circ\text{C}$ have been fabricated both on clear plastic and glass substrates. Active-matrix backplane pixel circuits made for polymer LEDs can provide sufficient drive current at low data voltage for bright displays and sufficiently low leakage current for active-matrix operation. Pulsed operation under various

timings shows that the leakage in the access transistor is very small, so that data is accurately latched in the pixel for the entire frame time. A small AMOLED array was successfully demonstrated with very high brightness ($> 1000 \text{ nits}$) at a relatively low data voltage (15 V) with only $\sim 9 \text{ V}$ of this across the TFT itself. These results show that amorphous silicon TFTs on clear plastic are an attractive route to AMOLED displays on clear flexible plastic substrates.

ACKNOWLEDGMENT

The authors would like to thank DuPont Company for providing the substrates, Planar for providing the electronic system for AMOLED testing, and B. Hekmatshoar for helping with circuit simulation.

REFERENCES

- [1] T. Tsujimura, Y. Kobayashi, K. Murayama, A. Tanaka, M. Morooka, E. Fukumoto, H. Fujimoto, J. Sekine, K. Kanoh, K. Takeda, K. Miwa, M. Asano, N. Ikeda, S. Kohara, S. Ono, C.-T. Chung, R.-M. Chen, J.-W. Chung, C.-W. Huang, H.-R. Guo, C.-C. Yang, C.-C. Hsu, H.-J. Huang, W. Riess, H. Riel, S. Karg, T. Beierlein, D. Gundlach, S. Alvarado, C. Rost, P. Muller, F. Libsch, M. Mastro, R. Polastre, A. Lien, J. Stanford, and R. Kaufman, "A 20-inch OLED displays driven by super-amorphous-silicon technology," in *Proc. SID Tech. Dig.*, 2003, vol. 34, pp. 6-9.
- [2] J.-J. Lih and C.-F. Sung, "Full-color active-matrix OLED based on a-Si TFT technology," *J. Soc. Inf. Disp.*, vol. 12, no. 4, pp. 367-371, Dec. 2004.

- [3] S. Wagner, H. Gleskova, J. C. Sturm, and Z. Suo, "Novel processing technology for macroelectronics," in *Technology and Application of Amorphous Silicon*, vol. 37, R. A. Street, Ed. Berlin, Germany: Springer-Verlag, 2000, pp. 222–251.
- [4] C.-S. Yang, L. L. Smith, C. B. Arthur, and G. N. Parsons, "Stability of low-temperature amorphous silicon thin film transistors formed on glass and transparent plastic substrates," *J. Vac. Sci. Technol. B, Microelectron.*, vol. 18, no. 2, pp. 683–689, Mar. 2000.
- [5] K. Long, H. Gleskova, S. Wagner, and J. C. Sturm, "Short channel amorphous-silicon TFT's on high-temperature clear plastic substrates," in *Proc. 62nd Device Research Conf. Dig.*, 2004, pp. 89–90.
- [6] D. Stryakhilev, A. Sazonov, and A. Nathan, "Amorphous silicon nitride deposited at 120 °C for OLED-TFT arrays on plastic substrates," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 22, no. 4, pp. 1087–1090, 2002.
- [7] G. Gustafsson, Y. Cao, G. M. Treacy, F. Klavetter, N. Colaneri, and A. J. Heeger, "Flexible light-emitting diodes made from soluble conducting polymers," *Nature*, vol. 357, no. 6378, p. 477, Jun. 1992.
- [8] H. Gleskova, S. Wagner, and Z. Suo, "A-Si:H TFTs made on polyimide foil by PECVD at 150 °C," in *Proc. Mat. Res. Soc. Symp.*, G. N. Parsons, C. C. Tsai, T. S. Fahlen, and C. H. Seager, Eds, 1998, vol. 508, pp. 73–78.
- [9] D. B. Thomasson, M. Bonse, R. J. Koval, J. R. Huang, C. R. Wronski, and T. N. Jackson, "Tri-layer a-Si:H TFTs on polymeric substrates," in *Proc. 56th Device Res. Conf. Dig.*, 1998, p. 126.
- [10] J. C. Sturm, I.-W. Wu, and M. Hack, "Leakage current modeling of series-connected thin film transistors," *IEEE Trans. Electron Devices*, vol. 42, no. 8, pp. 1561–1563, Aug. 1995.
- [11] H. Becker, H. Spreitzer, W. Kreuder, E. Kluge, H. Schenk, I. Parker, and Y. Cao, "Soluble PPVs with enhanced performance—A mechanistic approach," *Adv. Mater.*, vol. 12, no. 1, pp. 42–48, Jan. 2000.
- [12] K. Long, A. Z. Kattamis, I.-C. Cheng, H. Gleskova, S. Wagner, and J. C. Sturm, "Stability of amorphous-silicon thin-film transistors deposited on clear plastic substrates at 250 °C to 280 °C," *IEEE Electron Device Lett.*, vol. 27, no. 2, pp. 111–113, Feb. 2006.
- K. Long** (M'03), photograph and biography not available at the time of publication.
- A. Z. Kattamis**, photograph and biography not available at the time of publication.
- I.-C. Cheng**, photograph and biography not available at the time of publication.
- H. Gleskova** (M'01), photograph and biography not available at the time of publication.
- S. Wagner** (SM'80–F'00), photograph and biography not available at the time of publication.
- J. C. Sturm** (M'80–S'81–M'85–SM'95–F'01), photograph and biography not available at the time of publication.
- M. Stevenson**, photograph and biography not available at the time of publication.
- G. Yu**, photograph and biography not available at the time of publication.
- M. O'Regan**, photograph and biography not available at the time of publication.