Amorphous Silicon Thin-Film Transistor Backplanes Deposited at 200 °C on Clear Plastic for Lamination to Electrophoretic Displays

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***Abstract*—The transition of thin-film transistor (TFT) backplanes from rigid plate glass to flexible substrates requires the development of a generic TFT backplane technology on a clear plastic substrate. To be sufficiently stable under bias stress, amorphous-silicon (a-Si:H) TFTs must be deposited at elevated temperatures, therefore the substrate must withstand high temperatures. We fabricated a-Si:H TFT backplanes on a clear plastic substrate at 200 °C. The measured stability of the TFTs under gate bias stress was superior to TFTs fabricated at 150 °C. The substrate was dimensionally stable within the measurement resolution of 1 μm, allowing for well-aligned 8 × 8 and 32 × 32 arrays of 500 μm × 500 μm pixels. The operation of the backplane is demonstrated with an electrophoretic display. This result is a step toward the drop-in replacement of glass substrates by plastic foil.**

***Index Terms*—Amorphous silicon thin-film transistor (a-Si:H TFT), clear plastic, electrophoretic display, flexible, stability.**

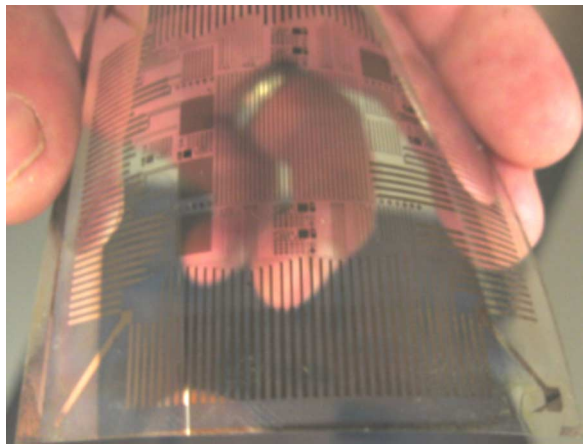

Fig. 1. Competed a-Si:H TFT backplane on clear plastic prior to electrophoretic frontplane lamination.

I. Introduction

THE success of active-matrix liquid-crystal displays (AMLCDs) and X-ray sensor arrays has encouraged research into next-generation flexible electronic surfaces. A flexible amorphous silicon thin-film transistor (a-Si:H TFT) backplane on a clear flexible substrate would be most desirable for the drop-in replacement of the a-Si:H TFT backplane on glass. In early research on flexible a-Si:H TFT backplanes on plastic the process temperature was reduced to the glass temperature $\mathrm{T_g}$ of common clear plastic substrates such as polyethylene terephthalate (PET, $\mathrm{T_g}$ = 78 °C) and polyethylene naphthalate (PEN, $\mathrm{T_g}$ = 120 °C) [1], [2]. While the initial performance of the a-Si:H TFTs made at temperatures down to 140 °C is acceptable for AMLCD use, it has become clear recently that for adequate long-term stability the a-Si:H TFT stack must be deposited at high temperature [3]. A high-temperature compatible clear polymer substrate is the crucial enabler for such a process.

We have been working with experimental clear plastic substrates that can be processed at high temperature [3]. While optical clarity and high glass temperature are the primary requirements for a plastic substrate, it also must have a small coefficient of thermal expansion to prevent fracture of the device structure during processing [4]. Discrete a-Si:H TFT devices have been made at temperatures in excess of 250 °C [3] on clear plastic, but complete matrices are more challenging because they require larger areas that are free of cracks. The current direction of development of optically clear flexible TFT backplanes is to fabricate active matrices at increasing process temperature, while continually adjusting parameters for deposition and device fabrication to allow for crack-free layers. Here we report an a-Si:H TFT backplane deposited on clear plastic at 200 °C and its use to drive an electrophoretic (EP) display. EP displays have been made on flexible stainless steel [5] and plastic substrates [6] and have been driven with a-Si:H [5], polysilicon [7], and organic [8] TFTs. Our active-matrix EP display demonstrates that a-Si:H TFT backplanes made on clear plastic foil can be laminated with EP frontplanes to form functional displays. Fig. 1 shows a completed sample prior to EP lamination.

Because the experimental clear plastic substrate had a glass temperature of > 250 °C and a coefficient of thermal expansion (CTE) of ∼ 5 ppm/°C, it easily allowed depositing the a-Si:H TFT stack at 200 °C, which is our present standard temperature for the fabrication of active matrices. The clear substrate foils were 75 μm thick and had an optical transmittance of

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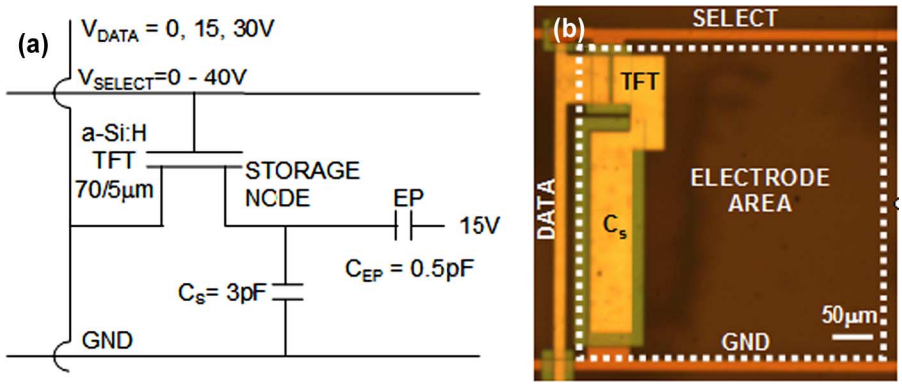

Fig. 2. (a) Circuit schematic of a pixel with data and select line voltages labeled. (b) Optical micrograph of a pixel, with the electrode area designated by a dashed square.

$>$ 84% over the visible spectrum. To test the functionality of the TFT backplane we used the electrophoretic display technology standard, employed at the Flexible Display Center. Electrophoretic display frontplanes [9] were laminated onto the backplanes, which consisted of 8 $\times$ 8 and 32 $\times$ 32 arrays with 500 μm $\times$ 500 μm pixels allowing for 50 dpi monochrome displays. The EP is a sheet of microcapsules, which contain negatively charged white particles and positively charged black particles suspended in a clear fluid. The top contact to the EP is an indium tin oxide (ITO) transparent conductor. By applying $+15$ V to the EP with respect to the bottom electrode produces "white," and -15 V produces "black." A voltage of 0 V is used as a hold. Each pixel consisted of one a-Si:H TFT with $W/L = 70\ \mu\text{m}/5\ \mu\text{m}$ and a 3-pF storage capacitor (C_s), as shown in Fig. 2(a).

II. Experiments

The a-Si:H TFT backplanes were fabricated at 200 °C on free-standing substrates using a radio frequency (13.56 MHz) plasma-enhanced chemical vapor deposition (PE-CVD) process for inverted-staggered back-channel etch TFTs [3]. Source and drain overlaps where made 20 μm to ensure sufficient feature alignment in case the substrate changed size during processing [10]. The masks contained special alignment marks to monitor substrate size after each process step. All Si containing layers were deposited at 500 mTorr. The clear plastic substrate was first coated with 200 nm SiN_x on both sides from $\text{SiH}_4:\text{NH}_3 = 1:9$ using a plasma power density of 55 mW/cm^2 at 200 °C. This layer protects the substrate from process chemicals and formed an adhesion layer for the gate metal lines. Next, tri-layer metal gate lines consisting of 20-nm Cr, 50-nm Al, and 20-nm Cr were deposited by thermal evaporation. They were patterned using photolithography and Cr-7 wet chemical etch for Cr, and a mixture of water, phosphoric, acetic, and nitric acids in the ratio $\text{H}_3\text{PO}_4 : \text{H}_2\text{O} : \text{HNO}_3 : \text{CH}_3\text{CO}_2\text{H} = 16:2:1:1$ for Al. The bottom Cr serves for adhesion to the SiN_x, Al for its conductivity and ductility, and the Cr cap to prevent Al diffusion into the gate dielectric. Next, the a-Si:H TFT stack was deposited: 300 nm SiN_x gate dielectric from $\text{SiH}_4 : \text{NH}_3 = 1:9$, 200 nm i a-Si:H channel layer from SiH_4, and 50 nm n^+ a-Si:H source-drain contacts from $\text{SiH}_4:\text{H}_2:\text{PH}_3 = 730:100:1$. The a-Si:H islands and gate vias were then patterned by reactive ion etching (RIE) at 100 mTorr and power density of 140 mW/cm^2, with $\text{SF}_6:\text{CCl}_2\text{F}_2 = 6:2$ for the a-Si:H, and $\text{CF}_4:\text{O}_2 = 7:1$ for the gate vias. Next, 300 nm Al was deposited by thermal evaporation and patterned to form the source-drain and interconnects, completing the a-Si:H TFTs.

After TFT characterization a 200-nm layer of SiN_x was deposited from $\text{SiH}_4:\text{NH}_3 = 1:9$ at 200°C to passivate the backplane. Vias were then etched using $\text{CF}_4:\text{O}_2 = 7:1$ at 100 mTorr and 100 nm Al was sputtered to serve as an electrode layer to the bottom of the EP film. After patterning this electrode into pixels, an E-Ink electrophoretic foil [9] was laminated onto the backplane to complete the display. Fig. 2(b) shows an optical micrograph of a completed pixel.

III. Results

At the end of the TFT process, marks positioned at the corners of a 1.7 cm $\times$ 1.6 cm rectangle were aligned within the resolution of the optical microscope of $\sim 1\ \mu$m. This observation suggests that the plastic substrate did not deform substantially during the TFT fabrication. Most of the misalignment is due to the CTE mismatch between the substrate and the SiN_x gate dielectric [10]. The differences in CTE between the a-Si and SiN_x are negligible since they are both between 2–3 ppm/°C.

Characterization of the TFTs and pixel circuits was performed using an HP4155A parameter analyzer. The TFTs were measured within the pixels by contacting the storage node at C_s and the external leads, to ascertain that the interconnects were operating properly. The transfer characteristic for an a-Si:H TFT is shown in Fig. 3(a) for drain-to-source voltages (V_DS) of 100 mV and 10 V. The TFTs had $\text{V}_\text{T} = 4$ V, saturation electron mobility $\mu_\text{sat} = 0.5\ \text{cm}^2/\text{V}\cdot\text{s}$, sub-threshold slope $\text{S} = 500$ mV/dec, ON-OFF current ratio $\text{I}_\text{ON}/\text{I}_\text{OFF} > 1\times10^6$, and OFF currents between 1 pA and 10 pA. The output characteristic for gate-to-source voltages (V_GS) from 0 to 25 V in 5 V steps is plotted in Fig. 3(b).

The principal motivation for fabricating a-Si:H TFT backplanes on clear plastic at high deposition temperatures is to increase the TFT stability under gate bias. The stability of the a-Si:H TFTs under constant gate bias stress was measured at room temperature by grounding source and drain, and biasing the gate at fixed voltages ranging from 10 to 40 V. The stress time was 600 s for each gate bias voltage and the tests were performed at room temperature [3], [11]. After each bias step the a-Si:H TFT was evaluated and the threshold voltage was

[1]Cyantek Corporation Inc., Fremont, CA 94539, USA.

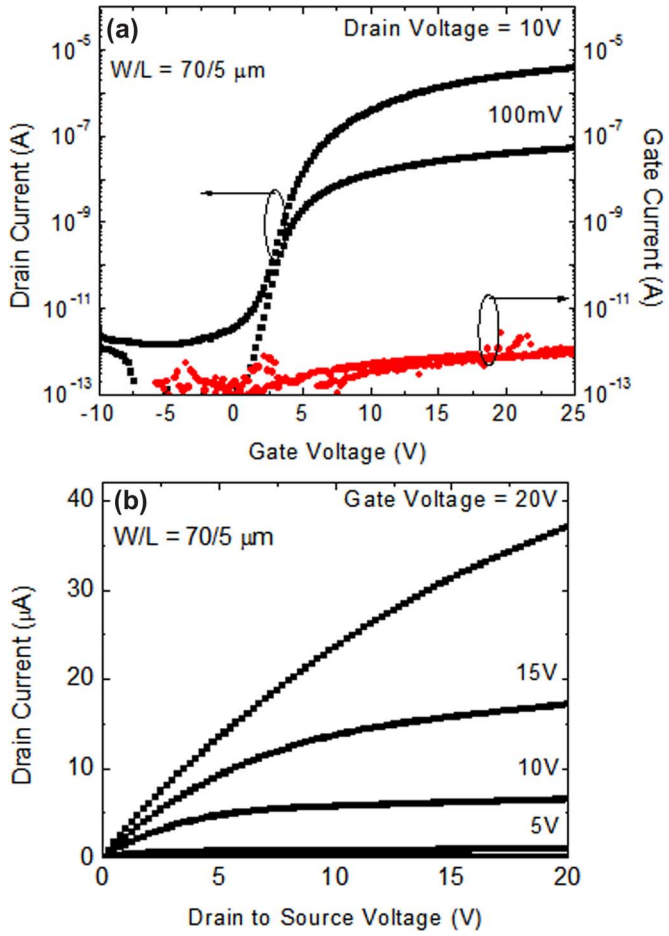

Fig. 3. (a) Transfer characteristic for an a-Si:H TFT for drain to source voltages of 100 mV and 10 V. The gate currents are also plotted. (b) Output characteristic for gate voltages of 0 to 25 V in 5-V steps.

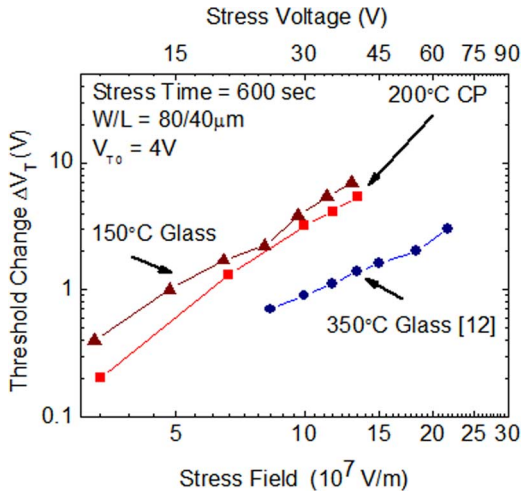

Fig. 4. Change in threshold voltage versus gate stress field. Two sets of data for 150 °C and 350 °C [11] TFTs on glass are given for comparison.

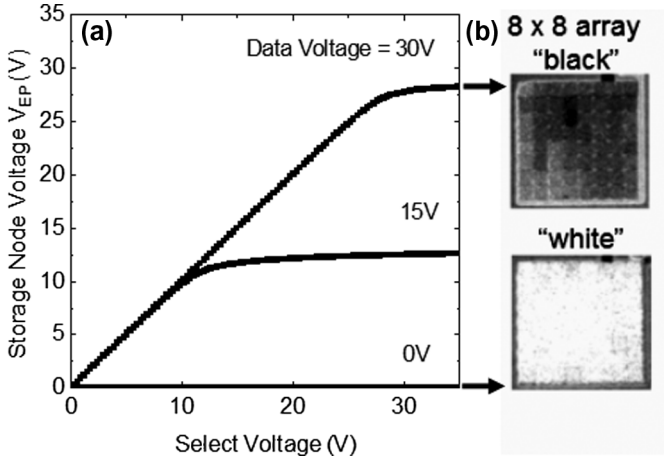

Fig. 5. (a) EP voltage versus select voltage for three data voltages of 0 V, 15, and 30 V. (b) Corresponding optical micrographs of 8 × 8 arrays displaying "white" and "black".

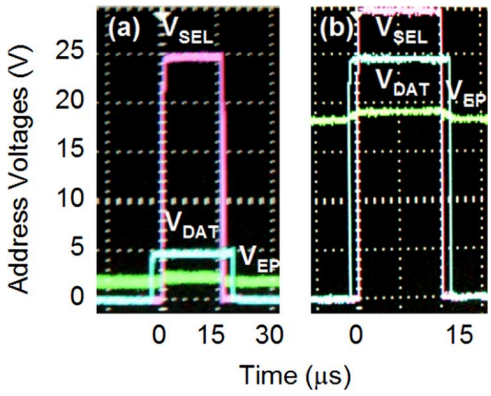

Fig. 6. Transient EP voltage measurement for 16-ms frame time and 26 ms V_{DATA} width for (a) $V_{DATA} = 4$ V and (b) $V_{DATA} = 25$ V.

measured. The changes in threshold voltage (ΔV_T) are plotted versus the applied stress field in Fig. 4. The plot also contains reference data for a-Si:H TFTs on glass deposited at 150 °C by our group, and on glass at 350 °C [11]. It is evident that a-Si:H TFTs made at 200 °C are more stable than those made at 150 °C, and that the deposition temperature should be pushed even higher.

The pixels were characterized before lamination of the EP foil by measuring the storage node voltage at C_s, while sweeping the select line from 0 to 35 V for data voltages 0, 15, and 30 V. Fig. 5 shows the storage node voltage on the aluminum electrode [storage node V_{EP} in Fig. 2(a)] versus select voltage and data voltage prior to EP lamination. The voltage across the EP is 15 V minus the storage node voltage. After EP lamination the select line was swept from 0 to 35 V and the data line was swept from 0 to 30 V. A data voltage of 0 V equals +15 V on the top of the EP (ITO) and displays a "white"; 15-V data biases the EP to 0 V and is used as a "hold"; 30 V biases the EP to −15 V, which displays a "black." A contrast ratio of 1:8 was measured using a luminance meter.

An important characteristic of a TFT backplane is the decay time of the pixel voltage caused by the OFF current of the TFT. Transient measurements were performed on individual pixels to ensure proper active-matrix operation. To avoid the loading of the oscilloscope, an OpAmp buffer was used to measure the storage voltage node in the absence of the EP laminate. Pulse widths for V_{SELECT} and V_{DATA} were 16 and 26 μs, respectively, with a frame time of 16 ms. V_{SELECT} was kept between 25 and 30 V and V_{DATA} was swept from 0 to 30 V. Fig. 6(a) shows V_{EP} for $V_{DATA} = 4$ V and Fig. 6(b) for $V_{DATA} = 25$ V.

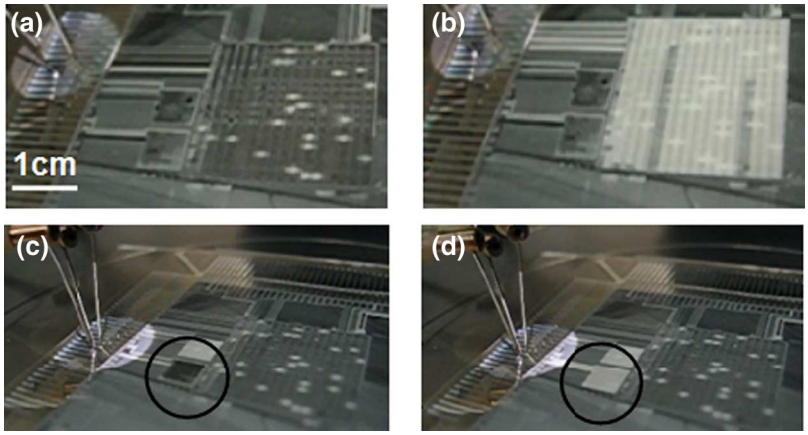

Fig. 7. Photograph of a 32 × 32 display (a) "black" and (b) "white," and an 8 × 8 display (c) "black" and (d) "white."

The pixel circuit maintains the V_{EP} over the 16-ms frame time within 200 mV. This is more than sufficient for an EP display.

The entire 8 × 8 and 32 × 32 arrays were switched on and off to examine yields. Fig. 7(a) and (b) show the 32 × 32 display in "black" and "white", respectively. Some defective pixels are evident. These result from point defects in the substrate, which cause breaks in narrow metal interconnect lines, rather than inadequate lamination. Fig. 7(c) and (d) shows an 8 × 8 display which has no defects.

IV. Conclusion

We fabricated a-Si:H TFT pixel backplanes on clear plastic substrates at a deposition temperature of 200 °C. The TFTs made at 200 °C are more stable under gate bias stress than TFTs made at 150 °C and the substrate was dimensionally stable at this temperature. The backplanes were tested by lamination to electrophoretic frontplanes. Our results highlight the desirability of high process temperature on plastic substrates.

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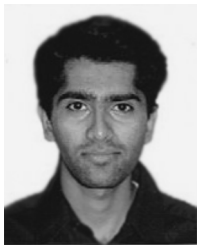

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